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Design of a 41.14–48.11 GHz Triple Frequency Based VCO

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Abstract: Growing deployment of more efficient communication systems serving electric power grids highlights the importance of designing more advanced intelligent electronic devices and communication-enabled measurement units. In this context, phasor measurement units (PMUs) are being widely deployed in power systems. A common block in almost all PMUs is a phase locked oscillator which uses a voltage controlled oscillator (VCO). In this paper, a triple frequency based voltage controlled oscillator is presented with low phase noise and robust start-up. The VCO consists of a detector, a comparator, and triple frequency. A VCO starts-up in class AB, then steadies oscillation in class C with low current oscillation. The frequency of the VCO, which is from 13.17 GHz to 16.03 GHz, shows that the frequency is tripling to 41.14–48.11 GHz. Therefore, its application is not limited to PMUs. This work has been simulated in a standard 0.18 μm CMOS process. The simulated VCO achieves a phase noise of -99.47 dBc/Hz at 1 MHz offset and -121.8 dBc/Hz at 10 MHz offset from the 48.11 GHz carrier.

Keywords: CMOS; phase noise; phasor measurement unit; power; triple frequency; VCO

1. Introduction

Recently, there has been an increased demand in radio frequency design [1–3]. One of the most important blocks in transceiver communication systems are the voltage controlled oscillators (VCOs) [4–9]. Voltage controlled oscillators are the circuits which are used to generate alternative signals in many parts of the radio frequency systems. In power systems, operators need to communicate with each other in different locations. Therefore, data exchange and communication among people and assets require wireless transceiver communication devices. Radios are widely utilized in power systems to make connections among actors, especially system operators such as a phasor measurement unit (PMU) [10]. A block diagram of the basic PMU is demonstrated in Figure 1. PMUs are used to estimate the magnitude and phase angle of an electrical phasor quantity, like voltage or current, in the electricity grid. As shown in Figure 1, one of the main components of a PMU is the phase locked oscillator which uses voltage controlled oscillators [11,12]. Therefore, in order to design a wireless transceiver system and also make a bridge between actors including operators and assets in the electrical industry, designing voltage controlled oscillators with high performance is needed.

The most popular structure of a VCO which is more used in CMOS technology is as follows: ring oscillators and LC tank based oscillators [13]. The most important characteristics of each VCO are phase noise, consumption power, and wide frequency tuning range [14–16]. In VCOs, there is a special trade-off between them. It has been proven that the phase noise of LC VCOs is much better than phase

noise of the loop VCO. But LC VCOs are worse than loop VCOs in terms of area and sometimes power consumption [17]. LC VCOs are usually great choices for RF applications because of desirable and rough start-up conditions and appropriate phase noise [18].

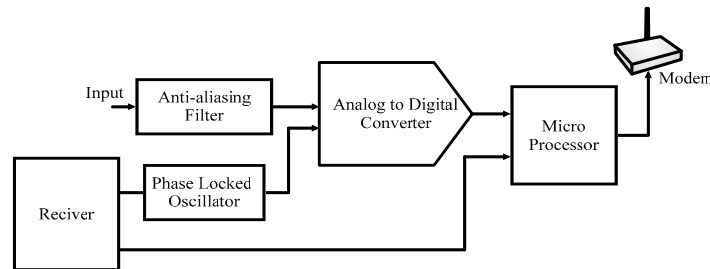


Figure 1. Block diagram of the basic phasor measurement unit (PMU) [10].

Among different LC tank VCOs, Colpitts and cross-coupled structures are utilized more [19]. The cross-coupled VCO has a simple start-up condition and good phase noise, and the type of Colpitts has low consumption power [20,21]. Concurrent utilization of two types of the voltage controlled oscillator, Colpitts and cross-coupled in circuit structure, improves start-up conditions and the phase noise of the circuit with low power consumption.

In recent years, there have been a lot of investigations to achieve low phase noise along with low consumption power in RF applications [22–26]. For example, in [22], in order to obtain low phase noise with low consumption power, two LC oscillators are coupled together.

In this paper, we present a VCO designed using triple frequency, a detector, and a comparator for increasing the frequency and obtaining low consumption power with low phase noise and a robust start-up condition. In this VCO, the trade-off between frequency and phase noise in the low-frequency range is better than in the high-frequency range. Therefore, in this paper, firstly, the trade-off between phase noise and oscillator frequency is performed in low frequency, and then the operation frequency is increased using a triple frequency. This results in achieving low phase noise and low consumption power in the desired frequency.

In the design of a VCO, a combination of cross-coupled oscillators and Colpitts is considered to gain the benefits of both structures. Simultaneous utilization of these two types of voltage controlled oscillators in the structure of the circuit improve the start-up condition and phase noise of the circuit with low consumption power. The proposed VCO is started in class AB, and it will be in class C that the VCO has a better start-up condition with low power consumption.

The structure of this paper is formed as follows: First, the general block diagram of the proposed circuit is introduced in Section 2, then different elements of the circuit are briefly described. In Section 3, simulation results are compared with other existing proposals of this circuit. The paper is concluded in Section 4 with some remarks.

2. Circuit Design

The block diagram of the proposed voltage controlled oscillator with triple frequency is represented in Figure 2. The second harmonic of the oscillator is a result of the common node of a differential pair. The mix of frequency f_0 and second harmonic ($2f_0$) creates a frequency equal to $2f_0 + f_0$ at the mixer output, which makes frequency $3f_0$ if the mixer output frequency is filtered. The VCO is initially oscillating in class AB, and then it keeps the oscillation in class C. The output magnitude of the oscillator is passed to a comparator by a detector circuit, and it generates a gate voltage for the oscillator.

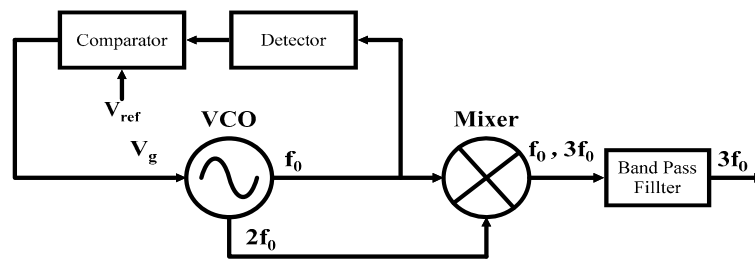


Figure 2. Block diagram of the proposed voltage controlled oscillator (VCO) with triple frequency.

2.1. Voltage Controlled Oscillator

The proposed voltage controlled oscillator is illustrated in Figure 3. This VCO concurrently uses both cross-coupled and Colpitts structures. As shown in Figure 3, Colpitts structure is used in the upper part of the circuit, while the cross-coupled structure is designed for the lower part of the circuit. In order to change frequency, tunable capacitors are used between the two structures of cross-coupled and Colpitts. The voltage is fed into the bulk of M_3 and M_4 transistors to improve consumption power.

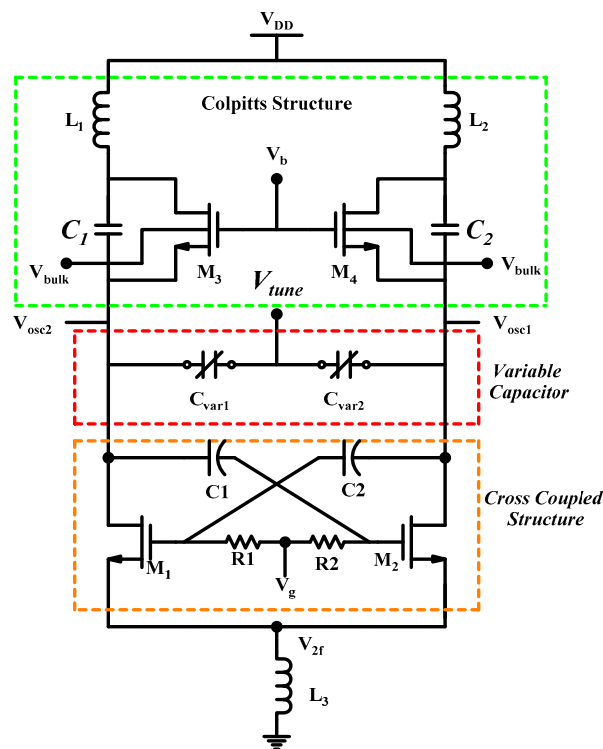


Figure 3. Proposed voltage controlled oscillator with combination of the Colpitts and cross-coupled structures.

In the proposed VCO, in order to achieve a robust start-up condition with appropriate phase noise, the VCO first oscillates in class AB, and then it continues oscillating in class C. To have strong initial conditions, transistor transconductance should initially be multiple times higher than oscillation transconductance. Therefore, the gate voltage supply of cross-coupled transistors should be different in class C and class AB. This is done by feedback including a detector and comparator.

As shown in Figure 3, the threshold voltage of the transistors $M_{3,4}$ and $M_{1,2}$ are not equal. The threshold voltage of the transistors $M_{3,4}$ is reduced by applying a voltage to the body for improving start-up conditions. It should be noted that although threshold voltages of the transistors are different,

drain currents of the transistors $M_{3,4}$ and $M_{1,2}$ are equal. According to Equation (1), this is because the value of $V_{GS} - V_{th}$ must be the same in the transistors to generate an equal amount of the current [27,28].

$$I_D = \frac{1}{2(1 + \theta V_{ds})} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \tag{1}$$

where I_D , μ_n , C_{ox} , W , L , V_{gs} , and V_{th} are drain current of the transistor, electrons mobility, oxide capacitor, transistor width, transistor length, gate-source voltage, and threshold voltage of the transistor, respectively. Moreover, θ is $1/(E_c \times L)$ that E_c is critical electrical field at which velocity saturation occurs.

2.1.1. Oscillation Frequency

Since the transistors used in Figure 3 are biased in the saturation zone, the amount of gate-source and gate-drain capacitors are obtained based on Equation (2) [28,29]:

$$C_{gn} = \frac{\partial Q_g}{\partial V_n} \tag{2}$$

where n is the transistor terminal. Q_g is charge associated with the gate terminal. The gate charge is as follow [28]

$$Q_g = -Q_{sub0} + W_{active} L_{active} C_{ox} \left[V_{gt} - \frac{V_{ds}}{2} + \frac{A_b V_{ds}^2}{12(V_{gt} - \frac{A_b}{2} V_{ds})} \right] \tag{3}$$

where W_{active} and L_{active} are the effective length and width of the intrinsic device, respectively. Also, Q_{sub0} is the substrate charge at zero source-drain bias. V_{ds} and A_b are the drain-source voltage and bulk charge effect, respectively.

The cross-coupled structure in the lower part of the circuit is affecting oscillation frequency and oscillator status due to the producing parasitic capacitors. The equivalent capacitor from cross-coupled can be calculated using Equation (4) [29]:

$$C_{cross} = C_{GS} + 4C_{GD} \tag{4}$$

where C_{GS} and C_{GD} capacitors represent gate-source and gate-drain capacitance of the cross-coupled transistors, respectively. To calculate oscillation frequency, the equivalent half-circuit of the proposed VCO is formed as Figure 4.

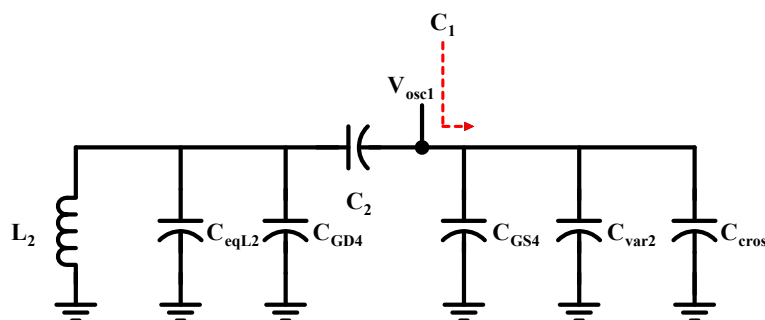


Figure 4. Half-circuit of the proposed voltage controlled oscillator.

In Figure 4, C_{cross} is the equivalent capacitance from the cross-coupled; C_{eqL2} represents equivalent capacitance of inductor L_2 , C_{var2} refers to variant capacitance, and C_{GS2} and C_{GD2} are gate-source and gate-drain capacitance of the transistors M_2 , respectively. C_2 is a constant capacitance of

the Colpitts oscillator. Oscillation frequency can be calculated based on Equation (5) using total observed capacitance:

$$f_0 = \frac{1}{2\pi \sqrt{L_{total} C_{total}}} \tag{5}$$

where C_{total} and L_{total} are the total capacitor and inductor that are obtained in Equations (6) and (7):

$$C_{total} = C_1 + \frac{C_2}{1 - \omega_0^2 L (C_2 + C_a)} \tag{6}$$

$$L_{total} = \frac{1 - \omega_0^2 L (C_2 + C_a)}{C_2 C_a L \omega_0^4} \tag{7}$$

where C_a and C_1 are defined in Equations (8) and (9):

$$C_a = C_{eqL2} + C_{GD4} \tag{8}$$

$$C_1 = C_{GS4} + C_{var2} + C_{cross} \tag{9}$$

2.1.2. Phase Noise

To determine the phase noise around the carrier frequency, all noise sources must be identified in the VCO circuit. The phase noise of the oscillator in the fundamental frequency at offset frequency is defined as Equation (10) [29,30].

$$L(\Delta\omega) = 10 \log \left(\frac{\sum_i N_{L,i}}{2\Delta\omega_0^2 C_{total}^2 A_T^2} \right) \tag{10}$$

where C_{total} and $N_{L,i}$ are the total capacitor and the noise source. A_T is the amplitude oscillation that is defined as:

$$A_T = \frac{4}{\pi^2} R_{pout}^2 I_{\omega_0}^2 \tag{11}$$

where R_{pout} and I_{ω_0} are the output resistance and the fundamental current, respectively. The noise of the L_2 and L_3 inductor is achieved in Equations (12) and (13), respectively.

$$N_{L,Rp} = \frac{4K_B T}{R_{pL_1}} \tag{12}$$

$$N_{L,Rp} = \frac{4K_B T}{R_{pL_3}} \tag{13}$$

where K_B and T are the Boltzmann constant and temperature. R_{pL_1} and R_{pL_2} are the parasitic resistance of the L_1 and L_2 , respectively. The thermal noise of the transistor M_2 and M_4 is as follows:

$$N_{L,nMOS} = 4K_B T \gamma_n g_{m_2} \tag{14}$$

$$N_{L,nMOS} = 4K_B T \gamma_n g_{m_4} \tag{15}$$

where γ_n is the constant and equal amount of the temperature noise of the transistors to its transconductance. g_m is the transconductance of the $M_{2,4}$. With substitute Equations (11)–(15) into Equation (10), the phase noise is defined as follows:

$$L(\Delta\omega) = 10 \log \left[\frac{\pi^2 K_B T}{2\Delta\omega_0^2 C_{total}^2 R_{pout}^2 I_{\omega_0}^2} \left(\frac{1}{R_{pL_1}} + \frac{1}{R_{pL_3}} + \gamma_n (g_{m_2} + g_{m_4}) \right) \right] \tag{16}$$

As shown in Equation (8), the phase noise depends on temperature, fundamental current, offset frequency, and tank quality factor. For example, increasing the current would improve the phase noise situation, but consumption power would increase at the same time. Increasing offset frequency results in lower phase noise. According to this equation, there is a trade-off between selecting the appropriate current to obtain low consumption power, low phase noise, and robust start-up conditions. To satisfy these requirements, the voltage controlled oscillator first works with voltage 1 V, and then it continues operating with voltage 0.65 V to consume lower power. Figure 5 depicts variations of the gate voltage.

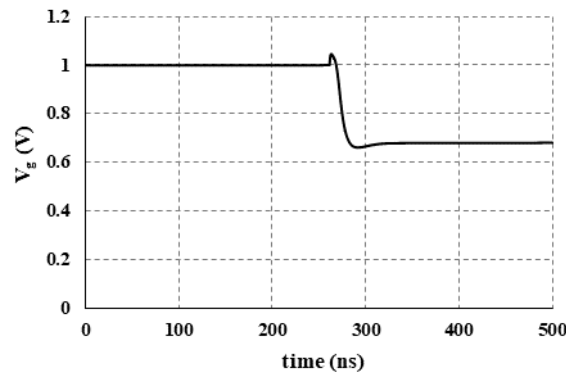


Figure 5. Variations of the gate voltage versus time in the proposed voltage controlled oscillator (VCO).

2.2. Amplitude Detector and Comparator

Figure 6 shows the detector and comparator circuit. Initially, when a VCO is not oscillating, the output voltage of the detector is zero, and the output voltage of the comparator is equal to 1 V. As soon as all conditions of oscillation are met, the oscillator starts oscillating. When transistors M_1 and M_2 turn on, the output voltage of detector increases, which reduces the output voltage of the comparator to the desired level of 0.64 V. In order to make a VCO work in class C, the maximum gate voltage of each transistor should not exceed more than a threshold voltage, with respect to the minimum drain voltage. In order to keep transistors in the operation zone, we can use Equation (17) to obtain the required voltage to make VCO oscillate in class C [29]:

$$V_g \leq V_{dd} - \frac{3V_p}{2} + V_{th} \tag{17}$$

where V_{dd} is the supply voltage and its value is equal to 1 V. Also, V_p represents the variation of drain voltage and is equal to 0.59 V. Therefore, gate voltage should be 0.64 V according to Equation (17).

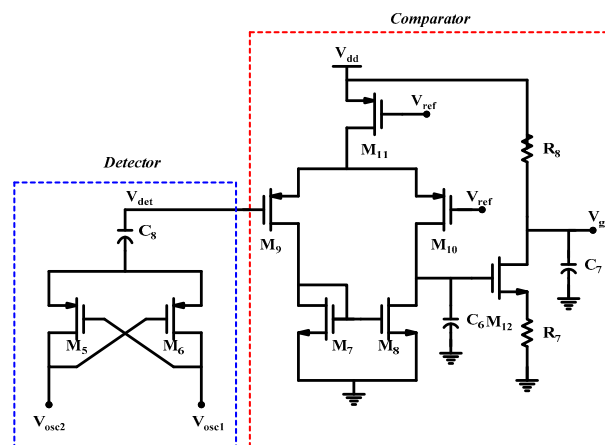


Figure 6. Circuit of the detector and comparator in the voltage controlled oscillator.

The main elements of the comparator include five transistors (i.e., M_7 to M_{12}) along with one transistor as the buffer. Initially, the output of the detectors is zero, and the comparator output is equal to 1 V. Thus, a big voltage is applied to the gate of the transistors M_1 and M_2 in the proposed VCO circuit. This big voltage produces a high current according to Equation (1). This current creates strong initialization conditions for the oscillator.

2.3. Designing Mixer

In order to triple frequency, a nonlinear differential amplifier is used. Figure 7 shows the mixer used in the triple frequency [28]. This mixer contains an RF switch (transistor M_{13}), differential pair switch intermediate frequency (IF) (M_{14} and M_{15}), and an inductor (L_4) which is in resonance with loss capacitors like a band-pass filter.

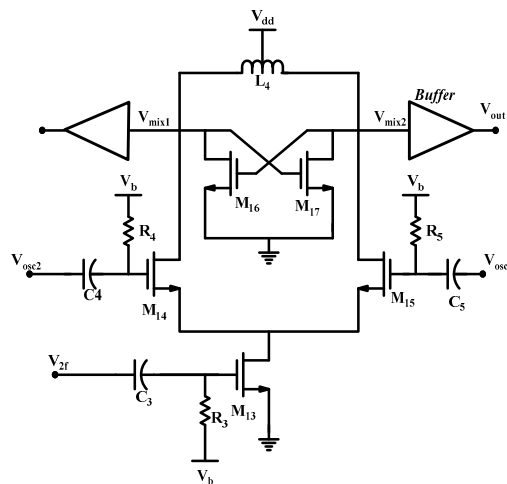


Figure 7. Circuit of the triple frequency.

3. Results

In this paper, we designed and simulated a VCO with low phase noise, low consumption power, and robust start-up conditions using technology $0.18 \mu\text{m}$ CMOS. The oscillation frequency versus the voltage V_{tune} is demonstrated in Figure 8. The oscillation frequency of a VCO is from 13.17 GHz to 16.03 GHz, and the triple frequency covers a range frequency between 41.14 GHz and 48.11 GHz. The phase noise of a VCO at 48.11 GHz is shown in Figure 9; where at offset frequencies of 1 MHz and 10 MHz, the phase noise of -99.47 dBc/Hz and -128.8 dBc/Hz is achieved, respectively. The output power spectrum for the frequency 48.11 GHz is depicted in Figure 10. Correlation of the simulated phase noise versus the oscillation frequency at 1 MHz offset frequency is shown in Figure 11. The phase noise changed from -91.43 dBc/Hz to -98.46 dBc/Hz with respect to the variation frequency. The oscillation frequency and phase noise by Monte Carlo for 50 samples are illustrated in Figure 12a,b.

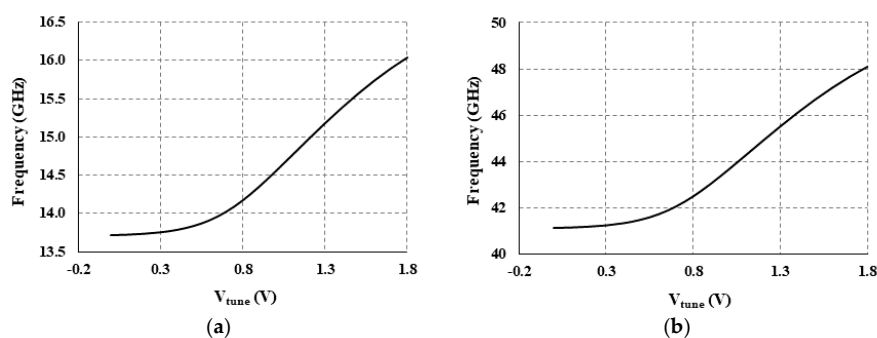


Figure 8. Simulated VCO tuning range (a) output of the VCO; (b) output of the triple.

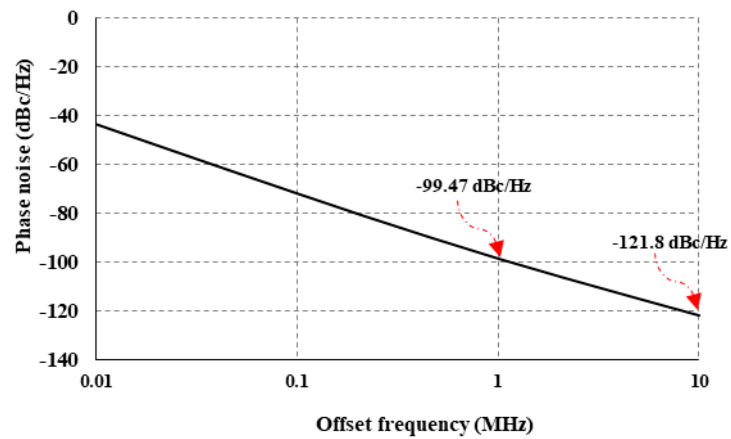


Figure 9. The simulated phase noise of the VCO at 48.11 GHz.

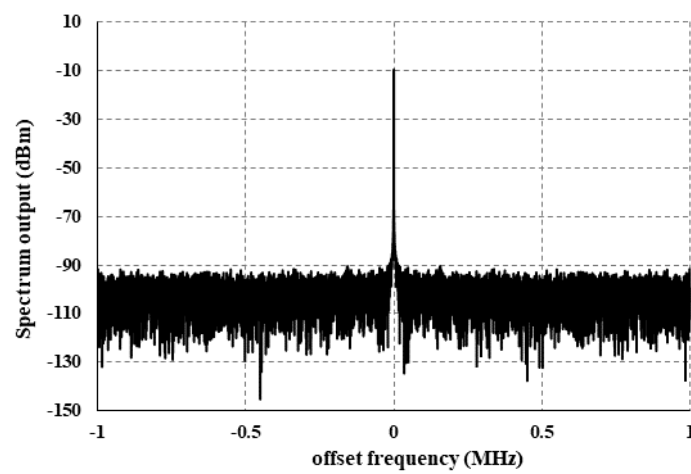


Figure 10. The simulated output power of the VCO at 48.11 GHz.

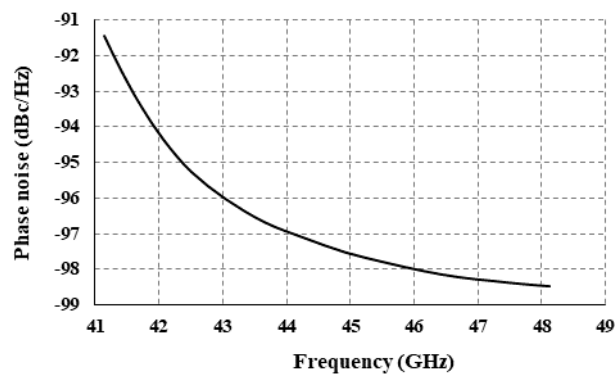


Figure 11. The simulated phase noise and frequency versus the oscillation frequency at 1 MHz offset frequency.

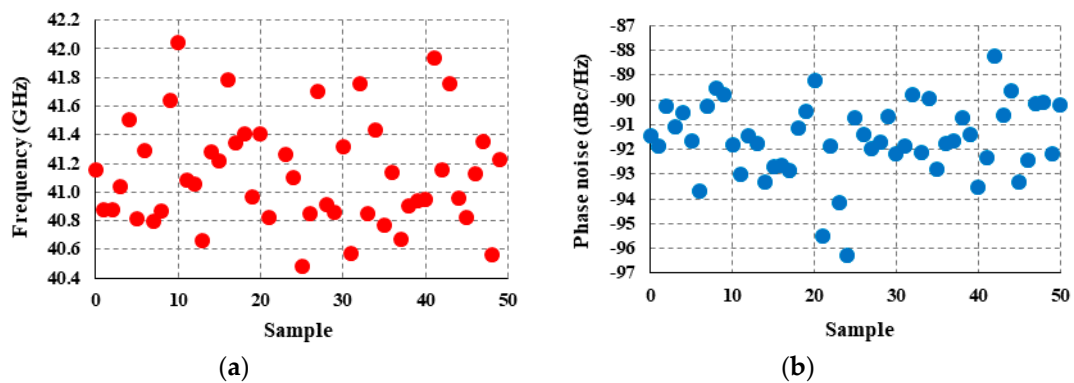


Figure 12. The Monte Carlo of the (a) oscillation frequency; (b) phase noise.

Table 1 summarizes the phase noise results of the designed VCO in different corners process and normal condition. In the typical-typical (TT) condition, the phase noise of -99.47 dBc/Hz is obtained at 1 MHz offset frequency of 48.11 GHz. In corners slow-slow (SS) and fast-fast (FF), the frequencies 48.12 GHz with phase noise of -97.49 dBc/Hz and 47.66 GHz with phase noise of -94.41 dBc/Hz are obtained in offset frequency of 1 MHz, respectively.

Table 1. Simulation of the proposed voltage controlled oscillator (VCO) in different corners.

Corners	Phase Noise (1 MHz)	Phase Noise (10 MHz)
Typical-typical (TT)	-99.47	-121.8
Fast-fast (FF)	-94.41	-119.57
Slow-slow (SS)	-97.49	-120.61

Table 2 compares the performance of VCOs with other works in terms of the fundamental frequency phase noise, consumption power, and figure of merit. The figure of merit (FOM) and total figure of merit (FOM_T) for evaluating VCO performance is defined in Equations (18) and (19) [5,15]. Based on this table, our designed VCO has lower phase noise with better consumption power and figure of merit compared with previous works.

$$FOM = L(\Delta\omega) - 20 \log\left(\frac{f_0}{\Delta f}\right) + 10 \log\left(\frac{P_{DC}}{1mw}\right) \tag{18}$$

$$FOM_T = L(\Delta\omega) - 20 \log\left(\frac{f_0}{\Delta f}\right) + 10 \log\left(\frac{P_{DC}}{1mw}\right) - 20 \log\left(\frac{FTR}{10\%}\right) \tag{19}$$

where $L(\Delta\omega)$, f_0 , P_{DC} , and FTR are phase noise, oscillation frequency, consumption power, and frequency tuning range, respectively.

Table 2. Comparison of the proposed VCO with other works.

Ref.	[3] ²	[9] ¹	[16] ²	[25] ²	[26] ²	This Work ¹
Process	56 nm SOI ⁵	0.13 μ m CMOS	65 nm CMOS	40 nm CMOS	65 nm CMOS	0.18 μ m CMOS
Frequency (GHz)	18.57	25.5	54	55.45	46.8	44.62
Tuning range (%)	5.38	43	9.1	25.4	5.8	15.6
Phase noise at offset frequency (dBc/Hz)	-117.6 at 5 MHz	-96 at 1 MHz	-95.5 at 1 MHz	-100.1 at 1 MHz	-100 at 1 MHz	-99.47 at 1 MHz
P_{DC} (mW)	2.56	12	24	22	5	14 ⁴ 4.16 ³
Figure of merit (FOM) (dBc/Hz)	-185.1	-173.33	-179	-179.8	-186.415	-187.95 ⁴ -193.22 ³
Total figure of merit (FOM_T) (dBc/Hz)	-190.43	-186	-179.8	-187.9	-188.5	-191.81 ⁴ -197.08 ³

¹ Simulation result; ² Measurement result; ³ Including the power consumption of the VCO; ⁴ Including the power consumption of the total structure; ⁵ Silicon on insulator.

4. Conclusions

In this paper, we presented our designed VCO based on triple frequency whose output frequency oscillates in the range of 41.14 GHz to 48.11 GHz. It uses 0.18 μm technology, and it is simulated in ADS (2016.01, Keysight EEsof EDA, California, USA, 2016) software. Because the varactor works well in the low-frequency range, the proposed VCO is designed in low-frequency, then the operation frequency increased using triple frequency. This achieves low phase noise, low consumption power, and high tuning frequency range in high operation frequency. Therefore, better phase noise can be achieved in the desired frequency. Moreover, the combination of both cross-coupled and Colpitts structures with novel circuit for VCOs is presented in this paper. In order to reach a robust start-up condition for VCO, it first runs in class AB, and then, it steadies in class C to be featured with better phase noise and suitable consumption power.

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