A Wide Range and High Swing Charge Pump for Phase Locked Loop in Phasor Measurement Unit

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***Abstract*— Phasor Measurement Units are widely utilized in power systems to provide synchrophasor data for a verity of applications, mainly performed by Energy Management Systems (EMS). Synchrophasors are measured at different parts of the network and transmitted to Phasor Data Concentrator (PDC) at a rate of 30–60 samples per second. The synchronization is done by means of a phase locked oscillator inside PMU which uses clock signal of the Global Positioning System (GPS). In this paper a novel charge pump with an appropriate operation capability in phase-locked-loops is presented. By using this phase locked loop in phase measurement unit, the total performance of this circuit will be improved. The proposed charge pump uses current mirror techniques in order to achieve a wide range of output voltage to control the oscillator and also has a good performance in a wide range of frequency from 33MHz to 555MHz. This circuit is designed and simulated in TSMC 0.18um CMOS technology. The proposed charge pump only consumes 390uW power in supply voltage of 1.8V at 500MHz and has a maximum current of 16.43uA with a acceptable current matching between source and sink currents. It is also capable to be used in a wide frequency range and low power applications.**

Keywords — charge pump, phase locked loop, phasor measurement unit, low power.

I. INTRODUCTION

Phasor Measurement Units (PMUs) play an important role in power system wide area monitoring supporting dynamic operation and control of system. Critical parameters of power system like voltage of nodes, current of lines, load angle, and system frequency should be monitored in real time to avoid system failures in case of fault occurrence [1]. For proper monitoring, synchronized measurement of power system parameters is needed. PMUs provide such synchronized time-stamped data using global positioning system (GPS) clock. The data from PMUs are widely used in frequency control systems [2], state estimation [3], power quality measurement [4], etc. PMU sends the synchro-phasor data to the phasor data concentrator (PDC) through unicast or multicast. A block diagram of key components of a PMU is shown in Fig. 1. Current and voltage transformers (CT and VT) collect current and voltage measurements from the field. These signals are sent to analog to digital converts through an anti-aliasing filter which limits the bandwidth of instantaneous signal based on sampling theorem. The analog to digital converter works according to IEEE C37.118 standard specifications. The digital output will be then converted to phasors by a phasor estimator. The GPS clock uses a crystal oscillator to provide clock pulses. The possible errors between pulses per second and clock frequency is then corrected by a phase locked oscillator. The outcome of the overall system is synchro-phasor data to be communicated to the PDCs [5].

Phase locked oscillator utilizes phase locked loop (PLL). PLL is widely used in integrated circuits like time recovery, frequency multipliers and synthesizers [6], timing extraction from data streams, memories, hard disk drive electronics, clock generation, microprocessors, clock and data recovery, and in phase measurement unit (PMU). A PLL with a desired performance has short settling time, and generates low noise and low spur signals. Based on their applications, PLL can be classified into digital PLLs, programmable PLLs, PLL-based frequency synthesizers, etc. Moreover, according to the type of phase detector used in PLLs, they can be divided into “simple” and “charge pump” PLLs (CPPLL); where the former has simple phase detector, and the latter uses phase frequency detector coupled with charge pump. Looking closely to the structure of CPPLLs, one can find a basic PLL which is extended with a charge pump put between phase detector and loop filter. Charge pump is used to inject and remove current to/from loop filter for integration operation [7]. The challenges during the charge pump design include input and output currents (UP and DN currents), low power consumption, operation frequency range and circuit output voltage range [8].

As mentioned, one of the applications of charge pump circuit is in phase locked loops (PLLs). An analog PLL circuit according to Fig. 2 consists of important blocks of phase frequency detector (PFD), charge pump (CP), loop filter (LF) and voltage-controlled oscillator (VCO) [9], so one of the main difference between phase locked loop and delay locked loop (DLL) is that delay locked loop uses voltage controlled delay line instead of VCO [10-11]. In an analog PLL, a phase frequency detector, receives its inputs from reference input signal and the output of VCO and its output is based on phase difference between its inputs. In fact, this output determines charge pump operation procedure and the output of PFD is transmitted to charge pump circuit as a voltage pulse or current pulse.

Finally, loop filter, integrates charge pump output. In order to obtain the desired frequency of output signal, the voltage control oscillator is regulated by the capacitor voltage. Loop filter, upon triggered to operate, and minimizes the phase difference among phase detector inputs by setting the appropriate control voltage. When frequency difference is small enough, the mechanism of PLL feedback makes the input frequencies of the 2 phase detectors equal. At this time, VCO is actually locked with input frequency. This is a locked state of PLL.

In Fig. 3, structure of a conventional charge pump is depicted. It uses negative OPAMP feedback technique and has good time of switching and perfect current matching. It uses body bias to prevent the current increase [12].

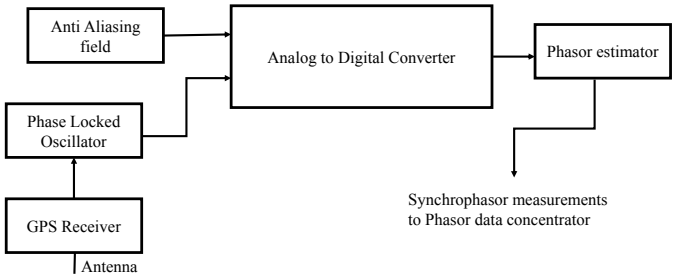


Fig. 1. Block diagram of Phasor Measurement Unit (PMU)

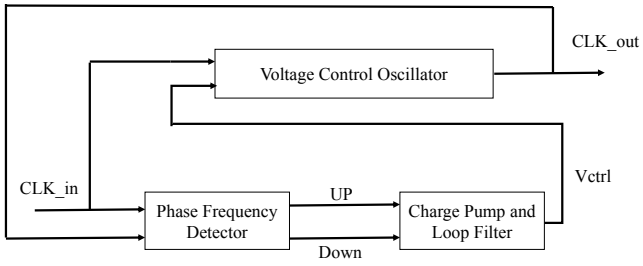


Fig. 2. Block diagram of charge pump based phase locked loop (CPPLL)

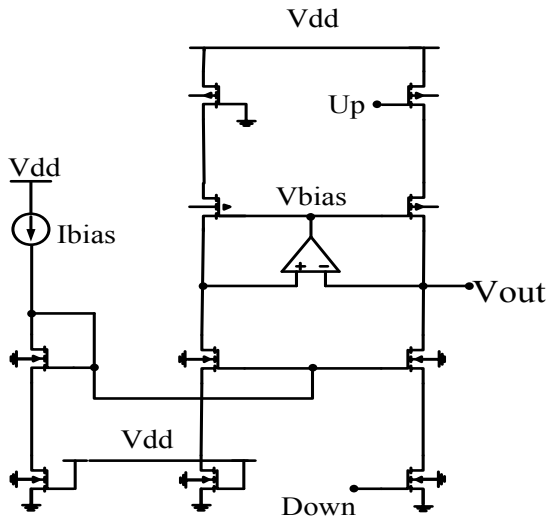


Fig. 3. Structures of a conventional charge pump

The channel length modulation effect is reduced by using negative feedback, but this CP has a high-power consumption and area. To improve these problems, the structure in [13] is presented. This charge pump has a high UP and DOWN currents and the current variation is not very low in all range of output voltage of CP. The other structure which is used as charge pump, and does not this problem, utilizes adaptive body bias to compensation current variation which results to good current matching [14]. This charge pump has low power consumption, but when charge pump needs to be protected from switch noises, this topology may have some concerns. Moreover, this structure has a high UP and DOWN currents. An improvement for this type of charge pump is presented in [15], which uses rail-to-rail input stage and have four current sources, two regulation loops, and three OPAMPs to reduce current mismatch and to use for short-channel devices. But, this CP has high source current and sink current.

The rest of this paper is structured as follow: in section II the proposed charge pump is introduced. In section III the simulation results of the proposed circuit is discussed and at the end in section IV a conclusion is provided.

II. PROPOSED CHARGE PUMP

Charge pump is one of the important blocks in delay locked loops and phase locked loops which aim to control this circuits operation and performance. Structure of the proposed charge pump is shown in Fig. 4.

It consists of a differential amplifier which has NMOS transistors of M3 and M4, and they are placed in the center of this CP. The outputs of this transistors affects in the M8 and M9 and therefore, when Down signal is high, M3 is on and M4 is low, so the current of M6 is injected to the M3. By the current mirror sources consists of M10 and M7 the Down current can affect the loop filter. In fact, with the proper relation between the gate width of the current mirror (M10 and M7), the suitable Down current is produced and discharge the capacitor in loop filter.

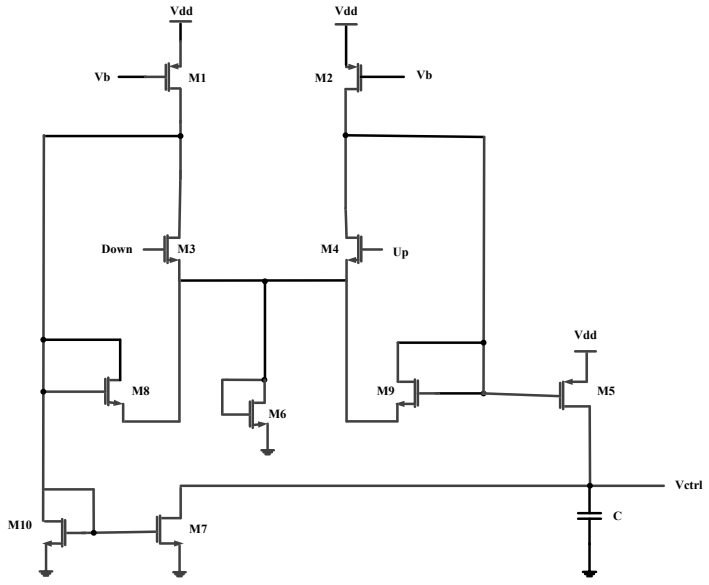
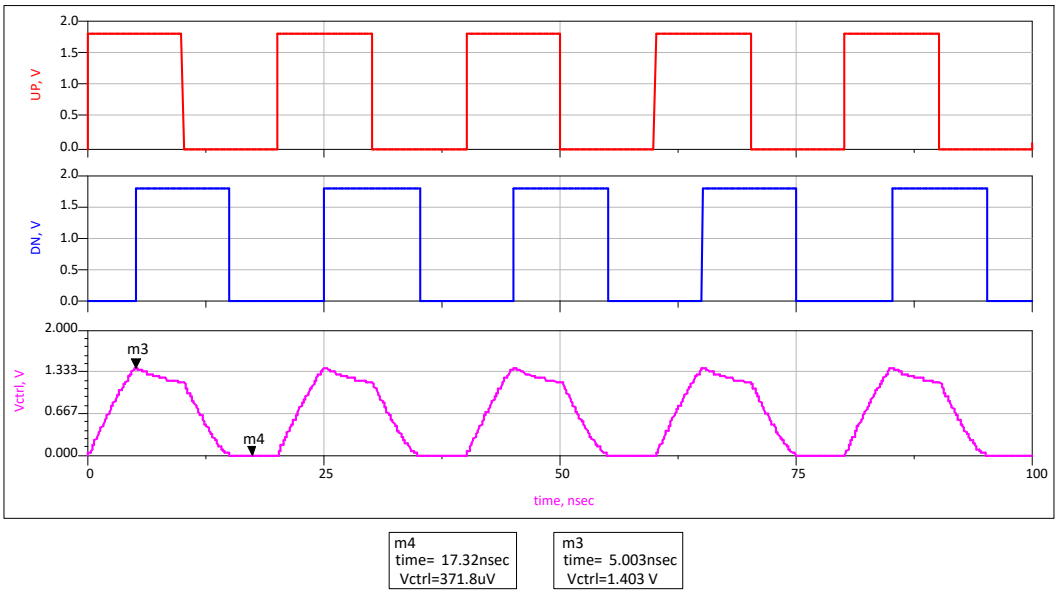
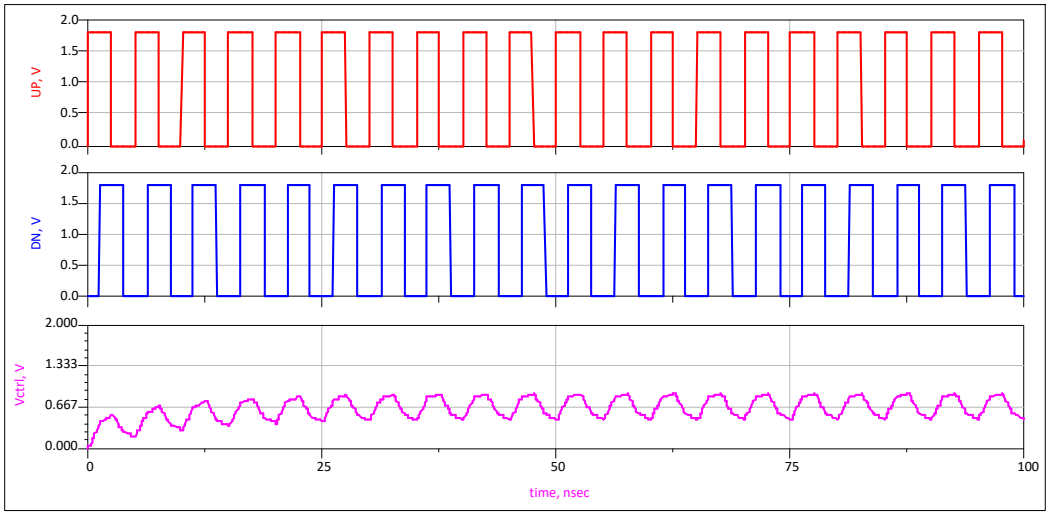


Fig.4. The proposed charge pump



(a)



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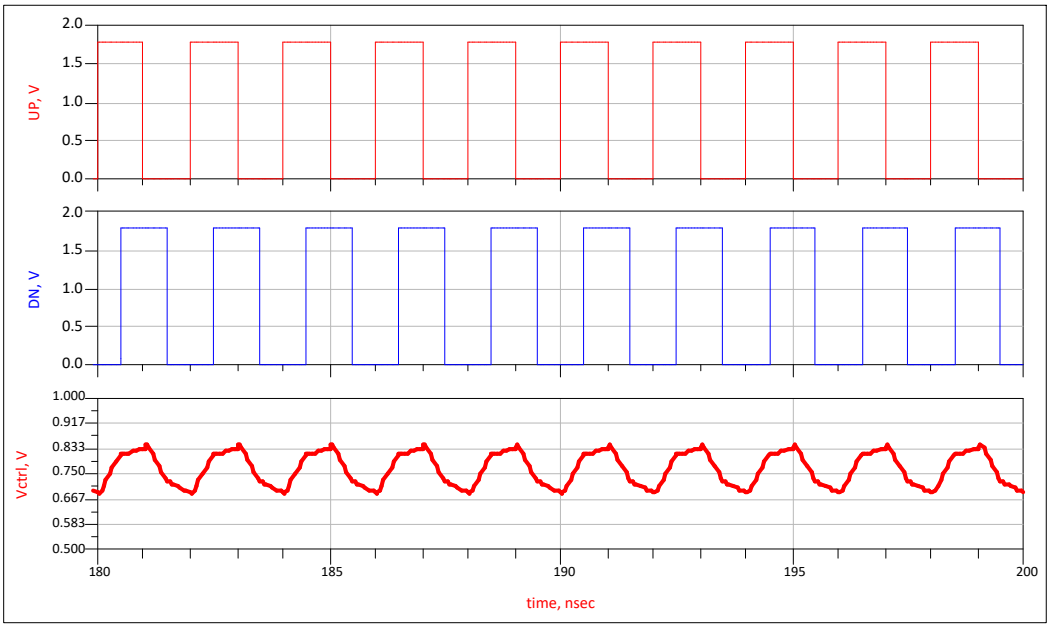


(c)

Fig. 5. UP, DN, and Vctrl (output of charge pump) signals at: a) 50MHz, b) 200MHz, c) 500MHz

Transistors M2 and M1 are biased by a voltage source of 0.8V. On the contrary, when UP signal is high, the current of M6 is injected to the M4, so M4 and M9 will be on and with the transistor of M5 the current will inject to the capacitor. So in this case, the capacitor will charge. This would result in accuracy and also increase of control voltage range. The NMOS differential pair (M3 and M4) which is considered in the center of circuit activates the current mirror sources according to the Up and DOWN input signals. To charge the capacitor of loop filter, the proposed charge pump uses the direction consist of transistors M4, M9 and M5. Considering the correlation between input and output currents to and from loop filter, this is easily observed by using the simulation tool and through DC analyses. In other words, the output current from M5 is equal to the current from M7. Therefore, in this case charge pump carries out charge and discharge operation of output node capacitance with the same speed.

III. SIMULATION AND RESULTS

The proposed charge pump circuit is designed and simulated with TSMC 0.18um CMOS technology. A challenge in increasing the output voltage of charge pumps is the need to increase the value of current source. Since current increase will result in bigger power consumption of the device, the output voltage swing of charge pumps is hence limited. But as it is shown in Fig. 5 (a), in this proposed charge pump at 50 MHz, the result for voltage of charge pump (CP), shows range of 0 V to 1.403V that is appropriate and also the power consumption will be low. Moreover, this voltage range is suitable to control voltage controlled oscillators which operate in a phase locked loop. In Fig. 5 (b and c) the waveform of output control voltage are depicted for frequencies 200MHz and 500MHz. In Fig. 6, Up and Down current curves are shown with respect to control voltage. This charge pump generates a suitable current matching with maximum current of 16.43uA. As shown in Fig.5, when the control voltage (Vctrl) is from 0.8V to 1.4V, the charge pump will have an acceptable current variation. In addition, the proposed circuit consumes 315.8uW power at 50MHz with supply voltage of 1.8V. Also, it can be used in an analog PLL.

In Fig. 7, the amount of up and down currents (I_UP and I_DN) are shown in process, voltage and temperature variations (PVT), when control voltage changes from 0 to Vdd. For example, at fast- fast and slow- slow condition, the maximum currents are 29 uA and 9.3uA, respectively.

As it was discussed earlier, this charge pump has a very good performance in frequency range of 33MHz to 555MHz with a power consumption range of 308uW to 387uW for 33MHz and 555MHz, respectively. Power consumption of this CP in PVT variations is summarized in TABLE I, and in TABLE II a comparison between previous charge pump structures with this proposed structure is provided.

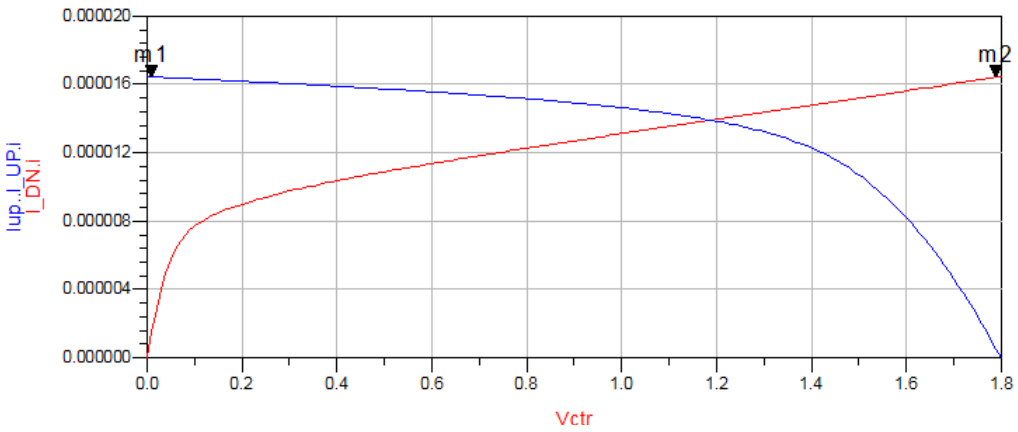
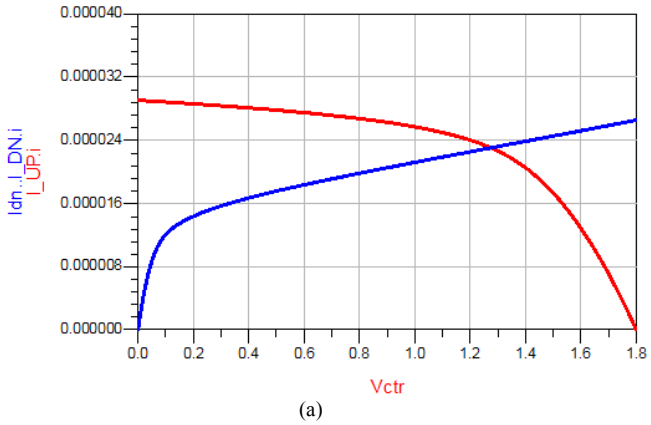
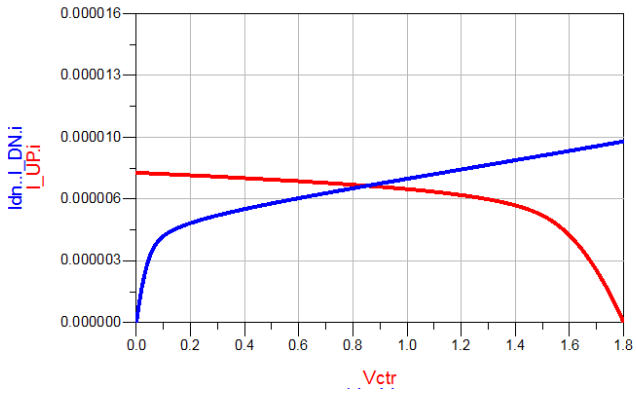


Fig. 6. UP and DN current curves with respect to control voltage (Vctrl)



(a)



(b)

Fig. 7. The amount of Up and DN currents when the voltage control changes from 0 to Vdd for corner cases of, a) Fast Fast, b) Slow Slow

TABLE I. POWER CONSUMPTION OF CHARGE PUMP IN DIFFERENT CORNER CASES AT 200MHZ

Corner case	Power consumption
Typical_ Typical	357.6 µW
Fast_ Fast	511.1 µW
Fast_Slow	346.1 µW
Slow_Fast	159.1 µW
Slow_Slow	169.0 µW

IV. CONCLUSIONS

The proposed circuit in this paper is a charge pump with the capability of being used in the PLL of the oscillator inside PMUs. This charge pump has a wide range of frequency and high voltage swing. The simulation results performed in ADS software and TSMC CMOS 0.18um technology, shows that this circuit only consumes 390 µW power in supply voltage of 1.8V, and has a maximum current of 16.43µA. The proposed charge pump is able to operate in a wide frequency range from 33MHz to 550MHz and generate output control voltage in the range of 0V to 1.403V at 50MHz.

TABLE. II. COMPARISON OF PERFORMANCE OF PROPOSED CHARGE PUMP WITH PREVIOUS WORKS

	[14]	[16]	[17]	[18]	[19]	This work
Process CMOS	0.18um	0.18um	90 nm	0.18um	90 nm	0.18um
Supply voltage	1.2 V	1.8 V	1.2 V	1.8 V	1.2 V	1.8 V
Power consumption	N/A	570 uW	1.4mW @ 500MHz	6.84 mW	404 uW	334.2uW @ 100MHz 357.6 uW @ 200MHz 390 uW @ 500MHz
Current of charge pump	140 uA	100 uA	100 uA	475 uA	N/A	16.43 uA

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