DESIGN OF WIDEBAND SILICON-GERMANIUM RF FRONT END CIRCUITS FOR BROADBAND COMMUNICATIONS SYSTEMS

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By

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DESIGN OF WIDEBAND SILICON-GERMANIUM RF FRONT END CIRCUITS FOR BROADBAND COMMUNICATIONS SYSTEMS

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SUMMARY

This thesis discusses the design of wideband front-end circuits for broadband communications systems, designed in silicon-germanium technology. The bandwidths of these circuits cover from 2 GHz to 18 GHz.

In Chapter 1, an introduction to wideband communications systems is presented. In addition, a brief summary of phased array radars and the need for wideband radars are discussed. Also, an overview of Silicon-Germanium technology and its advantages in the context of wideband circuit design are discussed.

In Chapter 2, the design challenges associated with wideband RF front-end circuits are presented. In particular, the design space of wideband power amplifiers and low-noise amplifiers is discussed. Both the active and passive circuit design difficulties for each circuit are evaluated. In addition, traditional approaches to amplifier design and their drawbacks for wideband circuits are explained.

In Chapter 3, the design of a wideband 1-20 GHz Silicon-Germanium power amplifier is discussed. In this design, a distributed amplifier topology is utilized with transistor stacking to simultaneously achieve high output power and wideband impedance matching. This amplifier is designed in a highly scaled 90 nm SiGe BiCMOS process. Measurement results and a comparison to state-of-the-art wideband power amplifiers are shown. This work, "A 1-20 GHz Distributed, Stacked SiGe Power Amplifier" was published in the 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium [1].

In Chapter 4, the design of a wideband 1-18 GHz Silicon-Germanium low noise amplifier is presented. A resistive feedback topology is used to achieve wideband operation with moderate gain and low noise figure. In addition, a cryogenic characterization of this amplifier is conducted with measurements of S-parameters, 1 dB compression point, and noise over temperature. A comparison to state-of-the-art cryogenic amplifiers is shown. Fur-

thermore, the demonstration and explanation of an on-wafer cryogenic noise measurement scheme are presented. This work, ”A Low Power, Wideband SiGe Low Noise Amplifier for Cryogenic Temperature Operation” will be submitted to the 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS).

In Chapter 5, a summary of the achieved results is shown. In addition, future research directions are discussed.

CHAPTER 1
INTRODUCTION

1.1 Motivation

With the increased development of fully-integrated wireless transmit/receive modules and phased array systems, there has been growing interest in efficient, wideband circuits and systems [2]. Applications of wideband wireless systems include phased-array radar, imagers, and broadband communications. The necessity of efficient wideband RF circuits is emphasized with the move to large element phased-array systems and imagers [3].

Broadband or wideband communication systems typically encompass many of the designated communication bands set by the IEEE. A visual representation of this is shown in Fig.1.1. To estimate the degree of wideband operation, the fractional bandwidth (FBW) provides a metric for comparison. This is defined in equation 1.1 where f_{upper} and f_{lower} represent the upper and lower bounds on the bandwidth.

$$FBW = \frac{f_{upper} - f_{lower}}{\frac{f_{upper}+f_{lower}}{2}} \tag{1.1}$$

For example, X-band (8-12 GHz), has a FBW of 40 %. Whereas, for the wideband system in Fig 1.1, a system operating from 2 GHz to 18 GHz has a FBW of approximately 160 %. There are many advantages to using a system with such a large bandwidth. One major advantage is that it lets the system have high frequency agility, allowing it to switch frequency bands without compromising the gain of the system. In addition, a fully integrated wideband system greatly simplifies the system level design. In particular, it only requires the system designer to control one chip for the full frequency range rather than individual chips for each frequency band of interest. Also, with only a single chip, the cost of a single wideband system can be more affordable than aggregating many narrowband systems. Each of

these advantages allows wideband communication systems to be attractive to system level designers.

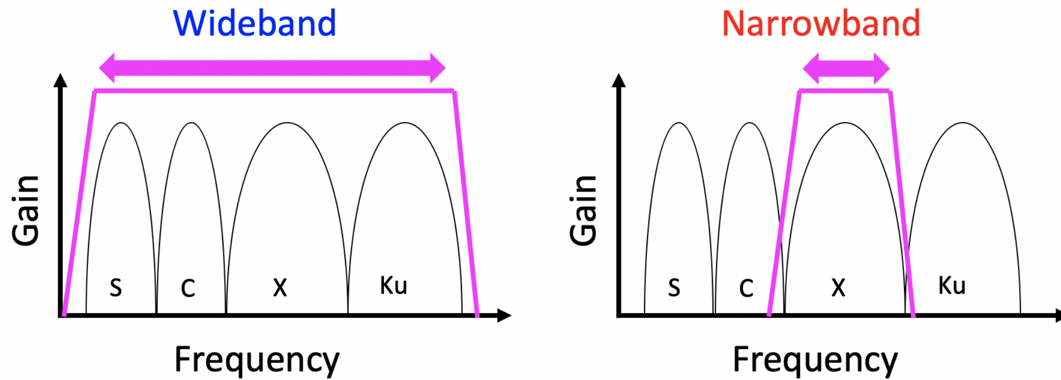

Figure 1.1: Comparison of a Wideband and Narrowband System.

1.2 Broadband Radar Systems

As mentioned previously, there are many applications for wideband systems. However, one of the main applications is for broadband radar systems. In particular, phased array radars have grown in popularity over the last few decades [4]. A phased array operates off of an array of individual element antennas. By changing the spacing between antennas, the mutual coupling between elements can be adjusted. In addition, each element can be driven with a different phase excitation. As a result of optimal mutual coupling and the driven signals at each antenna, a radiated pattern, at some distance from the observation point, from a single element can be constructively combined with a nearby element [5]. This concept can be scaled to a large number of elements. This will increase the directivity of the antenna array system, effectively providing a larger gain.

From this understanding of a phased array system, the required components are an array of antenna elements and a phase shifter for each antenna. This describes a passive phased array system. Two examples of a passive phased array system are shown in Fig. 1.2 and 1.3.

In this system, there is only phase control, and the losses of the components are absorbed into the system design. This requires a high input driving signal. The phase control is typically implemented with an electronic phase shifter. Unfortunately, electronic phase shifters are traditionally lossy structures. With a large number of elements, the overall loss from all of the phase shifters can be very significant [6].

Figure 1.2: An example of a passive phased array system embedded into a plane. [7]

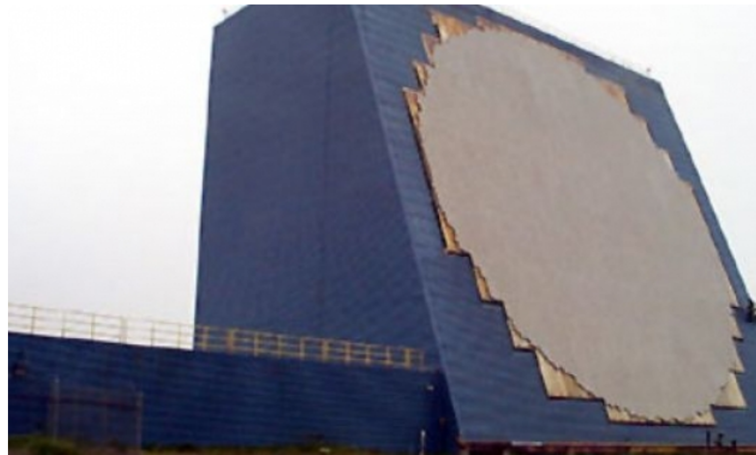

Figure 1.3: Cobra Dane passive phased array radar from Raytheon. [8]

An alternative of the passive phased array system is an active phased array system. In an active phased array system, a front-end transmit/receive module and supporting amplifiers are included in the system. There are a number of advantages to active phased array systems. A clear advantage is that there is some degree of loss compensation of the phase shifter and feeding elements. On the receiver side, the inclusion of a front-end module will

improve the sensitivity of the overall receiver by reducing the noise figure of the overall receive path. On the transmit side, with an amplifier, the power excited into the antenna will also increase [6]. From a system level perspective, this provides a different optimization strategy. In a passive array, the approach is to minimize the loss of the elements and scale the number of elements for the desired radiated power. However, in an active array, the amplifiers can be used to achieve the desired driving signal for the antenna. This can reduce the number of elements for the same radiated power or can be kept the same for a higher radiated power.

In addition, with a front-end module, this provides the system designer with precise control over the amplitude and phase variation in each path. An example of an active phased array system is the PAVE PAWS system shown in Fig 1.4.

Figure 1.4: PAVE PAWS active phased array system. [9]

Another important advantage of both active and passive phased array systems is the beam steering capabilities. With phase shifters, the excitation phase of each element can be tuned to focus the beam along different angles. This property allows the beam to be steered to scan across a larger area. The ability to dynamically steer the beam, electronically, is a

significant advantage. It avoids having to mechanically move the structure, which is very slow compared to electrically steering the beam.

The logical question is to ask, why are broadband phased array systems desirable if the narrowband system by itself provides such flexibility. The answer to this comes down to the detection resolution and frequency. The detection resolution is related to the frequency used in the radar system. For example, in weather radar applications, there are typically many different frequency bands that are used to determine different details of weather patterns [10]. In weather radar, S-band (2-3 GHz), C-band (5-6 GHz), and X-band (8-12 GHz) radars each provide different physical information. This is due to the tradeoff of resolution and distance. For example, at lower frequencies, S-band, weather patterns far away can be observed that would not be able to be resolved at X-band. Conversely, at X-band, a high detection resolution can provide more detail on weather patterns at a close distance compared to S-band systems. One limitation of distance on high-frequency radars is the amount of path loss, including weather absorption, incurred at the frequencies increase. This will limit the usable distance by the detectable reflected signal. These tradeoffs of detection resolution and distance apply to phased array systems in general.

Rather than having multiple narrowband radars that each provide different range and resolution data, it would be ideal to have a radar system that can capture all of the relevant frequency bands of interest. With a wideband radar system, the phased array system can dynamically switch between frequency bands or scan a small area over all frequencies. For a weather radar, this can provide a good picture of activity using only one radar installation. Similarly, for defense focused radar systems, the distance and detection resolution can provide a significant amount of data using only a single structure. Considering that the radar systems, such as PAVE PAWS and Cobra Dane, are immense structures with a very large number of elements in the array, it is especially attractive to capture this amount of data with a single structure.

1.3 SiGe HBT Technology

Over the last decade, SiGe heterojunction bipolar transistor (HBT) technology has become a strong contender for the wireless integrated circuit design space. With peak transition frequency, f_T, on the order of 250-350 GHz commercially available it is well suited for high-frequency design. In fact, a SiGe HBT in a 130 nm process node has been presented with f_T/$f_{MAX} \approx$ 505 GHz/720 GHz [11]. A significant advantage of SiGe HBT technology over compound semiconductors, which achieve excellent AC performance, is the ability to integrate CMOS transistors on the same die. With CMOS available in SiGe technology, supporting analog and digital circuits can be incorporated onto the same die, making it ideal for full system integration. When compared with advanced node CMOS, which also has high f_T/f_{MAX}, SiGe technology has the advantage of not needing highly scaled lithography nodes. With commercially available SiGe HBT processes using 90 nm to 130 nm lithography nodes, the fabrication cost savings compared to advanced CMOS makes it a highly attractive technology platform.

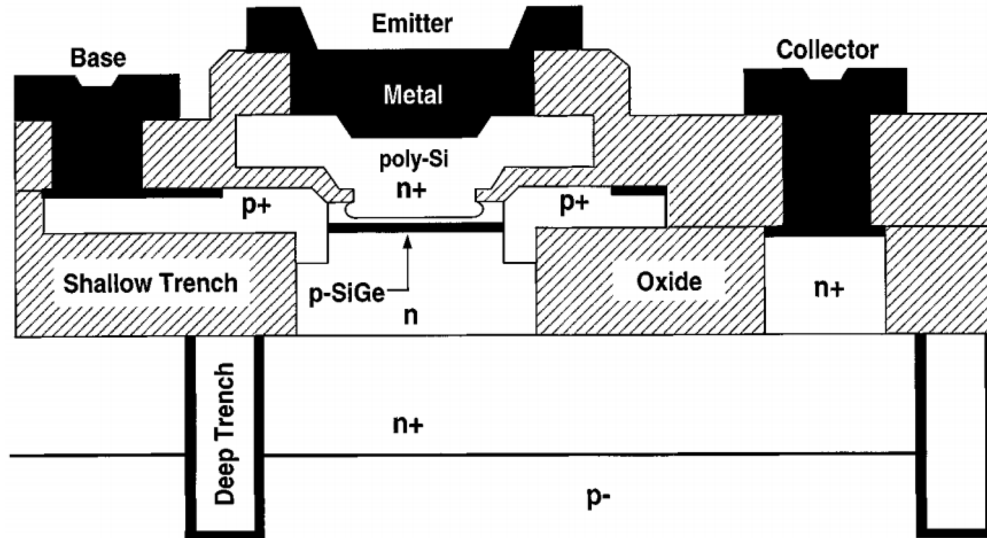

Figure 1.5: Cross Section of a SiGe HBT from [12]

SiGe HBT technology is able to achieve these advantages due to the underlying physics

of the device. SiGe HBTs have a n-type emitter, p-type SiGe base, and an n-type collector to form the npn transistor. A cross-section of a SiGe HBT is shown in Fig. 1.3 [12]. The SiGe base utilizes a graded germanium (Ge) layer through the base along with the highly doped p-type silicon. Due to the lower bandgap of Ge, compared to silicon, a drift field in the base is produced. This drift field in the base is controlled by the grading of the Ge. [13] This effectively allows device designers to employ bandgap engineering techniques with Ge to construct profiles for SiGe HBTs. By introducing the graded Ge in the base, the resulting drift field will allow electron entering the base to more quickly exit through the collector. The outcome of this is lower emitter-collector transit times which will result in higher f_T. Another benefit of the graded Ge in the base is the reduced conduction band barrier at the emitter-base junction. This allows more electrons to enter the base for a smaller base-emitter voltage. When compared with a Si BJT, the SiGe HBT achieves a higher current gain (β) as a consequence of bandgap engineering the emitter-base junction. Another relevant result of the graded Ge in the base is the decrease in broadband noise from the device. This is afforded by the improvement in f_T and β. The improvement in noise performance is particularly relevant for low-noise amplifiers and wireless receivers.

With scaling in SiGe technology, the f_T/f_{MAX} performance has improved with each generation [13]. At the same time, with improved AC performance, the breakdown voltages are also decreasing. However, compared to CMOS equivalent technologies, the breakdown voltages afforded in SiGe technology are higher.

For wideband applications, the reduced parasitics, improved noise performance, and high power gain of SiGe HBTs that make SiGe technology attractive to use. With reduced parasitics, broadband impedance matching can be more easily achieved. With improved noise performance, the receiver noise figure can be improved, increasing the overall dynamic range of the transceiver. With higher power gains, smaller devices, with fewer parasitics, can be used to output high power at RF frequencies. Each of these advantages plays a key role in designing efficient wideband RF front-end modules.

CHAPTER 2

WIDEBAND RF FRONT END DESIGN CONSIDERATIONS

The RF front-end module is a critical component for any wireless communication system. It is typically comprised of a single-pole double-throw (SPDT) switch, a power amplifier (PA), and a low noise amplifier (LNA). A block diagram of this system is shown in Fig. 2.1. Each of these components plays a key role in the overall performance of the wireless link. The SPDT switch allows control to switch between whether the LNA or PA is connected to the antenna. Essentially, switching between the transmitter and receiver mode of operation in the transceiver. The LNA is the first amplification block in a receiver, and is critical in setting the receiver sensitivity. The PA is the final block in the transmitter chain that will amplify the driving signal to high power levels that will be radiated through the antenna. Each of these blocks come with significant design challenges. For this thesis, the design considerations of the PA and LNA will be expanded on in this chapter.

To achieve wideband operation, a naive approach would be to simply place an RF switch at the input and output and have several amplifiers. This type of system is shown in Fig. 2.2. The major problems associated with this are power consumption and incurred losses. With many narrowband amplifiers, the overall front-end module power will significantly increase compared to using a single wideband amplifier. In terms of incurred losses from the switches, this will increase the system noise figure on the receive side, lowering the dynamic range. On the transmit side, this will reduce the output power from the PA, again lowering the dynamic range of the transmitter. Due to these limitations, it is more attractive to design a single amplifier that covers the full bandwidth of interest.

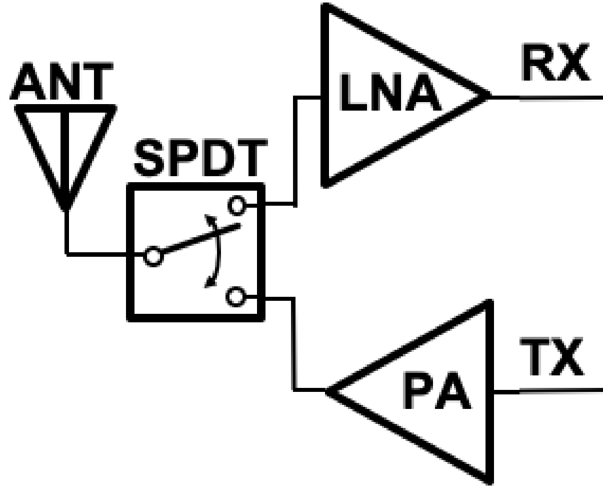

Figure 2.1: Typical block diagram of an RF front end module.

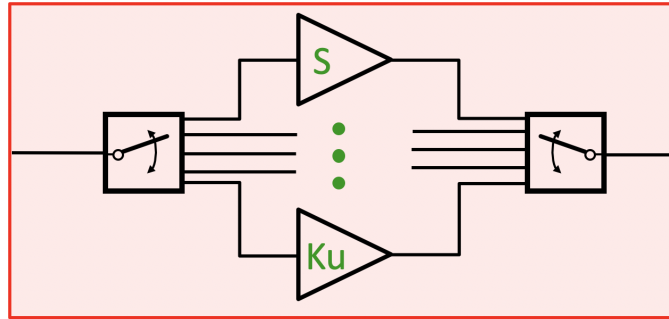

Figure 2.2: Naive approach to a wideband system design.

2.1 Wideband Power Amplifier Design

When considering a wideband PA, there are three performance metrics that are highly desirable. These include wideband impedance matching, high saturated output power (P_{sat}), and high power added efficiency (PAE). P_{sat} is maximum output power that the PA can provide. PAE is defined by equation 2.1. In this equation, P_{out} is the output power for the input power, P_{in}. P_{dc} is the dc power consumption for the input power.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{2.1}$$

In a narrowband design, the impedance matching networks can be readily synthesized over the small bandwidth. This allows the PA designer to focus on optimizing for output power and PAE. In a wideband design, the PA designer must balance impedance matching with P_{sat} and PAE. A Venn diagram of this tradeoff can be seen in Fig. 2.2. To increase P_{sat} in a typical PA, the device size can be increased to get higher output power from the transistor. At the same time, to improve PAE, the amplifier gain can be increased. However, these techniques tend to reduce the bandwidth of amplifiers. A larger device size will have higher input and output capacitance which will make it harder to synthesize a wideband impedance match at the input and the output. By increasing the gain of the amplifier, there is an inherent tradeoff between gain and bandwidth, where for a larger gain the bandwidth will be reduced. Another limitation for both narrowband and wideband high output power PAs is the modest breakdown voltage of highly scaled SiGe technology. With these constraints, a balance must be reached in the design procedure to accommodate broadband operation.

To achieve broadband operation, the conventional approach is to use a distributed amplifier. A distributed amplifier provides an attractive method to alleviate wideband matching difficulties by absorbing amplifier input and output capacitances into the transmission line synthesis. At low frequencies, where physical transmission lines are prohibitive on-chip, artificial transmission lines made of LC sections are used. An important consideration is to ensure the constructed inductors are not close to their self-resonant frequency. Since the artificial transmission lines are designed with a specific inductance and capacitance over frequency, self-resonance frequency of an inductor will limit the transmission line from operating at the designed impedance. Furthermore, as inductors approach self-resonance, the inductance will start rapidly increasing. For this reason, the designed inductors must have self-resonant frequency significantly higher than the maximum frequency of interest. For smaller bandwidths, this is typically not as difficult but with a large bandwidth, such as 2 GHz to 20 GHz, the inductance required to synthesize the desired impedance can be large. With a large inductance, there is a risk of self-resonance close to the high-frequency

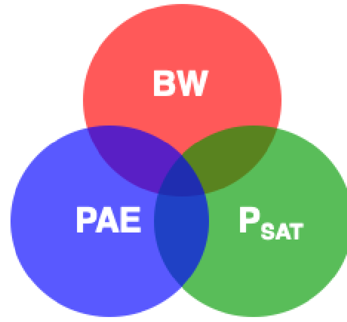

Figure 2.3: Wideband PA Design Space.

edge at 20 GHz. To overcome this, two or more smaller inductors can be placed in series which individually have higher self-resonant frequencies. This will fix the problem, but can make the layout more challenging.

For power amplifiers, the another concern with artificial transmission lines is with regard to electromigration. To synthesize an artificial transmission line with a large transistor, with high input capacitance, the required inductance can be large. Typically, for high inductance density, thin signal lines with small spacing between turns are used. However, this not only increases the loss of the inductor, but will also limit the permissible maximum current before electromigration is a concern. For a PA, with high current swings depending on the output power, wider signal lines may be needed. By using wider signal lines, the inductance will drop and the self-resonance frequency will be a concern. This will need to be compensated with additional turns or splitting the inductor into multiple series inductors.

2.2 Wideband Low Noise Amplifier Design

For a wideband LNA, the design tradeoffs are different than the PA. In a wideband LNA, it is desirable to have wideband impedance matching, low noise figure across the bandwidth, as well as moderate 1 dB compression point. A Venn diagram of the tradeoffs can be seen in Fig. 2.3. The compression point is especially important for radar systems, as the received signal may be large. Ideally, the amplifier will have a high dynamic range such

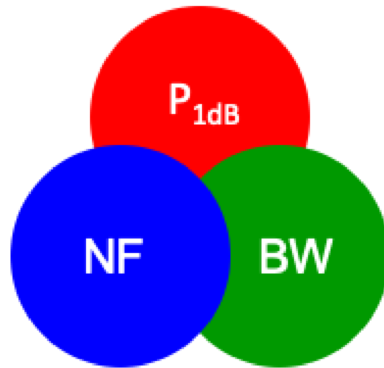

Figure 2.4: Wideband LNA Design Space.

that the LNA does not limit the overall receiver dynamic range. In a narrowband design, there are many techniques such as transformer feedback, noise cancellation, and tuned loads [14]. However, many of these techniques typically only operate over a small range of frequencies.

There are two main approaches in wideband LNA design. First is to use a distributed amplifier approach to alleviate the matching constraints. While the distributed approach provides very good input and output matching, the passive performance needs to be considered. For a distributed amplifier used as an LNA, the loss of the input transmission line will directly add to the overall noise figure of the amplifier. Similar to the PA, at low frequencies, the transmission lines are constructed using an artificial transmission line. Therefore, the added noise from the input artificial transmission line comes down to the quality factor of the inductors and capacitors used in the line. An advantage of the distributed amplifier is that the input and output matching networks can be decoupled. In addition, the gain of the amplifier cells can mostly be designed separately from the matching network.

A second approach is a resistive feedback topology that can be used to achieve broadband impedance matching. For a resistive feedback amplifier, the noise from the feedback resistor will directly affect the overall noise figure. However, unlike the distributed amplifier approach, with feedback, the input and output of the amplifier are now coupled and the gain of the main amplifier cell will directly affect both.

Another consideration for an LNA is the optimum noise impedance. For a narrow-band LNA, the optimum noise impedance can be much more closely matched the the input impedance when compared with a wideband design. If the optimum noise impedance is not matched across the full bandwidth, then the noise figure of the LNA will be high at frequencies where it is not matched. This is undesirable for a wideband LNA. Therefore, the noise and gain matching needs to be balanced over the full bandwidth.

CHAPTER 3

DESIGN OF A WIDEBAND 1-20 GHZ SIGE POWER AMPLIFIER

Wideband power amplifiers are highly sought after for wideband radar systems. However, as SiGe technology continues to scale to lower process nodes to achieve faster speeds, breakdown voltages necessarily decrease. For power amplifiers (PAs), this reduced breakdown voltage manifests itself as limited output power due to limits on maximum achievable voltage swing. In addition, over large bandwidths, the optimum bias and impedance for maximum output power change significantly. A wideband power amplifier requires robust wideband input and output matching, a reasonable saturated output power, and high power added efficiency (PAE) across band.

There have been several demonstrations of wideband power amplifiers. The conventional approach is to utilize a distributed amplifier (DA) topology [15, 16, 17, 18, 19]. This technique utilizes on-chip transmission lines and the intrinsic input and output capacitance of amplifiers to achieve wideband impedance matching. Theoretically, a large number of stages could be used to achieve matching across all frequencies. However, a major limitation of this approach is the loss associated with the on-chip transmission lines. As the number of PA stages increase, the passive loss of the input and output transmission lines in DAs degrade the output power and the PAE. In a linear PA with high voltage or high current traveling down the output transmission line, series resistance can significantly lower the signal power prior to reaching the output of the circuit. This places a practical limit on the number of realizable stages in a DA used as a power amplifier. Transistor stacking has been used to achieve high output power ([20],[21]). However, these solutions, by themselves, tend to be for narrowband applications. In this approach, instead of using many stages to achieve high output power, the design incorporates the benefits of transistor stacking and a distributed amplifier topology. To further increase the output power, a tapered impedance

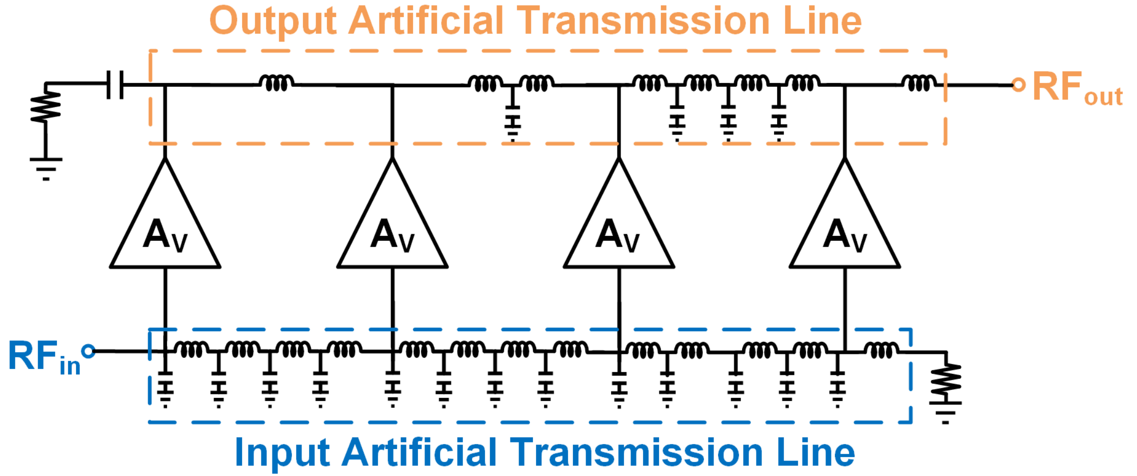

Figure 3.1: Schematic of a wideband distributed power amplifier with artificial transmission lines at the input and output. The core amplifier sub-circuit is shown in Fig. 3.2.

output transmission line is used to combine the powers from each stage.

3.1 Design Methodology

The circuit schematic of the wideband power amplifier and the core amplifier stages are shown in Fig. 3.1 and Fig. 3.2, respectively. For the stacked transistors, SiGe HBTs are used with single collector, base, and emitter (CBE) stripes. For each level in the stacked structure, there are two 8 μm emitter length SiGe HBTs wired in parallel.

The two key features of the present design include the distributed amplifier and the stacked transistor cores. To decouple the wideband matching from the power amplifier cores, a distributed amplifier topology was used. Lumped element inductors were used in conjunction with the input and output capacitances of the power amplifier cores to synthesize artificial transmission lines and thereby achieve wideband matching at the input and output. For the distributed amplifier configuration, a reverse termination resistor of 200 Ω was also added on the output transmission line to maintain stable operation. On the output collector transmission line, large trace widths in the inductors were used to minimize resistive losses, which limits the PAE degradation associated with passive loss at the output. The

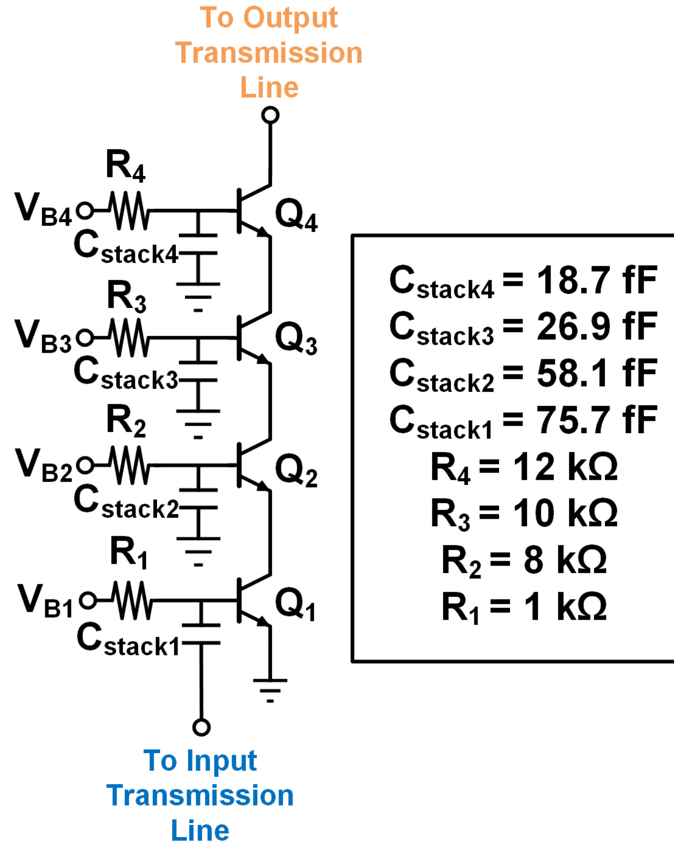

Figure 3.2: Schematic of stacked SiGe HBT core amplifiers. The bias resistors and capacitors are the same for all stages of the amplifier.

design of the artificial transmission lines was simulated in SONNET, an electromagnetic solver, to accurately model the inductance and capacitance. For the output collector transmission line, this design utilizes a tapered impedance technique. For a tapered transmission line, the characteristic impedance of the first section is largest where each consecutive section has a lower impedance. In a traditional distributed amplifier, the output transmission line characteristic impedances are all equal and half of the power goes to the reverse termination resistor that is matched to the characteristic impedance. In the present design, the output impedance was designed for $50\,\Omega$, with a reverse termination resistor of $200\,\Omega$. By tapering the impedance, the ratio of current that flows to the output was engineered to achieve a higher output power.

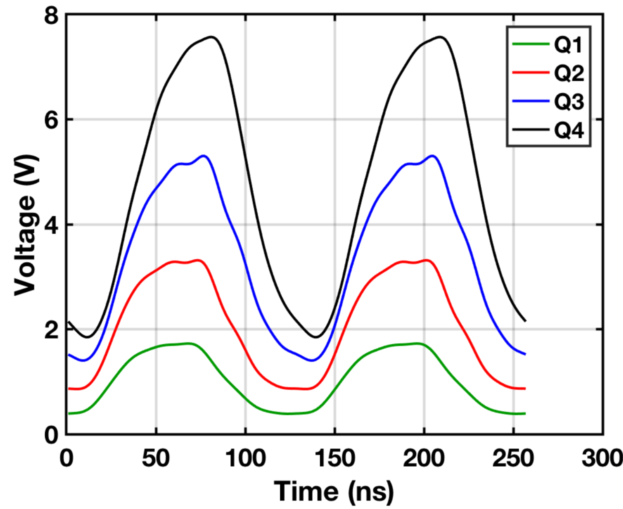

Figure 3.3: Simulated collector voltage waveform for the first stage in the wideband power amplifier. Increasing collector voltage swing for each transistor moving up the stack. Q1, Q2, Q3, and Q4 correspond to the transistors in Fig. 3.2.

3.2 Transistor Stacking

To deliver high power to the load, a stacked transistor topology was used in the power amplifier core cells. Transistor stacking relaxes the breakdown limitations of the individual transistors by sharing the maximum AC swing across the full stack. The amplifier was biased in Class-AB for operation as a linear amplifier and to maintain adequate small-signal gain to support both low and high input drive power. The waveform of the collector voltages, along the first stage transistor stack is shown in Fig. 3.3. The even division of voltage swing has been engineered along the stacked structure to alleviate stress on any single device. In addition, unlike the traditional cascode topology with an AC grounded common-base transistor, in a stacked configuration each transistor in the stack has AC swing at the base node. This AC swing is set through capacitive division between the shunt capacitance on the base (C_{stack}) and the base-emitter capacitance of the device (C_{be}). If C_{stack} is not set properly for the device size it can affect the amount of AC swing amplified further up the stack. The typical size of C_{stack} is on the order of 50 fF. This nominal value is largely influenced by the C_{be} of the devices being used in the stacked structure.

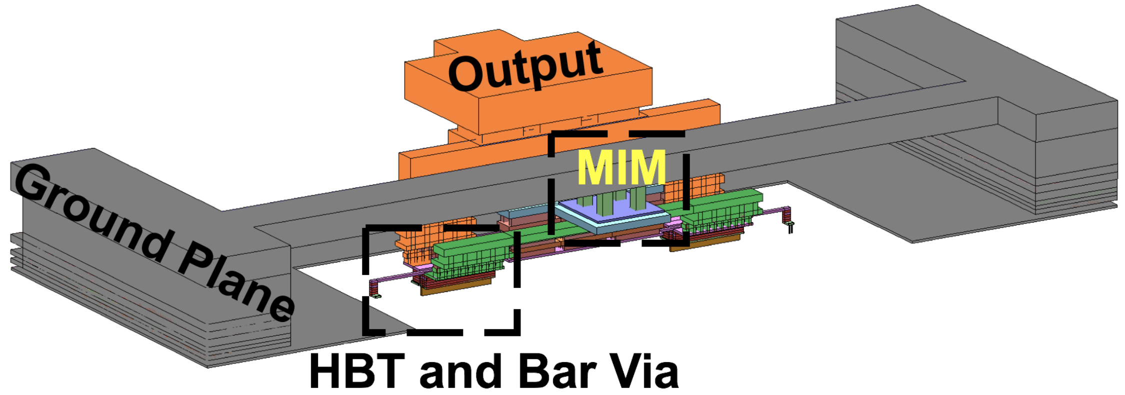

Figure 3.4: Core layout of SiGe HBT core with C_{stack} (labeled MIM). A ground plane surrounds the core SiGe HBT and connects the capacitor to ground. The connection of the capacitor to ground, as well as to the base of the SiGe HBT, both contribute to parasitic inductance. A high density of bar-type vias are placed to minimize inductance.

As a result, if the layout is not accurately extracted to minimize unwanted inductance, the true C_{stack} value can be noticeably different resulting in an undesired amount of AC swing. In a wideband amplifier, this can degrade high frequency performance, where small inductance becomes significant. For the C_{stack} capacitors, high-Q metal-insulator-metal (MIM) capacitors available in the process were used. A 3D view of the core layout can be seen in Fig. 3.4. The connection from the MIM capacitor to the base of the SiGe HBT is kept short. In addition, the ground connection for the MIM capacitor is fed to the ground plane, from a top metal layer, on both sides to reduce inductance. Finally, high-density bar-type vias were used in order to minimize additional via inductance from the capacitor plate to the base of the SiGe HBT. Starting from the bottom stack to the top, the C_{stack} values utilized are: 75.7 fF, 58.1 fF, 26.9 fF, and 18.7 fF.

In order to realize the benefits of transistor stacking, careful attention to the DC bias at each base node is critical. Based on the expected AC swing at each base, set by capacitive division, the DC base bias can be determined. Each bias should be chosen such that the transistor stays within the forward-active mode of operation. To connect the DC pad to the base of each stacked transistor, a series resistor was placed to isolate the AC swing from the pad connection. The value of series resistor should be chosen such that the DC voltage at

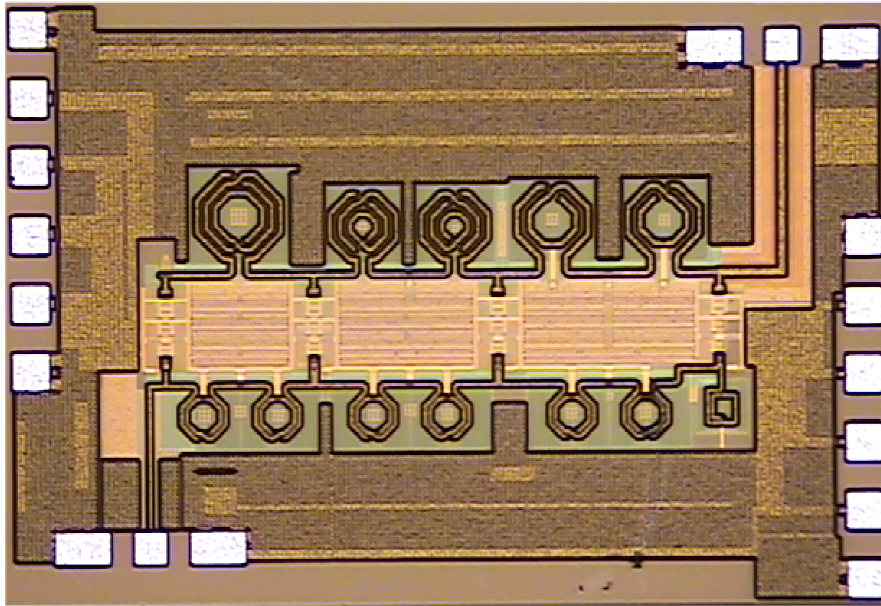

Figure 3.5: Chip micrograph of power amplifier.

the base is not dropped significantly between low and high input power levels. Otherwise, the amplifier will saturate as segments of the stacked transistor structure begin to deviate from forward-active mode, degrading performance. Starting from the bottom stack to the top the series resistor values are: 1 kΩ,8 kΩ,10 kΩ, and 12 kΩ.

3.3 Measurement Results

The chip micrograph of the power amplifier is shown in Fig. 3.5. The dimensions are $1.95\times1.3\text{mm}^2$. The power amplifier was biased at $V_{CC} = 5\,\text{V}$ and consumes a DC current of 38 mA during small-signal operation. Starting from the bottom transistor in the stack, the transistor biases at each base are: 0.88 V, 2.17 V, 3.25 V, and 4.35 V. Bias tees were used at the input and output for DC decoupling and to apply V_{CC}.

The small-signal S-parameters are shown in Fig. 3.6. The S-parameters are measured on an Agilent E8364B PNA with 50-GHz RF GSG probes. DC probes were used to facilitate on-die testing of the amplifier. The input and output return loss (S_{11} and S_{22}) match

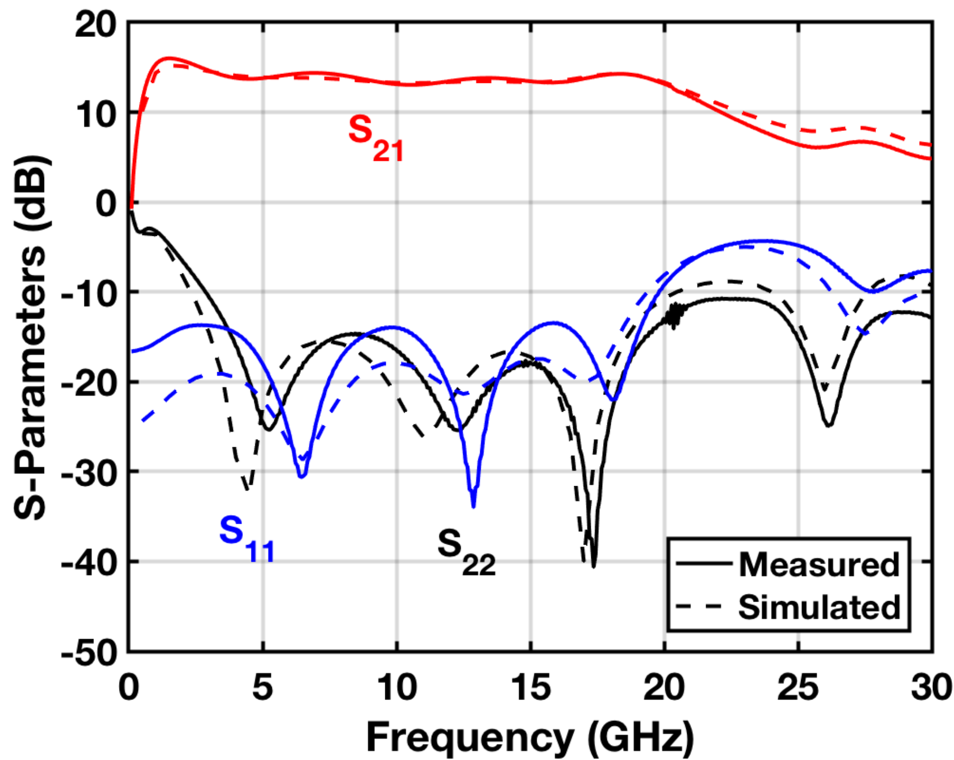

Figure 3.6: Measured and simulated S-parameters across frequency.

well with the simulated results. The input matching is below -10 dB from 100 MHz to 20 GHz. The output matching is below -10 dB from 2.5 GHz to 30 GHz. The small-signal gain is approximately 14 dB with a 3-dB bandwidth of 20 GHz.

The large-signal PA characteristics were measured using an Agilent E8257D 67-GHz RF signal generator, an Agilent E4413A Power Sensor, and an Agilent E4419B Power Meter. The loss of bias tees, cables, adapters, and probes were accounted for in calibration to accurately determine the output power of the circuit. Fig. 3.7 shows the output power and PAE measured from 1 GHz to 22 GHz, in 1 GHz increments. The output power was measured with $P_{in} = +9$ dBm, which yields peak PAE. The peak output power was achieved at 1 GHz with $P_{out} = +19.5$ dBm at a PAE of 28.5%. The measured results are well-matched to the simulated results at frequencies under 10 GHz. Beyond 10 GHz, due to additional parasitic capacitance in the layout, the large-signal performance was degraded by approximately 1 dB to 1.5 dB from 10 GHz to 20 GHz. At the top stack of the final stage in the

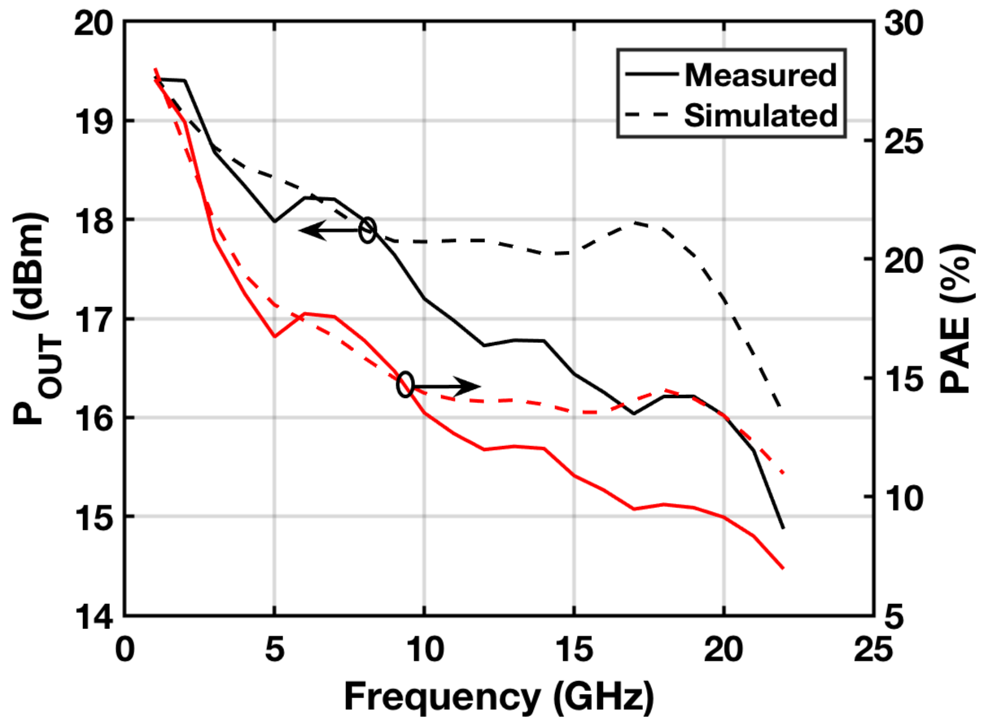

Figure 3.7: Measured and simulated large-signal characteristics over frequency.

distributed amplifier, a parasitic capacitance around 75 fF to 90 fF from the connection of the top stack to the output artificial transmission line degrades the large-signal performance. This capacitance degrades the output power and therefore the PAE of the amplifier at high frequencies where 90 fF becomes a significant impedance in the circuit.

The P_{in} vs. P_{out} relationship is shown in Fig. 3.8 at 2 GHz, where output power and PAE are plotted as a function of input power. At this frequency, the input power that results in peak PAE is $P_{in} = +9$ dBm.

Table 1 compares this SiGe power amplifier with other state-of-the-art wideband power amplifiers from various Si-based and III-V technologies. The present design presents the highest peak PAE compared to other silicon-based wideband power amplifiers, and operates over a larger bandwidth than III-V based wideband power amplfiers.

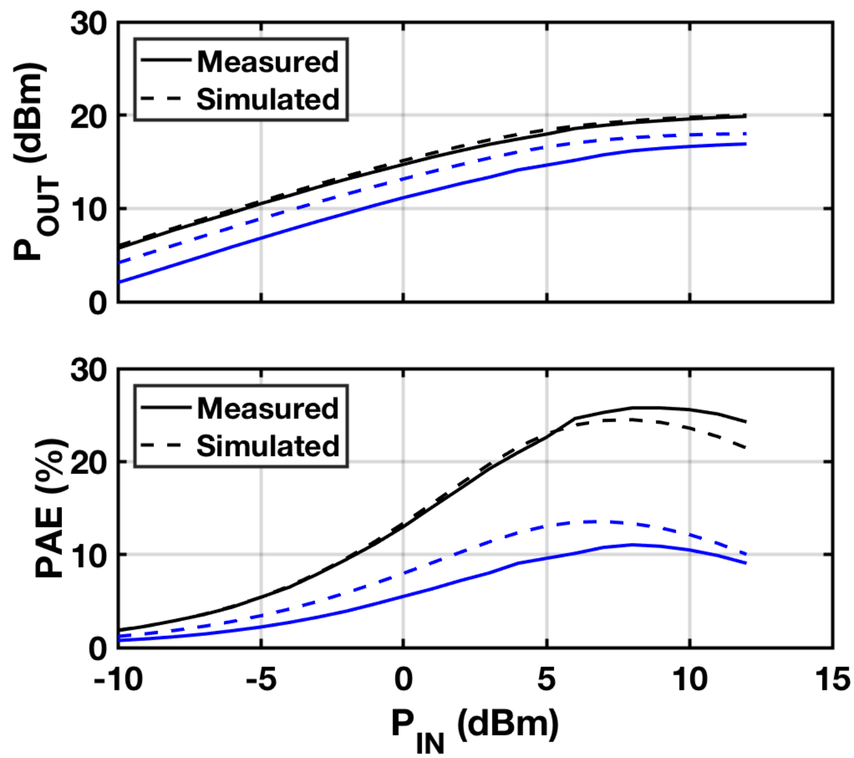

Figure 3.8: Relationship of output power and PAE with increasing input power at 2 GHz (black) and 15 GHz (blue).

Table 3.1: COMPARISON OF STATE-OF-THE-ART WIDEBAND POWER AMPLIFIERS

References	**Technology**	**Topology**	**Bandwidth (GHz)**	P_{OUT} **(dBm)**	**PAE (%)**
TMTT 2011 [15]	130 nm SiGe	DA (8-stage)	DC - 77	14.5-17.5*	6-13.5*
TMTT 2009 [16]	250 nm SiGe	TWA**	2 - 10	–	10.3-22.1
JSSC 2016 [17]	90 nm SiGe	DA (8-stage)	15 - 85	13.9-17*	6-12.6*
TMTT 2015+ [22]	130 nm SiGe	Push-Pull	4.5 - 15.5	21.3-25.5	11.9-28.7
ISSCC 2010 [23]	90 nm CMOS	Push-Pull	5.75 - 13	21-25.2*	12.5-21.2*
ISSCC 2015 [24]	65 nm CMOS	Push-Pull	2 - 6	20.1-22.4	19-28.4
JSSC 2009 [18]	250 nm GaN	DA (10-stage)	1.5 - 17	39.5-42*	20-38
TMTT 2017 [19]	100 nm GaAs	DA (4-stage)	1.5 - 10	29-30.5*	33-44
TMTT 2016 [21]	100 nm GaAs	Transistor Stacking	3.5 - 7	26.2-27.8	45-62
This Work	**90 nm SiGe**	**DA (4-stage) w. Transistor Stacking**	**1-20**	**16-19.5**	**9.1-28**

*Graphically estimated

**TWA = Traveling Wave Amplifier

+ Two Parallel Cells

CHAPTER 4

DESIGN OF A WIDEBAND 1-18 GHZ SIGE LOW NOISE AMPLIFIER

As mentioned previously, wideband low noise amplifiers have grown in popularity due to their broad bandwidth and improved noise performance with technology scaling. In addition, the extreme environments associated with deep space exploration applications add another layer of design complexity as shown in [25]. With the added twist of operation in extreme environments, circuit designers must embrace design topologies which can retain performance over extreme temperatures, for instance [25]. In addition, for practical uses in emerging cryogenic applications such as those associated with radio astronomy, and even quantum computing, circuits must retain their low noise performance with very low power consumption [26].

4.1 Wideband Low Noise Amplifier Design

For the wideband LNA, a resistive feedback topology was employed. It has been demonstrated and shown in [27] that a resistive feedback topology naturally lends itself to stable operation with decreasing temperature. For biasing at lower temperatures, in order to maintain the same bandwidth, the collector current should be kept fixed with cooling. This allows the circuit to maintain the same operational bandwidth while still receiving the benefits of higher gain.

The amplifier core was designed to operate over a broad bandwidth while consuming minimal power. To achieve this a V_{CC} of 2 V is used, allowing for a maximum collector current (I_{CC}) of approximately 15 mA. The resulting J_C is 4.8 mA/μm^2 for the amplifier core. Three $8\,\mu m$ emitter length HBTs are combined in parallel for both the common-emitter and cascode transistors. The emitter length and bias were chosen as a tradeoff between device parasitic capacitance, noise performance, and gain. The base of the upper

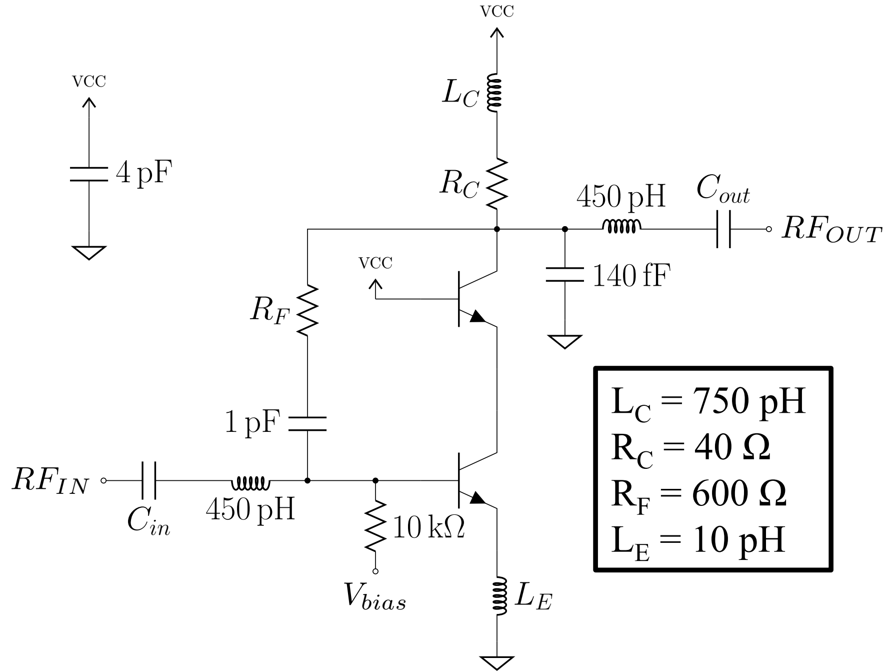

Figure 4.1: Simplified circuit schematic of designed wideband SiGe LNA.

transistor is tied to V_{CC} for biasing convenience. A simplified circuit schematic can be seen in Fig. 4.1.

In a resistive feedback LNA the collector current of the main cascode amplifier and feedback resistor are used to set the input return loss and bandwidth of the amplifier. For an ideal $50\,\Omega$ match, there is a specific R_F for a given collector current that will provide broadband matching. However, with this approach, the value of R_F will be small, leading to increased noise. In addition, since the source impedance for minimum noise does not typically align with $50\,\Omega$, the noise performance will be sacrificed even further. As the noise from R_F adds directly to the output of the amplifier, a small R_F will have a large noise contribution. To overcome this limitation, a large resistance of $600\,\Omega$ is utilized here for feedback. To compensate for the degraded input matching, an L-type matching network is added to resonate out the input capacitance of the transistors. To move the optimum noise impedance close to $50\,\Omega$, a small inductive degeneration (L_E) is utilized. The L-type matching network also transforms the optimum noise impedance, along with the input

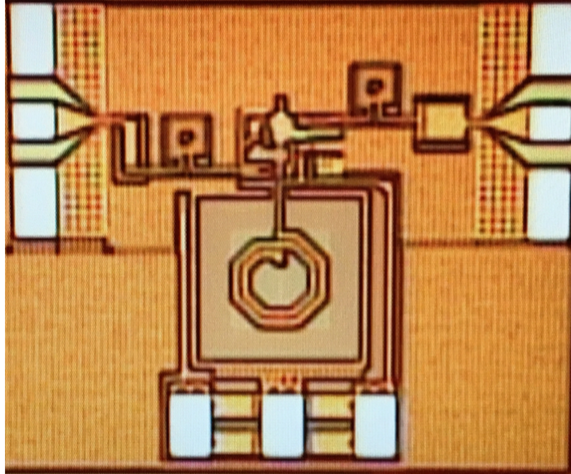

Figure 4.2: Die photograph of fabricated SiGe LNA. The chip occupies 590x520 μm^2 and 950x750 μm^2, excluding pads, and with pads, respectively.

impedance, to be close enough for inductive degeneration to sufficiently match both over a broad bandwidth. Finally, to further increase the bandwidth, a shunt peaking inductor is applied at the load to compensate for high frequency gain roll-off. The collector resistance and inductance, R_C and L_C, were designed together to provide minimal gain variation over the designed bandwidth. As a result of this design methodology, this topology provides a reasonable tradeoff between gain, bandwidth, and noise figure.

4.2 Measurement Results

The circuit was designed in the GlobalFoundries BiCMOS 8XP technology platform, with $f_T/f_{MAX} \approx 250/330$ GHz at 300 K. The die photograph is shown in Fig. 4.2. The amplifier was measured on-wafer with a 67 GHz Agilent E8361C PNA for S-parameter characterization. P_{1dB} measurements were also completed using a 67 GHz Agilent E8257D signal generator with a 26.5 GHz power sensor and EPM E4419B power meter. Noise figure was characterized using an Agilent PXA N9030A in noise figure mode.

Fig.4.3 shows measurement results at room temperature, demonstrates acceptable agreement vs. simulation results. The peaking inductor is larger than simulated, shifting the high-frequency zero down slightly, resulting in a small reduction of bandwidth. At 300 K,

the V_{CC} and I_{CC} were 2 V and 15 mA, respectively, resulting in a $P_{DC} \approx 30$ mW. The noise figure at 300 K was also measured. The measured noise figure is higher than simulated. This is due to the slightly lower gain of the measured LNA compared to simulation. In addition, the increase in noise figure beyond 15 GHz is likely caused by the slight reduction in bandwidth observed from the S-parameter measurements.

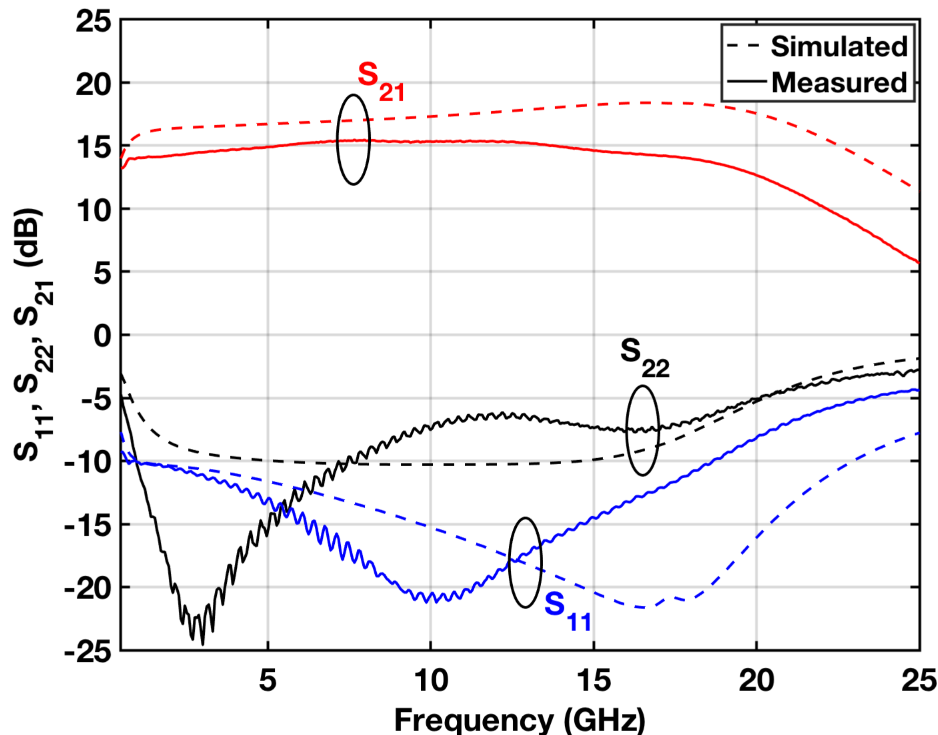

Figure 4.3: Simulated and measured S-parameters at 300 K.

4.3 Cryogenic Characterization of a Wideband SiGe LNA

It is well established that silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have improved f_T/f_{MAX} and broadband noise performance at cryogenic temperatures as shown in [28]. However, with increased frequency response and noise performance, the risk of instability grows as the gain of amplifiers increases with decreasing temperature. As a result, the chosen circuit topology must not be sensitive to instabilities induced by device variations over temperature.

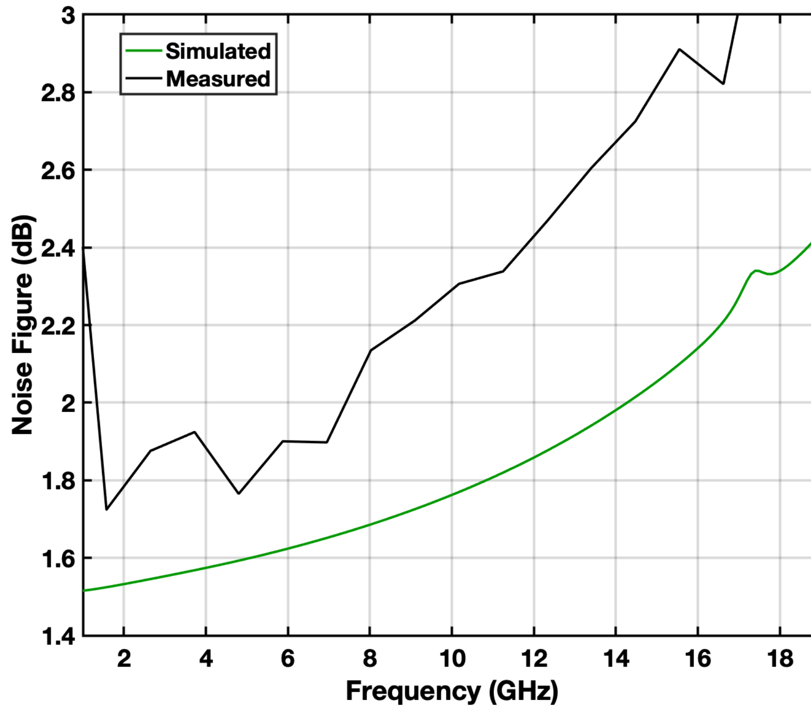

Figure 4.4: Simulated and measured Noise Figure at 300 K.

There have been several demonstrations of cryogenic LNAs implemented in SiGe technology as reported in [29, 30, 31]. Each of these circuits demonstrate the potential for SiGe LNAs operating at cryogenic temperatures. However, these circuits operate over a very limited bandwidth. The authors in [32] demonstrated a broadband cryogenic SiGe LNA with low noise performance, but at the cost of relatively high power consumption. The LNA described in the previous section operates over a similarly broad bandwidth and consumes up to a third of the DC power compared to state-of-the-art cryogenic LNAs.

4.4 On-Wafer Cryogenic Noise Measurements

To accurately measure the noise performance at cryogenic temperatures, the cold attenuator method was used [33]. Fig. 4.3 shows a diagram of the measurement setup for on-wafer cryogenic noise measurements. By using the cold attenuator method, an external noise source can be used in cryogenic noise measurement. The attenuator effectively shrinks

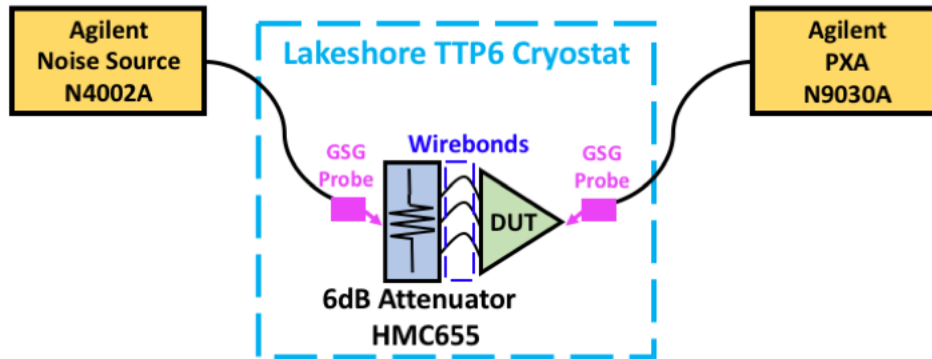

Figure 4.5: Block diagram of on-wafer cryogenic noise measurements.

the hot and cold noise temperature to provide more resolution when the device under test exhibits low noise at cryogenic temperatures. The cold attenuator method requires the measured cable loss and attenuation over frequency (and temperature). To accomplish this, a standalone attenuator and thru are used to extract the losses using a power meter and signal generator. To accommodate the cold attenuator setup with on-wafer probing, a standalone fixed attenuator is bonded directly to the input of the LNA. An Analog Devices HMC655 attenuator is used. The wirebonds are kept as short as possible to minimize any effect on circuit performance. This was verified using S-parameters. A separate standalone attenuator is also placed in the cryostat to be characterized at each temperature for accurate de-embedding of noise temperature (T_e). Using the measured loss and attenuator at each physical temperature, on-wafer noise measurements can be conducted with RF and DC probes. This is the first demonstration of on-wafer cryogenic noise measurements using the cold attenuator method. Traditionally, the amplifier is packaged and then measured with a coaxial cryogenic attenuator. This is problematic for cryogenic system design due to the wirebonds. At high enough frequency the packaging of the amplifier with wirebonds will cause a shift in expected circuit performance. If the wirebonds are not included in the design, the measured results will not show the true performance of the circuit. For full

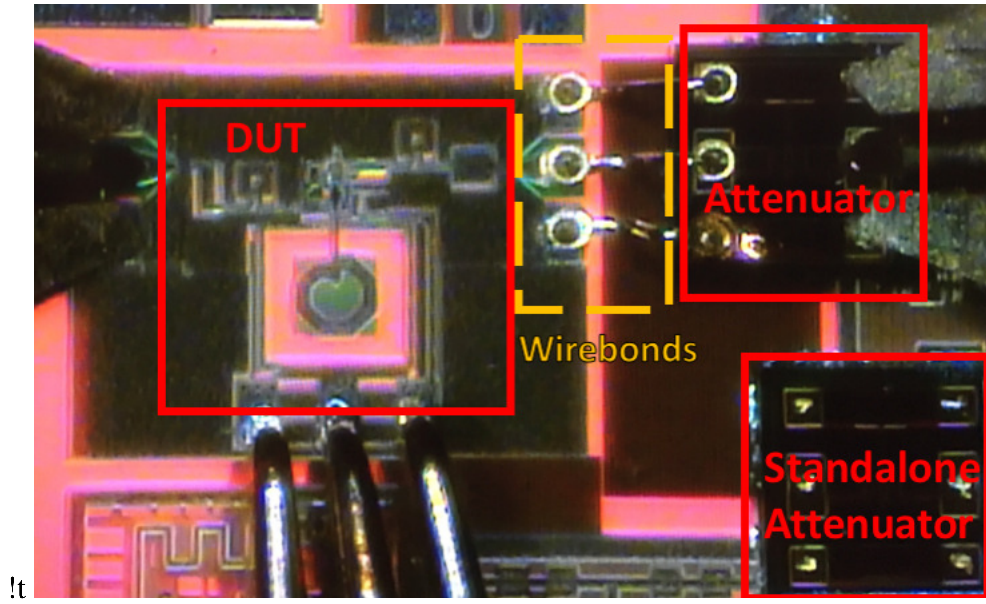

Figure 4.6: Photo of on-wafer cryogenic noise measurement setup.

system integration, getting an accurate measurement of noise is important such that the following stages don't need to be over designed.

4.5 Measurement Results

For cryogenic characterization, a custom-designed Lakeshore TTP6, open-cycle, 67 GHz capable, cryostat with liquid helium was utilized for on-wafer measurements. Due to the naturally larger g_m of SiGe HBTs at cryogenic temperatures, the power dissipation can be reduced while maintaining gain and bandwidth. The minimum power dissipation was experimentally found to be $P_{DC} \approx 23$ mW. Fig. 4.5 shows the S-parameters over temperature. Physical temperatures (T_A) of 300 K, 77 K, and 40 K were used, since they are relevant temperatures for cryogenic applications in space exploration missions [25]. At 300 K, 77 K, and 40 K, the input return loss shows very minimal variation, which demonstrates the robustness of this circuit topology. In addition, S_{21} increases at lower temperatures, as expected, while retaining the originally designed bandwidth. No oscillation was observed at any temperature or bias measured. Furthermore, the gain flatness at all temperatures is

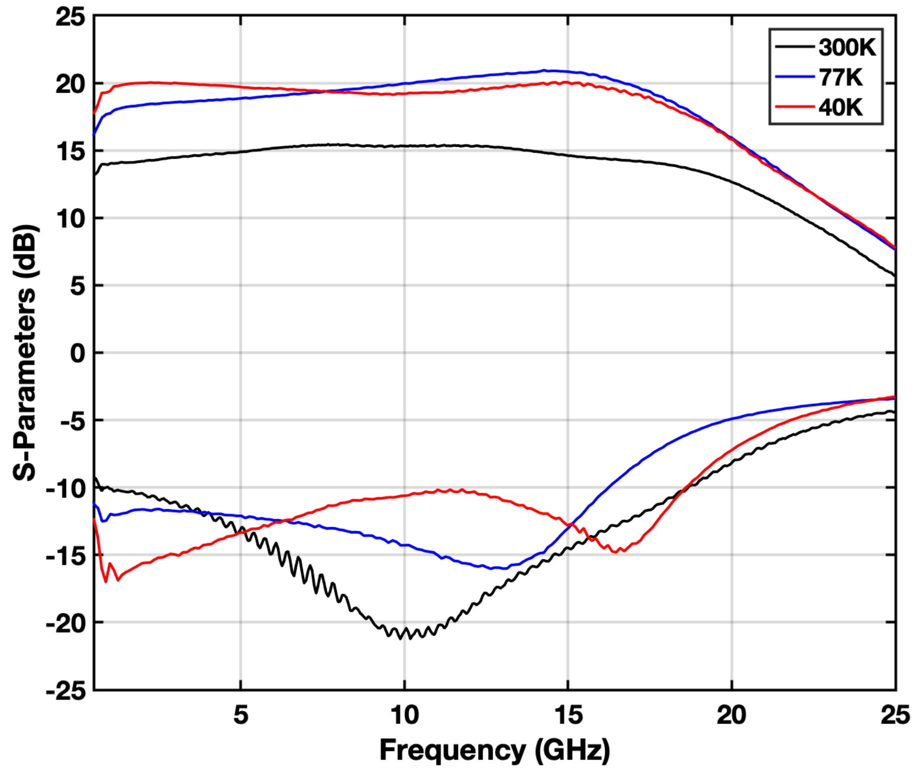

Figure 4.7: Measured S-parameters over temperature.

maintained, with only 1 dB gain variation up to 18 GHz at 40 K.

The output-referred P_{1dB} was also measured across temperature, as shown in Fig. 4.6. The input power was swept on the signal generator between -35 dBm and -10 dBm at each frequency in the band. The output power was then measured on an EPM power meter. The measured results indicate that even with the lower voltage headroom utilized at cryogenic temperatures, the gain compression of the amplifier is not significantly affected.

The noise performance of the amplifier was evaluated at cryogenic temperatures using the cold attenuator method. Fig. 4.7 shows the measured noise temperature (T_e) at 300 K, 77 K, and 40 K. The minimum achieved noise temperature is approximately 47 K at a physical temperature of 40 K, while consuming only 23 mW of DC power.

Table 1 compares this work with state-of-the-art LNAs operating at cryogenic temperatures. For an LNA operated at cryogenic temperatures to be practical for use in real

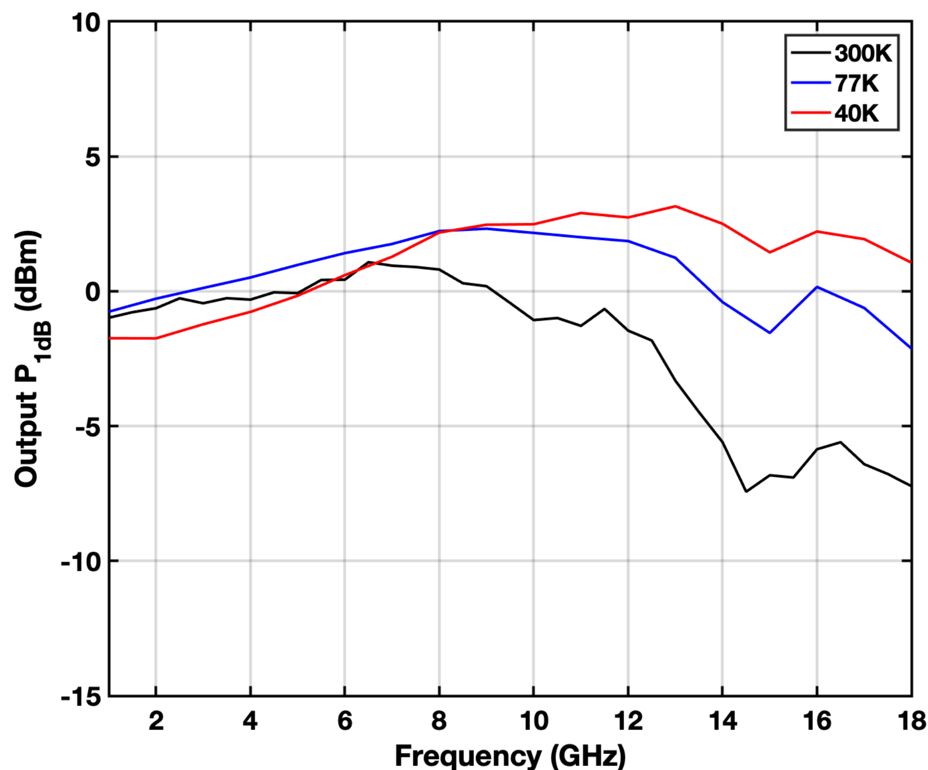

Figure 4.8: Output-referred P_{1dB} over temperature.

systems, it must balance gain, noise, and power consumption. From Table 1, it can be seen that the present work achieves higher T_e and less gain per mW of DC power compared to the narrowband cryogenic LNAs demonstrated in [29, 30]. However, this tradeoff is expected, since a narrowband design can be further optimized for minimum noise temperature and consume less power. Compared to a wideband cryogenic LNA reported in [32], this LNA presents competitive bandwidth at a much lower power consumption.

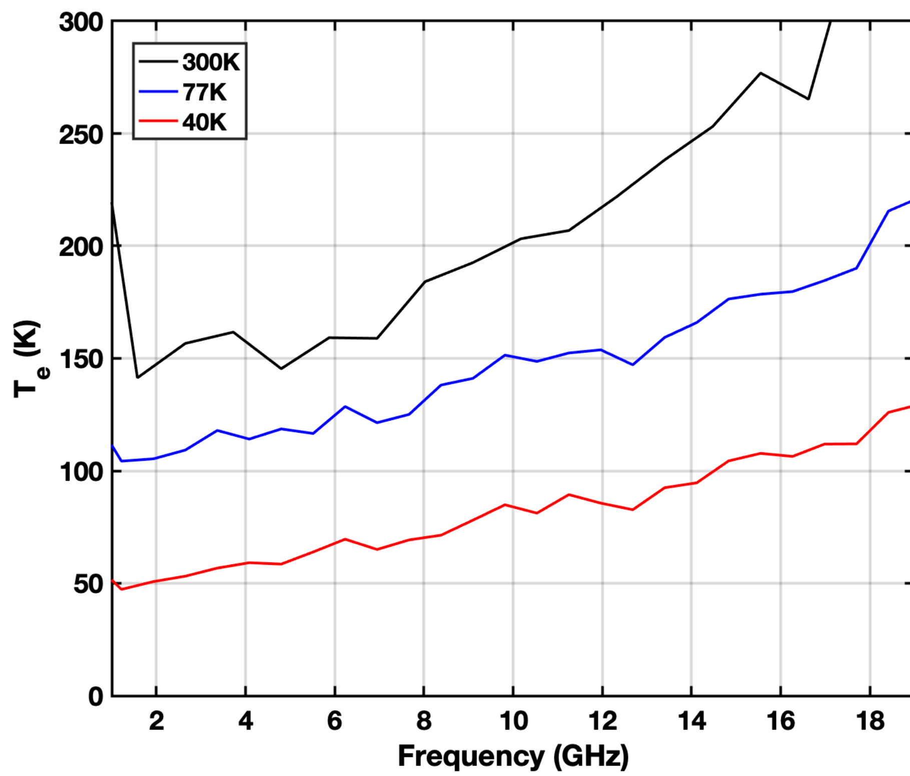

Figure 4.9: Measured noise temperature over physical temperature.

Table 4.1: COMPARISON OF STATE-OF-THE-ART CRYOGENIC LOW NOISE AMPLIFIERS

Reference	**[31]**	**[29]**	**[30]**	**[32]**	**This Work**
Technology	100 nm InP mHEMT	0.13 μm SiGe HBT	0.13 μm SiGe HBT	0.13 μm SiGe HBT	0.13 μm SiGe HBT
Packaged/Wafer	Packaged	Packaged	Packaged	Packaged	Wafer
Gain (dB)	31.5	28	15	23	20
Bandwidth (GHz)	4-12	2-4	8-12	1-20	0.3-19
T_A **(K)**	15	16.5	15	17	40
Minimum T_e **(K)**	5.3	3.3-4	21	10	47
P_{1dB} **(dBm)**	-	-	-	3*	2
Gain Ripple (dB)	3	1	3	6	3
Power (mW)	8	3	2.25	60	23

CHAPTER 5
CONCLUSION

This thesis presented the design and measurement of wideband RF front-end circuits designed in a SiGe BiCMOS technology. In particular, the power amplifier and low-noise amplifier are evaluated for their performance across frequency. The motivation for wideband systems in the context of a wideband radar system was presented. SiGe BiCMOS technology was shown to be a promising contender for wideband circuit design.

The design space for a wideband front-end T/R module was covered. The inherent tradeoffs that exist for the wideband power amplifier and low-noise amplifier were discussed. Beyond transistor level tradeoffs, the impact of passive components on output power and efficiency in the PA and noise figure in the LNA were discussed.

The design and measurement of a 1-20 GHz wideband power amplifier implemented in a highly-scaled 90 nm SiGe BiCMOS technology was discussed. The designed power amplifier used a distributed amplifier topology along with transistor stacking to simultaneously achieve high output power and wideband impedance matching. This work achieved wideband operation with a peak output power of 19.5 dBm and peak power-added efficiency of 28 % at 1 GHz. At the time of publication, this work demonstrated the highest peak PAE among other silicon-based wideband power amplifiers operating over a similar bandwidth.

The design and measurement of 1-18 GHz wideband low-noise amplifier design in a 130 nm SiGe BiCMOS technology was discussed. This work utilized a resistive feedback topology to achieve wideband operation and low noise figure. In addition to room temperature characterization, the low noise amplifier was characterized at cryogenic temperatures. The measured results demonstrate 20 dB of gain with better than 1 dB gain flatness at 40 K, with retained wideband matching up to 18 GHz. This work exhibits a minimum noise

temperature of 47 K at an ambient temperature of 40 K while only dissipating 23 mW of power. To the best of our knowledge, this work demonstrates a high performance wideband SiGe LNA that consumes one-third of the power of comparable state-of-the-art cryogenic amplifiers.

The measured performance of these RF front-end circuits demonstrate the potential for SiGe technology to be used in wideband radar systems.

5.1 Future Work

Regarding future research directions, there are a number of open opportunities. First, to complete the wideband front-end T/R, an investigation of a wideband RF switch will be conducted. Unlike the power amplifier or low noise amplifier, the RF switch has no gain, only loss, and, as a result, has an entirely different trade space. With the development of a switch, a fully integrated wideband front-end T/R can be produced, suitable to radar applications.

Furthermore, for space-based radar applications, the electronics are subjected to wide temperature ranges. To accommodate the extreme environments that electronics are subjected to, a cryogenic characterization of the RF switch and power amplifier can be conducted. As SiGe technology has been shown to have numerous advantages at lower temperatures, characterization of a fully-integrated chip would be an excellent demonstration of these properties.

Finally, with the push to millimeter-wave frequencies, there is growing interest in millimeter-wave capable radar systems [2]. In addition, with SiGe technology approaching THz speeds [11], there is potential for high-performance radar systems at higher frequencies. At millimeter-wave, the design tradeoffs change compared to the 2-20 GHz design space. At millimeter-wave frequencies, the intrinsic gain of the transistors is low. As a result, the minimum noise figure of the receiver and the power-added efficiency of the transmitter are limited. An investigation into wideband millimeter-wave front-end circuits

poses an interesting trade space that has yet to be thoroughly examined. The goal of future work in this research would be to evaluate millimeter-wave bandwidth limitations and investigate potential circuit level solutions to enhance both the gain and bandwidth of circuit designs.

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