CAPACITIVE MICROMACHINED ULTRASOUND TRANSDUCER (CMUT) DESIGN AND FABRICATION FOR INTRACARDIAC ECHOCARDIOGRAPHY

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CAPACITIVE MICROMACHINED ULTRASOUND TRANSDUCER (CMUT) DESIGN AND FABRICATION FOR INTRACARDIAC ECHOCARDIOGRAPHY

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In the loving memory of a beautiful heart, strong woman and caring mother, Soori Saber-Navaei, who battled with "Scleroderma" for 17 years, and never gave up. Although I have not been able to see her during the past 6 years, she was, is and will be in my heart and thoughts forever <3

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LIST OF SYMBOLS AND ABBREVIATIONS

ALD – Atomic layer deposition

ASIC – Application-specific integrated circuit

BEM – Boundary element method

BW piezoelectric micromachined ultrasound transducers

CMOS – Complementary metal oxide semiconductor

CMUT – Capacitive micromachined ultrasonic transducer

DOF – Depth of field

ECR – Energy conversion ratio

FEA – Finite element analysis

ICE – Intracardiac echocardiography

IVUS – Intravascular ultrasound

LPCVD – Low pressure chemical vapor deposition

MIMO – Multiple-input multiple-output

PECVD – Plasma enhanced chemical vapor deposition

PMUT – Piezoelectric micromachined ultrasound transducer

PZT – Lead zirconate titanate

Rx – Receiver

SNR – Signal-to-noise ratio

TEE – Transesophageal echocardiography

TIA – Transimpedance Amplifier

TTE – Transthoracic echocardiography

TSV – Through silicon via

Tx – Transmit or transmitter

SUMMARY

The objective of this research is to develop capacitive micromachined ultrasonic transducer (CMUT) arrays with novel geometry for intracardiac echocardiography (ICE) imaging along with a novel reliable CMUT fabrication process to improve the system performance. We used custom CMOS electronics and monolithically integrated our CMUT arrays to CMOS chips. The arrays are designed for 9-Fr (<3mm) ICE catheters over a total area of about 2.6x11-mm^2 at around 7-MHz center frequency with ~80% fractional bandwidth in both 1D and 2D configurations. The 1D array transducer includes 64 channels with beam-steering capabilities for cross sectional ICE imaging application at distance range of about 5-cm. The ICE image with 40-dB dynamic range from 7 metal wires has been obtained. Several 2D (sparse) arrays are designed based on signal-to-noise ratio (SNR) optimization capable of generating volumetric images. The CMUT-on-CMOS technique is used for arrays integration with our ASICs using vias for top and bottom electrode connections to the related electronics pads. A 60-V pulse is optimized during transmit operation and 2-MPa surface pressure has been achieved that is in agreement with our simulation results. We also developed an improved CMOS compatible low temperature sacrificial layer fabrication process for CMUTs. The process adds the fabrication step of silicon oxide evaporation which is followed by a lift-off step to define the membrane support area without a need for an extra mask. The parasitic capacitance is reduced about 15% and device long-term test demonstrates 72-hours stable output pressure showing no significant degradation on performance. We have also developed a new energy-based calculation method for CMUT performance evaluation that is valid during both small and large signal operation since well-known frequency and capacitance based coupling

coefficients definitions are not valid for large signal and nonlinear operation regimes. The quantitative modeling results show that CMUTs do not need DC bias to achieve high efficiency large signal transduction: AC only signals at half the operation frequency with amplitudes beyond the collapse voltage can provide energy conversion ratio (ECR) above 0.9 with harmonic content below -25-dB. The overall modeling approach is also qualitatively validated by experiments.

CHAPTER 1. INTRODUCTION AND BACKGROUND

1.1 Medical Ultrasound Imaging

Ultrasound has long been used in the medical diagnosis field for various types of diseases including obstetrics, abdominal diagnostics, pelvis related diseases, cardiology, urology, ophthalmology, gynecology and orthopedics [1, 2, 3]. In addition to diagnosis, ultrasound has been recently used for several types of cancer treatment in both high and low intensity form [4, 5, 6, 7]. In the following sections, a brief history of ultrasound principles in cardiac imaging and catheter technologies will be discussed.

1.1.1 History of Medical Ultrasound Imaging

Lazzaro Spallanzani, an Italian priest, biologist and physiologist, first discovered echolocation among bats, which led to the discovery of ultrasound principles [8]. By publishing his famous book about sound waves, "The Theory of Sound" in 1877, Lord Rayleigh has been instrumental in the development of the science of acoustics. [9]. During the same epoch, 1880, Pierre Curie and Jacques Curie demonstrated the piezoelectric effect in Quartz and Rochelle salt [10]. In fact, their research was the first experimental exhibition of the relationship between material crystal structure and macroscopic piezoelectric effect. Later in 1915, Physicist Paul Langevin, inspired by the sinking of the Titanic, invented a transducer for sound transmission underwater [11]. Subsequently, ultrasonic and acoustic became separate sciences after the applications of ultrasonic technology was discovered. Most notably, in World War I, underwater tools such as Sound Navigation and Ranging, or SONAR, used sound propagation underwater to navigate, communicate with, or detect objects such as submarines or mines. The time of transmission and reflection of the sound wave is measured at a low frequency, which could detect the distance of the objects, even up to 10 miles away [12]. Several ultrasound concepts were understood during the high power transmission in the ocean during a sonar procedure; for example, ocean life that was lost due to the wave intensity characteristics of the sonar. These achievements led to a deep understanding of high intensity ultrasonic and other wave propagation concepts [12].

During and after World War II, technologies such as electronics, signal processing, medical instrumentation and transducers were rapidly developing, which led to realization of the entire ultrasonic system for military, medical and also domestic use [12]. Following attempts by Karl Dussik – scientist and neurologist – to use ultrasound waves to detect tumors in the brain, the Naval Medical Research Institute developed a new method to diagnose gallstones with a basic A-mode imaging platform. After World War II, in 1953, physician Inge Edler and engineer C. Hellmuth Hertz demonstrated successful ultrasound image from the structure of the heart and made the first echocardiogram system [13] (Figure 1.1). After successful demonstrations of several cancer tumor detection and cardiogram systems, scientists designed a Doppler ultrasound platform for sensing moving structures; their developments resulted in

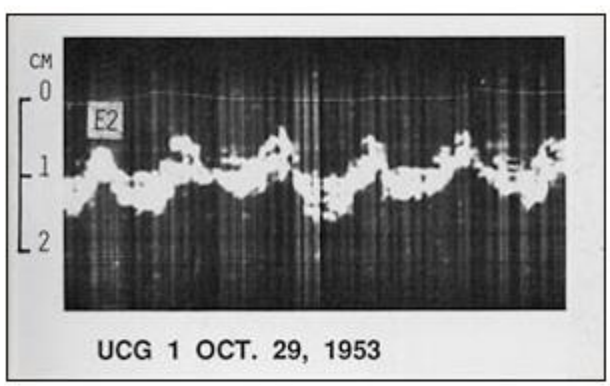


Figure 1.1. First recording of the heart ultrasound echo at 1953

imaging of the blood flow in the heart.

Japanese researchers started exploring ultrasound technology in medical imaging in the same era; soon after they exhibited how to detect gallstones, breast masses, and tumors. Further progress in transducer developments, clinical procedures, IC design and front-end electronics integration with medical transducers opened new avenues for both medical diagnosis and treatment; gynecological ultrasound, mammography, laparoscopy, endoscopy, endorectal ultrasonography, vascular ultrasonography and etc. [14, 15, 16, 17].

1.1.2 Principles of Ultrasound Imaging

Ultrasound imaging is the most important application of ultrasound waves, which is normally defined as acoustic waves with a frequency range more than 20 kHz. Ultrasound imaging systems usually consist of an acoustic wave generator, receiver and the target object [18]. Ultrasound transducers are excited by electrical signals and generate pressure waves, and considering reciprocity, they are capable of sensing reflected acoustic waves. The focus of this research is ultrasound imaging in liquids and specifically blood. Despite solid mediums that can carry both longitudinal and shear waves, liquid mediums are only capable of carrying longitudinal wave. The longitudinal wave travels at the speed of sound in a medium, which is a characteristic of the material. When a wave travels from one medium to another one, part of the wave's energy reflects. A reflection of a wave occurs due to the acoustical impedance mismatch of two mediums; acoustic impedance (Z) is defined as $\rho_0(density) * c(speed\ of\ sound)$ with Rayl unit. Based on the wave theory for a single frequency acoustic plane wave, the larger difference between medium impedances causes larger reflection factor (RF) – equation 1.1.

$$RF = \frac{Z_2 - Z_1}{Z_2 + Z_1} \qquad Eq. 1.1$$

A general medical imaging system is depicted in figure 1.2. Different beams are sent to a specific organ in the blood medium and the reflections detected are used in echo image construction.

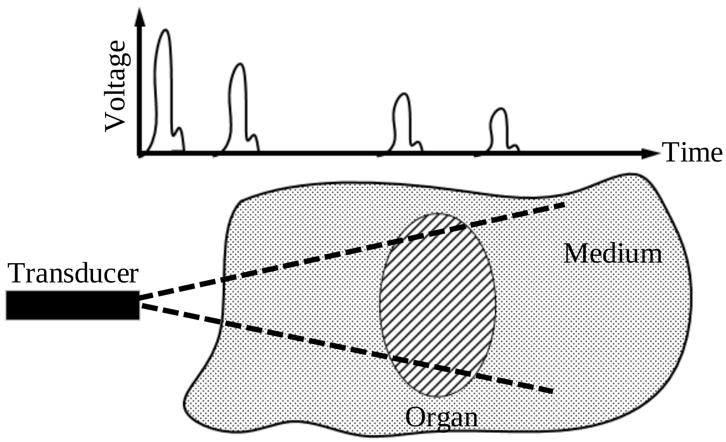


Figure 1.2. General pulse-echo medical imaging system.

In order to generate an ultrasound image, three different types of losses have to be compensated; medium acoustic attenuation, diffraction loss from source and reflection loss from the object, which is a soft tissue in this research – intracardiac echocardiography (ICE) [18]. The acoustic attenuation (α - $dB.cm^{-1}$) in blood has different mechanisms, on both cellular and molecular levels, including absorption, viscosity, thermal conduction, structural and thermal relaxation processes [19]. Treeby et al. demonstrated a new method to measure the acoustic attenuation in blood tabulated in Table 1.1. In this table, c is the speed of the sound and ρ is the density of the medium. From Table 1.1, it is clear that higher frequencies correspond to a higher loss factor. As an example, for a typical intracardiac echocardiography system, the frequency range is between 5-15-MHz and image is taken at a distance of about 5-10-cm. Therefore, a 10-MHz wave with 5 cm target object, in which the pulse-echo two ways travel is 10cm, the medium loss is about 21.6-dB.

Table 1.1. α_{0-70} and α_{0-15} are the power law fit for the measured data from 0-70-MHz and 0-15-MHz, respectively [19].

Component	c [m/s]	ρ [kg m^{-3}]	α_{0-70}	α_{0-15}
RBC in saline (10 g/dL)	1562 (0.7)	1036 (4.9)	$0.0106f^{1.88}$	$0.0475f^{1.47}$
RBC in saline (15 g/dL)	1576 (1.0)	1047 (5.6)	$0.0291f^{1.69}$	$0.0657f^{1.47}$
RBC in saline (20 g/dL)	1593 (1.0)	1058 (5.7)	$0.0596f^{1.56}$	$0.0798f^{1.49}$
Whole blood (15.1 g/dL)	1590 (2.8)	1049 (9.2)	$0.0546f^{1.58}$	$0.0596f^{1.56}$
Plasma	1553 (0.8)	1022 (2.6)	$0.0231f^{1.62}$	$0.0431f^{1.45}$
Phosphate buffered saline	1535 (2.7)	*997	–	–
Deionized water	*1524	*993	* $0.00139f^2$	* $0.00139f^2$

Figure 1.3 illustrates the attenuation loss in different frequencies; it can be concluded that lower frequencies result in lower signal loss and better penetration depth. A system level design approach for ICE arrays will be discussed in chapter 4 explaining how we achieve the required signal to generate the ICE image.

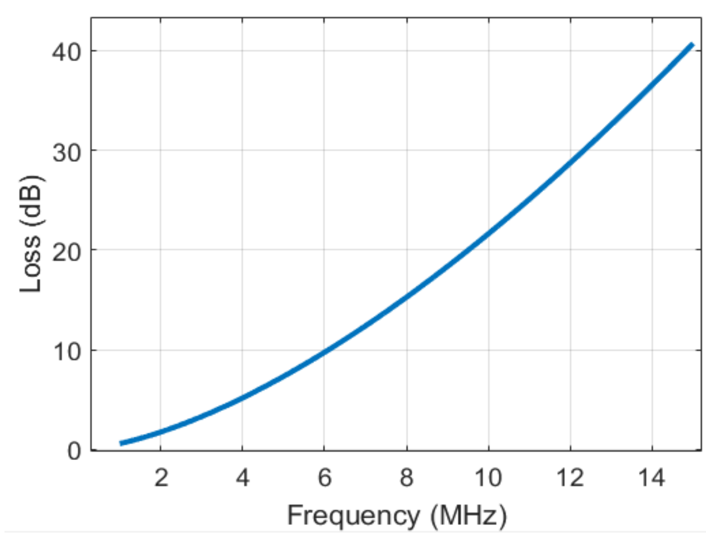


Figure 1.3. Medium attenuation for an object at 5cm in blood (10-cm 2 ways wave travel)

Another important parameter for the design of an ultrasound imaging system is the resolution; a better resolution helps physicians accurately detect anatomical features. In a typical 2D image, the resolution is defined as two perpendicular directions, axial (R_{axial}) and lateral ($R_{lateral}$) as shown in Figure 1.4. and given in equations 1.2 and 1.3, where

$$R_{axial} = \frac{c}{2 \cdot BW} \qquad Eq. 1.2$$

$$R_{lateral} = \frac{F \cdot \lambda}{D} \qquad Eq. 1.3$$

c and BW are the speed of the sound in medium and the bandwidth of the transducer respectively, therefore, a higher bandwidth denotes a better resolution in axial direction. Considering a fractional bandwidth of about 60-80% - which is the typical bandwidth for medical ultrasound transducers–

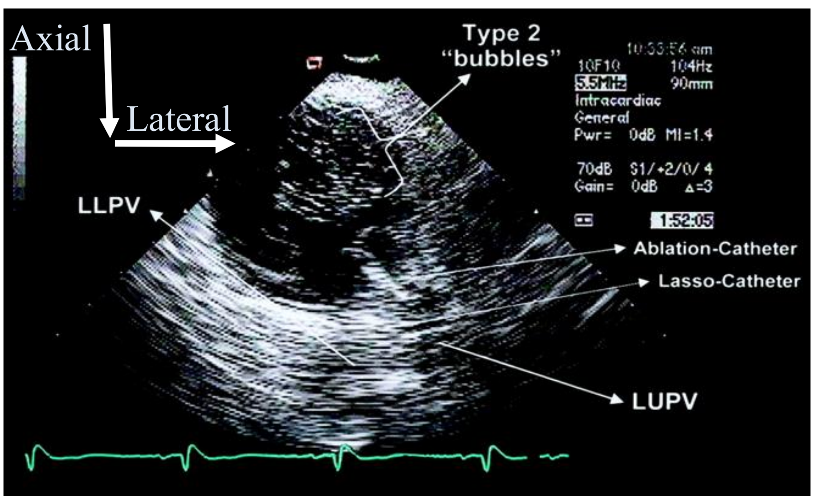


Figure 1.4. Definition of axial and lateral resolution in 2D ultrasound image. [39]

, higher bandwidth is then associated with the higher frequencies. The bandwidth comparison for different types of ultrasound transducers will be discussed later in this chapter and the next – energy analysis. In lateral resolution – equation 1.3 - λ, F and D are the wavelength, focal depth and aperture diameter of the transducer. Similar to axial resolution, higher frequencies lead to a higher resolution. Another design parameter is the aperture size of the transducer; larger diameters give better resolutions but larger near-field regions, which are not desirable for medical imaging purposes that usually work in the far-field region [18]. In this research, our goal is to achieve a ~200-μm resolution for a transducer array with 5-10-MHz center frequency.

1.1.3 Catheter-Based Echocardiography Modalities

Heart disease is the leading cause of the deaths worldwide [20]. About 630,000 Americans die from heart disease each year - that is 1 in 4 deaths [21]. Several types of heart disease can be diagnosed and treated by minimally invasive surgery that has less pain, shorter postoperative cares and less clinical complications rather than open-heart surgery. Minimally invasive procedures are performed by interventional cardiologists with the help of ultrasound imaging guidance for a variety of intravascular and cardiac diseases such as aortic valve replacement, atrial septal defect closure and atrial fibrillation ablation [22].

Although catheter based modalities are widely used for minimally invasive surgery, ultrasound probes are used as a non-invasive assessment of the overall health of the heart. Transthoracic echocardiography (TTE) is a method where a probe shows several details of the structure of the heart including the functionality of all four chambers (Figure 1.5) [23]. During TTE procedure, the probe is placed on the chest and may not have a clear path to the heart and blood vessels. Although TTE is the most common ultrasound system in the cardiac imaging field and can calculate several cardiovascular hemodynamics parameters, a transesophageal echocardiography (TEE) probe is more accurate. TEE is a system with a transducer on the tip of a flexible probe that reaches the heart through the esophagus and shows real time images of the shape of the heart, blood vessels, heart chambers and valves. As a diagnostic tool, TEE is useful in guiding catheters into the arteries. TEE can also detect blood clots or lesions in the arteries that can cause poor blood flow or heart failure.

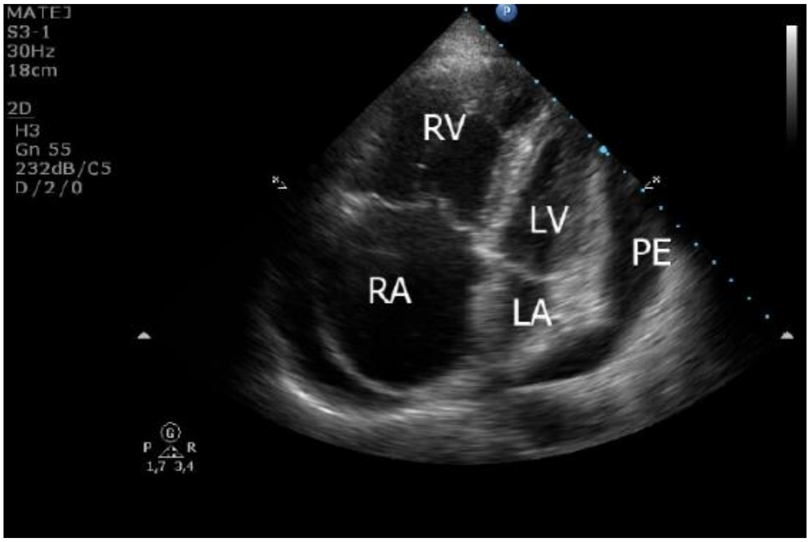


Figure 1.5. An example of transthoracic echocardiography (TTE) image of all 4 chambers of the heart [41].

TEE provides more detailes of the heart structure than TTE [24, 25, 26]. TEE is also capable of providing both 2D and 3D image from the heart which unveils many details and has significanly improved cardiovascular disease diagnosis including coronary, congenital and heart valve disease, heart attack, aortic aneurysm endocarditis, cardiomyopathy – figure 1.6 [27].

Similar to TEE, intracardiac echocardiography (ICE) is a promising technique that commonly used for structural heart imaging and can provide real-time images to guide cardiac interventions [28]. Typically, an ICE catheter employs a transducer with a center frequency of about 5-10-MHz for a depth penetration of about 5 – 15-cm [28, 29]. The size of an ICE catheter is usually 8-10 Fr (Φ = 3-mm). In order locate the ICE catheter inside the heart, a cardiologist inserts the ICE catheter inside the femoral vein and navigate to reach into the right atrium of the heart.

Although TEE and ICE can have similar functions to monitor the structure of the heart, ICE has several advantages over TEE (figure 1.7). The TEE probe needs to be guided by X-ray fluoroscopy and the procedure requires general anesthesia that needs extra personnel and cost. Current TEE systems are suitable to monitor the heart structure before and after procedure, although the probes are not suitable to be manipulated during therapeutic procedures [30]. The TEE system is also limited by esophagus route, lung tissue and bone. Moreover, a TEE probe is larger than the ICE catheter tip and usually is not suitable for children. A current commercial ICE catheter, ACUSON AcuNav, utilizes 1D piezoelectric transducer arrays capable of generating 2D echo images.

AcuNav is a side-firing 90 cm ultrasound catheter available in both 8-Fr (2.7-mm) and 10-Fr (3.3-mm) size. Although new techniques have recently been introduced to generate 3D ICE images from limited 2D arrays, they suffer from limited field of view - 24°x 90° image (figure 1.8) [31].

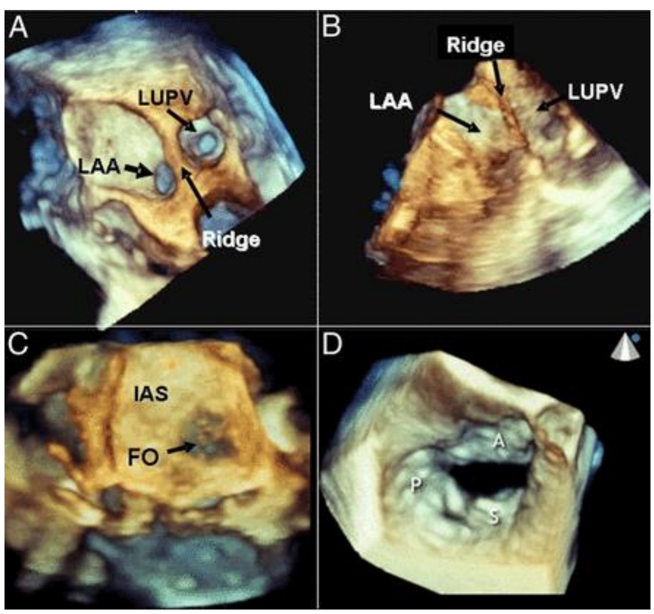
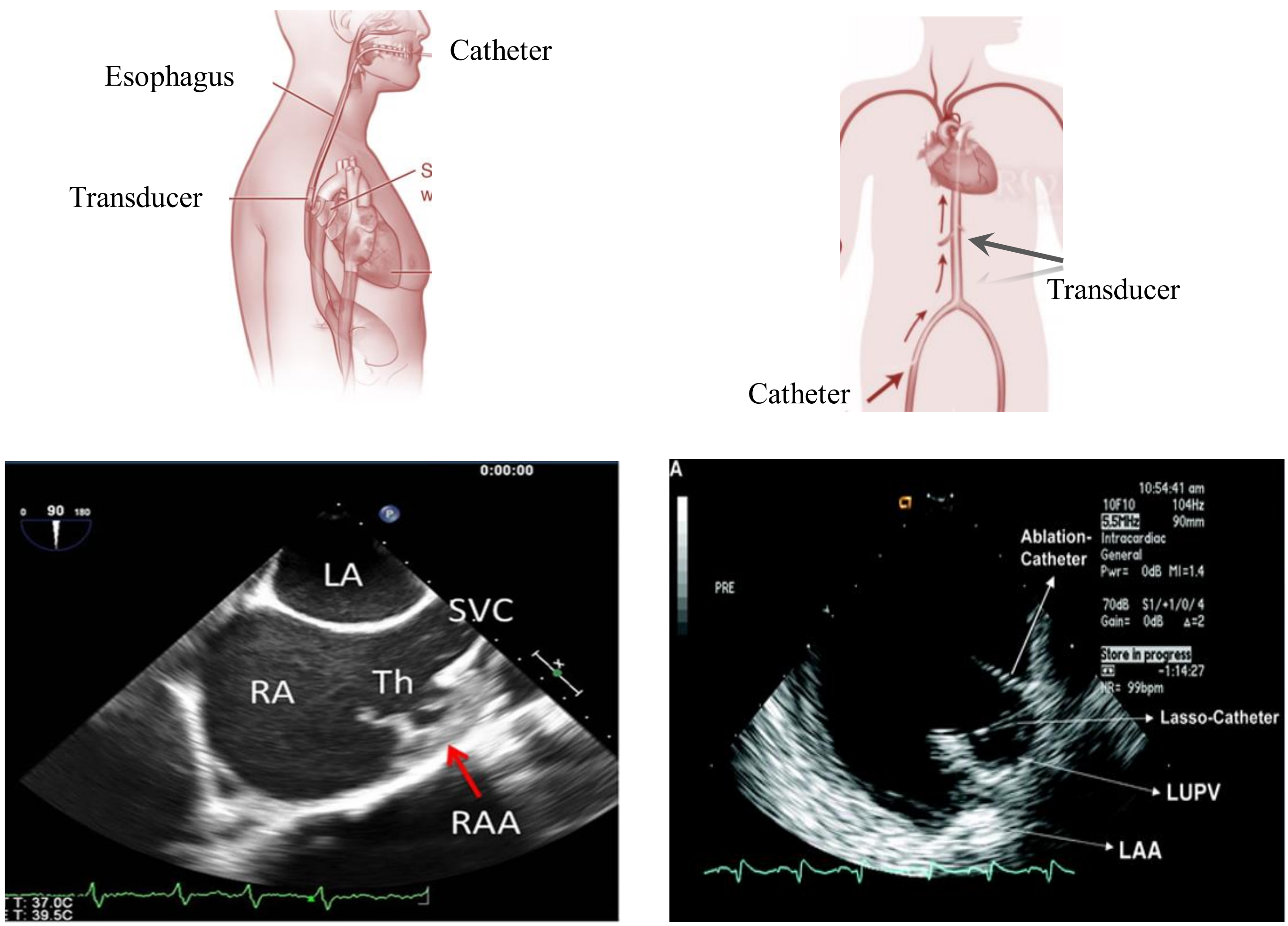


Figure 1.6. Example of 3D TEE image from heart. A) The left atrial appendage (LAA) in the long-axis view. B) The ridge separating the LAA from left upper pulmonary vein (LUPV). (C) Interatrial septum (IAS) from the left side showing the foramen ovale (FO). (D) Tricuspid valve showing the septal (S), anterior (A), and posterior (P) leaflets [42].

Transesophageal echocardiography (TEE) | Intracardiac echocardiography (ICE)



- Needs general Anesthesia and intubation
- Fluoroscopy to guide catheter
- Not suitable for children
- Unsuitable to guide catheter during therapeutic procedures

- No anesthesia/other personnel
- Better resolution
- Small enough for children
- Suitable for intraprocedural

Figure 1.7. TEE and ICE comparison [40, 39]

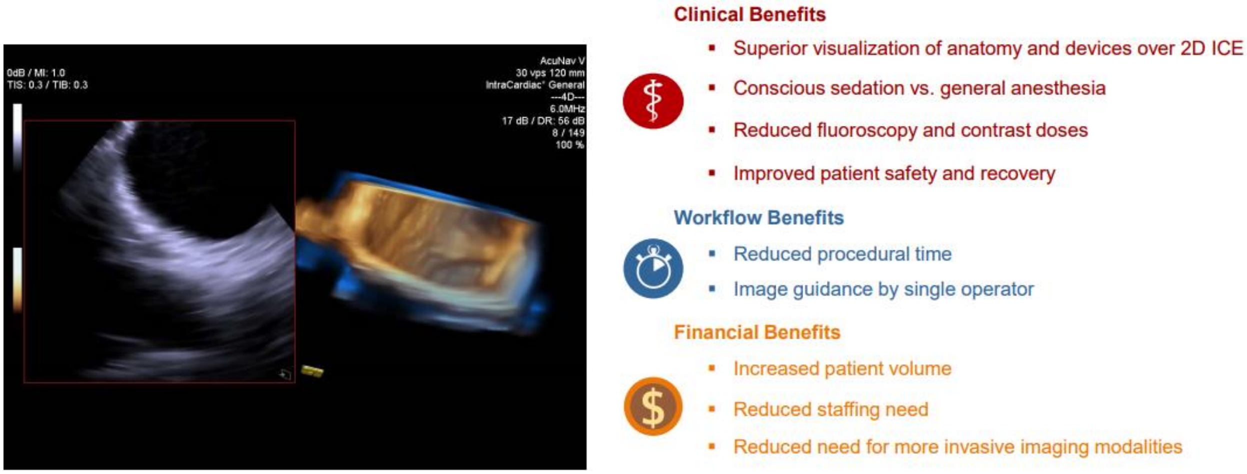


Figure 1.8. AcuNav real-time volume ICE image of heart [31]

In order to generate a 3D ultrasound image with sufficient dynamic range, high-density 2D imaging arrays are required. Wildes et al. [32] have recently developed a piezoelectric 2D array transducer with integrated transmit/receive application-specific integrated circuit (ASIC) for real-time 3D intracardiac echocardiography (4D ICE) applications. A 10-Fr 3D volumetric ICE imaging catheter with an area of about 2.5×6.6-mm^2 with over 800 2D arrays are connected to the imaging unit with 88 cables. Piezoelectric transducers are required several extra layers for proper operation including matching, dematching and backing layers. In order to realize the piezoelectric arrays within the tight constraints of the catheter, a stack of ASIC, acoustic layers, transducer and catheter flex circuits is required that causes the manufacturing process extremely challenging. Capacitive micromachined ultrasound transducers (CMUTs) can be an alternative for piezoelectric transducers and the challenging Piezo-on-ASIC process can be replaced by CMUT-on-CMOS (figure 1.9). By using CMUT-on-CMOS technique, a CMUT array can be fabricated over a custom design CMOS chip with surface micromachining techniques that makes the entire manufacturing process cheaper and easier.

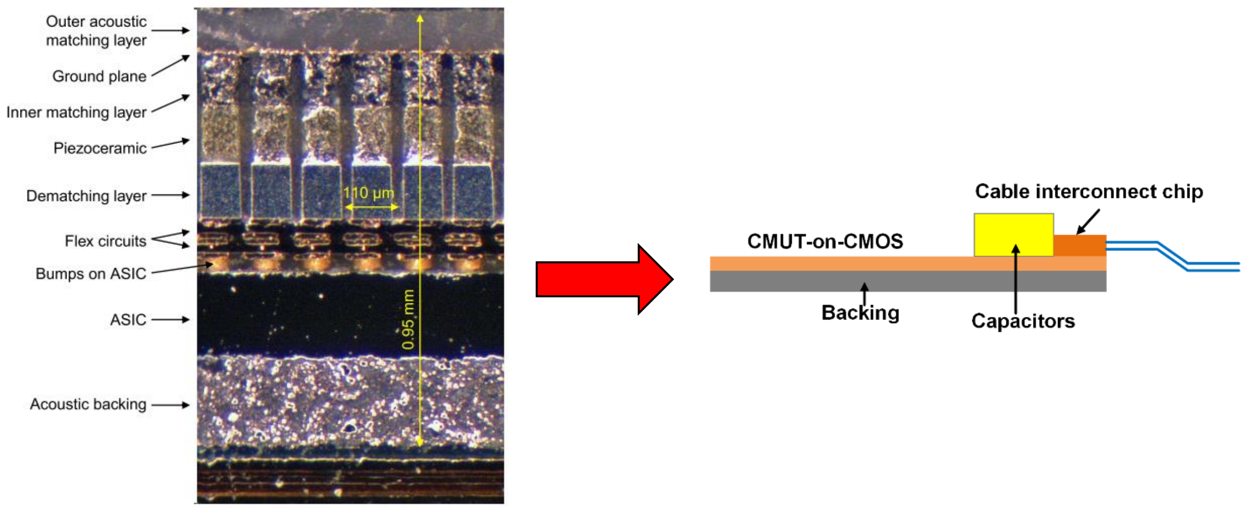


Figure 1.9. a) Cross section of the complicated state-of-art piezo-on-ASIC 2D array [32] b) Our CMUT-on-CMOS single chip solution.

1.2 Ultrasound Transducer Technologies for ICE

Piezoelectrics are the most common materials used in transducer technology for commercial ultrasound catheters [33]. Due to high relative permittivity, bulk-piezo materials are usually able to withstand relatively high voltage (>300-V) and as a result generate high pressure in transmit mode [34]. Piezoelectric manufacturing by the mechanical dicing method is relatively easy for catheters that are in the range of a millimeter and up to 50-micrometer size, however, for high frequency transducers that work around 20-40-MHz center frequency, mechanical dicing is not suitable and dry etching can be more efficient. Due to impedance mismatch between piezoelectric and surrounding medium (equation 1.1), a matching layer is required to improve acoustic performance of transducer [35, 36]. There are several limitations for a piezoelectric transducer array manufacturing: miniaturization in large arrays and front-end electronics integration.

Micromachined ultrasound transducers (MUTs) are membrane-based transducers that can be easily fabricated with current micromachining techniques and integrated with CMOS technology.

Capacitive micromachined ultrasound transducers (CMUTs) can be an alternative for piezoelectric transducers on the tip of a catheter and especially for 2D arrays that high-density imaging arrays are required. Although there are no commercial 3D volumetric ICE arrays available, it has been a hot research topic. Nikoozadeh et al. [37, 38] have developed a 12-Fr (4-mm) forward looking ICE catheter based on CMUT technology. The development of low temperature surface micromachining and wafer bonding methods have facilitated monolithic integration with CMOS electronics that is critical for CMUT-ASIC integration in catheter-based applications.

The aim of this research is to demonstrate a CMUT transducer suitable for ICE imaging. To realize the CMUT arrays for ICE catheter, we need an efficient and reliable CMUT array capable of generating high output pressure in Tx mode and high sensitivity in Rx mode. We also need to integrate our CMUT arrays with a custom design ASIC for Tx-Rx operation and data collection. For both 1D and 2D array, we demonstrated reliable and efficient CMUT transducers that occupy $2.6\times11\text{-mm}^2$ and can fit in the catheter size of 9-F (<3-mm).

In this research, we first developed a new method to analyze the CMUT's performance in large signal operation - Chapter 2 [44]. We propose a new energy approach to calculate the output mechanical energy of the CMUTs and defined energy conversion ratio (ECR) as a new method for CMUT performance evaluation in both small and large signal regime. We then use our method to evaluate the efficiency of the CMUT arrays in AC only and DC biased operation. We qualitatively validate our approach with some measurements.

In chapter 3, we first describe a reliable low temperature CMUT fabrication process where a lift-off step is introduced into the process flow [45]. This step deposits a thick dielectric layer between the top and bottom electrode, except for the regions where there is a CMUT membrane. We fabricate a 1D ICE array with 64 elements using this modified technique. We present electrical and acoustic measurements of the arrays that show functionality with reduced parasitic capacitance. Finally, we compare the reliability of the devices with and without the lift-off step to demonstrate the reliability improvement.

In chapter 4, the design and simulation of both 1D and 2D CMUT arrays suitable for ICE catheters are discussed. We employ a system level design approach to determine the number of elements in our 2D arrays. The geometry of the arrays is optimized for a 60-V pulse. The simulation is in very good agreement with measurements. Finally, we discuss CMUT noise level and angular response.

In chapter 5, we use our custom designed CMOS electronics to monolithically integrate our CMUT arrays to CMOS chips. We include several designs in our CMUT-on-CMOS wafer. The electrical and acoustic measurement for 1D and 2D CMUT-on-CMOS arrays are presented.

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CHAPTER2. ENERGY CONVERSION ANALYSIS OF CMUT DURING LARGE SIGNAL OPERATION

2.1.1 CMUT Basic Principles

A capacitive micromachined ultrasound transducer (CMUT) is a movable membrane that is actuated with applied electrostatic force (figure 2.1). A CMUT membrane consists of a top and bottom electrode with an isolation layer in between to ensure two elements do not short during large membrane displacement.

2.1.2 CMUT Operation and Parallel Plate Model

CMUT has linear mechanisms for small amplitude of vibration, and without considering nonlinearity, any electroacoustic transducer can be modeled as a vibrator; with mass (m), stiffness (k), and resistance (b) (figure 2.1-b), connected to a source of electrical energy that provides force (equation 2.1).

$$m\ddot{x} + b\dot{x} + kx = F_{electrostatic} \qquad Eq. 2.1$$

In static operation, derivative of displacement is 0, therefore equation 2.1 rewritten as:

$$kx = F_{electrostatic} \qquad Eq. 2.2$$

Equation 2.2 sets the electrostatic force equal to the mechanical force (kx) in static operation. It can be shown after a certain voltage the electrostatic force is always greater than mechanical force. This voltage is called collapse voltage that causes membrane permanent deflection.

In a simple parallel plate model, the force is the derivative of the electrostatic energy and by

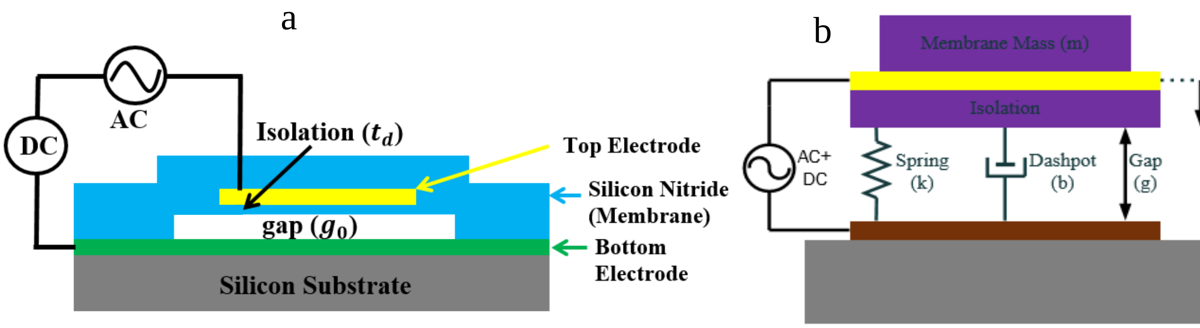

Fig. 2.1. a) CMUT general schematic and bottom-top electrode location where electrostatic force is made in between. b) A CMUT membrane can be modeled as mass (m), stiffness (k), and resistance (b) connected to an electrical source.

Ignoring dielectric thickness, the electrostatic energy (E_{es}) is calculated as given:

$$E_{es} = \frac{1}{2}\frac{\mathcal{E}_0 A}{g_0 - x}V^2 \qquad Eq.2.3$$

Where $\mathcal{E}_0$ is the permittivity of free space (F.m^{-1}); A is the area, x is the displacement, g_0 is the initial gap of the CMUT and V is the voltage over the top-bottom electrodes. The electrostatic force is further calculated in equation 2.4:

$$F_{ES} = \frac{dE_{es}}{dx} = -\frac{\varepsilon_0 A}{2(g_0 - x)^2}V^2 \qquad Eq.2.4$$

Considering DC voltage applied over top electrode while bottom electrode is grounded in the static operation, equation 2.2 can be written as:

$$kx = \frac{\mathcal{E}_0 A V^2}{2(g_0 - x)^2} \qquad \begin{cases} x_{collapse} = \dfrac{g_0}{3} \\[2ex] V_{collapse} = \sqrt{\dfrac{8Kg_0^3}{27\mathcal{E}_0 A}} \end{cases} \qquad Eq.2.5$$

Equation 2.5 explains the collapse condition under DC voltage operation. The membrane deflects 1/3 of the initial gap ($\frac{g_0}{3}$) and then permanently collapses ($x_{collapse}$). Although CMUTs can operate in collapse mode, the applications discussed in this thesis are in non-collapse mode. An isolation layer is required to ensure the electrodes will not short to each other during non-collapse operation. Initial gap (g_0) is replaced with effective gap (g_{eff}), when dielectric with thickness (t) and relative permittivity ($\mathcal{E}_r$) is added as an isolation layer. g_{eff} is defined as given:

$$g_{eff}(t) = g_0 + \frac{t}{\mathcal{E}_r} \qquad Eq. 2.6$$

and the modified collapsed displacement is calculated in equation 2.7:

$$x_{collapse} = \frac{1}{3} g_{eff} \qquad Eq. 2.7$$

Usually the CMUT is directly driven with a voltage $v(t)$ that includes both DC and AC components (figure 2.1 –a), i.e.,

$$v(t) = v_{DC} + v_{AC}\cos(\omega t) \qquad Eq. 2.8$$

From equation 2.4, the electrostatic force is related to input voltage square, therefore, output force generates second harmonic content:

$$v(t)^{\,2} = (v_{DC}{}^2 + v_{AC}{}^2/2) + 2v_{DC}v_{AC}\cos(\omega t) + (v_{AC}{}^2/2)\cos(2\omega t) \qquad Eq. 2.9$$

The ratio of second and first harmonic content is an important factor to determine the effect of 2ω component. In small signal regime that v_{AC} is significantly smaller than v_{DC}, the second harmonic can be ignored and CMUT can be idealized as a linear transducer. In case of not having DC voltage applied, the operation is called AC only operation and Eqn. 2.9 is rewritten as:

$$v(t)^2 = \frac{{v_{AC}}^2}{2} + \frac{{v_{AC}}^2}{2}\cos(2(\omega)t) \qquad Eq. 2.10$$

2.1.3 CMUT Small Signal Model

A CMUT is modeled with a lumped element circuit that can evaluate the small signal behavior of CMUT in both transmit and receive operation. The mason equivalent circuit is based on a two-port network modeling that is discussed in detail in Mason and Hunt books [1, 2] (figure 2.2). An electrostatic transducer can be modeled in 3 parts; electrical, mechanical and acoustical part. In electrical part, C_0 is the initial capacitance of the CMUT when there is no deflection and C_p is the parasitic capacitance of the CMUT that can be from bondpads, fabrication imperfection and inevitable top-bottom electrode overlap. $-C_0$ is the term used for spring softening that reduces the static stiffness of the membrane. In fact, the electrical field that applies over the top-bottom electrode changes the spring constant of the membrane [2, 3]. The softened spring is calculated as:

$$k_{softened} = k - \frac{A\mathcal{E}_0}{(g_0 - x)^3}V^2 \qquad Eq. 2.11$$

Transformer ratio (n) that is defined as the force at the mechanical domain to the voltage at the electrical domain with units of (Newton/Volt) is an important characteristic of a transducer.

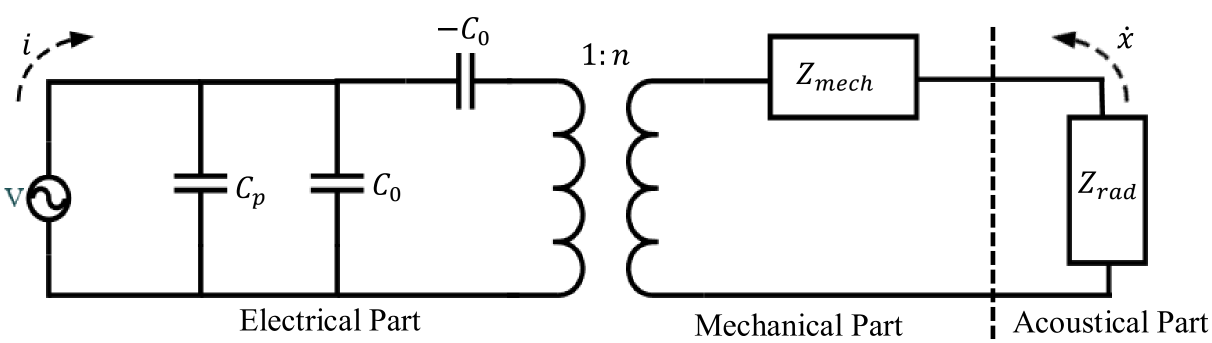

Fig. 2.2. a) CMUT small signal model in transmit mode. The equivalent circuit consists of passive elements and a transformer ratio links electrical and mechanical domain.

Electromechanical transfer ratio is an important parameter for CMUT receive mode when the sensitivity plays a key role in transducer performance. n is calculated by dividing mechanical force to the input voltage or mechanical plate velocity divided by the input electrical current and can be calculated as given:

$$n = \frac{F_{mechancial}}{V_{electrical}} = \frac{A\mathcal{E}_0}{(g_{eff}-x)^2} V_{DC} \qquad Eq. 2.12$$

From equation 2.12, it can be concluded that for a CMUT with a fixed geometry and dielectric material, n is a function of applied DC bias, and since CMUT cannot be biased more than its collapse voltage, n_{max} is calculated as given ($V_{DC} = V_{col}$) [4]:

$$n_{max} = \frac{A\mathcal{E}_0}{(g_{eff}-x)^2} V_{col} = \sqrt{\frac{3k\mathcal{E}_0 A}{2g_{eff}}} \qquad Eq. 2.13$$

2.1.4 Mechanical and Acoustical Domain Parameters

In figure 2.2, mechanical domain demonstrates the mechanical impedance of the vibrating plate (Z_{mech}). Typically, the thickness of the CMUT membrane is significantly lower than its lateral size (1:20 or less); therefore thin plate approximation method is used to determine the behavior of the membrane vibration [5]. The mechanical impedance of the CMUT using this approach has been calculated in Nikoozadeh thesis in detail [6]. The first resonance frequency for rectangular and circular plate are calculated as given:

$$f_{rectangular} = 0.2570\sqrt{\frac{E}{\rho(1-\nu^2)}}\frac{t}{a^2} \qquad Eq. 2.14$$

$$f_{circular} = 0.4694\sqrt{\frac{E}{\rho(1-\nu^2)}}\frac{t}{a^2} \qquad Eq. 2.15$$

where E, ν and ρ are the membrane Young's modulus, Poisson's ratio and density.

t is the plate thickness and a is the lateral dimension of the plate; diameter of the circular and width of the rectangular membrane. Form equation 2.14 and 2.15, it can be seen that CMUT's resonance frequency depends on the ratio of $t/_{a^2}$ and this ratio is an important CMUT design parameter. Depending on the application, for example 5-15-MHz for ICE and 20-40-MHz for IVUS, the lateral size (t) and thickness (a) can be chosen to set the desired working frequency.

The acoustical part of the CMUT model (figure 2.2) is basically the model of the surrounding medium and its interaction with CMUT vibration. Typically the force over the CMUT has two components; external force (F_e) and reaction force (F_{rad}) [7]. External force is the sound force coming from an acoustic source when the CMUT operates in receive mode. The reaction force denotes the interaction between medium and the vibration of the membrane. Considering the uniformity of the surface motion at all points ($\dot{x}$), the reaction force is calculated as given [7]:

$$F_{rad} = -\iint p(\vec{r})\, dS \qquad Eq. 2.16$$

Where $p(\vec{r})$ is the pressure in the direction of $\vec{r}$, and negative sign is due to the reactionary force of the medium. The radiation impedance (Z_{rad}) is further defined as equation 2.17:

$$Z_{rad} = -\frac{F_{rad}}{\dot{x}} = R_{rad} + jX_{rad} \qquad Eq. 2.17$$

Where R_{rad} and X_{rad} are the transducer radiation resistance and reactance. The radiated output energy depends on the efficiency of the CMUT operation. Therefore, the mechanical to acoustical efficiency (mechanoacoustical) is a key parameter in CMUT design optimization and can be obtained by the following equation [7]:

$$\eta_{ma} = \frac{acoustical\ energy}{mechanical\ energy} = \frac{R_{rad}}{R_{rad} + R_{mech}} = \frac{1}{1 + \frac{R_{mech}}{R_{rad}}} \qquad Eq. 2.18$$

Where R_{mech} is the real part of the membrane mechanical impedance (Z_{mech}). From 2.18, one can conclude that the higher R_{rad} results in higher efficiency, hence, one of the important design parameter for CMUT is to maximize the R_{rad}.

The analytical form of the radiation impedance for a baffled circular piston (a is the radius) is calculated by Kinsler et al. [8] and demonstrated in figure 2.3. From figure 2.3, it is inferred that a larger transducer ($2ka > 4 - \ k \ is \ wavenumber$) will have a higher acoustic resistance however, the size of a transducer is usually limited by the application and the number of required arrays at a certain operation bandwidth.

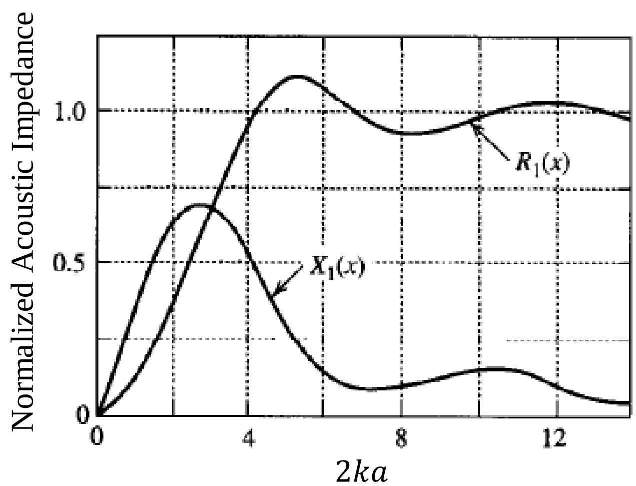

Fig. 2.3. Normalized acoustic Impedance to characteristics impedance of the medium for a circular piston with radius a and wavenumber k [8].

2.1.5 CMUT Coupling Coefficient

Electromechanical coupling coefficient is frequently used to evaluate transducer performance [2]. The definitions used to calculate and measure this coefficient for CMUTs follow the usual small signal approximation which assumes that the energy conversion occurs at the input frequency and the coupling coefficient is independent of the drive level [2, 9, 10]. With these constraints, the coupling coefficient for a CMUT can be obtained by capacitance and resonance frequency measurements, similar to piezoelectric transducers [11, 12]. Coupling coefficient (κ^2) is a dimensionless measure of a transducer performance. In CMUT, it is defined as the ratio of output mechanical energy to the total input energy ($w_{total} = w_{mech} + w_{electric}$).

$$\kappa_T{}^2 = \frac{w_{mech}}{w_{mech} + w_{electric}} \qquad Eq. 2.19$$

The concept of coupling coefficient is defined for static or quasi-static operations and can be derived from several approaches [7]. Quasi-static operation implies low frequency condition at which the frequency dependent terms in impedance – related to kinetic energy calculations- are ignored [7]. The concept was first defined by Hunt that is based on membrane stiffness (k) definition for electrostatic transducers [2] (equation 2.20). When there is no electrical excitation, κ^2 is 0, and in collapse situation where $k_{softened} \to 0$, κ^2 becomes 1.

$$k_{softened} = k(1 - \kappa^2) \qquad Eq. 2.20$$

Another method for κ^2 calculation is the capacitance method that by neglecting frequency dependent terms in CUMT quasi-static operation, can be written as:

$$\kappa_T{}^2 = 1 - \frac{C_{static}}{C_{free}} \qquad Eq. 2.21.a$$

$$C_{static} = \frac{Q(x)}{V}\ ; x_{DC}\ , V_{DC} \qquad Eq. 2.21.b$$

$$C_{free} = \frac{dQ(x)}{dV}\ ; x_{DC}\ , V_{DC} \qquad Eq. 2.21.c$$

Equation 2.21-a can also be re-written as equation 2.22, referring to stored energy ($Eq. 2.22$):

$$\kappa_T{}^2 = \frac{\frac{1}{2}C_{free}\ v^2 - \frac{1}{2}C_{static}\ v^2}{\frac{1}{2}C_{free}\ v^2} \qquad Eq. 2.22$$

As it is discussed in [7], the denominator is the total input energy from electrical domain, and numerator is the difference between total energy and the clamped mechanical energy - when there is no electrical excitation. This term is called motional energy that is linked to the concept of motional impedance. In general, the difference between clamped and free-to-move impedance is called motional impedance which determines the electromechanical coupling factor of a CMUT.

Measuring coupling coefficient with capacitance method in clamp and free states are not feasible. Hunt [2] explained how to relate resonance frequency of an electrostatic transducer to stiffness and capacitance in small signal lumped model. The alternative definition can be obtained as:

$$\kappa_T{}^2 = 1 - \left(\frac{f_a}{f_r}\right)^2 \qquad Eq. 2.23$$

Where f_a and f_r are resonance and anti-resonance frequency of a CMUT.

2.1.6 CMUT Operation and Non-linear Model

In order to analyze large signal operation of CMUT, a model which takes into account the nonlinear electrostatic forces with large membrane displacements is employed while the acoustic interactions are modeled in linear regime [13]. In the transmit system Simulink model shown in figure 2.4, the CMUT is considered as linear time-varying capacitor $C(t) = C_m(t) + C_P$, where $C_m(t)$ is the moving time varying part of the capacitor and C_P is the static, non moving part of the capacitance. Transmit circuitry is modeled with the source impedance (Z_s) assuming the interface circuit is linear within the operation range [14].

Given the source voltage v_S(t), which includes both DC and AC components, the instantaneous voltage, $v(t)$ and current, $i(t)$ on the CMUT is given as in Eqn. 2.24.

$$v(t) = v_S(t) - i(t) * \mathcal{F}^{-1}\{Z_S(\omega)\}$$

Eqn. 2.24

$$i(t) = \frac{dQ(t)}{dt} = \frac{dv(t)(C_m(t) + C_p)}{dt}$$

where $\mathcal{F}^{-1}\{Z_S(\omega)\}$ is the inverse Fourier transform of the source impedance, $Q(t)$ is the charge on the CMUT capacitance $C(t)$. The impact of higher order membrane modes are included by dividing the moving electrode into patches with related electrostatic force distribution. The total capacitance is found by adding parallel plate approximated capacitance from each patch, $C_i(t)$.

$$C(t) = \sum_i C_{mi}(t) + C_p = \sum_i \frac{\varepsilon_o Ai}{g_0 + u_i(t)} + C_p \qquad \textit{Eqn. 2.25}$$

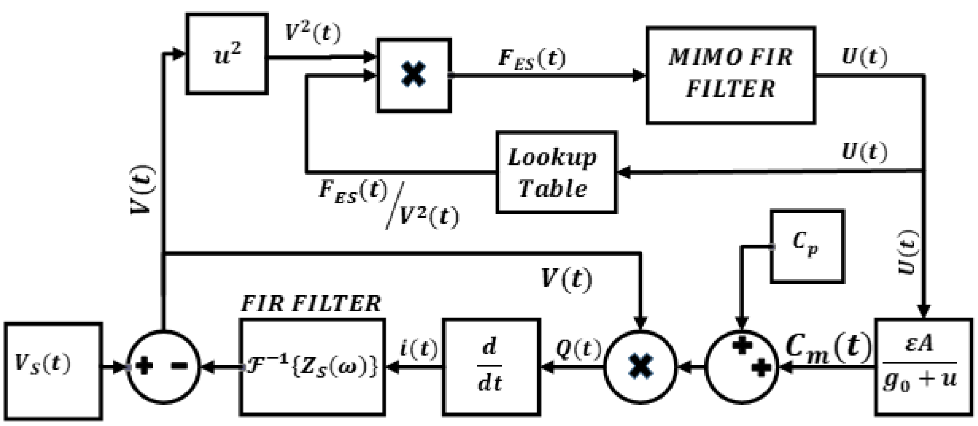

Fig. 2.4.a is the Simulink model of the calculation method [13].

Here the A_i is the area of the i[th] patch, ε_o is the permititivity, g_0 is the initial effective gap and $u_i(t)$ is the displacement of the ith patch. To ensure the CMUT operates in non-collapse mode, membrane displacements are limited by the gap height which controlled by a conditional command. The MIMO FIR filter block in Simulink model describes the acoustic response of each patch in accordance with the electrostatic force (F_{ES}) and patch displacement vectors ($U(t)$). The surface of the CMUT is meshed by the boundary element method (BEM) and this MIMO FIR block is derived by solving the system of force equations $G(\omega)$ on each node [14]. $G(\omega)$ is the matrix relates stiffness (K), mass (M) and fluid coupling ($Z_r(\omega)$) matrices given by Eqn. 2.26:

$$G(\omega) = K - \omega^2 M + j\omega(Z_r(\omega) + b) \qquad \textit{Eqn. 2.26}$$

In order to model the mechanical loss in the CMUT membrane structure, the damping proportional to the velocity, b, is added to fluid coupling. Since the electrical source is the only source of energy input, given $i(t)$ and $v(t)$, the total instantaneous power input to the CMUT, $p(t)$, can be calculated by:

$$p(t) = i(t)v(t) \qquad \textit{Eqn. 2.27}$$

This expression can be integrated to find the total electrical input energy (E_{total}) that is defined as:

$$E_{total} = \int p(t)dt = \int i(t)v(t)dt \qquad \textit{Eqn. 2.28}$$

This energy level is the total input energy used in the energy definition of coupling coefficient shown in the denominator of the equation 2.19, as the electrical source is the only energy source.

2.2 ECR Calculation

The critical information required for energy based coupling coefficient calculation for large signal operation is the mechanical energy or work done by the input electrical energy. This is obtained by considering the CMUT as a linear time-varying capacitor, i.e. $q(t) = C(t)v(t)$, and separating the instantaneous power input to the system into two components. The circuit delivers energy to the CMUT capacitor at the rate of $p(t)$ as in equation 2.27. While some of this energy is stored as electrostatic energy $E_c(t)$ in the capacitance, the remainder of the energy is the mechanical work done [15]. This is clearly seen in the following Eqn. 2.29.

$$p(t) = i(t)v(t) = \frac{dq}{dt} \; v(t) \xRightarrow{q(t)=C(t)v(t)}$$

$$= \frac{d\big(C(t)v(t)\big)}{dt} v(t) = \dot{C}(t)v(t)^2 + C(t)\dot{v}(t)v(t)$$

$$= \frac{1}{2}\dot{C}(t)v(t)^2 + (\frac{1}{2}C(\dot{t})v(t)^2 + C(t)\dot{v}(t)v(t))$$

$$= \frac{1}{2}\dot{C}(t)v(t)^2 + \frac{d}{dt}(\frac{1}{2}C(t)v(t)^2)$$

$$= \frac{1}{2}C(\dot{t})v(t)^2 + \frac{dE_c}{dt} \qquad \text{Eqn. 2.29}$$

We assert the difference between $p(t)$ and $\frac{dE_c}{dt}$, $(\frac{1}{2}C(\dot{t})v(t)^2)$, $\dot{C}(t)$ denoting the time derivative of capacitance, is the instantaneous mechanical power input to the CMUT by the electrostatic forces in the capacitor. It is interesting to note that the unit of $\dot{C}(t)$ is mho, conductance unit which models the mechanical power as power lost in a resistor. By integrating this quantity, the mechanical energy the general energy based definition of coupling coefficient can be obtained for the CMUT. We denote this ratio as Energy Coupling Ratio (ECR) (equation 2.30) to prevent confusion with the regular coupling coefficient, which is valid only for linear small signal case.

$$ECR = \frac{Mechanical\ Energy}{(Mechanical+Electrical)\ Energy} = \frac{\int \frac{1}{2}\dot{c}(t)\ v(t)^2 dt}{\int i(t)v(t)dt} \qquad Eq. 2.30$$

In addition to handling large signal operation, ECR can be calculated for different membrane geometries for design optimization as the acoustic model of equation 2.26 allows for arbitrary K and M matrices [13]. Similarly, impact of parasitic capacitance C_p is inherently included in the total capacitance as in equation 2.25.

2.2.1 ECR Calculation Example

In order to observe how the CMUT variables related to ECR and ECR itself change over time during dynamic operation, an example calculation is performed on a CMUT with properties listed in table 1 and geometry shown in figure 2.5. Figure 2.6 shows the voltage, the average displacement of a CMUT membrane, corresponding current and time derivative of total capacitance for this single membrane. With these variables, one can calculate the instantaneous power input to the CMUT and the mechanical power dissipated, based on equations 2.27 and 2.29, respectively. Note that, for this particular case, no DC bias is applied to the CMUT membrane.

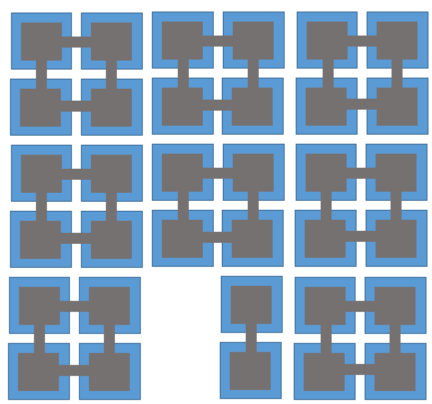

Figure 2.5. The array used in the simulation and discussed in table 1. The calculations are for the 4 center membranes and adjacent membranes can include array behavior including crosstalk in the simulation.

Table 2. CMUT Properties

Parameter	**Value**
Membrane size	46-µm * 46-µm
Electrode area	38-µm * 38-µm
Membrane thickness	2.25-µm
Device center frequency	9-MHz
Vacuum gap	95-nm
Dielectric relative permittivity	6.3
Si_xN_y isolation thickness	250-nm
No. of membrane	4
Collapse voltage (Vcol)	32 V
Membrane Poisson ratio	0.22
Membrane Young's Modulus	110e9-Pa
Membrane density	2200 kg/m^3

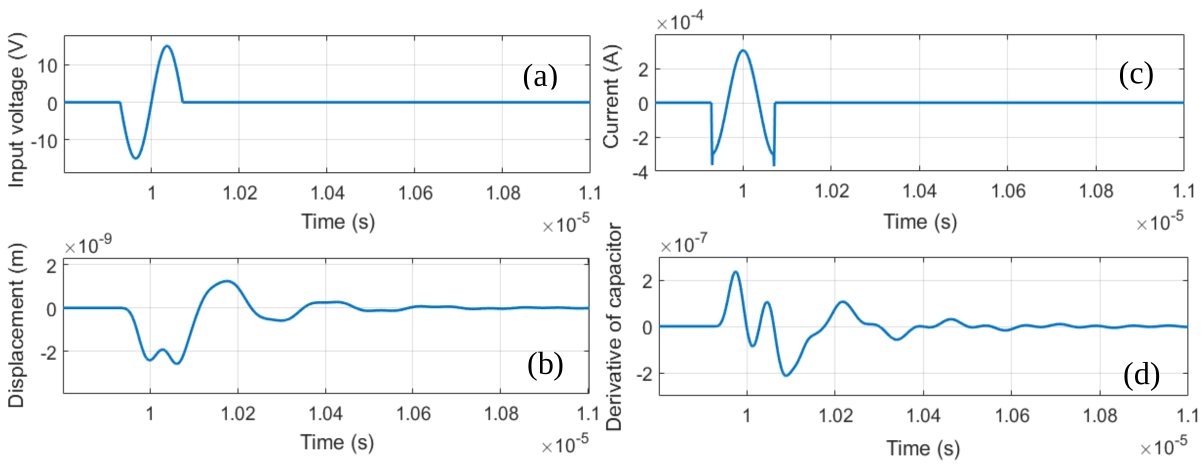

Figure 2.6. a) The input voltage over the CMUT. b) The membrane average displacement profile. c) The current generated by the CMUT. d) Derivative of the capacitance, which is used in the mechanical energy calculation.

The energy variables for ECR are then calculated by integrating instantaneous power, which can be performed both for transient pulsed operation as well as long tone burst, or close to CW operation, for any DC and AC bias combinations. Figure 2.7 shows a set of calculations in small signal regime for low and high coupling conditions, which depends on the applied DC bias. In Figure 2.7-a, the solid lines indicate the instantaneous input power whereas the dashed lines show the mechanical power in the CMUT for 20% (red) and 80% (blue) ECR. Note that, although the peak values of the input to mechanical power ratio seem very different, when the energy is calculated through integration to obtain ECR, it is seen that these ratios are indeed 80% and 20%. Also note that, with DC bias and small signal operation the ECR values are independent of time since the coupling coefficient is determined quasi-statically by the DC bias. Figure 2.7-c shows the same calculation as Figure 2.7-a but this time the CMUT is operated without DC bias by

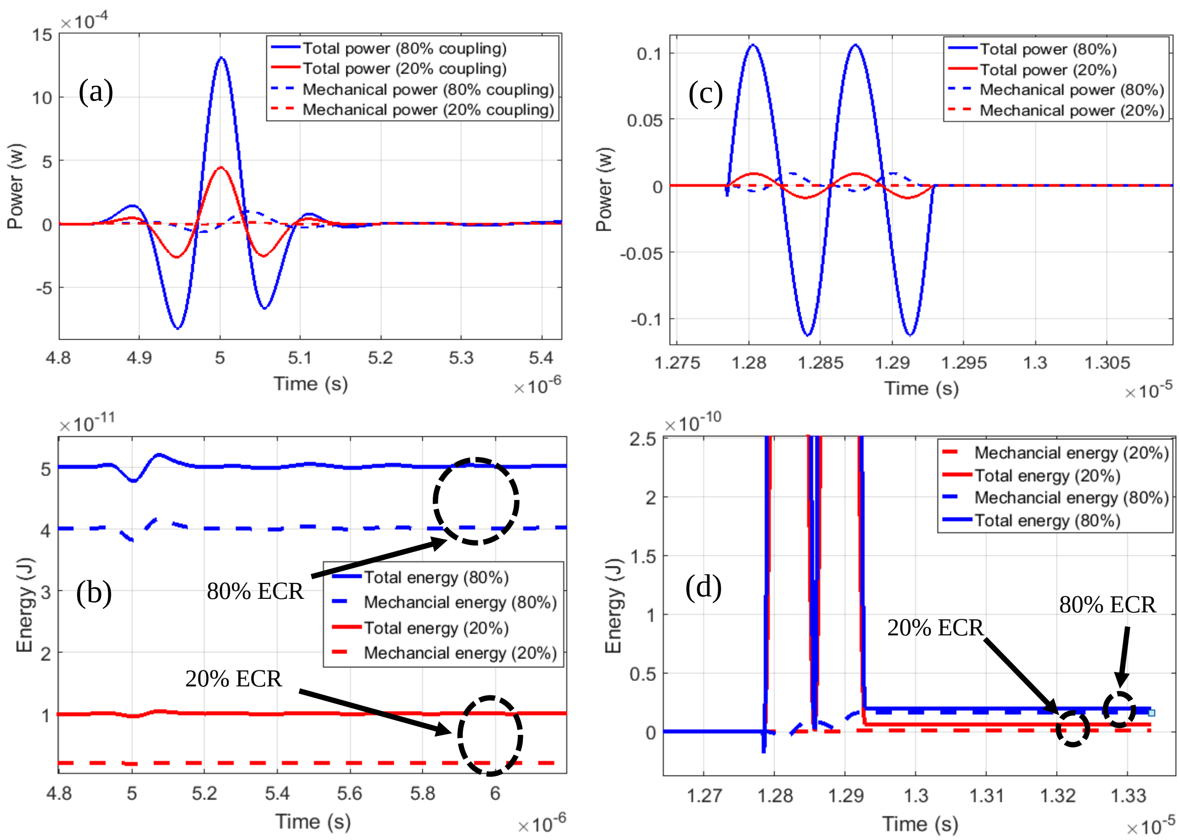

Figure 2.7. Small signal a) mechanical and total power and b) energy (power integral) variation over time. c) Large signal mechanical and total power and d) energy calculation (power integral) in AC only operation.

applying a large AC only signal. In this case, ECR is zero before the application of the input signal since there is no energy (stored or dynamically changing) on the CMUT before the input signal. However, ECR increases to 80% (blue) or 20% (red) depending on the input level, i.e. higher input level (blue) resulting in higher ECR. This is different from the small signal case, where ECR or coupling coefficient is determined by the DC bias but not the input level. Therefore, this example clearly illustrates the added capability of handling large signal operation of CMUTs with the proposed method.

Note that unlike small signal coupling coefficient which can be obtained assuming quasi-static operation [11], ECR is obtained through dynamic variables. Therefore, its frequency dependence needs to be considered. This frequency dependence is explored by applying 100-cycle tone burst signals calculating ECR in the 1-12-MHz range for the example CMUT with 9-MHz center frequency in immersion. Figure 2.8 shows the variation of ECR with frequency for large AC only signals for two cases, where V_{ac} = 0.4Vcol and V_{ac}=0.9Vcol. As explained in the equation 2.10, for AC only excitation cases a voltage signal at the half of the desired output frequency is applied to the CMUT. As expected, ECR values for higher AC signal cases are higher in the 80-90% range

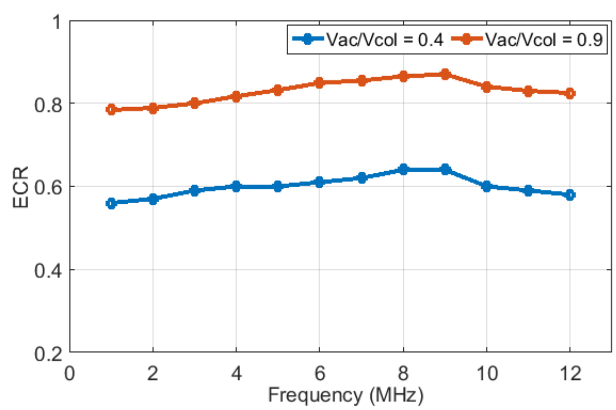

Figure 2.8. ECR shows relatively similar values in different frequencies where Vac/Vcol is set to 0.4 and 0.9.

as compared to about 60%, with a maximum around the first order mode resonance frequency of the CMUT membrane. More importantly, the variation of ECR in the whole 1-12-MHz range is small, indicating that ECR can be used as a design guide for a broad range of frequencies. However, assuming that for high power applications like HIFU and ARFI the CMUT will be used around its resonance frequency, in the rest of this paper ECR is evaluated for the case where the output center frequency is around 9-MHz.

2.3 ECR Verification in Small Signal Operation

To test the validity of ECR as an equivalent to the coupling coefficient in the small signal regime, the CMUT coupling coefficient is calculated using resonance frequency and capacitance methods and compared to ECR as a function of DC bias. In this calculation, the center element shown in figure 2.5 is used with neighboring elements, so that the ECR calculation has the effects of acoustic crosstalk as well. The resonance frequency method is evaluated by obtaining the electrical impedance of the CMUT in air, and the capacitance is calculated, all using the same model. The results shown in figure 2.9 indicate that all three methods follow the same variation in the whole

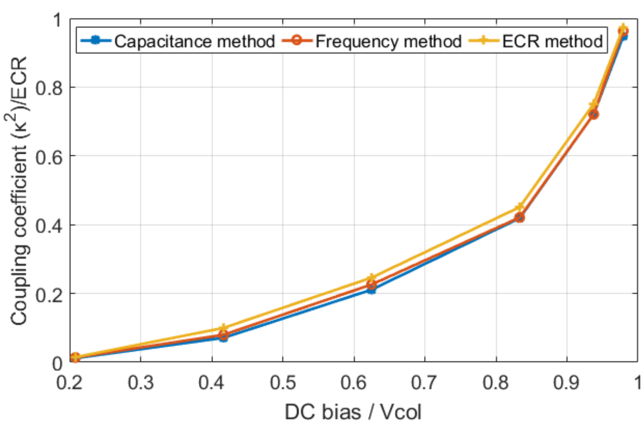

Figure 2.9. The coupling coefficients of CMUT versus DC bias which shows all three methods have the same value in small signal range.

voltage range, and validate that ECR is equivalent to small signal coupling coefficient.

2.4 Large Signal Operation

Unlike small signal based coupling coefficient, ECR enables one to explore the large signal energy conversion performance of CMUTs. An application of this approach is used to quantitatively compare CMUT operation for various DC and AC signal combinations. Figure 2.10 shows the variation of ECR as a function of AC signal amplitude normalized to the collapse voltage for different DC bias conditions. In these curves, high DC bias and low AC signals correspond to small signal operation. The curves are calculated until the instability due to collapse is encountered. In all cases increasing AC signal level increases the ECR with a limit approaching to 1. The interesting observation is that ECR values more than 0.9 can be achieved with AC only (no DC) or small DC bias when large AC signals exceeding the collapse voltage are applied to the CMUT. For example, ECR of 0.9 is obtained by AC only operation with 1.14Vcol peak amplitude at 4.5-MHz to obtain pressure output at 9-MHz. Noting that in this case the second harmonic level at 18-MHz is about -26-dB and the maximum pressure is 0.8dB higher than the DC biased operation, these results show that AC only operation can be quite efficient for large signal CMUT operation [16, 17] .

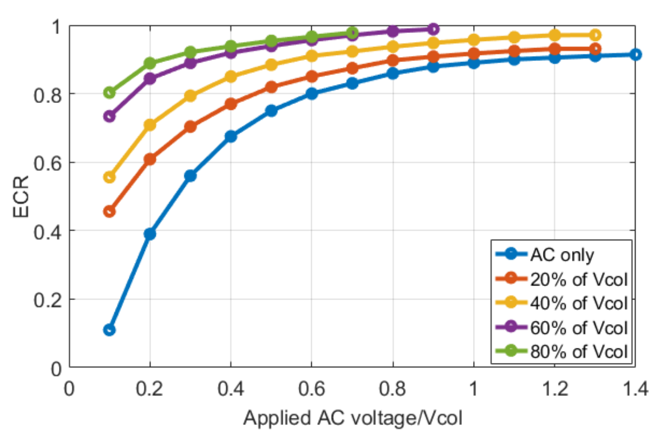

Figure 2.10. CMUT ECR vs. input signal amplitude.

2.4.1 *Impact of Parasitic Capacitance on ECR*

The impact of parasitic capacitance on ECR is also analyzed as shown figure 2.11, where the ECR is evaluated for both DC biased and AC only operation for different parasitic capacitance values. Similar to [11, 18] the ECR is reduced by parasitic capacitance. It is observed that parasitic capacitance in the order of the active capacitance of the CMUT causes a significant reduction of ECR and it has more impact on AC only operation as compared to DC biased operation.

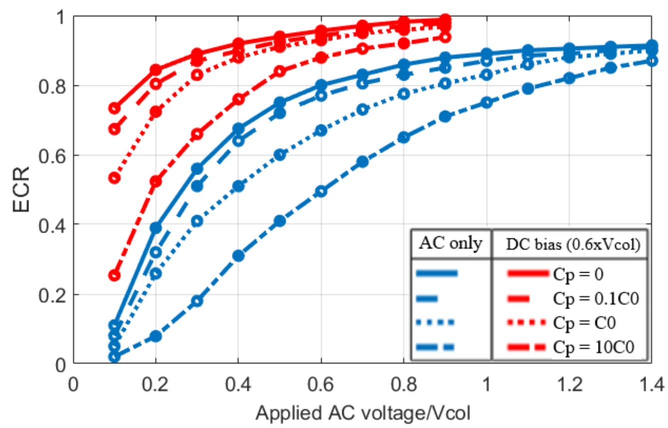

Figure 2.11. The effect of the parasitic capacitance on ECR in both AC only and DC bias operation.

2.5 ECR Application: Mass Loaded and Uniform Membrane Performance Comparison

Since the coupling coefficient of both piezoelectric transducers and CMUTs depend on the mechanical boundary conditions [19], a similar dependence is expected for ECR during large signal operation of the CMUT. To demonstrate this possibility to optimize CMUT performance, a uniform membrane CMUT is compared to a CMUT with non-uniform membrane in figure 2.12. The uniform membrane device has the parameters shown in Table 1, whereas the non-uniform membrane is designed to have similar lateral size (46-µm membrane pitch) and collapse voltage (32-V). Specifically, 1-µm thick silicon nitride is added over the top electrode area to achieve the similar collapse voltage and resonance frequency. The results show that non-uniform membrane improves the ECR for both DC biased and AC only operation as it provides more piston-like motion, with more improvement seen for AC only operation. Given that the ECR formulation allows for arbitrary membrane geometries, this approach can be used for ECR optimization for different electrode size and membrane geometries.

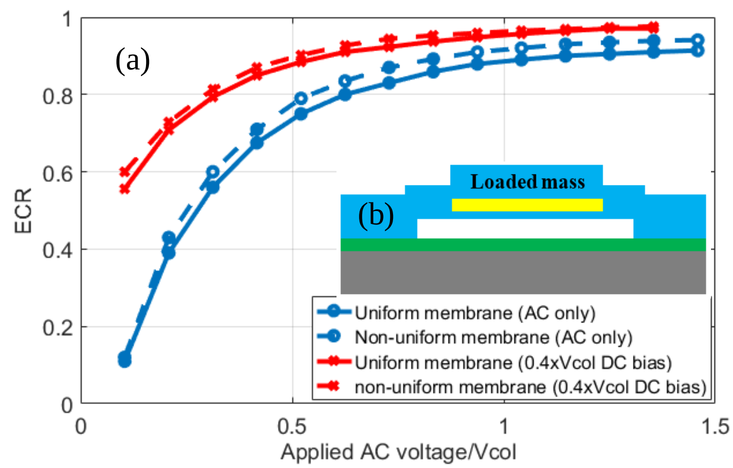

Figure 2.12-a) The ECR calculation for uniform and non-uniform membranes show non-uniform membrane improves the ECR in both DC biased and AC only operation. 2.12-b) The schematic of the mass loaded CMUT.

2.6 Experimental Validation of Mechanical Energy Output

The experimental validation of ECR method is not straightforward as measurement of $\dot{C}(t)$ is difficult given many sources of parasitic capacitances. Therefore, in order to qualitatively validate the ECR approach, it is considered that the mechanical energy output for a CMUT is proportional to the acoustic intensity, which can be measured through pressure in the far field [20]. For this purpose, a 4 membrane CMUT element is fabricated [21] as part of an array using the parameters of Table 1 as shown in figure 2.13. Then, pressure measurements in a water tank are performed and compared with model predictions for both AC only and DC biased operation. The pressure is measured by a hydrophone at a distance of 9-mm. The input signal is a 10-cycle burst with an amplitude of 1.1Vcol at $f_0/2$ for AC only operation and at f_0 with 0.6Vcol DC bias for DC biased operation (figure 2.14-a). Figure 2.14-b demonstrates the CMUT hydrophone voltage output

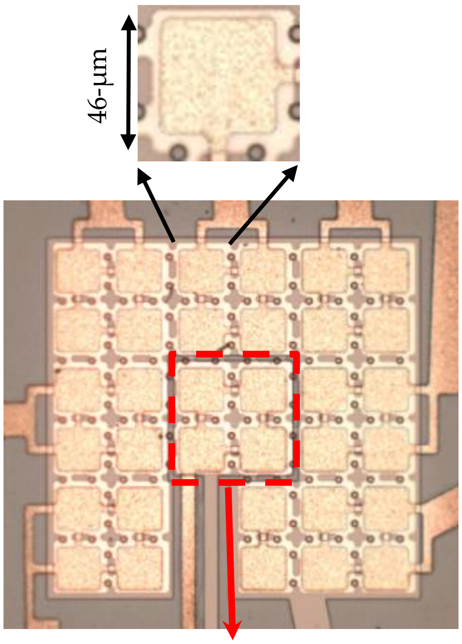

Figure 2.13. The optical image of the CMUT element that is used in ECR measurements – similar to figure 2.5 that used for simulation.

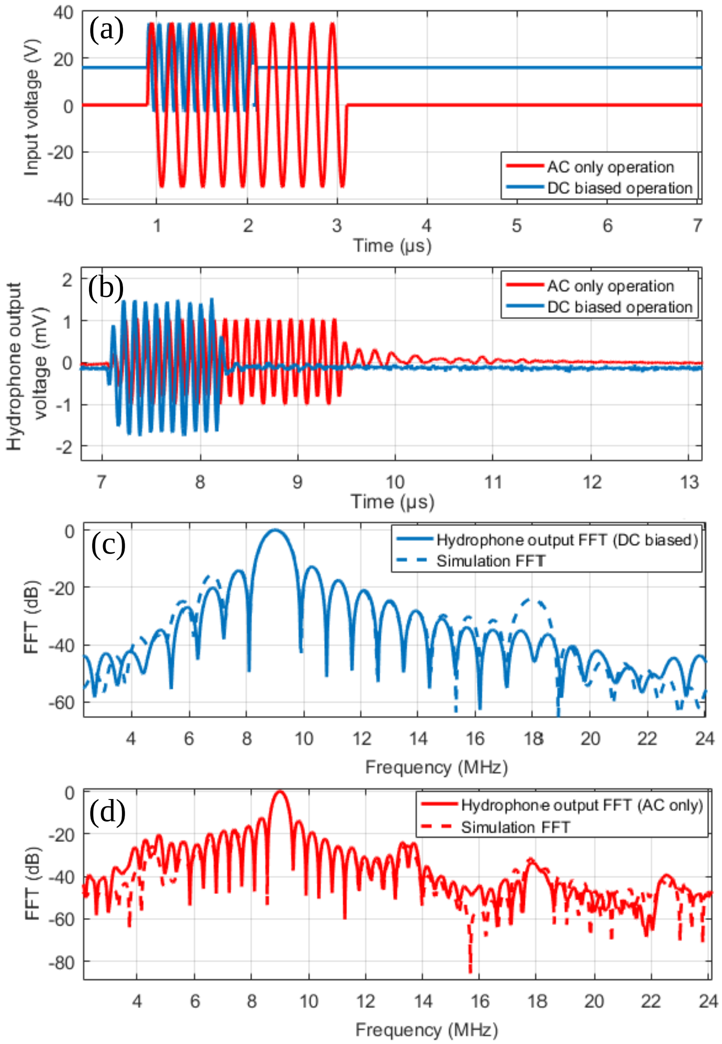

Figure 2.14.a) Hydrophone measurement of the CMUT. b) DC biased operation measurement and simulation show the output and input signals are at f_0 while, c) AC only operation shows the $f_0/2$ harmonic is -25-dB lower than f_0.

results – which were measured by HGL-1000 series hydrophone, ONDA Corp., Sunnyvale, CA 94089- and simulations with large signal model used for ECR calculations. Note that due to frequency doubling, the time domain signal for AC only operation continues twice as long as the DC biased operation (figure 2.14-a and b). In both operation modes, simulations are in agreement with the hydrophone output in time and frequency domain (figure 2.14-c and d).

To further verify the variation of mechanical energy calculation for ECR, the square of measured output pressure, which is proportional to the acoustic intensity, is qualitatively compared to variation of mechanical energy calculation for full range of AC only excitation voltages. The results shown in figure 2.15 show very similar variation where AC peak amplitude is increased up to 1.5Vcol, indicating that the mechanical energy obtained by the model is a good indication of actual acoustic output of the CMUT. Overall, these experimental results support the calculations leading to ECR evaluation for CMUT transmit performance in the large input signal range. Note that, although only non-collapsed mode is considered here, the basic behavior of collapsed mode CMUT is the same, i.e. linear time varying capacitor. Therefore, the ECR approach outlined here can be used to evaluate CMUT performance in collapsed more as well. Furthermore, it can be used to devise optimized transmit pulse signals for higher efficiency pulses for imaging applications.

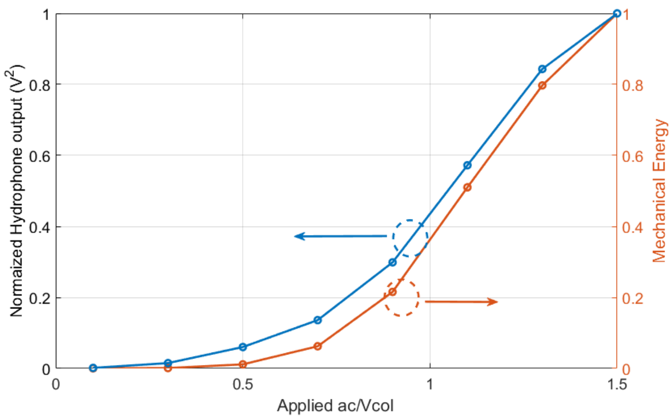

Figure 2.15. Normalized pressure square (left axis) and mechanical energy calculation (right axis) Vs. AC amplitude in AC only operation.

In conclusion, a large signal CMUT model can be used in conjunction with the energy definition of electromechanical coupling coefficient to determine a parameter called ECR, to quantify efficiency of CMUTs in both small and large signal operation. The model predictions compared with experimental results in the large signal regime show the validity of the model and the mechanical energy calculations for acoustic output of the CMUT. The results indicate that DC bias is not a requirement for efficient large signal CMUT operation. By applying AC only signals at the half of the operating frequency, high power operation with high efficiency (ECR = 0.9) is possible potentially reducing the charging problems. The ECR concept also enables one to evaluate impact of parasitic capacitance and CMUT membrane design on the large signal operation performance.

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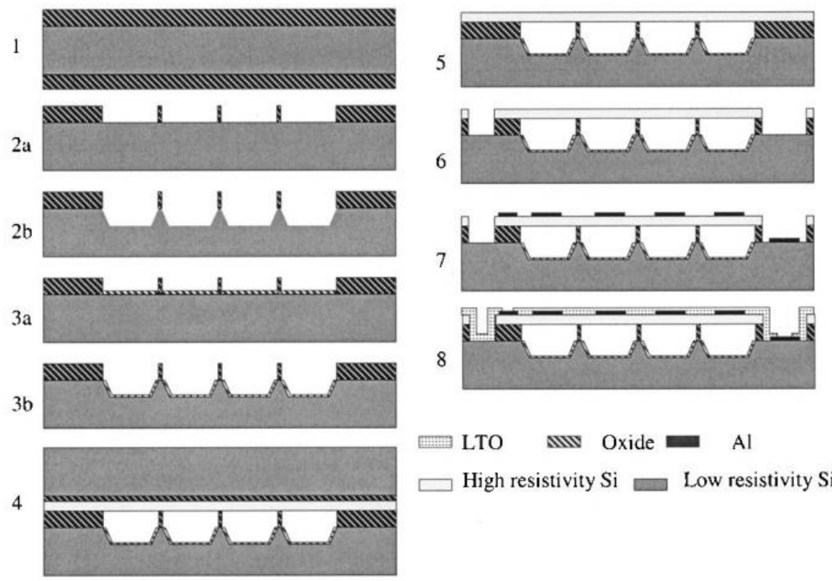
CAPTER 3. RELIABLE LOW TEMPERATURE CMUT FABRICATION

3.1 CMUT Fabrication Methods

A significant premise of the capacitive micromachined ultrasound transducers (CMUTs) is electronics integration. Monolithic integration of CMUTs with CMOS electronics provides ultimately compact imaging systems where significant functionality of the front-end electronics can be realized right under the CMUT imaging array, practically eliminating parasitic capacitance to achieve near ideal signal to noise performance [1, 2, 3]. This enables single chip systems for high frequency applications like intravascular ultrasound (IVUS) imaging where the array elements have sub pF capacitances [4]. The fabrication process temperature is the key for CMUT-ASIC monolithic integration. Typically, CMUT arrays are fabricated with 2 different approaches; wafer boding and sacrificial release (Figure 3.1). The difference between two methods is the cavity definition step. In the wafer bonding approach, the cavity and membrane are fabricated on different wafers and then bonded to form the CMUT while in sacrificial release method a sacrificial layer is etched at a later step and released the membrane. Silicon bonding methods usually requires surface preparation including non-CMOS compatible chemicals usage such as BOE and KOH and high temperature material deposition and annealing. Although, low temperature wafer bonding [5, 6] is demonstrated, sacrificial layer based processes are also widely used [3, 7, 8, 9]. Sacrificial layer process does not need large areas for reliable bonding which can reduce the active area of the transducer element, and hence can be especially suitable for high frequency applications with smaller lateral membrane dimensions. In sacrificial release method, silicon micromachining including deposition, dry and wet etching can be done in low temperature results in CMOS compatible fabrication process.

a



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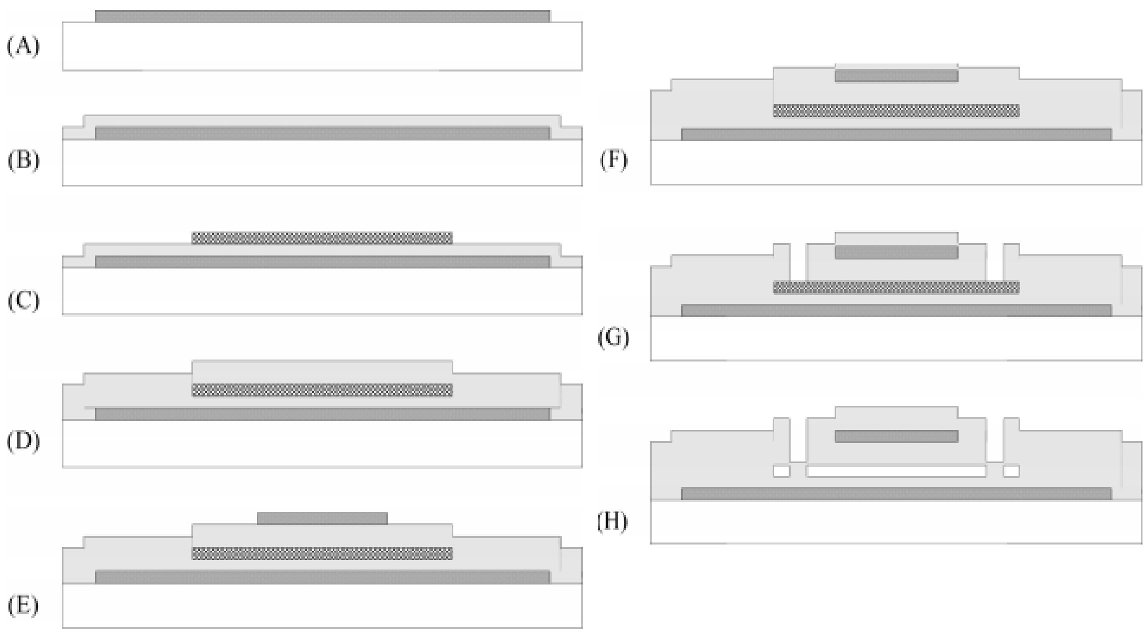


Fig. 3.1. a) CMUT fabrication using wafer bonding technique. Thermal oxidation and silicon etch define the cavity [31], b) CMUT fabrication steps using sacrificial release technique. A sacrificial layer is deposited and then released to form the membrane [32].

3.2.1 Improved Low Temperature CMUT Fabrication Process and Motivation

The cross section of the typical CMUT fabricated using a sacrificial layer process is shown in Figure 3.2-a. In this process, a thin layer of dielectric separates the top electrode (TE) and the bottom electrode (BE) over the vacuum gap. CMUT efficiency depends on a high electric field over a thin vacuum gap and a dielectric isolation layer. Ideally, this high electric field should only exist over the membrane of the CMUT vibrating over the vacuum gap, but electrical connections between the membranes also pass over thin dielectric isolation layers. The resulting high fields on the thin isolation layer cause charging [10], dielectric breakdown and reduces the CMUT reliability. Furthermore, it increases the parasitic capacitance which is especially detrimental during the receive mode operation. Although some remedies such as LOCOS regions [11, 12] between the CMUT membranes have been proposed to decouple gap height from isolation layer thickness between CMUT membranes (Figure 3.2-b), due to the high temperature processes including wet-oxide growth in 1050°C, high-temperature annealing, LPCVD silicon nitride deposition and using BOE for etching the oxide layer, the process is not suitable for monolithic CMOS integration.

Another approach to reduce the CMUT parasitic capacitance is using embedded patterned BR layers to minimize the overlap between top and bottom electrodes [13, 14]. Using embedded electrode method to make topography-free surfaces adds an extra etching step, significantly increasing the roughness of the dielectric surface due to etching [15]. In addition, having 2 insulation layers on the top and bottom side of the sacrificial layer increases the effective gap of the CMUT which degrades the CMUT performance. Furthermore, with large CMUT arrays (that will be discussed in chapter 4) where the active area needs to be maximized, the space between the membranes for electrical connections on the patterned BE needs to be small leading to thin electrical lines to reduce overlap. This leads to larger resistance over long CMUT elements such as in 1D arrays. One may increase the BE electrode thickness, but that results in large step heights which may be difficult to pattern the metal layers for subsequent fabrication steps.

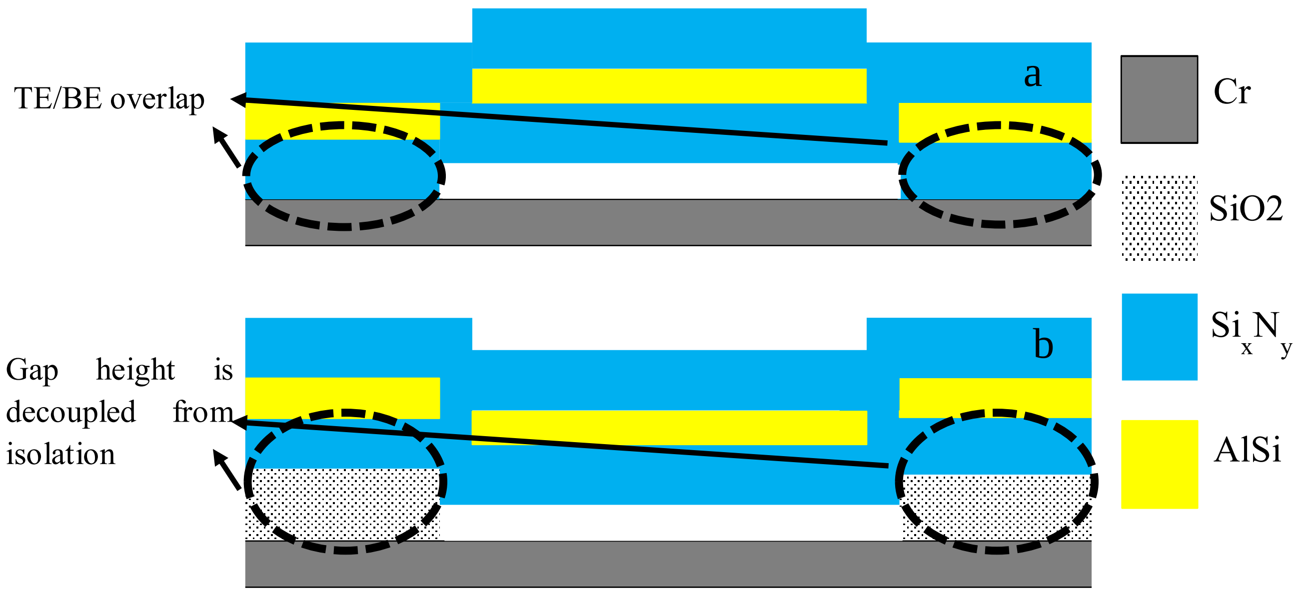


Fig. 3.2 a) Cross section of a conventional surface micromachined CMUT with thin isolation layer over TE-BE overlap area. b) Proposed lift-off based process where an extra layer of dielectric is deposited over TE-BE overlap area without impacting the gap thickness.

The details of fabrication process involved in the improved CMUT fabrication are shown in Figure 3.3 (Table 3.1). All steps are performed at a temperature less than 250°C which leads to CMOS compatibility. The presented results demonstrate a feasible approach that can be applied to CMUTs fabricated with sacrificial release process. The two key advantages of this approach are the use of low-temperature fabrication technique and minimum manipulation in the device structure. In the figure 3.3, the fabrication process steps are described in detail and critical parameters are provided.

3.2.1 Bottom Electrode and Sacrificial Layer

The process starts with 3-µm furnace wet oxide deposition for electrical isolation on a 4” <100> silicon wafer. In CMOS compatible version of the process, this oxide layer is replaced by low temperature PECVD oxide. Although furnace oxide has more uniformity over the wafer, the PECVD shows around 1% uniformity over the wafer that is smooth enough for CMUT fabrication. To form the bottom electrode (BE) - (Figure 3.3-a), Chromium (Cr) is deposited using Unifilm sputterer tool; the sputtering system which deposits thin metal films in an argon-enriched low vacuum. The tool accurately monitors source distributions, by using a computer-controlled planetary system. Cr has strong adhesion to both metals and dielectric layers, and to have low resistance less than 100 ohm, the thickness is chosen to be in the 275-400-nm range. Moreover, Cr is good choice for bottom electrode due to its uniform deposition, resistance to sacrificial layer etchant (APS 100– Cu etchant) and its resistance to oxidation. Copper (Cu) is used as the sacrificial layer as it can be etched very selectively with Cr and silicon nitride membrane layers. To pattern the sacrificial (gap) layer (Cu), the adhesion of the Cu and photoresist (PR) has to be enhanced by spinning a monolayer of P-20 HMDS Primer. The gap has a key role in CMUT operation since thickness variation severely degrades CMUT performance, therefore, Cu thickness is usually characterized exactly before actual deposition on the device and carefully measured after the process to ensure the desired thickness is achieved. The gap (Cu) thickness is optimized to obtain the maximum membrane displacement – full gap swing - and generate maximum pressure based on a large signal CMUT model [16]. Figure 3.3b shows the cross section after Cu is patterned. Note that the PR layer is not removed which is used for the lift-off process.

3.2.2 Dielectric Lift-off and Material Discussion

In terms of the dielectric material and thickness used for the lift-off process, several issues need to be considered. Since the added capacitor is in series with the isolation layer capacitor (figure

3.2-b), a dielectric with lower relative permittivity is preferred. Low temperature deposited dielectrics such as HfO_2, TiO_2, Si_xN_y have relatively large dielectric constant. Although some polymers [17] like Teflon, Polyimide and Fluorinated polyimide have smaller (2.5 - 3) dielectric constants as compared to SiO2 (3 - 3.5), the ease of fabrication and CMOS compatibility indicates that silicon dioxide is a suitable material. The silicon dioxide deposition temperature is limited to < 110 °C because of the photoresist thermal sensitivity. This reduces the quality of the oxide layer with high pinhole density, but sputtering and atomic layer deposition (ALD) systems which may provide higher quality films could not be used due to the side wall coverage. It is worth noting that although lift-off is a usual fabrication technique for patterning metal films, some successful attempts have been accomplished in dielectric and PZT materials patterning [18, 19, 20, 21]. Overall, the results show that evaporated silicon dioxide is a suitable material.

The benefit of lift-off over the regular deposition and patterning is the self-alignment and ease of fabrication. The thickness of lift-off dielectric is chosen to reduce the step height that is caused by bottom electrode (figure 3.3-c). The edge effect in dielectric lift-off is less than the metal lift-off. Besides, considering relatively low thickness of the oxide and 75% top electrode coverage on the membrane, edge effect does not affect the fabrication process.

The breakdown voltage of the thin isolation layer limits the maximum voltage applied to CMUTs. This should be higher than the transient high voltages which may exceed the static collapse voltage. Dielectric breakdown strength of silicon nitride is typically in range of 4 to 8 MV/cm, depending on the plasma power, gas ratios, temperature, and processing pressure of deposition [22]. For 4 MV/cm, breakdown voltage for 200-nm Si_xN_y isolation layer is about 80-V, above the 60-V maximum pulse intended to be used for this ICE application. Using a lift-off step with a 200-220-nm of SiO_2 provides a breakdown voltage of 170-V, well beyond the voltage levels used for this particular application, and it does not introduce a large topography causing any TE step coverage issues. The critical addition to the fabrication process is the SiO_2 lift-off step shown in figure 3.3-c. In order to ensure that the leakage paths are blocked, a self-aligned process is essential since inevitable misalignments in conventional optical mask aligner tools would create problems. Although oxide can be deposited and patterned, the lift-off process helps achieve this goal by minimum additional effort. To lift-off the silicon dioxide, after patterning the sacrificial layer (Cu) and before stripping of the photoresist (PR) with acetone, the silicon dioxide is evaporated using CHA Evaporator chamber at a pressure of about $5e^{-7}$ Torr. In order to reduce the parasitic capacitance and increase the breakdown voltage the silicon oxide layer thickness should be large. However, large topographical steps in the TE layer should be avoided as well. As it can be seen at figure 3.3-c, the difference between Cu and oxide layer thickness make the step height for further process. Therefore, the oxide thickness is chosen about two times the sacrificial layer thickness, which is typically 40-200-nm for the CMUTs considered here. The PR thickness in lift-off process has to be at least 3-4 times more than the deposited layer. Shipley 1813 resist is sufficient for this process as it can form a 1.3-µm thickness when it is spun at 3000 rpm following by a 45-s dwell time. Photolithography is performed using 405-nm UV light with a dosage of 150-mJ/cm^2, the wafers are developed in Microposit MF-319 for about 60-s with gentle agitation after 30s, and followed by oxygen descum process in a Vision RIE (reactive ion etching) chamber with power of about 250-W. This ensures that the entire exposed PR is properly removed before the isolation layer deposition in a PECVD chamber at 250°C.

3.2.3 Isolation, Top Electrode and Membrane Formation

Low stress PECVD silicon nitride (Si_xN_y) is deposited as the isolation layer to ensure that the BE and TE are not electrically shorted when the membrane fully swings and touches the BE (Figure

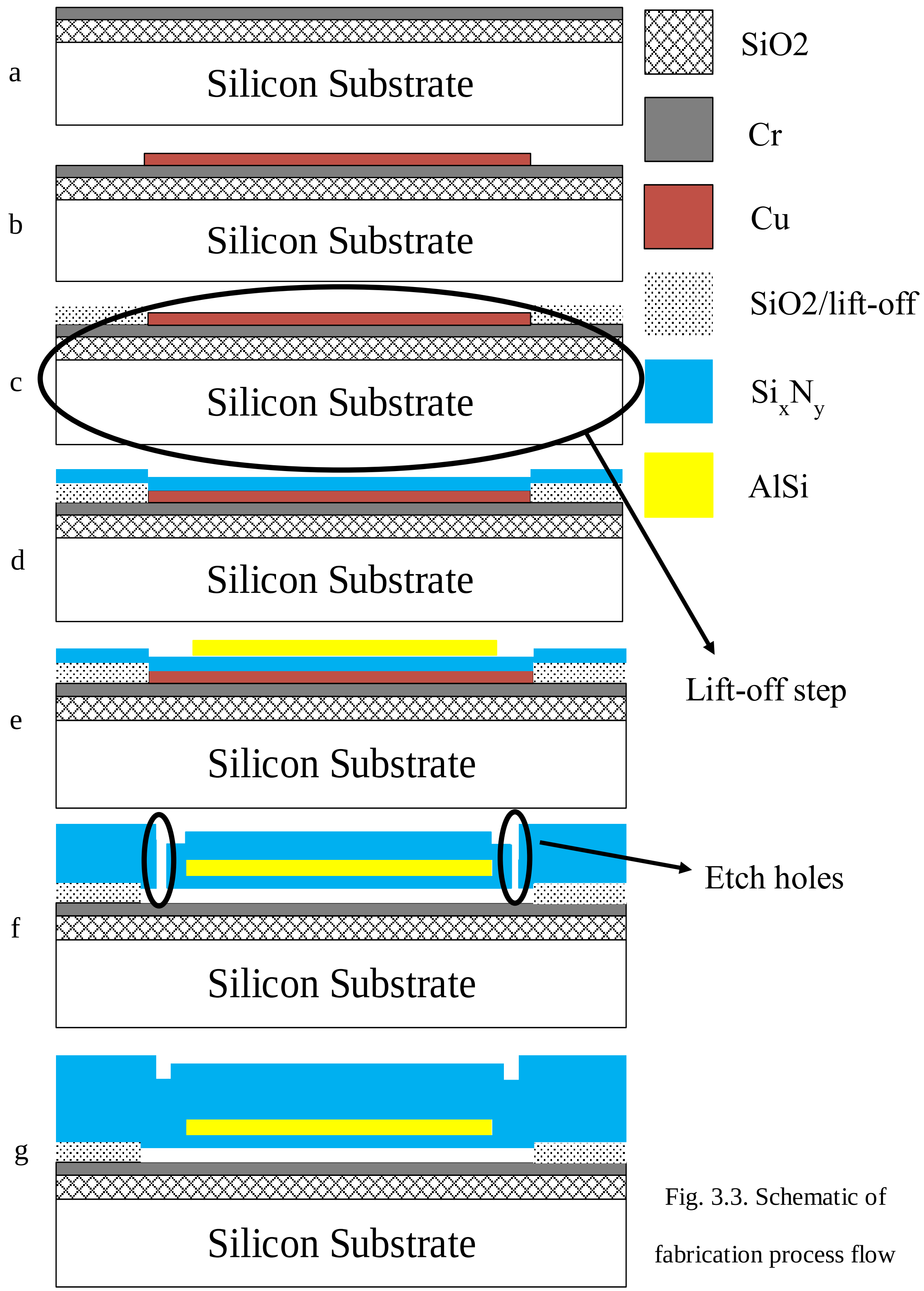


Fig. 3.3. Schematic of fabrication process flow

3.3-d). In order to minimize the pinhole effect in thin dielectric layer, the Si_xN_y is deposited in several steps; the plasma switches 3 - 4 times – each time deposits about 1/3-4 of total thickness. There is trade-off between process temperature and film thickness in Si_xN_y deposition and since the thermal budget is limited in CMOS compatible process, the thickness has to be adjusted to minimize the pinhole density [23]. There are several issues with Copper thin film; the fast oxidation after a short time (about 8-10 hours) and its delamination in the PECVD chamber in relatively low temperature (250°C). Therefore, the time interval between the sacrificial layer deposition and the isolation layer deposition should be minimized and the PECVD chamber temperature should be gradually increased up from 100°C to actual process temperature (250°C), and it has to be either load-lock system or a temperature-controllable tool.

Another approach that can be employed for the isolation layer deposition is with atomic layer deposition (ALD) tool. ALD has a few advantages over PECVD technique; it is using load lock system to load the wafer in the chamber and mitigate the oxidation problem, besides the deposited layer has good uniformity, however the approach has several drawbacks; the process duration is usually long and the tool cannot deposit more than certain thickness in one run. Besides, the deposited layer is usually charged that will eventually degrade the device performance and reduce the collapse voltage [24].

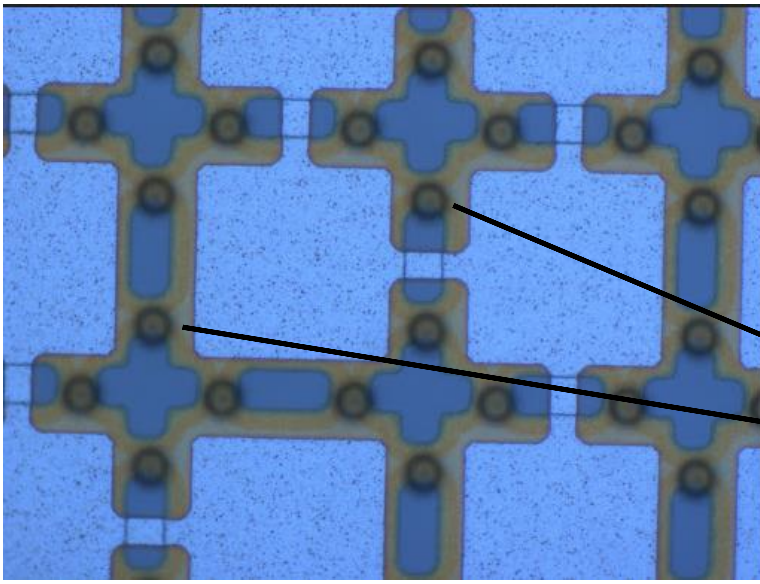
After the isolation layer, aluminum silica (AlSi 1%) is deposited to form TE of the device (Figure 3.3-e). AlSi 1% is a good choice for top electrode due to its low resistivity and low density that does not affect the membrane dynamics. AlSi also tends to be oxidized which affects the TE bond pad resistivity, so a thin layer of Cr (20-30-nm) is usually deposited on top to protect the Al TE surface. After TE formation, Si_xN_y is deposited to the half of the eventual membrane thickness to seal the electrodes.

TABLE 3.1
CMUT PROPERTIES

Parameter	Value
Membrane size	46-µm * 46-µm
Electrode area	38-µm * 38-µm
Membrane thickness	2.2-µm
Device center Frequency in immersion	9-MHz
Vacuum gap	95-nm
Si_xN_y relative permittivity	6.3
Si_xN_y isolation thickness	200-nm
No. of membrane per element	80
Collapse voltage (Vcol)	32-V
Membrane Poisson ratio	0.22
Membrane Young's Modulus	110e9-Pa
Membrane density	2200-kg/m^3
SiO_2 relative permittivity	2
Sacrificial layer (Cu) thickness	110-nm

Etch holes are then patterned and etched using a CHF_3 based dry etch process in RIE chamber to reach the sacrificial layer (Cu) which illustrated in Figure 3.3-f. Figure 3.4 shows the micrograph of the etch holes; the sample is immersed in Cu etchant and the etching is started at the edge of the etch holes. The sample is further rinsed 3-4 times in water to ensure all the Cu residues are removed. The sample is dried in CO_2 super critical dryer chamber. The super critical dryer has to be extremely clean; since contamination can negatively affect the device performance through dielectric charging problems. Alternatively, drying can be performed in oven with temperature of about 85-90°C for about 1 hour.

As the final step, Si_xN_y is deposited to reach the desired membrane thickness (Figure 3.3-g). The



Cu starts etching and showing color change at the etch holes.

Fig. 3.4. Micrograph of the Cu starts etching at the etch hole location.

BE/TE bond pads are then opened followed by 30/500-nm Cr/gold lift-off for wirebonding to test PCBs. Silicon nitride dry etching also etches the photoresist (PR) which is a soft polymer, therefore

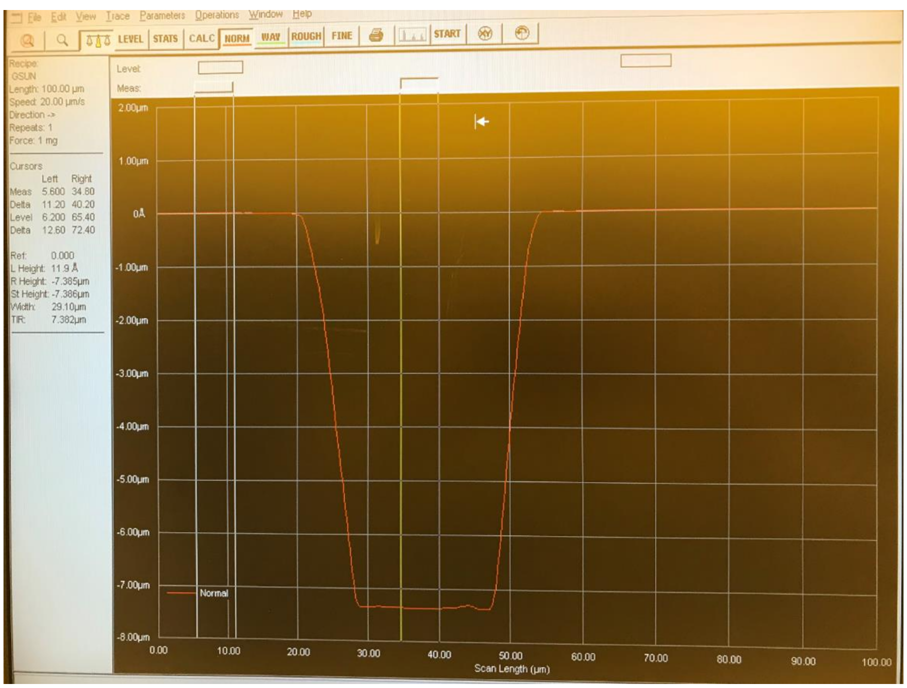


Fig. 3.5. AZP 4620 photoresist shows about 7.3-µm thickness when the spin speed is 3000 rpm following by 90-s hotplate softbake at 125°C.

a thick photoresist is needed to ensure the photoresist layer remains during the entire process. In order to perform 2.2-µm silicon nitride etching and the thick layer lift-off (~500-nm), AZP 4620 photoresist is used. In the speed spin of 3000rpm for about 40s and using AZ 400K 1:3 as developer, ~7.3-µm PR thickness can be achieved. The profile of the photoresist step height is measured with KLA-Tencor P-15 profiler depicted in figure 3.5.

3.3 CMUT Design

The CMUTs fabricated with the lift-off membrane supports are designed in the form of 1D imaging arrays (Figure 3.6-a) for Intracardiac Echocardiography (ICE) application. The array is designed to have a center frequency of about 9-MHz with a 60-70% fractional bandwidth. The fabrication is performed on 300-µm thick silicon wafers so that substrate thickness resonance is moved to 14-MHz (Figure 3.11), which is beyond the transducer bandwidth [25].

In the CMUT design, the simulations are performed using a large signal model [16, 26] which predicts the output characteristics of a CMUT array operated in the non-collapse mode. In order to find the dynamics of the non-uniform electrostatic force accurately over the CMUT electrode, the membrane electrode is divided into patches shaped to match higher order membrane modes [26]. Based on this model, the lateral dimensions of the square membranes are determined to be 46 x 46 μm^2 with CMUT characteristics obtained through the design and modeling process are listed in Table 3.1. The optimized membrane thickness in bandwidth of interest is 2.2-µm, and the gap (95-nm) is optimized to obtain ~1-2-MPa peak-to-peak pressure with 30-60-V pulses when operated in the non-collapsed mode [27]. Due to the residual stress and atmospheric pressure [28, 29] on the Si_xN_y membrane, the static deflection of about 15-18-nm is observed and as a result, the sacrificial layer (Cu) thickness which forms the CMUT's gap is designed to be around 110-nm

3.4 Process Characterization

Figure 3.6-a and b show the micrograph of the completed 1D CMUT array including 64 single elements consisting of two rows of 40 square membranes. The middle image (Figure 3.6-c) shows two membranes after the oxide lift-off step where only the oxide between the square membranes

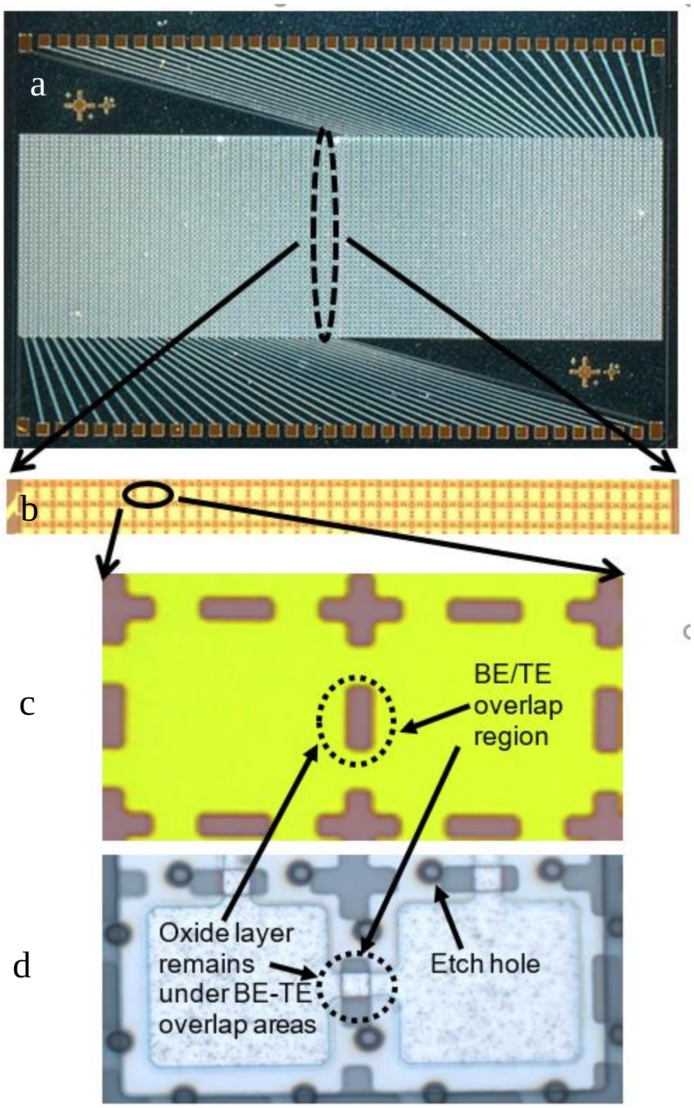


Fig. 3.6. Optical image of oxide lift-off process, (a) The 1D CMUT array suitable for intracardiac echocardiography, (b) Single 1D element. In the figure (c), the green parts are the regions where the oxide is lifted-off on top of copper sacrificial layer. (d) The final CMUT fabricated using the improved method.

remains. The bottom image (Figure 3.6-d) shows the same area after the process is completed. TE traces between the membranes, which earlier passed only over the isolation dielectric, now clearly go over the oxide steps. A scanning electron micrograph (SEM) was also obtained to provide detailed information on the cross sectional structure by cleaving the device along the dashed lines shown in Figure 3.7-a.

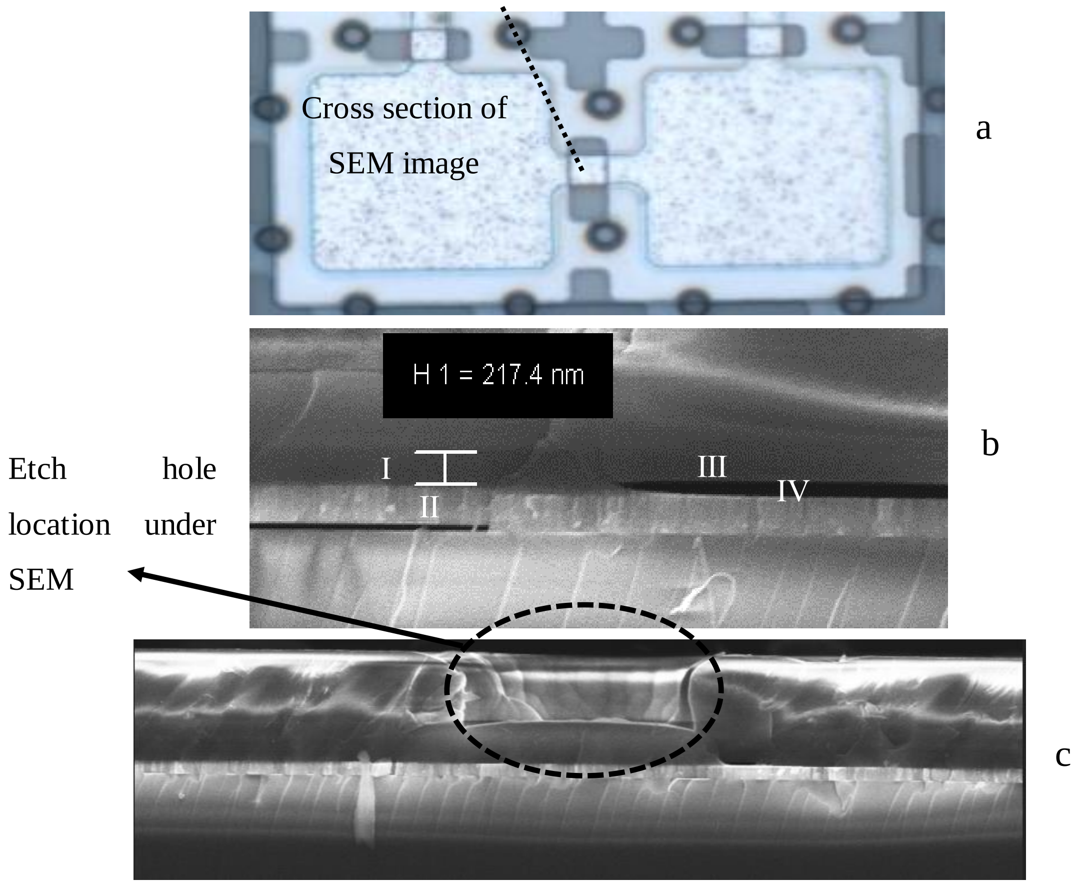


Fig. 3.7: a) Black line shows the cross section used for SEM. b) I) oxide between BE-TE overlap, II) BE (Cr), III) Dielectric isolation, IV) Gap (Cu). The SEM cross section showing a deposition of silicon dioxide (~217-nm) between 2 adjacent membranes. The color of silicon dioxide is different from silicon nitride under the SEM (region I and III). c) Cross section of the membrane depicting release etch hole and further sealing process.

Figure 3.7-b shows the SEM which clearly indicates 95-nm the vacuum gap, and ~200-nm thick lift-off oxide layer, The vacuum gap as well as the ~200-nm thick oxide layer in between membranes is clearly seen, showing the successful lift-off process (Table 3.1). Figure 3.7-c shows the cross section of the membrane clearly illustrates the etch hole and further sealing for the membrane.

Figure 3.8 shows the atomic force microscopy (AFM) measurements on the fabricated membrane which shows about 15-nm of bending at the center of the membrane mainly due to atmospheric pressure as expected. The collapse voltage of the CMUT with this gap is simulated to be 32-V.

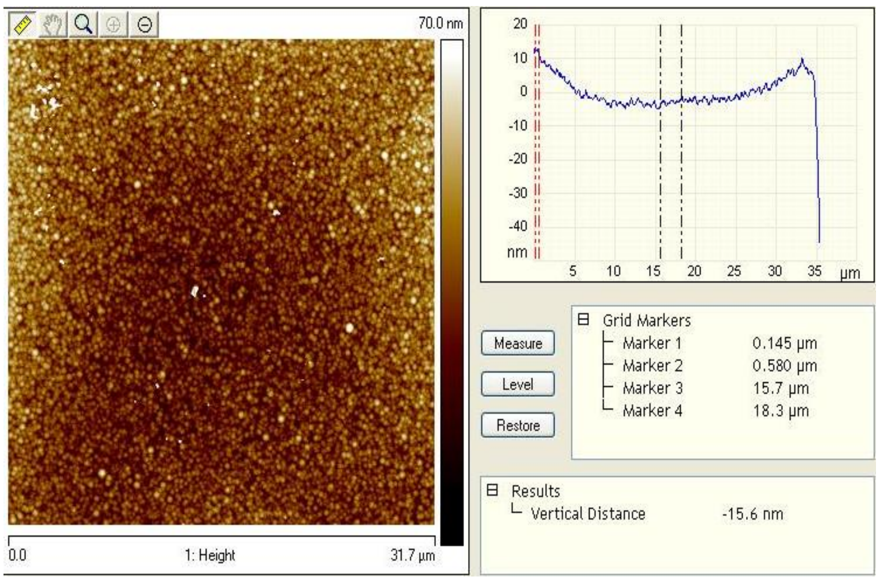


Figure 3.8. AFM measurement on the membrane. The maximum displacement of 15.4-nm occurs at center of the membrane.

3.4.1 Electrical Characterization

To quantify the improvement in parasitic capacitance and coupling coefficient, the device capacitance for CMUT array elements with and without oxide lift-off supports are measured using a Signatone probe station. Figure 3.9 shows the capacitance as a function of applied DC bias, the

C-V curve. The capacitance is minimum at 0-V DC bias for both devices and by increasing the DC bias close to collapse voltage, the capacitance value increases about 4.5-pF as expected in our model [16]. The capacitance value for oxide lift-off device is 2-pF (15%) less, because the parasitic capacitance due to unnecessary TE-BE overlap areas is reduced. The difference between overlap area capacitance in figure 3.9-a and b shows the same difference (~2-pF) that proves the stray capacitance reduction in the overlap regions.

When the DC bias is taken to 30-V (93% of collapse voltage) and brought back to 0-V, there is significant hysteresis in C-V characteristics for the regular CMUT and the capacitance minimum

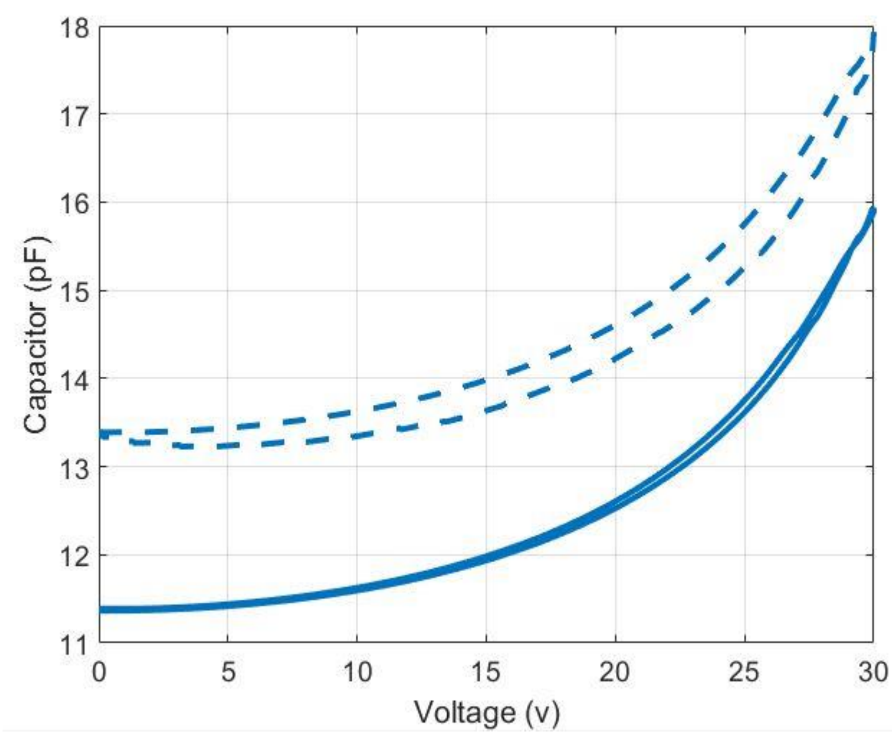


Figure 3.9. The C–V curve of the two CMUT array elements which are identical except for the oxide support.

shifts to a positive voltage indicating that there is charging. In contrast, charging for the CMUT with oxide support is significantly reduced, indicating that the dielectric layer between the TE-BE overlap areas is primarily responsible for charging. The C-V curve can also be used to measure the electromechanical coupling coefficient (κ^2) of the CMUT through the following relations:

$$\kappa^2 = 1 - \frac{C_{static}}{C_{free}}$$

where C_{static} and C_{free} are defined as:

$$C_{static} = \frac{Q(x)}{V} \; ; x_{DC} \, , V_{DC}$$

$$C_{free} = \frac{dQ(x)}{dV} \; ; x_{DC} \, , V_{DC}$$

As a consequence of reduced parasitic capacitance, κ^2 for the CMUT with oxide support is calculated to be around 0.5 while the regular CMUT coupling factor is about 0.40 for 30-V DC bias.

The AC device impedance, functionality and characteristics of the CMUT was also measured with network analyzer (Agilent 8753ES). Figure 3.10 depicts the impedance of the CMUT in air under different DC bias voltages from 0-V to 25-V. The resonance frequency of the device is around 12-MHz in the air that is expected based on our model [16] and it is lowered with increasing DC bias due to spring softening effect.

3.4.2 Acoustic Characterization

The devices with oxide support were also tested in water tank to verify functionality as an acoustic transducer. Figure 3.11 shows the output pressure measured by a hydrophone (HGL-1000 series hydrophone, ONDA Corp., Sunnyvale, CA 94089) when the CMUT array element was used as a

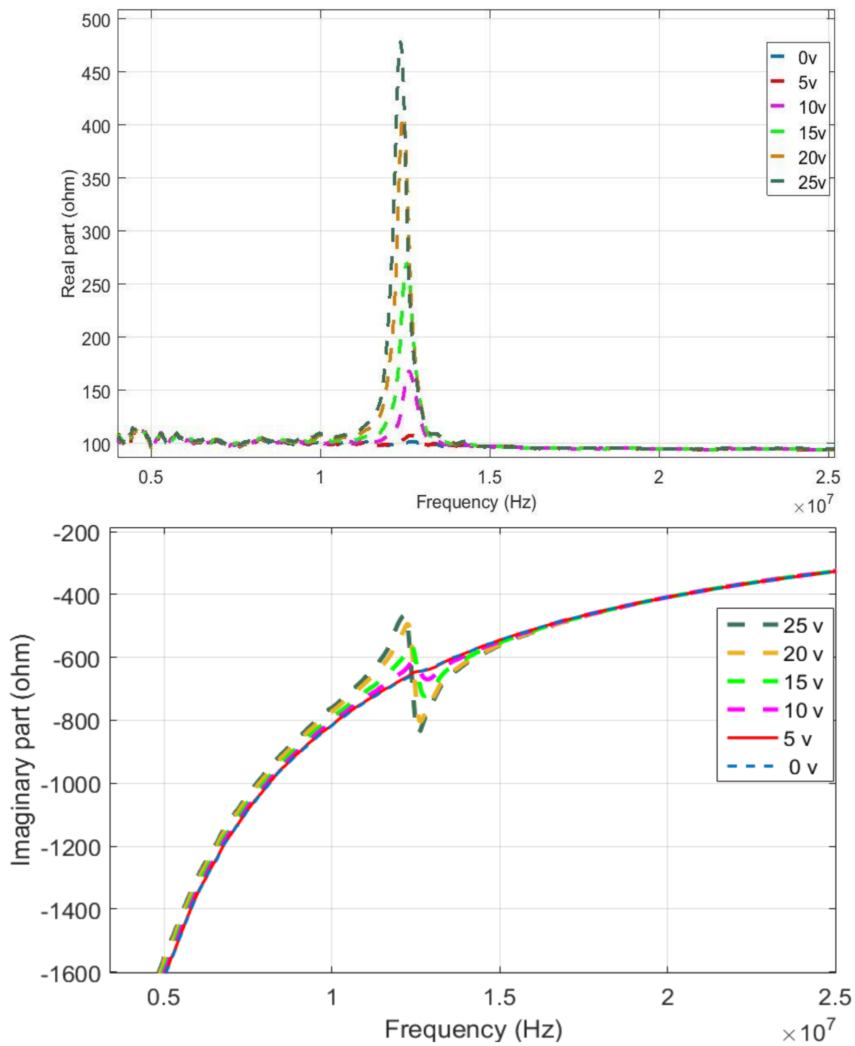


Figure 3.10. Measured electrical input impedance of the devices in air, (a) real part and (b) imaginary part. The resonance frequency is about 12-MHz in air and it reduces with increasing DC bias.

transmitter and was excited with a 50-ns long 30-V pulse with no DC bias. The measured center frequency is about 9-MHz with 65% fractional bandwidth, in very good agreement with the simulations [26, 16] and suitable for the ICE application. The dip around 5.3-MHz predicted in the simulations is due to crosstalk resonance that would be more pronounced in a perfectly uniform array, whereas in the fabricated device it is less pronounced due to unavoidable non-uniformities [30]. The disturbance seen around 14-MHz is due to the silicon substrate ringing which is not considered in the simulations.

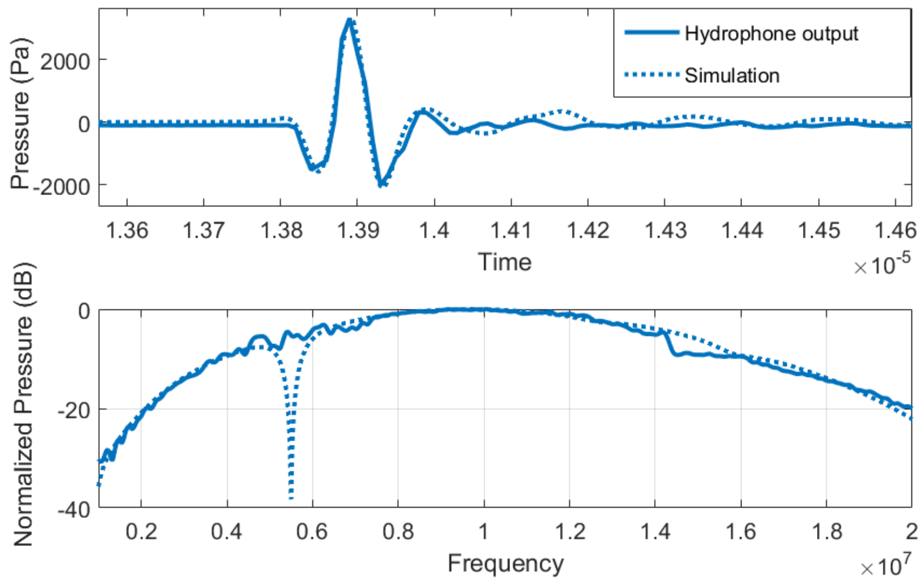


Figure 3.11. Comparison of simulated and measured pressure signals for 1D CMUT element with 80 membranes. The input is 50-ns long 30-V pulse.

3.4.3 Reliability Testing

Repetitive pulsing and DC bias in CMUTs can accumulate charge in the isolation layer which degrades the device performance and will reduce the hydrophone output pressure [14]. Since reducing this non-ideal behavior was one of the goals of the lift-off oxide support CMUT structure, the devices were subjected to a long term transmit pressure measurement test. Both CMUTs with and without the oxide support were excited with 55-ns long, 30-V pulse over 10-V DC bias with 100-kHz repetition rate and the pressure output at 5-mm distance from CMUT is recorded hourly.

The results are plotted in Figure 3.12. The oxide lift-off device output pressure changes about 5% over 2.5×10^{11} vibration cycles in 72 hours without any apparent sign of degradation, whereas the comparison device fails after 5×10^{10} cycles, or about 10 hours. This set of results demonstrates the improvement in reliability achieved by using the lift-off oxide supports in CMUT fabrication.

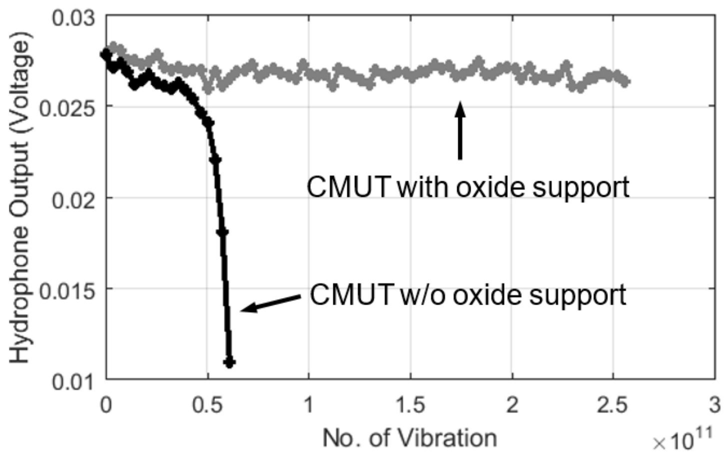


Figure 3.12. Long-term operation test results. Hydrophone output is measured over 72 hours while the devices were excited with 55-ns long, 30-V pulse over 10-V DC bias with 100-kHz repetition rate.

In order to demonstrate the environmental robustness of the newly designed CMUT, the output pressure of the CMUT has been recorded while the water tank temperature is set to 50°C and the device is continually excited with 55-ns long, 30-V pulse over 10-V DC bias with 1-MHz repetition rate. Figure 3.13 illustrates the hydrophone output voltage of the CMUT during this particular experiment. The pressure output changes less than 4% over about 4.5×10^{10} cycles during this period, corresponding to 2,500 hours of use which is suitable for a single use catheter based imaging application.

Consequently, in the improved CMUT, the acoustic performance of the devices have been compared to simulations and long term output pressure measurements even at elevated temperatures showed no significant degradation on performance indicating that this simple addition to the low temperature sacrificial CMUT fabrication process can mitigate the charging issues for catheter based CMUT imaging devices.

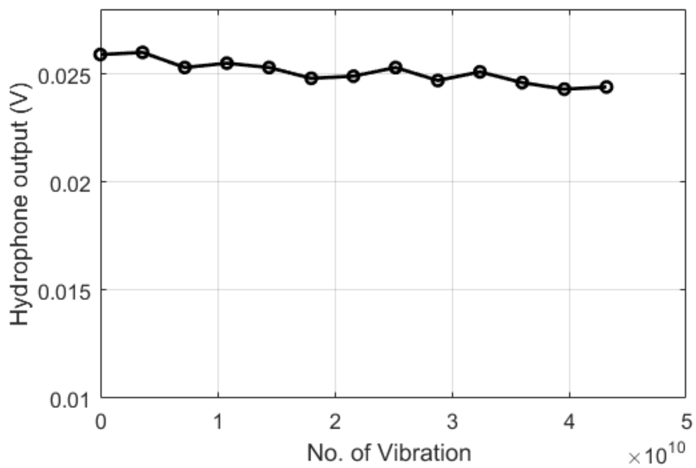


Figure 3.13. Environmental reliability test results. Hydrophone output is recorded while the devices were excited with 55-ns long, 30-V pulse over 10-V DC bias with 1-MHz repetition

3.5 Fabrication Considerations and Issues

3.5.1 Low Stress Silicon Nitride Deposition

The aspect ratio of the membrane lateral size to the gap is usually more than 100 and in our design is about 450 (46-µm/110-nm). This high aspect ratio makes the entire release process challenging since the capillary force during release process causes membrane stiction to the bottom layer. In order to overcome the aforementioned issues, a low stress silicon nitride is deposited. Typically, by setting the ratio of silane to ammonia, 14:1, a low stress deposition can be obtained in PECVD [7]. We optimized our recipe – Table 3.2 - to keep the stress lower than 100-MPa.

3.5.2 Silicon Nitride Etching

Dry etching of silicon nitride is performed in reactive ion etching chamber (RIE) using CHF_3, O_2 and Ar gases (Table 3.3). The recipe is directional and capable of etching the silicon nitride etch holes for about 1-µm height (3-µm diameter) and bondpads opening for a thickness of about 2.2-µm (100-µm x 100-µm square).

TABLE 3.2
SILICON NITRIDE PECVD

Parameter	Value
Silane	200 sccm
Ammonia	8 sccm
Nitrogen	150 sccm
Helium	560 sccm
Pressure	900 mTorr
Temperature	250 °C
Power	45 W

TABLE 3.3
SILICON NITRIDE RIE ETCHING

Parameter	Value
CHF3	40 sccm
Ar	20 sccm
O2	6 sccm
Pressure	40 mTorr
Power	200 W

3.5.3 Copper Delamination

As mentioned elsewhere, in our sacrificial release process, copper is used for the sacrificial material. Copper is deposited with sputtering method and has a good uniformity over the entire wafer. Despite aluminum, copper does not oxidize so is a good choice for low gap CMUTs (~100-nm).

The only disadvantage of copper is the film stress that can cause film delamination and buckling. The delamination exacerbates during higher temperature processes (more than 250°C) that is required for silicon nitride deposition. Figure 3.14 shows how copper film peels off from beneath substrate during a 30 minutes high temperature process. In order to mitigate the delamination process, the PECVD chamber temperature is reduced to 100°C in standby mode, the wafer is loaded and the temperature is gradually increased to the actual recipe temperature (250°C) while the wafer is in the vacuum. This technique protects the film from oxidization and buckling.

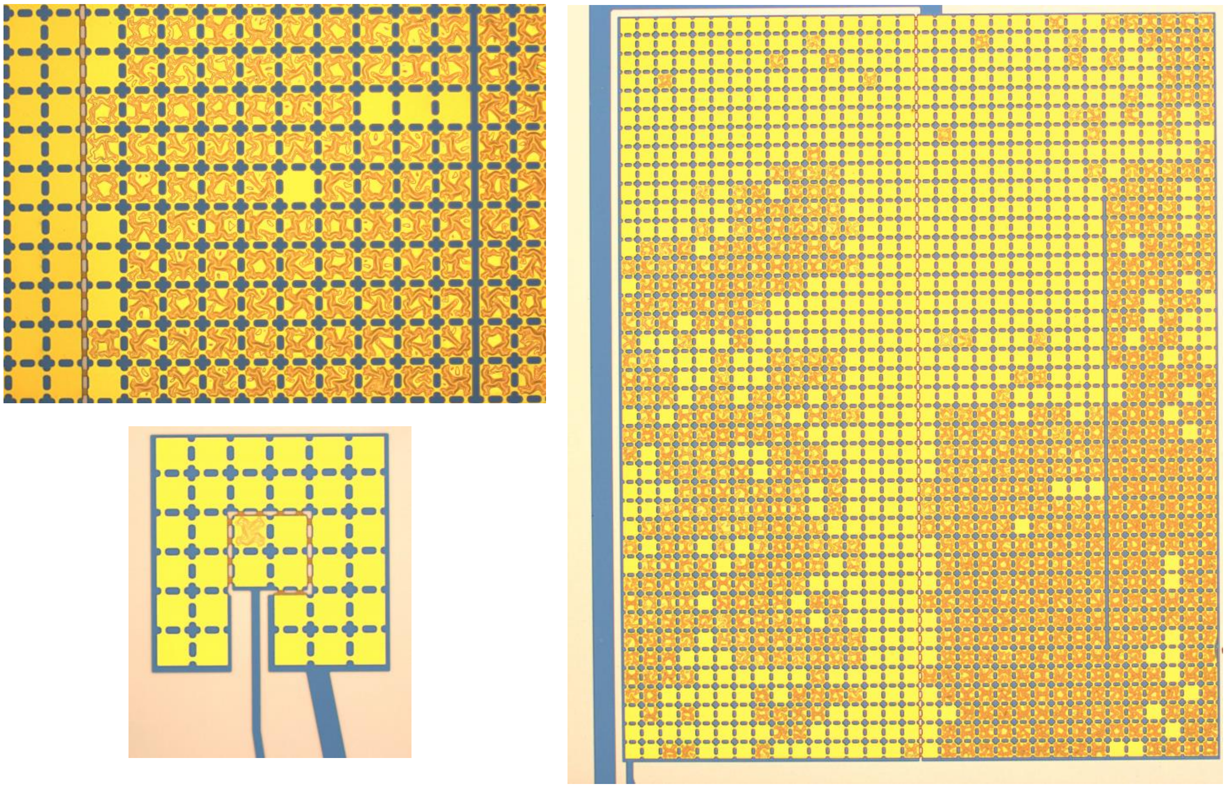


Figure 3.14. The copper deposited on the Cr surface after depositing PECVD silicon nitride. It can be seen that Cu is peeled off and delaminated in several places.

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CHAPTER 4. CMUT ARRAY DESIGN SUITABLE FOR ICE APPLICATION

Intracardiac echocardiography (ICE) imaging has become an essential procedure to diagnose many structural heart diseases and to serve as a guiding tool in interventional cardiology [1]. Commercially available 1D ICE imaging catheters provide 2D images with limited 3D volumes using rotating catheter tip mechanisms [2]. 3D ICE using two-dimensional matrix arrays could provide true volumetric images in real time which help these tools to be more attractive in clinical practice. Implementation of 2D arrays on a small ICE catheter is substantially challenging in many aspects. Particularly, hundreds of array elements need to be diced in sub-hundred micron size which is extremely difficult or sometimes impossible with current transducer technology. In addition, the required number of cables and interconnects of the transducer arrays with imaging platform makes the integration of front-end electronics very challenging. CMUT technology has been a promising alternative for the conventional piezoelectric transducers since it utilizes standard silicon micromachining fabrication process, and hence ensures the compatibility with CMOS technology which allows compact integration with electronics [3]. CMUTs have also many advantages, such as high electromechanical coupling, wide bandwidth in immersion and low cost unit price, compared to piezoelectric transducers [4].

4.1 System and Device Level Design Specifications

In order to implement densely populated 2D CMUT arrays for ICE imaging, the CMUT elements are required to be carefully designed considering output pressure, bandwidth and cross talk. Recent progresses in CMUT modeling, design and fabrication methods [5] have led to an accurate realization of both 1D and 2D CMUT arrays in immersion for ultrasound imaging applications [6, 7]. The integrated front-end electronics design needs detail characteristics of the CMUT arrays which can be simulated accurately with the large signal model that previously developed in our research group [5]. The bandwidth of the CMUT suffers from membranes crosstalk especially in large arrays in which several elements are actuated simultaneously. In order to mitigate crosstalk effects along CMUT arrays, thin layer of PDMS type coating materials such as RTV-60 and RTV-615 can be used to suppress surface waves due to attenuation in lateral direction [8, 9]. CMUT thermal-mechanical (TM) noise caused by the Brownian motion and random vibration of microscopic particles in the membrane, is also an important factor for CMUT design and front-end electronics integration that can limit the signal detection [10].

4.1.1 Design and Simulation

Transducer area and operating frequency are the two limiting factors when designing an ICE array. Commercial ICE catheters have a catheter size of 8-10-Fr (3-Fr = 1-mm) which operate at a frequency range between 5 to 10-MHz. Considering these specifications, we determined the target operating frequency as ~8-MHz for the ICE catheter. In ultrasound imaging, the element pitch is chosen to be around $\lambda/2$ to satisfy the Nyquist sampling criteria which is required to avoid unwanted grating lobe artifacts and also to have large directivity. As a result, the element pitch that we used for our design is around 100 μm. It is worth noting that for a 9-Fr catheter design, the transducer should fit on a 2.6-mm x 7-mm rectangular space similar to the commercial ICE catheter, AcuNav, Siemens [11].

4.1.1.1 Signal to Noise Ratio

The performance of an ultrasound imaging system is usually evaluated by signal to noise ratio (SNR). An ICE system with higher SNR generates an image with higher dynamic range that more accurately exhibits heart anatomical features and eventually helps cardiologists to better diagnose heart diseases and disorders. SNR calculation requires both the signal and noise level. In CMUT operation, the signal level is the output current in pulse-echo operation (figure 4.1) from CMUT operated in receive mode. In ICE application, the reflection target in figure 4.1 is the heart tissue. The noise level is the CMUT thermal-mechanical noise that caused by the Brownian motion and random vibration of microscopic particles in the membrane [10].

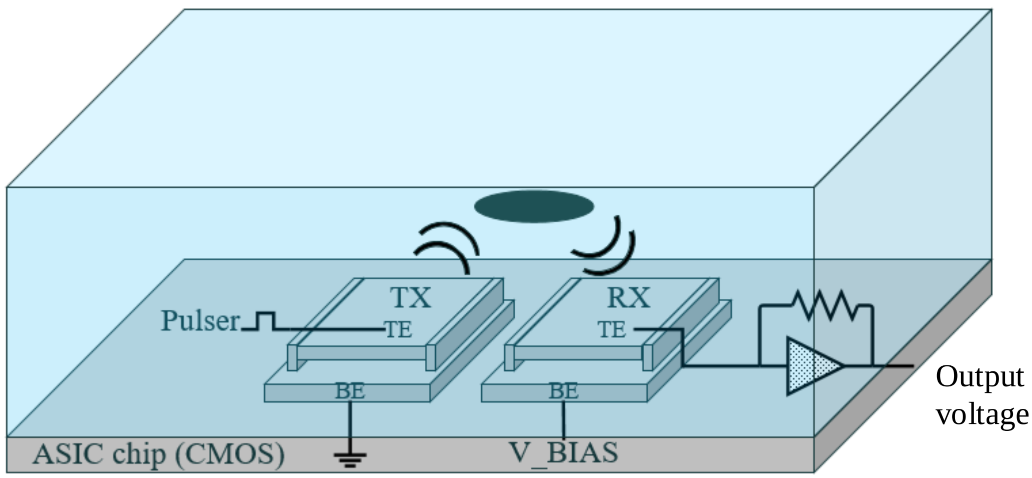


Figure 4.1. Simple pulse-echo platform. The receiver CMUT is connected to an amplifier to amplify the CMUT output current.

In receive mode, CMUT is usually connected to a transimpedance amplifier (TIA) or low-noise amplifier (LNA) depending on the design of the CMUT, noise level and the system requirement. In TIA, assuming op-amp input current is negligible, the entire CMUT current flows into the feedback resistor and the voltage over the resistor is considered the output voltage. In LNA design, the voltage over CMUT is amplified using a low noise amplifier on the output node. The system noise is measured at the end of the receiver circuitry and depends on both CMUT and LNA/TIA noise level. We will discuss about noise measurement in this and the next chapter. In order to calculate the system SNR for a 2D CMUT array suitable for a 8-Fr catheter, the designated transducer area - 2.6x7-mm^2 - is filled up with the elements with 100-µm pitch (8-MHz center frequency) results in 1820 elements on the predefined transducer space. In the case of full phased array, where all the array elements are used in Tx and Rx mode, a 2D array with 1820 elements would generate 97.6-dB beamforming SNR gain calculated by the following formula [12]:

$$Phased\ array\ SNR = 20 * SNR\ (n\sqrt{n}) \qquad Eq. 4.1$$

The ratio between the pressure generated on the transmitter CMUT and the minimum detectable pressure level in receive mode, which reflects the sensitivity, determines the dynamic range of the system. This dynamic range should be high enough to overcome the losses in the system and higher dynamic range corresponds to higher image SNR and quality.

There are 3 different types of loss in an ultrasound system; medium attenuation, diffraction loss and reflection loss from the target. For 5-cm penetration depth – typical distance in ICE application -, which results in transmit-receive propagation distance of 10 cm, the attenuation loss is calculated as 15.2-dB considering the attenuation in blood, given as $0.0596 \times f^{1.56}$ (table 1.1), where f is the frequency [13]. The diffraction loss for the same distance is also calculated as around 69-dB using the approximation in [14]. The reflection loss from soft tissue (heart) is typically calculated as around 40-dB. Considering the beamforming SNR gain (Eqn. 4.1) and to obtain 60-dB image dynamic range, a single array element should have a dynamic range of 86.6-dB with respect to minimum detectable pressure level as calculated in equation 4.2.

$$Gain - Loss = 97.6 - (15.2 + 69 + 40 + 60) = -86.6\ dB \qquad Eq. 4.2$$

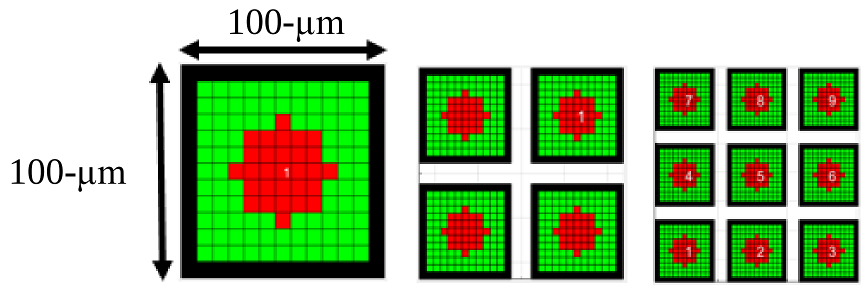
Assuming 2-MPa peak-to-peak Tx pressure and having 60-80% of fractional bandwidth at center frequency of 7-8-MHz, the dynamic range in equation 4.2 results in 93.5-Pa minimum detectable pressure over the full bandwidth or 41.8 mPa/√Hz for 5-MHz frequency band. In the next sections, we will design the CMUT arrays that meet the discussed specifications required for ICE catheter.

4.1.1.2 CMUT Membrane Simulation and Pulse Optimization

In CMUT transmit mode, pressure level and bandwidth are the two key design parameters. Although, the size of an element is set to 100-μm x-100-μm, the configuration of membranes inside the element area determines the overall behaviour of the CMUT element. All the simulations are performed using the large signal model [15]; which predicts the output characteristics of a CMUT array operated in the non-collapse mode and discussed in chapter 2 [97].

Figure 4.2-a shows the 3 different designs to fill the element area with the membranes. The element can be filled with 1, 4, 9, etc. membranes. Simulation shows having 16 membranes or more, significantly degrades the performance of the CMUT element due to high crosstalk. Figure 4.2-a shows the CMUT element with 1, 4 and 9 membranes inside. The simulations and optimizations are based on 60-V input pulse. For each design, we optimized the membrane thickness and gap height and calculated the output pressure. The thickness are optimized to keep the center frequency at around 8-MHz. It can be seen that smaller membranes have larger resonance frequencies so need to be thinned down to adjust the center frequency at around 8-MHz. A membrane displacement is limited by the gap height which determines the CMUT output pressure in a medium. Figure 4.2-b illustrates the simulation results for all three designs. 3x3 design suffers from high acoustic crosstalk, lower bandwidth and also lower pressure than the other two designs.

(a)



	1 membrane	2x2 membranes	3x3 membranes
Thickness (um)	8	2.2	1
Gap (nm)	70	95	120
Collapse Voltage (V)	50	47	49
P-P Pressure (Pa)	4495	7586	436

(b)

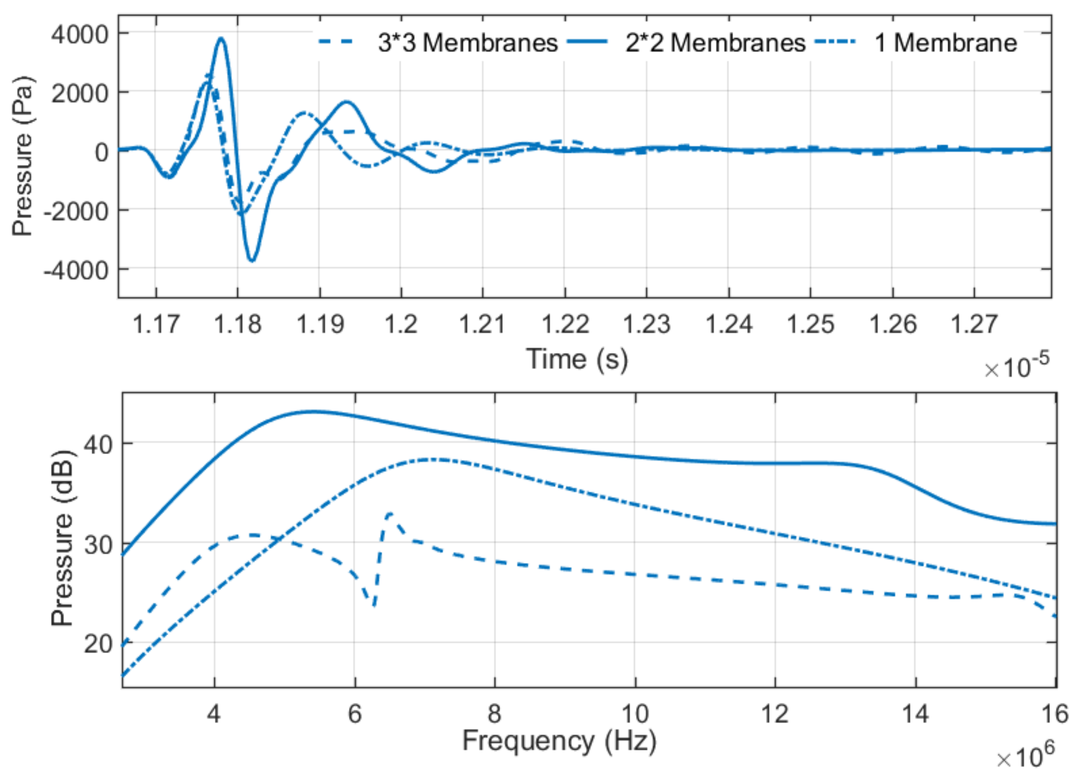
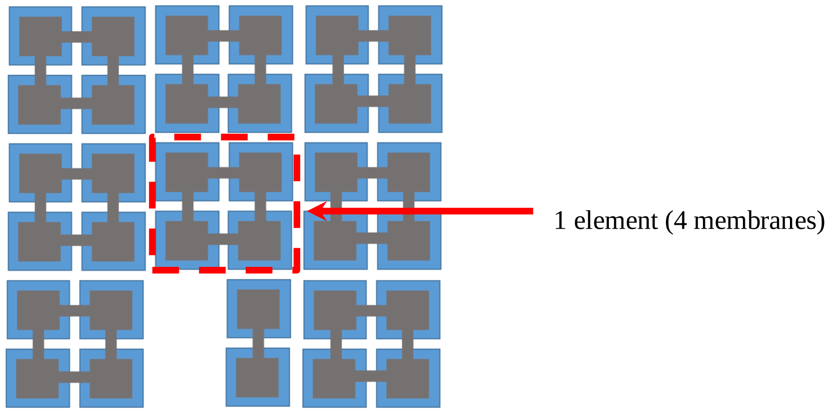


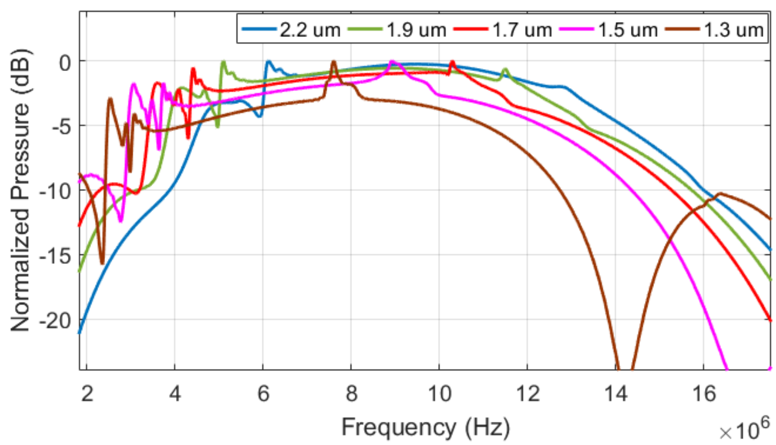
Figure 4.2. a) 3 different membrane designs for a 100-µm x-100-µm element size. Gap and thickness are optimized to generate maximum pressure. b) Simulated pressure level.

In 2x2 design, crosstalk is not significant and the pressure is about 2 times larger than single membrane design besides, the thickness in 1 membrane design is about 8-µm that is not feasible

(a)



(b)



(c)

Thickness (um)	Optimized gap (nm)	Peak-peak pressure at 5mm (Pa)
1.5	115	6850
1.7	105	8565
1.9	100	8765
2.2	95	9925

Figure 4.3. a) Simulated CMUT array. b) The normalized FFT of the CMUT pressure showing membrane thickness between 1.9-µm and-2.2-µm results in optimized pressure and bandwidth. c) The optimized gap is obtained for each thickness and the pressure is

for a single run CVD/PVD deposition. In conclusion, 2x2 membrane design is our optimized geometry. After setting the element area and membrane configuration, the membrane thickness effects are observed. Figure 4.3-b illustrates the pressure and bandwidth of the CMUT depicted in figure 4.3-a. We simulated a single element in an array (figure 4.3-a) to include possible crosstalk effects. The pressure level is relatively low when the thickness is 1.3 and 1.5-μm. It can be observed that the membrane thickness between 1.9 and 2.2-μm results in a highest bandwidth and pressure – Table 4.3-c. It is worth noting that the sharp dip around 4-6-MHz predicted in the simulations is due to crosstalk resonance that would be more pronounced in a perfectly uniform array, whereas in the fabricated device it is less pronounced due to unavoidable non-uniformities [17].

The simulated membrane is silicon nitride with density of 2200-kg/m^3, Young's Modulus of 110-GPa and Poisson ratio of 0.22. The optimized gap height for CMUT element with different thickness is calculated in Table 4.3-c to maximize the CMUT pressure in the surrounding medium. The output pressure is a function of membrane displacement and is optimized when the membrane fully swings the gap height. The thinner membrane deflects easier and swings more; therefore, it needs a larger gap height to maximize the output pressure.

In this research, for the ICE application, the pressure optimization of the CMUT is based on 60-V. Figure 4.4-a shows a unipolar pulse with 60-V pulse height that is also called push mode which implies the membrane is not biased or deflected when pulse is applied. The pressure is simulated at 5-mm distance above the center CMUT element (figure 4.3-a) and optimized pulse width is calculated. The pulse rise and fall time is 5-ns. The collapse voltage of the device is around 34-V therefore, a pulse more than collapse voltage is applied only in a short period to keep the CMUT in non-collapse mode. Figure 4.4-b explains the higher pulse widths correspond to the higher pressure until the membrane collapses that occurs at 60-ns pulse width. The effect of DC bias in push mode is also observed in figure 4.5-b. The entire 60-V pulse is divided in two 30-V; 30-V constant DC bias and 30-V pulse level. Apparently, the membrane collapses at a lower pulse width compared to no DC bias case (figure 4.4-b) as a 30-V DC bias is already applied. The maximum

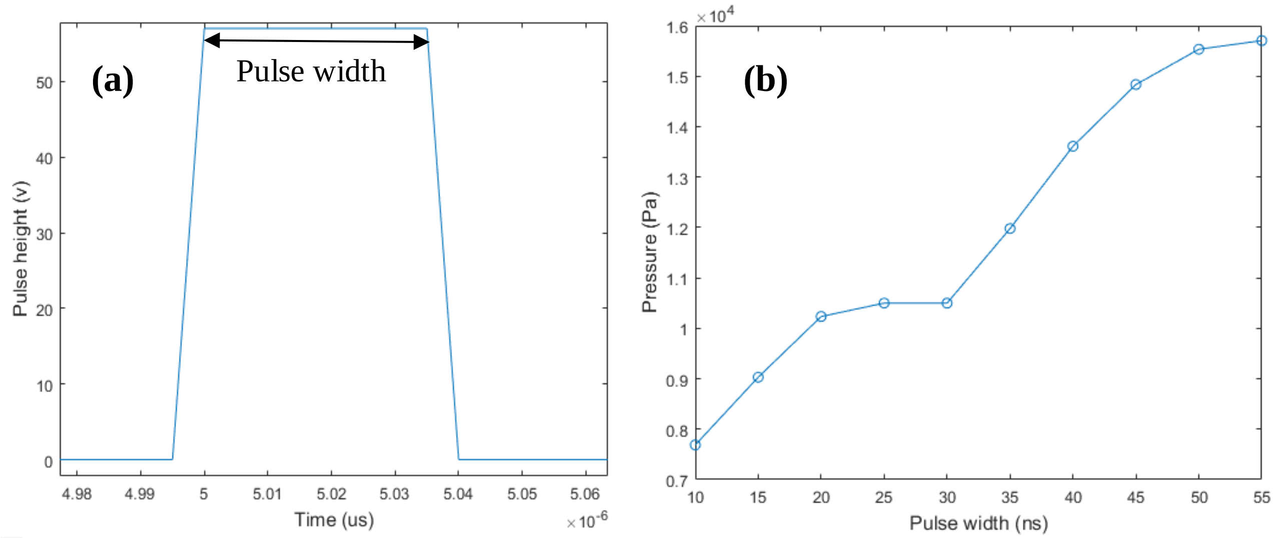


Figure 4.4. a) Unipolar pulse with 60-V pulse height. b) The optimized pressure is calculated in different pulse width.

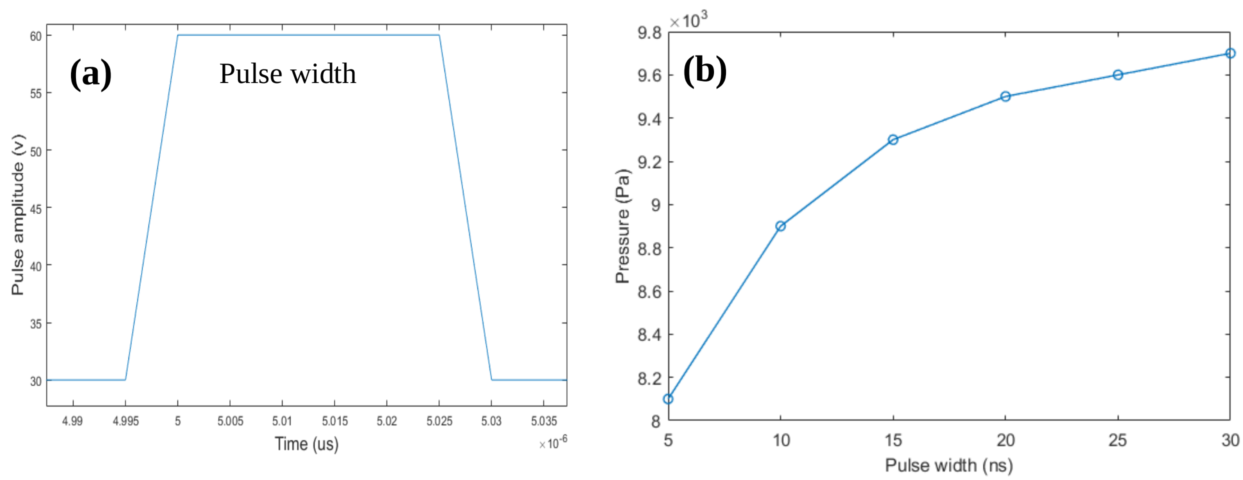


Figure 4.5. a) Unipolar pulse with 30-V pulse height over 30-V DC bias. b) The simulated pressure at 5-mm on the CMUT array with different pulse widths.

pulse width is 30-ns and the pressure is nearly half of the maximum pressure compared to the case that no DC bias is applied (Figure 4.4-b). Another way to excite the CMUT is pull mode in which, a pulse is applied on top of a constant DC bias and the net voltage over the CMUT becomes 0 for a short period and reaches again to the applied DC level (figure 4.6-a). In this technique, the membrane is constantly pulled and only released during the pulse time. This method is limited by the collapse voltage as the constant DC bias cannot exceed the collapse voltage. In addition, having large DC bias on CMUT in transmit mode causes charging on the dielectric layer that reduce the performance of the CMUT.

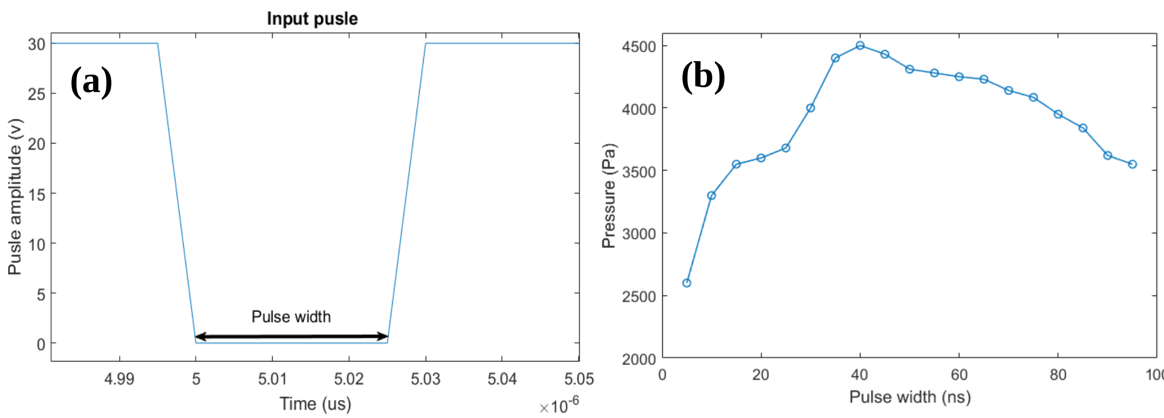


Figure 4.6. a) Unipolar pulse for release mode. b) The simulated pressure at 5-mm on the CMUT array with different pulse widths.

Figure 4.6-b shows the pressure values with different pulse widths. 40-ns is the optimum time that the deflected membrane biased with 30-V can efficiently swing the gap height. Shorter or longer pulse widths lead to lower output pressures. A bipolar pulse described in figure 4.7-a can also be used for CMUT excitation. Despite unipolar pulse, a bipolar (3 state pulse) excitation is a 3 level pulse and able to better excite the membrane displacement profile. As we mentioned before, our total voltage budget is 60-V however, a bipolar pulse can exceed the collapse voltage in both

positive and negative level and is able to generate more pressure than the other two methods. As an example, a bipolar pulse similar to the unipolar pulse depicted in figure 4.4-a, can be from -60-V to 60-V that efficiently excites a CMUT however, in this research we use -30-V to 30-V to keep the net voltage over CMUT 60-V. In figure 4.7-b, the DC level in bipolar pulse (V_{dc}) shown in figure 4.7-a is swept; it can be seen that the pressure is optimized when the pulse is entirely positive or negative (V_{dc} is either -30-V or +30-V). Both 1st and 2nd pulse width have been optimized in

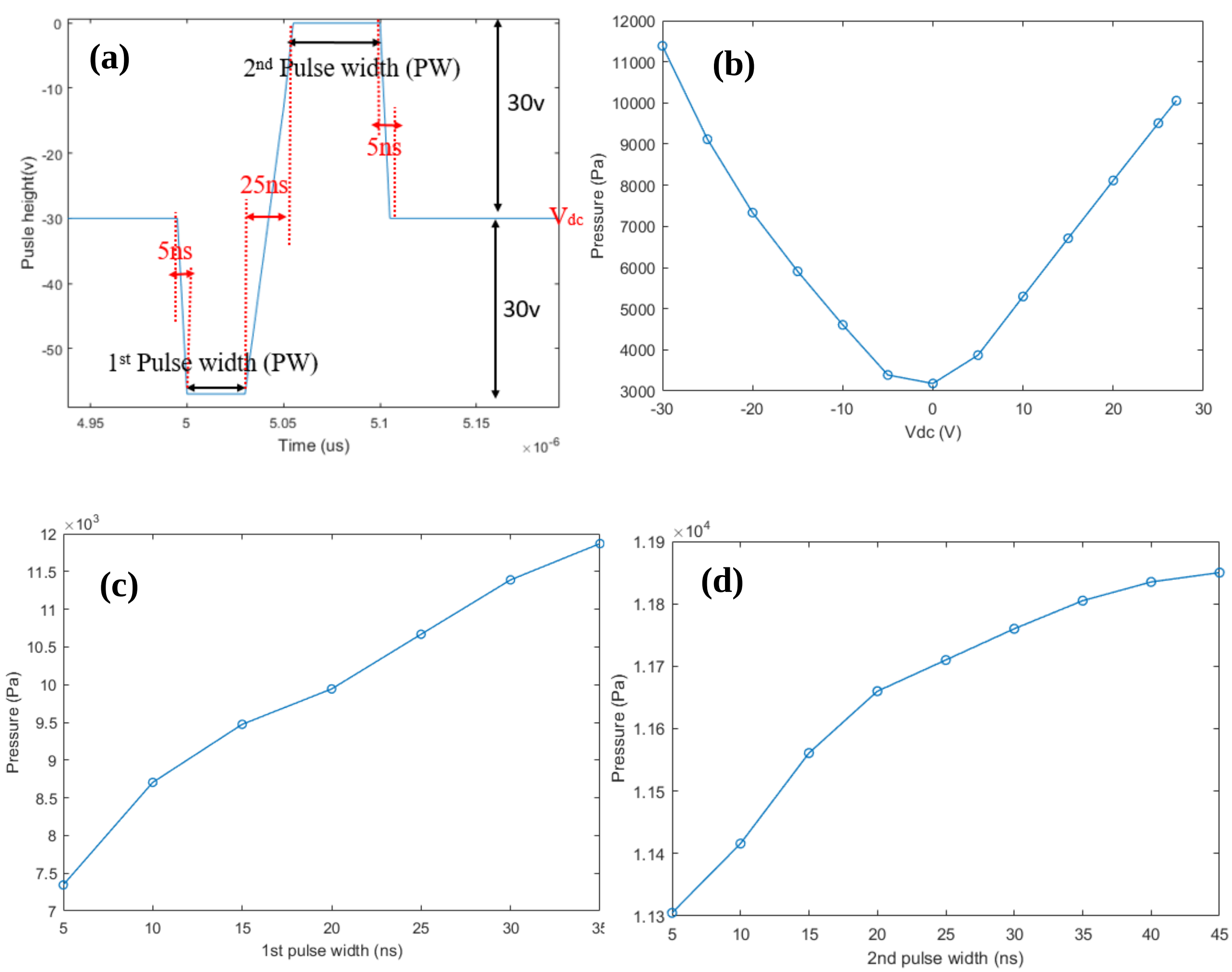


Figure 4.7. a) A bipolar pulse with 5-ns rise and fall time and 25-ns transition time between high and low level. b) DC level optimization - V_{dc} is defined in figure 4.7-a. c) The optimization of the 1st pulse width at V_{dc} = -30-V. d) The optimization of the 2nd pulse width at V_{dc} = -30-V

figure 4.7-c and d. In figure 4.7-c, 1st pulse width has been optimized while the 2nd pulse width is set to 45-ns. The pressure is increased as we increase the pulse width until the membrane collapses at 40-ns pulse width. In figure 4.7-d, the width of the 2nd part of the pulse is optimized when the 1st pulse width is kept at 35-ns that is the optimized width demonstrated in figure 4.7-c. As expected, the output pressure is increased by increasing the 2nd pulse width until the collapse point that occurs at 50-ns. Another parameter of the bipolar pulse is the transition time between low and high level. Figure 4.8 shows the effect of pulse slope on CMUT output pressure. It is clear that shorter slope improves the performance of the CMUT operation therefore, fast transition from low to high level pulse is a design factor for the pulser circuitry.

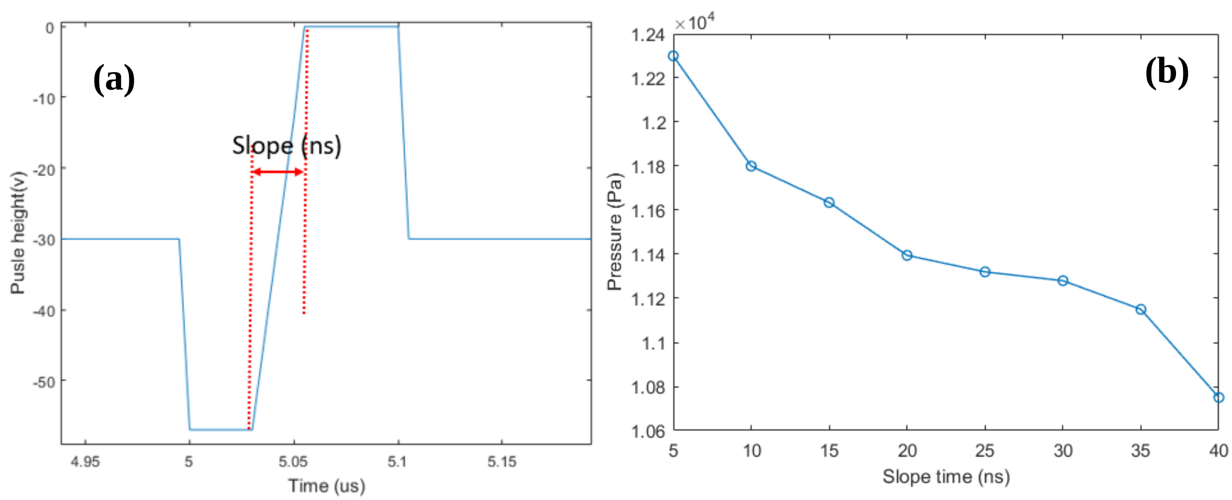


Figure 4.8. a) A bipolar pulse with constant 1st and 2nd pulse width. b) Slope transition optimization.

By setting 60-V net voltage over CMUT bottom and top electrode, the push mode, unipolar pulse, (4.4-a) with no DC bias is more efficient than release mode and bipolar pulse however, bipolar pulse is capable of carrying larger net voltage over bottom and top electrode for the similar gap height. In the next section, the unipolar pulse is applied on the CMUT element that is discussed in figure 4.3-a and the output pressure is measured and simulated.

4.1.1.3 Simulation Verification

In order to verify our simulation results, the test array designed in figure 4.3-a is fabricated with sacrificial release method discussed in chapter 3. The goal is to verify the output pressure simulation with the hydrophone (HGL-1000 series hydrophone, ONDA Corp., Sunnyvale, CA 94089) measurement at a certain distance and then calculate CMUT surface pressure and Tx sensitivity. We also want to find the maximum pressure that CMUT can generate by sweeping input pulse level. In non-collapse mode, CMUT maximum pressure occurs when the membrane fully swings the gap height. A CMUT array similar to figure 4.3-a is fabricated and then packaged onto a custom PCB board via UV curable epoxy. Subsequently, the PCB is coated with 3-µm parylene using parylene coater machine to ensure all the exposed electrical contacts are isolated when the array is placed in water tank. Figure 4.9-a shows the acoustic measurement setup using a water tank. Figure 4.9-c shows there is a good agreement between the simulation and measurement results that obtained at 5-mm above the CMUT element. Optimum pressure is obtained from 55-V pulse height with 55-ns pulse width on top of 5-V DC bias. The hydrophone output voltage is converted to pressure using hydrophone calibration data showing around 10-kPa pressure. The 14-MHz dip is the silicon substrate ringing that occurs outside our bandwidth of interest. It is worth noting that the substrate ringing for a 500-µm silicon wafer is at around 8-MHz so we used 300-µm thick silicon or IC substrate for all the fabrications performed in this thesis.

Since the simulation is in a good agreement with the measurement, we use our model [15] to calculate the Tx sensitivity on the CMUT surface. Besides, we are not able to measure the pressure directly on the CMUT surface. Figure 4.10 demonstrates the CMUT surface pressure calculated with our model [15] showing about 2-MPa peak-to-peak Tx pressure and confirms our assumption that we used in section 4.1.1.1 for SNR analysis.

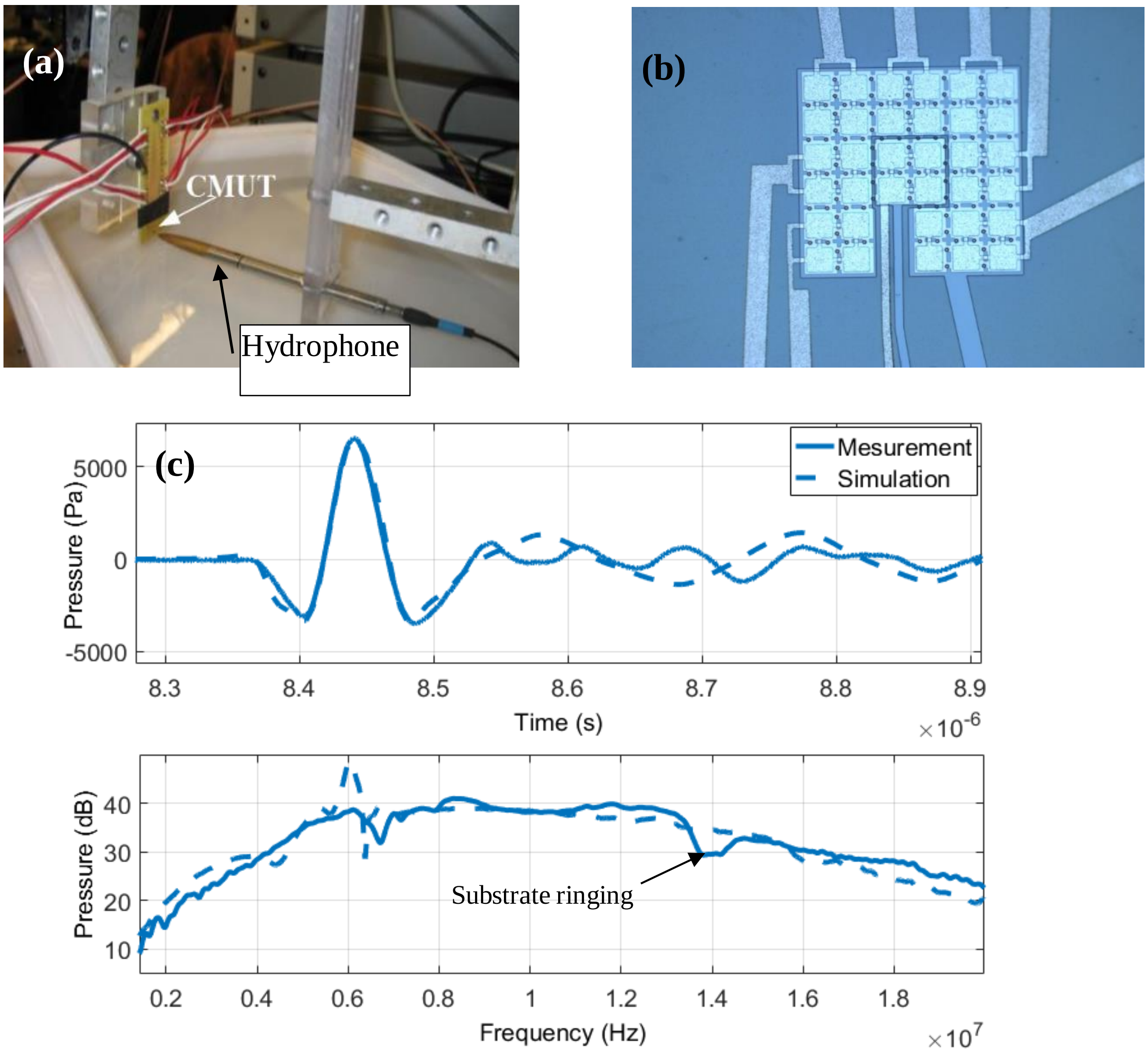


Figure 4.9. a) Hydrophone measurement setup. b) Fabricated CMUT array. c) The measurement and simulation of a CMUT element in a 2D array at 5-mm above the device shows the simulation and measurement are in good agreement.

Studies on high power CMUT arrays have shown about 1-2-MPa surface pressure [18, 19] with thick silicon membranes however, we could achieve similar surface pressure with relatively thin silicon nitride membrane. 2-MPa surface pressure with 60-V input pulse excitation corresponds to

30-kPa/V transmit sensitivity that is significantly larger than its counterpart, PMUTs, with a sensitivity of about 2-3-kPa/V [20].

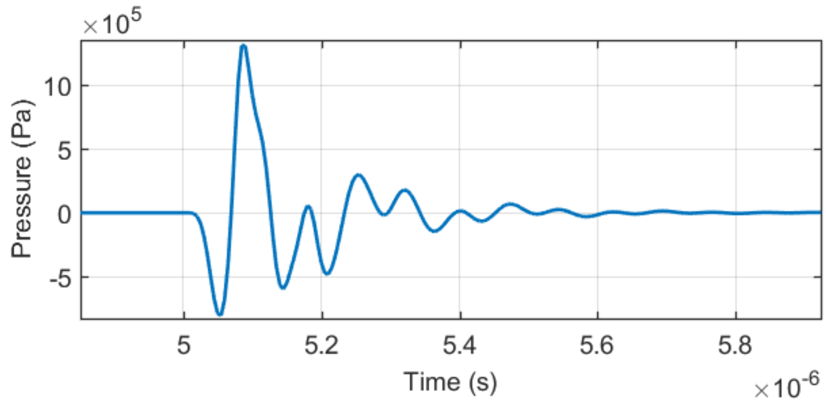


Figure 4.10. The surface pressure simulation shows the pressure could reach above 2-MPa.

4.1.1.4 Element Impedance, Electromechanical Transformer Ratio and Noise Calculation

Impedance is one of the key characteristics of a CMUT element that reveals information about device working frequency, bandwidth and thermal-mechanical noise. In this section, we calculate the impedance and transformer ratio for the element that is designed during section 4.1.1. To calculate the impedance ($Z_{CMUT,ELEC}$) of a CMUT array, a very small AC (Gaussian pulse) pulse over a relatively large DC bias is applied to ensure the CMUT is operated in small signal regime. It is worth noting that large DC bias – e.g. 90% of collapse voltage – is needed for CMUT during receive operation to increase the sensitivity (Chapter 2). CMUT impedance is given as:

$$Z_{CMUT,ELEC} = \frac{V}{I} \qquad Eq. 4.4$$

where V the is total applied voltage and I is the CMUT output current. Figure 4.11 illustrates the real and imaginary part of the impedance calculation in immersion using our large signal model [15]. The simulation is performed on a 3x3 CMUT array -figure 4.3-a – instead of a single element in order to observe the acoustic crosstalk effects of the neighbor elements on the performance of the CMUT in the bandwidth of interest. The green dashed line is the static capacitance with constant gap that matches well with the imaginary part of the CMUT impedance after 10-MHz. The membrane resonance activity is around 6-7-MHz (figure 4.11).

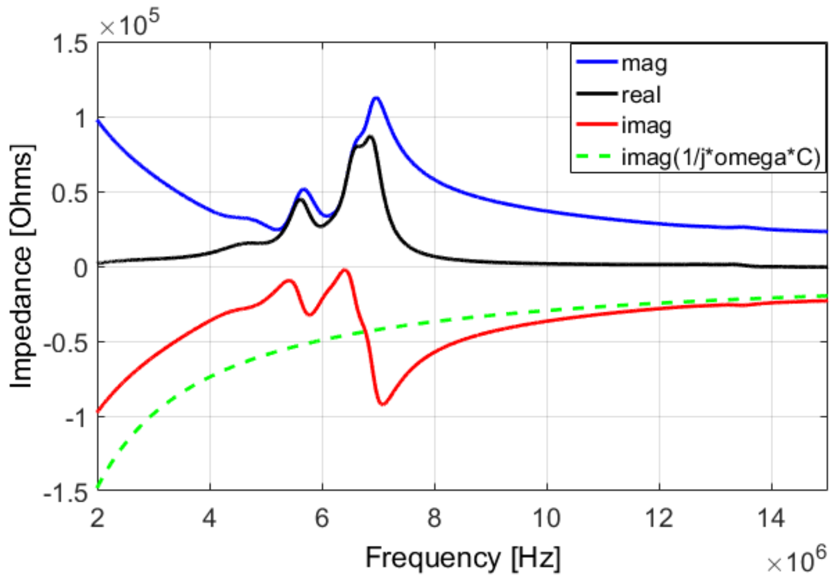


Figure 4.11. CMUT impedance calculation in water for a single 2D element

In general, transducers transfer a signal from electrical domain to mechanical or vice versa. A key parameter to link the mechanical domain to electrical domains is called transformer ratio (n). n is defined as the ratio of the force (velocity) at the mechanical domain to the voltage (current) at the electrical domain of the transducer –figure 4.12 - with units of (N/V) or $(A/(m/s))$ and defined as given:

$$n = \frac{V_{DC} C_0}{g_{eff}} \qquad Eq. 4.5$$

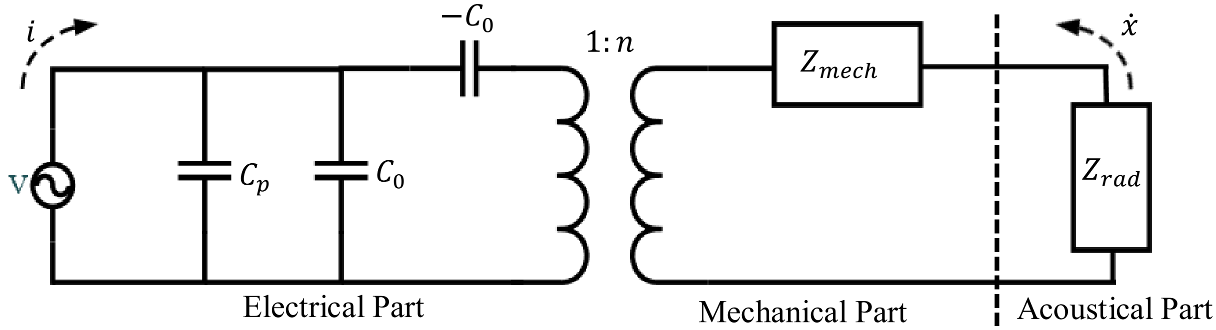


Figure. 4.12. CMUT small signal model in transmit mode. The equivalent circuit consists of passive elements and a transformer ratio links electrical and mechanical domain.

where V_{DC} is the applied DC bias, C_0 is the initial capacitance of the CMUT and g_{eff} is the effective gap of the membrane. Figure 4.13 illustrates the theoretical value (equation 4.5) and the calculation of transformer ratio with our model [15]. CMUT current and membrane velocity is calculated when the CMUT is excited with a Gaussian pulse over a relatively large DC bias (0.9Vcol). From figure 4.13, it can be seen that n is a real number implying the imaginary part of the transformer ratio is zero. It also denotes that current and velocity are in phase in small signal

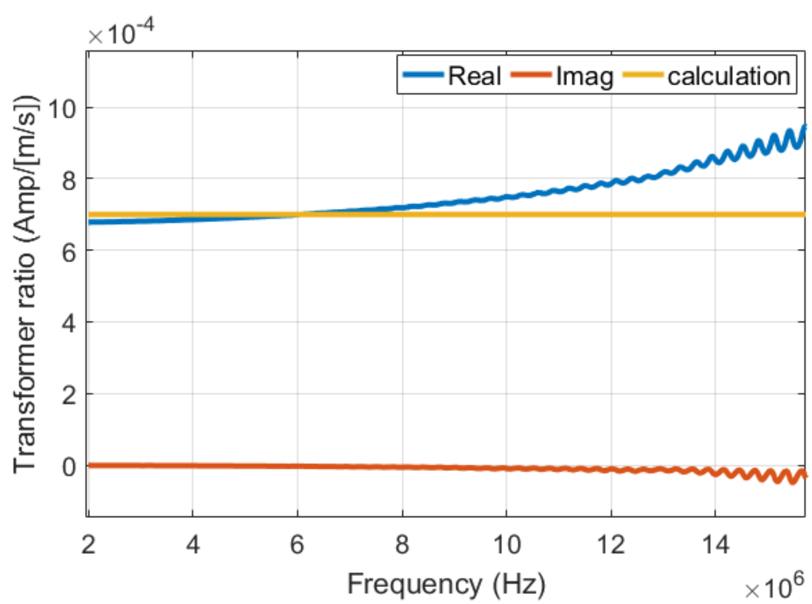


Figure 4.13. Transformer ratio of a single CMUT 2D element.

model. As equation 4.5 states, n is proportional to C_0 value and to observe it with our model, the transformer ratio for the entire 2D array (8 elements - depicted in figure 4.3-a) is calculated using our model. The transformer ratio for the array is ~8 times larger than single element confirming our expectation as the size of the array is 8 times larger than single element.

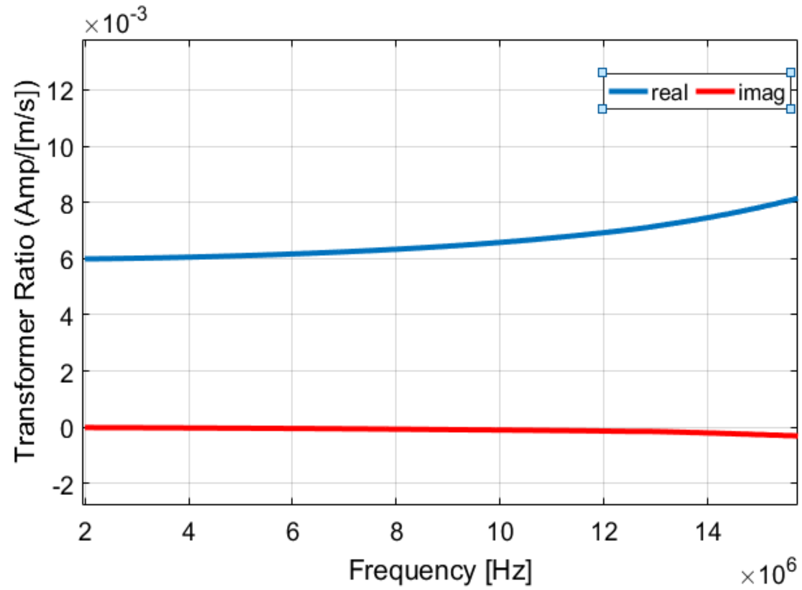


Figure 4.14. Transformer ratio of the entire CMUT 2D array (8 element) depicted in figure 4.3-a.

As noted at the beginning of the section, the CMUT impedance is one of the key characteristics of a CMUT element that reveals information about CMUT thermal-mechanical noise (TM). TM noise is caused by the Brownian motion, which is the random vibration of microscopic particles caused by collisions of molecules and atoms in the surrounding space [10]. The TM current noise can be calculated from equivalent small signal circuit model for a CMUT element in receive mode that discussed in detail in [10]. The CMUT TM current noise is calculated as [10]:

$$i_{noise} = n\sqrt{\int \frac{4KTRe[Z_{CMUT,MECH}(f)]df}{|Z_{CMUT,MECH}(f)|^2}} = \sqrt{\int \frac{4KTRe[Z_{CMUT,ELEC}(f)]df}{|Z_{CMUT,ELEC}(f)|^2}} \qquad \text{Eqn. 4.6}$$

In Eqn. 4.6, K is the Boltzmann's constant (1.38x10e^{-23} J/K), T is the temperature of the surrounding environment in Kelvin and $Z_{CMUT,MECH}(f)$ and $Z_{CMUT,ELEC}(f)$ are impedance of CMUT from mechanical and electrical side respectively (figure 4.12). To simplify the expression one step further, at resonance frequency, $Z_{CMUT,ELEC}(f)$ becomes $R_{CMUT,ELEC}$ and, hence, CMUT current noise (Eqn. 4.6) can be calculated as [10]:

$$i_{noise} = \sqrt{\frac{4KT}{R_{CMUT,ELEC}}} \qquad Eq. 4.7$$

The value of $R_{CMUT,ELEC}$ in immersion can be calculated as 60-kΩ from figure 4.11; using this value in Eqn. 4.7 suggests an expected CMUT TM noise current of about 0.52-pA/√Hz.

4.2 Angular Response, Directivity Measurement and Simulation

CMUT arrays radiate acoustic waves into surrounding medium that can be air or fluid. In ICE application, the generated ultrasound wave from CMUT travels through blood. One of the key characteristics of a CMUT array is the wave propagation behavior and its angular pattern. The angular response is defined in far filed region that wave behavior is predictable. For directivity measurement, a single element in an array with neighbors (figure 4.15-c) has been used in immersion. The center element is excited with a 20-V pulse without DC bias. Both simulation and measurement demonstrate 3-dB bandwidth of about 40 degree. In this design, the thickness is slightly more than the design discussed in figure 4.3-c – 2.3-µm- and the CMUT center frequency is about 9-MHz (Figure 4.15-b). Figure 4.15-b shows the simulation results for calculated pressure from -50 to 50 degree. In figure 4.15-b, similar to figure 4.9-c, a peak and dip can be seen before the center frequency around 6-MHz duo to the element crosstalk.

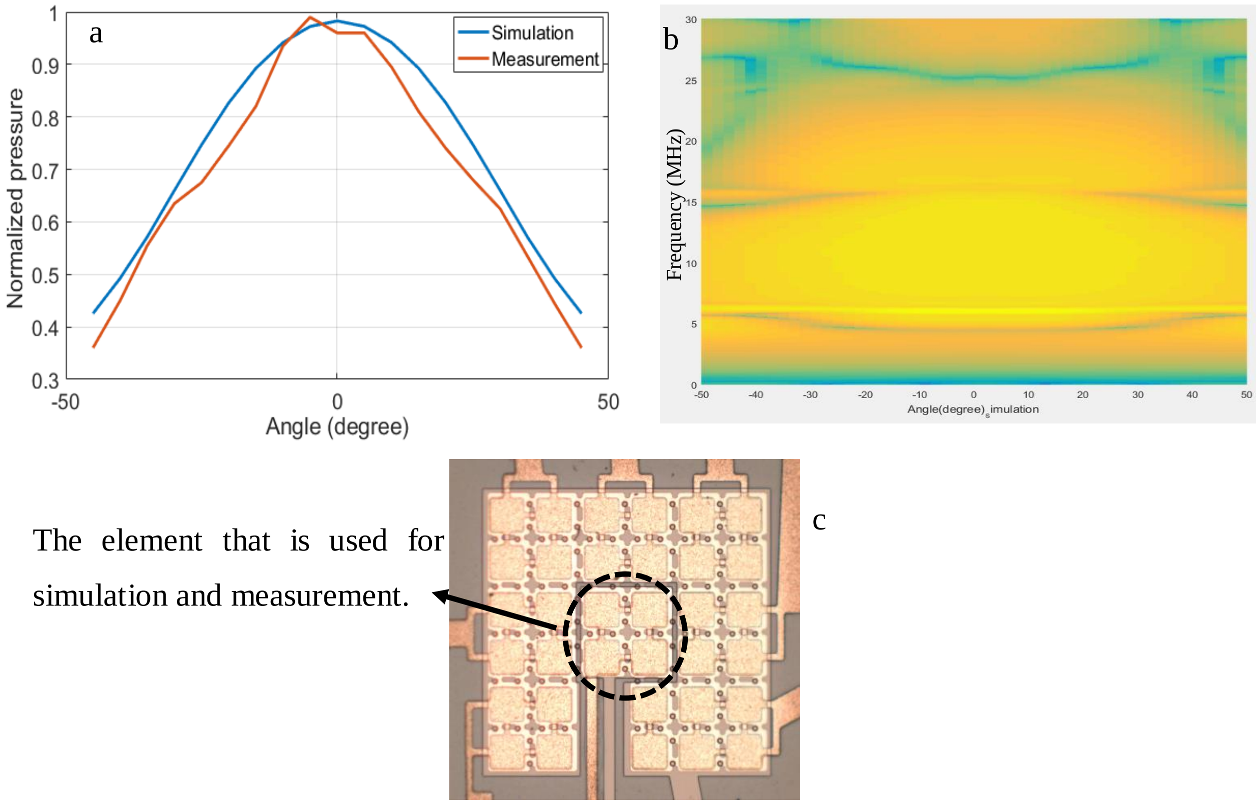


Figure 4.15. a) Directivity simulation and measurement of a single element. b) Frequency response of a center element. c) Micrograph (optical image) of the measured element.

In this chapter we discussed 2D CMUT design, simulation, electrical and acoustic measurement and system requirement. In order to generate 3D volumetric images, a high-density 2D array is required. Due to the front-end electronics design complications and number of channels the data collection for 2D arrays is extremely challenging. Another design for ICE catheter that can only generate 2D image is the 1D arrays (long elements) over the entire CMUT designated area. In next section, we discuss about our 1D array design and measurements.

4.3 1D Array CMUT Design, Simulation and Measurements

A CMUT 1D array suitable for 8-Fr ICE application is also designed, simulated and measured in this thesis. To keep the center frequency around 8-MHz, similar membrane geometry, lateral size and thickness has been used – section 4.1.1. The 95-nm gap height results in a collapse voltage of approximately 25-V, is also optimized for a 60-V pulse suitable for ICE application. For a 8-Fr catheter (2.6x7-mm^2), the transducer area can be filled with 64 1D arrays (figure 4.16). Each 1D CMUT element consists of a 2x40 membranes for a total length of 2.1-mm. The details of CMUT fabrication can be found in [21]. The array elements have a pitch of 104-µm, with a 46-µm x 46-µm membrane size, resulting in an 8.5-MHz center frequency with 80% fractional bandwidth. The CMUT array is coated with a 3-µm Parylene C to isolate the electrical connections in water. Silicon Nitride (Si_3N_4) was used for the dielectric isolation layer with a thickness of 200-nm and the total Si_3N_4 membrane thickness is 2.2-µm. Aluminum-Silicon (AlSi) was deposited using sputtering to form the top electrode that covers 80% of the membrane area.

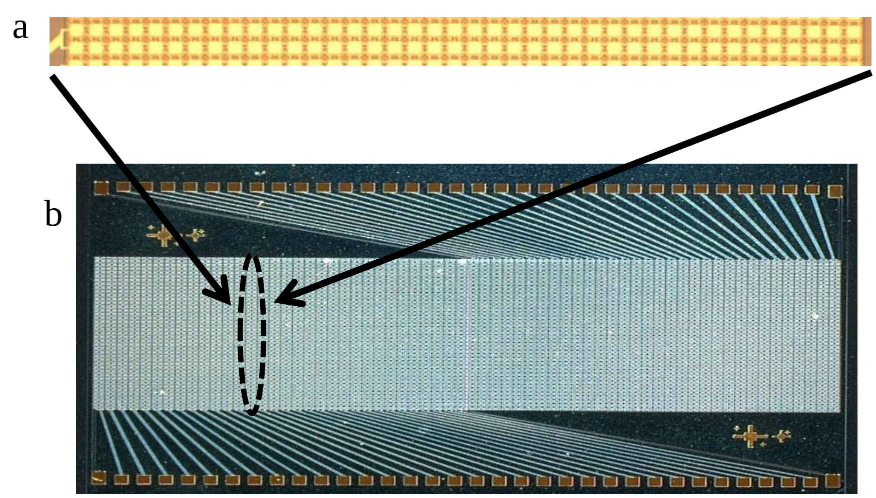


Figure 4.16. a) a 1D single element contains 80 membranes with the size of 46-µm x 46-µm. b) An ICE array includes 64 1D elements.

Similar to 2D array characterization, the impedance of 1D array is simulated (figure 4.17) in immersion using the same method discussed in section 4.1.1.4 where the CMUT is biased with 90% of its collapse voltage. Since the 1D array is larger than small 2D element, the real and imaginary part of the impedance is lower. To qualitatively verify the calculation, the static capacitance – green dashed line in figure 4.11 and 4.17 - of the small 2D and 1D CMUT array is compared. It can be seen that at 10-MHz, the ohmic value of the static capacitance for the 1D array is around 20 times smaller than 2D element, denoting the 1D array is 20 times larger.

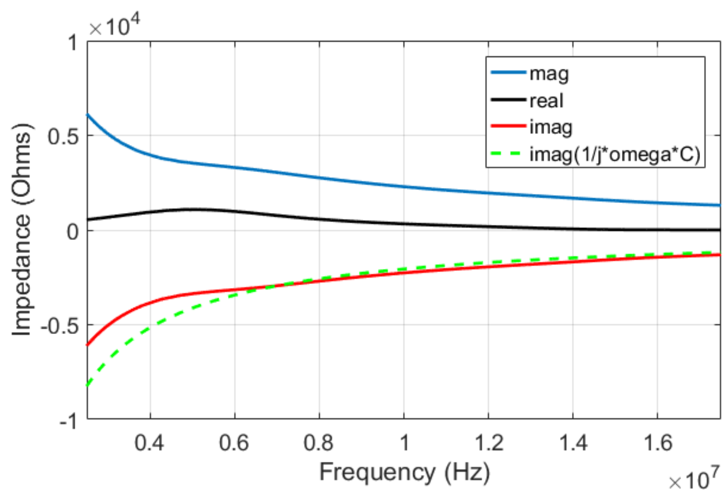


Figure 4.17. CMUT impedance calculation in immersion for a 1D array.

The value of $R_{CMUT,ELEC}$ in immersion can be calculated as ~1-kΩ from figure 4.17 that by using Eqn. 4.7, the expected CMUT TM noise current is ~3.9-pA/√Hz implying a larger array will have a larger TM noise level – compared to 0.52-pA/√Hz for a CMUT 2D element.

4.3.1 Analog Front-end Electronics Considerations and Array Beamforming Capability

CMUT Tx and Rx circuitry for 1D CMUT array are also designed and implemented, the details can be found in [22, 23]. The front-end electronics design is focused on reducing the number of cables used in the catheter. X-ray guidance is required for current ICE catheters however, by reducing the number of cables, the catheter can be guided under MRI to avoid the X-ray harmful radiation to both patients and physicians. Under MRI, The RF induced heating caused by cable metal lines limits the cable count.

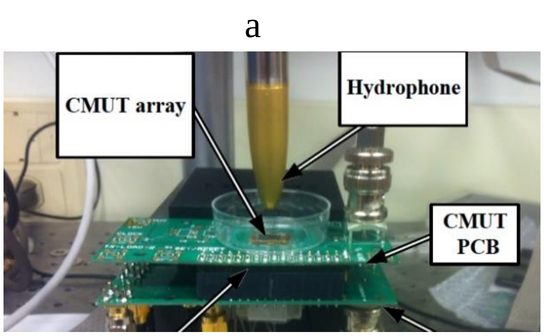
In order to achieve this goal, programmable Tx beamforming and Rx time division multiplexing technique is used. We used single cable for Tx beamformer at the catheter tip to load the data and the delays. The delays for different channels are implemented with a down counter and shift register. The system is designed to be operated and programmed at 20-MHz clock that corresponds to 5-ns relative minimum delay. The beamformer electronics is then connected to a high voltage pulser to generate the desired pulse.

In the Rx electronics design, time division multiplexing (TDM) technique is used to significantly reduce the number of cables. The received signal is first amplified using a low noise amplifier (LNA) with 3-dB bandwidth from 1-MHz to 12-MHz designed for 1D CMUT arrays that is suitable for ICE catheter. The amplified signal from each Rx 1D element, is then sampled at 25 MSPS, and then multiplexed into a 200 MSPS TDM channel using the same 200-MHz clock in Tx beamformer circuit. The noise measurement and design specifications can be found in [22, 23].

Beamforming capability of the 1D array in immersion has been measured and simulated. Immersion experiments were performed to characterize and test the performance of the fabricated 1D CMUT array. 16 elements of the CMUT arrays were first wirebonded to a secondary PCB, and then connected to the external electronics circuitry. A Petri dish was placed enclosing the CMUT array to be used as a water tank for the experiments – figure 4.18-a. A hydrophone (HNA-0085, Onda Crop., Sunnyvale, CA) was used to measure the 2D transmitted pressure field. For this purpose, the hydrophone was mounted on a XYZ stage connected to three linear actuators which were controlled by a motion controller (ESP 300, Newport Co., Irvine, CA).

The CMUT elements were excited by a 27-V unipolar pulse width of 65-ns pulse width without applying any bias voltage. A sample focused beam was generated on axis under immersion. The pressure signal was captured by the hydrophone located at the focal point with 32 averaging. Figure 4.18-b demonstrates the received hydrophone signals and the corresponding frequency spectrum showing ~8.5-MHz center frequency with 80% fractional bandwidth.

A non-steered plane wave was generated and a horizontal 1D scan with the hydrophone was performed to determine the center point of the scan by finding the maximum pressure location. A raster 2D scan on the XZ plane was then performed. The hydrophone was stepped in 100-µm increments to form a 6-mm x 6-mm plane using 3721 measurement points. Each point of pressure data for a particular scan location was averaged and captured for further analysis. The data was further processed to find the peak-to-peak pressure values for each raster point. Three different beam profiles were generated to demonstrate the functionality of the beamformer IC. The focal



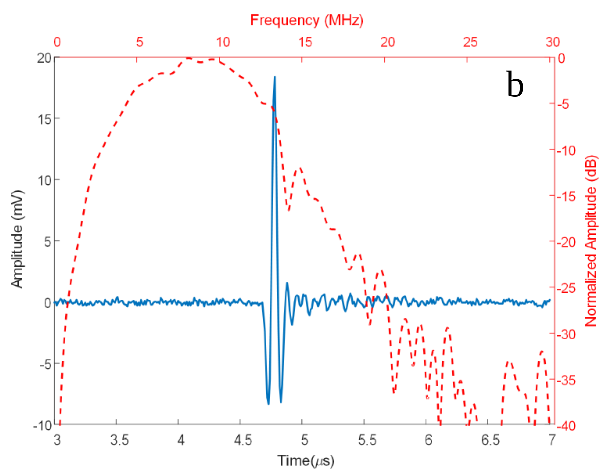


Figure 4.18. a) Immersion measurement setup with hydrophone. b) Time and frequency domain response of a single 1D element in an array.

point for the focused beams both in steered and non-steered cases was 4-mm and the steering angle was 25° for the steered beam (figure 4.19).

Simulated beam patterns were also calculated for the same array structure using Field II [24] and plotted together with the measured beam patterns in Figure 4.19. All beam pattern plots were normalized to their own maximum values. The measured beam patterns show close match with the simulated results up to -10-dB. The discrepancy between two plots especially on larger angles from the normal of the array is mostly due to decrease in the sensitivity of the hydrophone for large acceptance angle and non-uniformity of the array elements. The focal points in the beam pattern plots were observed as slightly closer than the actual focal distance because of the delay errors of the system and possible tilt on the raster scan plane in the elevation direction.

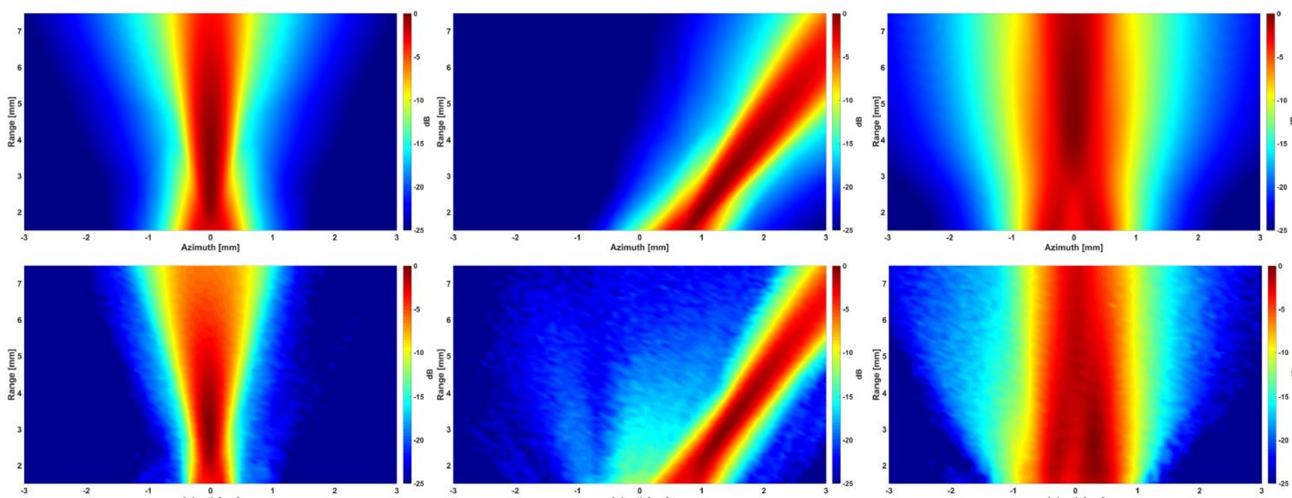


Figure 4.19. Simulated (top) and measured (bottom) beam patterns for non-steered focused beam (left), steered focused beam (middle), and plane beam (right).

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CHAPTER 5. CMUT-ON-CMOS PROCESS DEVELOPMENT SUITABLE FOR ICE APPLICATION

5.1 Monolithic CMUT-on-CMOS Integration

A significant premise of the capacitive micromachined ultrasound transducers (CMUTs) is electronics integration. Monolithic integration of CMUTs with CMOS electronics provides ultimately compact imaging systems where significant functionality of the front-end electronics can be realized right under the CMUT imaging array, practically eliminating parasitic capacitance to achieve near ideal signal to noise performance [1, 2, 3]. In addition, in sparce array that several small elements are connected to front-end electronics in a small area, other CMUT-ASIC connection methods such as flip chip bonding is not feasible. In CMUT-on-CMOS method, the CMUT fabrication is performed on the custom designed CMOS wafer instead of silicon wafer. The CMOS and CMUT layout is designed on a single mask file to ensure all the required Tx/Rx connections are aligned and located at the exact similar places. The CMOS wafer fabricated with 0.18-µm process, on 8-inch diameter wafers with ~720-µm thickness. In order to develop the process for CMUT-on-CMOS, the CMOS wafer needs to be diced in smaller wafers suitable for post-processing at Marcus nanotechnology facility located at Georgia Institute of Technology. We decided to dice the 8-inch CMOS wafer to 3 smaller wafers with 3.4-inch diameter. The CMOS can be diced with mechanical saw or laser cutting technique. The wafer is then thinned down to around 300-µm to shift the substrate ringing frequency of the CMOS substrate from 5-MHz to around 14-MHz [4]. The CMUT bandwidth is around 4-11-MHz and therefore the thinned wafer substrate resonance is beyond the bandwidth of interest, at ~14-MHz. Another important step before starting CMUT fabrication is the wafer planarization. It is very important to have a flat surface (< 5-nm roughness) because of the CMUT small vacuum gaps of about 10-nm. The incoming CMOS wafer has step height of about 2.5-μm that makes the CMUT fabrication impossible. The polishing process includes depositing of about 3-μm silicon nitride with a PECVD tool at 250°C temperature following by 3-μm chemical mechanical polishing (CMP) to reduce the topography of the CMOS wafer surface to about 25-nm in a line of 200-μm (figure 5.1). The CMP process degrades the quality of passivation silicon nitride layer and adds contaminations to the

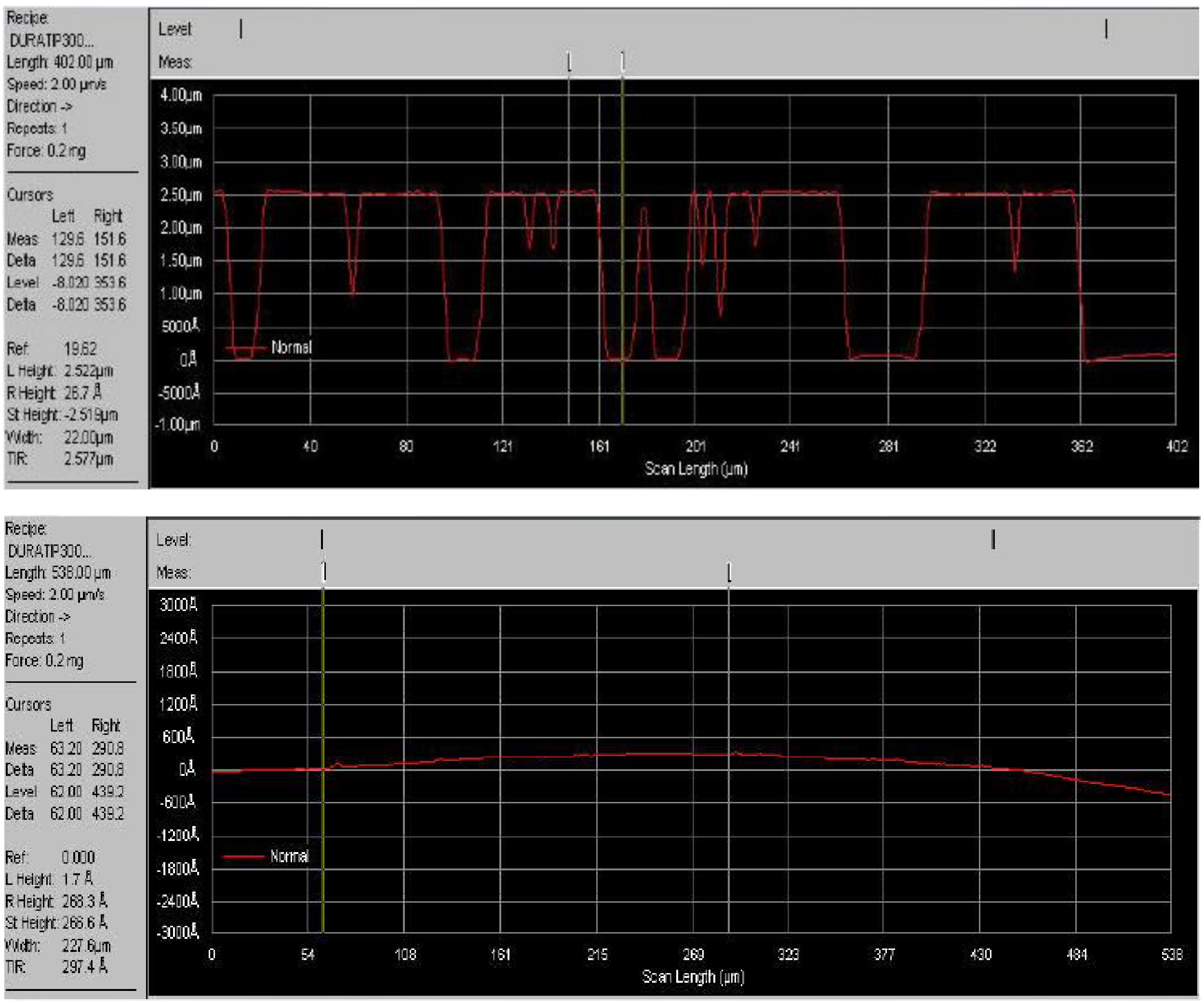


Figure 5.1. Top image is the topography of the surface before planarization. The bottom image is the surface after planarization. Topography reduced from 2.5-μm to 25-nm.

wafer surface. These contaminations will evaporate and re-deposit during post-processing processes especially in isolation layer (Si_3N_4) deposition that the temperature will rise up around 250°C. To avoid this contamination re-deposition, we etched 400-500-nm nitride layer with RIE to reach to a cleaner layer. To ensure the thickness of Si_3N_4 layer is sufficient to isolate the CMUTs from the beneath CMOS substrate, the similar thickness of about 400-500-nm of silicon nitride is deposited using PECVD. The fabrication process is very similar to the process that explained in chapter 3 [5] with 2 more set of photolithography and dry etching steps. Despite CMUT on silicon process that the CMUT arrays are externally excited, in CMUT-on-CMOS process, both bottom and top electrodes are connected to the CMOS substrate. The CMOS wafer connection pads are patterned and etched with RIE. Since ~3-µm silicon nitride is etched, AZ4620 photoresist with thickness of 7-µm is used to ensure the photoresist thickness is sufficient for the etching process. The critical difference between this etching – called slope etching – and the nitride etching discussed in chapter 3 is that the step needs to be covered with the top and bottom electrodes metal deposition and therefore, the sidewalls are required to be sloped – not vertical (figure 5.2) [6].

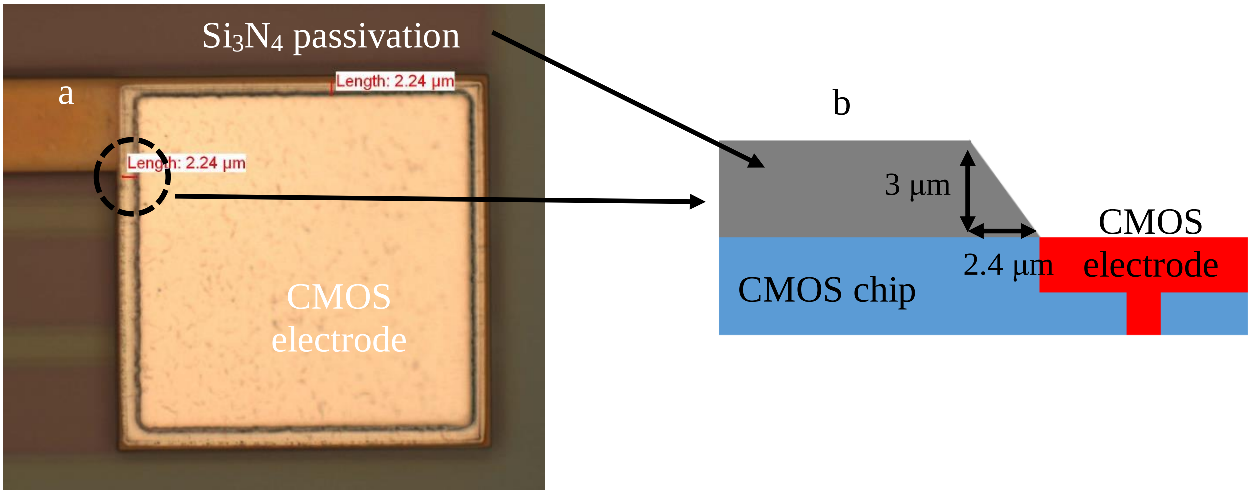


Figure 5.2. a) The top image of the etched silicon nitride and CMOS electrode. b) The side view schematic of the sloped etching process.

Table 5.1 describes the sloped etching recipe. The main difference between slope and common etching recipe (used in chapter 3) is the additional Argon (Ar) in the plasma that causes directionality of the etching process. Argon atoms are mainly responsible for physical etching while the chemical etching is mostly carried out by Oxygen (O_2) and Tri-fluoro-methane (CHF_3). In addition, Ar atom is heavier than O_2 and will not be freely scattered after bouncing back hitting a surface and eventually makes the etching plasma more directional [7]. Then the bottom electrode (Cr) is deposited using sputtering system to form the CMUT bottom electrode and connects the electrode to the CMOS chip. The rest of the process is similar to chapter 3. Figure 5.3 illustrates the micrograph for CMUT-on-CMOS wafer (figure 5.3-a), reticle (figure 5.3-b) and arrays. Several designs including 1D and 2D arrays, test structures and standalone CMUTs are included. The standalone CMUT arrays are included for the testing purpose to ensure if the CMUT arrays are successfully fabricated.

5.2 CMUT-on-CMOS Characterization

5.2.1 1D Array Characterization

CMUT 1D arrays have been fabricated and characterized in chapter 4. We fabricated similar

TABLE 5.1
Silicon nitride RIE slope etching

Parameter	Value
CHF3	45 sccm
O2	5 sccm
Pressure	40 mTorr
Power	300 W

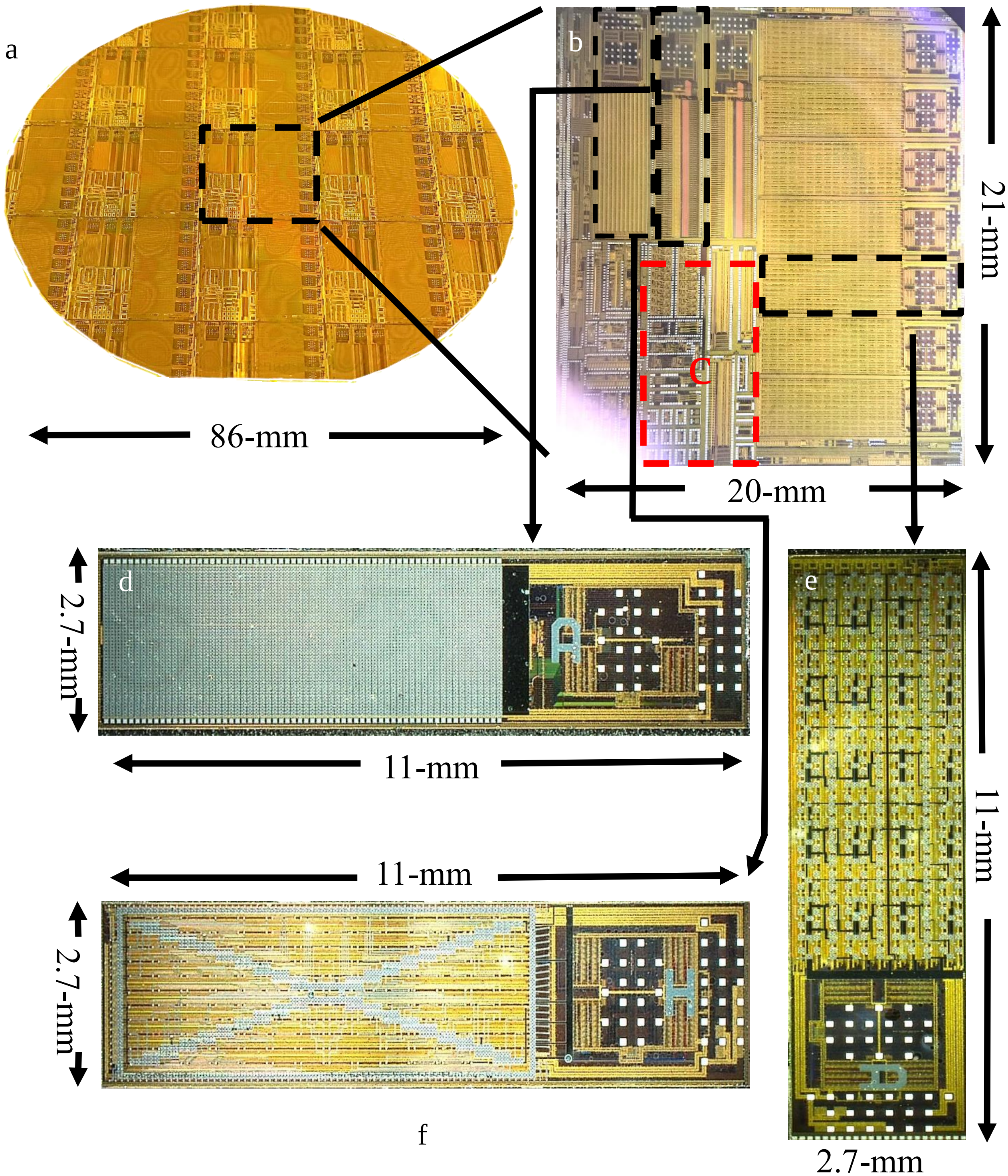


Figure 5.3. a) The CMUT-on-CMOS wafer run. b) The reticle size is 21-mm x 20-mm. c) Test CMOS and CMUT arrays. d) 1D array CMUT-on-CMOS design with electronics. e) 2D sparce array f) 2D cross array.

CMUT 1D array with CMUT-on-CMOS technique (Figure 5.3-d). The first step to ensure if the fabrication process successfully performed, is the C-V measurement of the test CMUTs. For a 1D array, the capacitance is typically changed around 2-pF when the voltage is swept from 0-V to 25-V. Each 1D array transducer comprises 64 1D elements (2x40 membranes – figure 5.3-d). We use common bottom electrode for the entire array and in our design, the elements can switch from Tx to Rx and vice versa. Since DC bias is required for Rx operation and all the elements can be either Tx or Rx, the transmit pulse is the combination of DC bias and a pulse optimized for ICE application. In our design, 20-V DC bias is constantly applied to all the CMUT arrays during both Rx and Tx operation.

The array performance and uniformity in transmit mode is measured using hydrophone (HGL-1000 series hydrophone, ONDA Corp., Sunnyvale, CA 94089) in a water tank. The CMUT 1D arrays are excited by 20-V pulse with 55-ns pulse width and the pressure is measured at 2-cm

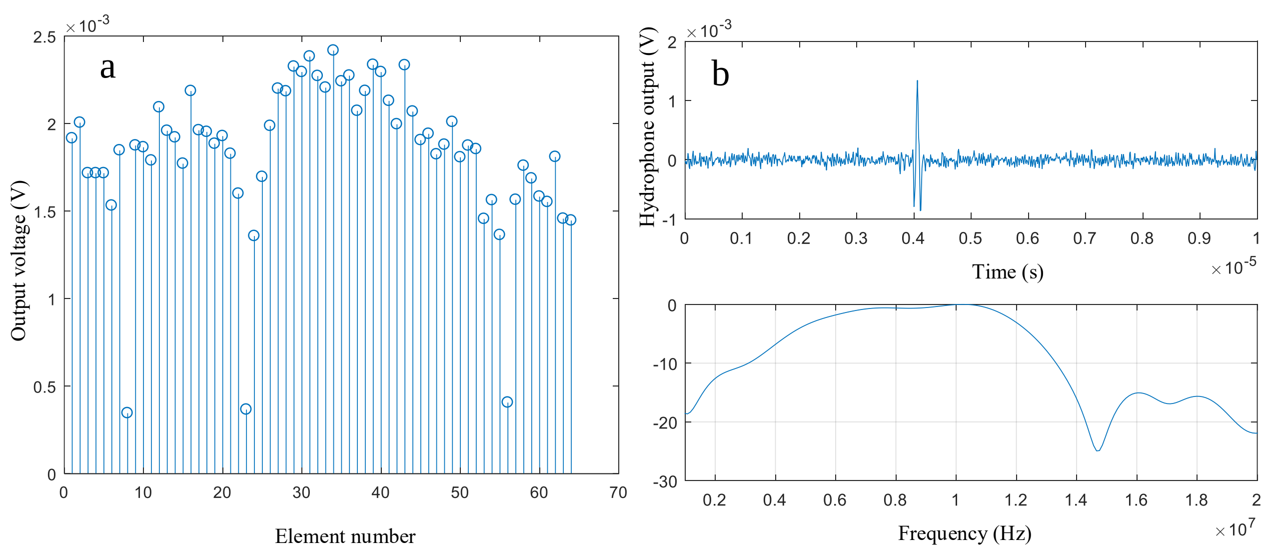


Figure 5.4. a) The uniformity of the CMUT array. b) Hydrophone output pressure (average) shows ~8.5-MHz center frequency with ~80% FBW.

above the CMUT 1D arrays for all 64 elements (figure 5.4). As mentioned before, 20-V dc bias is also constantly applied. The spectrum (figure 5.4-b) shows around 8.5-MHz center frequency with 80% fractional bandwidth (FBW). It can be seen that 61 arrays out of 64 (~95%) are functional showing acoustic response in immersion (Figure 5.4-a). The variation of the response can be due to the fabrication imperfection and hydrophone misalignment. The pulse-echo is also measured using an aluminium plate – as a perfect reflector. The plate is placed at 1-cm above the CMUT-on-CMOS 1D array. 1 element (80 membranes) is excited with 20-V pulse with 65-ns pulse width and the echo signal is received by the same element. Figure 5.5 illustrates the pulse echo signal in frequency domain.

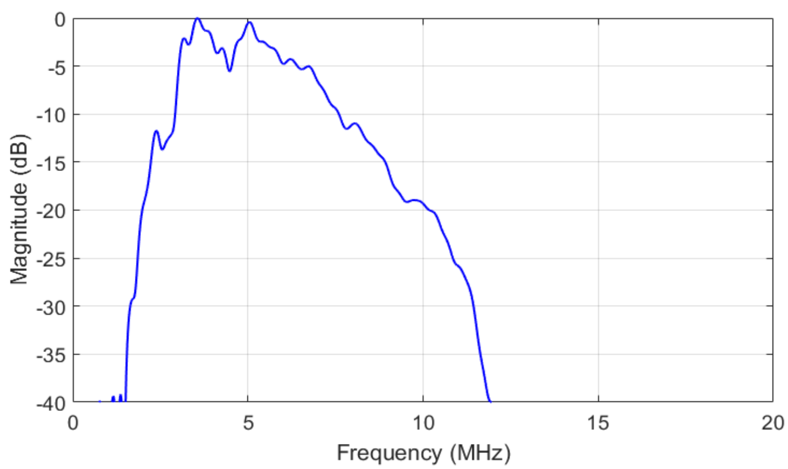
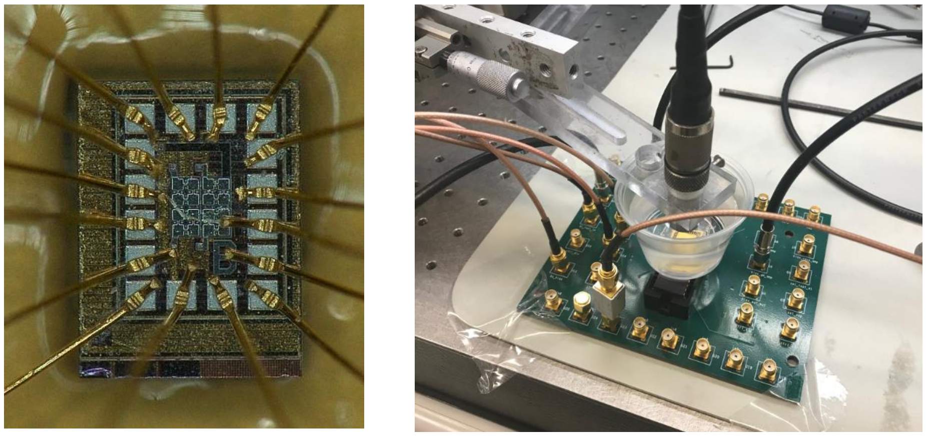


Figure 5.5. The pulse-echo response of the CMUT-on-CMOS array.

5.2.2 2D Array Characterization

In order to characterize the test 2D element (4 membranes – figure 5.6-a), the transmit and receive sensitivity are separately tested. For Tx characterization, a hydrophone is placed at a distance of about 2-cm above the CMUT array and the pressure is measured. The CMUT is excited by 40, 45 and 50-V pulse with 55-ns pulse width (figure 5.7-a) and the surface pressure is calculated. The maximum Tx sensitivity on the CMUT surface is about 25 kPa/V. For Rx sensitivity, the CMUT is excited by an external piezoelectric transducer and the output current is measured (figure 5.6-b).

a



b

Figure 5.6. a) The wirebonded test 2 D element on PCB. b) Rx test setup when the CMUT is excited by a piezoelectric transducer and the output current is measured.

The receive signal from a 2D CMUT element (4 membranes) is not sufficient to be read with a typical oscilloscope so the element is connected to a transimpedance amplifier (TIA) with a resistive feedback depicted in figure 5.8. The feedback resistor determines the gain of the TIA and since the input current of TIA is negligible, the output voltage (V_{out}) is equal to the voltage over the feedback resistor. Higher feedback resistor leads to a larger TIA gain however, the output voltage level and dynamic range will be limited. In our design, the feedback resistor is 50-kΩ that means 90-dB current to voltage gain explained in figure 5.8 – Eqn. 4.3. For example, 1-μA CMUT output current results in 50-mV TIA output voltage.

There is a trade-off between TIA gain and dynamic range. We previously used a 3-MΩ resistor feedback for our TIA resulted in 130-dB gain that was suitable for IVUS application however, the dynamic range is relatively low ~ 20-dB [1].

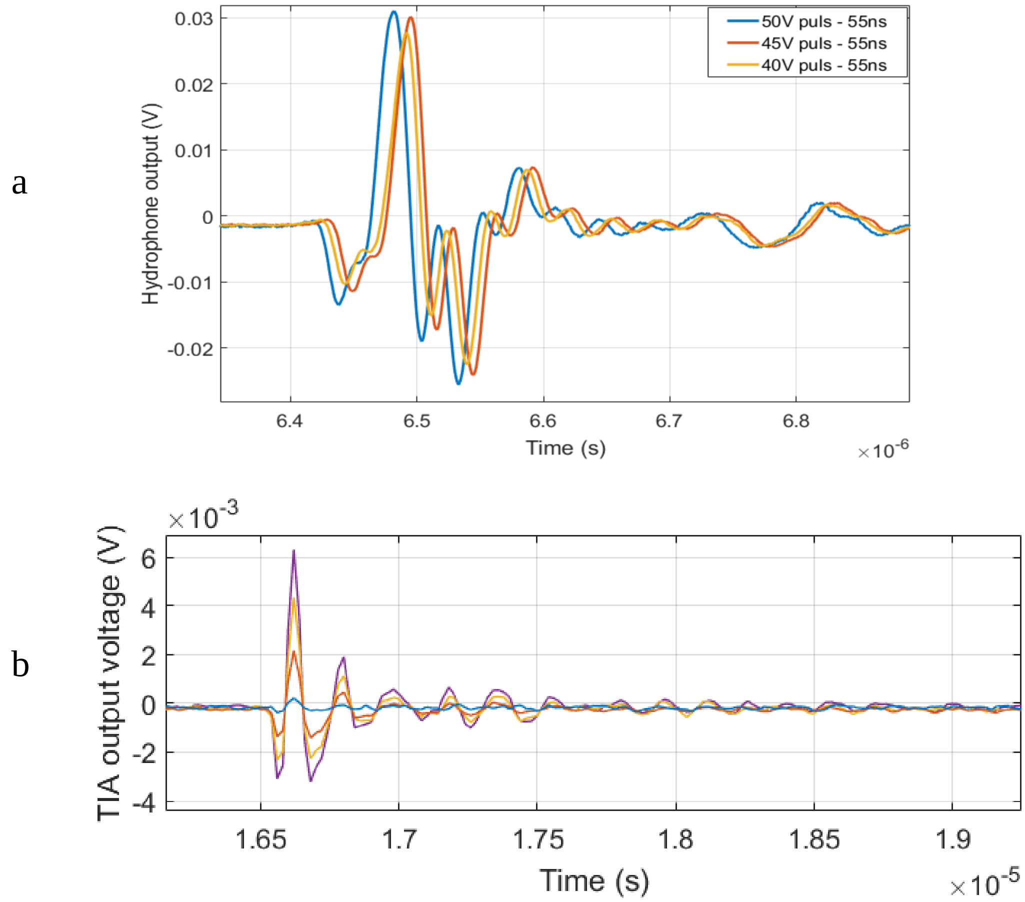
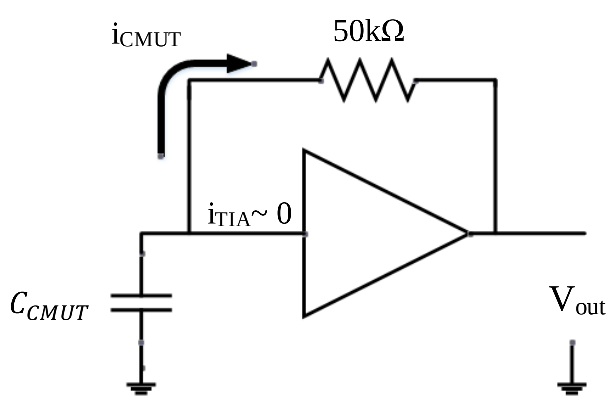


Figure 5.7. a) Output voltage of the hydrophone when the CMUT is excited by different pulses (Tx mode). b) TIA output voltage with different DC biases in Rx mode (0,10,20, 30-V).



$$V_{out} = i_{CMUT} \times 50k\Omega \qquad \textit{Eqn. 4.3}$$

Figure 5.8. The simplified configuration of CMUT connected to the TIA.

The Rx sensitivity highly depends on the DC bias, and as it discussed in chapter 2, the goal is to bias the Rx CMUT close to collapse voltage. Figure 5.7-b implies that TIA output voltage is increased when we apply more DC bias on the Rx CMUT. The maximum sensitivity is ~1-mV/kPa that occurs when the CMUT is biased with 30-V DC (~90% of collapse voltage).

One of the important characteristics of CMUT-ASIC system integration is the noise floor of the entire system that limits the minimum detectable pressure (MDP). CMUT is not able to detect a quantity below the MDP. In our measurement we assume the CMUT thermal-mechanical (TM) noise is dominant the TIA noise. CMUT-on-CMOS TM noise is measured by connecting the chip to the network analyzer – Agilent 8753ES. The noise level is maximum at device resonance frequency and is increased with DC bias. Figure 5.9 illustrates the noise measurement results in air. The CMUT resonance frequency in air is around 12-MHz at which the noise is measured, and it is observed that bias voltage increases the noise level. The maximum noise voltage on the output of TIA is ~8e-8-$V/\sqrt{Hz}$ that corresponds to input referred noise of about ~1.6e-12 pA/√Hz.

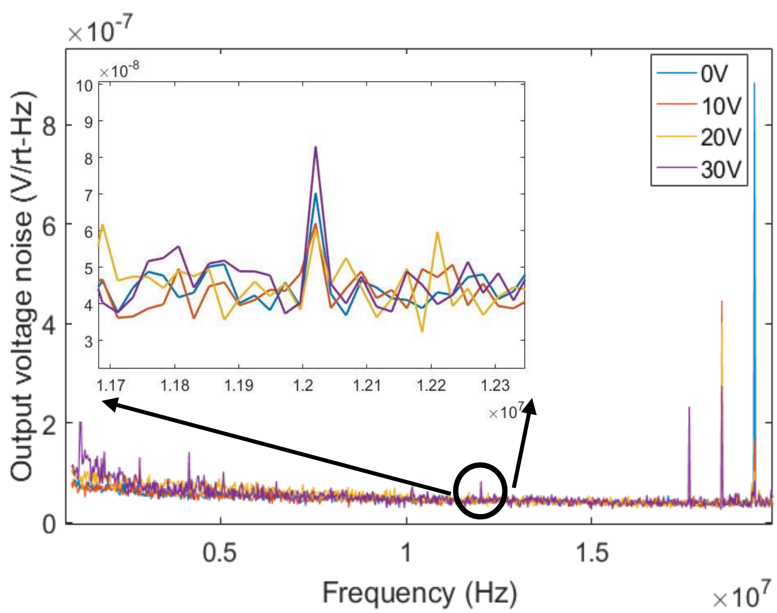


Figure 5.9. The noise measurement in frequency domain.

The Rx sensitivity is also measured as 1-mV/kPa that results in minimum detectable pressure (MDP) of about 80-mPa/√Hz.

5.3 Imaging Experiment and Results

We designed and fabricated both 1D and 2D arrays with CMUT-on-CMOS technique however, duo to the limited number of channels and challenging system implementation and data collection for high-density 2D arrays, we have only tested the 1D array for ICE imaging.

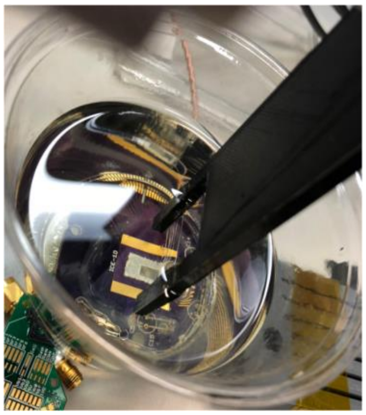
For imaging experiments to demonstrate the imaging capability of the 1D CMUT-on-CMOS ICE arrays, we constructed a custom setup for data collection. We first wirebonded the fabricated 1D ICE CMUT array to a custom designed PCB and placed small petri dish on the top of the PCB which was filled with water – figure 5.10-a. As it was shown in figure 5.5, the pulse-echo measurement results in 5-MHz center frequency with 80 % of -3-dB fractional bandwidth, which is suitable for ICE imaging.

The details of CMOS chip design and measurement are described in [8]. We used programmable transmit (Tx) beamforming method and receive (Rx) time-division multiplexing (TDM) technique for the cable reduction purpose, similar to the circuitry we used in chapter 4. The ASIC is designed for driving a 64-channel 1D transducer array suitable for ICE catheters. The ASIC is implemented in 60-V 0.18-μm HV-BCD technology, integrating Tx beamformers with high voltage (HV) pulsers and Rx front-end in the same chip, which occupies 2.6×11-mm^2 that can fit in the catheter size of 9 Fr (<3-mm).

Imaging experiments were performed using 7 metal wires (38-AWG, 101-μm in diameter). The CMUT-on-CMOS chip was immersed in the water and facing 7 wires vertically as shown in Figure

5.10-a. Transmitter arrays send steered beams to scan ±45° sector image and the data is collected after each firing. The obtained image has 40-dB of dynamic range, which clearly shows 7 wires – figure 5.10-b [8]. The details of the system implementation and imaging can be found in [9].

a



b

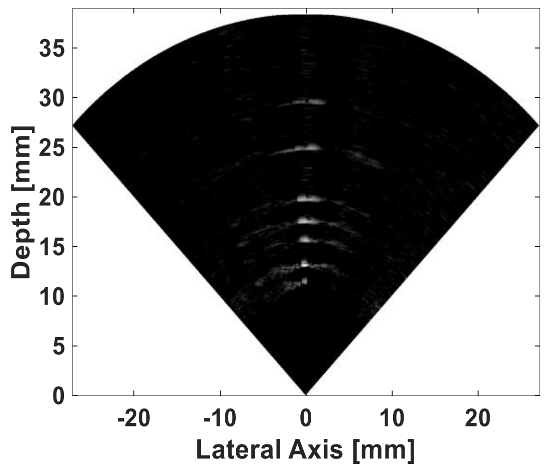


Figure 5.10. a) The imaging measurement setup with petri dish. b) B-mode image of 7 metal wires in the water.

5.4 REFERENCES

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CHAPTER 6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusion

The objective of this research was to design and fabricate suitable CMUT arrays for the intracardiac echocardiography (ICE) catheter with the tip size of about 2.7-mm x 11-mm. In addition, we have developed a low temperature fabrication process for monolithic integration of CMUTs with custom CMOS electronics. We also developed a new fabrication method to significantly improve the reliability of conventional CMUTs, reducing the charging of the device that eventually results in performance improvement. In addition, we developed a new calculation method – called energy conversion ratio - to evaluate the performance of the CMUT arrays in a large signal operation that leads to device assessment in high power and continuous wave mode.

6.2 Contributions

6.2.1 *Energy Conversion Ratio Analysis*

In many applications, the CMUTs are operated with large input signals, in either pulse or continuous mode, to increase the output pressure. In order to evaluate the performance of the CMUTs in large signal mode, an energy-based method – energy conversion ratio (ECR) - is described and derived using a nonlinear CMUT model.

First, we described how to use this large signal model to evaluate a simple expression to determine the mechanical energy stored in the CMUT, both in small and large signal operation regime. A small signal coupling coefficient based on ECR is then verified by comparison with the usual definitions. We then used ECR to analyse and compared large signal CMUT operation with

DC biased and AC only operation. We then employed ECR to assess the large signal efficiency of a CMUT with uniform and non-uniform membrane to demonstrate optimization capability.

The validity of the mechanical energy prediction was also tested experimentally through an output pressure spectrum and intensity measurements, by a hydrophone, for a CMUT element similar to our simulation element.

6.2.2 *CMUT Array Design and Fabrication for ICE application*

As part of CMUT array development, we first described a modified low temperature CMUT fabrication process where a new lift-off step is introduced into the process flow. This step deposits a thick dielectric layer between the TE and BE, except for the regions where there is a CMUT membrane. Lift-off step is a self-aligned process that blocks all the leakage paths with adding only one step to the fabrication process.

Subsequently, we went over a specific CMUT device design for ICE applications fabricated with this process. We present electrical and acoustic measurements showing functionality with reduced parasitic capacitance. We further compared the reliability of the devices with and without the lift-off step to demonstrate the improvement.

6.2.3 *CMUT-on-CMOS Integration*

Monolithic integration of CMUTs with custom CMOS electronics has been accomplished for different array sizes and designs. In this technique, CMUTs electrodes are connected to the CMOS chip through vias that are dry etched by the RIE process, following with a common metallization procedure. In order to ensure the CMUT and ASIC electrodes are connected, we employed the slope etching technique, in which the side walls are sloped and the steps are all covered by metals. Figure 6.1 illustrates the 1D and 2D array CMUT-on-CMOS chip.

The proposed CMUT-on-CMOS system occupies 2.6×11-mm^2 and reduces the number of wires from over 64 to only 22 with potential for larger reduction in 2D arrays. We successfully demonstrated the functionality of all system blocks in the ASIC chip. The signals show 5-MHz center frequency with 80% bandwidth, which is suitable for ICE catheters.

a

b

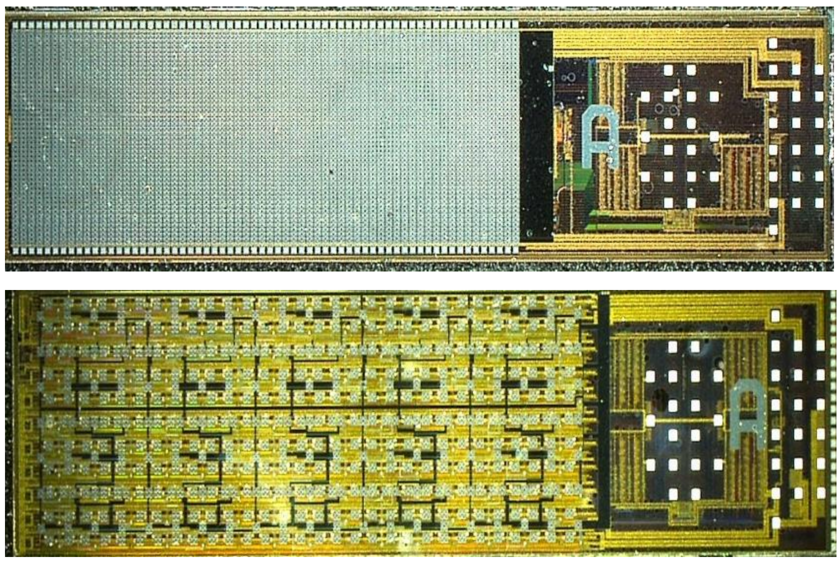

Figure 6.1 a) 1D CMUT-on-CMOS array. b) 2D CMUT-on-CMOS array.

6.3 Future Work

The energy conversion ratio (ECR) is proposed and the mechanical energy has been validated through comparing CMUTs pressure measurement with our simulation results. The validation can be extended to total energy measurement and simulation and subsequently, ECR.

The oxide lift-off technique improved the reliability of the CMUT arrays. For the lift-off step, other dielectric materials with different dielectric constant and different heights can be explored. Based on the theory, lower dielectric constant results in parasitic capacitance reduction and CMUT performance improvement.

The functionality of 1D CMUT on CMOS process has been demonstrated. Transmitter and receiver performance and pulse-echo measurement indicated successful CMUT on CMOS integration. We have 2 amplifier designs for receiver circuitry; low noise amplifier (LNA) and transimpedance amplifier (TIA). We have collected data from the LNA-based system and the images from wire targets have been constructed, indicating the functionality of the entire transducer and ASIC system. We plan to explore more devices to optimize our signal conditioning, pulse properties and image reconstruction method.

The TIA-based CMUT on CMOS devices should be explored further. The sensitivity of transmitter and receiver elements can be measured, and the elements uniformity data can determine the yield of integration process. The image from wires target will be reconstructed and compared with LNA based systems.

Several 2D array designs were fabricated and integrated with the CMOS chips. The sensitivity of transmitter and receiver and pulse-echo have been measured for small 2D test arrays however, it is still challenging to measure pulse-echo for the entire array. One important plan is to implement our data collection setup for 2D arrays.

The CMUT-on-CMOS packaging and placement on the tip of the catheter significantly affects the performance of the entire system. Different passivation materials can be studied to understand the effects of passivation materials on the overall system performance. The packaging of an entire CMUT-on-CMOS system can also be investigated to achieve suitable packaging material for real ICE application.

The successful integration method that was used in this dissertation is the monolithic integration of CMUT on the ASIC wafer. Other integration methods including flip-chip bonding can be explored to compare the yield, efficiency and cost of the CMUT-ASIC integration.