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Impact of transmission topology for protective operations in multi-terminal HVDC networks

Sul Ademi[1], Richard McMahon[1], Lianchen Zhu[2], Ramtin Sadeghi[3],

[1]Warwick Manufacturing Group, University of Warwick, Coventry, UK
[2]School of Electronic and Information Engineering Liaoning Anshan, CN 114051, China
[3]Dept. of Electrical Engineering, Faculty of Engineering, University of Isfahan, Isfahan, Iran

Abstract—This paper presents an outcome of a comprehensive study which evaluates the transient behaviour of point-to-point and multi-terminal high voltage direct current (MT-HVDC) networks. The behaviour of the HVDC system during a permanent pole-to-pole and pole-to-ground fault is assessed considering a range of fault resistances, fault positions along the line, and operational conditions. The emphasis of this investigation is on DC fault characteristics which would facilitate a reliable method of faulty line discrimination in a multi-terminal direct current (MTDC) system using local measurements only (i.e. assuming that no communication media is used). All the simulated waveforms (and subsequent analysis) utilise the sampling frequency of 96 kHz in compliance with IEC-61869 and IEC-61850:9-2 for DC-side voltages and currents.

I. INTRODUCTION

In recent years, voltage source converter high-voltage direct-current (VSC-HVDC) transmission systems have become competitive compared to systems that employ thyristor current source converters in terms of power handling capability, DC operating voltage and technology maturity [1]. Such improvements have been realised employing two-level converters with series connected insulated gate bipolar transistors (IGBTs) and modular multilevel converters (MMCs) [2]. Such architectures are expected to be the technology of choice for efficient AC/DC grid integration, although barriers for the deployment of HVDC systems is the clearance of DC-side faults.

Fault vulnerability and the requirement for ultra high-speed protection are the major issues that constrain the development of VSC-based DC networks [2], particularly high-power MT-HVDC networks. Similarly to power system protection in AC systems, the isolation of a faulted DC line can be achieved by the dedicated DC circuit breakers installed at both ends of the line. This approach is suggested by a number of studies [3], however, the development of such breakers for high-voltage DC applications presented a challenge since there is no zero crossing current. Therefore, such a breaker would have to actively drive the current to zero and dissipate the energy stored in the system inductance [4]. The VSC-based transmission systems are robust to the fault conditions on the AC-side, however, the most critical challenge for VSC-HVDC systems lies in its response to DC-cable faults [5]. Unfortunately, the two-level VSCs are defenceless against DC-side faults since their freewheeling diodes function as uncontrolled bridge rectifier feeding the DC fault from the AC side [6], [7]. Efforts to characterise the pole-to-pole/ground faults for VSC systems are carried out [7], [8], but further in-depth analysis into the converters behaviour is desired to improve the understanding of the system response to fault conditions, and thus aid the development of effective DC protection methods.

This paper is an extension to the work in [9] by presenting a detailed analysis on the behaviour of a VSC-HVDC during the DC pole-to-pole and pole-to-ground faults for two-level and half-bridge submodule (HB-SM) converter systems. Such thorough study evaluates and gives a comprehensive synopsis on the DC fault characteristics and their transient behaviours, while addressing the utilisation of inductive termination installed at each end of the dedicated networks. Such study aims to provide an insight into the voltage and current fault signatures which could aid towards a reliable acumen amongst internal and external faults.

II. HVDC FAULTS

A. Pole-to-pole faults

Such faults occur as a result of direct contact or insulation breakdown between positive and negative conductors of a DC cable but such fault are not common, however, they can be severe to the system [7]. The HB-MMC converter arrangement during a pole-to-pole fault can also be classified into three sequential stages, however, due to the lack of DC-link capacitor the initial response is somewhat different to the aforementioned two-level converter topology [8].

B. Pole-to-ground faults

Faults of such nature are more common but they are less harmful to the system. In practice such faults are triggered when the insulation of the cable breaks and the live conductor gets in contact with the ground. During this type of faults the earthing arrangement of the converter plays a decisive role, as different current loops can be formed. Various earthing configurations can be achieved, but there is no specific standard in this respect, especially for MTDC networks [6]. Ground fault resistance cannot be ignored as its value can vary significantly, hence it is considered as one of the influencing factors in the short-circuit analysis. Assuming a Δ/Y_g transformer (with the

Y winding on the converter side) and mid-point earthed DC-link capacitors, a pole-to-ground fault for a two-level converter can be analysed systematically [7]. In MMC configuration with the same earthing arrangement of the transformer, the analysis of a pole-to-ground fault is much simpler. In fact since the DC-link capacitor is absent, the pole-to-ground fault evolves only around the steady state [8], which is initiated after the blocking of the IGBTs. Again, in this case the faulty-pole voltage collapses to zero, while the healthy pole voltage rises towards 2 p.u., similarly to the two-level converter.

III. System Modelling and Control

For the purpose of fault transient analysis two-level converter and half-bridge modular multilevel converter (HB-MMC) are investigated. The two-level converter is developed utilising detailed modelling of semiconductor devices, whilst the HB-MMC model is 201-level Type 3 and is developed utilising analysis in [10]. Specifically, the entire MMC is represented by the controlled voltage and current sources (Fig. 1). In equations and symbols describing the operation of the MMC index j defines the phase ($j = a, b, c$) and index k defines the upper and lower position of the arm ($k = u$ for upper arm and $k = l$ for lower arm) in (1) and (2) respectively.

$$v_{ctr(j,k)} = v_{Ctot(j,k)} \cdot s_{(j,k)} \tag{1}$$

$$i_{ctr(j,k)} = i_{(j,k)} \cdot s_{(j,k)} \tag{2}$$

where $s_{(j,k)}$ is the sum of switching functions of the arm (j,k) as defined in (3), $v_{Ctot(j,k)}$ is the sum of all capacitor values of an arm and $i_{(j,k)}$ is the current flowing through the corresponding arm of each phase.

$$s_{(j,k)} = \frac{1}{N} \sum_{i=1}^{N} s_{(j,k)(i)} \tag{3}$$

where N is the number of sub-modules and $s_{(j,k)(i)}$ is the switching function of each sub-module.
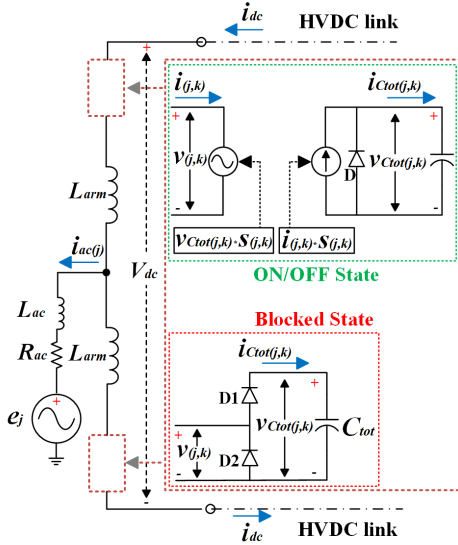

Fig. 1. A detailed single-phase representation of the MMC Type 3 model.

In order to satisfy a successful operation of an MMC the corresponding expressions (4)-(6) consequently define the DC voltages which must be satisfied simultaneously under all conditions and for each phase $j = a, b, c$ accordingly.

$$V_{dc} = v_{(j,u)} + v_{(j,l)} \tag{4}$$

where $v_{(j,u)}$ and $v_{(j,l)}$ are the output voltages of upper and lower arm respectively (in phase j). The total voltage of each arm composites half of the DC voltage and it can be expressed for upper and lower arms by (5) and (6) respectively.

$$\frac{V_{dc}}{2} = v_{(j,u)} + L_{arm}\frac{di_{(j,u)}}{dt} - L_{ac}\frac{di_{ac(j)}}{dt} - R_{ac} \cdot i_{ac(j)} + e_{(j)} \tag{5}$$

$$\frac{V_{dc}}{2} = v_{(j,l)} + L_{arm}\frac{di_{(j,l)}}{dt} + L_{ac}\frac{di_{ac(j)}}{dt} + R_{ac} \cdot i_{ac(j)} - e_{(j)} \tag{6}$$

where L_{arm} and L_{ac} are the arm and AC-side inductance respectively (as shown in Fig. 1), R_{ac} is the AC-side resistance, and $e_{(j)}$ is the AC-side grid phase voltage. The upper and lower arm current in each phase can be expressed by (7) and (8) respectively.

$$i_{(j,u)} = \frac{i_{ac(j)}}{2} + i_{diff(j)} \tag{7}$$

$$i_{(j,l)} = -\frac{i_{ac(j)}}{2} + i_{diff(j)} \tag{8}$$

where $i_{ac(j)}$ is the output/input AC phase current and $i_{diff(j)}$ is the differential current in each phase. Such current flows through the upper and lower arms without having any effect on the AC current and can be defined as:

$$i_{diff(j)} = \frac{i_{(j,u)} + i_{(j,l)}}{2} = i_{dc(j)} + i_{cc(j)} \tag{9}$$

$$i_{dc} = i_{dc(a)} + i_{dc(b)} + i_{dc(c)} \tag{10}$$

where $i_{dc(j)}$ is the DC phase current and $i_{cc(j)}$ is the circulating current which occurs due to the unbalance of the upper and lower arm voltages of each phase [11]. The voltages in upper and lower arm can be expressed as in (11) and (12) respectively, taking the neutral point of the DC link as a reference point.

$$v_{(j,u)} = L_{arm}\frac{di_{(j,u)}}{dt} = v_{diff(j)} - v_{ac(j)} \tag{11}$$

$$v_{(j,l)} = L_{arm}\frac{di_{(j,l)}}{dt} = v_{diff(j)} - v_{ac(j)} \tag{12}$$

where $v_{diff(j)}$ is the differential voltage between the upper and lower arm and can be considered as the inner e.m.f generated in each phase and can be expressed as:

$$v_{diff(j)} = \frac{V_{dc}}{2} - v_{(j,u)} = -\frac{V_{dc}}{2} + v_{(j,l)} = \frac{v_{(j,l)} - v_{(j,u)}}{2} \tag{13}$$

By amalgamating (7), (8), (11) and (12) the relationship between AC phase current $i_{ac(j)}$, the inner e.m.f $v_{diff(j)}$ and the AC phase voltage $v_{ac(j)}$ can be formulated as:

$$e_{(j)} = \left(\frac{L_{arm}}{2} + L_{ac}\right)\frac{di_{ac(j)}}{dt} + R_{ac} \cdot i_{ac(j)} + v_{diff(j)} \tag{14}$$

Converters AC current is therefore regulated by controlling the inner e.m.f $v_{diff(j)}$, thus, the classic current vector control strategy for conventional three-phase converters is applied by decoupling the controlled quantities in the corresponding $d-q$ frame alignments. An outer power controller and an inner current controller can also be employed in MMC, similar to that in Fig. 2. To control the AC current, the Clark-Park transformations are utilised to transfer (14) into the $d-q$ frame and the corresponding reference signals are described by (15) and (16) accordingly.

$$v_d^* = -(i_d^* - i_d)\left(K_p + \frac{K_i}{s}\right) + e_d - \left(\frac{L_{arm}}{2} + L_{ac}\right)\omega \cdot i_q \tag{15}$$

$$v_q^* = -(i_q^* - i_q)\left(K_p + \frac{K_i}{s}\right) + e_q + \left(\frac{L_{arm}}{2} + L_{ac}\right)\omega \cdot i_d \tag{16}$$

where i_d^* and i_q^* are the reference signals from outer controller, i_d, i_q, e_d and e_q are the measured AC currents and voltages for d and q frame respectively, k_p and k_i are the PI-control parameters and ω is the fundamental frequency of the network. Fig. 2, illustrates the structure of the controller where the coupling and linearisation is performed according to [10]. In order to eliminate the circulating current $i_{cc(j)}$ which has a double fundamental frequency in the differential current in each converter leg, a Proportional Resonant-Circulating Current Suppression Controller (PR-CCSC) has been added to the main controller algorithm as described in [12]. Such controller will output a supplementary voltage reference v_{abc-2f}^* which will be utilised during coupling and linearisation process. In
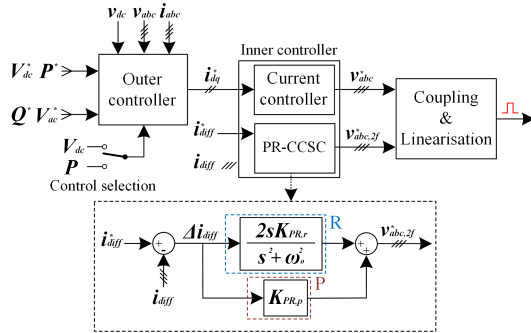

Fig. 2. Schematic diagram of the control structure for the HB-MMC detailing the entire control structure of MMC and control structure of PR-CCSC.

order to emulate the over-current protection function of each sub-module, a DC fault current controller has been included in the operation of the converter. In this case the converter would behave as an uncontrolled rectifier as shown in Fig. 1 (blocked state). This is achieved by setting the control signal $v_{ctr(j,k)}$ in (1) to 0. The over-current threshold has been set to 1.5 kA according to [13]. The converter parameters for two-level and HB-MMC are enlisted in Table I.

A. HVDC Networks

The two-level VSC and half-bridge MMC architectures described in Section III have been employed in the case study networks. In particular, the fault analysis which has been carried out for point-to-point transmission system includes

TABLE I
CONVERTER PARAMETERS

Parameter	HB-MMC	Two-Level VSC
DC Voltage $[V_{dc}]$	± 400 kV	± 400 kV
DC-Link Capacitance $[C_{dc}]$	-	40 μF
IGBT $[R_{on}]$	1 mΩ	1 mΩ
Arm Inductance $[L_{arm}]$	2.3 mH	-
Sub-module Capacitance $[C_{SM}]$	50 μF	-

both converter architectures (although not included in the paper for space reasons), while in the case of MTDC system (Fig. 3) only MMC based approach is considered.
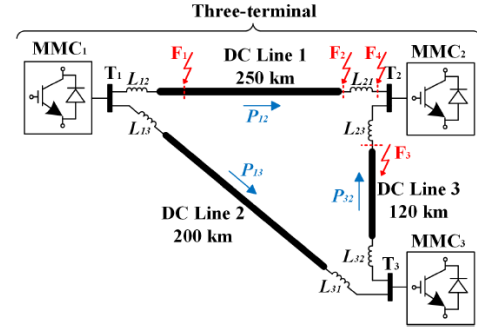

Fig. 3. HVDC networks investigated as separate of three-terminal network.

The DC cable model is based on the Bergeron's travelling wave method (also used in the Electromagnetic Transient Program (EMTP) [14]). Each transmission line is terminated with inductors L_{dc}=100 mH to limit the rate of rise of current in the case of the fault. Additionally as described in [15] such inductive cable termination can assist in the faulty line discrimination based on the DC voltage signatures imposed by the inductors. Network parameters used for the AC grid and DC cable model are presented in Table II.

TABLE II
DC CABLE AND AC NETWORK PARAMETERS

Parameter	Value
DC Cable Resistance $[R_{DC}]$	15.0 mΩ/km
DC Cable Inductance $[L_{DC}]$	0.96 mH/km
DC Cable Capacitance $[C_{DC}]$	0.012 μF/km
AC Voltage (L-L, RMS)	400 kV
AC Frequency	50 Hz
X/R Ratio of AC Network	10
AC Short-Circuit Level	2 GVA
Interfacing Transformer Voltages	400/400 kV

IV. SIMULATION-BASED FAULT ANALYSIS

This section includes comparative analysis of the HVDC network transients during DC faults for point-to-point and MTDC networks. The natural response of the converters has been investigated to provide the basis for the development of fast and highly discriminative DC protection method to ensure that the DC-line faults are isolated in such a way as to permit the VSC station to ride through the fault and remain connected to the DC grid. To comply with the IEC-61869 and IEC-61850:9-2 standards the simulated DC currents and voltages have been re-sampled at 96 kHz (in conjunction with the anti-aliasing filter applied prior to re-sampling). In all presented case studies the distance to fault is measured from the sending end of each line (indicated by the arrows in Fig. 3).

A. Point-to-point HVDC network

An automated simulation routine was developed to iteratively change the fault position and resistance in order to capture the natural response of the system under a variety of fault conditions. Due to space limitations those waveforms are not included here, however, they follow very similar pattern to those presented in [9]. Based on these waveforms the rate of change of DC current (di/dt) and voltage (du/dt) have been calculated. For VSC-HVDC applications it is believed that the transient current components are more applicable in protection as the DC capacitors form the fundamental boundaries of the DC transmission [16]. Nevertheless, in order to offer a better insight into the fault response, maximum values of du/dt are also included in Table III. For the two-level converter, it was

TABLE III
VALUES OF CURRENT [KA/S] AND VOLTAGE DERIVATIVES [MV/S].

R_f [Ω] →	25		50		100		200		300		0 (pole-to-pole)	
Dist. [km] ↓	di/dt	du/dt	di/dt	du/dt	di/dt	du/dt	di/dt	du/dt	di/dt	du/dt	di/dt	du/dt
Two-level												
5	1601.1	25.4	1341.1	22.5	997.8	18.3	642.4	13.3	465.6	10.5	3641.2	252.4
25	1548.6	24.9	1308.9	22.1	991.6	18.1	656.2	13.3	484.3	10.5	3126.4	230.8
50	1460.7	24.1	1250.8	21.5	961.5	17.7	647.2	13.1	483.5	10.3	2714.7	210.3
100	1375.4	21.4	1186.6	19.4	928.1	16.3	642.4	12.3	488.6	9.9	2116.8	178.5
125	1110.5	21.8	970.4	19.5	788.2	16.1	571.4	12.0	444.5	9.7	2286.8	169.3
150	1020.3	22.7	886.1	20.1	700.8	16.4	492.6	12.0	380.8	9.6	2406.7	159.9
200	964.0	21.0	854.4	18.7	695.0	15.4	503.5	11.4	392.6	9.0	2401.1	148.3
225	881.8	18.9	788.5	16.9	650.0	14.0	478.7	10.4	376.7	8.2	2395.8	141.6
250	913.2	17.1	764.0	15.3	581.0	12.7	433.7	9.4	344.0	7.5	2392.5	136.3
295	905.9	13.5	752.5	11.8	547.0	9.7	407.1	7.2	325.2	5.7	2402.5	131.6
HB-MMC												
5	1298.2	61.2	1086.5	52.4	807.2	44.0	520.4	38.2	374.1	31.8	1630.6	790.7
25	1259.0	59.2	1067.3	53.4	809.4	45.8	537.3	37.2	394.0	32.1	1616.0	792.2
50	1216.3	57.7	1041.1	51.0	804.0	45.2	544.7	37.6	404.8	32.5	1261.7	825.3
100	1154.8	77.2	1003.7	64.3	791.5	53.6	546.6	41.9	409.2	35.2	1450.3	761.5
125	1024.4	71.8	886.7	64.3	705.8	53.8	496.0	41.6	375.5	35.1	1535.1	775.8
150	968.2	78.3	839.3	64.1	661.8	53.7	461.7	41.8	352.2	35.1	1525.4	791.6
200	946.3	83.8	842.2	70.2	689.1	53.5	503.1	41.5	394.2	34.8	1506.8	793.0
225	884.7	81.6	802.0	64.9	671.9	53.6	502.3	43.7	398.6	37.1	1497.8	793.2
250	874.8	71.3	743.5	65.8	609.9	57.2	462.7	46.4	371.2	39.9	1488.3	793.4
295	933.1	64.0	784.2	58.5	581.8	51.5	391.8	46.1	315.2	39.6	1495.5	792.5
	Pole-to-ground										Pole-to-pole	

observed that distance to fault has a significant impact on the current characteristics. As expected, for close up faults the rise of current is faster and the current magnitude reaches higher levels due to lower overall fault loop impedance. Therefore, the converter and associated cables are more vulnerable. With increasing distance to fault, the values of R and L included in the fault loop naturally increase. The higher values of L increases the rise time (by limiting the rate of change of current), while the higher values of R reduces the current peak values. The reduction of rate of change can be observed on voltages and currents in Table III.

In case of pole-to-ground faults the fault resistance seems to have a predominant limiting effect on the fault current. However, higher fault resistance does not provide any increase of the rise time, as it does not include any additional inductance. Regarding the cable current and its rate of change, the MMC follows the decreasing pattern similar to the two-level converter. However the maximum values reached for cable current and di/dt are significantly lower due to the lack of DC-link capacitor and the arm inductance of the converter.

Note that the values of du/dt are significantly higher and they are not affected so much by the distance and fault resistance. This is due to the fact that after a certain threshold of fault current the sub-modules will turn-off to protect themselves from damage. During such fast transition the converter will behave as an uncontrolled rectifier which will result in high fall rate of DC voltage. However, in the case of two-level converter the fall rate of DC voltage is lower due to the

voltage support of DC-link capacitor. To better illustrate the impact of distance to fault and ground fault resistance, Table III includes maximum values of di/dt and du/dt for the two-level converter and HB-MMC.

B. HV-MTDC network

Pole-to-pole faults have been applied to the MTDC network in Fig. 3 in four different locations. The analysis in this section takes into account Terminal 1 (T_1) as the point of reference where local DC voltage and current measurements are taken. In this convention F_1 is considered a close-up internal fault (20 km from T_1), F_2 is considered a remote internal fault (250 km from T_1), F_3 is an external fault, and F_4 is a busbar fault (also external to the line). The challenging is the discrimination between remote internal fault F_2, and external fault F_3 and F_4.

C. Internal Fault

Fig. 4, shows the system response for F_1 triggered at $t_0 = 0.1$ s and as expected, during the fault high currents flow through all the lines, especially through the faulty DC Line 1. Observing the voltages, it can be seen that at $t = t_1$ the first wave reaches T_1 which corresponds to the time that takes the first wave to travel from the fault location F_1 to T_1 (20 km) and is equal to 0.068 ms. At $t = t_2$ another set of waves reach T_2 and T_3 which correspond approximately to 0.78 ms after the fault inception. It is difficult to distinguish the time difference in such voltages as the fault distance from T_2 is 230 km and from T_3 is 220 km. However, there are some very distinctive features in the voltages at T_1 and T_2. In particular, T_2 has only one inductor (L_{21}) separating it from the fault while between T_3 and F_1, three inductor exist in the fault path ($L_{32} + L_{23} + L_{21}$).
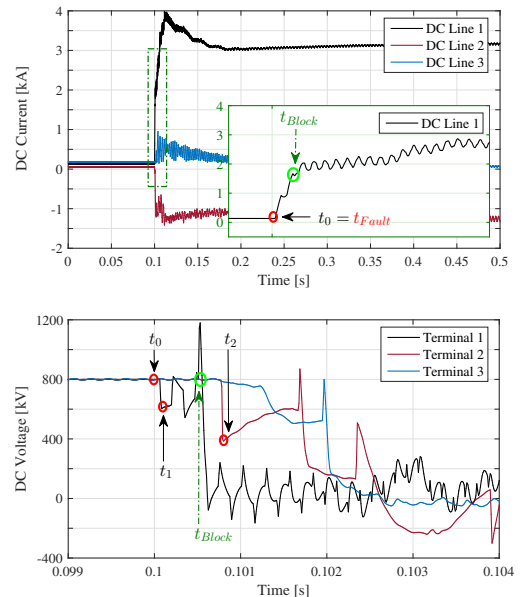

Fig. 4. System response for pole-to-pole internal fault (F_1) at DC Line 1. Cable currents and terminal voltages.

This results in reduction of the rate of rise of fault current (especially for the fault fed from MMC$_3$), and also the voltage

waveform at T_2 at $t = t_2$ shows clearly much sharper step change than the voltage waveform at T_3, where the change is much more gradual. What is also important to report in the context of protection is the blocking (or bypassing) action of the converters control system ($t = t_{Block}$), which has a clear impact on the currents and voltages. The blocking operation is really hard to predict as it depends on the location of the fault within the HVDC grid, the fault type, the operating condition of each converter (i.e. rectification or inversion) but also on the control mode selection (e.g. V_{dc} or P/Q)

D. External Fault

Fig. 5, shows the system response to an external pole-to-pole fault F_3 on the DC Line 3 triggered at $t_0 = 0.1$ s. Again, during the fault high currents flow through the lines but this time the faulty DC Line 3 is the most stressed. The voltage waveforms have a different response due to the different fault location within the HVDC grid and the formation of different fault paths and operating conditions. In particular, when observing voltages, its seen that at the fault inception $t = t_0$ the first wave is present at T_2. This is due to the fact that the distance is practically zero and there are no propagation delays involved. At $t = t_1$ (which is approximately 0.4 ms after the fault) the first wave reaches T_3 which corresponds to the time that takes the first wave to travel from the fault to T_3 (120 km). At $t = t_2$ another wave reaches T_1. Such wave is not so sharp as the other waves due to the total inductance included in the fault path as seen by T_1 which is equal to $L_{12} + L_{21} + L_{23}$.
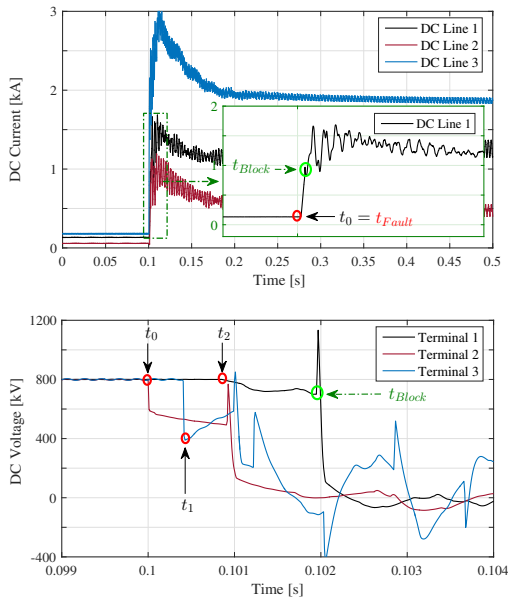

Fig. 5. System response for pole-to-pole external fault (F_3) at DC Line 2. Cable currents and terminal voltages.

E. Fault Discrimination

This section provides a way of discrimination between internal and external faults and is assumed that the local measurements are taken at T_1 and the protected line is DC

Line 1. The line currents, DC voltages at T_1 as well as the voltages on the line side of the inductor L_{12} are recorded. The key challenge here is to achieve discrimination for end-of-line forward faults. In the case of reverse faults (i.e. on DC line 2) it would result in the reversal of current direction in DC Line 1 which is easy to detect through suitably selected threshold. To establish if the forward fault is internal or external this paper suggests that voltage signals are used only. Fig. 6, illustrates the voltage signatures (on the terminal and line side of inductor L_{12}) for the four fault case studies. In all cases there is a significant difference between the two (top plots) captured voltage waveforms for internal faults which appear to have distinctive sharp edges which are more pronounced on the line side of inductor L_{12} (as the measuring point is closer to the fault and does not have any lumped reactor in-between).

As for external faults, there are no sharp edges on the voltage waveforms. This is expected since for any external fault the equivalent inductance included in the fault current path is always significantly larger than for the internal fault due to the installed lumped reactors. For example, in the case of busbar fault (F_4, Fig. 6-bottom right) the equivalent inductance includes the reactors $L_{12} + L_{21}$ while for any external fault on DC line 3 (F_3, Fig. 6-bottom left) the equivalent inductance includes $L_{12} + L_{21} + L_{23}$.

The key feature for the achievement of the end-of-line discrimination lies in the utilisation of the rate of change of the line side voltage which is illustrated in Fig. 7-top for all considered fault cases. By observing the close-up inspection area depicted in Fig. 7-bottom it can be seen that for the remote internal fault the rate of change of DC voltage reaches the values approximately $1.5 \cdot 10^6$ kV/s. However, for any external fault the values are below $0.5 \cdot 10^6$ kV/s during the first ms after the fault. This gives a relatively wide margin to achieve reliable discrimination. In order to ensure both dependability and security of protection a scheme with two-stage logic could be used. The first stage would include a criterion to indicate the occurrence of a fault within the DC grid. This could be based on instantaneous over-current, under-voltage or a combination of the two. The second stage would utilise the rate of change of DC voltage which would be compared with a pre-defined (carefully tuned) threshold in order to provide an indication whether the fault is internal or external.

V. CONCLUSIONS

In this paper, pole-to-pole/ground fault analysis of the two-level VSC-based and MMC DC systems have been performed. Both point-to-point and multi-terminal HVDC networks have been considered. Stage definitions of the fault response for each of the converter architectures are described which have assisted in characterising the DC faults. Based on the fault current waveform analysis and point-to-point studies, it can be observed that the two-level VSC generates larger DC fault currents than the MMC which is primarily due to the large DC-link capacitor. The utilisation of inductive terminations in DC lines limits the rate of rise of fault current and provides very useful voltage signatures which assist in reliable discrimination
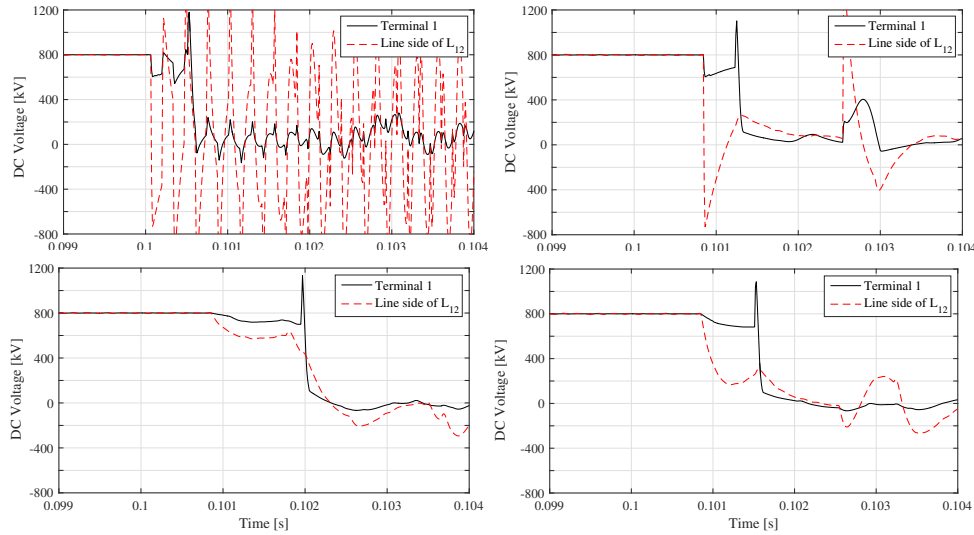
Fig. 6. Terminal 1 and inductor voltage for pole-to-pole internal, external and busbar faults. Close-up internal fault (F_1) at DC Line 1 (20 km from T_1), remote internal fault (F_2) at DC Line 1 (250 km from T_1), external fault (F_3) at DC Line 3 (0 km from T_2) and busbar fault (F_4) at T_2.
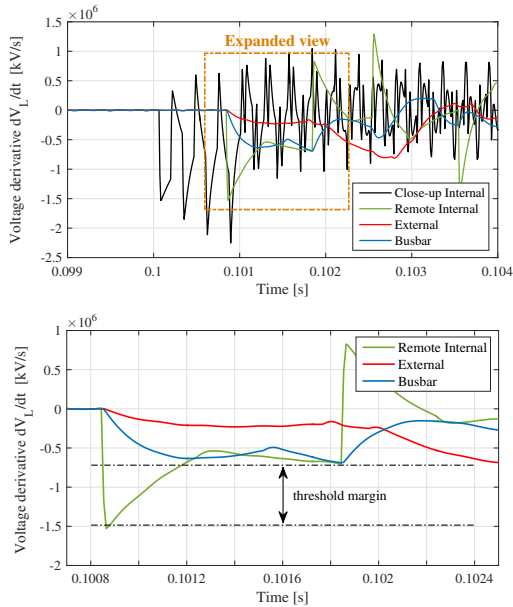

Fig. 7. Rate of change of line side inductor voltage for pole-to-pole faults. Close-up internal fault at DC Line 1 (20 km from T_1) and close-up inspection.

between internal and external faults. In particular, in the case of multi-terminal network such discrimination can be achieved by calculating and continuously monitoring the rate of change of DC voltage on the line side of the installed inductor.

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