RISK MITIGATION FOR THE USE OF NON-SPACE QUALIFIED COMMERCIAL OFF THE SHELF (COTS) AVIONICS IN SMALL SATELLITES

A THESIS SUBMITTED TO THE GRADUATE DIVISION OF THE UNIVERSITY OF HAWAI`I AT MĀNOA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

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By

Jeremy Kaiming Chan

Thesis Committee:

David Garmire, Chairperson

Olga Boric-Lubecke

Tep Dobry

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Dedication

I dedicate this thesis to all the past, present, and future spacecraft builders at the University of Hawai`i at Mānoa. For those of us who truly enjoy engineering, it is my hope that this research provides you with helpful knowledge, and the inspiration to advance our understanding of all the difficult problems you encounter.

May we and our creations reach the stars.

JC

Acknowledgements

First, I like to acknowledge the Hawai`i Space Flight Laboratory (HSFL), an excellent cooperation between the engineers from the UH College of Engineering (UH CoE), and scientists from the School of Ocean and Earth Science and Technology (SOEST). HSFL has generously provided me the opportunity to work there and gain experience on spacecraft and mission design for the past two and a half years. In addition, HSFL has graciously provided thermal/vacuum and vibration test data from its testing work for my analysis in this study. Specifically, thank you to Miguel Nunes, Lance Yoneshige, and Daniel Wukelic.

It has been a pleasure to spend my personal time and resources on this thesis to discover new risks and mitigations that can broaden the cognizance of risk mitigation in HSFL. With this research, I hope to give back to the organization that has helped me to sharpen my skills

I would like to especially thank Lloyd French, who has mentored me on spacecraft and mission design since 2007. I owe a great deal of the opportunities I have had to work on spacecraft missions to him. Through all the trials we've gone through in the past 4 years, Lloyd has never tired in his willingness to share his knowledge and advice.

To Byron Wolfe and Jason Akagi, thank you for all your mentorship during my CubeSat years. Your advice has stuck with me through these years, and has been invaluable.

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For my thesis committee, I'd like to acknowledge Dr. David Garmire, for his guidance on this thesis. And last but not least, thank you to the thesis committee members Dr. Olga Boric-Lubecke, and Dr. Tep Dobry, for serving on my committee, and for being excellent teachers for essential knowledge that I have applied to numerous circuit and embedded system designs.

Abstract

With the growing popularity of small satellites, low end 'small sat' missions are now being used for science, military, and educational efforts. Low end missions may typically be allocated less, or much less than a few million dollars. But in an industry where a single space qualified flight computer stack can easily cost upwards of a million dollars, entire low end budgets can be quickly spent on a single space qualified subsystem.

Mass produced 'commercial off the shelf' (COTS) components, designed and manufactured for only terrestrial applications, are now becoming the only solution to enable low end missions to fly. However, there are many risks that avionics experience during storage, transport into space, and orbit operations. There are also risks that COTS avionics would pose to the satellite's own payload.

Since terrestrial COTS is vital to small projects, there is a great need for a comprehensive guide for COTS risk identification and mitigation specific to small project needs. This study not only provides a comprehensive survey of disparate sources which facilitate risk management, but also selects specific information specific to COTS. I have also included new test data that I have gathered from my work at the Hawai`i Space Flight Laboratory, and my personal notes from my four years of experience working on small satellite projects. The recommendations that I have included are tailored specifically for small satellite projects. Risks specific to metallic whiskers, outgassing, and radiation are given special attention due to their potentially mission-ending risk factors.

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AO	Atomic Oxygen
CoE	College of Engineering, University of Hawai`i at Mānoa
COTS	Commercial Off The Shelf (terrestrial only unless otherwise noted)
DoD	Department of Defense
ETM+	Enhanced Thermatic Mapper Plus (NASA LandSat Series Instrument)
GCR	Galactic Cosmic Ray
GEO	Geostationary Orbit
GSFC	NASA Goddard Space Flight Center
Forbidden Metals	Pure forms of Zinc, Cadmium, and Tin
HIGP	UH Hawai`i Institute of Geophysics and Planetology (Part of SOEST)
HSFL	Hawai`i Space Flight Laboratory (Joint SOEST and CoE Organization)
HS1	HSFL Hawai`iSat-1 Mission
LDEF	NASA Long Duration Exposure Facility
LEO	Low Earth Orbit
LEONIDAS	Low Earth Orbit Nanosatellite-Integrated Defense Autonomous System
Nadir	From a particular location, the direction pointing directly below
NASA	National Aeronautics and Space Administration
ORS	Office of Responsive Space
PCB	Printed Circuit Board
PWB	Printed Wiring Board, a.k.a. PCB
SAA	South Atlantic Anomaly
SMAD	Space Mission Analysis and Design, 3rd Edition: Reference [01]
SOEST	UH School of Ocean and Earth Science and Technology
TPM	Technical Performance Metrics
UH	See UHM
UHM	University of Hawai`i at Mānoa

Chapter 1: Introduction

1.1 COTS Problems

As of 2011, the small satellite community has launched numerous successful missions using low cost 1-150kg class satellites. Many of these are tiny university satellites, often with budgets less than $100k. At a $100k level, about half or more of the money is reserved for catching a ride on the next suitable launch opportunity. On the lower end of the spectrum, these satellites even use commercial off the shelf (COTS) parts with no guarantee of reliability in space, and may even just be meant for hobbyist use at home.

If it can be done, just why isn't it done more often? First of all, the space and launch environments of a spacecraft introduce a plethora of risks that are not seen in everyday terrestrial applications. Space COTS components are designed for mitigating these risks, and can range from no guarantee of reliability at the low end, to high reliability with quantifiable environmental ratings and traceability data. Thus, with space COTS, risk assessment and mitigation can be reasonably done in cooperation with the manufacturer. The same cannot be said for terrestrial COTS products.

Accommodating terrestrial COTS is usually cost or performance driven. But, it comes at a steep price of reliability. Projects which can tolerate COTS must relax their requirements to make things work. Thus, for a mission requiring any minimum period of performance, relaxing requirements, and then not knowing the risks of COTS can be completely unacceptable. Terrestrial COTS satellite designs need a way to show an acceptable level of risk management.

Another issue for small projects is that COTS in avionics assemblies are not the only source of risk in a project. Risk reduction may also be needed for different levels of team expertise and fabrication capabilities. A COTS product could actually provide a higher quality product than a team which lacks the expertise and tooling to produce it. Thus, clearly there is also a need for COTS to supplement a void in expertise and facilities.

Closer to home at the university level, COTS based satellites are designed by students who may have never built an embedded device before. Where do student driven projects start with showing their level of risk to sponsors, and also to judges at launch opportunity competitions? There really exists no good guide for risk assessment and mitigation for this type of small low-budget project. The need for a guide is growing as more students enter the small satellite arena, with a desire to become better candidates for the aerospace industry.

Ultimately, the goal is to be able to take an off the shelf COTS component, and just put it through an straight forward process to determine its viability for spacecraft avionics. I have been thus far unable to find a helpful guide which is tailored specifically for a low cost spacecraft using COTS.

There do exist large amounts of risk mitigation documents from the National Aeronautics and Space Administration (NASA) and the European Space Agency (ESA), many of which I have referenced in this paper, but they are not specific enough to aid inexperienced project teams. There is far more material for designing space electronics from raw silicon than there are about figuring out how to utilize existing COTS assemblies. Albeit for good reason, this leaves us with minimal COTS oriented material to work with. This commonly results in small projects moving along without the right data and considerations for engineering. To facilitate proper engineering, I fervently believe that we need a guide on utilizing COTS with good engineering and risk management practices, even on a shoe-string budget.

This study is focused mainly on using low cost terrestrial COTS products which were designed with no intent of being used in space. And as such, the term *COTS will from here on be used to refer only to COTS components intended for terrestrial use*.

1.2 Addressing the Problem

After going through four years of not knowing what I didn't know, and being advised at many design reviews, I now write this thesis to provide my successors some guidance from my last four years. The last four years, of which I have spent researching, designing, and building spacecraft avionics for the University of Hawai`i at Mānoa. The most important feature of this paper is to promote the basic understanding of risks to spacecraft avionics. An

unknown risk can never be intentionally mitigated, and could be exacerbated. Thus, through the awareness and understanding of risks, you'll be able to take action to manage your risks.

Information from disparate sources each have a part to play in risk identification and mitigation. But rarely does one single source tell the whole story about a risk. Thus, the approach that I have used is to aggregate existing information sources, and highlight the most important aspects for converting COTS products into space avionics. Each highlighted issue incorporates explanations from my experience. I have also included lists of materials which I have collected over the years to aid in product selection to avoid risks in the first place.

As the focus here is on risk identification, it is important to note that significant future work is ahead in the area of risk mitigation. Some issues can be so complex that very specific cases of mitigation research must be performed. It is the intent of this study to provide you with a starting point for these mitigation research topics. Through additional research, a library can be built and referenced for future design decisions. Such a library would greatly accelerate all projects which have a need for COTS.

This study can be used to directly benefit of all future University of Hawai`i (UH) space flight projects which will use COTS products. At the time of writing, the two current UH laboratories which build spacecraft are the joint School of Ocean and Earth Science and Technology (SOEST) and College of Engineering (CoE) organization called the Hawai`i Space Flight Laboratory (HSFL), and the College of Engineering's (CoE) Small Satellite Lab. I propose that this study be used by both laboratories as a baseline set of COTS risk identification knowledge for all personnel intending on producing flight products.

1.3 Research Questions

The main goal is to discover what kind of risks apply to satellite avionics, and what needs to be researched for operating COTS components in space. Specifically, this thesis will address the following research questions:

- What are the various environments space avionics go through?
- What are the risks do avionics face in each different environment?
- What can be done to mitigate the risks?

1.4 Benefits of Study

This study will provide the following benefits:

- Provide insight into risk mitigation for the use of COTS devices
- Discover cost effective methods for risk mitigation on COTS devices
- Designate areas of further research for converting COTS devices to space avionics

1.5 Scope

This study applies to terrestrial COTS components and assemblies that could be used for spacecraft avionics. Terrestrial COTS includes commercial, industrial, and non-aerospace military components. This study will provide guidance to all satellite designs which could potentially tolerate the use of COTS.

1.6 Methodology

The following will be performed in this study:

- Conduct literature review and interviews to determine current practices for COTS
- Conduct literature review of spacecraft environments to identify and discuss the major issues that need to be considered
- Incorporate my own experiences from work performed on spacecraft avionics
- Suggest future work that should be done to help to quantify risks

1.7 Thesis Overview

Chapter 2 describes the overview of various risks that have been identified

Chapters 3-6 describe the various environments that a spacecraft will go through.

Chapter 7 discusses radiation exposure specific to avionics operation in space.

Chapters 8 and 9 describe risks that involve all stages of the satellite life cycle.

Chapter 10 summarizes the risks identified, and draws conclusions on actions to be taken.

Appendix A is attached as a guide to performance metrics of remote sensing satellite, and how the identified risks apply to them.

Chapter 2: Overview of Risks for Satellite Avionics

To provide you with an overview of satellite risks at a glance, I have compiled the below table which shows risks that satellite components will experience. Some risks are normal terrestrial risks which may already be accounted for in a COTS device, and other risks are specific to the launch and space environments.

Table 2-1: Overview of Identified Risks for Avionics

Period	Risk Category (w/ Overall Risk Color)	Risk Impact	Probability of Impact
S&H	Handling Risks	Moderate	Moderate
Storage	Handling Risks	Moderate	Moderate
	Self and Cross Assembly Contamination with Outgassing	High	High
	Corrosion	Moderate	High
	Component Expiration and Material Degradation	High	Moderate
	Metallic Whiskers	High	High
Launch	Explosive Atmosphere (Hot Launch Only)	High	No Risk for Cold Launch, High for Hot Launch
	Electromagnetic Interference (Hot Launch Only)	High	Moderate for Cold Launch, High for Hot Launch
	LV Integration Handling	High	Moderate
	Shock and Vibration	High	High
	Acceleration	High	Moderate
	Aerodynamic Heating	Moderate	Very Low
	Venting of Atmosphere	High	Moderate
Space	Vacuum and Temperature De-Rating	Moderate	Moderate
	Thermal Cycling	High	High
	Micrometeroids	Moderate	High
	Spacecraft Charging and the Plasma Environment	Low	Moderate
	Atomic Oxygen	Low	High
	Space Radiation Exposure	High	High

Based on the findings in this research, I have assigned risk levels to each risk category. The risk level for the category is specified based on Dr. Trevor Sorensen's technique [86] of assigning risk levels based on risk impact versus probability of impact. The baseline risk level begins with the magnitude of risk impact, and downgraded only if the probability is

low. From lowest to highest risk, I have colored each risk category with green, yellow, and red. This helps to identify the risks that should be looked at first. The assigned probabilities and impacts were based on my experience, design reviews, and research. The next table covers mitigation methods that I'd like to highlight for each risk, as well as their relative costs.

Table 2-2: Summarized Risk Mitigation Methods Specific to COTS Avionics

Period	Risk Category (w/ Overall Risk Color)	Mitigation Cost	Mitigation Method
S&H	Handling Risks	Low	Safe Handling Procedures & Inventory Tracking
Storage	Handling Risks	Low	Safe Handling Procedures & Inventory Tracking
	Self and Cross Assembly Contamination with Outgassing	Low-Moderate	Assembly Modifications, Careful Material Selection
	Corrosion	Moderate	Assembly Modifications, Careful Material Selection, Metal Surface Conversions and Platings
	Component Expiration and Material Degradation	Moderate-High	Strategic Procurement Scheduling or Periodic Inventory Performance Testing
	Metallic Whiskers	Moderate-High	Conformal Coating, Board Rework, Prohibition of Forbidden Metals
Launch	Explosive Atmosphere (Hot Launch Only)	Moderate	Explosive Atmosphere Testing Per Range Safety Guide, or Launch Cold
	Electromagnetic Interference (Hot Launch Only)	Moderate	EMC Testing, Shielding, and Limiting 'on' Devices, or Launch Cold
	LV Integration Handling	Moderate	Safe Spacecraft Handling Procedures & Handling Points
	Shock and Vibration	Moderate	Natural Frequency Dampening on Avionics Boards
	Acceleration	Moderate	Quasi-Static Load Support for Avionics Boards
	Aerodynamic Heating	Moderate	Thermal Isolation of Avionics Components from Vehicle
	Venting of Atmosphere	Very Low	Small Holes in Avionics Boxes
Space	Vacuum and Temperature De-Rating	Low	TVAC Confirmation of Temperature Ranges
	Thermal Cycling	Moderate	Insulation or Design for Thermal Expansions
	Micrometeroids	Moderate	Bumper Layers for Impact Fragmentation and Stopping
	Spacecraft Charging and the Plasma Environment	Moderate	Grounding, Low Voltage Bus, Insulation
	Atomic Oxygen	Low-Moderate	Materials Selection on Directly Exposed Exterior Surfaces
	Space Radiation Exposure	High	Radiation Screening of Lot Parts, Software Radiation Tolerance, Circuit Radiation Tolerance, Supervisory Circuits

Using these risk summary tables, you can make a decision on which risk to consider first. All these identified risks can become high impact risks based on varying situations. Once each risk has been assessed for a particular component, a weighted scoring system can be used to prioritize risk mitigation efforts. In addition, the risks can be used to support trade studies, where multiple similar components are compared against each other. If some component shows less risk, that could positively influence the effectiveness of the study.

The next chapters cover the various spacecraft environments, and the details of risks to avionics as summarized in **Table 2-1**. Mitigations and proposed processes are also included for areas in which I have had experience, or where effective methods of mitigation were found from other sources.

Chapter 3: Shipping and Handling

From the very beginning, and throughout the lifecycle of avionics, components and assemblies will need to be handled and shipped multiple times. MIL-STD-810G figure 1-4a (shown in **Figure 3.1**) describes the lifecycle of military products, points of handling, and hazards during all stages of procurement and supply.

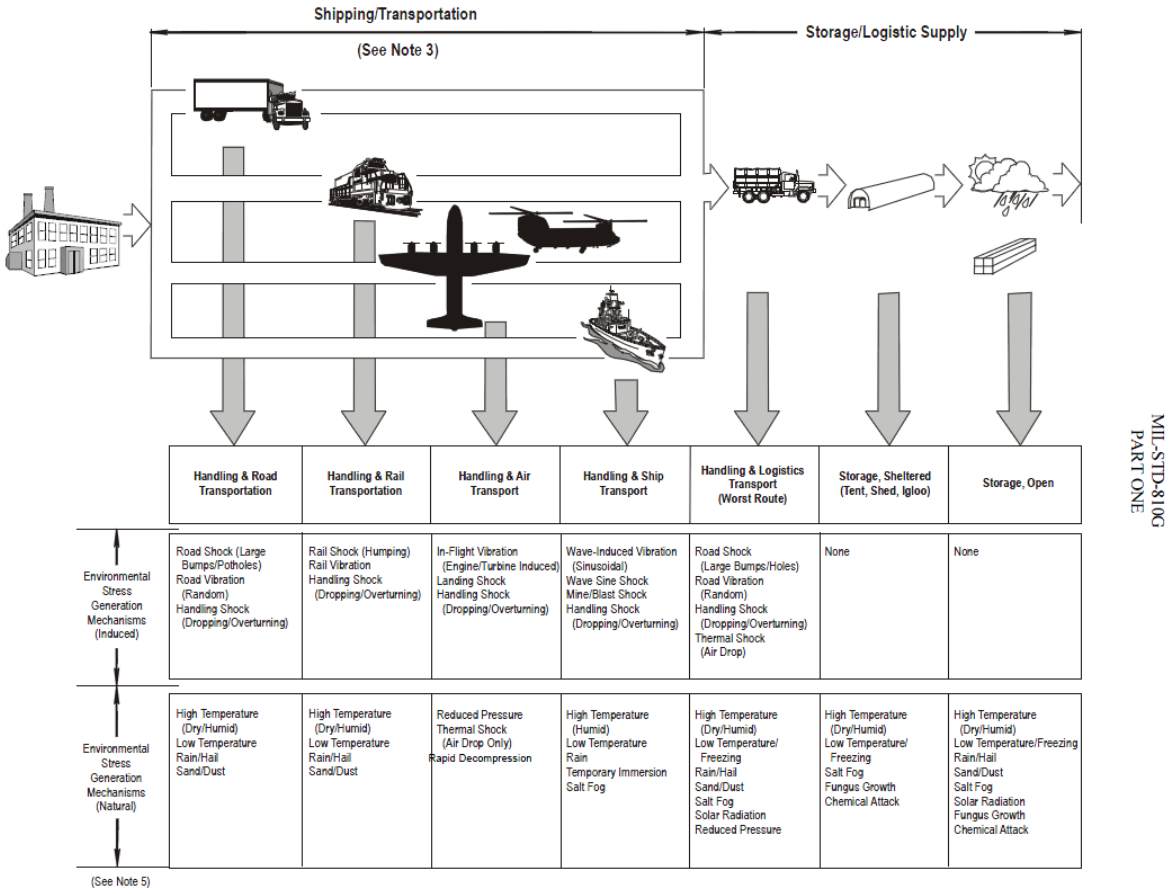


FIGURE 1-4a. Generalized life cycle histories for military hardware.

Figure 3.1: From MIL-STD-810G: Generalized Life Cycle Histories for Military Hardware

The individual parts that make up COTS assemblies, as well as the assemblies themselves have already gone through multiple cycles of shipping/transportation and storage. The figure shows all the hazards from induced and natural sources. Unfortunately, the COTS supply chain and manufacturing process is normally available for public examination. Thus, you are likely to be unaware of whether a part has previously been dropped, or whether a part has been environmentally stressed beyond survivable limits. This lack of visibility into

manufacturing and logistics is the tradeoff you make for acquiring COTS products. Thus, the first risks for COTS include pre/post delivery environmental over-stress.

Before and immediately after delivery, the ideal situation is to ensure that all parts are working, and are being stored/used within their durability and environmental specifications. Thorough burn-in testing of each part received can reveal workmanship defects, dead-on-arrival parts, and component infant mortality.

Since avionics will be launched in a rocket and sent into space, COTS environmental specifications will be violated (if there were any specifications to begin with). Thus, testing a part in each target environment can build data for survivability, and mitigate risks of unknown performance. Where environmental specifications will be intentionally violated, such as taking a terrestrial part into space, testing in a simulated or actual environment is necessary to understand out-of-spec performance.

As each COTS product is received, engineering and flight model hardware should be treated in a way that is traceable. This will allow the best chance for catching problems caused by handling before final integration for flight. Problems from handling can come from common sources such as dropping a component, foreign material contamination, and electro-static discharge (ESD). Since physical damage can occur during handling, it is important to keep a record what an assembly has gone through.

David Squires from Nanospace Systems [31], a systems engineer who has worked on NASA flight projects, has recommended that handling should be tracked on a log sheet referred to as a 'parts traveler'. The parts traveler enables convenient logging of any important events like normal wear and tear, damage, and testing. Any damage to a part can be quickly noted, and flagged for being addressed before the part makes it onto a launch. One parts traveler is needed for each serialized assembly intended for engineering qualification and flight, and travels with the part as it is moved around.

One case where a parts traveler is especially helpful is tracking the number of mating cycles used for connectors. Each connection and disconnection is referred to as a mating cycle. Electrical connectors specify a certain contact resistance over a limited number of mating cycles. For an example, a commercial grade gold plated terminal (e.g., Molex KK series [32]) may be rated for 50-100 mating cycles. Beyond the rated number of mating cycles, the

gold plating may be scraped off to a point where it is no longer protecting the base material nor maintaining baseline conductivity. If no parts traveler exists, there may be no way to determine if the number of mating cycles have been exceeded before flight. The potential problems can range from increased contact resistance, increased vulnerability to corrosion, decreased mechanical performance, and ultimately lead to under/non-performing circuits.

Since a lot of time can be invested in testing and converting a COTS product into a space-worthy product, the parts traveler is invaluable for maintaining confidence in the avionics inventory. Once avionics products have gone through sufficient testing, integration into the satellite, and final integrated testing, the satellite is ready for launch. However, launches almost never line up with satellite completions, so the next stage can be long term storage.

Chapter 4: Storage Environment

Flight avionics for satellites are usually built, cleaned, and then stored in a clean room. However, fabrication methods for avionics almost always include dirty processes such as soldering, cutting, and application of chemicals. Avionics which are not cleaned properly can contaminate other assemblies in clean storage.

Long term storage can have serious risks to avionics. During this study, the most notable risks discovered include outgassing, corrosion, contamination, perishable components and metallic whisker formation. Any one of these risks can potentially render avionics unusable, or go undetected and cause premature mission failure.

4.1 Contamination and Outgassing

Contaminants are any foreign material that has deposited into an assembly. In avionics assembly areas, this can include dust and chemicals. The devices most affected by contamination are typically optical devices. Electronics, wire harnesses, and structural components can also be damaged by contamination. Cross contamination between assemblies can also cause damage. The primary mitigation for this is thoroughly clean, inspect, and store all avionics in controlled environments.

However, even in a very clean and sealed environment, materials within an assembly can damage its own components. This is usually caused by a phenomena known as outgassing. One example of outgassing is observing a film build-up on windows in a car. The film can be made up of many outgassed particles from console molding, dashboard protectors, and other materials in the car's interior. When the film is lit by street lights or the sun, the film can cause the window to become slightly, or complete opaque. This kind of contamination is highly undesired for spacecraft optics. Since outgassing affects all stages of the spacecraft's lifecycle, outgassing will be discussed in its own chapter.

4.2 Corrosion

There are many different types of corrosion that can affect a satellite. However one thing that they all have in common is time. During storage, the satellite may be sitting on the shelf for months or even years at a time. Long term storage comes exposes the many different factors which can result in satellite corrosion. Assuming a completely clean satellite, the most

serious sources of corrosion discovered in this study come from chemical attack from outgassing materials, as well as galvanic corrosion which occurs in the presence of moisture as the electrolyte.

Galvanic corrosion is an especially important risk to consider for high current circuits, transmission lines, RF, and EMI shielding applications. To begin to understand this corrosion, each metal has a different voltage potential versus a standard electrode. The higher the potential between two metals, the more likely galvanic corrosion will be significant.

In order for galvanic corrosion to occur, two conditions must be satisfied. First, two dissimilar metals must be joined electrically. Second, the two dissimilar metals must touch the same electrolyte. This results in the creation of a galvanic cell. The electrolyte facilitates a redox reaction where the anode in the galvanic cell will oxidize, and the cathode will be plated with the anode material.

Surface area of electrolyte 'wetting' is also a factor. According to Atlas Steels, if the electrolyte contacts a large surface area of the cathode, and a small surface of the anode, galvanic corrosion can occur rapidly due to high current densities. On the other hand, if the electrolyte contacts a large surface area of the anode and a small surface area of the cathode, there will be a comparatively lower rate of galvanic corrosion [76]. In storage, the effective surface area of moisture in the air will vary.

Eliminating any potential electrolyte will prevent galvanic corrosion all together. Moisture minimization can be accomplished by using a humidity controlled storage locker, or a moisture barrier anti-static bag with sufficient desiccant. Dry nitrogen storage can also accomplish the same moisture elimination.

However, during testing, assemblies may be exposed to moisture for months at a time. Thus, galvanic corrosion must be addressed early in the satellite design. Minimizing the potential difference (e.g., to tens of milivolts) between anode and cathode will slow or eliminate galvanic corrosion. Satellites can easily form strong galvanic cells if the designers have not considered galvanic corrosion. Aerospace grade aluminums are typical light-weight structural materials for satellites. Aluminum is a very anodic metal (corrosion prone), and the corrosion effect is quite pronounced when the metal is brought into contact with common

avionics structural and RF interconnection materials. This includes brass, copper, nickel, and especially gold (a very strong cathode).

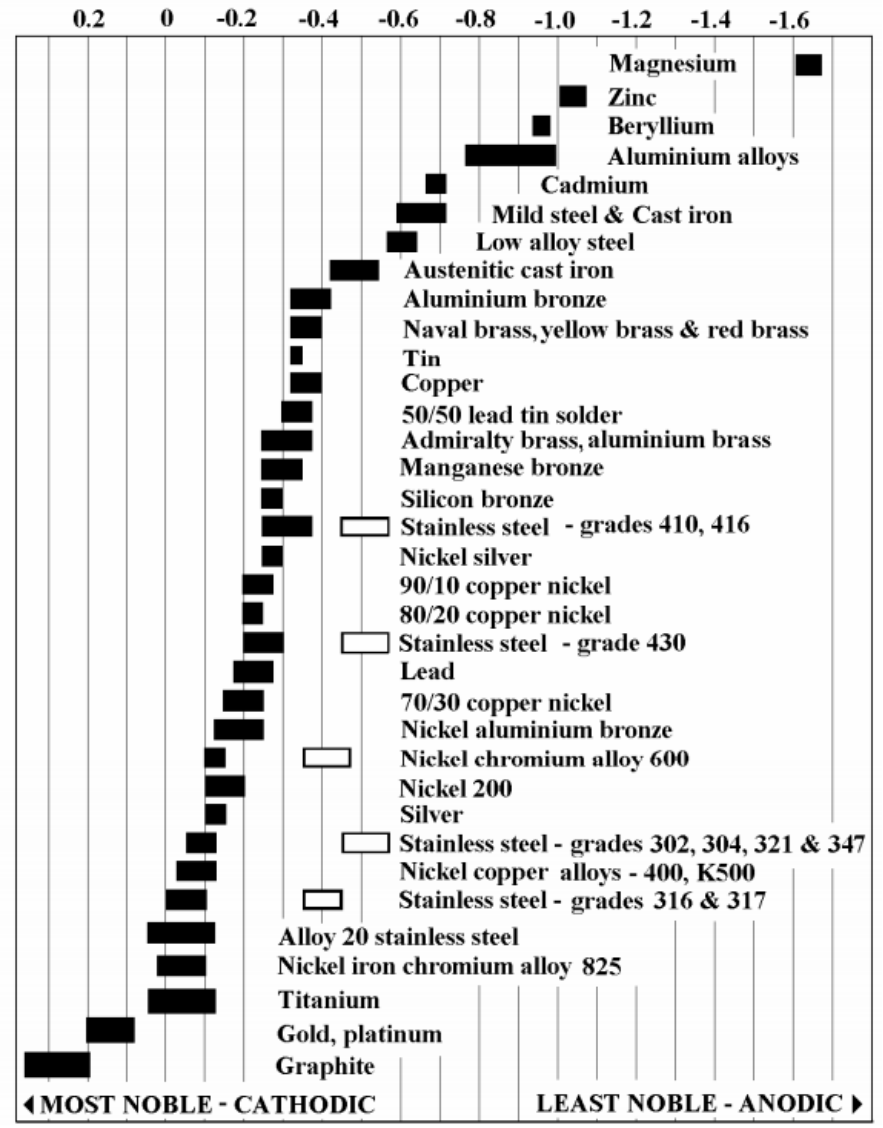


Figure 4.1: Potentials [Volts] vs Standard Calomel Electrode, Source: Atlas Steels [76]

For applications such as RF/EMI grounding, low impedance grounding is required at all grounding interfaces, and thus significant corrosion of interfaces becomes unacceptable. MIL-STD-889 describes methods for minimizing galvanic corrosion when joining dissimilar metals.

To address the anodic nature of aluminum, surface conversion and metal plating can help. Surface conversion provides the added benefit of aluminum oxide elimination. In addition, conversion to a non-oxidizing material has the added benefit of providing higher electrical

conductivity. If direct surface conversions do not provide a cathodic enough potential, additional metal plating can be performed (e.g., aluminum with electro-less nickel plated with gold). If spot plating is used, galvanic corrosion will only be able to occur along the edge boundaries of the plating. Thus, spot plating can be done strategically to provide sacrificial boundary areas. Note that scratches, which penetrate through plating, become additional sites of galvanic corrosion.

Per NASA-HDBK-4003, a class 3 conductive surface conversion per MIL-C-5541E can be used to minimize contact impedance. The procedure for surface conversion removes the natural resistive aluminum oxide surface, and replaces it with a conductive material such as chromium. Chromium has a much smaller galvanic series potential with RF interconnect materials such as brass or copper [34]. Ideally however, the surface conversion would convert the surface to, or allow plating of a material which is within NASA-HDBK-4003 galvanic series tolerances.

Regarding chemical attack from outgassing, another important corrosion issue arises from storing avionics in sealed anti-static bags. These bags may be moisture barrier bags with desiccant, and sealed to be gas tight. The gas tight environment may lead to outgassing chemicals building up within the bag. Certain gasses can be very corrosive to many common avionics materials, so consideration should be given to what kind of materials are part of the assembly. A balance between protecting avionics against electrostatic discharge, galvanic corrosion, and eliminating outgassing chemical corrosion must be achieved.

Outgassing is influenced by pressure and temperature. Minimizing temperature, and increasing pressure can reduce the amount of outgassing which occurs. Deposition of outgassing chemicals on surfaces can be reduced by using a continuous low-flow dry nitrogen flush.

One example of outgassing corrosion comes from a common material aerospace material called Tefzel. The material is considered low outgassing, and is commonly used for spacecraft wire insulation. The wire has been stored both by itself, and in spacecraft connector assemblies. Over time, the Tefzel material releases fluorine. If the fluorine mixes with moisture, it can form a gaseous hydrofluoric acid. Copper, among other metals, is extremely susceptible to hydrofluoric acid attack. In wire itself, this is known to the industry

as the red plague. Even gold plated conductor pins/sockets, which use copper as its core material, can also be corroded through micro-scratches in the plating. This issue was documented in NASA Advisory NA-GSFC-2003-03 [30]. Copper RF micro-strips and antennas are especially vulnerable to this kind of corrosion if there is direct gas exposure.

Other contaminants, such as the oils and salts from human fingerprints, can also chemically corrode avionics. Thus it is very important that any flight hardware that is stored for long term, is cleaned thoroughly before it enters storage. And equally as important, the storage facility must be designed to prevent corrosion.

4.3 Perishable Components and Materials

Compared to other avionics components, parts such as batteries and solar cells have a relatively short shelf live. Highly influenced by environment conditions and their electrical states, parts can come out of storage and not meet their original specifications. Others may be on the brink of not meeting their original specifications, and will fail during the period of performance.

There are a number of reasons why a project would order these types of degrading parts well before the mission. This includes lot screening of parts, bulk discounts, additional startup costs for fabrication runs, availability of funding, and availability of personnel. Ideally, a project would order or refresh the satellite's perishable hardware just before launch. However, this type of late procurement may not always be possible.

In the worst case, mitigations to perishable parts include: to design margin into the system to account for degradation; work with the manufacturer to optimize the storage method for shelf life; and perform proactive testing on sacrificial parts which are stored beyond their documented lifetimes.

Beyond part expiration, manufacturers are unlikely to provide any guarantee of performance. If years of time are between procurement and launch, it would be preferable to have enough sacrificial parts and equipment to allow for regular (potentially destructive) characterization of perishable parts. The resultant data will ultimately be helpful for trending and updating the mission's chance for success, allowing for proactive decisions.

Other materials vital to avionics such as passives, EMI gaskets, insulators, adhesives, and coatings can also degrade over time. Degradation can be minimized by strict compliance with storage environment requirements. When specifying materials for assemblies, the lifetime and storage compatibility should be considered.

COTS assemblies should also be inspected, characterized, and evaluated for their materials to determine any material degradation risks.

Chapter 5: Launch Environment

The most common power source for moving satellites into space is rocket propulsion. Both manned (e.g., NASA STS, Russian Soyuz) and unmanned delivery systems have been used for placing satellites into their orbits. As the satellite taken out of storage to be integrated onto launch vehicle, the satellite is again vulnerable to handling risks. And when launched, a whole new set of issues arise.

Terrestrial COTS products are usually not built for launch environments. The figure to the right shows the MIL-STD-810G missile launch induced environment. Of the induced environment issues, we're concerned with all of the listed issues. We will examine each one of these issues and examine the risk to avionics.

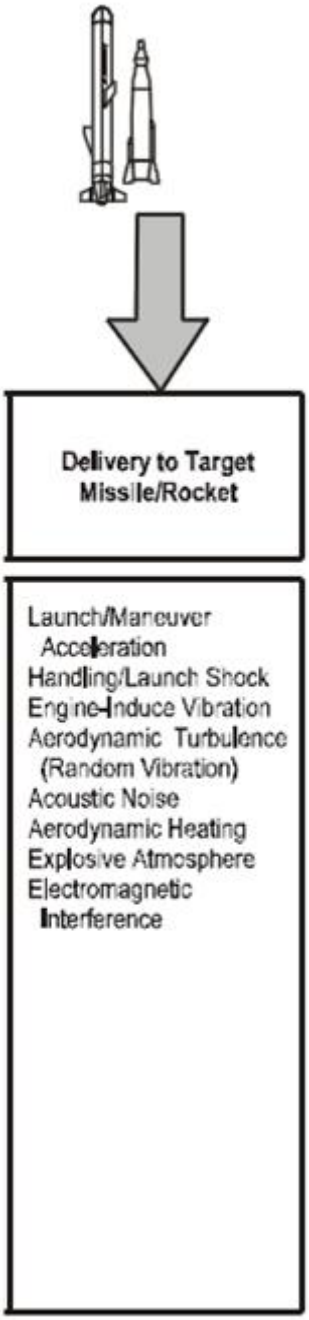


Figure 5.1: Missile Launch Induced Environment from MIL-STD-810G

5.1 Explosive Atmosphere

There are many different propulsion systems made for rockets. Rockets will use solid propellant motors, liquid hypergolic fuel, and other liquid/gas systems. Certain propellant systems have a risk of leaking fuels in gaseous form. The gas can become explosive either by itself, or when mixed with air. Any type of electrical arc initiation occurring within the gas can ignite it.

To eliminate risks to personnel, property, and the primary mission, any secondary payloads such as CubeSats are forbidden from energizing any systems during/after launch vehicle integration. For CubeSats, the next opportunity for powering up is when the satellite is deployed into space, so there should theoretically be no explosive atmosphere risk.

In the case of the primary payload, different missile range safety requirements may or may not allow it to be energized after integration into the launch vehicle. Launching cold (with no batteries connected) is the least risk scenario for an explosive atmosphere. If the primary payload is allowed to be launched hot, or operational, the electronics may need to be tested for an explosive environment. COTS avionics candidates are almost never specifically built for use in an explosive environment. Thus, before the satellite is allowed to launch hot, certification of the part may be required to demonstrate safety in an explosive environment.

5.2 Electromagnetic Interference

During ascent, the launch vehicle will likely be sending telemetry down to launch control, as well as listening to commands. The launch vehicle should also be carrying flight termination radios to allow aborting the missile in mid-flight. Complete control over the missile is extremely important to ensure safety within the missile's hazard area.

Telemetry transmissions and unintentional EMI from the launch vehicle can affect satellites which are launching hot. But even worse, intentional and unintentional EMI emanating from hot satellites may jam the rocket's communications and flight termination system.

To prevent EMI issues, launching with all satellites de-energized is the simplest solution. However, as the above explosive environment indicated, customers may need the satellite to be on at all times. In this case, electromagnetic compatibility (EMC) testing, such as tests specified in MIL-STD-461, can be required to first ensure that the launch vehicle will not be compromised. Secondly, testing can be used to ensure that the satellite will function within the launch vehicle's RF environment. COTS components will typically only be qualified to FCC and/or CISPR EMC standards, if at all. Regardless, as a system, the satellite must be tested as a whole to meet any launch vehicle EMC requirement.

Certain launch vehicles may also have provisions for the primary payload to piggyback on the rocket's telemetry stream. This would be preferred, as it will eliminate the need for another potentially powerful source of EMI.

5.3 Satellite-Launch Vehicle Integration

During integration into the launch vehicle's deployment mechanisms, a satellite must be physically handled. The normal ground handling risks apply (as discussed in chapter 2). The difference however, is that now you have a much heavier and complex structure than any one individual COTS component. Thus, damage in a drop would be catastrophic.

As discussed earlier the satellite is usually stored in a clean room environment with possible humidity and temperature controls. Integration of the satellite onto launch vehicle requires that the satellite is taken out of that original controlled environment for at least a brief time. Depending on the launch site, the environment may also be extremely dirty. The risk of contamination is much higher after integration. Potential sources for contamination include other satellites, personnel, work areas, and the launch vehicle itself.

During launch, materials within the payload fairing can shake off and contaminate the satellite. And for deployment preparation, the payload fairing is jettisoned to allow satellite deployment. This can involve explosives which sever bolts that hold the fairing onto the launch vehicle. For satellites, it is preferred the launch vehicles are 'clean'. That is, they should use non-contaminating explosive bolts, low outgassing materials, and keep fuel away from the payload. However, this may not always be the case.

Minimizing the amount of contamination from each of these post-integration sources is especially important to an optical remote-sensing mission. However, it may not always be possible to dictate the cleanliness or selection of a launch vehicle. It is thus upon the satellite designer to find out about the launch vehicle, and take necessary steps to control contamination.

5.4 Launch Shock and Vibration

Launches into LEO can be on the order of ten minutes, but the most severe environmental issues in the mechanical domain arise during that time. From the launch vehicle's initial ignition, the spacecraft will experience multiple sources of shock, vibro-acoustics, and vibration.

Vibration and vibro-acoustics can do a variety of damage to avionics. Under these sources of dynamic loading, screws can back out, solder joints can repeatedly flex and crack, and connector contacts can bounce. On top of vibration, launch vehicles capable of orbital insertion will typically have several stages, and separating the stages and fairing may involve explosive bolts. Thus, multiple shock events should be expected. Explosive bolts and engine ignitions will cause pyrotechnic shock. The shock levels near an explosive bolt can peak at several thousand g over a period of a few miliseconds. Not many electronics, and especially not COTS electronics, will come with a rating anywhere near that level. Even military standard connectors will have a shock ratings of equal or under 300g [77]. Fortunately, once a launch vehicle is proven to work, it is likely to be used over and over again. If a launch vehicle has such flight heritage, the launch provider should be able to provide a user's guide which will include a maximum predicted environment of all environmental issues.

Simulations can help to reveal the natural frequency of spacecraft assemblies. But ultimately, testing is needed to determine if components will survive launch. Testing can be performed on the assembly level, but it is more important to perform testing on the spacecraft level for a more accurate result. Both dampening and resonances from the spacecraft's structure can significantly alter the vibration response at components.

Satellites take a long time to build, so early mitigation of risk can be achieved by testing an avionics assembly for shock and random/sine-sweep vibration. MIL-STD-1540 covers the testing procedure that is done for military spacecraft. The testing verifies workmanship, and provides risk reduction to the mission. The testing may also be required to minimize risk to the launch vehicle and other payloads. **Figure 5.2** shows the HSFL vibration table that can be used for both vibration and low G shock testing.

Figure 5.2: HSFL Vibration Table

The **Figure 5.3** shows a test setup for random vibration. The vibration spectral density used for this particular test was the NASA GSFC-STD-7000 proto-qualification spectral density, increased to $11g_{rms}$ to account for estimated vibro-acoustic loading for a new HSFL launch vehicle. The vibration table is only able to vibrate in one axis at a time, so testing was performed one axis at a time for two transverse axes along the plate's top surface plane.

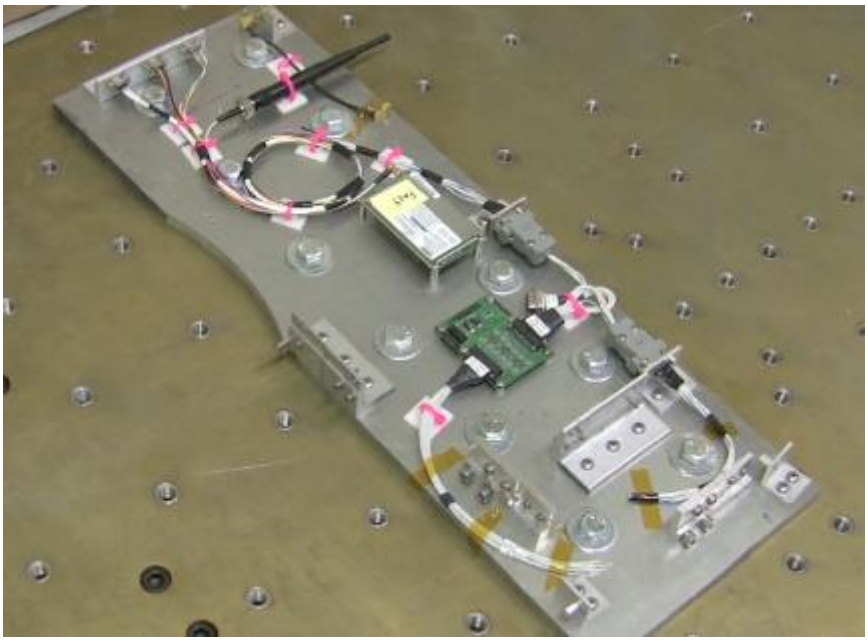


Figure 5.3: Vibration Test Plate for Screws, Connectors, and Avionics Candidates

In this particular test session, approximately thirty four (34) individual tests were performed on the one test plate. Most of the tests involved stainless steel metric and standard fasteners. Fastener torques were applied to generally accepted industry specifications, and connector systems were torqued to manufacturer or military specifications. This test verified that even with or without secondary retention of fasteners, as long as the standard torque specification was met for each screw, the screws would not back out from aluminum. In addition, Kapton tape was used to hold down various lengths of wire/cable. The tape was able to hold the wire and cable secure throughout testing. Ultimately, the fastener, connector system, and Kapton tape experiments were very helpful in understanding risks from vibration, and helped to verify the durability of the tested avionics.

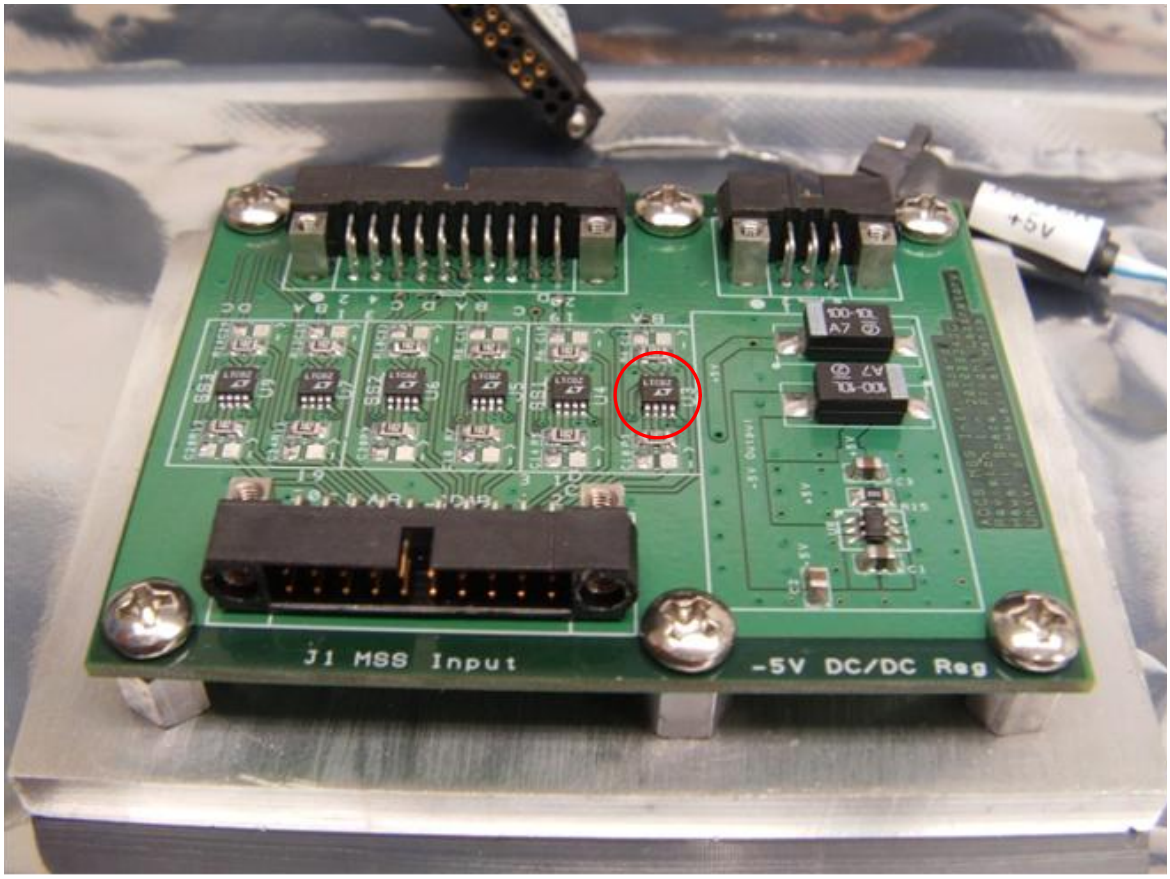


Figure 5.4: HSFL Photodiode Amplifier Array

As for avionics, the avionics candidate pictured in **Figure 5.4** was not so fortunate. After vibration testing, one of the solder had joints failed. This resulted in a faulty amplifier output.

Had this failure occurred on orbit, the satellite would have an impaired attitude determination capability.

The failure occurred at one of the MSOP-8 package leads circled in red (**Figure 5.4**). The solder joint cracked, and resulted in an open circuit. Upon re-soldering the affected pin, the amplifier was restored to normal operation. This indicates an issue with workmanship in the soldering process. Improvements to the fabrication process can turn this design into a flight worthy product.

Large and heavy components should be given additional support to prevent vibration loads from over-stressing solder joints. Note from **Figure 5.4**, the black board-mounted connectors are Harwin M80 series connectors with board-mount screws. The connectors are inserted to the board, and the screws are torqued to manufacturer specifications before soldering. This helps to relieve stresses from the solder joints from heavy attached connectors under vibration and acceleration loading. The chassis mounting screw holes were also placed next to the connectors for strain relief. The SSE book notes that other components such as large capacitors and crystals should be either strapped down, or supported by vacuum rated RTV [03].

Normally, a part would be designed specifically to provide support against vibration damage. But with COTS, you what you see is what you get. If a COTS assembly has a natural frequency that is too low, either discovered by analysis or testing, it might be possible to stiffen it. Lloyd French suggests that single board COTS assemblies can be glued onto an stiff aluminum box with to help support and dampen vibration [78].

Dave Steinberg's book also recommends metal ribs to be glued onto circuit boards to increase their natural frequency. The support rib approach appears to be most helpful for stiffening stackable or chassis based architectures (e.g., PC/104, VME, CPCI, etc.). A glue with a high modulus of elasticity is preferred to ensure that the circuit board cannot flex very much more than the metal rib [34]. However, a very hard glue can crack assemblies under thermal expansion, so CTE's should be closely matched between the circuit substrate and glue, or if not possible, low modulus material should be used. This is even more critical for assemblies which have a double sided load (e.g., components are on both sides of the board). Since the rib essentially reduces drum-heading, the rib goes right through the center of the board.

You're almost guaranteed to have to glue a rib over components for a board with a double sided load. Unfortunately, that means that once the rib is glued on, the board is no longer completely repairable.

To prevent electrical shorts on metal ribs, the book suggests that the adhesive should be cured over the metal rib first (for insulation), before attachment to the circuit board. Holes can also be drilled into the metal rib to allow the glue to form rivets that will not detach under thermal cycling. The book is an excellent reference for implementing structural ribs on existing circuit boards [34].

5.5 Acceleration

Launch vehicles for satellites can accelerate up to 8g or higher. Terrestrial COTS components are not specifically built to withstand this kind of acceleration. The acceleration force can cause circuit boards to bend and subsequently crack off solder joints or fracture components. Shear stresses as a result of acceleration induced deflection can delaminate circuit traces from substrates substrate. On COTS assemblies, this typically means copper clad on FR-4 substrates. Properly supporting the avionics circuit boards will minimize static drumhead effects. This may limit the selection of COTS components, as not all components will be easily supportable.

To mitigate the risks from acceleration, it is extremely important to evaluate the mechanical stresses that would be acting on each board, and attempt to orient them in ways that will minimize the amount of flexing. In addition, COTS boards may need to be modified to add additional support (e.g., gluing boards to rigid substrates, adding structural ribs, etc.). Dave Steinberg [34] lists several methods of increasing the rigidity of assemblies, and also includes several test cases in his book.

To perform static acceleration testing, a centrifuge or similar equipment is required. The maximum amount of deflection for each assembly will be different, based on what kind of components are being used. Through the course of this study, no non-aerospace COTS parts have been found to have accelerating ratings. Analysis can be very difficult, since each COTS assembly may have hundreds of parts. Thus, testing easily becomes the common denominator of reducing risk in this area. However, testing may be difficult to perform for a

low cost mission, so in lieu of testing, risk can be reduced by comparing your assembly to others that have been launched on equal or worse conditions. The factors to consider include acceleration peak, maximum jerk, and axes of accelerations.

5.6 Aerodynamic Heating

During ascent, aerodynamic heating will occur due to frictional forces within the atmosphere. The fairing may reach several hundred degrees, but does not appear to be a major issue for the payloads. The fairing is put in place for aerodynamic, thermal, and impact protection reasons. As the launch vehicle reaches sub-orbital altitudes, the atmosphere is vented, so radiation is the only direct heat transfer mechanism to the payload. And as the launch vehicle ascends further, the heated fairing will be jettisoned to prevent conduction of the fairing's remaining heat energy to the launch vehicle. This in turn, cuts the amount of time available for transferring heat indirectly to the satellite payloads via conduction and directly via radiation.

A well designed and documented launch vehicle will have specified temperatures inside the fairing, and at the payload adapter where the satellite will directly attach. If the payload area temperatures exceed the satellite's storage temperature (or operational temperature if launched hot), then a time domain thermal analysis may be required to show that the satellite avionics will not exceed survivable temperatures.

5.7 Venting of Atmosphere

During ascent, the atmosphere surrounding the launch vehicle can decrease to almost zero within a matter of minutes. OEM COTS parts typically come as bare boards. As we will examine later in the space radiation environment, a conductive box (e.g., made of aluminum) may be required for survivability.

If an avionics assembly is built with no seams, venting of atmosphere will result in the assembly becoming a pressure vessel. Boxes not designed to be pressure vessels may explode upon ascent. In addition, during vacuum testing, different rates of vacuum pump-down and vacuum release may even result in the box either exploding, or imploding under test. It is entirely possible to destroy a vacuum chamber due to an exploding assembly. Thus, even under test, venting is a serious issue.

During launch, an exploding assembly during launch can cause destruction to the spacecraft itself, multiple other payloads, and result in the loss of a launch vehicle. NASA APR 8070.2 requires analysis for the worst case pressure differential with assemblies. Analysis can be accomplished with FEA software. If the margin of safety does not exceed a factor of two (2), testing is required to confirm that the assembly will not result in a catastrophic event.

However, putting arbitrary vents in an assembly can defeat EMI suppression measures on avionics boxes. In order to provide more venting, more effective cross sectional area must be provided for gas transport into and out of assemblies. At the same time, the more seams there are in assemblies, the more EMI can pass in and out of the assembly. One consideration is that holes look like wave guides to EM waves. The largest dimension of any seam determines the fundamental mode and cutoff frequency of the wave guide.

To keep the cutoff frequency high, multiple small holes in the shape of a circle are preferred over one large hole [40][41]. Any deviation from a circle will result in a lower cutoff frequency, and can contribute to increases in EMI susceptibility and radiation. The good news is that circular holes are cheaper and easier to manually manufacture than square or rectangular holes. However, the limit on how small the hole can be may be an issue of what tooling is available. The following figure shows a grid of 0.5mm inner diameter holes.

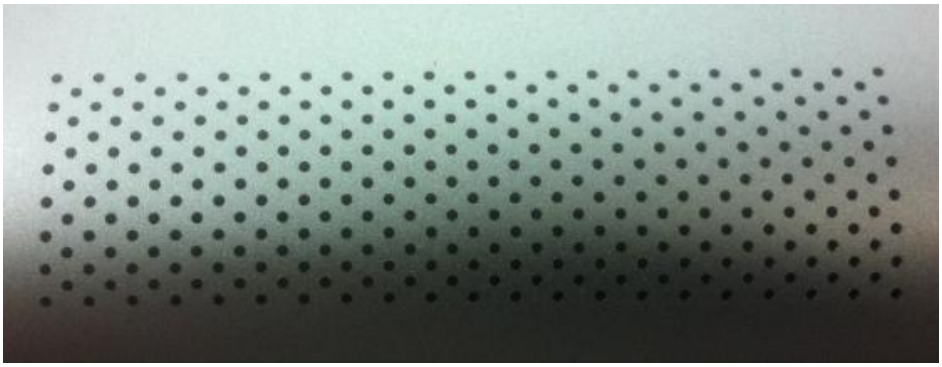


Figure 5.5: Example 0.5mm I.D. Holes for Acoustic Transmission and EMI Suppression

According to Iskander [40], the cutoff frequency of a rectangular waveguide of dimensions a=b excited in $TE_{mn}=TE_{10}$ mode is:

$$(f_c)_{10}^{TE} = \frac{1}{2\pi\sqrt{(\mu\epsilon)}}\sqrt{\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2} \qquad (4\text{-}1)$$

Balanis [79] shows that the cutoff frequency of a circular waveguide of an inner diameter a is:

$$(f_c)_{11}^{TE} = \frac{1.8412}{2\pi a\sqrt{\mu\epsilon}} \tag{4-2}$$

For comparison, both waveguide materials are assumed perfect electrical conductors (PEC) in a free space medium. Dimensions for the above waveguide calculations are in meters, from a range of 0.5mm to 10mm. The following graph shows cutoff frequency vs hole size.

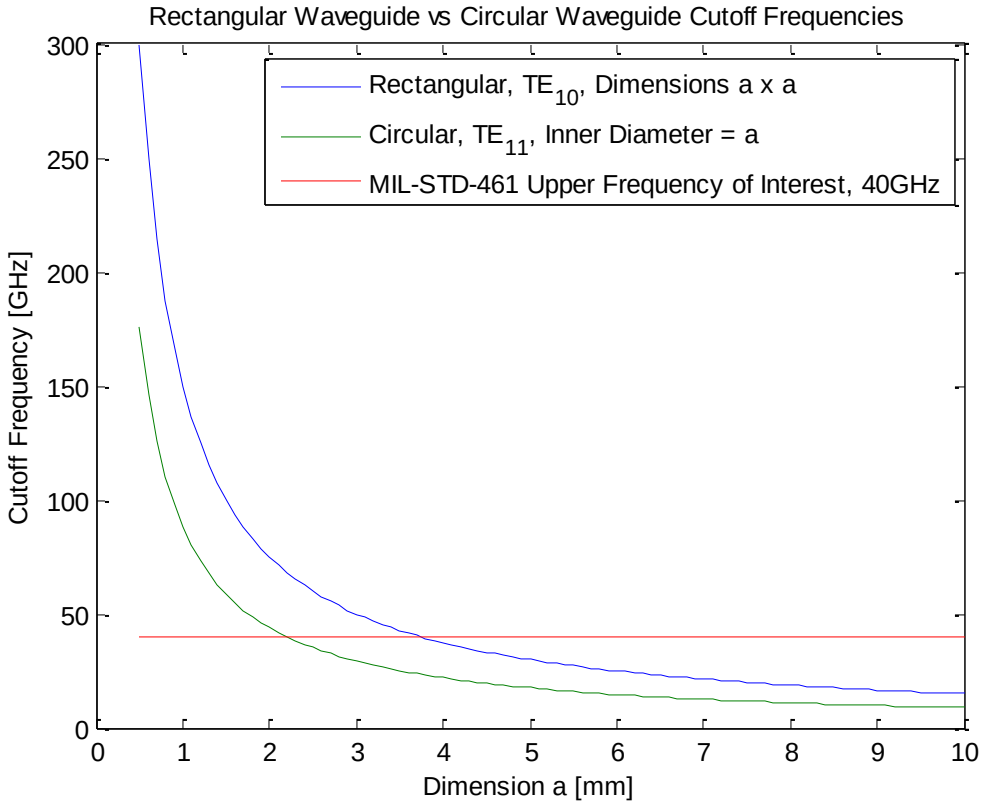


Figure 5.6: Cutoff Frequencies of Rectangular and Circular Waveguides

Note that circular waveguide cutoff frequencies are lower than its rectangular counterpart. The comparatively simpler circle hole manufacturability offsets the lower cutoff frequency.

Using MIL-STD-461 as a reference, the highest frequency of interest in EMC is 40GHz. A circular hole dimension of about 2mm or less will prevent the hole from acting as a waveguide to frequencies of interest. With waveguide excitation eliminated, shielding thickness, conductivity, and skin depth (versus frequency) will dominate EMI transmittance.

Aside from EMC issues of vent holes, when the atmosphere of the spacecraft is completely vented, all board level components not in pressure vessels will eventually experience high vacuum. High vacuum can cause immediate and long term damage to components. And since electronic components are designed very compact, drilling holes to relieve pressure is not an option. Thus, non-vacuum compatible components must be replaced with vacuum compatible equivalents. After a COTS board has been removed of all known vacuum vulnerable components, it should be tested under vacuum to verify that the remaining components will survive.

According to the spacecraft systems engineering (SSE) book, plastic packages for IC's will remain relatively stable in vacuum [03]. However, the plastics used for packaging can absorb moisture and outgas once the spacecraft experiences vacuum. Thus, COTS electronics, and any other avionics assemblies containing plastic packaging should be stored in conditions where moisture absorption is prevented (e.g., moisture controlled bags, or dry nitrogen environment).

One notable type of component that is susceptible to damage by high vacuum is the electrolytic capacitor. Electrolytic capacitors can be found very commonly on COTS parts due to their low cost and high bulk capacitance values. According to an application note by Cornell Dublier [35], this type of capacitor has a built-in vent which is used to safely expel hydrogen and other gasses which evolve during operation. The document also lists several common electrolyte solvents such as ethylene-glycol. According to NASA-HDBK-4006, pressures within 100-1000km altitudes can range between 10^{-10} to $5x10^{-8}$ Torr. At these high vacuum levels, the ambient pressure is much lower than the vapor pressure of common liquid electrolytes [35][36]. Thus, the differential between electrolyte vapor and ambient pressures will result in the solvent flashing off and being vented out of the capacitor. The loss of the solvent results in a defective capacitor. The mitigation for this type of issue is board rework and substituting the capacitor with a vacuum survivable capacitor. Products like Vishay's or Sanyo's OS-CON series [38][39] of capacitors eliminate the issue of electrolyte vaporization, while providing a range of equivalent electrolytic capacitances.

Chapter 6: Space Environment

6.1 Vacuum and Temperature De-Rating

In space, the satellite will be operating under vacuum. The simplest thermal issue that comes up is from power dissipation and heat transfer. On satellites dealing with hundreds of megabytes of data, you will likely require a microprocessor based computer which can simply interface with large mass storage devices. Microprocessors alone can easily use multiple watts of power during normal operation. On Earth, this is usually not a problem since a high power device can use a heat sink and fan. In space however, there are only conductive and radiative heat transfer mechanisms. Thus, it is important to select COTS components which do not require any convective cooling. In addition, because convection has been removed from the equation, a COTS assembly's 'ambient' operating temperature range will no longer be the same. To prevent over-temperature conditions, hot spots should be located to get a baseline maximum temperature.

As an example of vacuum temperature derating, the following describes a case of HSFL thermal testing for a candidate flight computer. A thermal image is shown below of a COTS MPL MIP405 PowerPC based PC/104 single-board computer operating in air. The worst case hot spot was at the IBM PowerPC 405GPr CPU. With an ambient temperature of around 23C, the PowerPC CPU shows a 10.5C rise in case temperature.

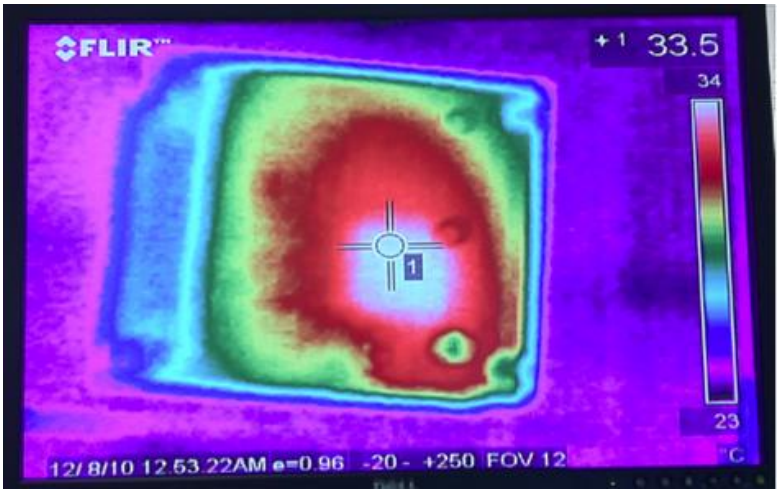


Figure 6.1: Thermal Image of MIP405 PowerPC Computer, 3-5W Nominal Dissipation

According to the MPL MIP405 datasheet, the extended temperature test confirms operation of the assembly from -40 to 85C [44]. However, the IBM PowerPC 405GPr datasheet specifies that the recommended operating case temperatures are from -40 to 85C [43], with a absolute maximum biased temperature range of -40C to 120C. The datasheet notes that damage can result if the CPU is operated outside of recommended temperatures. Thus, to prevent violation of the CPU's recommended thermal specification, the higher end ambient temperature should kept at least 10.5C less than the maximum 85C. Thus, in air, the actual ambient temperature should be kept at less than 74.5C.

From the above testing, we confirmed the temperature range when operating in air. But what we really want to know is its usable temperature range in vacuum. Using the above gathered information, the PowerPC CPU was confirmed as the worst case high temperature component. Thus, we can now carry out a targeted set of measurements under vacuum. In the below figure, the MIP405 PC/104 is mounted on an aluminum base plate, along with its hard drive and power regulation board stacked on top. The MIP405 is on the bottom, which partially simulates the thermal environment that the CPU would have in its flight configuration.

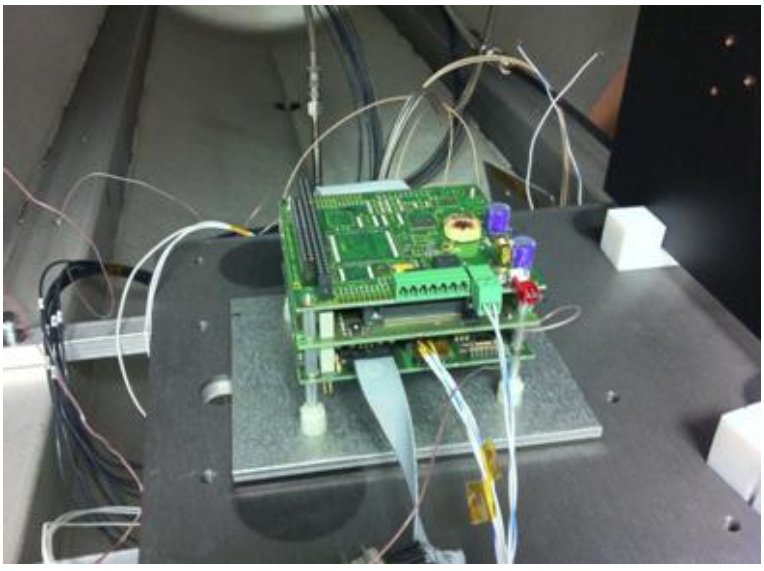


Figure 6.2: Setup of MIP405 PC104 Stack in Vacuum Chamber for Testing

The PC/104 stack's thermal path to the base plate is via four 15mm threaded spacers and #4-40 screws. Thermocouples were attached both to the CPU with an adhesive pad and to the base plate. Note the purple electrolytic can style capacitors on the top board. Those

capacitors are actually the solid-state OS-CON capacitors which were are mentioned in the previous section. To date, the capacitors have survived through multiple vacuum cycles, and still continues to operate more than a year later.

To initiate the test, the chamber is closed, and a vacuum roughing pump is used to pump down the pressure to below 10^{-4} Torr. When vacuum is sufficiently achieved, the MIP405 board was turned on. The next figure shows the transient thermal response of the CPU versus the base plate temperature. The graph shows that the CPU peaks at around 61.5C. After about 1.5 hours, the differential (CPU - Base Plate) temperature settles at around 32C.

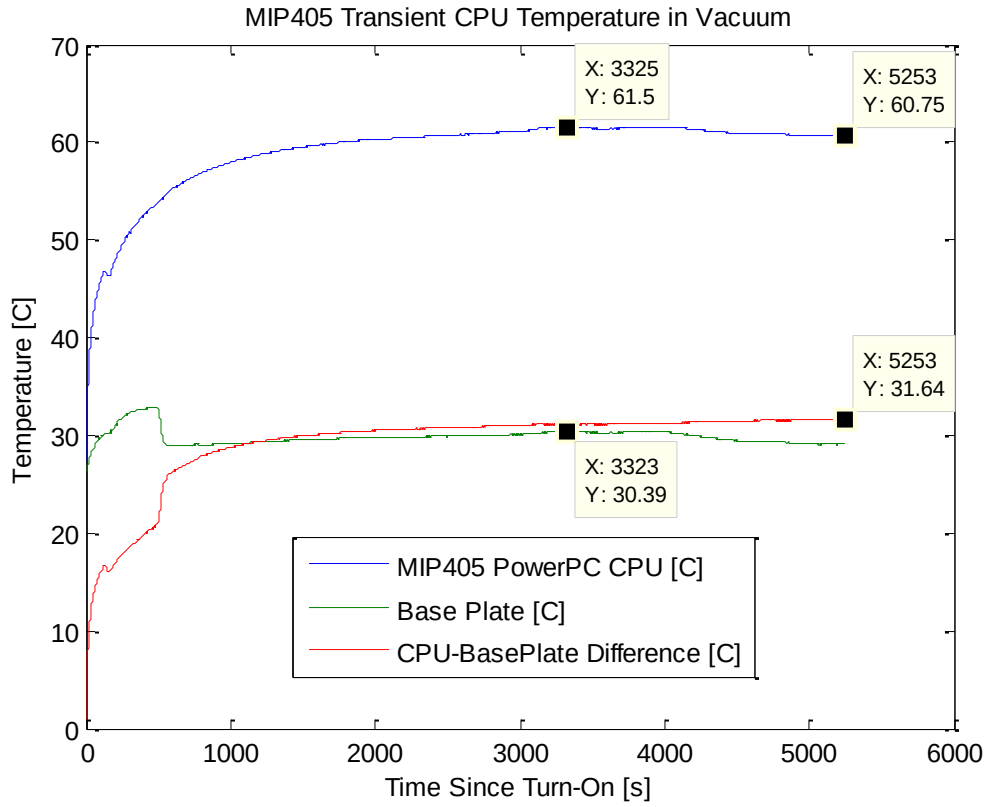


Figure 6.3: MIP405 Transient CPU Temperature in Vacuum

Since ultimately, we are concerned about the CPU's temperature going beyond manufacturer specifications, we are now finally able to de-rate the assembly for vacuum operation. At a maximum CPU case temperature of 85C, a temperature rise of 32C versus its base plate, and a measurement error of around +/- 2C, the base plate temperature must not exceed 51C. Thus, from the initial -40C to 85C rating in air, we now have a -40C to 51C rating under vacuum. Ideally, the test would be repeated by ramping up and regulating the temperature on

the base plate to verify CPU temperatures. This would reveal any non-linear power dissipations as a function of temperature.

If a re-test is not possible, then a larger operating margin is necessary to attempt to compensate for increasing power consumptions with increasing temperatures. For instance, Power MOSFETs commonly used in DC/DC converters have a rising R(on) when its junction temperature rises. This results in higher power being dissipated for the same amount of power demanded by the system. Thus, a simplification such as superposition cannot fully define the relationship between a reference base plate and component temperature.

In this MIP405's case, if a greater temperature range is desired, better heat transfer paths can be added from CPU to the base plate. In a flight configuration, the internal base plate would be the PC/104 stack's avionics box, which is driven by the actual spacecraft interface temperature. As long as the spacecraft interface is kept at the right temperature, the internal temperatures should follow.

Note that the FLIR camera that was used in this testing is quite expensive. Although it is an extremely useful piece of equipment, most small laboratories would not be equipped with such a IR camera. At the time of writing, the lowest cost FLIR camera available, the FLIR i3, costs approximately $1,200 [52]. Alternatives include using contact thermometers, and slowly sweeping a board with a small bolometer. One such non-contact temperature sensing bolometer product is the Texas Instruments TMP006 [51].

Other alternatives considered include IR guns and modified web cameras in IR operation. IR guns turned out to be quite unwieldy for locating hot components, especially on boards where tiny surface mount components dominate. Thermal infrared energy lies in mid-IR or far-IR ranges. A survey of web cameras modified for IR operation appear to only sense near-infrared energy, and thus is not a usable solution for survivable avionics temperatures.

This type of test should be performed especially when devices have a relatively high power density, or when the assembly uses power on the order of watts. In addition, a device should be tested in the worst case operational power dissipation case. In the above case, the MIP405's worst case power consumption would be when all its normal spacecraft interfaces and computational capabilities are being actively used.

De-rating COTS components for the expected vacuum environment should be considered a normal part of COTS to space avionics conversion. When the resulting bounds of operation for all avionics are established, the data can be used as bounding conditions to optimize the spacecraft's thermal control design. However, in long space mission developments, custom flight hardware is typically not built until after a critical design review (CDR). So if post-CDR testing of flight hardware yields unfavorable thermal results, either the part or spacecraft thermal redesign can be very expensive. This is one area where COTS becomes helpful useful. Hardware in-hand, possibly right after a preliminary design review (PDR), allows for the generation of advance information to better shape a satellite design.

6.2 Thermal Cycling

A satellite orbiting the Earth in LEO will go through about 15.5 orbits in 24 hours. The below figure shows a satellite's orbit which goes through umbra (eclipse) and penumbra (sunlit). At the least Sun case, roughly 33% of the time will be spent in eclipse, and the rest will be spent in the Sun. That means that a satellite will go through about 472 thermal cycles a month, and about 5673 thermal cycles a year.

According to Dave Steinberg [34], slow sustained thermal cycling has more severe effects than vibration. This is because materials with different coefficients of thermal expansion can induce tremendous stresses on its interfacing materials. High stress concentrations, which slowly increase with slowly increasing temperatures can permanently deform materials. This is referred to as creep. Subsequently, during the downward transition of a thermal cycle, the permanently deformed material now is faced with double the stress induced for the same amount of reverse deformation. Repeated cycles will fatigue materials twice as much stress until they ultimately fail.

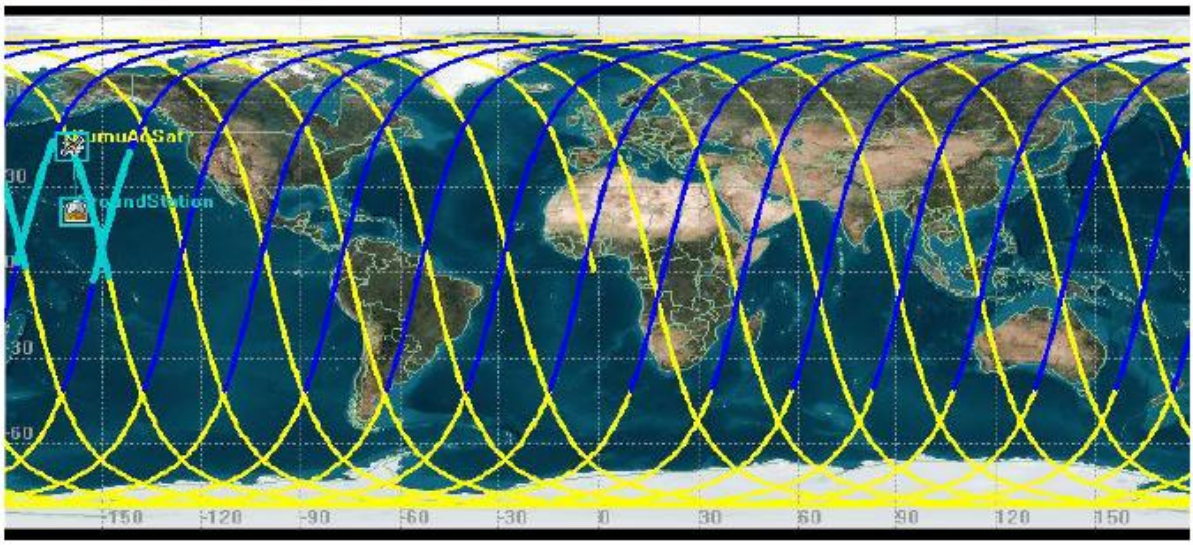


Figure 6.4: 98 Degree Inclination Orbit with Sun and Darkness Ground Tracks

Vibrations on the other hand, flex materials repeatedly and very rapidly, but their cycles are so quick that materials like eutectic (Sn63/Pb37) solders do not have time to relieve stress by permanently deforming. Thus, vibration is much less likely to initiate cracks in a material like solder, but rather exacerbate already existing fatigue. Vibration induced failures in electronics can actually be traced back to thermal cycling more often than vibration itself [34]. Fortunately, the only vibrations a satellite should experience are upon ascent, or when active attitude maneuvers are being performed.

Electronics industry standards organizations such as JEDEC and IPC can steer designs and testing for tolerating thermal cycling, but the standards are not mandated across the industry. COTS assemblies are not likely to be built for large thermal cycling amplitudes.

Dr. Reza Ghaffarian, at JPL, has done extensive testing for thermal cycling on BGA IC packages [46][47]. He demonstrated that with accelerated test profiles under IPC 9701A and MIL-STD-883, a couple hundred thermal cycles in the -55C to 125C range can crack BGA solder joints. The research applies both for NASA/ESA accepted space solders, as well as SAC305/405 solders being used in RoHS electronics assemblies. Going along with the MIP405 example, the PowerPC chip uses a high density BGA package which is subject damage by thermal cycling.

Solder reliability with thermal cycling has been heavily researched for other package types for both leaded and lead-free solders. The common result is that solder will eventually fail through extreme and repetitive to thermal cycling damage [58].

Another issue is that nearly every COTS part you can find will be built with FR-4 fiberglass epoxy laminate. The FR-4 coefficient of thermal expansion in the Z direction (along plated through holes) can be between 4 to 20 times higher than in the XY direction (along component top/bottom component planes) [54][55]. Thus, plated through holes are more likely to fail well before solder joints [34]. The thinner the plated through hole material, the less cycles it will take to fracture under thermal cycling. COTS vendors are not likely to volunteer process information for board fabrication, so calculation of thermal cycles to failure may be extremely difficult and an inefficient use of time. It would be much more efficient if there was a way to just eliminate thermal cycling all together.

The primary mitigation against thermal cycling damage is to dampen the thermal cycling amplitudes. Dampening can be accomplished maneuvering the satellite to thermally favorable attitudes, and with thermal insulation. Attitude maneuvers for thermal mitigation may be very disruptive to missions which require pointing, and to power generation. Thus, thermal insulation is the preferred method of mitigation. By creating an semi-adiabatic environment for avionics can greatly reduce thermal cycling from cyclic sun exposure.

Unfortunately, a semi-adiabatic environment may mean that a spacecraft's solar panels will feel the brunt of thermal cycling. Left completely insulated from the spacecraft, solar cells such as Emcore's BTJM triple-junction cells can quickly cycle through enormous temperature differentials of over 100C [45]. Although solar cells like the BTJM are built for high amplitude temperature cycling, solar cells have lower efficiencies at higher temperatures [53]. The thermal issues for solar cells can be reduced by routing heat conduction paths to the opposite side of sun exposure, but at the expense of mass and volume. Thus, in a small and tightly integrated satellite, solar power efficiency/reliability, mass/volume, and protecting avionics against thermal cycling are all in contention.

To verify a thermal model of a satellite, the ultimate test would be in the actual space environment. Before then, a lower cost method is desired for testing of the satellite's thermal balance and transient thermal performance. In **Figure 6.5**, the HSFL thermal vacuum

chamber is shown. The vacuum chamber was designed to be large enough to fit entire remote sensing microsatellites, and accommodate tens of feed-throughs for sensors, external test equipment, and RF interfaces. For thermal cycling tests, the chamber can simulate free space for radiative heat loss during eclipse, provide radiated heat to simulate the sun, and be used as a temperature forcing gas chamber. In addition, MIL-STD-1540 thermal vacuum and thermal cycles can be performed for flight qualification and acceptance.

Figure 6.5: HSFL Thermal Vacuum Chamber for Microsatellite Testing

Building an ideal thermal environment around avionics allows COTS products to be used with much less risk of damage from thermal cycling. Using this type of thermal vacuum chamber enables verification of thermal balance, thermal isolation, and allows for testing beyond maximum predicted environments for risk reduction.

If thermal cycling is expected (in the case of solar panels), FEA analysis should be used to determine stresses on components, and estimate lifetimes based on existing fatigue data. Then actual thermal cycling should be performed for a worst case flight-like simulation.

6.3 Plasma Environment and Spacecraft Charging

Radiation from various sources (e.g., sun) can ionizing create plasma in LEO, which is the range of orbital altitudes that this study is concerned with. Plasma is atoms which are ionized, and have inter-atomic distances similar to a gas. In LEO orbit, satellites routinely fly through these plasma fields. Combined with high electric fields from avionics and solar panels, a plasma atmosphere can lead to unintended conducting paths.

Perhaps most exposed device to the plasma environment, are the solar arrays. NASA-HDBK-4006 [37] shows detailed photos of devices that have arced, and then have subsequently burned up. However, the handbook notes that the voltages that are being used are in excess of 100V. It also notes that prevention can be achieved by not using voltages over 55V, and not placing electrical contacts with >40V differential between each other.

Thus, for COTS avionics which operate on 28V and lower voltage busses, this may not be a concern. However, some remote sensing experiments may require high voltage power supplies, which could also be COTS products. In this case, the NASA handbook [37] can provide some guidance on protecting against arcing.

Related to the plasma environment, Dr. Holbert has an detailed explanation of spacecraft charging [80]. There are many factors to how spacecraft charging occurs. What we are most interested in for this study is what is the risk of spacecraft charging. According to Dr. Holbert, the two categories of spacecraft charging are surface charging, and internal dielectric charging.

As we will discuss in the space radiation environment chapter, electrons of tens of keV can be injected into the magnetosphere by the sun. Upon hitting a spacecraft, the electron can charge up surfaces of a spacecraft. If the charge cannot be redistributed to the spacecraft, charge will build up, and eventually result in electrostatic discharge (ESD). Any IC's hit with ESD may be destroyed. Localized arcing can also produce random EMC issues within circuit boards, and around the spacecraft. Dr. Holbert notes that the solution is to have common grounding for all internal metallic structures, as well as the rest of the spacecraft structure [80]. In other words, never leave a metallic structure floating.

Next, Dr. Holbert explains that internal dielectric charging results from the penetration of high energy electrons which end up 'trapped' in dielectrics. If the charge cannot be dissipated quick enough, the buildup of trapped charge will continue to increase, until dielectric breakdown. This especially occurs in materials such as Kapton or Tefzel [80]. Shielding around Tefzel insulated wire harnesses cables will help to ground any ESD from insulation. There does not appear to be a lot that can be done for charge buildup in COTS FR-4 circuit boards. In a custom circuit board, ground planes and guard traces can be used to provide the a measure of mitigation similar to harness shielding.

6.4 Atomic Oxygen

The NASA LDEF project was a long-term space materials degradation experiment. During several years of exposure to the space environment, materials were characterized for their different sources of degradation. As mentioned previously, different sources of radiation can ionize materials in LEO, generating ions like atomic oxygen. Atomic oxygen is very reactive with a wide variety of materials, and is one of the most abundant species of ions in LEO. This can lead to failures in conformal coatings, wire insulation, and other exposed materials. A NASA study [50] shows that atomic oxygen can very quickly erode double aluminized Kapton to the point of disappearing. If Kapton were used on the outside of a spacecraft, the material would eventually be eroded away. Atomic oxygen degradation poses a risk to all space exposed materials. Significant research has been done by NASA, ESA, and its suppliers to mitigate risks posed by atomic oxygen exposure. All avionics directly exposed to space should be evaluated for their exposed materials, and any material vulnerability to atomic oxygen.

6.5 Micrometeoroids

Typical LEO satellite velocities will be around 7 to 8 km/s. At these speeds, collisions with large space debris and other objects can be catastrophic, and there is not much that can be done to shield against a major collision, such as another similarly sized satellite. But for smaller debris in the sub-millimeter range, called micrometeroids, cost effective protection can be achieved. Micrometeroids can come in any shape, material, and with varying kinetic energies, so the best that can be done is mitigate the majority of expected impacts. The SSE book notes that micrometeroids impacting a satellite at 5-20km/s have been known to cause

damage to satellites and even perforate honeycomb structures [03]. The figure below show meteroid damage on the NASA Long Duration Exposure Facility (LDEF).

The primary protection that the SCSE book recommends is using one more sacrificial bumper layers to fragment debris, and have a gap between the next layer to allow for fragments to spread their energy over a larger surface area. Bumpers can be in the form of metals, structures, and other lightweight materials like Kevlar and multi-layer insulation. NASA's public lessons learned entry 0705 [49] provides guidance on using MLI for micrometeoroid protection.

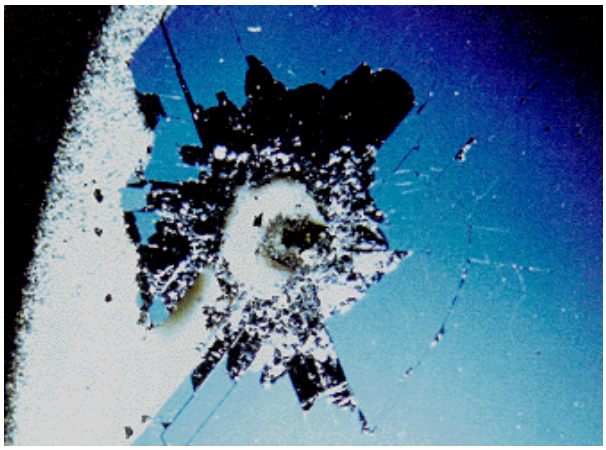


Figure 6.6: Meteroid Damage on MOS Detector, Courtesy of NASA

COTS avionics can be protected if placed in aluminum box, or at least behind one or more bumper layers. For a small satellite, the solar panels and main structure can end up as the bumper layers. In areas where no solar panels are covering, multi-layer insulation is commonly used for micrometeroid protection, among its other favorable characteristics.

Chapter 7: Radiation Exposure

7.1 Radiation Environment in LEO

Perhaps the most difficult issues to handle for COTS avionics come from space radiation exposure. Radiation in the space environment varies with space weather conditions, and is always present at some level. Understanding radiation sources, estimating exposure, and knowing its effects are vital for cost effective risk mitigation. Fortunately, in the past few decades of satellite activities, a great deal of analyzed data has been compiled. As a result, reasonable predictions of radiation effects on satellites now can be made based on periodic sun characteristics, and observed worst case transients.

To better understand radiation, we first must look at its sources and what kind of exposure to expect. According to a NASA, the nearest source of radiation we have is the sun [20]. Radiation can come in the form of highly energetic protons, neutrons, electrons, and heavy ions with sharp peaks in the X-ray portion of the spectrum. Earth-bound energy either gets to Earth, escapes the Earth's influence, or becomes trapped in its magnetosphere. The areas of trapped energy are referred to as the Van Allen radiation belts [21].

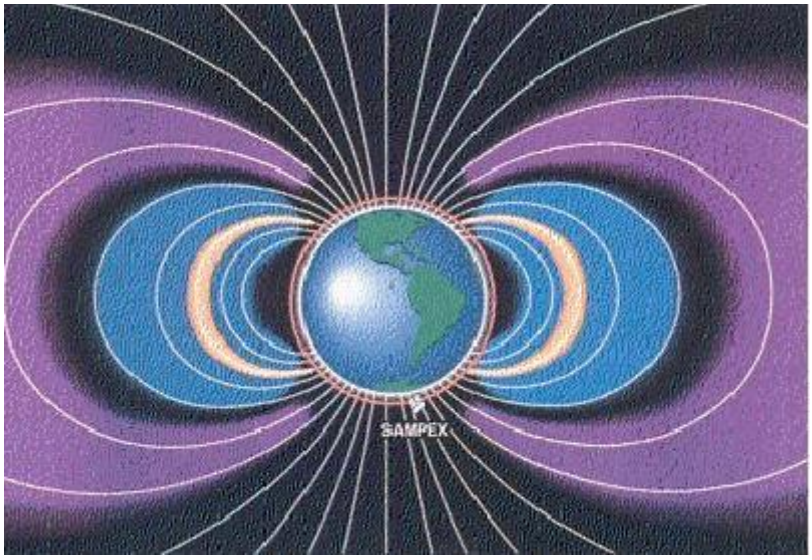


Figure 7.1: The Van Allen Belts, Courtesy of NASA

Figure 7.1 shows an artist's visualization of the belts and their relative intensities. From lowest to highest radiation energy, the drawing shows purple, blue, and orange-red. The orange-red area is hypothesized to be made up of trapped galactic cosmic rays (GCR) which come from outside our solar system. GCR's, of which are made up of extremely high energy

particles. The blue region represents the next highest energy level, which consists mainly of trapped protons and electron. These trapped electrons and protons have energies greater than 30keV, and stay in the Van Allen belts until their energy is dissipated or they escape [20]. LEO satellite radiation exposure increases monotonically from altitudes of 300km to 3000km, which is the transition from the inner blue region to orange-red GCR region.

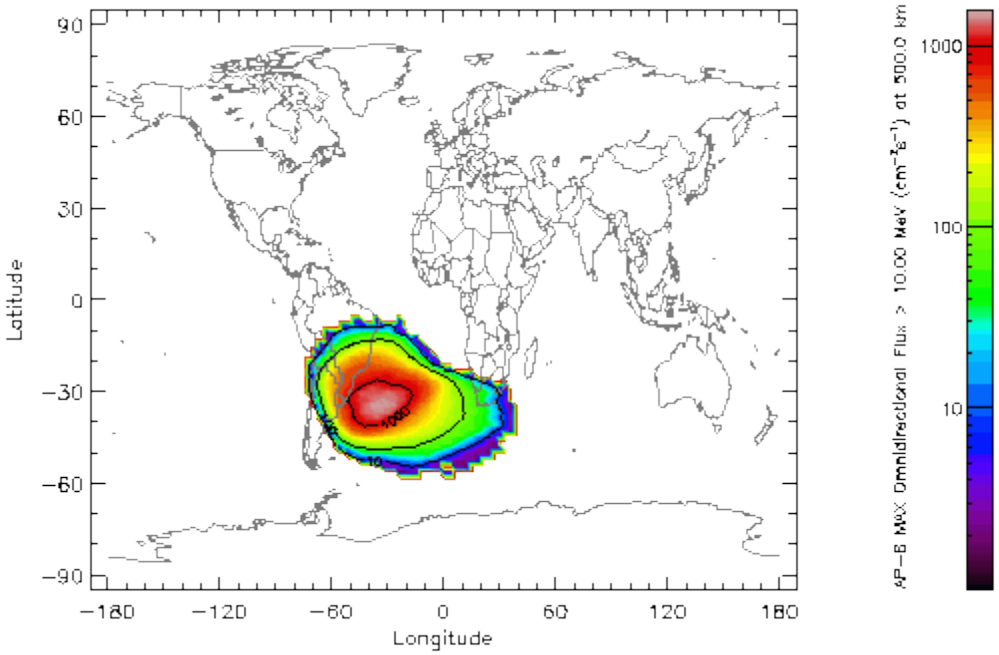


Figure 7.2: The South Atlantic Anomaly, Courtesy of NASA

Earth observation satellites may actually prefer lower altitudes to use smaller telescopes and to achieve better spatial resolution. But even lower altitude satellites are not completely safe from extreme exposures of radiation. **Figure 7.2** shows an area of high radiation, referred to as the South Atlantic Anomaly (SAA). The SAA reaches deep into LEO orbits, affecting all satellites which cross it. A satellite passing through the SAA will result in a higher occurrence of radiation induced issues, as well as increased radiation dose rate.

The important thing to know is that radiation exposure is a normal part of operating satellites in LEO. All the issues that come with radiation exposure will especially be present for COTS components which are not hardened for radiation. COTS components are designed to operate without regard for radiation effects, and thus must be handled carefully to prevent potentially mission ending problems. All types of semiconductor devices are affected in one way or

another, and thus the software that runs on them will be affected as well. The next sections will cover what types of radiation induced issues can be expected.

7.2 Cumulative Effects

7.2.1 Total Ionizing and Displacement Damage Dose (TID/DDD)

First, we'll take a look at the long term effects of radiation exposure. According to JPL [24], a constant source of damaging radiation dosage comes from protons and electrons trapped in the Van Allen belts. Less predictable, but significant sources include GCR's. Measured in the SI units 'rad', the total ionizing dose (TID) is the cumulative amount of ionizing radiation dosage that a device has received.

Ionizing radiation is radiation which interacts with atom inside a device and ionizes it. SNL [28] describes two different mechanisms of ionization. The first is direct ionization, in where a heavy charged particle (e.g., nickel) collides with, and dissipates its energy in semiconductor material. If the charged particle dissipates all its energy in the medium, it will stop. If not, the particle will exit the material. Direct ionization is seen especially with GCRs where heavy ions plow through semiconductor material with extremely high levels of energy. This leaves a highly conductive plasma 'funnel' in its wake. This type of direct ionization can result in thousands of secondary ionizations, and cause large amounts of charges to be collected at arbitrary semiconductor terminals.

The second type of ionization that SNL discusses [28] is indirect ionization. Light particles like protons can pass through semiconductor material without colliding with any nuclei. In fact, according to REIS [54], protons have a hit/miss ratio of 1 about 100,000. Even though the hit/miss ratio is quite low, the fluence of these particles can be quite high, still resulting in significant ionization. So when an impact does occur, protons and neutrons can cause a nuclear reaction. SNL describes a case where a high energy proton-silicon collision causes the recoil of an Si atom, emitting alpha/gamma radiation and results in spallation reactions. The spallation causes Si to breaks down into C and O atoms. Since C and O are much heavier than protons or neutrons, direct ionization can now occur by the now energized products. Because indirection ionization results in the generation of high energy ions, the linear energy transfer as is equal to that of a heavy ion strike [28]. Thus, high energy protons

can provide a significant amount of ionizing dosage. The long term effects of ionization occur when defects are created in the semiconductor material. Electron-hole pair separation is a result, an can commonly result in trapped charges either at interfaces or within gate oxides.

Additionally, Bogarets [23] explains that high energy particle interactions can cause the displacement of atoms from their place in crystalline structures such as semiconductors or glass. This is referred to as a displacement damage dose (DDD). Displaced atoms in semiconductors can result in altered operating characteristics. Effects such as increased leakage current and shifted threshold voltages are common. In optics, such as solar cell cover glasses or lenses, displacement damage can degrade their performance by causing discoloration (e.g., yellowing).

7.2.2 Cumulative Effects on MOSFETs

Take for instance an NMOS device. Used as a switch, the drain can be driven to high voltages, and where the gate is driven at lower control voltage. Electron-hole pairs generated within the gate oxide are especially prone to being swept apart due to the drain/gate electric field across the oxide [54]. The electrons, having high mobility, will rapidly move toward the bulk p-Silicon due to the gate/drain electric field, and the holes will slowly move toward the gate terminal which has the lower potential. Any electrons gaining energy enough from the electric field can get injected into the bulk silicon. This results in hole trapping in oxides.

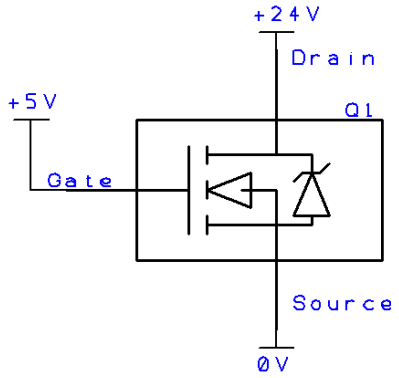


Figure 7.3: Idealized Example of NMOS Bias for Hole Trapping In Gate Oxide

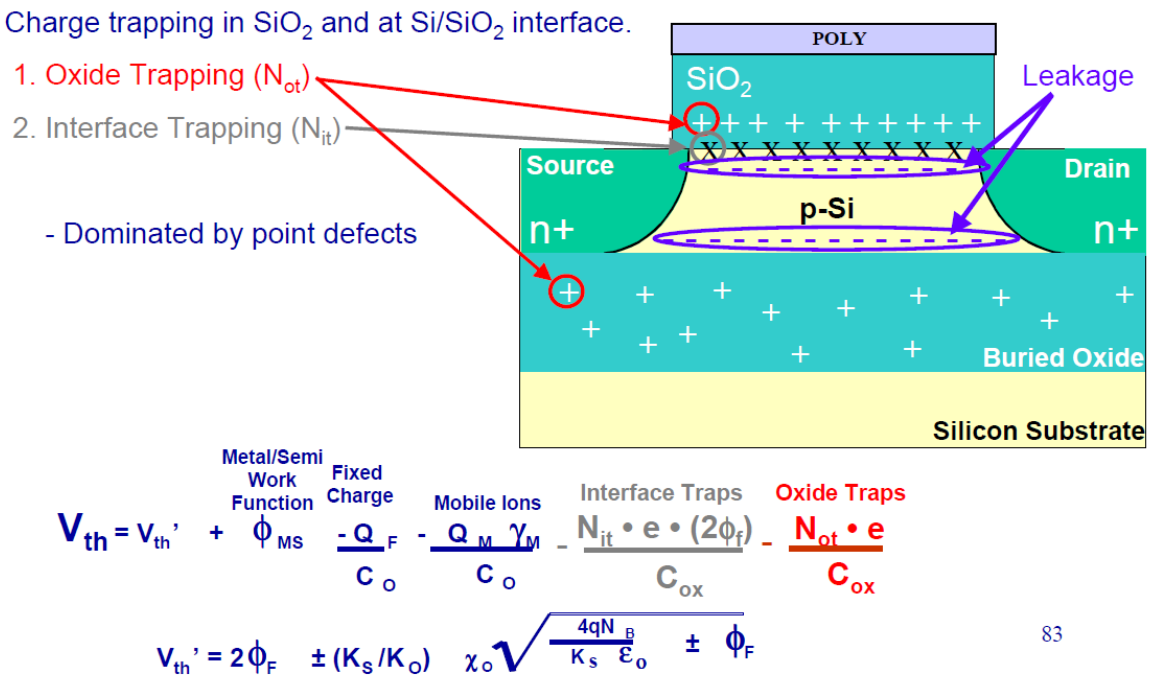


Figure 7.4: TID Effects in MOS Devices, Source: JPL [24]

Trapped charges result in a change of threshold voltage [24]. **Figure 7.4** shows how threshold voltage is calculated, based on the number of trapped charges in the oxide. Notice how the trapped holes in the oxide start to build up an electron channel in the bulk silicon. This is equivalent to driving positive charges to the gate capacitance with a bias voltage.

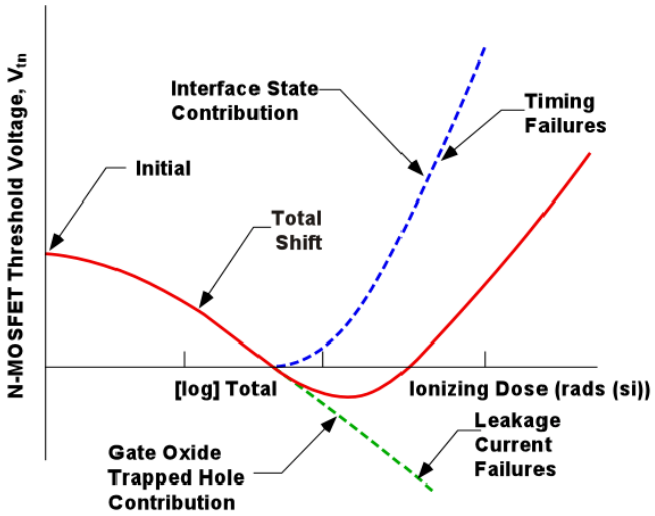


Figure 7.5: TID Effects on NMOS Threshold Voltage, Source: JPL [24]

Figure 7.5 shows a graph of ionizing dose versus threshold voltage for an NMOS device. Because the trapped holes in the oxide start to form a stronger and stronger built-in minority carrier channel, the threshold voltage looks like it is decreasing. Eventually, the trapped holes will attract sufficient minority carriers to facilitate a permanent conducting channel. The effect of decreasing threshold voltage is shown by Esqueda [81] in **Figure 7.6**. At V_{T3} and V_{T4}, zero V_{GS} is still conducting drain current.

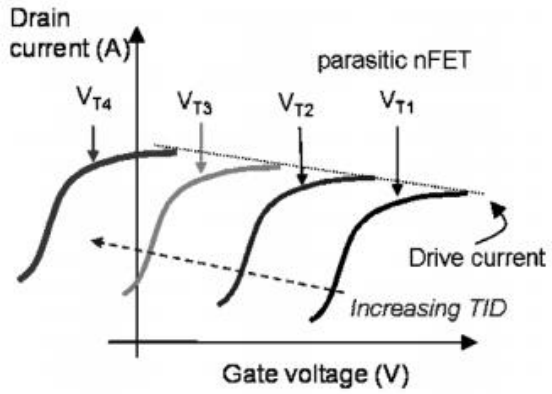


Figure 7.6: Decreasing Vth Effects on I-V Curve, Source: Esqueda [81]

Since most modern COTS technologies are based off of MOSFET technology, the same kind of charge trapping applies to nearly every MOSFET structure. The circuit effects of leakage current and changing thresholds however, are different for each circuit. Thus, to provide more tolerance for TID, it may be helpful to use MOSFETs with higher initial V_{TH}.

During the design phase, a TID rating can be used to define the expected radiation dosage under a given shielding level. In a terrestrial COTS design, devices do not come with ratings for TID. In order to get a TID rating, amongst other radiation tolerance data, NASA has recommended that MIL-STD-883E method 1019.5 be used [20] for radiation screening of non-radiation tolerant devices (883E has been superseded by MIL-STD-883H with test method 1019.8 [26]). Today, there is at least one commercial testing facility for method 1019 [27], amongst several government/research labs which also can perform at least part of the testing [28]. However, purchasing entire lots of candidate flight parts can mean upwards of hundreds of lot component purchases. Thus, radiation testing of all flight parts will be extremely costly in both time and money. Since the COTS paradigm is more cost cutting and performance focused, reliability testing may be waived in favor of a 'typical' TID rating based on assumed complexities of components.

7.2.3 Cumulative Effects on Memory

There are two main categories of memory, volatile and non-volatile. Most memories today will utilize MOSFET technology to build memory cells, and thus will have the same issues stemming from MOSFET radiation exposure. Nearly every COTS avionics assembly will contain some sort of SRAM, DRAM, or Flash memory.

Memory of the volatile nature is dominated by SRAM and DRAM. SRAM latches a state with two cross-linked inverters, and constantly requires power to preserve its state. Large shifts in threshold voltages will prevent the normal operation of SRAM. Leakage current within the SRAM cell increases power consumption, and can leak current to/from shared bit lines, corrupting bit reads/writes and resulting in stuck bits [54].

DRAM stores state in a capacitor. Leakage current will especially have issues for DRAM since the amount of charge stored in each DRAM state-holding capacitor is shrinking with process sizes. Similar to SRAM, leakage current from DRAM cells can corrupt bit lines. But DRAM has the added problem of discharging its small capacitors into bit lines. This will eventually corrupt readings just as SRAM did. In addition, the very nature of DRAM requires constant refreshing of charges in DRAM capacitors. A sufficient amount of leakage current can discharge individual DRAM state capacitors before it has a chance to get refreshed. If a DRAM cell is unable to refresh the state in time, the leakage of charges will leave an insufficient number of charges to recover the original state [24][54].

As for non-volatile memory, typical MOSFET based non-volatile memory types include NAND/NOR flash. Typical NOR and NAND flash technologies utilize MOSFET technology with capacitive coupled floating gates. They are non-volatile because their floating gates can trap electrons, altering the threshold voltage of the MOSFET. Over time, or with just one very high energy particle, ionizing radiation can alter the amount of charges in the floating gate, which cannot be resolved by with a reprogramming cycle. This results in permanent 'stuck' bits. This effect is in addition to ionization induced trapped holes in the oxide, which actually work against the electrons to alter threshold voltages [54].

A relatively new technology is Ferro-Electric RAM, or FeRAM/FRAM. FRAM reads and writes similar to DRAM's charge sensing method. Both technologies utilize capacitors, and both read operations discharge their storage capacitors completely, requiring re-setting of the

capacitor to its original '1' state if charge is sensed. The difference is that FRAM utilizes a ferromagnetic material within the capacitor structure, and instead of storing charge, a polarization state is induced by applying a voltage. The polarization versus voltage curve has a hysteresis characteristic. Thus, a threshold electric field must be induced in order to toggle the polarization.

Because the FRAM cell stores state in the ferroelectric polarization, this makes the device much more resilient to ionizing radiation. Transient charges which are injected into an FRAM structure will eventually dissipate. As long as the transient induced electric field across the ferroelectric material is not higher than the hysteresis voltage, the state will be retained. However, defects induced on oxide layers will still be a problem.

Nguyen and Scheick have explored TID effects on FRAM, and show that some of the earlier models of FRAM can take at least up to 12krad(Si) TID before failing [82]. At a TID of under 5krad(Si), no significant affects were seen on leakage current nor errors in memory. FRAM appears to be a very good candidate for use in spacecraft assemblies containing COTS components. Since it is resilient against radiation, FRAM can be used to implement software error detection and correction schemes to scrub flash and other memories.

7.2.4 Cumulative Effects on Materials

Figure 7.7 shows a table of materials organic insulating materials which was compiled by NASA contractors [73]. Starting from radiation dosages from 1krad and up, materials are shown to have either incipient to mild effects, all the way to severe damage. Radiation exposure for insulating material can be quite high when directly exposed to space (e.g., solar panel substrates and external sensor insulation). Note that the gamma dose is in terms of carbon as the target material. Different materials have different rates of TID accumulation.

More up to date information can be found in a survey performed by JPL in 2008 [74]. This includes a summarized compilation of current data for main categories of spacecraft materials. With the exception of the TFE variant of Teflon, the JPL presentation generally shows that most materials hold their properties up to 10kRad.

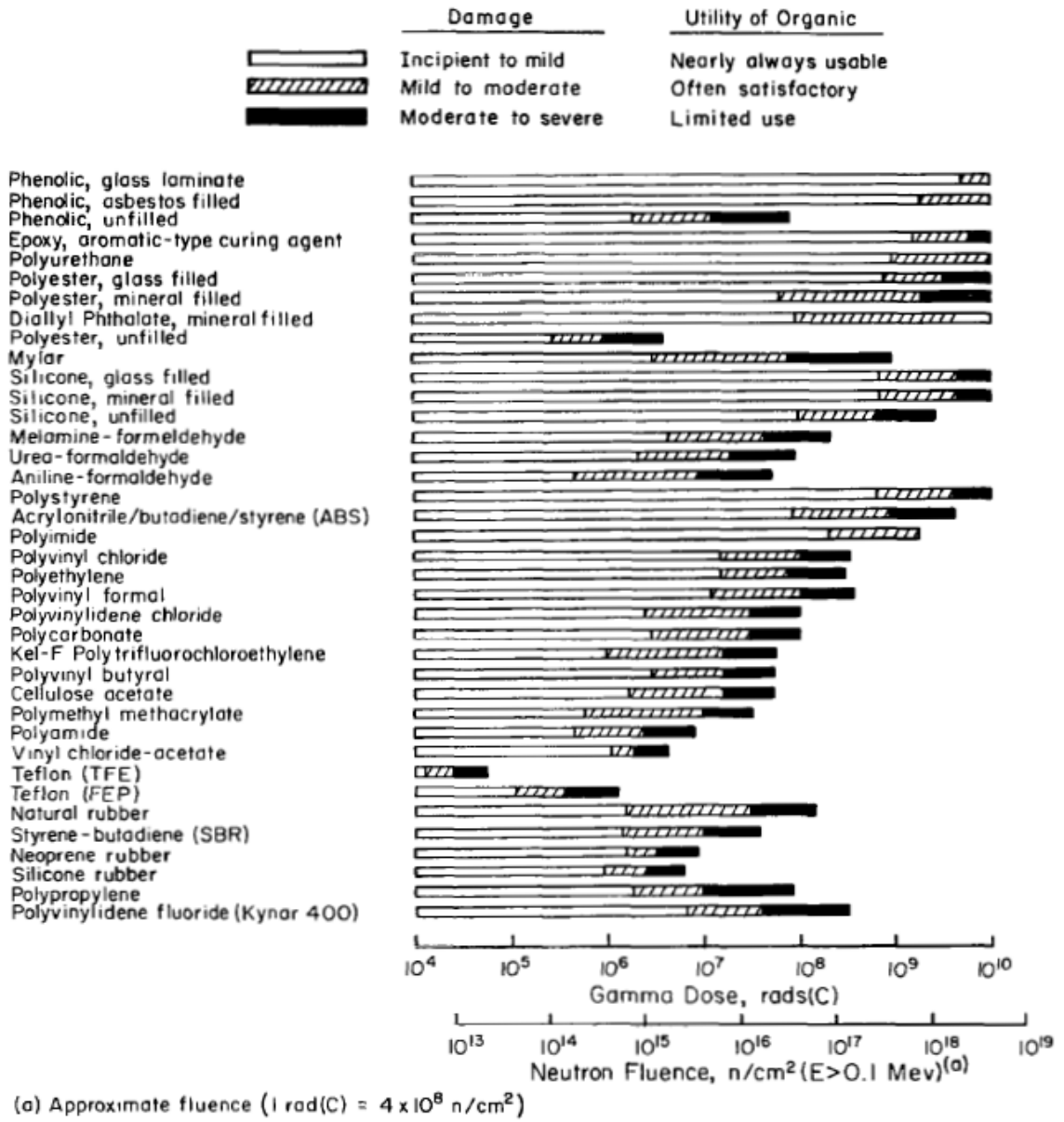


Figure 7.7: Relative Radiation Resistance of Organic Insulating Materials Based Upon Changes in Physical Properties, Source: NASA [73]

As we will see in a later section, shielding is the primary protection against cumulative radiation dosage. Both unshielded and shielded doses can be calculated with radiation and shielding models.

7.3 Non-Destructive Single Event Effects

Single event effects (SEE) are defined by single effects induced by a single charged particle. The European Cooperation for Space Standardization (ECSS) has an excellent summary on radiation effects, and design guidelines [83] which cover all types of SEE's. Nearly every type of SEE results in problems for either power consumption, operating characteristics of hardware, or software. Of the SEE's, non-destructive events are problems that can be cleared by means of software, time, or by resetting a device. Destructive events are referred to as the permanent alteration or damage to a device's operation.

7.3.1 Single Event Upsets (SEU)

Single event upsets are digital symptoms of radiation effects. This can be observed as bits in digital memory that are flipped. For instance, if a picture was stored in memory, and its bits start to be flipped, the picture will no longer contain its original data. According to JPL [24], SEU's are caused primarily by galactic cosmic rays, cosmic solar particles, and trapped protons in radiation belts. Upon striking a transistor, or areas near a transistor, linear energy transfer (LET) occurs. High enough quantities of charges generated at, or in a transistor, can enable it, or inject significant charge into high impedance nodes.

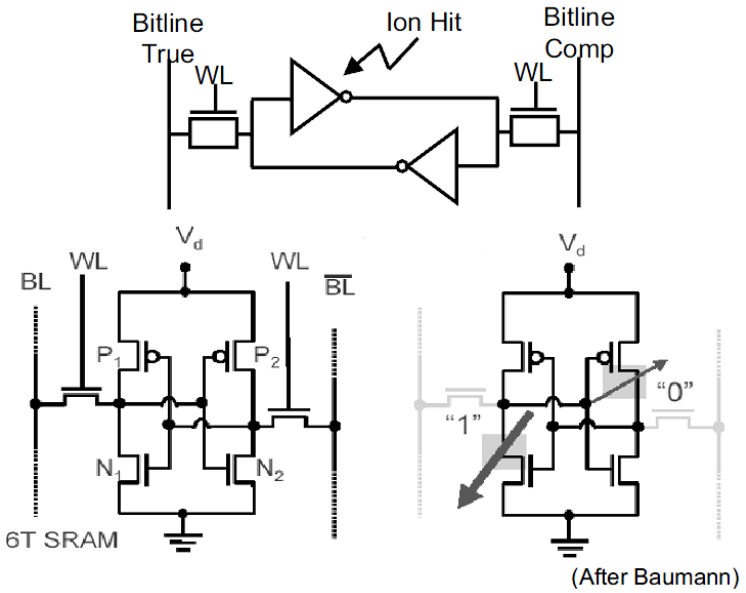


Figure 7.8: SEU in SRAM Memory Cell, Source: F. Sturesson, ESA [25]

CMOS SRAM is a an example of an especially vulnerable circuit. Each bit in SRAM is made up of a pair of CMOS inverters which have their outputs cross-linked to the other's inputs.

Even just a small amount of linear energy transfer to a the interlocked inverters can cause sufficient charges to destabilize its state. This is illustrated in **Figure 7.8** where the output of an inverter is struck with an energetic ion. The presentation states that as long as the ion is able to induce a voltage drop past Vdd/2 (by overcoming the inverter's restoring current), the inverters will both change state and the bit is flipped.

Dynamic Random Access Memory (DRAM) is also vulnerable to SEU, but in a different manner. A typical implementation of a DRAM bit is with one capacitor and one NMOS transistor. The bit's state is read out by emptying the capacitor into a charge sense amplifier. If charge is detected, the bit is a '1'. If not, the bit is '0'. A high energy particle can directly deposit both positive and negative charges in the capacitor, possibly changing its state.

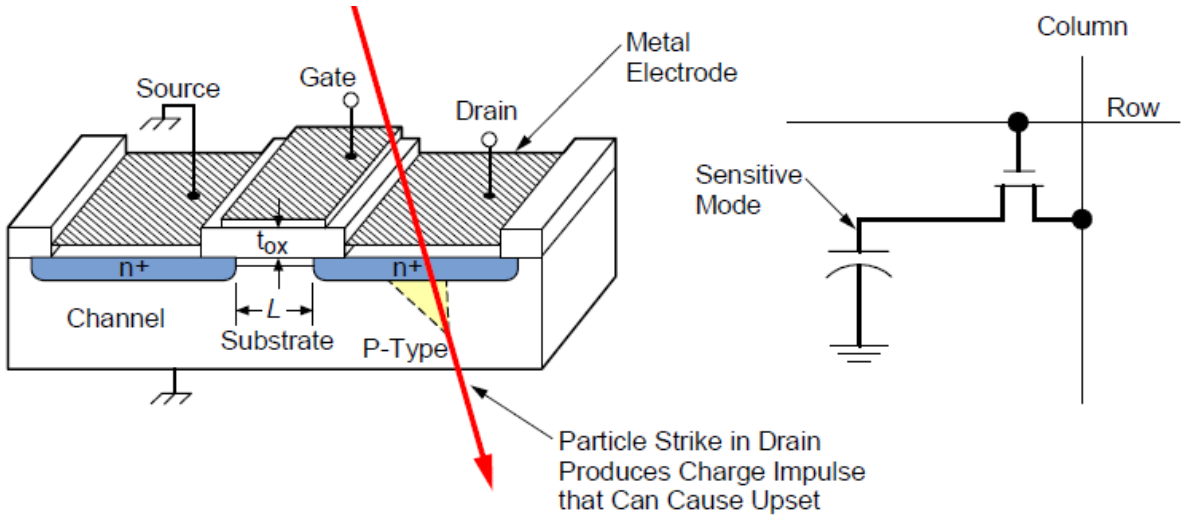


Figure 7.9: DRAM Vulnerability to SEU, Source: JPL [24]

SEU's can also happen in flash memory. A flash memory cell's floating gate is used to store electrons to indicate state, and is surrounded by insulating oxide. **Figure 7.10** shows the structure of an flash cell. Electrons are normally injected and removed from the floating gate via hot carrier injection and quantum tunneling. If a high energy particle is able to deposit sufficient charges in its floating gate, the next read will be incorrect.

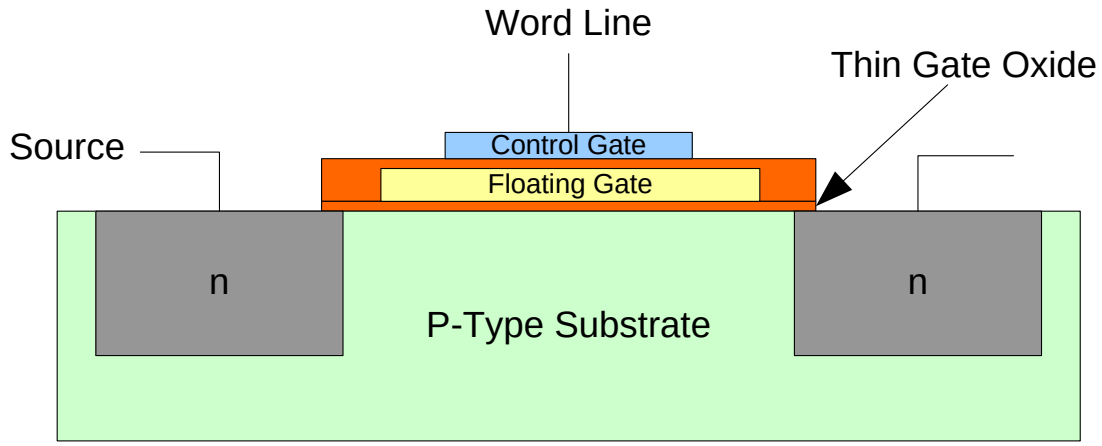


Figure 7.10: Representative Flash Memory Cell

The primary mitigation for SEU's is implementation of memory 'scrubbing' with ECC memory or software error detection and correction (EDAC). This is the periodic run-through of each word stored in memory, and correcting all flipped bits. If done often enough, and dependent on the algorithm, all memory elements flipped by random SEU's can be fixed.

In ECC RAM modules, the algorithm is implemented in hardware, and each time a word (e.g., 64 bits) is accessed, the word is run through an ECC algorithm (e.g., Hamming code) and corrected before use. All that is necessary to scrub memory is to read memory word and write back the result (if not already performed by hardware). ECC memory usually has the capability to correct a single bit of error. Multiple SEU's occurring in the same word will not be properly recovered, so scrubbing very often will help to reduce the chance of permanent memory corruption. While it is possible to get ECC memory in COTS devices, but it is quite uncommon, and usually only in more expensive embedded industrial or military products.

Implementation of software error detection and correction (EDAC) involves the same type of algorithm used in ECC. The difference is that ECC memory is built to store the code word with the actual data. In a software EDAC implementation, the code bits must be of the type where it is simply appended to the original data. That allows the storage of the code bits in another memory space. Although this is entirely a custom addition to COTS components, being able to perform EDAC can greatly extend the life of COTS devices in space. A single bit can make a serious impact every subsequent decision that a device makes.

7.3.2 Multiple Bit Upsets

REIS refers to multiple-bit upsets (MBU) as multiple bits within the same logical word being flipped. Multiple-cell upsets (MCU) are MBU's, but with more than one bit affected across different logical words. Either of these events can occur when many secondary ionizations occur due to a high energy particle. Densely packed SRAM is especially vulnerable to this type of upset [54].

Multiple bit upsets are much more serious than SEU's because this defeats most low computational cost error detection and correction (EDAC) techniques. The minimum EDAC techniques used can only detect and properly correct one or two bits of error per word. If more bits are flipped than the EDAC can correct, the algorithm will make generate an incorrect 'corrected' result.

The tradeoff between number of correctable bits and computational time can lead to a necessary tolerance for code corruption due to MBU's. Thus, it may be necessary to have multiple failover capable copies of critical code which can repair the other damaged copies, and constantly monitor critical regions of code that can bootstrap the failover process. The multiple copies can be across different memory areas within the same storage device.

7.3.3 Single Event Transients (SET)

Single event transients (SET) are caused by a similar mechanism as SEU's, which is charge deposition. Transients appear in random areas of a semiconductor as a pulse of positive or negative current. Transients can even be amplified by transistors if it occurs in, or is transferred to a transistor's control area (e.g., MOSFET gate, BJT base, MOS channel).

In the case of analog circuitry, such as the output stage of an amplifier, the symptoms can include glitches in analog readings, or threshold tripping for protection circuitry among other effects.

In digital circuits, an SET can induce the propagation of a transient straight through combinational logic chains (e.g., combinational logic which comprises a CPU's ALU). If no memory is at the end of the combinational logic, then the transient will reach the final output stage, and be cleared at the end of the transient period. However, if there is some sort of memory, such as a D type flip-flop (common for microcontroller input ports and internal

registers), it is entirely possible for the flip flop to be clocked in during the transient. According to REIS, as long as the transient is able to hold the logic state for at least the setup-and-hold time of the flip-flop, the transient can be properly latched in. Thus, logic with faster response times will be able more readily capture transients.

Factors that influence digital SET effects include device voltages and clock frequency. As device voltages go lower, so do the logic thresholds. Thus, lower voltage devices are more susceptible to low magnitude SET's [54]. In addition, as clock frequency of memory elements go up, so do the number of chances that an improper logic level will be latched.

SET's can also affect optocouplers, which have output transistors. This can cause transient enabling of devices, improper logic states, or isolated control loop interruption.

7.3.4 Single Event Functional Interrupt (SEFI)

Single event functional interrupts (SEFI) are mostly related to reconfigurable digital and mixed signal circuits. Xilinx defines the SEFI as 'the interference of the normal operation of a complex digital circuit', which includes 'failure in support circuitry, and configuration capability' [29]. An example would be an SRAM configuration memory cell within an FPGA which experiences an SEU. The SRAM's controlled logic blocks may no longer serve its function within the larger complex system (e.g., a soft core CPU).

More common to microcontrollers, an SEU in a simple state machine variable (e.g., states 0,1,2,3,4), can cause the state to jump to an arbitrary state, or an invalid state. At best, a catch-all 'default' case will reset the state machine to a safe state. At worst, the execution of arbitrary or normally unreachable code will be executed without exception.

Microcontrollers typically store their volatile configuration and CPU registers in SRAM. Thus, SEFI's will result if a SEU/MBU occurs in configuration and CPU registers. Effects include program counter changes, corrupted calculations, and reconfiguration of peripherals such as clock generation/distribution, communication timing.

SEFI's can also interfere with the operation of digital IC's with state (e.g., memory controllers, motor controllers, real time clocks, etc).

Microprocessors running a full operating system, such as Linux, will have even more individual software states being managed. The microprocessor and support IC's will have

many hardware state machines that can be affected by SEFI's. Thus, large complex software is very vulnerable to SEFI. Due to the amount of processing going on at any given time, and the sheer amount of code to be scrubbed, mitigation for software errors would be best handled by hardware based ECC.

In any case, the configurations should be regularly reconfirmed to ensure that any SEFI's that occur in a flight computer, or controlled devices with programmable states, can be resolved in a timely manner. Multiple copies of registers, and more rigorous multi-bit ECC algorithms can be used to protect critical configurations.

7.4 Destructive Single Event Effects

7.4.1 Single Event Latch-up (SEL)

Single event latch-up (SEL) is specifically an issue with CMOS circuits. CMOS structures readily form parasitic thyristor structures (e.g., N well MOSFET on P+ substrate). This type of parasitic structure is usually present in COTS CMOS analog and digital circuits. SEL describes the behavior where a single charged particle is able to inject charges into the parasitic thyristor's base, resulting in an unintended conduction path between supply rails.

Figure 7.11 shows the latch up path in the CMOS structure. If a high energy particle injects enough holes into the node between r_{sl} and r_{bl}, or electrons into r_{bv}, a self sustaining latch-up condition can result. **Figure 7.12** shows a typical I-V curve of the parasitic thyristor. In order for latch up to be sustained, the power supply must provide sufficient holding current.

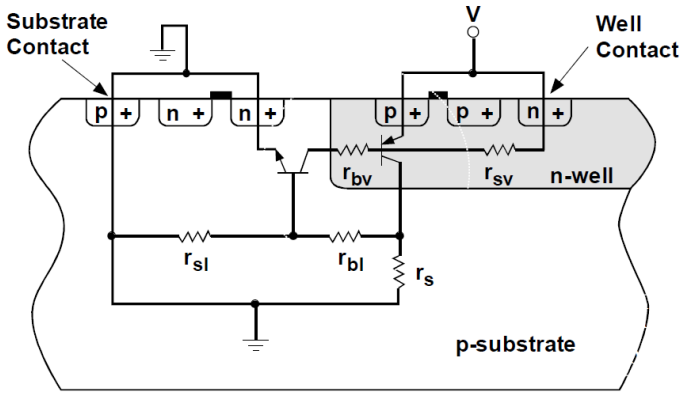


Figure 7.11: Latch-Up Path, Source: JPL [24]

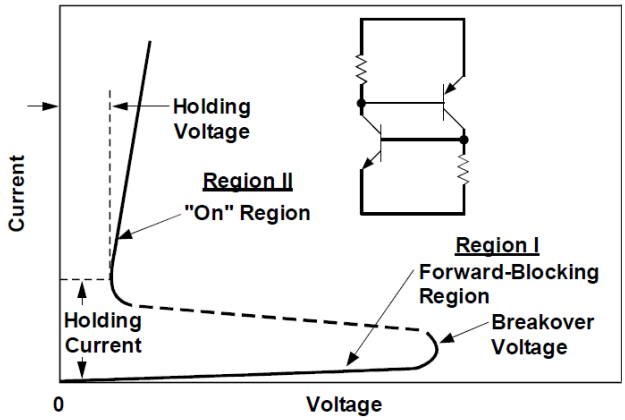


Figure 7.12: Representative Parasitic Thyristor I-V Curve, Source: JPL [24]

Latch-up will have the symptom of increased current consumption of the IC. In severe latch-up, unusually large amounts of current will run through a device. Severe latch-up can be detected and cut off within tens or hundreds of miliseconds by using over current protection circuits. For COTS assemblies, this will likely be done with an external protection circuit. To rapidly cut off the latch up, a low impedance shunt, called a 'crowbar', should be implemented in the OCP. This will rapidly discharge all bypass capacitors directly on the supply lines.

However, at lower levels of current, called 'micro latch-up', the levels may be within normal expected current levels. Micro latch-up may not immediately damage a device, but may cause malfunctions within the device. JPL notes that micro latch-up can prevent bits from being changed until power cycling [24].

Like thyristors, removing voltage from the supply rails will clear the latch-up condition.

Any level of latch-up over a will cause increased instantaneous power consumption, and over time, an elevated device temperature. Detection circuits for latch-up may be set for a threshold which is based on a device's worst case normal operating current. However, without more intelligence than a single threshold, the will be too high to detect micro latch-up. Thus, the condition can go unresolved until the next power cycle. In low power satellites, parasitic power consumption as a result of micro latch-up is especially of concern due to tight power budgets. Regular power cycling of all COTS assemblies is recommended to clear micro-latch conditions.

As a note, there do exist semiconductor processes that will nearly eliminate latch-up. However, since there is rarely visibility into the stack-up of COTS IC's, it is not covered in this study. Further information on several different radiation hardened semiconductor architectures that prevent the initiation of latch-up can be found in LaBel [20], Iniewski [54], and Johnston [83].

7.4.2 Single Hard Error (SHE)

A SHE refers to a permanent deviation or loss in functionality which cannot be reversed. This is mostly associated with memory devices such as RAM or non-volatile storage. As mentioned in the cumulative effects in MOSFET section, a single high energy particle can cause enough damage in a device to cause its threshold voltage to shift drastically. This can result in changes in threshold voltages in memory cells such as flash, or permanently disable a MOSFET in SRAM and DRAM technologies.

7.4.3 Single Event Burnout (SEB)

Latch-up at sufficiently high levels will cause thermal run-away, and consequently destroying the device. Individual power MOSFETs don't have the same thyristor structure as CMOS devices. Instead, MOSFETS in general, have the possibility of having a parasitic BJT structure which can result in the same type of thermal damage.

Shown in **Figure 7.13**, a power HEXFET scenario is shown with its parasitic NPN BJT structure formed between the n epitaxial layer, p body, and n+ terminal. This connects the n+ body, driven to V_{DS}, and a source or drain terminal connected to ground. When a highly energetic particle injects charge into, or near the body of the p channel, this can trigger regenerative currents which result in a fully 'on' BJT structure, conducting current directly between the source and drain [25].

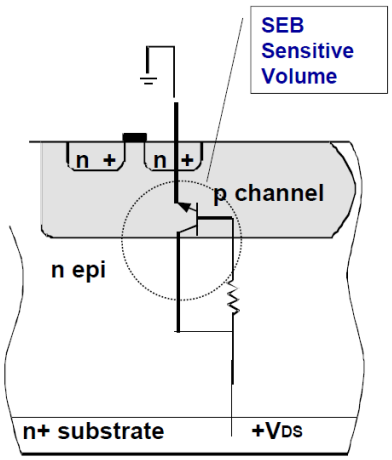


Figure 7.13: Single Event Burnout with Parasitic BJT Exposed, Source: F. Sturesson, ESA [25]

7.4.4 Single Event Gate Rupture (SEGR)

The Single Event Gate Rupture (SEGR) occurs when a gate oxide is ruptured by interaction with a charged particle. JPL notes that gate ruptures occur when there are very thin gate oxides, such as in VLSI devices. Gate ruptures are also a big issue for power devices [24].

The rupture of a gate's oxide could cause unintended conduction paths between a MOSFET's source/drain and gate contact. This happens when a heavy ion traverses the structure from top to bottom, it will directly ionize atoms in its path, and form a conductive plasma in its wake. Shown in **Figure 7.14**, the plasma wake can reach all the way down into a power MOSFET's n+ substrate and cause conduction between the body and gate terminal. Gate oxides typically have lower V_{GS} and V_{GD} breakdown voltages than $V_{DS\ and}$ $V_{BS.}$ Thus, if a high enough supply voltage was being applied to the body versus the gate, the gate oxide can break down and result in the gate rupture.

Secondary effects after a gate rupture can include conduction of high supply voltages to a low voltage gate driver. This includes general purpose outputs on a microcontroller. Having an excessively high voltage routed to a low voltage IC can destroy its output stage, as well as the entire device along with it.

Since SEGR's are caused by high supplied voltages between the body/gate terminals, it would be preferable that the a transistor's V_{GS} tolerance would be capable of handling the worst case body/gate (positive and negative) voltage.

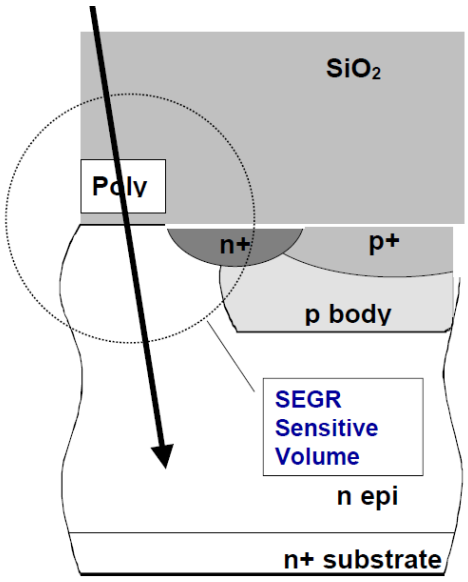


Figure 7.14: Single Event Gate Rupture, Source: F. Sturesson, ESA [25]

However, power MOSFET having V_{GS} tolerances beyond +/-20V are more rare. For higher voltage situations, further work is necessary to investigate the various processes, and determine which types of MOSFETs are less susceptible to SEGR.

7.5 Radiation Models for Spacecraft Design

7.5.1 Radiation Modeling

As mentioned earlier, radiation has been measured to great length over the past few decades As a result, several radiation models were created to help estimate the rate of cumulative dosage and single effect events. These models are essential to a cost effective plan for counteracting radiation effects.

Radiation models begin with a few key parameters. This includes the period of flight, varying altitudes, and varying inclinations. This data is used to drive models of the sun, trapped radiation, and galactic cosmic ray estimates. The resulting radiation spectra and exposure time can be integrated, and then subsequently used with shielding models.

The Space Environmental Information System (SPENVIS), designed by ESA, and operated by the Belgian Institute for Aeronomy, is a web based interface to many of the latest and popular space weather models [75].

7.5.2 Case Study: Small Satellite in 450km Circular Orbit using SPENVIS

In this case study, we have a satellite which may be inserted into a circular orbit with an altitude of 450km. This following case was chosen to be representative of a midrange orbit for a small remote sensing satellite. Simulations were performed for 90 days, 1 year, 2 years, and 3 years. This represents some common desired cases.

Additional orbital parameters include:

- Mission Duration: 90 days baseline (1 year, 2 year, 3 year for TID w/ Shielding)
- Altitude: 450km
- Inclination: 97.6 degrees
- RAAN: 71.6186 degrees
- Representative Orbits: 16

By using SPENVIS to generate spacecraft coordinates, we get the following plot of altitude and inclination.

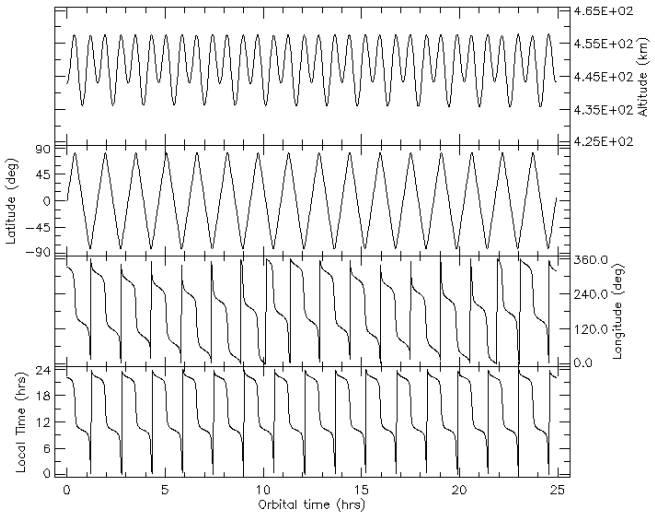


Figure 7.15: SPENVIS Generated Spacecraft Trajectory

Taking the spacecraft trajectory, we then run the AP-8 and AE-8 models for estimated proton and electron fluxes respectively. Plotting the AP-8 and AE-8 radiation exposure over 100keV versus latitude/longitude results in the following plots. From these plots, we see that the high energy proton flux occurs mainly around the SAA, and high energy electron flux occurs along the Earth's magnetic field. SEE's are more likely to occur in these regions.

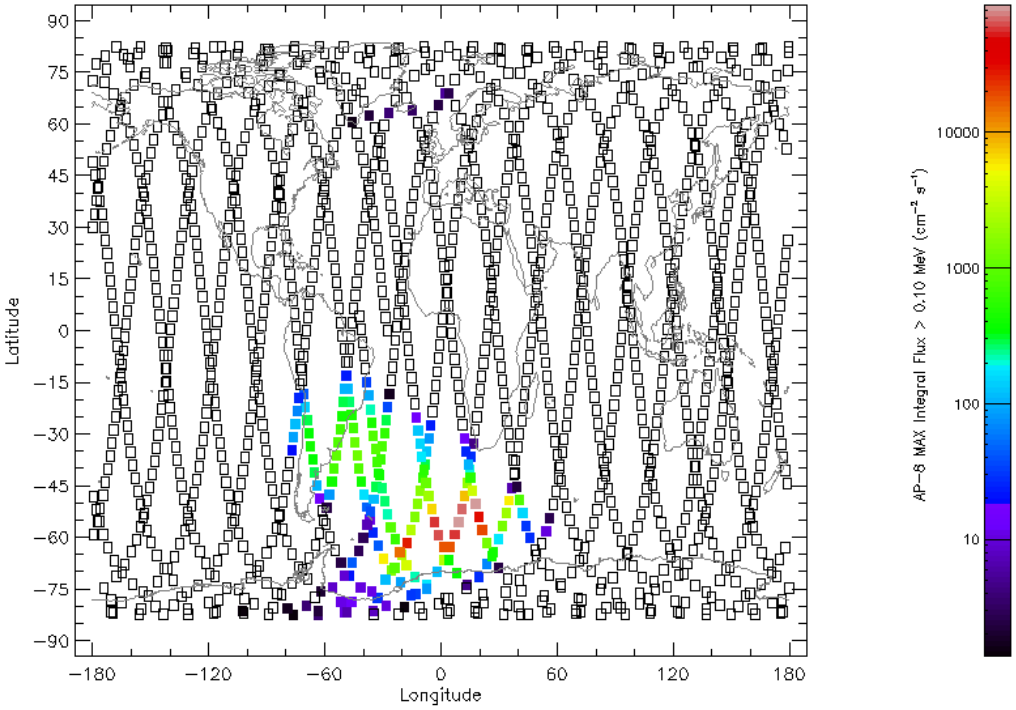


Figure 7.16: SPENVIS Generated Map of Trapped Proton Flux

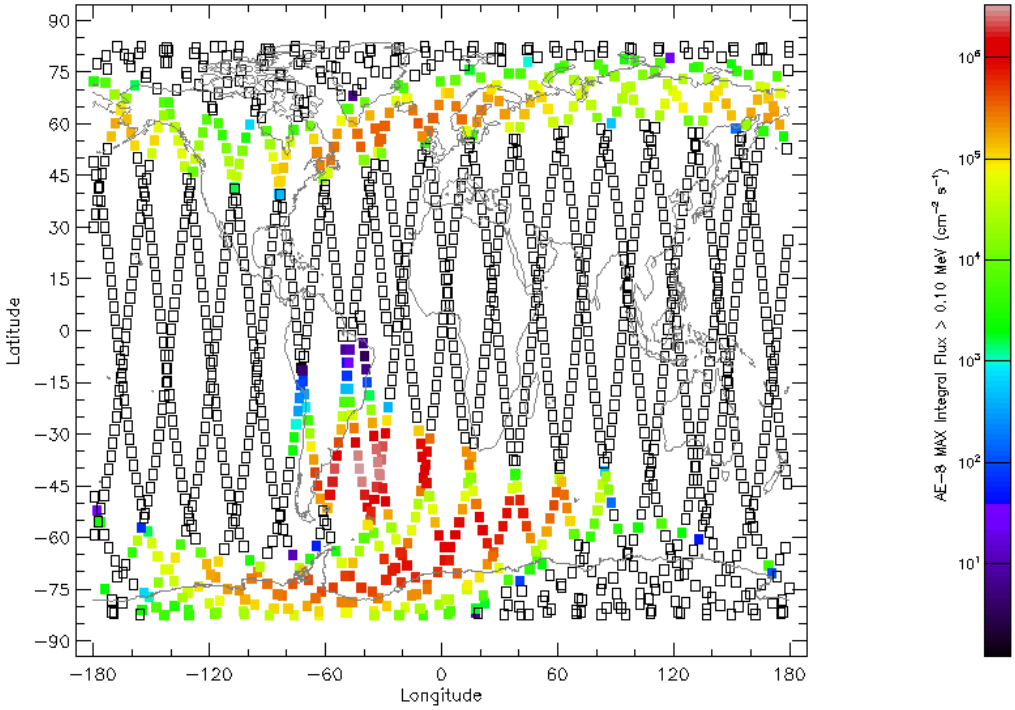


Figure 7.17: SPENVIS Generated Map of Trapped Electron Flux

The electron flux map resembles the following figure which shows the trajectory of trapped particles. When the particles reach a mirror point, they get reflected in the opposite direction along its magnetic field line. Knowing where SEE's are more likely to occur can assist in planning mission operations.

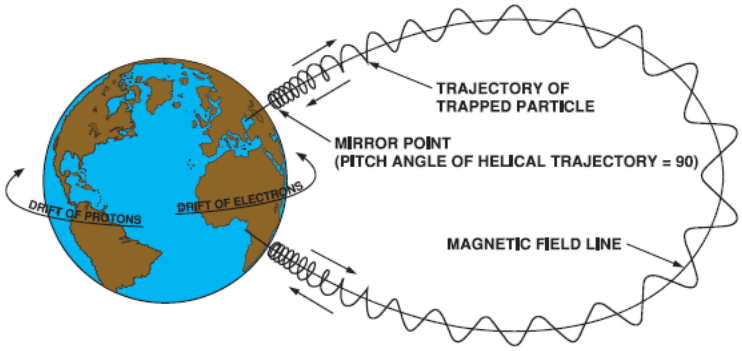


Figure 7.18: Trapped Particle Trajectories, Source: SNL [28]

Next, we take a look at total ionizing dose. As mentioned earlier, simulations were run for 90 days, 1 year, 2 years, and 3 years. This will provide an idea of what the trapped radiation environment looks like in a 450km circular orbit. In addition, we compare the effects of radiation on silicon, versus gallium arsenide.

SPENVIS provides the SHIELDDOSE-2 model, which has several modes of operation. The model has parameters for the shielding material, thickness, and an inner target material. For most radiation dosage calculations, silicon is the target material. The radiation spectra an intensity data comes from the AP-8 and AE-8 results in the previous step. For this case study, aluminum was chosen for the shielding material because of its light weight and versatile properties for avionics structures. Shown in **Figure 7.19**, the model utilizes a uniform shell thickness, and radiation impinges on the target device from any direction.

To provide a better idea of what shielding does to protect against electrons and protons, the next two graphs show the effectiveness of varying aluminum thicknesses in reducing the radiation dosage. Note the different sources of radiation are affected in varying degrees by the shielding.

In both the 90 day and 1 year cases (shown in **Figure 7.20** and **Figure 7.21**), we see that increasing amounts of shielding thickness reduces all the trapped radiation effects. At the higher end of increasing shielding thickness, electrons have the sharpest decline in dosage. Protons starts to plateau in decreased TID contribution as shielding thickness increases.

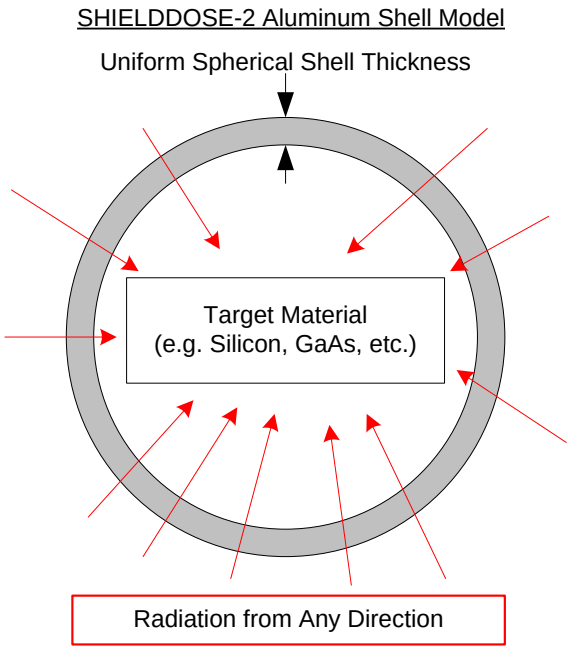


Figure 7.19: SHIELDDOSE-2 Spherical Model, Illustration for Aluminum Shell

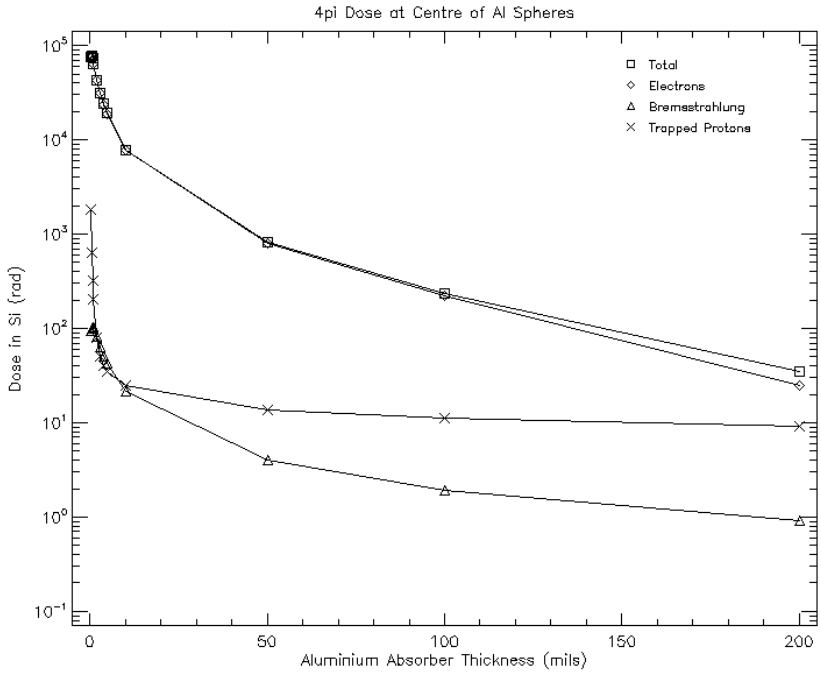


Figure 7.20: Radiation dosage at 450km 98 degree inclination orbit for 90 days, based on NIST SHIELDDOSE-2 model from SPENVIS

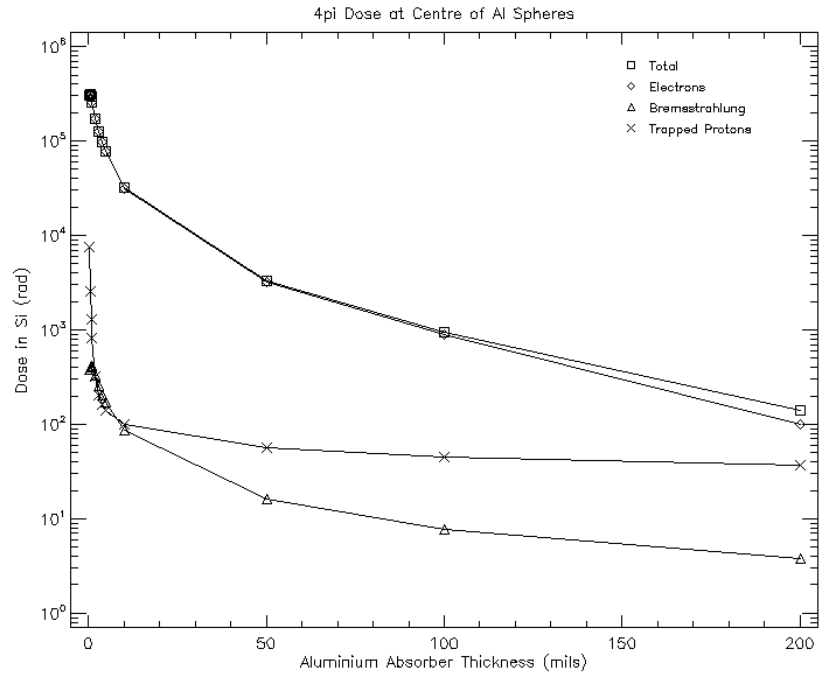


Figure 7.21: Radiation dosage at 450km 98 degree inclination orbit for 1 year, based on NIST SHIELDDOSE-2 model from SPENVIS

Note that there is a category of TID dosage called Bremsstrahlung. Bremsstrahlung radiation is comprised of secondary X-ray particles which are produced as a result of electrons decelerating through shielding. Shielding thickness affects the amount of X-rays which ultimately make it to the target device.

Next, we compare the radiation dosage over time for a 3 month to 3 year mission. The below graph shows that for longer mission durations, a greater amount of shielding is necessary. Take for instance a 1 year mission. In order to stay between 2-5krad of exposure, about 50-70 mils of shielding is necessary.

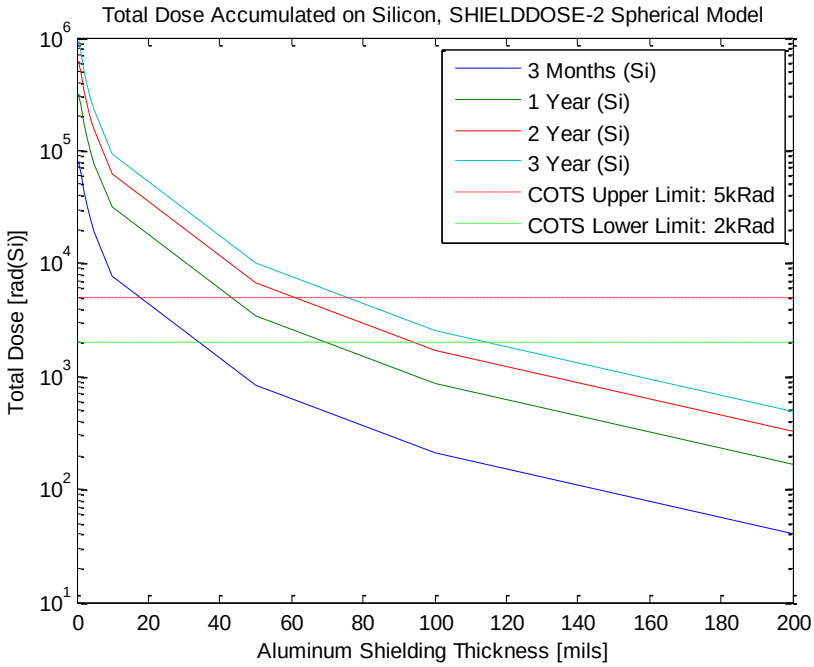


Figure 7.22: Comparison of TID over 3 Month to 3 Year Mission Durations

Radiation design factor (RDF) for shielding, as discussed in NASA APR 8070.2, general shielding for TID can use an RDF of 2. In specific cases where additional protection is needed, an RDF of 3 is required. RDF is calculated with the following formula:

$$\text{RDF} = \frac{\text{Radiation-resisting capability of a part or component in a given application}}{\text{Radiation environment present at the location of the part or component}}$$

Figure 7.23: Radiation Design Factor (RDF), Source: NASA APR 8070.2 [33]

If we go with the upper 5krad COTS exposure limit, that would be our chosen radiation-resisting capability. Over 1 year with 70 mils of aluminum shielding, we get approximately 2krad of dosage at the device. That gives us a RDF of 5krad/2krad = 2.5. If we didn't have to account for other additive sources of TID, 70 mils of shielding would be more than enough for general shielding.

Another interesting comparison is TID between materials for the same duration. From highest to lowest radiation dosage: SiO_2, silicon, and gallium arsenide. SiO2 in MOSFET gates is where ionization appears to have a higher chance inducing trapped charges, versus ionization in bulk silicon. Thus, for a more pessimistic RDF, SiO_2 can be used instead.

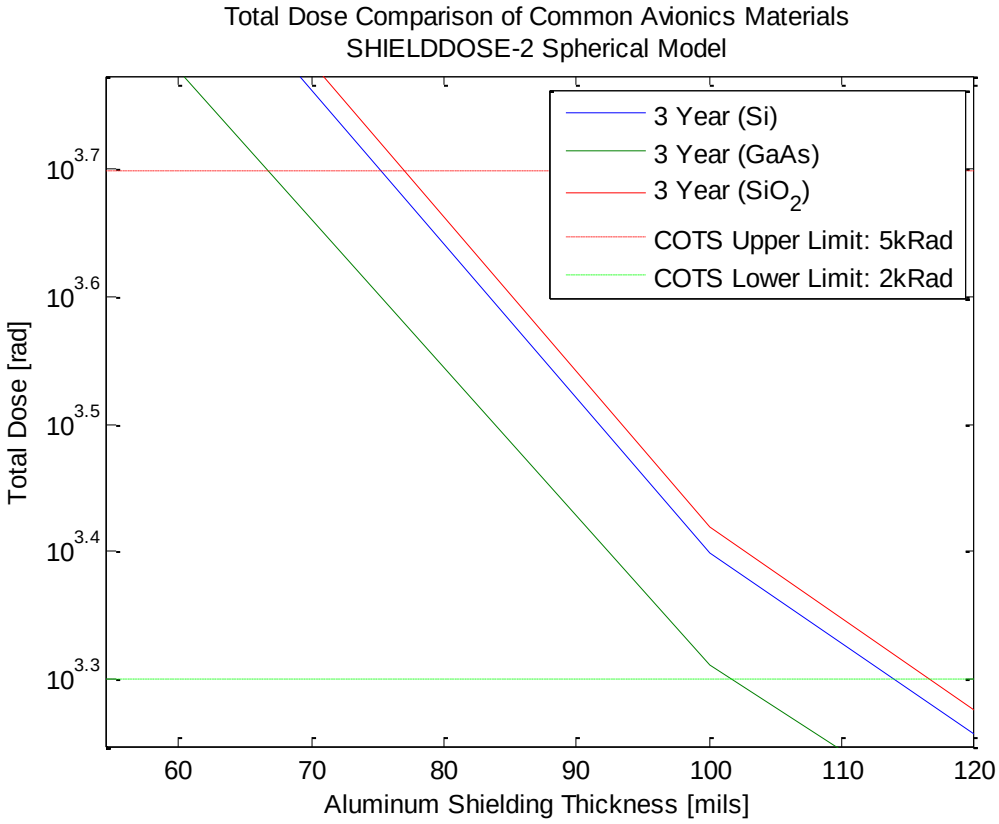


Figure 7.24: Comparison of TID for Common Avionics Materials

Sandia National Laboratories notes that trapped electron and proton fluxes are highly dynamic compared to the AP8 and AE8 models. They also go on to say that the models may severely underestimate the concentration of protons an electrons, but this discrepancy is most severe in higher orbits beyond LEO [28].

Aside from just trapped radiation, other sources of TID and SEE's include GCR's, solar cycle influenced GCR flux, and solar flares. Many other plots are available on SPENVIS to help analyze these phenomena, including spectra of trapped proton and electron flux. All of these models are can be quite complex and specific to each case. Thus, further analysis is best left for specific cases in future work.

7.5.3 Typical Component TID Exposure Limits

JPL's Radiation Effects Group has an excellent course presentation on space radiation effects [24]. The presentation shows typical device failure levels for TID, shown in **Table 7-1**.

Table 7-1: Typical Total Dose Failure Levels of Various Technologies

Technology	Failure Level [Krad(Si)]
Linear IC's	2-50
Mixed-Signal IC's	2-30
Flash Memory	5-15
DRAM	15-50
Microprocessors	15-70

Source: JPL Radiation Effects Group [24]

Small spacecraft typically have at least linear, mixed signal, and flash memory containing IC's. Thus, components on-board a typical COTS based spacecraft will 'typically' be able to sustain about 2-15Krad of TID. The SECE book describes 5krad(Si) as a reasonable design limit for COTS devices. Thus, the range of 2-5krad was used in the previous analysis for the TID limits.

Regardless of rules of thumb however, you can assume that devices will be high risk until they have been tested either in space, or through radiation screening. An unproven device designed without regard for radiation carries the risk of failing at any time. As much as possible, COTS parts which have flown in space before, and have a good track record, should be preferred.

Once in space, radiation exposure will happen, and SEE's will happen. The question is when, and which type of SEE occurs. In the worst case, an SEL can burn out a critical region of a satellite's avionics right after deployment.

7.6 Summary

Radiation effects on satellites, and their implications on COTS avionics can be quite serious. A number of issues were discussed regarding short term and cumulative effects of radiation.

However, using COTS devices usually means that the design is for the most part, fixed. Without heavily modifying (and potentially damaging) a part, COTS imposes serious limitations on the types of mitigations that can be used for radiation risks. Limited part replacements can be done to help with certain issues, but most of the mitigations will be external (which entails custom hardware designs) or be implemented in custom software.

Thus, because both the need for COTS and the risks of radiation in COTS are high, this is one area of research that will require much more future work.

A helpful guide for performing a full radiation assessment is ECSS's ECSS-E-HB-10-12A 'Calculation Of Radiation And Its Effects And Margin Policy Handbook' [83]. The handbook includes all the various issues discussed here, and covers additional radiation effect mitigation techniques.

Chapter 8: Outgassing

On Earth, outgassing can be found all around us. When you smell adhesives, paints, or anything else for that matter, the scent is made up of are volatile chemicals and material which has made it to your senses.

The rate at which gasses are expelled is closely related to a material's temperature dependent vapor pressure. Vapor pressure can be determined by putting a solid or a liquid into a container, and sealing it in (can include a vacuum for low vapor pressures). Solids can sublimate, and liquids can vaporize. After a long period of time, the container will have an equilibrium pressure at a certain pressure, which is referred to as the vapor pressure. Higher temperatures result in higher vapor pressures.

Volatile organic compounds (VOC) are materials which have especially high vapor pressures. For VOC's, the main difference between outgassing in space versus outgassing on the ground is the much higher pressure differential between its vacuum environment and the high vapor pressure. The larger the differential, the faster VOC's will vaporize.

Almost all of a small satellite is manufactured under one atmosphere of pressure. Under this pressure, materials such as plastic can absorb gasses and moisture. Preparation of raw materials can mean the addition of VOC's such as soldering flux solvents. And during manufacturing, additional foreign material, which can outgas, may become entrapped in bulk material. Finally, when the product is exposed to vacuum, the absorbed materials are extracted, and unconstrained VOC's flash off.

In space, high vacuum and zero gravity enables outgassed materials to drift in all directions. The material can then be electro-statically attracted to surfaces, and condense on relatively cool surfaces. More seriously, material can attach to optical surfaces, or can even coat and degrade surfaces specifically designed for radiative heat transfer. In both cases, the function of the part is degraded, and the entire mission could be compromised. A large amount of material at any outgassing rate can still mean a significant amount of outgassing.

Another important issue for outgassing is the mechanical and electrical integrity of the material. A material which loses too much of its mass will not have the same material properties anywhere near its baseline. One example of where this would matter is when using

high voltage power supplies. If wire insulation outgases and cracks, arcing can readily occur to the nearest conductor. Minimizing outgassing in spacecraft materials is important to have a predictable design.

8.1 Where Outgassing Matters

Satellites flying on a shared launch vehicle as a secondary payload may be required to use low outgassing materials to minimize contamination to the primary payload. If requiring the use of low outgassing materials is optional, the risk of outgassing to the overall mission should be assessed. This includes a review of how you intend to fulfill the success criteria of the mission, and what that means for outgassing. A very short 24-hour duration mission with no optics will have a much smaller need for outgassing mitigation than a multi-year optical remote sensing mission. After the risk has been assessed, determine what mission critical parts of the satellite could possibly be degraded or destroyed by outgassing.

Outgassing is most likely to occur in plastics, foam, coatings (e.g., paint, conformal coating), lubricants, adhesives, encapsulants, and casting/potting materials. Due to impurities, outgassing may still occur from glass and metals. However, based on the focus of NASA outgassing tests [8], non-metal and non-glass materials seem to have the most potential for outgassing. Outgassing rates will also vary between different materials and formulations.

One of HSFL's main focuses is on scientific optical remote sensing missions. The investment in each of its larger multi-million dollar remote sensing microsatellites comes with the design requirement for at least one year of operation. Further use of the satellite is desired until the satellite either de-orbits. Over this span of time, even a microsatellite made entirely of low outgassing materials may still outgas a sufficient quantity of material to degrade functionality. For these satellites, the main vulnerabilities include the remote sensing instrument optics and solar panel optics. In this case, the solar panels were built with a good amount of power margin at end of life, and the satellite could be operated differently if there was ever a severe drop in power generation. However, the remote sensing instrument optics could fail to provide science data if inbound photons are attenuated and scattered due to outgas material condensation. Thus, the most attention must be paid to minimizing the outgassing which could make its way to the instrument's optics.

Next, we take a look at the likeliest threats. This considers the entire chain from outgas generation, transport, and attachment to surfaces. In space, all the materials will be subject to the same vacuum. However, not all materials will be at the same temperature. The main areas you would find higher temperatures include sun exposed surfaces, and high power consumption devices (e.g., high power amplifiers, microprocessors, and high power instruments). That means that you'll get different outgassing rates for the same materials across the satellite.

On the other hand, take for instance a minimally vented high power amplifier which is not near any optics. If all its possible outgassing materials are contained within its chassis, any condensable material would stick to the coldest walls, and exit through its small vent port. If the small vent port is also cold, or vents out onto a cold surface, condensable material can readily condensate without spreading a large quantity of material throughout the spacecraft. Thus, threat of outgassing materials could be reduced by strategic venting and placement.

8.2 Outgassing Tests for Materials

NASA's Goddard Space Flight Center (GSFC) runs an outgassing test program specifically for aiding spacecraft material selection. The original measurement method [8] used 100 to 300mg of material samples which were placed into a aluminum foil boat. The boat was then placed into a copper chamber with a single vent hole. Located just 0.5 inches out from the vent hole, a chromium plated disk was kept at room temperature (25°C). The chamber was then put into vacuum and brought up to 125°C. This bake-out lasts for 24 hours. Any volatiles which vaporize, and could condensate on a 25°C surface, would end up attached to the chromium plated disk.

This test measures two things: First, any mass loss from the sample material was compared against the original mass to find the total mass loss percentage, or TML. Secondly, any added mass to the chromium plated disk was compared against the original sample mass. That determines the percentage of collected volatile condensed material, or CVCM. The benchmark for a low outgassing materials is as follows:

Table 8-1: NASA Low Outgassing Material Criteria

Outgassing Test Metric	NASA Low Outgassing Criteria
Total Mass Loss (TML)	Less than 1.0%

Collected Volatile Condensable Material (CVCM)	Less than 0.1%

Their testing needs have since been adopted by ASTM International, and standardized in ASTM E595 [7]. These tests are highly labor intensive and require expensive measurement equipment. Each material considered for flight should be checked against NASA GSFC outgassing data [8]. The major caveat however, is that manufacturers change their formulations over time. Thus, outgassing characteristics will likely differ between batches of chemicals or product lots. Materials which have no outgassing data should not be preferred for use in flight, and be put through a vacuum bakeout (discussed later in this chapter) before integration into a contamination sensitive satellite.

8.3 Outgassing from COTS Products

In low-cost spacecraft missions, the entire spacecraft could be made entirely of terrestrial type COTS. The most likely culprits for outgassing will be insulation/seals for connectors, liquid containing vessels such as electrolytic capacitors, plastic packaging for IC's, adhesives, and any coatings/paints in the assemblies. A threat assessment should be done to determine what kind of outgas mitigation should be taken for each COTS product.

JPL has compiled an excellent report on outgassing from materials used in plastic chip packages [69]. The guide is geared toward the usage of plastic packaged microcircuits when the product is not guaranteed to work in space, and is a good reference for assessing risk when using COTS products where nearly all IC's are packaged in plastic. And as mentioned in the launch environment chapter, moisture absorption by plastic packaging can outgas when the satellite reaches vacuum.

Popular COTS materials, like Polyvinyl Chloride (PVC) insulation can sublimate and significantly contribute to outgassing. PVC's low cost, electrical insulation, and versatility makes it a popular material for a wide variety of consumer and industrial products. For electronics, PVC can be found on nearly every commercial grade wire and cable. If outgassing is an issue for the mission, then nearly all standard terrestrial electronics cabling systems must be replaced on COTS assemblies.

Another mitigation is to require conformal coating on all avionics boards. Conformal coating does not form a pressure vessel, so outgassing will still occur. But, the coating does provide a

measure of mitigation by restricting the directions that gasses can travel. The coating also provides an elongated path for gas to travel up against the circuit board, and thus increases the chances for condensation on the same assembly.

8.4 Multi-Part Liquid Products

Aside from the risk of manufacturers changing base formulas of resins and curing agents, special care must be taken to observe the mixing and cure schedules. This must be examined both on the manufacturer's datasheet and the source of outgas test results.

The testing done at GSFC includes experimental batches which vary mix ratios to determine its effect on outgassing. However, no mechanical or electrical data was published for the experimental mixtures. So, if an experimental mix ratio or alternate cure schedule was used to attain a low outgassing property, the manufacturer's data sheet may no longer be completely valid. That means you either have a new technical risk, or will need to do your own testing to ensure that the experimental product is sufficient for the intended application.

The preferred route however, is to find a complete set of products which are all low outgassing, and are meant for space. These products are engineered to minimize solvents and other volatiles to minimize the amount of entrapped volatiles. From an outgassing and mass loss standpoint, the result is a superior material integrity under long term space exposure.

Manufacturers, such as Nusil Silicone Technology, are providing low-outgassing 'controlled volatility' products which are tested with ASTM-E-595. Nusil in particular even offers material test services to determine any outgassing, mechanical, or electrical property. The testing can be done on a per-lot basis to increase confidence in a particular batch of product.

8.5 Preferred Spacecraft Materials

Metal and glass appear to have the least outgassing issues. The following preferred materials list will specify mostly non-metals which are likely to have low outgassing, or near low outgassing properties per ASTM-E-595 type testing. More materials can be found in the GSFC database [8]. These basic materials have generally produce low-outgassing results. However, a check on the GSFC database would be advisable, as preparation, mix ratio, or cure schedule affect outgassing. This list is by no means complete, but is intended to be expanded in future work.

Table 8-2: Preferred Basic Spacecraft Materials

Product Name(s)	Uses
Dupont Tefzel ETFE Crosslinked ETFE	Cable and Wire Insulation, Cable Ties
Dupont Teflon PTFE FEP	Cable and Wire Insulation
Glass Filled Liquid Crystal Polymers (LCP) Ticonia Vectra Series LCP	Connector Insulation and Connector Housings
Glass Filled UL94 Thermoplastic	Connector Insulation and Connector Housings Note: Not all glass filled thermoplastics are low outgassing
Poly Phenylene Sulfide (PPS) Techtron PPS	Connector Insulation and Connector Housings
Kynar	Wire Insulation, Shrink Tubing
Polyolefin	Shrink Tubing
Dupont Kapton (Polyimide)	Tape
Dupont Nylon (Polyamide)	Electrically Insulating Nut/Bolts/Washers Note: Be very careful with this material, not all nylon products are low outgassing
Silicone	Adhesives, O-Rings, Connector Insulation, Interfacial Seals, Potting, Casting, Encapsulants, Heat Transfer Pads, EMI Gaskets (Metallized Silicone) Note: There are a lot of different silicone formulations. Some will have unacceptable outgassing.
Urethane	Adhesives, O-Rings, Connector Insulation, Interfacial Seals, Potting, Casting, Encapsulants
Parylene	Conformal Coating

Table 8-2 (Continued): Preferred Basic Spacecraft Materials

Circuit/RF Laminates FR4 G10 Nelco N-105 Nelco N-4105 Rogers/Duroid 5870 Rogers/Duroid 6010	Microwave and Standard Printed Circuit Board Substrates
Brady B-342 Brady B-361	Printable Shrink Wrap Labels, Adhesive Backed Labels
Copper Tape Aluminum Tape Aluminum Foil	Lightweight Shielding, Spot EMI Control Note: Food grade aluminum foils can be coated with peanut oil. This must be thoroughly cleaned off before use. Food grade foil should not be used for spacecraft material

8.6 Vacuum Bakeout of Flight Assemblies

There is a significant difference between zero and low outgassing. It is not practical to use only absolute zero outgassing materials, largely because they are rare for non-metal/non-glass materials. In addition, routine handling of parts also adds contaminants which could outgas. The more quantities of outgassing material you have in a spacecraft, the more significant a tenth of a percentage point of CVCM becomes. While it may not be practical to eliminate all outgassing, a thermal vacuum bakeout can be used to reduce outgassing to an acceptable rate.

As phrased in NASA MSFC-SPEC-1238, the "Thermal Vacuum Bakeout Specification" is to "provide the methodology to achieve an acceptable level of molecular outgassing," and "the verification that these levels have been achieved" [10]. Performing the action of baking out an assembly is just as important as being able to tell when it is done. Per the specification, outgassing rates can be measured by using a temperature controlled quartz microbalance (TQCM). The procedure could take a full week or more of continuous operation, ending only when outgassing rates are below a low threshold for 36 hours.

One important parameter which will limit batch processing is the temperatures of bakeouts. It is important to consider the expected thermal environment of each spacecraft part in space. If

a component will be constantly running cold throughout the mission, a bakeout will not need to be as hot as a part that has temperature cycles beyond 100°C. Since a bakeout is performed over days, all components of bakeout batch will be driven to the bakeout temperature. Nearly every part for a spacecraft has a temperature specification for survivability, so care must be taken to not over-stress components beyond their specifications.

With these two considerations in mind, the goal remains to bake out all devices at a higher temperature than they will actually experience on orbit. In this way, the worst case on-orbit outgassing rates will be lower than the baked-out rates. And thus, you will have margin for compliance with all outgassing requirements. In the case of MSFC-SPEC-1238 [10], the bakeout should be "at least 10°C above its in-flight operating extreme".

It is important to note that any post-process contamination can quickly nullify the benefits. Thus, a clean room is very important, and handling/storage must be done in a manner which will maintain cleanliness for flight.

Chapter 9: Metallic Whiskers

Over time, certain metals may develop metallic whiskers in the micrometer to millimeter range of lengths. This issue is very commonly found on metals such as tin, cadmium, and zinc. Other metals can also whisker, but the aforementioned metals are the most notorious for whiskering in space applications. Thus, in their pure form, these metals are hereby referred to as the 'forbidden metals'. Metal whiskers can develop at any time, and can be very difficult to visually spot. Whiskers can grow on Earth, and in space, making unintentional circuit connections that could lead to catastrophic failures. Thus, for any long-term storage, or missions requiring any minimum period of performance, it is imperative to understand the risks of using materials which have the risk of whiskering.

According to research done by NASA [11], materials such as Zinc, Cadmium, and Tin are especially prone extrude microscopic whiskers. Other metals, which include gold and silver, have also been seen to extrude whiskers. The whiskers can cause unintentional circuit paths, break off, block optics, and interfere with MEMS devices. The problem exists even with terrestrial systems, but they are typically much less expensive to repair than satellites. NASA has compiled a list of the numerous 'publicly reported' cases where metallic whiskers resulted in the failure of military, communications, and remote sensing satellites [12]. The amount of money invested in the satellites lost to whiskers is quite alarming.

Table 9-1: Pictures of metal whiskers

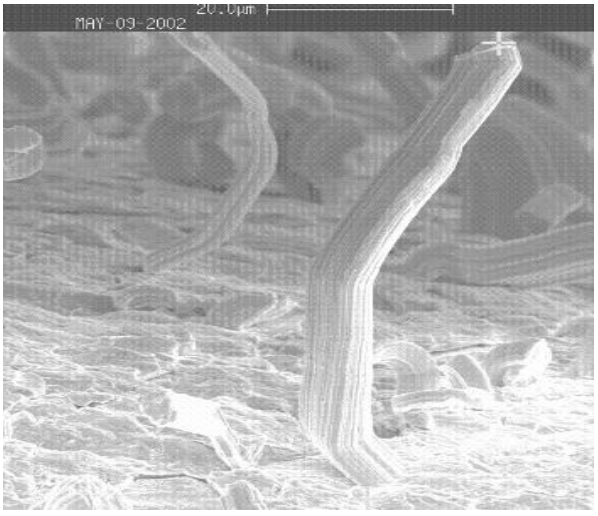


Figure 9.1: Tin whiskers, Courtesy of NASA

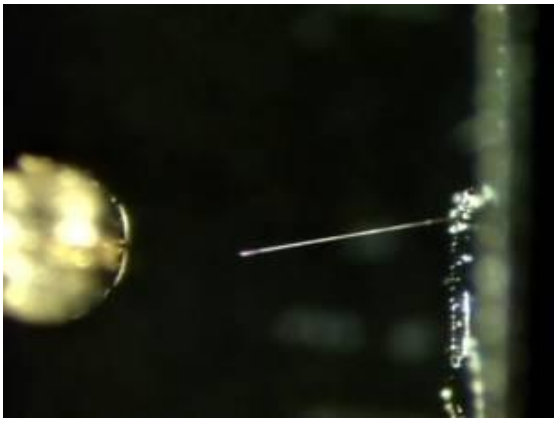


Figure 9.3: Tin whisker on a D-Sub connector shell which is growing toward a connector pin, Courtesy of NASA

Figure 9.2: Zinc whiskers on a hot dip galvanized steel pipe, Courtesy of NASA

Figure 9.4: Damage to a relay caused by a tin whisker and secondary metal vapor arc, Courtesy of NASA

We can find a material like tin and zinc inside just about every COTS electronic assembly, and especially in their pure form on connector shell platings, with tin also being on connector contacts. So if materials like zinc and tin are such a problem, why are they so commonly used in electronics? Take for instance electrical contacts, the low cost versions will commonly have copper or copper alloy cores with a tin finish. Copper by itself has a conductivity of about 6.5 times that of tin [56], so it may seem counterproductive to use. But under ambient conditions on Earth, bare copper will easily oxidize in the presence of moisture, developing a high resistivity surface. If bare copper is used for contacts, high contact resistances will develop over time. Thus, to produce a higher reliability contact with the high conductivity of copper, a conductive anti-oxidation surface conversion or plating is needed. This is where metal finishes like tin and zinc come into play. They provide a sacrificial layer which limit their oxidation, while protecting the more valuable and higher conductivity metals.

According to Molex, tin is very stable in the presence of moisture and oxygen, forming only a thin layer of oxidation over it. For connectors, tin contact surfaces are 'wiped' upon mating to scratch off the thin oxidation layer for direct tin to tin contact. For power connectors at >1A, the current will 'burn off' any remaining oxidation in the conduction path which further decreases contact resistance [55]. Note: For currents lower than 1A, Molex recommends gold plating, since lower currents cannot reliably 'burn off' the layer of oxidized tin.

In the case of printed circuit boards, many different finishes, including lead-free solder or immersion tin, can be used for finishing to protect copper traces from oxidation [57]. Immersion tin is highly compatible with both leaded (e.g., Sn63/Pb37) and lead-free (e.g., SAC 305: Sn96.5/Ag3/Cu0.5) soldering processes, whereas lead-free solder finishing is designed specifically for lead free processes.

Other finishes like silver and gold will dissolve into, and alloy with leaded solders. This alters their mechanical properties somewhat, but gold is especially known for an effect called gold embrittlement. This effect makes the solder joint much more prone to cracking [19].

Thus, due to the high content of tin in solders, tin finishing remains one of the most solder compatible finishes for circuit board traces. But at the same time, any traces which are not soldered to (e.g., vias, unused pads, etc.), will remain exposed, and will allow very long tin whiskers to grow [11].

According to NASA advisory NA-044 [13], pure tin is the most prone to whiskering. Alloying tin with other metals in significant quantities, namely lead, can reduce or eliminate whiskering. Alloys between tin and lead (at least 3% lead by weight) are acceptable for space flight use. Additional lead content can be added to pure tin by hot Sn/Pb solder dipping or manual solder rinsing.

The Center for Advanced Life Cycle (CALCE) has compiled a document which discusses the mitigation of tin whiskers [15]. The most notable categories of mitigations for pure tin surfaces include pure tin avoidance, stripping/replating, reflowing, annealing, and using conformal coating on exposed tin surfaces.

All of these processes are labor intensive, and carry their own risks of damage to parts, especially when other low melting temperature materials are attached to them (e.g., thermoplastics, epoxies, etc.). The most practical approach appears to be avoiding pure tin plating, tinning pure tin surfaces with Sn/Pb solder, and using an adequately thick layer of conformal coating [11].

After reviewing different COTS products in the course of this study, **Table 9-2** shows types of products are likely contain a pure form of a forbidden metal, or a form of the forbidden metal which does not contain any content of lead.

Table 9-2: Compilation of Products Which Include Unleaded Zinc, Cadmium, and Tin

Tin	Lead-Free Solder, Relays, Transistor Cans, Connector Shell Platings, Wire Plating, Fastener Plating, Finishes for RoHS electronic components (e.g., passives, IC's, etc.)
Cadmium	Weatherized/Ruggedized Connector Shell Platings
Zinc	Nuts, Bolts, Washers, Spacers, Connector Shell Platings

9.1 Electrical Effects

NASA [11] has documented metallic whiskers which ranged from 1-10mm in length, and up to 10μm in thickness. Throughout the course of this study, the longest tin whiskers appear to protrude from pure tin finishes on arbitrary surfaces. At these lengths, whiskers can easily bridge electrical contacts.

As mentioned earlier, the primary mechanism in where an undesired effect results is where a metallic whisker shorts two conductors. In addition, research at NASA GSFC has shown that whiskers have been shown to be electrostatically attracted between two conductors [71], and thus is a risk to high voltage or fine pitch circuits.

In cases of low current circuits, a whisker may permanently form a shunt between two conductors. This can disable sensors, high impedance feedback loops, and other low current electrical interfaces. Quantifying 'low current' is subject to the thickness, length, and material of the whisker. The NASA presentation provides a formula to calculate the threshold of melting [11]. As long as the current run through the whisker is lower than the threshold of melting, the short will remain in place. A current at, or slightly higher than the whisker will result in a melting behavior similar to a fuse.

If the electrical connection of a whisker causes a significant amount of current to flow between conductors, such as shorting a power supply or battery pack, the violent surge of energy can vaporize the whisker [11]. The metallic vapors can then facilitate arc initiation between nearby conductors at different potentials [59]. The arc in turn can form a highly conductive plasma, which will then result in an extremely low impedance path. The low impedance plasma could cause an extremely high current short which can damage everything

in the short circuit path. And finally, the arc can also violently eject material, which can cause even more damage.

The primary and secondary modes of avionics failure due to metallic whiskers is a threat to mission success for all spacecraft. Thus, the three metals in their pure form, Zinc, Cadmium, and Tin are forbidden from space use. There are some limited exceptions, but they all involve mitigation of their whiskers.

9.2 Electronic Solders

Lead-free solders, known to grow metal whiskers, can be found in nearly all consumer/industrial COTS parts manufactured since the 'Restriction of Hazardous Substances' (RoHS) directives were implemented by the European Union (EU). While the United States has not adopted this on a federal level, each state has the option of adopting similar directives. California is one of the first states to enact a very similar policy called the Electronic Waste Recycling Act of 2003 (EWRA). Both of these policies forbid lead from use in electronics. Thus, COTS products marketed for sales in those markets, will be using some sort of lead-free solder.

Lead free solders typically involve mixtures of >90% tin, silver, and copper. In SAC305 and SAC405 lead-free solders, Snugovsky [85] notes that the solders grow whiskers of 10-140μm lengths with thicknesses of around 1.5-2μm.

The only exceptions to the above policies are for high reliability electronics such as aerospace (which includes satellites), medical, or military use. Ultimately to avoid tin whisker issues, the preferred solder alloys for general satellite work are leaded. The most general purpose alloy accepted by NASA and ESA is the eutectic alloy Sn63/Pb37. The eutectic nature allows the solder to rapidly transition between a liquid and solid. This is as opposed to Sn60/Pb40 solders which go through a plastic stage during cooling, and can become prone to cracking if moved in the brief time it's in the plastic state.

However, tin/lead solders will aggressively dissolve silver. High quality spacecraft/military wire and solar cell contacts may have silver plating. To prevent the silver plating and solar cell contacts from dissolving into the Sn/Pb alloy, Sn62/Pb36/Ag2 is used exclusively for solder joints which join at least one silver surface.

Leaded Sn/Pb solders will also dissolve gold finishes, and results in a weak and dull solder joint. This is called 'gold embrittlement'. More details, including SEM images can be found in a paper written by SEM Lab, Inc. entitled 'Gold Embrittlement of Solder Joints' [19]. Gold plating can commonly be found on high reliability component finishes, microwave components, RF connectors, and is an option for printed circuit board finishes. For PCB's, both NASA and ESA require that gold plated surfaces intended for soldering shall be 'de-golded' [17][18]. The de-golding process starts by stripping the gold plating off of contacts with a bath in a hot SnPb solder pot. Then, all the contacts are tinned in a non-contaminated SnPb bath.

Gold plated solder cups can be individually rinsed with SnPb solder, a soldering iron, and solder braid. Individual de-golding of solder cups is the only way to prevent air entrapment in solder cups, which will result in residual gold.

Many RF applications use gold plating for connectors and RF IC lead finishes. This can either be handled in the same de-golding procedure, or the direct use of Indium-Lead solder (e.g., In70/Pb30).

9.3 Mitigation by Prohibition

For COTS electronics, you will likely be stuck with forbidden metal alloys in solder, or lead-free platings. In other components such as connectors, forbidden metal avoidance can be one of the least costliest and least risk routes of mitigation.

Alternatively, stripping platings like tin, and re-plating with another material is a potentially costly process which may require hazardous material disposal. The costs of stripping and re-plating can easily exceed the cost of avoiding the tin part. One such example is the D-subminiature series of connectors, commonly made with tin and zinc shell platings. Fortunately, this type of connector is very wide spread in its use, and extends to military products. Thus, the preferred route is to find the military version of connectors (e.g., D-Sub = MIL-C-24308) which have versions with no pure tin, zinc, nor cadmium.

Note: Cadmium can commonly be found on military connectors due to its good salt spray corrosion resistance, but is prohibited for space use by NASA. According to NASA's Electronic and Packaging Program (NEPP), cadmium is known to sublimate and redeposit

conductive sublimation products, resulting in short circuits [60]. This is in addition to the cadmium whisker problem. Thus, with very limited exceptions (e.g., a sealed scientific payload), cadmium should not be used at all in a spacecraft.

9.4 Mitigation by Conformal Coating and Leaded Process Rework

Arathane 5750 (formerly Uralane 5750) has been commonly used in NASA in satellites for many years to mitigate tin whiskers [71][72]. Conformal coatings such as this can help in cases where large surfaces of forbidden metals are exposed. Arathane/Uralane 5750 appears to be a very popular conformal coating for space which is based on Urethane. The previously mentioned NASA presentation shows that a conformal coating thickness of >2 mils is sufficient for holding tin whiskers underneath the coating [11].

Any alternate conformal coating material should be selected to have similar mechanical and electrical properties. Other considerations for selecting a new conformal coating material include outgassing, coefficient of thermal expansion, young's modulus, hardness, glass transition temperature, thermal conductivity, and electrical insulation. However, new materials may will lack the heritage for tin whisker mitigation, and carries the risk of penetration at unknown thicknesses.

Conformal coating can be very effective for areas where large spaces exist between adjacent metal surfaces. This includes passive, IC, and transistor packages with large spacing between their contacts.

However, without an exotic application technique, conformal coatings will be unable to naturally penetrate between all contacts and solder joints on small pitch packages such as TSSOP and TQFP. In addition, for devices with directly soldered thermal pads (e.g., HTSSOP or TQFN), conformal coating will not penetrate beneath the IC to isolate the thermal pad. Packages such as CSP and BGA, have their lead-less contacts concealed on the board mounting side of the package. High density BGA's have extremely small 170 micron contact-to-contact spacing.

New compact technologies have also driven passives, such as resistors and capacitors, to similarly small contact spacing. 0201 and 01005 packages have a 100 micron worst case spacing beneath its package [84]. Whiskers could easily grow beneath the package as it does

on the top side. High density COTS assemblies could utilize 0201 and 01005 packages, and thus represents a new risk.

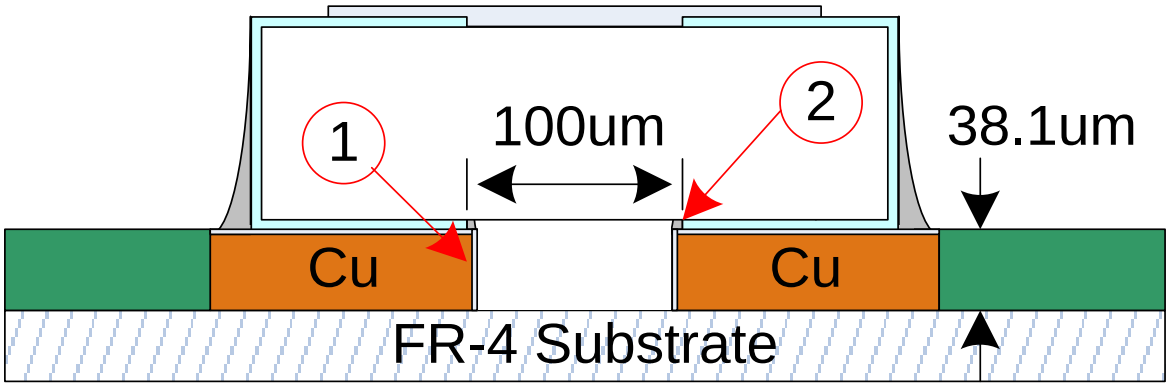


Figure 9.5: Cross Section of 0201 Chip w/ SAC Solder on Tin Plated Copper

Shown in **Figure 9.5**, we have lead-free plated 1oz. copper pads on top of FR-4 substrate. The drawing is roughly to scale, and based on a Koa Spear RK73H precision 0201 chip resistor, which is soldered on top of Koa Spear recommended pad layout. Assuming very little solder flows into the center of the two copper pads, there is a clear open space underneath the resistor for whiskers to grow.

Label #1 represents the risk of the *lead-free plating* on the PCB resulting in a tin whisker bridging over to the other side, essentially shorting out the resistor. Label #2 represents the risk of the *lead-free solder* forming a tin whisker over to the other side. The short 100 micron distance is small enough that either case is possible based on tin whisker measurements provided by Snugovsky [85] and NASA [11]. In either case, the integrity of either connected circuit node can be compromised.

Vacuum application techniques could possibly be the solution for filling in all the tiny gaps between solder joints and contacts. This would involve placing a board and conformal coating liquid under vacuum, and once high vacuum is achieved, applying the liquid to the board. A gentle pressurization procedure can then be used to gradually work the liquid into the voids. However, conformal coating underneath such confined spaces introduces a new risk, which is added stresses due to mismatched coefficients of thermal expansion under thermal cycling loads.

Thus, the most direct and known approach is to rework a RoHS component to use leaded solder in areas where conformal coating cannot naturally penetrate. To maintain the reliability of a COTS product through rework, it is important to use industry standard rework processes defined by IPC and JEDEC, which are, specific to each package type. In addition, datasheets for all components should be examined for the number of rework cycles that a component can handle. If a part can be replaced with fresh components, that is preferred. In small laboratories, this work may be better outsourced to companies who specialize in rework and fine pitch circuit repair.

9.5 Proposed Whisker Mitigation Rules

9.5.1 Electronic Component Package Rules

Table 9-3 shows my proposed rework and conformal coating mitigation rules for popular types of electronic packaging. Also listed with each package is the worst case minimum electrical contact to contact spacing on the package itself before soldering. These rules are based on the minimum gap, and the ability of simple brush and syringe conformal coating techniques to provide whisker mitigation.

Table 9-3: Compilation of Contact-Contact Spacing & New Proposed Mitigation Rules

Package Type	Pin Count Range	Min Contact Gap [mm]	Post-Assembly RoHS Whisker Mitigation
SMT Passives [84]			
01005 R/C	2	0.100	Remove, Hot Dip, Solder
0201 R/C	2	0.100	Remove, Hot Dip, Solder
0402 R/C	2	0.350	Conformal Coat
0603 R/C	2	0.600	Conformal Coat
0805 R/C	2	0.800	Conformal Coat
1206 R/C	2	1.800	Conformal Coat
Transistor, Diodes, and Low Pin Count IC Packages [66]			
SC70	3	**0.900**	Conformal Coat
SC70	5	0.250	Conformal Coat w/ Syringe
SC70	6	0.350	Conformal Coat w/ Syringe
SOT-23	3	**1.360**	Conformal Coat
SOT-23-5	5	1.390	Conformal Coat
SOT-23-6, 23-A	6	1.390	Conformal Coat
SOT-223	3 + HS Tab	1.460	Conformal Coat

HS = Heat Sink or Thermal Pad, **Reball/Hot Dip** in Sn63/Pb37 Process

Table 9-3 (Continued) Compilation of Contact-Contact Spacing

Package Type	Pin Count Range	Min Contact Gap [mm]	Post-Assembly RoHS Whisker Mitigation
DDPAK	3-7	0.279	Conformal Coat w/ Syringe
TO-220	3 + HS Tab	0.060	Conformal Coat
TO-92	3	0.737	Conformal Coat
Dual-Inline Pin			
CERDIP	28	0.889	Conformal Coat
PDIP / SPDIP	8-40	0.762	Conformal Coat
CERQUAD	68-84	0.950	Conformal Coat
Small Outline IC			
SOIC	8-28	0.760	Conformal Coat
SMD Flatpack No-Lead IC's, Exposed Thermal [63][66]			
DFN	6,8+1HS	**0.200**	Remove, Hot Dip, Solder
DFN	10 + 1HS	**0.200**	Remove, Hot Dip, Solder
DFN-S	8+1HS	**0.200**	Remove, Hot Dip, Solder
TDFN	6,8,10 + 1HS	**0.200**	Remove, Hot Dip, Solder
QFN 0.5mm Pitch	16,20,24,28,40,64 + 1HS	**0.200**	Remove, Hot Dip, Solder
QFN 0.65mm Pitch	16,20,28 + 1HS	**0.200**	Remove, Hot Dip, Solder
QFN 4x4mm	28 + 1 HS	0.150	Remove, Hot Dip, Solder
QFN-S 6x6mm	28 + 1 HS	**0.200**	Remove, Hot Dip, Solder
QFN 8x8mm	44 + 1 HS	**0.200**	Remove, Hot Dip, Solder
SMD Micro/Shrink Outline Pinned IC [66]			
MSOP 0.650mm Pitch	8	0.250	Conformal Coat w/ Syringe
MSOP 0.5mm Pitch	10	0.170	Conformal Coat w/ Syringe
SSOP 0.65mm Pitch	20,24,28	0.270	Conformal Coat w/ Syringe
TSSOP 0.65mm Pitch	8-40	0.350	Conformal Coat w/ Syringe
TSSOP 0.50mm Pitch	20-64	0.230	Conformal Coat w/ Syringe
TSSOP 0.40mm Pitch	14-100	0.170	Conformal Coat w/ Syringe
LQFP 0.8mm Pitch	32	0.350	Conformal Coat w/ Syringe
LQFP 0.5mm Pitch	144	0.230	Conformal Coat w/ Syringe
TQFP 0.8mm Pitch	32,44,64	0.350	Conformal Coat w/ Syringe
TQFP 0.5mm Pitch	64,80,100	0.230	Conformal Coat w/ Syringe
TQFP 0.6mm Pitch	80	0.270	Conformal Coat w/ Syringe
TQFP 0.4mm Pitch	100,144	0.170	Conformal Coat w/ Syringe
TQG 0.5mm Pitch (TQFP)	144	0.230	Conformal Coat w/ Syringe

HS = Heat Sink or Thermal Pad, **Reball/Hot Dip** in Sn63/Pb37 Process

Table 9-3 (Continued) Compilation of Contact-Contact Spacing

Ball Grid Arrays [64][65]			
BGA: Xilinx FB, FF 1mm Pitch	484-1927	0.300	Remove, Reball, Solder
BGA: Microstar 0.5mm Pitch	62-256	0.150	Remove, Reball, Solder
BGA: Microstar Jr. 0.5mm Pitch	8-195	0.150	Remove, Reball, Solder
BGA: micro-FCBGA8	559	0.150	Remove, Reball, Solder
BGA: VF-BGA 0.5mm Pitch	356	0.150	Remove, Reball, Solder
BGA: PBGA 1mm Pitch	360	0.650	Remove, Reball, Solder
XBGA	112	0.400	Remove, Reball, Solder
BGA: Xilinx CP(G)	196	0.150	Remove, Reball, Solder
BGA: Xilinx CS(G)	225	0.350	Remove, Reball, Solder
BGA: Xilinx FT(G)	256	0.400	Remove, Reball, Solder
BGA: Xilinx CS(G)	324	0.300	Remove, Reball, Solder
BGA: Xilinx FG(G)	484	0.300	Remove, Reball, Solder
BGA: Xilinx CS(G)	484	0.250	Remove, Reball, Solder
BGA: Xilinx FG(G)	676	0.300	Remove, Reball, Solder
BGA: Xilinx FG(G)	900	0.300	Remove, Reball, Solder

HS = Heat Sink or Thermal Pad, **Reball/Hot Dip** in Sn63/Pb37 Process

9.5.2 Exposed Lead-Free Plated / Lead-Free Solder Surfaces

Aside from just electronic packages, COTS assemblies will often contain blank lead-free finished copper pads, exposed vias, and other exposed lead-free surfaces. The following sequence handles these surfaces:

1. If the surface must be permanently exposed for testing, mechanical, or other electrical reasons, rinsing the surface with SnPb solder is required. This applies mostly to mechanical fastener areas and test points. For surfaces supporting mechanical fasteners, the final residual coating of solder should be kept minimal (e.g., only what a solder wick cannot remove).

2. If conformal coating will not effectively isolate metal whiskers to/from other electrical contacts, perform the SnPb rinse procedure, allowing its (partial) exposure. Perform a check to make sure that any whisker touching this surface, in the final assembly, will not cause a problem.

3. In all other cases, conformal coat the surface.

9.6 Proposed Mitigation Procedure for COTS Assembly

Based on the hybrid rework and conformal coat mitigation strategy, I propose the following process to mitigate whiskers on COTS assemblies.

1. Identify all components that must be 'reworked' based on the rules in **Table 9-3**

2. Identify metal whisker risk areas that cannot be conformal coated for whisker mitigation
- Includes areas for mechanical/electrical contacts and plated board mounting holes

3. Remove all 'rework' parts and rinse/clean/prep for SnPb process in accordance to industry standard practices (e.g., moisture bakeout with J-STD-033, and J-STD-001 solder purity for solder dipping)

4. For all areas that must have bare metal exposed after the pending conformal coating, rinse/clean with SnPb solder

5. Solder all previously removed 'rework' parts back onto the circuit board, and clean thoroughly to remove all fluxes

6. Perform conformal coating of as much of the assembly as practical to complete mitigation

9.7 Applying Proposed Whisker Mitigation Rules

Figure 9.6 shows an example of specifying areas, based on the mitigation rules in **Table 9-3**.

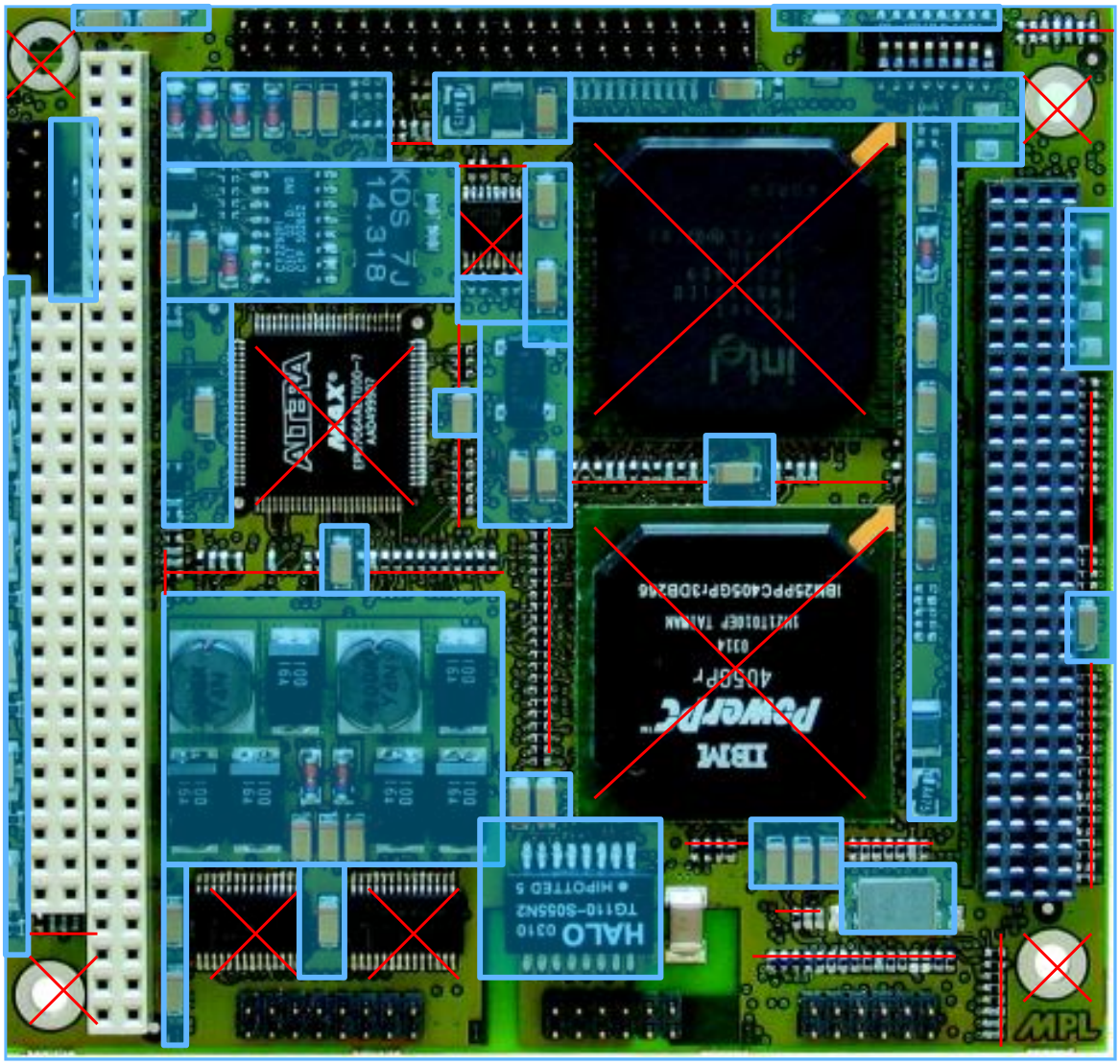


Figure 9.6: Application of Mitigation Rules to RoHS Compliant MPL MIP405 Assembly. (Items to be reworked are marked with red X's and Lines)

There are several key items that are worth mentioning in this rework specification:

- The blue areas only show the items that do not need to be reworked in order to be conformal coated. However, as the previously defined process says, coating should be done after all rework has been completed, and the coating should cover every surface which needs to be protected from whiskers, or requires whisker inhibition.

- All lead-free finished surfaces pads, regardless of the presence of solder or components, have been conformal coated. The only exceptions were the lead-free plated mounting holes at the corners.

- For the plated holes at the corners of the MIP405 assembly, they were marked for rework. The method of mitigation chosen was rework. This is preferred as opposed to conformal coating since maintaining electrical conductivity is necessary for grounding the otherwise floating hole plating. This also maintains thermal conductivity to spacers, versus a conformal coating layer which has a very low relative thermal conductivity. The plating can be reworked by rinsing the holes with Sn63Pb37 solder

9.8 Summary

Tin whiskers are a serious problem for satellite avionics, especially since they cannot be serviced once on orbit. After a review of tin whisker research from NASA, ESA, and other third party entities, I have established that tin whisker mitigation must be performed on COTS electronic assemblies.

With emerging new compact surface mount technologies, I have also identified a new risk, which is the growth of tin whiskers underneath chip resistors and capacitors in 0201 and 00105 packages. These passives are vulnerable to whiskers which extrude from exposed lead-free plating on copper pads, as well as whisker extrusion from SAC solders.

The proposed mitigation techniques include the prohibition of non-pre-soldered parts that contain the forbidden metals in their pure form, conformal coating, and reworking assemblies where conformal coating alone cannot mitigate the issue.

An application of the COTS mitigation procedure has been performed on a relatively complex assembly with mixed surface mount technologies of various sizes. The level of final rework must be decided based on risk tolerance and ultimate cost of rework.

Chapter 10: Conclusions

10.1 Summary of Environmental Risks to Avionics

The following table summarizes the different identified risk areas for avionics. Tied to each risk, I have identified the major research areas which can help mitigate each risk. Some risks areas are complex enough that not just one area of research can mitigate the risks. Spacecraft avionics have always required a multi-disciplinary approach to design and build. The adaptation of COTS products for use in space is no different.

Table 10-1: Summary of Risks to Avionics, and Mitigation Research Area

Period	Risk Category (w/ Overall Risk Color)	Mitigation Research Area
S&H	Handling Risks	Logistics and Safe Avionics Handling
Storage	Handling Risks	Logistics and Safe Spacecraft Handling
	Self and Cross Assembly Contamination with Outgassing	Chemistry and Avionics Materials
	Corrosion	Corrosion Mitigation
	Component Expiration and Material Degradation	Multidisciplinary
	Metallic Whiskers	Soldering, Conformal Coating, Metallurgy and Metal Finishing
Launch	Explosive Atmosphere (Hot Launch Only)	Explosive Atmos. Electronics
	Electromagnetic Interference (Hot Launch Only)	Electromagnetic Compatibility
	LV Integration Handling	Logistics and Safe Spacecraft Handling
	Shock and Vibration	Structural Dynamics and Avionics Materials
	Acceleration	Statics and Avionics Materials
	Aerodynamic Heating	Thermal Analysis
	Venting of Atmosphere	Pressure Vessels
Space	Vacuum and Temperature De-Rating	Electronics and Heat Transfer
	Thermal Cycling	Avionics Materials, Thermal, Fatigue
	Micrometeroids	Impact Protection
	Spacecraft Charging and the Plasma Environment	Electrical Insulation and Bonding,
	Atomic Oxygen	Chemistry
	Space Radiation Exposure	Radiation Effects on Microelectronics, Electronic Components, and Structural Materials

10.2 Recommendations on Future Work

This study is meant to lay the ground work for building a multi-disciplinary series of studies to facilitate the use of COTS in space. For a reader who is responsible for any part of a satellite mission, the recommendation is to first determine the goal of current and future satellite missions. Is the goal to provide an educational experience? What are the 'typical' success criteria for missions? The amount of weight placed on either answer will determine how much risk mitigation will be required.

Secondly, determine the parts needed to complete missions. Building a library of needed parts which have flown in space before can help demonstrate reduced risks, and can also reduce labor spent on searching for equivalent parts.

Third, prioritize which of the identified risks are most important to your type of missions. There are many risks which were discussed in this study. To achieve a mission's success criteria, this may not require all risks to be considered. For instance, if the primary goal is an education experience for a low cost, long term survivability could be disregarded.

Fourth, it is important to realize that a failure of even the smallest COTS part, such as a tiny surface mount resistor, can be catastrophic for the entire mission. Thus, a the resistor which initially cost $0.001 can now have a new value equivalent to the entire mission. Apply all necessary risks to the needed COTS components, and determine which risk are most serious.

Fifth, perform research and testing with an appropriately staffed team.

Finally, collaborate to share your results, and improve your results. Aside from proprietary information issues, although I am a proponent of learning the hard way some times, having each new spacecraft team starting from scratch is a gross waste of resources. Collaborations can be the key to magnifying and accelerating your COTS to space adaptation efforts.

10.3 Final Thoughts

The information that I have collected, processed, and contributed, all form an essential basis for risk prioritization. There is absolutely no question that using COTS in a space mission has significant risks. Thus, it must also be clear that small-budget small-sat programs must either accept the risks of COTS, or risk extinction. If the choice is to exist, knowing which risks to address first is vital to maximizing the outcomes of even the smallest budgets.

Appendix: Optical Remote Sensing Satellites: Risk/Performance Trades

Remote sensing is one of the Hawai`i Space Flight Laboratory's priorities. This provides new data for the scientists at the Hawai`i Institute of Geophysics and Planetology, as well as the many collaborators and sponsors (e.g., NASA, JPL) they work with. To better understand the needs for risk mitigation in low cost and short schedule missions, the risks exposed in this study are applied against several technical performance metrics for optical remote sensing.

Optical Remote Sensing Instruments

To design a satellite which performs all its required duties, we must first understand the needs of its users. Delivering an acceptable service level to users and stakeholders is the primary driver of identifying and mitigating risks. This understanding of the bigger picture especially important when there are expected problems from the lowest level parts.

Optical remote sensing is essentially taking pictures of the Earth over areas of interest. Instrument complexities can range from simple monochrome pictures, up to gathering hundreds of wavelengths for every ground spot in an image. These payloads typically image visible, near infrared, short-wave infrared, and also ultraviolet wavelengths. Microwave frequency electromagnetic (EM) waves, like visible EM waves (light), can also be considered to be observed in the 'optical' remote sensing category.

Typical applications include mapping the Earth, environmental science/monitoring, and military surveillance. One of the primary reasons for low-Earth orbit (LEO) remote sensing is the ability to provide global coverage with a single platform. Satellite orbits can be designed to provide sustained revisits of areas around the Earth. The costs per satellite may also be lower than typical large satellites operating in higher orbits, and thus lowers the bar for building entire groups of coordinated satellites called constellations.

Optical instruments aboard satellites operate with the same basic principles as consumer cameras. An example of a sensor is a basic silicon photodiode based CCD array. Unfiltered, each photodiode is sensitive to a wide range of photon frequencies. When a photon strikes a particular photodiode at a sensitive frequency, the transferred energy is converted into charges that can be accumulated, amplified, and digitized.

When particular wavelengths are of interest, filters can be applied to individual photodiodes to block out unwanted wavelengths. Of most interest to consumers are broadband wavelengths in the color spectrum to obtain red, blue, and green (RGB) intensities. However, since each pixel is expected to have an RGB value, but only one photodiode exists at a particular pixel's physical location, interpolation can used between adjacent R, G, and B pixels to reconstruct the original image. In more advanced techniques, called co-site sampling, the sensor is electro-mechanically moved to position actual red, blue, and green sensors to pick up photons at the same physical space. However, this requires at least three sets of movements, integration times, and data fusion. Thus, this type of sensor sacrifices image capture speed in favor of higher spectral fidelity.

More remote sensing science can be done on data which has more fidelity. For instance, narrowband wavelengths are used to detect different spectral compositions of a particular spot on the Earth. With sufficient amounts of narrowband information, spectroscopy can be applied to detect characteristics like levels of CO_2 in the air, soil composition, and health of vegetation.

However, arrays of high consistency narrowband filters can get quite expensive to manufacture and calibrate when you're using pixels that are on the order of a couple microns. One such method to simplify the splitting of wavelengths is the use of diffraction gratings. Diffraction gratings can take in a single slit of light, use diffraction to split the light into its different wavelengths, and then project a gradient of wavelengths toward a rectangular detector array. This is like how a prism can split sunlight into a rainbow, and can then be used to project the rainbow onto a grid patterned wall. The split rays of light will result in their different wavelength intensities at each pixel, thus allowing for the usual CCD charge accumulator readout. With the proper alignment, a pixel array n by m pixels can have either n or m different narrowband intensities from a single slit of light.

One important result of this particular diffraction grating method is that you can only take images which are 1 by n (or m) pixels. Thus, to take an image of a rectangular area, the sensor must be swept across an area like pushing a very thin broom forward which collects photons. And as such, this kind of imager is referred to as a push broom sensor. A satellite always has a 'ground track' which coincides with its velocity vector. Thus, the satellite simply

would need to ensure that the imager is oriented 'cross-track' so that it sweeps light up as the satellite orbits the Earth. Other similar sensor types include small pixel count sensor arrays which require electro-mechanical scanning to rapidly pan a sensor across a scene.

There are different classes of such remote sensing payloads. They range from wideband imagers, such as color cameras, all the way to hyper-spectral imagers which can gather up to thousands of narrowband data points. However, the data generated from higher band count imagers can be enormous, and thus demands more from a spacecraft bus in terms of data handling, storage, and downlink volume. All these factors are considered when balancing the cost of the satellite versus costs and remote sensing benefits.

Optical Remote Sensing Satellites Busses

A satellite, like an airplane, carries a payload. For an airplane, the bus is the aircraft itself. Passengers, crew, and cargo are the payload. Similarly, for a satellite, the bus is the structure, mechanisms, and all its supporting avionics. The sole purpose of the satellite bus is to support its payload. In this case, we're looking at optical remote sensing instruments.

With the idea of the bus in mind, there are a few basic things that an optical instrument needs. This includes a sturdy structure to mount to; an electrical system to provide it power; an unobstructed view port to look out of; a maneuvering system to point and orient its sensor the right way; a good operating/survival thermal environment; a well communicating onboard robot to remind it when to take pictures, a way to get its precious data down to Earth, and last but not least, a launch vehicle to put the whole satellite system in the right place at the right time.

In summary, these basic needs are covered by the following subsystems:

- Spacecraft Structure & Unobstructed View Port
- Electrical Power Subsystem
- Attitude Determination and Control Subsystem
- Thermal Control Subsystem (Passive and/or Active)
- Flight Computer
- Communications Subsystem
- Orbit Determination and Launch Vehicle

However, before the spacecraft ever gets put into orbit, a great deal of research and development must be done. This includes everything from selection of wiring, nuts and bolts, all the way up to complete off the shelf or custom built subsystems. Attention paid to every important detail will help ensure sure that a two cent screw or IC does not prematurely end a mission.

Technical Performance Metrics and Mission Considerations

To understand what needs to be protected against technical risks, the following sections discuss several key technical performance metrics (TPM) for remote sensing missions. Amazing measurement capabilities from an instrument means nothing if the data cannot be processed and/or sent down to Earth. The goal is to minimize any deviation from pre-launch performance. The technical details of how COTS risk varies with these parameters are provided later in the spacecraft design considerations chapter.

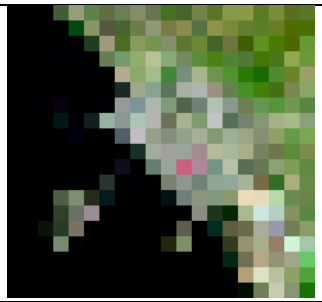
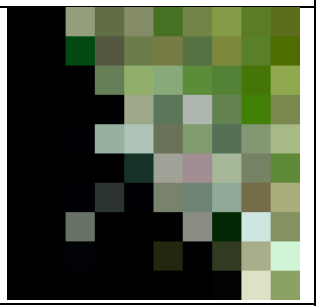
Spatial Resolution and Error

Each square pixel on a detector, looking through a telescope, projects an approximate rectangular spot size on the Earth. The larger spot size, the less detail you're able to resolve. In addition, large fields of view, or looking at significant angles off nadir (directly below) will have sometimes significant differences in slant range/angle.

Large differences in slant ranges result in non-uniformity of ground spot sizes. This problem is not easily fixed by physical means due to dynamic errors in satellite pointing. Software compensation can be used in conjunction with satellite attitude data to characterize and compensate for optical distortion. However, this is more desired to be performed on the ground to prevent loss of any fidelity. Scientific remote sensing users actually prefer acquiring raw data over any sort of processed data. For avionics, the need for raw data can quickly drive the storage and communications requirements of satellite avionics up. Each additional bit of storage represents more potential risk of data corruption and system failure.

Perhaps the most important question for spatial resolution is deciding what the remote sensing users need to look at. For instance, to differentiate between a football field and the desert, a spatial resolution of 25 meter square pixels may be sufficient. But, if the users wanted to read someone's license plate from orbit, the payload will need much finer spatial resolution.

Appendix Table 1: Examples of spatial resolution down-sampling

~15 Meter Pixels	~30 Meter Pixels	~60 Meter Pixels	~120 Meter Pixels
			
LandSat-7 image courtesy of NASA			

Depending on the satellite constraints, telescopes can be used to achieve a particular spatial resolution for a given altitude above ground. However, the more 'zoom' a telescope has, the larger and heavier it becomes. Each kilogram of payload costs tens of thousands of dollars to

launch. Thus, achieving a certain spatial resolution from low Earth orbit (LEO, ~160-2000 km) is much less costly than geostationary orbit (GEO, ~35,000km).

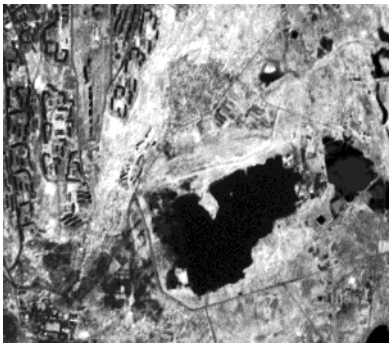
Major System Trades for Finer Spatial Resolution:

- Increase data handling volume or decrease image quantities
    - Additional data handling volume increases risk of data corruption in COTS parts
- Increase telescope size, or decrease altitude over areas of interest
    - May involve trading launch vehicles and ride sharing opportunities

Spectral Bands and Resolution

Whether the payload is using a filter array or diffraction grating, ideal monochromatic filters which let absolutely one wavelength through is not practically achievable. There is almost always some non-ideal effects which allow the bleed-through of nearby wavelengths. Thus, spectral resolution refers to the smallest group of wavelengths that can be differentiated in the spectrographic image. The number of bands that can be resolved are also of interest. For instance, multi-spectral imaging refers to tens of bands of photons. Hyper-spectral imaging can take up to thousands of spectral bands in at once.

Appendix Table 2: Example spectral down sampling on a LandSat-7 image

False Colored Original False coloring (24-bit: RGB) From select & panchromatic bands(Size: 234kB)	**Approximated Palette Colorizing** False coloring (8 bit palette) From false colored original (Size: 80kB, ~0.33 of Original)	**Normalized Wideband Intensity** Grayscale Mapping (4-bit) From false colored original (Size: 40 kB, ~0.17 of Original)
		
LandSat-7 image courtesy of NASA Select ETM+[1] Bands: 2: 525-605nm, 4: 759-900nm, 7: 2090-2350nm (30m Spatial Resolution) Panchromatic Band: 520-920nm (15m Spatial Resolution) Intensity Mapping: Normalized sum of RGB intensities from original false color image Image Dimensions: 301x264 Pixels (79464 Pixels)		

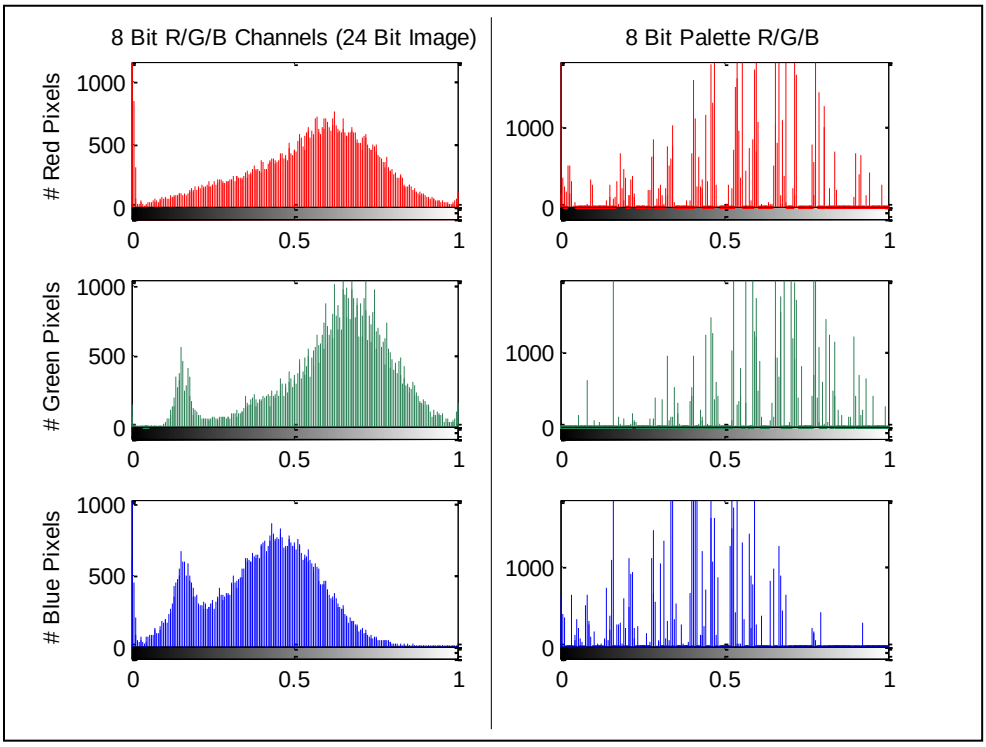
For color imaging, high resolution grayscale images can be downloaded separately, and then combined with low resolution color or other spectrum images. The fusion of the two images results in a colorized high resolution image. This is one common strategy used for reducing the amount of data volume transferred to the ground. As seen in **Appendix Table 2**,

[1] See Reference [6] for more details on ETM+ Bands

LandSat-7 images are shown with false coloring. The original image utilizes wideband panchromatic fifteen meter data, overlaid with thirty meter data from two NIR and green/blue bands.

Each spectral band can essentially be viewed as a separate image. For example, if an imager takes ten spectral bands in at a time, one picture of an area becomes ten times the data volume of a normal monochrome image. As with spatial resolution, a higher data volume means a higher risk of COTS data storage and handling failures.

Scientific data can typically only tolerate lossless compression versus 'lossy' algorithms. As an example, color and greyscale palettes were used for the **Appendix Table 2** image data reduction. The magnitude of data loss may not be completely visible to the naked eye, but the approximated data reduction can come at a severe cost to the fidelity of science data. Out of a previous 255 levels per each of the three spectral bands (>16 million combinations), the color palette reduces the combinations down to 255. At a more severe data reduction, the 4-bit greyscale intensity mapping goes down to 16 different categories of intensity.



Appendix Figure 1: Normalized Intensity Histogram of 24 Bit R/G/B vs 8 Bit Palette

Appendix Figure 1 shows a histogram comparison between the images in **Appendix Table 2** for 24 bit false coloring versus an 8-bit palette approximation of the data. Palettes can be acceptable for pictures where only the human eye will examine the data. But as the comparison shows, the amount of useful information for scientific purposes is greatly reduced. Since lossy algorithms like this may not even be tolerable, potentially massive amounts of data due to multi/hyperspectral imagers will have to be handled. Thus, it will be necessary to mitigate any associated risks of data corruption to an acceptable level.

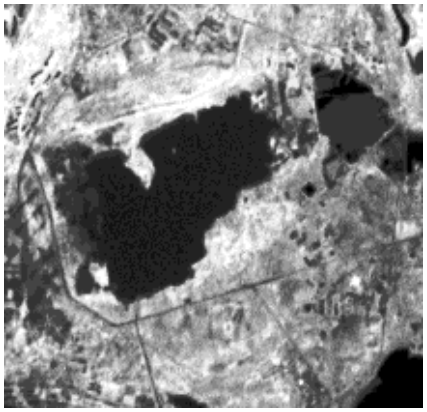
Major System Trades for More Spectral Bands:

- Each spectral band can be seen as a completely separate data set, thus:
    - Increase data handling volume or decrease image quantities
    - Additional data handling volume increases risk of data corruption in COTS parts
- Excess Spectral Resolution: High performance multi-spectral cameras may require band stripping or averaging to optimize routine data downlink volumes

Quantization Resolution and Error

Quantization resolution refers to the discrete intensity levels that each pixel in an instrument can differentiate. For example, a 12 bits of quantization can yield 2^12 (4096) different levels of intensity. However, all that resolution may not be useful if all your users need is 4 shades of gray. In addition, quantization noise may invalidate a few bits worth of resolution. Excessive amounts of quantization resolution results in either more expensive data handling/data transfer systems, or reduces the amount of images transferrable within a fixed period. As with spectral an spatial resolution, excess data volume increases the amount of necessary hardware, which in turn increases exposure to COTS failures. Ideally, the instrument would be customized to provide exactly the quantization resolution needed.

Appendix Table 3: Example quantization down sampling of a LandSat-7 image

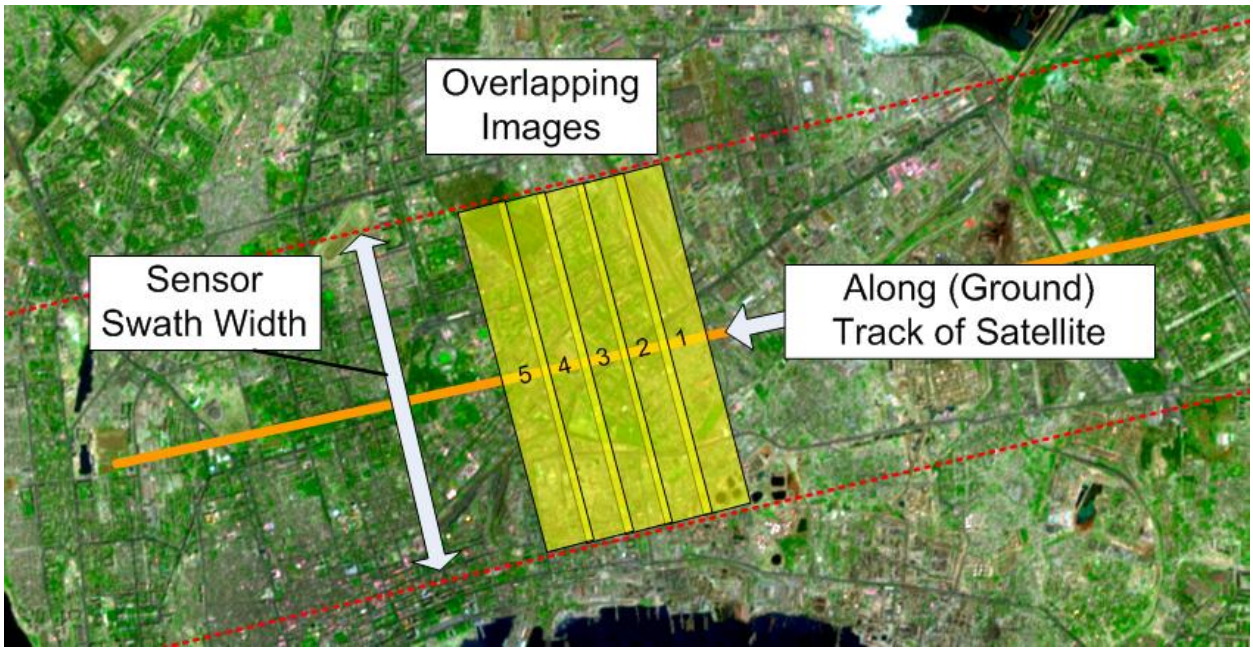
8 Bit Grayscale (Size: 46kB, 217x209 Pixels)	4 Bit Grayscale Palette (Size: 23kB, 0.5 of Original)	1 Bit Black and White (Size: 6kB, 0.13 of Original)
		
LandSat-7 image courtesy of NASA		

Major System Trades for Higher Quantization Resolution or Less Error:

- Increase data handling volume or decrease image quantities
    - Additional data handling volume increases risk of data corruption in COTS parts
- Excess Quantization Resolution: Increase onboard data processing requirements to accommodate for down-sampling data before downlink

Swath Width and Coverage

As a satellite orbits the Earth, the satellite virtually traces a line on the Earth below in the true nadir direction. The line of travel over the Earth is satellite's ground track. Swath width refers to the cross-track (versus along ground track) field of view. As discussed in spatial resolution, looking at angles significantly away from nadir can be detrimental to imaging uniformity. At large off-nadir angles, pixels which were approximately square become stretched and rectangular. There are limits on the amount of corrective post-processing that can be done. Thus, the orbit is strongly linked with how 'spatially' far you can move the swath along the cross track direction before pixel distortion becomes unacceptable.



Appendix Figure 2: Example swath width which includes overlapping coverage

As the instrument's swath width scans the Earth, it can generate a sheet of images. Coverage can either refer to possible targets that can be imaged, or targets that have been imaged. However, aside from pointing the satellite at desired targets, the greatest limitation on coverage is data handling capability and data transfer volume. For instance, imaging a single strip of Earth, from pole to pole, can potentially be on the order of gigabytes of data. As usual however, not everything is perfect. Some overlap is required to reconstruct a seamless image. Cameras which take rectangular blocks of images (frames) at low frame rates especially require overlap for image reconstruction. With the duplicated data from

overlapping images, onboard processing can either be done to perform stitching, or data handling volumes will need to be increased.

Space to Earth links, given enough power and bandwidth, can technically be any data rate. Small satellites have links that range from 300bps to 800Mbps. However, at the high end, the radio itself can easily cost over a million dollars per unit, and usually operate at higher frequencies (e.g., X-Band 8000-8500MHz) which incur very steep free space path losses.

Just as how the payload affects the system, the choice of the also radio makes ripples throughout the system. For example, the spacecraft will need generate enough power to feed the radio enough power. In a small spacecraft, high speed payload data transmitters can be the single highest power consumer on the bus. Directional and steerable antennas can be used to reduce power requirements, but it can also decrease reliability and shorten link times. Each increment of COTS parts and complexity increases the chances of problems.

Major System Trades for More Coverage

- Increase data handling volume or decrease image quantities
- Increased data handling volume increases cost, power consumption, and/or antenna steering requirements
- Constrain possible orbits for a desired coverage
    - May involve trading launch vehicles and ride sharing opportunities
- Excess Data Generation: Increase onboard data processing to strip out images that are not of interest, e.g., cloud cover, land, or ocean masses

Temporal Resolution (a.k.a. Revisit Time)

To study periodic Earth phenomena, or to conduct surveillance, temporal resolution is the frequency of re-visiting the same spot on Earth. Certain orbits may take up to a month or more to revisit the same spot. Thus, revisit times become an extremely important metric when getting the most up to date information is paramount.

However, revisiting the same spot does not always guarantee a usable picture. This includes cloud cover which can obscure an area of interest, or areas the Earth 'at night' in the case of a visible imager payload. In surveillance applications, a priority may be to minimize revisit times to maximize good imaging opportunities.

To optimize temporal resolution, orbits can be designed to maximize time over an area, as well as minimize the time to revisit. For example, an orbit can be designed to have a very high apogee (highest altitude in orbit) in order to maximize time over a target. However, a high apogee in a LEO or medium Earth orbit (MEO) will expose the satellite to orders of magnitude more radiation from the Van Allen Belts. This is an area of concern when considering COTS components for these types of orbits.

<u>Major System Trades for More Temporal Resolution</u>

- Increase data handling volume or decrease image quantities
- Constrain orbits to low-revisit times, and if that isn't enough:
    - Use a constellation of satellites with various orbits to maximize revisits
    - Move to geosynchronous orbit which maintains its field of view over areas of interest

Pixel Smear

There are the major determining factors of pixel smear are: spatial resolution, spacecraft ground track velocity, differential between spacecraft angular rate and nadir, and attitude stabilization system jitter, and finally, imager integration time. Typical LEO ground track velocities are around 7km/s. As an imager's integration starts, the satellite's ground track is still moving. If the satellite is fixed in a nadir pointing attitude, what was in the center of a pixel a second ago is now 7km away.

A common example is the smearing effect you get when taking long exposure pictures of traffic at night. Perhaps it is great for art, but it is not great for multi-million dollar science. Pixel smearing should be minimized, and as a rule of thumb, kept to less than half a pixel to retain image quality.

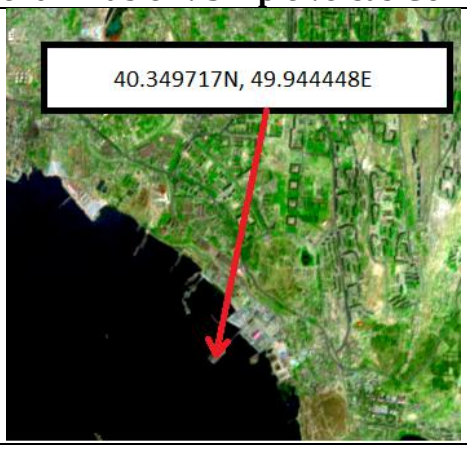
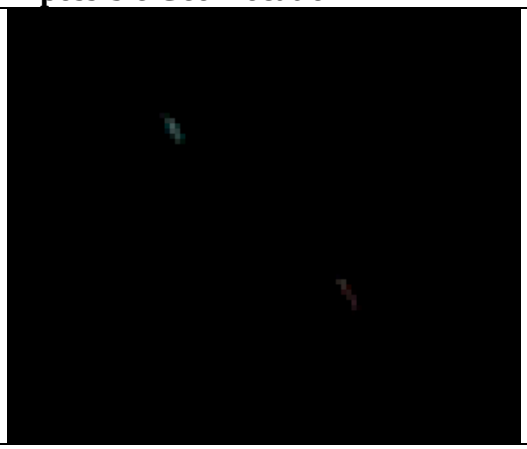
Major System Trades for Less Pixel Smear

- Increase altitude significantly in order to reduce ground track velocity
    - Not a preferred option since this gains you the least for the most cost and risk
    - Requires a larger telescope to compensate for new spatial resolution
    - May involve trading launch vehicles and ride sharing opportunities
    - Exposes satellite to more radiation
- Increase spatial resolution for more integration time
- Require one or more cameras with integration times of less than 1/3 pixel smear
    - But, frame rates may also need to in the range of hundreds of FPS
- Slew spacecraft to track a ground spot for larger integration times. Trade off continuous imaging coverage and varying optical distortion

Geo-location Capability and Accuracy

Especially in surveillance applications, it is very helpful to know where a picture was taken. Geo-location can be done either onboard, or in post processing. However, in either case, sufficient amounts of data about the spacecraft's position and orientation, or known landmarks in the image are necessary to get any sort of reasonable accuracy. In the case of imaging the desert, or large spans of water, providing spacecraft position and orientation is absolutely required to bound error in geo-location.

Appendix Table 4: Simple versus Complicated/Impossible Geo-Location

	
Manually Located with Google Maps	Unable to register ship locations, no context
LandSat-7 image courtesy of NASA	

Major System Trades for More Geo-Location Accuracy

- Higher accuracy attitude/location sensors, trades for cost
    - Subjective: Power/Size/Weight will also be affected, sometimes favorably
- Very high accuracy sensors may be only be available from space grade products
- Implement a routine geo-location calibration system, trades for complexity
- Require landmarks for geo-location registration, trades for areas of utility and increased post-processing delay. In addition, it may not be feasible with certain targets which have high absorption of particular spectral bands.

Data Latency

Data latency refers to the entire time from imaging to delivery to the end user. When you have a multi-million dollar camera flying around, it is imperative that the image data be

delivered to the end user before the data is invalid. For instance, when trying to track a speeding car down the freeway with a satellite, the data will become invalid much quicker than a slow cargo ship in the ocean.

Major System Trades for Minimization of Data Latency

- Approached by more often contact with an Earth stations: More satellite power consumption, increased system costs (which includes more Earth stations), and orbit types can be restricted.
- Higher data rates with Earth stations, traded for higher power utilization and system costs.
- Direct Broadcast System: Immediate real-time access by all Earth stations in view, traded for extreme power consumption increases, and a higher likelihood of legal roadblocks if continuous emissions are used everywhere around the world
    - If users are in position to receive the data, this reduces the time that data is kept onboard. Thus, this can significantly reduce the exposure of data to radiation induced data corruption.

Cost, Benefits, and Risk

Cost, benefits, and risks are all measures of feasibility for the entire remote sensing mission. Stripped down to its basics, if remote sensing from a terrestrial tower or airborne platform is sufficient for all of the mission's goals, a satellite is probably not a good choice. A satellite's main advantage for remote sensing is being able to provide access to global coverage from even a single platform. With passive remote sensing, global coverage can be even achieved without detection. Thus, sometimes a satellite may be the only choice for certain applications.

It is important to remember that satellites are systems operating within a larger mission 'system of systems'. The weakest link will be the mission system's upper limit on performance and reliability. In a low cost mission using COTS components, the satellite is very likely to be the weakest and riskiest link.

Summary

To recap, there are many major trades to be made within a remote sensing satellite itself, and across the mission. Being able to balance conflicting performance and reliability requirements is necessary to maximize the resources available.

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