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PAPER

Phase cascade lattice rectifier array: an exactly solvable nonlinear network circuit

M Nazari[1]**, J Chen**[2]**, A M Gole**[3]**, M K Hong**[4]**, P Mohanty**[4]**, S Erramilli**[4,6] **and O Narayan**[5,6]

[1] Electrical and Computer Engineering department, Boston University, United States of America
[2] Monta Vista High School, Cupertino CA, United States of America
[3] Electrical and Computer Engineering department, University of Manitoba, Winnipeg, Canada
[4] Physics department, Boston University, 590 Commonwealth Avenue, Boston, MA 02215, United States of America
[5] Physics department, University of California Santa Cruz, United States of America
[6] Authors to whom any correspondence should be addressed.

E-mail: shyam@bu.edu and onarayan@ucsc.edu

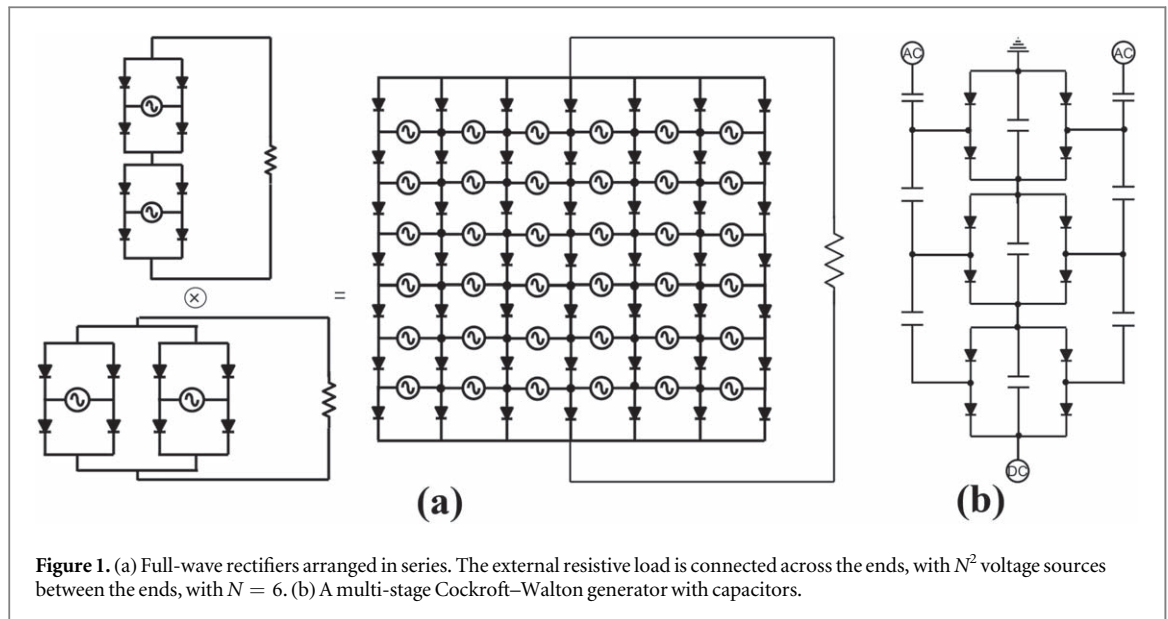**Keywords:** nonlinear network, diode array, lattice model

Abstract

An exact analysis of a 2-D lattice network consisting of $N \times N$ sites with rectifier and AC source elements with controllable phases reveals a method for generating ripple-free DC power without the use of any filtering circuit elements. A phase cascade configuration is described in which the current ripple in a load resistor goes to zero in the large N limit, enhancing the rectification efficiency without requiring any additional capacitor or inductor based filters. The integrated modular configuration is qualitatively different from conventional rectenna arrays in which the source, rectifier and filter systems are physically disjoint. Nonlinear networks in the large N limit of source-rectifier arrays are potentially of interest to a fast evolving field of distributed power networks.

Introduction

The need for DC electrical power generation from AC sources is arguably the most significant nonlinear problem of central importance to modern society. Solutions to the problem involve fundamental aspects of nonlinear networks as well as in extensions to higher frequency applications of interest to Physicists. It has long been appreciated that rectifiers are nonlinear devices that break Lorentz reciprocity [1]. Interest in distributed energy networks [2], the need for alternative energy technologies [3, 4], energy harvesting systems [5, 6] and energy scavenging systems [7] have spurred renewed interest in the problem of scalability. New approaches to hierarchical control of AC and DC microgrids have in turn sparked innovation [8]. A number of configurations have been investigated for power generation from AC source networks, extending to wireless power generation [5, 9], rectenna arrays and wireless power transfer systems [10–12] as well as smart grids [13]. A classic configuration consists of rectenna arrays in which diode arrays are used to rectify the output of a receiving antenna, followed by filters to provide the desired DC power. Such nonlinear networks have become very interesting recently for devices in which diode elements are integrated into plasmonic structures, and in the rapidly emerging new field of nonlinear metamaterial devices [14–16], efficient metamaterial based energy harvesters [17] among others. The ability to design and engineer local phase shifts within each element of a receiving array represents a new capability that has not been studied in detail, and the configuration space remains unexplored. Lattice networks consisting of nonlinear elements like diodes and random circuit elements have been extensively studied in Statistical Physics as models of directed networks and percolation problems [18–21]. More recently, networks of nonlinear circuit elements have been shown to exhibit symmetry-breaking transitions associated with bifurcations [22]. The range of phenomena is vast even for deterministic systems. Up to now, the inclusion of voltage sources within the lattice sites has not been widely considered. It may be expected that integration of sources with random or varying phases at each lattice site will lead to an even richer range of phenomena.

Figure 1. (a) Full-wave rectifiers arranged in series. The external resistive load is connected across the ends, with N^2 voltage sources between the ends, with $N = 6$. (b) A multi-stage Cockroft–Walton generator with capacitors.

In this article, we investigate rectification phenomena in a particular 2-D lattice network consisting of N^2 sites , in which each lattice site consists of an AC source in a bridge-rectifier like configuration. As shown in figure 1, each lattice site shares one diode with each of its nearest neighbors. The configuration is inspired by rectenna arrays, but now with the addition of AC sources at each lattice site. The system consists of N^2 AC sources, and $(N + 1)^2$ diodes. It can be seen that when $N = 1$, the configuration is identical to a classic bridge-rectifier combination. Each column of unit cells harks back to the iconic Cockroft–Walton generator. Each row of parallel cells is characteristic of a microgrid. Both the Cockroft–Walton generator and the microgrid configurations have disadvantages in terms of current carrying capacity and scalability of voltage. When arranged in a 2-D lattice, we show that new features emerge that overcome the shortcomings. Common to most nolinear circuit networks the current through the load resistor has many frequency components, with the zero frequency DC component being the most important for rectification.

The advent of distributed generation of power from both conventional and alternative energy sources provides motivation to study networks in which voltage sources are also distributed throughout the lattice. Of particular interest is the generation of DC power and ripple-free voltage sources, not only for their ubqiuitious use but also for efficiency in transmission over long distances with asynchronous power generators derived from a wide range of sources for energy harvesting.

Lattice model

We consider the challenge of how to arrange a lattice of $M \equiv N^2$ AC voltage sources, with suitably chosen relative phases and with diodes for rectification such that it can produce an almost dc source. For definiteness, consider a 2-D lattice of elements arranged as shown in the figure 1. In this section, we present the analysis for idealized diodes, which operate in just two states determined by the bias voltage across the diode: (i) an 'off' state, at negative bias, where the current is Zero; (ii) an 'on' state, at positive bias, where the current is an arbitrary positive value limited only by the load.

We will briefly consider in a later section more realistic diode models later using numerical simulations on commercially available Silicon diodes with a forward voltage of $\sim$.8 V, and with current set by a non-zero forward resistance.

The lattice arrangement of interest is shown in figure 1 with N^2 voltage sources arranged in series with a load resistor R_L. The total number of diodes required is $4M \equiv 4N^2$, with 4 diodes per unit cell. Motivation for this lattice network comes from shortcomings in simple series and parallel arrangements of rectifiers. In the simple series arrangement, each diode must then be rated to carry up to the maximum total current flowing through the load resistor, which limits the utility of the series configuration, as we show next. With the rectified sources in series, the total voltage at time t is

$$V(t) = \sum_{j=1}^{N^2} V_0 |\sin(\omega t + 2\pi j/N^2)|. \tag{1}$$

Clearly, this is a periodic function of time, with time period $T = 2\pi/(\omega N^2)$ that also violates time-reversal invariance. For the simple case when N is an even number, we have

$$V(\omega t = 2\pi k/N^2) = 2V_0 \cot(\pi/N^2)$$
$$V(\omega t = \pi(2k-1)/N^2) = 2V_0 \csc(\pi/N^2) \tag{2}$$

are the minima and maxima of $V(t)$.

The ratio of minimum to maximum voltage is $\cos(\pi/N^2)$, and the frequency of these ripples is $N^2\omega$. For large N, the ripples have height $\pi V_0/N^2$, and are superimposed on a DC voltage of $2N^2 V_0/\pi$. We note that the peak current carried through each diode is approximately $2N^2 V_0/(\pi R_L)$, which it carries for half the cycle. For large N this current can exceed the maximum rating for the diode in the series configuration. This limitation is inherent in any series configurations. The iconic Cockroft–Walton generator shown in figure 1(c) is constrained in its utility by such a limitation on the current.

As an alternative to the simple series arrangement, the current load in each diode can be reduced by adopting a parallel configuration shown on the left side of figure 1(a). For M bridge rectifiers arranged in a parallel configuration, the sources have to be in phase. The fraction of the ripple in the output voltage can be seen to be just as large it would be for a single rectifier, and additional filtering would be needed to get DC current through the load resistor. In the simple parallel arrangement shown in the figure, the current is distributed among the unit cells, but the voltage across the resistors is now limited by the forward voltage drop across two diodes.

These elementary arguments motivate us to investigate a hybrid system that combines series and parallel combinations into the 2-D lattice shown in figure 1, with each unit cell is mapped onto a conventional bridge-rectifier. Remarkably, we find that for a special choice of phases of the AC sources, the configuration provides the advantage of reduced ripple in the rectified DC voltage of a series combination, with the advantage of reduction in peak current that is the hallmark of the parallel combination. The lattice arrangement analyzed here solves both problems and the system is inherently scalable for both high voltage and high currents while remaining within the damage thresholds of the diodes. We now show how hierarchical control of the phases results in perfect conversion efficiency. In our configuration, the phases of the voltage sources are uniformly distributed between zero and 2π.

Figure 1(a) shows the proposed alternative arrangement of voltage sources. Diodes are placed on the vertical sides of the square, and voltage sources on the horizontal sides. Conducting strips at the top and the bottom are linked to the external load. The voltage across the source in the i'th row and j'th column is

$$v_{ij}(t) = (-1)^i V_0 \sin\left[\omega t + 2\pi\left(\frac{j}{N} + \frac{i}{N^2}\right)\right], \tag{3}$$

where $0 \leqslant i \leqslant N - 1$ and $1 \leqslant j \leqslant N$. The phase angle associated with the source at (i, j) is $2\pi(j/N + i/N^2)$ when the row index i is even or zero, and is $= 2\pi(j/N + i/N^2) + \pi$ when the row index is odd within the index range $0 \leqslant i \leqslant N - 1$. The sign of the voltage across a source is fixed by defining it as the difference between the voltage at the right end and at the left end of the source. Then one can verify that the voltage at the j'th junction between voltage sources in the i'th row is

$$V_{ij}(t) = \frac{(-1)^{i-1} V_0}{2\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j + \frac{1}{2}}{N} + \frac{i}{N^2}\right)\right] + c_i(t), \tag{4}$$

where $0 \leqslant j \leqslant N$ and $c_i(t)$ is a j-independent function of time in the i'th row that has to be determined. (Equation (4) can be verified by taking the difference in the voltages at successive nodes and comparing to equation (3).) The voltages V_{ij} are then the voltages at the ends of the various diodes. The functions $c_i(t)$ can be determined by the condition that, at any time t and in the approximation we are working with, none of the diodes can be forward biased, and at least one diode in each row must be at zero bias in order for current to flow from one row to the next. This ensures that

$$\min_j[V_{i+1,j}(t) - V_{ij}(t)] = 0 \tag{5}$$

independent of t, for $N - 1 > i \geqslant 0$. This fixes $c_{i+1}(t) - c_i(t)$. Similar reasoning can determine the voltages at the conducting strips at the top and bottom of the lattice.

To understand the results obtained, we first consider a continuum approximation, where the number of nodes in each row is very large. From equation (4), the voltage across any row is a sinusoidal curve with amplitude $N V_0/(2\pi)$. The sinusoidal curve for each row is upside down compared to the adjacent rows. (The curve in each row is also shifted horizontally by a phase of $2\pi/N^2$ with respect to the preceding row, but this shift is negligible in the $N \to \infty$ limit.) From equation (5), we immediately obtain

$$c_{i+1}(t) - c_i(t) \rightarrow -\min_j \frac{2NV_0(-1)^{i-1}}{2\pi} \cos\left(\frac{2\pi j}{N} + \phi_i(t)\right), \tag{6}$$

where $\phi_i(t) = \omega t + \pi/N + 2\pi i/N^2$. Thus $c_{i+1}(t) - c_i(t) = NV_0/\pi$. By the same reasoning, the voltages of the two conducting strips are $c_0(t) - NV_0/(2\pi)$ and $c_{N-1}(t) + NV_0/(2\pi)$. Therefore the voltage difference between the two conducting strips is $N^2 V_0/\pi$, and a DC current flows across the load resistor.

With an understanding of the behavior of the phase cascade shown in the $N \rightarrow \infty$ limit, we now consider the case of a finite lattice. The displacement in the sinusoidal curves for successive rows, i.e. $c_{i+1}(t) - c_i(t)$, is obtained by the condition

$$\min_j \frac{(-1)^i V_0}{2\sin(\pi/N)} \left\{ \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{i+1}{N^2}\right)\right] + \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{i}{N^2}\right)\right] \right\}$$
$$+ c_{i+1}(t) - c_i(t) = 0. \tag{7}$$

Because N is even, replacing $j \rightarrow j + N/2$ changes the sign of both cosine terms. Since the minimum over all j is taken, the factor of $(-1)^i$ can be dropped. We can also replace the minimum with the maximum, with a change of sign:

$$c_{i+1}(t) - c_i(t) = \max_j \frac{V_0 \cos(\pi/N^2)}{\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{i+\frac{1}{2}}{N^2}\right)\right]. \tag{8}$$

The voltage of the horizontal strip at the top of the array in figure 1(a) is

$$V_{\text{top}}(t) = c_0 + \min_j \frac{V_0}{2\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N}\right)\right]$$
$$= c_0 - \max_j \frac{V_0}{2\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{1}{N}\right)\right], \tag{9}$$

where we have replaced j with $j+1$ to get the extra phase of $2\pi/N$, and used the fact that $j \rightarrow j + N/2$ reverses the function. The voltage of the horizontal strip at the bottom of the array in figure 1(a) is

$$V_{\text{bottom}} = c_{N-1} + \max_j \frac{(-1)^{N-1} V_0}{2\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{N-1}{N^2}\right)\right]$$
$$= c_{N-1} + \max_j \frac{V_0}{2\sin(\pi/N)} \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{N-1}{N^2}\right)\right]. \tag{10}$$

The voltage difference between the two horizontal strips can be obtained by subtracting these two equations. It is convenient to write this as

$$\Delta V(t) = c_N(t) - c_0(t) + \delta V(t) \tag{11}$$

by formally extending equation (8) to $i = N - 1$, where

$$\delta V(t) = \frac{V_0}{2\sin(\pi/N)} \left\{ \max_j \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{N-1}{N^2}\right)\right] + \max_j \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{1}{N}\right)\right] \right.$$
$$\left. - \max_j \left\{ \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{1}{N}\right)\right] + \cos\left[\omega t + 2\pi\left(\frac{j+\frac{1}{2}}{N} + \frac{N-1}{N^2}\right)\right] \right\} \right\}. \tag{12}$$

For the first part of equation (11), using equation (8),

$$c_N(t - \tau) - c_0(t - \tau) = \frac{V_0 \cos(\pi/N^2)}{\sin(\pi/N)} \sum_{i=-N/2}^{N/2-1} \max_j \cos\left[\omega t + 2\pi\left(\frac{j}{N} + \frac{i}{N^2}\right)\right], \tag{13}$$

where we define $\omega\tau = \pi/N + \pi/N^2$, and we have used the periodicity of the summand with respect to $i \rightarrow i + N$ to change the limits of the sum. This is a periodic function of time, with a period of $2\pi/(\omega N^2)$. If $0 < \omega t < 2\pi/N^2$, which covers one time period, every term in the sum on the right hand side of equation (13) is maximized at $j = 0$. Thus the minima and maxima of $c_N(t - \tau) - c_0(t - \tau)$ occur at

$$c_N(-\tau) - c_0(-\tau) = \frac{V_0 \cos^2(\pi/N^2)}{\sin(\pi/N^2)} \qquad (14)$$

and

$$c_N\left(\frac{\pi}{\omega N^2} - \tau\right) - c_0\left(\frac{\pi}{\omega N^2} - \tau\right) = V_0 \cot(\pi/N^2). \qquad (15)$$

The ratio of the two is $\cos(\pi/N^2)$. Thus for large N, $c_N(t) - c_0(t)$ tends a DC voltage of magnitude $N^2 V_0/\pi$, with ripples whose frequency is $N^2\omega$ and height is $\pi V_0/(2N^2)$.

We now turn to the function $\delta V(t)$. In equation (12), it is easy to see that replacing $\omega t \to \omega t + 2\pi/N$ is equivalent to $j \to j + 1$, i.e. the function is periodic with a period $2\pi/(N\omega)$. Furthermore, $\delta V(t) = 0$ unless the two cosine functions have their maxima at different values of j. The first cosine has its maximum at $j = 0$ for $-2\pi/N < \omega t + 2\pi(1/N - 1/N^2) < 0$, while the second cosine has its maximum at $j = 0$ for $-2\pi/N < \omega t + 2\pi/N < 0$. Thus $\delta V(t)$ is non-zero within equally spaced narrow time intervals $0 < \omega t + 2m\pi/N < 2\pi/N^2$. The maxima of $\delta V(t)$ occur when $\omega t + 2m\pi/N = \pi/N^2$. It is easy to evaluate equation (12) and verify that

$$\delta V_{\max} = \frac{V_0}{2\sin(\pi/N)}\{\cos(-\pi/N + \pi/N^2) - \cos(\pi/N + \pi/N^2)\} = V_0 \sin(\pi/N^2). \qquad (16)$$

Combining with the result of the previous paragraph, $\Delta V(t)$ has a ripple of height $\pi V_0/(N^2)$ and frequency $N\omega$ and a ripple of height $\pi V_0/(2N^2)$ and frequency $N^2\omega$, superimposed on the DC voltage $N^2 V_0/\pi$.

We now compare the square lattice with N^2 voltage sources to N^2 full-wave rectifiers in series. For a distributed voltage source, it is reasonable to choose the amplitude of the individual sources to scale as $\sim 1/N$, i.e. $V_0 = V_c/N$. Then, the DC voltage for the square lattice is $N V_c/\pi$, compared to $2N V_c/\pi$ for the rectifiers in series. On the other hand, for large N there is only one diode per source instead of four. As mentioned earlier, for a load R_L the maximum current flowing through each diode is $2N V_c/(\pi R_L)$. Similarly, for the square lattice with idealized diodes, the maximum current is $N V_c/(\pi R_L)$ because at any instant the current flows from top to bottom along a unique set of diodes. However, with realistic diodes, the current is distributed over numerous parallel 'channels', reducing the maximum current. (Without numerical simulations, it is not obvious whether the number of channels n is $O(1)$ or $O(N)$.) Thus for the same current flowing through the load resistor, it is easier to exceed the maximum rating of the diodes for rectifiers in series. The maximum voltage across a diode when it is reverse biased is $V_0 = V_c/N$ for the rectifiers in series. For the lattice, the maximum reverse biased voltage can be approximately obtained from the continuum approximation, as $2N V_0/\pi = 2V_c/\pi$. Both of these are well behaved for large N. Finally, the power dissipated in the diodes is non-zero if they are not ideal. Since

$$\begin{aligned} I &= I_s(\exp[V/V_s] - 1) \\ &\approx I_s \exp[V/V_s] \qquad V > 0 \\ &\approx -I_s \qquad V < 0 \end{aligned} \qquad (17)$$

then the power dissipated is

$$\sim \sum_\alpha V_s I_\alpha \ln(I_\alpha/I_s) + \sum_\beta V_\beta I_s, \qquad (18)$$

where the sums run over the forward and reverse biased diodes, respectively. For the lattice, there are $O(N^2)$ reverse biased diodes with $O(1)$ voltages across them, and the power dissipated in them is $O(N^2)$. For the forward biased diodes, if the current flows along n channels, there are $O(nN)$ forward biased diodes each with a current $O(N/n)$ flowing through it. The power dissipated in the forward biased diodes is thus $O(N^2 \ln N)$. By comparison, for the rectifiers in series, there is an $O(N)$ current flowing in $O(N^2)$ forward biased diodes, so that the power dissipated in them is $O(N^3 \ln N)$.

Our results show prefect rectification and breaking of Lorentz reciprocity can be achieved using a nonlinear network consisting of a lattice of AC sources. This work provides an interesting example of an exact result that can be established for an infinite nonlinear network, consisting of ideal bridge rectifiers that are of interest for distributed energy generation. Simulations with realistic diodes confirm the exact results derived here. Importantly, the phase cascade sequence described is independent of frequency, and perfect rectification can be achieved for a wide range of frequencies, which makes it attractive for energy harvesting and distributed energy networks. A fabricated circuit constructed of light emitting diodes and phase cascaded AC sources confirms the results in the paper.

Numerical simulations

Simulations were performed in MATLAB Simulink, using Silicon diodes, with model parameters selected for a General purpose Rectifier (Fairchild 1N4004). The forward voltage was 0.8 V, with an internal resistance of 0.001 Ω, inductance 0. A snubber capacitance of 250 nF., and snubber resistance of 500 Ω were used to suppress
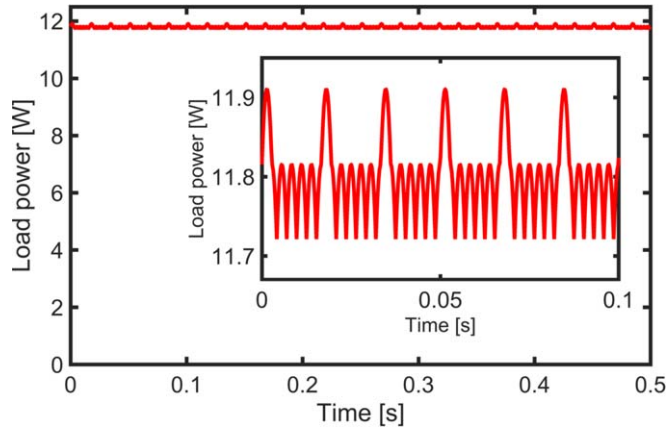
Figure 2. Load resistor power as a function of time for an array of 1N4004 diodes under the conditions indicated in detail in the text. The load resistor value has been set at 1 kΩ. Inset shows an the same time series with an expanded load power scale.
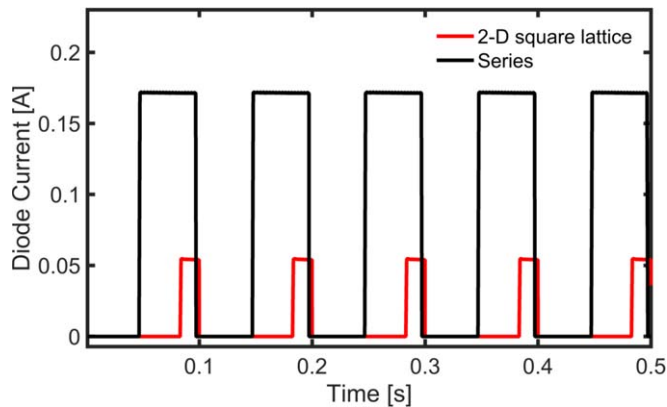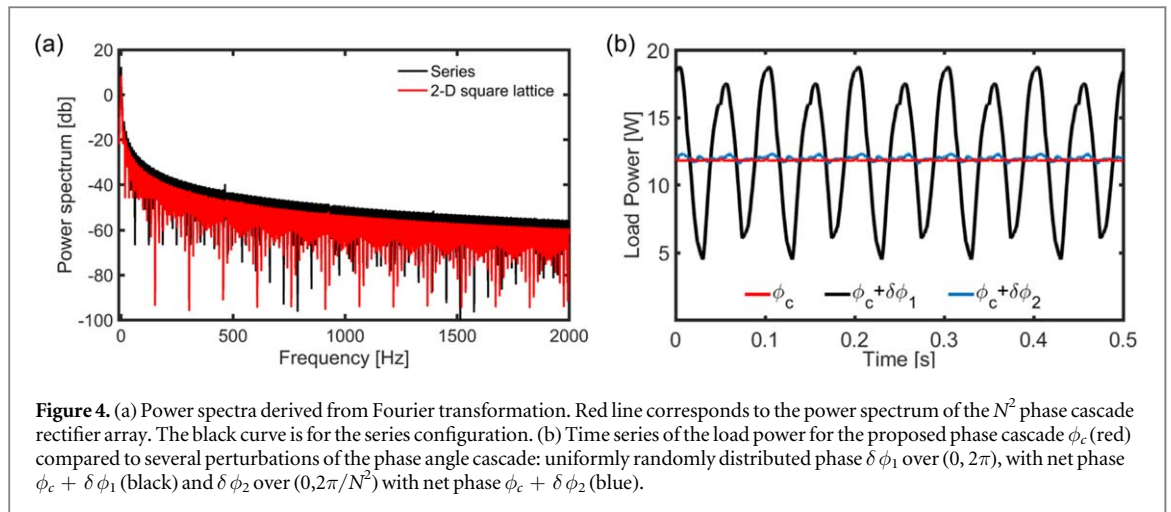

Figure 3. Current through a single selected diode in the series configuration compared to the phase cascade array.

voltage transients, but the values did not affect the steady state results discussed in the paper. More sophisticated models with nonlinear behavior arising from the diode effective capacitance were not considered. Parasitic effects in nonlinear circuits can give rise to non-local behavior affecting time synchronization and generate inhomogenieties in the periodic array. Inhomogeneities in in the electric fields and associated device characteristics have been shown by Xu and Teitsworth [23] to lead to bifurcations and the emergence of multiple current branches. The current is now a multivalued function of the driving voltage and the response is history dependent. Such effects are important in a variety of complex electronic systems [23] ranging from semiconductor superlattices [24] to quantum cascade lasers [25], but were not considered in our steady state analysis of a network circuit for power production. In our simulations, the amplitude of the AC sources was set at 10 V, and the frequency was set to 10 Hz, driving a load a 1 kΩ load resistor. Current probes were used to measure the load current, and the current and voltage difference across selected diodes and AC power sources. The load current was used to derive the load power. The lattice sizes were varied from $N^2 = 1$ to a maximum of $N^2 = 64$. Shown in figure 2 are the results of the simulation of the power for the 2-D square lattice with the Phase cascade array.

The simulations were used to calculate the representative duty cycle of the phase cascade array and compared to the series configuration, as shown in figure 3. It is evident that in the phase cascade array, the peak current is lower, and the duty cycle also lower than in the series configuration, reducing both thermal load and easing the limits on the forward current. One figure of merit is the efficiency of the phase cascade array estimated by considering the power delivered to the load compared to the power supplied to the sources. Fast Fourier transforms of the time series were used to calculate the power spectrum in the load resistor. Figure 4(a) shows a comparison of the power spectrum for the phase cascade array compared to the series configuration. The first consideration is the fraction of the power supplied to the load resistor compared to the total input power supplied by all the sources. For an ideal diode array, the efficiency is 1, but for the circuit shown in figure 1(a) with realistic diodes, the efficiency was 0.945 ± 0.005. A second perhaps more relevant figure of merit is the

Figure 4. (a) Power spectra derived from Fourier transformation. Red line corresponds to the power spectrum of the N^2 phase cascade rectifier array. The black curve is for the series configuration. (b) Time series of the load power for the proposed phase cascade ϕ_c (red) compared to several perturbations of the phase angle cascade: uniformly randomly distributed phase $\delta\phi_1$ over $(0, 2\pi)$, with net phase $\phi_c + \delta\phi_1$ (black) and $\delta\phi_2$ over $(0, 2\pi/N^2)$ with net phase $\phi_c + \delta\phi_2$ (blue).

noise-to-signal, or the relative standard deviation. The mean load power $\bar{P}$ and standard deviation σ_P for the 6×6 phase cascade array was 11.79 ± 0.05 W, corresponding to a coefficient of variation of $\sigma_v \equiv \bar{P}/\sigma_P \sim 0.4\%$, for the 6×6 array even in the absence of any filters. The question of how time synchronization affects the performance of the proposed phase cascade array circuit was addressed by adding random phase noise $\delta\phi$ to the cascaded phase ϕ_c of each source. Figure 4 (b) shows the time series of the load power for several realizations $\{\delta\phi\}$ of random phase noise configurations. In a lattice of random phase angles distributed uniformly over $(0, 2\pi)$ significant power now appears at all harmonics at the expense of DC power, as expected. The load power for the random phase configuration was 12.03 ± 4.66 W, with $\sigma_v \sim 39\%$ showing an enormous increase in the relative standard deviation. For configurations in which the phase noise is distributed uniformly randomly over a narrow range $(0, 2\pi/N^2)$ and then added to the fixed phase angle in Eq(3), the load power was found to be 11.93 ± 0.16 W, with $\sigma_v \sim 1.3\%$. The results suggest that the phase cascade is robust against small local phase angle variation. For ideal diodes in an infinite phase cascade array, the efficiency will tend to 1 as expected from the exact analytical results obtained in this paper.

Acknowledgments

ORCID iDs

S Erramilli ● https://orcid.org/0000-0003-3950-9122

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