Micro-Energy Harvesting System including a PMU and a Solar Cell on the same Substrate with Cold Start-Up from 2.38 nW and Input Power Range up to 10 ?W using Continuous MPPT

Esteban Ferro, Víctor Manuel Brea, Paula López and Diego Cabello

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***Abstract*—This paper presents a Power Management Unit (PMU) powered by a 1 mm^2 solar cell on the same substrate to rise up the harvested voltage above 1.1 V. The on-chip solar cell and the PMU are fabricated in standard 0.18 μm CMOS technology achieving a form factor of 1.575 mm^2. The PMU is able to start up from a harvested power of 2.38 nW without any external kick off or control signal. The PMU features a continuous and two-dimensional Maximum Power Point Tracking (MPPT) working in open-loop mode to handle a harvested power range from nW to μW, by modifying both the charge pump topology and the switching frequency. The MPPT is based on four voltage level detectors that define five working regions depending on the illumination and on a self-tuning reference current for a fine adjustment of the switching frequency. The chip also includes an auxiliary charge pump to generate the voltage level necessary for the control circuit, implemented as a Pelliconi charge pump of 8 stages with NMOS transistors in P-well as diodes. A Dickson charge pump with transmission gates as switches and with variable gain and capacitance per stage is also designed as the main charge pump. Finally, two relaxation oscillators are implemented to drive both charge pumps. This paper is accompanied by a video file demonstrating the PMU operation by powering an off-chip NAND gate.**

***Index Terms*—Energy harvesting, DC-DC power conversion, PMU, On-Chip Solar Cell, Analog MPPT.**

I. Introduction

MICRO-energy harvesting has become an extended solution for low maintenance, small size and battery-less systems, such as implantable devices [1]–[3], wearable computing [4] or smart dust wireless sensors [5]. In [6] it is claimed that light is the energy source with the greatest harvesting power density and some recent research has demonstrated the solar micro-energy harvesting to be a viable solution [1], [2]. As Fig. 1 depicts, the classical approach of light energy harvesting consists of an off-chip solar cell stuck over a CMOS chip with a Power Management Unit (PMU) [1]. Nevertheless, by integrating the solar cell and the CMOS circuitry on the same silicon substrate, a very small form factor and reduced cost can be met [7]. This approach, however, leads to several design challenges of the PMU.

First, the scavenged power can be as low as a few nW for on-chip solar cells, making it hard to work with such low power levels without external control signals or start-up mechanisms [7], [8]. Also, the voltage generated by micro-energy harvesting systems is usually not high enough for the accompanying processing circuits. Admittedly, there are solutions with photodiodes working as solar cells to provide the power supply of processing circuits on the same substrate, [2], [9], but in general, the generated voltage is too low. A direct solution can be to stack photodiodes in order to obtain a higher voltage level. Nevertheless, this solution implies a decrease in the efficiency for standard CMOS technologies [10]. Other solution to address this problem is to use either inductive or capacitive DC-DC converters. The former are attractive because of their high efficiency [11]–[13], however, they are not widely used because of the poor quality of integrated inductors in standard CMOS technologies [14]. On the other hand, capacitive DC-DC converters or charge pumps are particularly attractive because they can be fully integrated with a relatively small form factor [7], [15]–[17]. This is the solution adopted in this work.

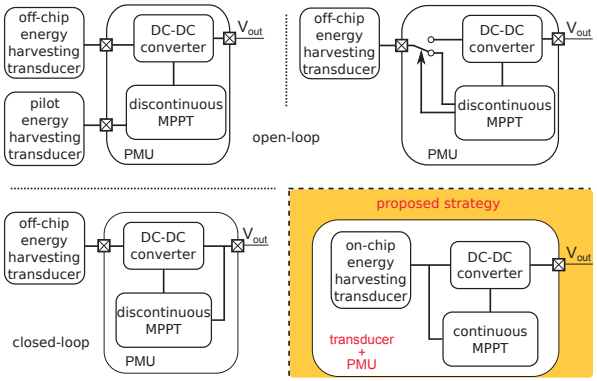

Fig. 1. Conventional energy harvesting strategies (top and bottom left) and proposed energy harvesting strategy (bottom right).

Another design challenge is to handle a large input power range [12], [15]. This is necessary to use the energy harvested by the photodiode under very different illuminations implying a change in the illumination, like indoor or outdoor locations. Taking as reference an on-chip solar cell of 1 mm^2, the input power can vary from a few nW to several μW for an illumination range from 100 lx to 100 klx [18]. This demands an efficient PMU with Maximum Power Point Tracking (MPPT) consuming only a few nW to transmit the maximum possible

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power from the photodiode to the load. The works in [16], [19], [20] are examples of PMUs which do not include neither the transducer on the same substrate nor MPPT capability, making it difficult to manage such a large input power range. Conversely, in [7] a system which includes a transducer and a PMU on the same substrate is presented, however, it does not include the MPPT capability.

As Fig. 1 also shows, two main conventional ways to perform the MPPT can be distinguished: closed-loop and open-loop [21]. The first one implements algorithms such as hill climbing where the PMU input impedance is adjusted step by step to reach the optimal point depending on the PMU output, which is measured discontinuously to reduce power consumption at the cost of a slow response to rapid input variations [17], [22]–[24]. The second approach is based on current or voltage measurements of the photodiode without taking into account the PMU output. This approach is less complex than the former, reducing the power consumption at the cost of less accuracy in the MPPT. Some examples of the open-loop approach are the algorithm proposed in [25] or the fractional open circuit voltage method (FOCV) [15], [26]. The latter consists of measuring the open circuit harvested voltage either by disconnecting the main transducer from the PMU and thus decreasing the PMU input power, or by using a pilot transducer, resulting in a larger form factor, with the goal of modifying the PMU input impedance to match photodiode and PMU impedances. Instead, as Fig. 1 shows, our approach performs an open-loop and continuous MPPT without disconnecting the photodiode from the PMU, overcoming the above limitations.

This paper presents a PMU powered by a 1 mm^2 on-chip solar cell to rise up the harvested voltage to an output voltage higher than 1.1 V, suitable for powering low-power circuits. This chip is intended for charging either on-chip or off-chip capacitors as energy reservoirs. Our approach can be of interest for applications such as implantable devices, which demand long-time maintenance cycles along with the capability of handling low and wide input power ranges. The key contributions of this work are: 1) an on-chip solar cell and a PMU fabricated on the same substrate in standard 0.18 µm CMOS technology; 2) a PMU starting up from a harvested power of 2.38 nW without any external kick off or control signal and 3) a continuous and two-dimensional MPPT which works in open-loop mode, where the charge pump topology and the switching frequency are modified, handling an input power range from nW to µW.

The different sections of the paper are organized in a top-down structure. Section II describes the proposed architecture of the on-chip solar cell and the PMU. Section III addresses the different circuits of the system. Section IV shows experimental results. Finally, the main conclusions are drawn in Section V.

II. Proposed Architecture

Fig. 2 shows the proposed architecture for the micro-energy harvesting system. The architecture is designed to work properly from nW to µW of input power without any external control signals or start-up mechanisms. An on-chip solar cell is the only power source of the system. It consists of a P$^+$ over P-well in N-well over P-substrate of 1 mm^2. The solar cell is connected directly to the PMU without an input capacitor in order to save area. The PMU comprises an auxiliary oscillator driving an auxiliary charge pump which acts as DC-DC converter to generate the voltage of the control circuit and the main charge pump switches. Two different operation phases can be distinguished in the PMU: start-up and normal operation. The circuits of the PMU working in normal operation are labeled NO in Fig. 2. Similarly, circuits working in both start-up and normal operation are labeled ST/NO. The main oscillator and DC-DC converter are OFF during the start-up process by means of power-gating to decrease energy consumption. The auxiliary DC-DC converter starts working when the voltage generated by the photodiode, V_{PD}, is high enough to switch on the auxiliary oscillator and to trigger the start-up process. The output voltage of the system, V_{out}, is provided by the main DC-DC converter, which rises up the voltage generated by the photodiode to a voltage level above 1.1 V during the normal operation phase of the PMU. Charge can be stored in a capacitor at V_{out} level in order to power an on- or an off-chip load. The clock signals needed by the main charge pump are provided by the main oscillator. The MPPT block tunes the main charge pump topology and the frequency of the auxiliary and the main oscillators.

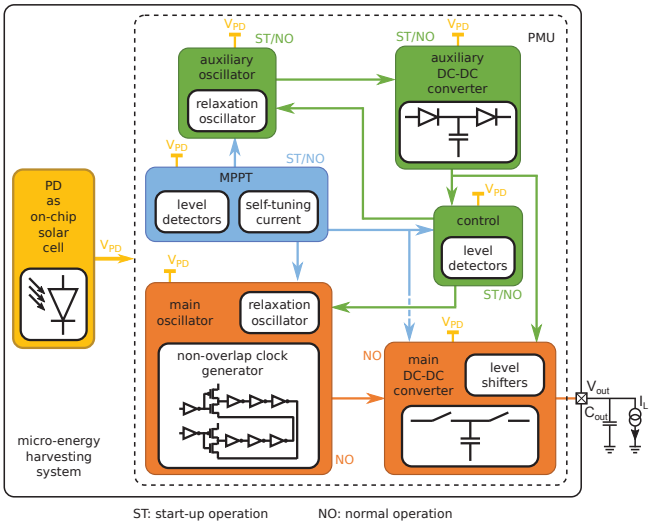


Fig. 2. Architecture of the proposed micro-energy harvesting chip which includes a PMU and an on-chip solar cell on the same substrate.

A. MPPT Architecture

The MPPT block works in open-loop, continuous and two-dimensional mode, so it is always connected to the photodiode to determine different working regions according to the illumination. In other words, the voltage harvested by the photodiode defines the working regions. Our MPPT approach is inspired by the FOCV method since the maximum power point is tracked through the photodiode voltage. Nevertheless, in our case the PMU is not disconnected from the photodiode, i.e. we do not measure the photodiode open circuit voltage. The MPPT block is designed to meet the maximum PMU efficiency

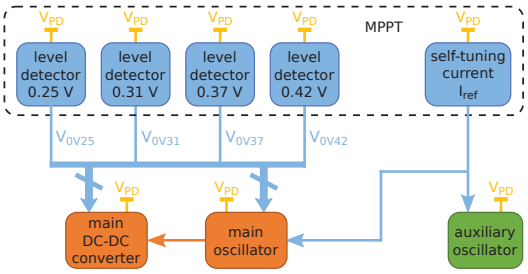


Fig. 3. MPPT architecture for the proposed chip.

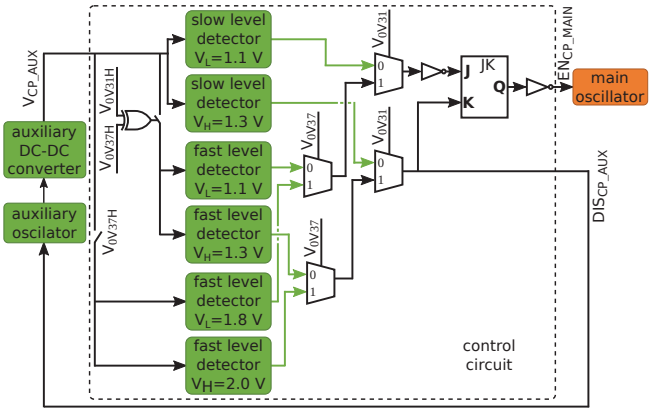


Fig. 4. Control circuit for the proposed chip.

adjusting both the gain and the capacitance per stage of the main charge pump and the clock signals' frequency of both charge pumps. A joint analytical model of photodiode and charge pump developed by the authors in [18], [27] is used to predict the photodiode response for every working region, searching for the maximum load ($I_{L_{MAX}}$) which yields 1.1 V at the PMU output during the design phase. So, our MPPT method can be regarded as a lookup table defined in the design phase. Current experimental measurements will be used to improve the joint model that it was originally extracted from the doping profiles provided by the technology manufacturer to get a more accurate MPPT. This MPPT strategy leads to ultra-low power consumption as it will be shown in Section III-F.

The MPPT architecture shown in Fig. 3 is powered directly and permanently by the on-chip solar cell. Five different working regions are defined by simulation in the design phase for the MPPT to cover the input voltage range of the photodiode, so four level detectors are designed to distinguish among the five working regions (WR1-WR5). The level detectors have a digital output which is high when V_{PD} is above the trigger voltage. Exhaustive Montecarlo simulations were run to avoid overlapping voltage detections. The nominal trigger voltages are indicated in Fig. 3 and were finally set to 0.25 V, 0.31 V, 0.37 V and 0.42 V. The level detectors set the gain and the capacitance per stage of the main charge pump and the frequency of the main oscillator. Finally, a self-tuning reference current, I_{ref}, biased by V_{PD}, adjusts the frequency of the auxiliary oscillator and it also performs a fine tuning of the frequency of the main oscillator independently of the working region, and thus independently of the charge pump topology, as it will be addressed in Section III-D.

B. Control Architecture

Fig. 4 shows the architecture of the control circuit. The control circuit limits the output voltage of the auxiliary charge pump, V_{CP_AUX}, to avoid increasing power consumption and very high voltage levels which could damage transistors. It also determines when the auxiliary and main oscillators and charge pumps are ON through power gating.

In order to perform the above tasks, two different threshold voltage levels in signal V_{CP_AUX}, V_L and V_H, are set through voltage level detectors. The values of V_L and V_H depend on the illumination. Their nominal values have been designed to be 1.1 V and 1.3 V, respectively, for low and medium illuminations (working regions WR1-WR3), and 1.8 V and 2.0 V for high illumination (working regions WR4-WR5). The reason to work with higher voltage levels for high illumination is to decrease the conduction losses in the switches of the main charge pump. To further increase the efficiency we optimized the trade-off between consumption and detection speed, so that for low illumination we designed slow and very low-power level detectors (WR1-WR2), whereas the opposite for medium and high illumination (WR3-WR5). A summary of the different types of level detectors in the control block is shown in Table I.

TABLE I
VOLTAGE LEVEL DETECTORS IN THE CONTROL BLOCK

Illumination	Working region	Speed	V_L (V)	V_H (V)
low	WR1 - WR2	slow	1.1	1.3
medium	WR3	fast	1.1	1.3
high	WR4 - WR5	fast	1.8	2.0

Regarding the circuits managed by the control block, the auxiliary oscillator, and consequently the auxiliary DC-DC converter, are OFF when $V_{CP\_AUX} > V_H$, limiting the voltage V_{CP_AUX}. A memory block based on an asynchronous JK flip-flop composed of four NAND gates was also included in the control circuit to discriminate between start-up and normal operation. The main oscillator is OFF during the start-up process until $V_{CP\_AUX} > V_H$ in order to cut power during the start-up process. In normal operation, the main oscillator is ON while $V_{CP\_AUX} > V_L$. If $V_{CP\_AUX} < V_L$, the main oscillator is turned OFF until $V_{CP\_AUX} > V_H$ again.

C. Oscillators and DC-DC Converters

As Fig. 2 shows, two oscillators are needed to drive the two charge pumps in our design. The auxiliary oscillator has a variable oscillating frequency controlled only by V_{PD}, while the frequency of the main oscillator is controlled by both V_{PD} and the MPPT level detectors. The only supply voltage of the oscillators comes from V_{PD}, which shows an exponential relationship with the photogenerated output current. Therefore, the main design constraint for the configuration of the oscillators is to have very low power consumption and to work at the point of the IV curve of the photodiode with the highest voltage for a given incident illumination power. With this approach, the system is able to start up autonomously

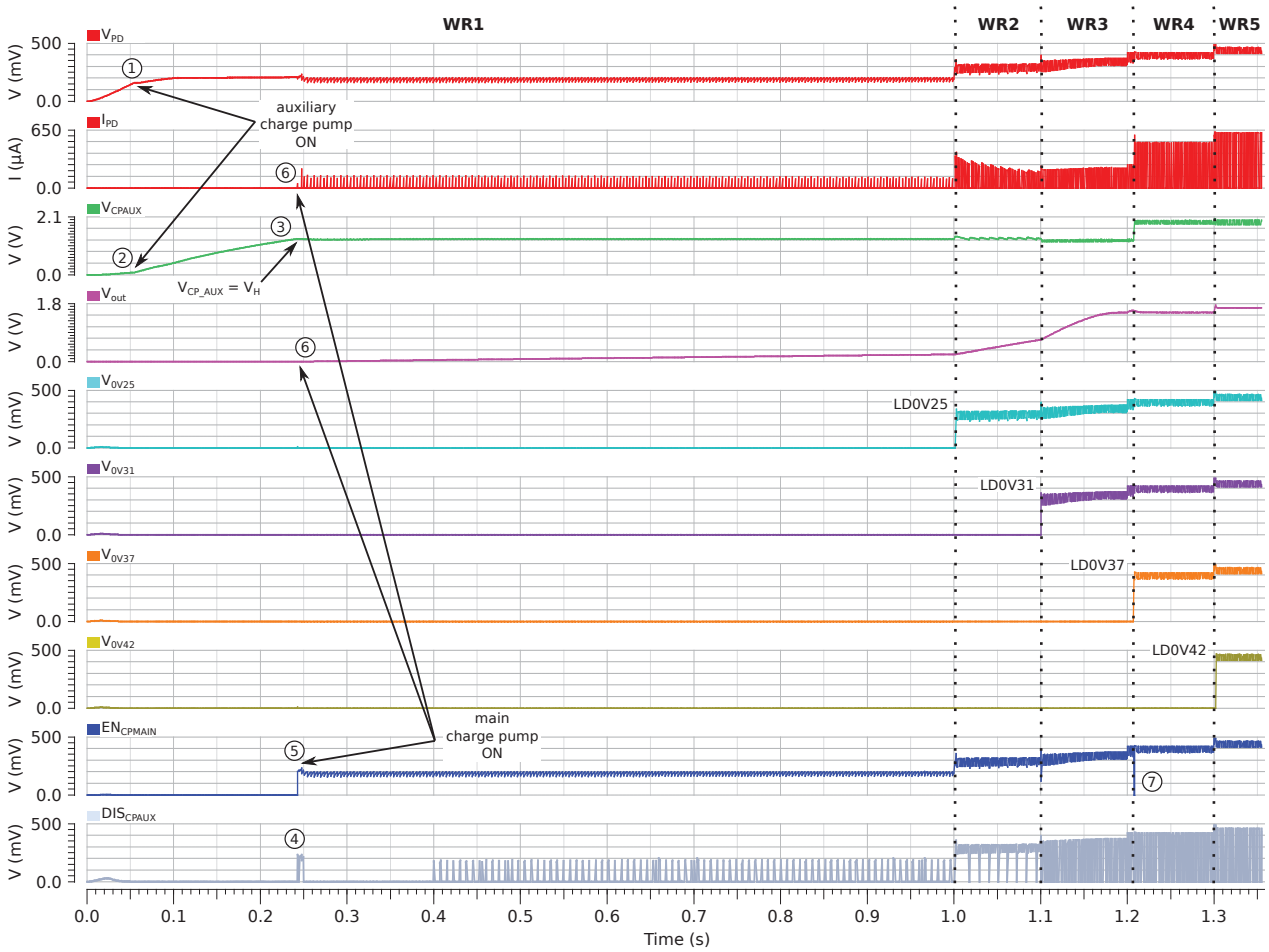


Fig. 5. Electrical simulation of the start-up process, level detectors (LD) and control operation. ①: V_{PD} reaches 0.17 V. ②: Auxiliary charge pump ON. ③: V_{CPAUX}=V_H. ④: DIS_{CPAUX} ON. ⑤: EN_{CPMAIN} high. ⑥: Main charge pump ON. ⑦: Transition from WR3 to WR4.

(cold start-up) even from very low illumination levels without any specific start-up circuit. Regarding the converters, the auxiliary converter has a fixed topology, while the MPPT block sets the gain and the capacitance per stage of the main converter. Finally, the switches of the main charge pump driven by the control and clock signals are implemented as NMOS transistors and transmission gates. As the voltage generated through the different stages of the main charge pump is higher than the digital output level of the control and clock signals, i.e. V_{PD}, the level shifters are designed to rise it up to V_{CP_AUX}.

D. System Operation

In order to illustrate the working principle of our architecture, an electrical simulation that includes the start-up process and the MPPT and control circuit operation extracted directly from the CAD suite is shown in Fig. 5. The target technology is standard 0.18 µm CMOS and the photodiode is introduced in the CAD simulator as an electrical model following [18]. At the beginning there is no illumination, so $V_{PD} = 0$. Then the illumination is increased and when V_{PD} crosses 0.17 V, ① in Fig. 5, the auxiliary oscillator, and consequently the auxiliary DC-DC converter, start working in WR1, ② in Fig. 5. This voltage value is enough to activate the auxiliary oscillator without any specific circuitry to start-up. Consequently, V_{CP_AUX} reaches V_L (1.1 V for low illumination) triggering the slow V_L level detector in the control circuit, while the memory block keeps EN_{CPMAIN} low, so the main charge pump is OFF. When V_{CP_AUX} reaches V_H (1.3 V for low illumination), the slow V_H level detector is triggered and the memory block enables the main oscillator and converter by changing EN_{CPMAIN} from low to high. These events are marked as ③, ⑤ and ⑥ in Fig. 5. The V_H level detector in the control circuit also limits the level of V_{CP_AUX} by disconnecting the auxiliary oscillator and the auxiliary charge pump with signal DIS_{CPAUX} ON (④ in Fig. 5). DIS_{CPAUX} will be OFF again when $V_{CP\_AUX} < V_H$ in order to activate the auxiliary charge pump to increase V_{CP_AUX} again, acting as a regulator of the level of V_{CP_AUX}. After the start-up and during normal operation the main oscillator and converter are maintained ON while the V_L level detector is high. As the illumination increases, the first level detector of the MPPT block is triggered at $V_{PD} = 0.25$ V, entering a new MPPT working region (WR2). A further increase of V_{PD} triggers the second level detector of the MPPT at $V_{PD} = 0.31$ V entering WR3, enabling the fast level detectors of the control circuit and maintaining V_{CP_AUX} below $V_H = 1.3$ V. If the illumination increases further, when $V_{PD} = 0.37$ V the third level detector of the MPPT block is triggered, entering WR4, setting up

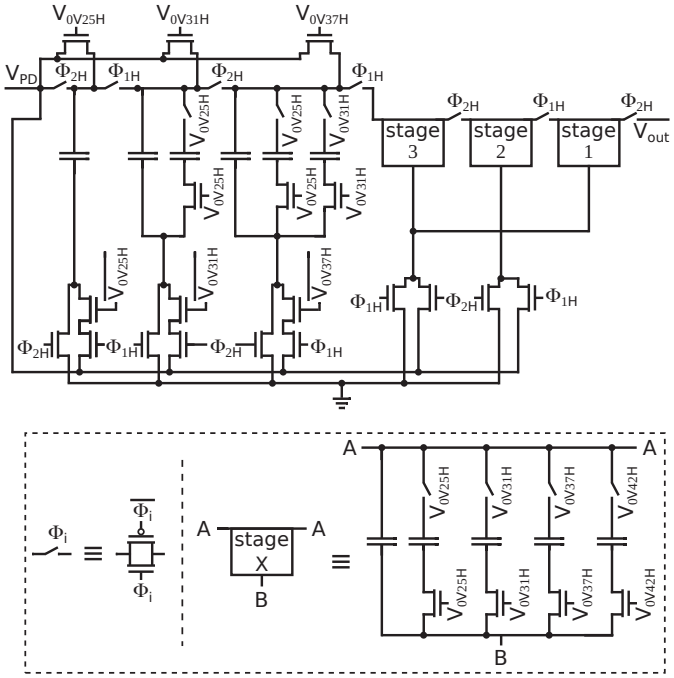


Fig. 6. Schematic of the main charge pump.

TABLE II
CONFIGURATION OF THE MAIN CHARGE PUMP

Working region	Gain	Capacitance per stage (pF)
WR1	7×	100
WR2	6×	200
WR3	5×	400
WR4	4×	600
WR5	4×	750

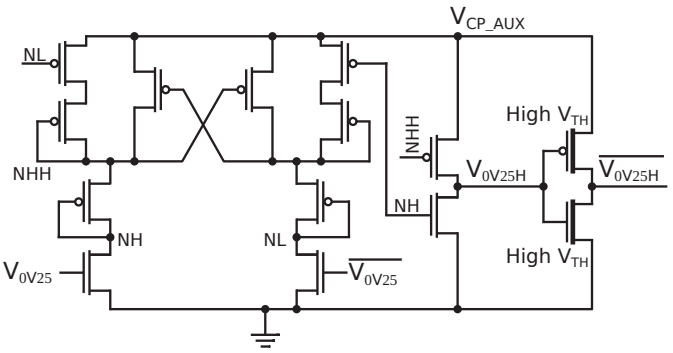


Fig. 7. Schematic of a level shifter.

V_{CP_AUX} below $V_H = 2.0$ V. At this point (⑦ in Fig. 5), EN_{CPMAIN} is turned low until V_{CP_AUX} reaches $V_H = 2.0$ V. Finally, for very high illumination, the last level detector of the MPPT block is triggered at $V_{PD} = 0.42$ V, entering WR5.

Fig. 5 also shows the input current of the PMU, I_{PD}. The shape of this current shows pulses with the same frequency as that of the main oscillator, as the main charge pump is the most power hungry block. The height of these pulses changes with the working region as the MPPT block adapts the input impedance of the PMU to match the impedance of the photodiode. As it is shown above, this is accomplished by measuring V_{PD} using four level detectors and a self-tuning reference current.

Finally, as expected, the output voltage of the level detectors oscillates around the trigger voltage that separates working regimes, leading to a loss in the end-to-end efficiency. This could be minimized using hysteresis, but this might lead to a decrease in the efficiency throughout the illumination range and not just at the transitions between working regions as four additional level detectors and additional control circuitry would be needed. Also, it would increase the area and the power needed to start-up. For this reason its use has been discarded in this approach.

III. CIRCUIT IMPLEMENTATION

A. Main Charge Pump

The voltage generated by the on-chip solar cell is risen up by the main charge pump, which provides the output of the system. The main DC-DC converter is based on a Dickson charge pump [28] with transmission gates as switches and with variable gain and capacitance per stage. The two non-overlapping clock signals needed by the converter are generated by the main oscillator. The control signals to modify the structure of the converter are provided by the level detectors of the MPPT block.

Fig. 6 depicts the schematic of the main charge pump. The gain and the capacitance per stage were designed with the circuit models introduced by the authors in [18], [27]. Table II summarizes the gain and the capacitance per stage of the main charge pump for the different working regions. These values are set by the MPPT circuit according to the voltage V_{PD} provided by the on-chip solar cell. Regarding the capacitors implementation, the stages that are active for high illumination are implemented with PMOS transistors (PCAPs) as capacitors in order to reduce area, while the stages that are active for low illumination have PCAPs and Metal Insulator Metal capacitors (MIMs) connected in parallel as capacitors in order to reduce leakages.

Finally, level shifters based on [29] are designed to make the voltage level of the control and clock signals suitable for the main charge pump switches, rising it up to the V_{CP_AUX} level. To optimize the trade-off between speed and power consumption, two different types of level shifters are designed by modifying the size of the transistors. Slow and low power consumption level shifters are designed for the control signals and faster and higher power consumption level shifters are implemented for the clock signals. Fig. 7 shows an example of schematic of a level shifter, in particular the level shifter for the MPPT level detector with trigger voltage of 0.25 V. High-V_{TH} transistors are chosen in order to reduce both area and power consumption in the last inverter. Signals V_{0V25H}, V_{0V31H}, V_{0V37H} and V_{0V42H} refer to high level voltage signals provided for the main charge pump. The same nomenclature is used with clock signals ϕ_{1H} and ϕ_{2H} in the main charge pump and in the control block with signals V_{0V31H} and V_{0V37H} (Fig. 4). Finally, in order to avoid clutter we label the inner nodes of the level shifter shown in Fig. 7 as NL, NH and

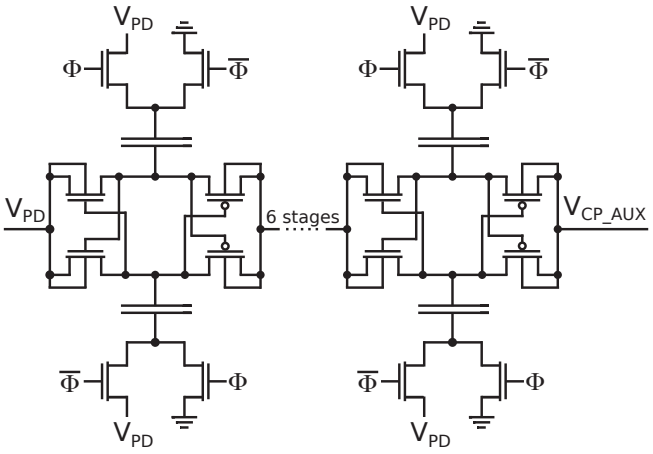


Fig. 8. Schematic of the auxiliary charge pump.

NHH.

B. Auxiliary Charge Pump

The auxiliary charge pump schematic is shown in Fig. 8. It is a Pelliconi charge pump [30] of 8 stages with NMOS transistors in P-well as diodes to avoid the substrate effect in order to increase the efficiency of the converter, and thus, that of the start-up process. The capacitors are implemented as MIM capacitors to maintain low leakage current. The clock signal is generated by the auxiliary oscillator. The converter has a fixed gain and capacitance per stage, so the frequency of the clock signal is the only way to adjust the output power of the converter depending on the illumination.

C. Oscillators

Two oscillators are designed to drive the auxiliary and main converters independently as the output power required by both converters is not the same. Both oscillators are relaxation oscillators without any specific start-up circuit.

The main oscillator consists of a relaxation oscillator based on [31] with a variable oscillation frequency. As Fig. 9 depicts, different branches with different capacitor sizes are designed to adjust the oscillating frequency. These branches are driven by the level detectors of the MPPT block. The frequency can also be controlled by means of the bias voltage, V_{BIAS}, so that a self-tuning reference current which depends on V_{PD} is designed to generate V_{BIAS} for a fine tuning of the oscillating frequency as it will be shown in Section III-D. The total frequency obtained by combining the two methods varies continuously from 100 Hz to 150 kHz. Finally, a non-overlapping clock generator [32], also shown in Fig. 9, is added to drive the main charge pump.

The auxiliary oscillator in Fig. 10 is a relaxation oscillator with the same topology introduced in [31]. In our case, we have adjusted the dimensions of the transistors for very low power applications and the oscillating frequency is controlled by only the same V_{BIAS} as in the main oscillator, designed to vary from 1.5 kHz to 500 kHz.

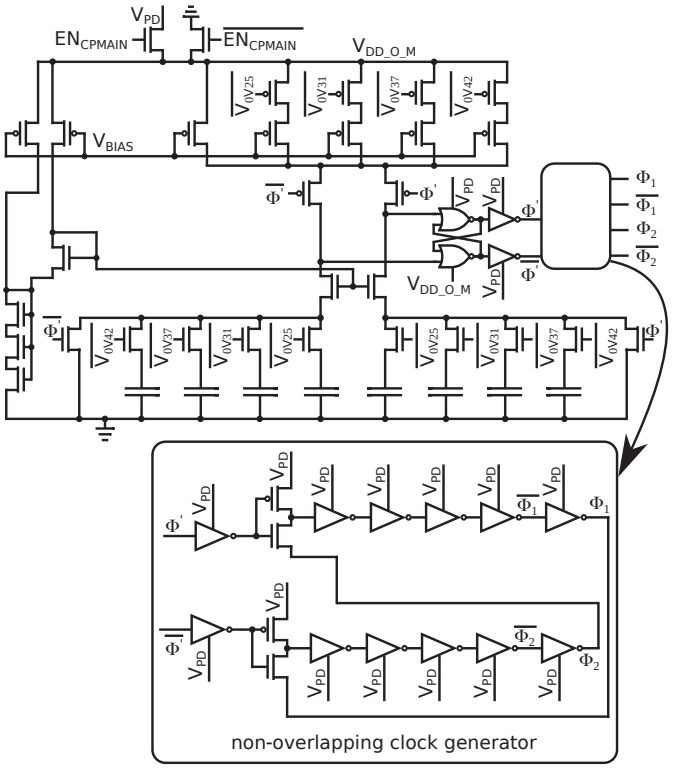


Fig. 9. Schematic of the main oscillator.

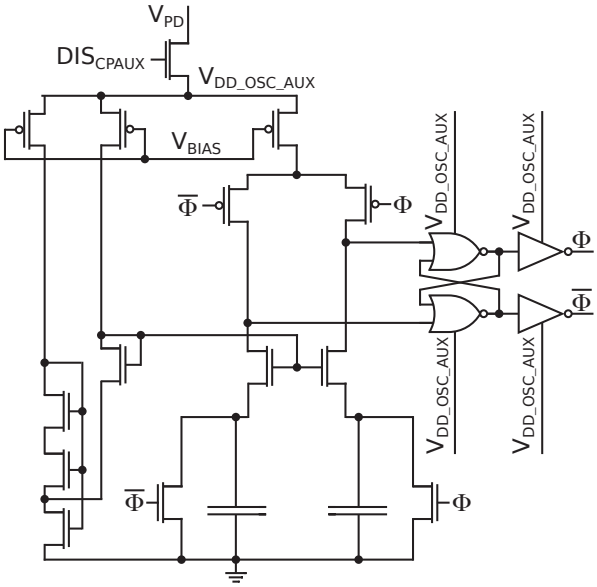


Fig. 10. Schematic of the auxiliary oscillator.

D. MPPT Circuits

The MPPT block generates the signals which adjust the system topology in order to follow the maximum power point of the photodiode. This block controls the gain and the capacitance per stage of the main charge pump and the frequency of both oscillators. The MPPT block comprises four level detectors and a self-tuning reference current.

Regarding the level detectors, the trigger voltage of each one is set by a PMOS cascode structure [33] and is determined

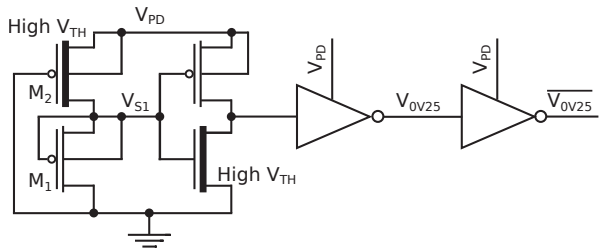
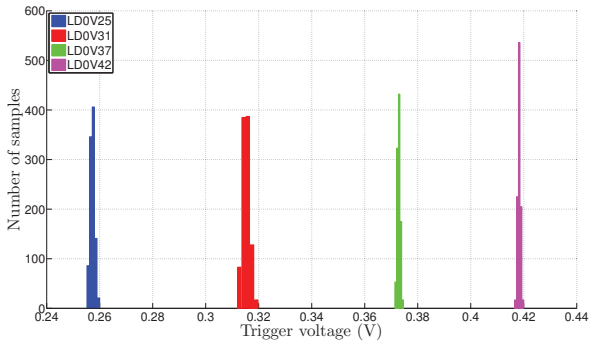
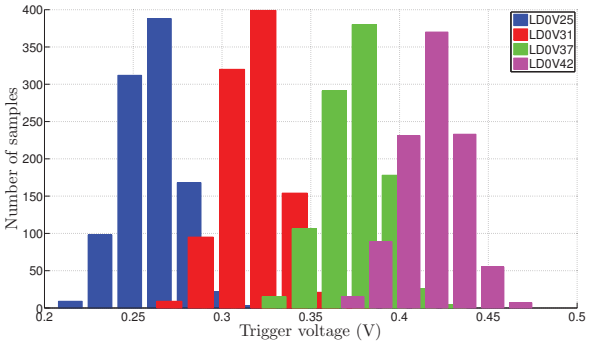


Fig. 11. Schematic of a level detector of the MPPT block with different threshold voltage transistors.



(a)



(b)

Fig. 12. Montecarlo simulations of the MPPT block level detectors (LD) for mismatch variations in (a) and for process variations in (b).

by comparing the currents through transistors M_1 and M_2 in Fig. 11. Since $V_{PD} < 0.5$ V, the transistors in this structure operate in subthreshold region with $V_{DS} > 0.1$ V, so the current though M_2 can be approximated by (1), where k is the Boltzman constant, μ is the hole mobility, C_{ox} is the gate oxide capacitance per area, n is the subthreshold swing coefficient and $\frac{kT}{q}$ is the thermal voltage. Regarding the current through M_1, it is constant and it can be expressed by (2) as the source and the gate of M_1 are short-circuited ($V_{GS} = 0$ V). The trigger voltage V_{tg} is defined as the value of V_{PD} which makes V_{S1} change from low to high and it happens when $I_2 = I_1$, (3). From (3) we can see that V_{tg} can be set by adjusting the dimensions of the transistors and also by using transistors with different threshold voltages. Regular-V_{TH} and high-V_{TH} transistors were chosen (see Fig. 11). Numerical methods for non-linear equations were used to solve (3) in order to find the appropriate dimensions of the transistors, with values shown in Table III.

TABLE III
SIZE IN µM OF THE TRANSISTORS OF THE MPPT LEVEL DETECTORS

V_{tg} (V)	M_1 (W/L) (µm)	M_2 (W/L) (µm)
0.25	27/10	25/14
0.31	29/10	14/31
0.37	38/3	7/31
0.42	47/3	3.5/43

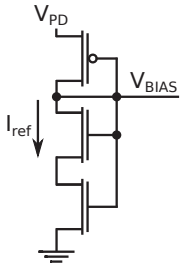


Fig. 13. Schematic of the self-tuning current circuit which provides V_{BIAS} to both oscillators.

$$I_2 = \mu C_{ox} \left(\frac{kT}{q}\right)^2 \frac{W_2}{L_2} e^{q\frac{V_{PD}-V_{TH2}}{nkT}} \quad (1)$$

$$I_1 = \mu C_{ox} \left(\frac{kT}{q}\right)^2 \frac{W_1}{L_1} e^{q\frac{-V_{TH1}}{nkT}} \quad (2)$$

$$\frac{W_2}{L_2} e^{q\frac{V_{tg}-V_{TH2}}{nkT}} = \frac{W_1}{L_1} e^{q\frac{-V_{TH1}}{nkT}} \quad (3)$$

An inverter with transistors of different nominal threshold voltages was also designed for a fine adjustment of V_{tg}. Two additional inverters sharpen the transition between MPPT working regions. In Fig. 12, 1000 Montecarlo runs of the MPPT block level detectors at room temperature (25°C) are shown. To assure non-overlapping voltage detections, Montecarlo simulations taking into account only mismatch variations were run in Fig. 12(a). The mean trigger voltages for each level detector and their standard deviations are 0.257±0.00086 V, 0.315±0.0013 V, 0.373±0.00057 V and 0.418±0.00049 V, providing five well defined working regions. Fig. 12(b) shows the large variability of V_{tg} due to process variations. However, as it will be shown in Section IV, experimental results have demonstrated that the variations in V_{tg} from one die to another due to fabrication defects are not so large and they do not have a substantial effect in the end-to-end efficiency of the system. Regarding the non-overlapping voltage detections, although it may appear that there is an overlap of trigger voltages in Fig. 12(b), this is not the case as all the transistors parameters are changed in the same direction because process variations affect all the transistors in the same way.

On the other hand, a self-tuning reference current shown in Fig. 13, I_{ref}, which changes with the illumination through V_{PD}, was developed to adjust the frequency of both oscillators through the bias voltage, V_{BIAS}. I_{ref} is designed to vary from 50 pA for $V_{PD} = 0.2$ V up to 4 nA for $V_{PD} = 0.5$ V.

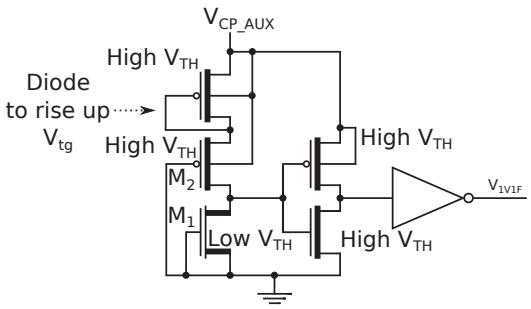


Fig. 14. Schematic of a fast level detector of the control block with different threshold voltage transistors.

E. Control Circuits

The control block limits the level of V_{CP_AUX} and manages the power supply of both oscillators and consequently, of both converters. The control block is based on six different level detectors following the same design procedure as in the MPPT block (Section III-D). The trigger voltages of the detectors are V_L and V_H, whose values depend on the illumination as explained before. Fig. 14 shows a level detector of the control block. A transistor connected as a diode is added to rise up the trigger voltage to maintain the dimensions of transistors M_1 and M_2 at acceptable values. Also, high-V_{TH} transistors are used for the following inverter in order to reduce power consumption. Finally, in the case of the fast detectors, M_1 is implemented as a low-V_{TH} transistor to increase the detection speed.

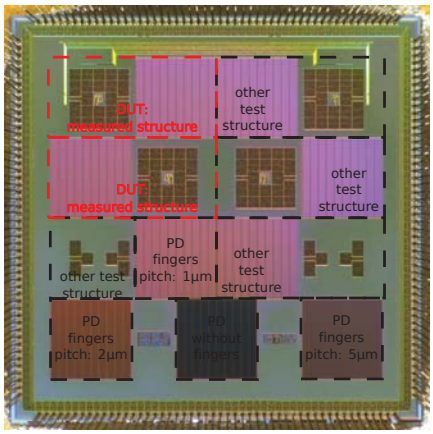
F. Power Breakdown

This subsection analyses the power distribution of the different blocks presented in the previous subsections. Electrical simulations were run including parasitic capacitances of the flying capacitors of both charge pumps for a more realistic power estimation. Parasitic capacitances of 10% and 5% of the flying capacitor values for bottom and top parasitic capacitances, respectively, were assumed [18], [27].

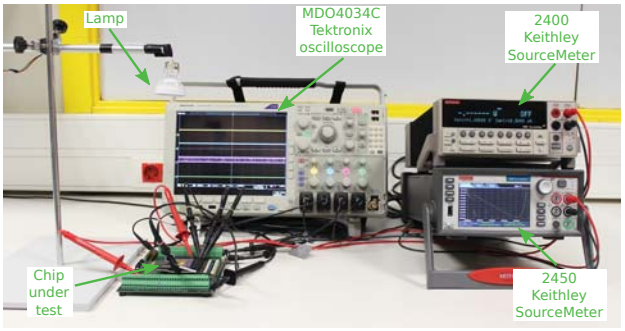
Table IV shows the power breakdown for the five working regions. The consumption of each block is shown as a percentage of the power consumed by the PMU, i.e., as a percentage of the difference of the average PMU input power minus the PMU output power. In WR1, with a PMU consumed power of 3.7 nW, the auxiliary charge pump consumes more than 60%. However, for the other working regions, the main DC-DC converter is the most power hungry block. These data show that the end-to-end efficiency of the whole system is limited by the main charge pump.

IV. Experimental Results

The system was designed and fabricated in standard 0.18 µm CMOS technology, achieving a form factor of 1.575 mm^2. Fig. 15(a) shows a photograph of the 5×5 mm^2 micro-energy harvesting chip, which includes different structures for testing. Different photodiode configurations were tested. It was seen that the photodiode with fingers of 1 µm pitch provides higher power than other photodiodes without



(a)



(b)

Fig. 15. Die micrograph of the 5×5 mm^2 micro-energy harvesting chip with different structures for testing is shown in (a) and the experimental setup of the chip under test is shown in (b).

fingers or with different pitches for the same illumination. The generated voltage goes from 0.27 V to 0.46 V for an illumination span from 100 lx to 100 klx, and a harvested power between 3.7 nW and 8.3 µW for the same illumination range. These results differ slightly from the theoretical values obtained by ATLAS (Silvaco) device simulator using the doping profiles from the technology provider [18]. This deviation will affect the PMU efficiency.

The experimental setup can be seen in Fig. 15(b). A regulated lamp is used to illuminate the chip. Both the voltage of the lamp and the distance between the chip and the lamp are modified to control the illumination. A digital lux meter (TES 1332) is used to measure the illumination. The output and the control signals are visualized through an oscilloscope (Tektronix MDO4034C). Two source meter units (2400 series Keithley SMU) are used to measure the efficiency of the system.

In Fig. 16 an example of the experimental behavior of the level detectors of the MPPT block captured directly from the oscilloscope is shown. The variation of the voltage generated by the photodiode, the output of the level detectors and the output of the PMU are depicted for a continuous variation of the illumination. The load of the PMU is a tantalum capacitor of 100 nF and the oscilloscope itself, which has an input capacitance of 20 pF and an input resistance of 1 MΩ, which leads to measured V_{out} values lower than the simulated ones in Fig. 5. In Fig. 16(a) the behavior of the level detectors

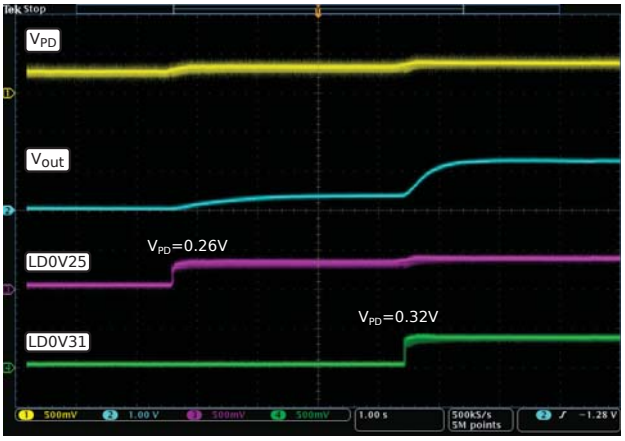
TABLE IV
POWER BREAKDOWN (SIMULATION RESULTS)

WR	Average PMU input power (μW)	PMU output power (μW)	PMU consumed power (μW)	MPPT (%)	Auxiliary oscillator (%)	Auxiliary DC-DC converter (%)	Main oscillator (%)	Main DC-DC converter (%)
1	0.0048	0.0011	0.0037	0.74	1.42	64.88	1.98	30.22
2	0.045	0.018	0.027	0.40	0.10	11.76	1.38	86.00
3	0.30	0.12	0.18	0.13	0.054	19.44	0.56	79.76
4	1.76	0.79	0.97	0.063	0.027	9.81	0.35	89.64
5	11.90	5.33	6.57	0.012	0.011	4.20	0.090	95.68

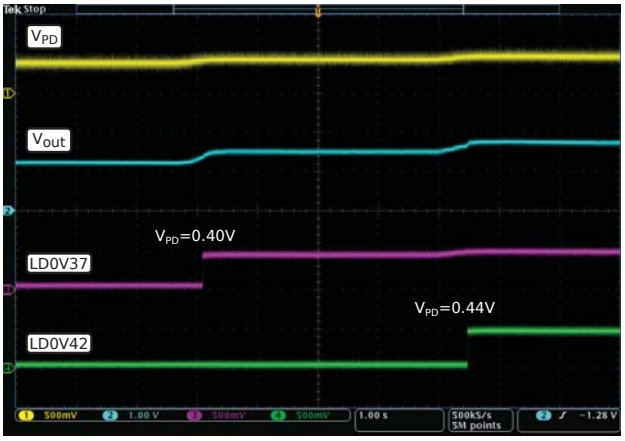
LD0V25 and LD0V31 are shown. First, all the level detectors are low and V_{out} is close to zero because the load of the PMU is too high for this situation. Then, the illumination increases to activate the level detector LD0V25. Under this situation, the harvested power is higher, so V_{out} increases. Finally, the illumination increases even further and LD0V31 is activated. Also, V_{out} increases reaching values higher than 1.1 V as the load is kept constant. Fig. 16(b) shows the transitions of the level detectors LD0V37 and LD0V42. As the illumination increases, the level detectors are activated. Also, V_{out} increases with the illumination as V_{PD} increases. Different MPPT blocks on different chips were measured obtaining the follow trigger voltages at room temperature: $V_{tg\_0V25} = 0.258 \pm 0.010$ V, $V_{tg\_0V31} = 0.316 \pm 0.012$ V, $V_{tg\_0V37} = 0.392 \pm 0.013$ V and $V_{tg\_0V42} = 0.433 \pm 0.011$ V, which differ from the nominal values (0.25 V, 0.31 V, 0.37 V, 0.42 V). The largest difference is in the trigger value of the third level detector and as we will see, this deviation will affect the efficiency of the system as the power generated by the photodiode in the two working regions separated by this third level detector (WR3-WR4) will not be the expected one and, as a consequence, the frequency of both oscillators and the topology of the main charge pump will not be optimal.

To demonstrate the start-up process, an external tantalum capacitor of 100 nF is charged at very low constant illumination. Fig. 17 shows experimental results directly extracted from an SMU. Fig. 17(a) depicts the PV curve of an isolated solar cell on the same substrate identical to the one in the energy harvesting system. The maximum power point is 2.38 nW and V_{PD} is around 0.2 V, which is close to the simulated value of 0.17 V in Fig. 5. Fig. 17(b) displays the charge process of a tantalum capacitor showing the voltage between its terminals versus time. The PMU working in WR1 is able to start-up from an input power of 2.38 nW and to charge the external capacitor at a voltage higher than 1.1 V.

The end-to-end measured efficiency defined by $\frac{P_{out}}{P_{mpp}}$ is shown in Fig. 18 for five different chips, where P_{mpp} is the maximum power generated by the photodiode and P_{out} is the PMU output power at $V_{out} = 1.1$ V, where the PMU is most efficient by design. To obtain P_{mpp}, the PV curve of the isolated on-chip solar cell is measured with an SMU at the same time as the output power of the PMU is being measured with another SMU. The efficiency is plotted for different input powers and consequently for different loads to keep $V_{out} = 1.1$ V. As can be seen, the efficiency is about 25% and 40% for low and high input powers, respectively,



(a)



(b)

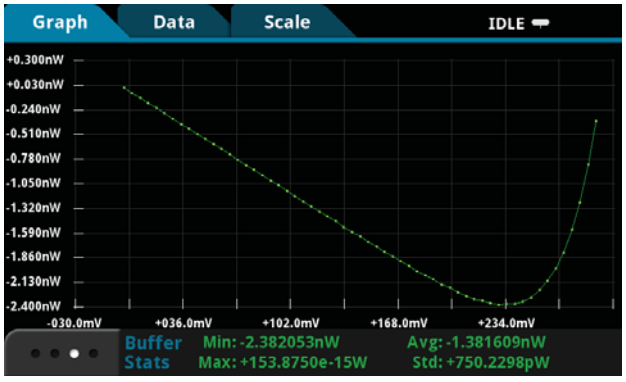
Fig. 16. Measured photodiode voltage (V_{PD}), output voltage of the PMU (V_{out}), and voltage level detectors waveforms in (a) for LD0V25 and LD0V31 and in (b) for LD0V37 and LD0V42.

reaching a peak of 57%. These lower efficiencies for very low illumination are due to the low available voltage and power in the system as under this situation the transistors are slower and more power hungry. The observed drops in the efficiency for low illumination are also expected due to the transitions of the level detectors. This effect is heightened by the deviation in the trigger voltage of the third level detector of the MPPT block whose actual trigger value is $V_{tg\_0V37} = 0.392$ V instead of the nominal value $V_{tg\_0V37} = 0.37$ V.

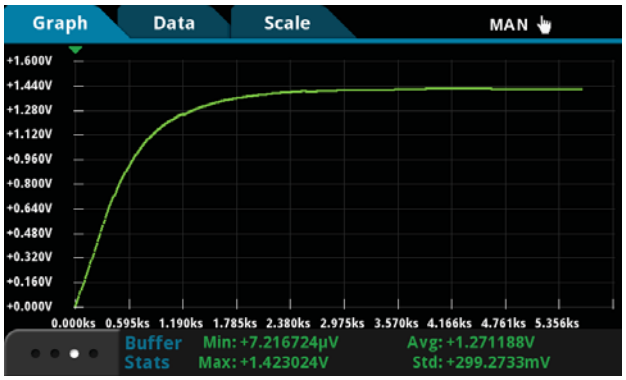
Apart from optimized circuit designs, we think that the key to achieving such a performance is the open-loop MPPT due to its low power consumption. Admittedly, this technique is

TABLE V
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

	[7]	[3]	[34]	[35]	[15]	This Work
Technology	standard 0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	standard 0.18 µm CMOS
Voltage boosting	charge pump	boost with voltage doubler	self-oscillating voltage doubler	charge pump	discontinuous charge pump	charge pump
Transducer + PMU on-chip	yes	no	no	no	no	yes
Transducer + PMU area (mm^2)	1.3 + 0.24	- + 1.53	- + 0.86	- + 0.552	- + 2.72 + off-chip cap.	1 + 0.575
Input power range (nW)	-	1.1 - 6.25	1.7 - 12500	5900 - 47000	0.02 - 1500	2.38 - >10000
Output power range (nW)	-	0.544 - 4	0.5 - 5000	3840 - 30550	0.005 - 600	0 - 4500
Cold start-up	yes	no	yes	yes	no	yes
Minimum input power to start-up (nW)	-	-	6	-	-	2.38
MPPT	no	no	user-operated	yes	yes	yes
Output regulation	no	no	no	yes	no	no
End-to-end peak efficiency (%) @ P_{out} (µW)	67@1.27	53@0.0012	50@0.12	72@-	50@0.008	57@2.07



(a)



(b)

Fig. 17. Experimental results extracted directly from an SMU for the start-up process with the PV curve of the on-chip solar cell in (a) and the output voltage of the PMU for such an input power in (b).

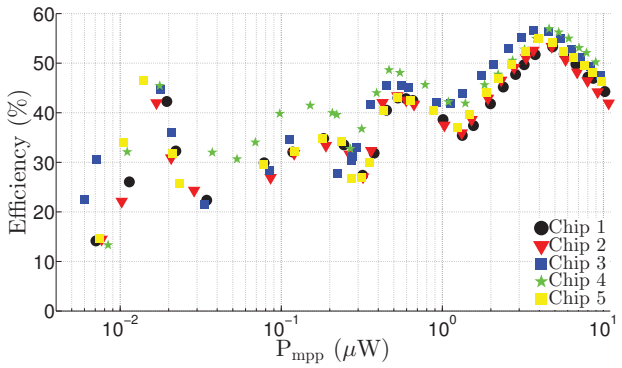


Fig. 18. Measured end-to-end efficiency for different input powers for five different chips.

technology dependent and it requires a joint model of the photodiode and the capacitive charge pump, but an iterative refinement of such a model from experimental results might increase the efficiency further, and the reduced form factor from the energy transducer and the PMU on the same substrate is of utmost interest for applications like implantable devices [1].

Finally, Table V summarizes the performance of our design and compares it to prior work. In [7] a system which includes a transducer and a PMU on the same substrate is designed, however it does not include MPPT circuits, making difficult to work with a high input power range. On the other hand, the works in [3], [15], [34], [35] do not include the transducer and the PMU on the same substrate. A boost converter is designed in [3], but it includes an external inductor and it does not incorporate MPPT strategies. In [34] a self-oscillating voltage doubler is designed reaching high peak efficiency, nevertheless it does not include MPPT capabilities as the authors manually change the gain by adjusting the number of cascaded stages of voltage doublers. The charge pump made in [35] reaches high efficiency with MPPT capabilities and cold start-up, however it is not intended for micro-energy harvesting since the minimum input power needed by the system is about µW with an input voltage about 1 V. Finally, in [15] the authors introduce the discontinuous charge pump concept achieving good efficiency, nevertheless the chip needs an external capacitor and it does not have cold start-up. Regarding the efficiency, it is worth noting that the proposed chip is the only one that includes the circuitry to start-up from 2.38 nW. This limits the end-

to-end efficiency compared to other works. In conclusion, the proposed chip is able to start-up without external signals or components from 2.38 nW of harvested power, being the only one with on-chip harvesting and MPPT capabilities on the same substrate capable of handling around 80 dB of input power range, with a total area of just 1.575 mm^2.

V. Conclusion

A new system for micro-energy harvesting including a photodiode and a PMU on the same substrate has been designed and fabricated in standard 0.18 μm CMOS technology achieving a form factor of 1.575 mm^2. The 1 mm^2 photodiode is the only power source of the system which varies from nW to μW. The PMU includes a continuous and two-dimensional MPPT based on four voltage level detectors which define five different working regions depending on the illumination. For each working region, the oscillating frequency of the main oscillator is changed and the gain and the capacitance per stage of the main charge pump is also adjusted. A self-tuning reference current which changes with the harvested voltage permits the variation of the frequency of the auxiliary oscillator and a fine tuning of the main oscillator. The system is validated through experimental results reaching a good efficiency for a high input power range and it is able to start-up from 2.38 nW of harvested power without any external kick off or control signal.

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