José Carlos Piñero Charlo

Universidad de Cádiz

Role of interface configuration in diamond-related power devices

Thesis committee composed by:

D. Jean-Daniel Ganière
Maître d'enseignement et de recherche, Laboratoire d'optoélectronique quantique – EPFL Lausanne (Switzerland)

D. Julien Pernot
Professeur des universités, Institut Néel – Université Joseph Fourier – CNRS Grenoble (France)

D. Javier Navas Pineda
Profesor Titular de Universidad, Química Física – UCA Cádiz (Spain)

Directed by:

D. Daniel Araújo Gay
Catedrático de Universidad, Ciencias de los materiales, IM y QI – UCA Cádiz (Spain)

Dª. María del Pilar Villar Castro
Profesor Titular de Universidad, Ciencias de los materiales, IM y QI – UCA Cádiz (Spain)

Reported by:

D. Tokuyuki Teraji
Principal Researcher, Wide bandgap Materials Group – NIMS (Japan)

D. Etienne Bustarret
Directeur de Recherche, Institut Néel – CNRS Grenoble (France)

UCA Universidad de Cádiz

A mis padres y mi hermano, por crear en mí un pensamiento crítico y autónomo. Por su continuo apoyo, mis actos son vuestro legado.

A Raquel, por su paciencia y comprensión, por ser el "punto de apoyo" que mueve el mundo.

To my fathers and my brother, for creating in me a critical and autonomous thinking. For their continued support, my acts are your legacy.

To Raquel, for her patience and comprehension, for being the "place to stand" which moves the world.

Departamento de Ciencias de los Materiales e Ingeniería Metalúrgica y Química Inorgánica

Thesis direction:

D. Daniel Araújo Gay
Catedrático de Universidad, Ciencias de los materiales, IM y QI – UCA Cádiz (Spain)

Dª. María del Pilar Villar Castro
Profesor Titular de Universidad, Ciencias de los materiales, IM y QI – UCA Cádiz (Spain)

Reported by:

D. Tokuyuki Teraji
Principal Researcher, Wide bandgap Materials Group – NIMS (Japan)

D. Etienne Bustarret
Directeur de Recherche, Institut Néel – CNRS Grenoble (France)

Thesis jury:

D. Jean-Daniel Ganière
Maître d'enseignement et de recherche, Laboratoire d'optoélectronique quantique – EPFL Lausanne (Switzerland)

D. Julien Pernot
Professeur des universités, Institut Néel – Université Joseph Fourier – CNRS Grenoble (France)

D. Javier Navas Pineda
Profesor Titular de Universidad, Química Física – UCA Cádiz (Spain)

Surrogate thesis jury:

D. David González Robledo
Catedrático de Universidad, Ciencias de los Materiales e Ingeniería Metalúrgica y Química Inorgánica – UCA Cádiz (Spain)

D. Etienne Gheeraert
Professeur des universités, Institut Néel – CNRS Grenoble (France)

Institut NEEL/CNRS
25 rue des Martyrs
BP 166
38042 Grenoble cedex 9
France
Tél. : +33 (0)4 76 88 7498
Mail : etienne.bustarret@neel.cnrs.fr
neel.cnrs.fr

TO WHOM IT MAY CONCERN

Grenoble, March 25th, 2016

Subject : report on the thesis manuscript submitted by José Carlos Piñero Charlo

In his manuscript entitled « *Role of interface configuration in diamond-related power devices* », José Carlos Piñero Charlo applied advanced electron microscopy tools to state-of-the-art unipolar electronic devices based on single crystal diamond epilayers.

Most of the samples have been electrically characterized before being investigated by EELS, STEM-HAADF and CTEM methods, providing additional strength to the conclusions of the candidate's systematic studies. Original sample and data processing schemes have been proposed whenever necessary, adding a welcome originality in the field of electron microscopy, but the main impact of this work will affect the diamond community : José Carlos Piñero Charlo has demonstrated in a convincing manner how local defects at the interface, in particular chemical and thickness inhomogeneities at the nanometric scale, could explain the low performance of actual diamond devices when compared to theoretical ideal models. In that sense, his work on Schottky diodes and on the MOS capacitor and MOSFET structures is quite original and timely, and will be particularly useful to the diamond electronic device community.

As for the scientific standard of this thesis, it is quite high : the variety of single crystal diamond devices and of TEM-based investigation tools is impressive, and their combination is shown to be quite powerful. The technical quality of the manuscript itself is also above average, with pedagogical, clear and self-contained presentations of the results and of their interpertation. Some of these results have already been published in at least 7 articles and presented by the author at various international conferences and workshops. I expect that more papers will appear within the next few months.

Overall, José Carlos Piñero Charlo's work meets international standards for a PhD thesis, and I recommend that he should be awarded a Doctor Degree.

Etienne BUSTARRET
Director of Institut NEEL

NATIONAL INSTITUTE FOR MATERIALS SCIENCE (NIMS)
1-1 NAMIKI, TSUKUBA, IBARAKI 305-0044, JAPAN

PHONE: 81-29-860-4776
FAX: 81-29-851-4005
e-mail : TERAJI.Tokuyuki@nims.go.jp

25 March, 2016

Thesis report for: **José Carlos Piñero Charlo**

Thesis title: **Role of interface configuration in diamond-related power devices**

The study being carried out by José C. Piñero Charlo during his PhD period will have a strong impact on diamond research society. Diamond is theoretically suitable material for power devices. However, their actual device performance is far from the theoretical ones at this moment. Also device stability at elevated temperature, which is alternative strong point of diamond originally, is not as high as being expected. José C. Piñero Charlo pointed out, though his PhD study, that an insufficient and/or unstable performance of diamond devices originated from the non-ideal interface formation in atomic scale, and made a correlation between change of electric properties of diamond devices and structural change of diamond interfaces in atomic scale. He started this very important but difficult subject from the state-of-the-art diamond Schottky diodes with different metals and proposed an unique interface structure for stabilizing diamond Schottky diode performance, as discussed in Chap. 3 of this thesis. He extended this analysis approach to diamond MOS and delta FETs., as can be seen in Chaps. 4 and 5.
I remark José C. Piñero Charlo's work is highly valued from both scientific and technological point of view. Models and data, obtained through a fine and systematic microscopic analysis, provide a guideline for the researchers working in the diamond device field.

Therefore, I suggest that José C. Piñero Charlo is suitable for the degree of Doctor.

Tokuyuki Teraji,

Wide Bandgap Material Group,
Optical and Electronic Materials Unit
National Institute for Materials Science,
1-1 Namiki, Tsukuba, 305-0044, Japan

Acknowledgements

I wish to convey my thanks to all my partners in UCA, especially those who shared with my all their wisdom: Fernando Lloret Vieira, Mª de la Paz Alegre Salguero, Jesús Hernandez Saz and Carlo Enzo Pastore. I want to express my sincere thanks to all the people who helped me during the development on my PhD project. These in particular:

Prof. Dr. D. Daniel Araujo Gay, who accepted the direction of this PhD project at the University of Cádiz. His expertise on luminescence, semiconductor physics and electronic power devices was essential in the success of this thesis. He gave me the possibility to work on this interesting and nice topic. Thank you for giving me this opportunity.

Dr. Dª. Mª del Pilar Villar Castro, who guided me during this PhD project and accepted the co-direction of this thesis. She gave me expertise on chemical diamond surface aspects, as well as training and knowledge in EELS mode of STEM.

Prof. Dr. D. Rafael García Roja, main group leader of the research group TEP 120 (science and engineering of materials), who accepted me as a part of the research group. He allows my integration in the context of the group, easing personal and professional relationship with other researchers.

Prof. Dr. D. Jean-Daniel Ganière, my main supervisor during my internship at EPFL, Lausanne Switzerland, who gave me full knowledge in quantum optoelectronic phenomena, and the opportunity to experiment time-resolved CL.

Prof. Dr. D. Etienne Bustarret and Dr. D. Julien Pernot, my main supervisors during my stage at Institut Néel (CNRS), Grenoble France, who gave me the opportunity to create a test power device, as well as a deep knowledge in power electronics.

I would also wish to thank the following people/institutions for their commendable effort during the development of this thesis:

- Dr. D. Gauthier Chicot and Dr. D. Aurèlien Merechal from the institut Néel (CNRS)
- Dr. D. Josep Montserrat and Prof. Dr. D. Philippe Godignon from Instituto de Microelectrónica de Barcelona (CSIC)

- Dr. D. Alexandre Fiori and Dr. D. Tokuyuki Teraji from National Institute of Materials Science in Japan (NIMS) for fruitful discussions.
- Dr. Samuel Sonderegger, Dr. Jean Berney and Mr. Olivier Gougeon from Attolight
- Dr. D. Mehran Shahmohammadi and Dr. D. Gwénolé Jacopin from Laboratoire de Opto-Electronique Quantique (EPFL)
- Institut Néel (France)
- École Polytechnique Fédérale de Lausanne (EPFL)
- Servicios Centrales de Ciencia y Tecnología at UCA
- Ministerio de Ciencia e Innovación for the grants BES-2010-039524 and EEBB-I-13-07696 of the project TEC2009-11399

Resumen

Durante los años transcurridos en el desarrollo de esta tesis, la generación de energía eléctrica mundial habrá crecido a un ritmo medio anual del 3.6%[1], que refleja las crecientes necesidades de la sociedad en términos de suministro eléctrico (voltaje, densidad de potencia, frecuencia de uso, fiabilidad o temperatura de trabajo). Estas necesidades se están volviendo más exigentes, las pérdidas de energía deben ser reducidas y el rendimiento mejorado. El progreso de las recientes décadas en el campo de la electrónica de potencia no se debe sólo a la introducción de arquitecturas novedosas, sino también a la evolución de la composición de los dispositivos. El progreso actual está obstaculizado por las limitaciones inherentes al silicio, componente del que están fabricados la mayor parte de los dispositivos electrónicos de potencia actualmente disponibles comercialmente.

Los semiconductores de ancha banda prohibida tienen propiedades particularmente atractivas para funcionar a altos voltajes y frecuencias en entornos de alta temperatura. Como semiconductores de ancha banda prohibida, los dispositivos basados en diamante semiconductor se han manifestado como un campo de investigación prometedor, no sólo por la amplia aplicabilidad en las ciencias biológicas, si no por sus extraordinarias propiedades eléctricas (elevada movilidad de portadores, alto valor de ruptura eléctrica y extraordinaria conductividad del calor). Tras casi quince años de investigación en diamante semiconductor se han resuelto gran cantidad de interrogantes, lo que ha permitido la aparición de los primeros prototipos. Es esta evolución en el conocimiento la que ha posibilitado la elección del diamante como candidato idóneo para la realización de componentes electrónicos de alta potencia, entendiendo estos dispositivos como aquellos que funcionan en condiciones de alta frecuencia de conmutación de señal.

Paradójicamente, a pesar de sus numerosas ventajas y de los amplios estudios en esta materia, la explosión de las tecnologías basadas en diamante aún no ha llegado a su madurez. Esto es debido, fundamentalmente, a la mala calidad estructural en la implementación de los diseños ideados para los dispositivos electrónicos con canal activo de diamante. Adicionalmente, las limitaciones en las aplicaciones tecnológicas del diamante derivan de otras de sus propiedades extremas, como la dureza (que dificulta su clivaje) o la alta energía de activación de dopantes tipo n.

Sin embargo, se han conseguido numerosos progresos en el crecimiento de estructuras de diamante para dispositivos eléctricos. En particular, estos esfuerzos han permitido minimizar la densidad de dislocaciones producidas durante el crecimiento de estructuras

[1] OECD, library: http://www.oecd-ilibrary.org/economics/oecd-factbook-2013_factbook-2013-en

multicapa u optimizar la densidad de dopantes activos durante el crecimiento de capas dopadas (lo que ha requerido de amplios estudios sobre la incorporación del boro en la red cristalina del diamante). Paralelamente a los esfuerzos desarrollados en la comprensión y el estudio de la incorporación de dopantes en la red del diamante, se han desarrollado otros no menos loables avances en el diseño de estructuras óptimas para establecer contactos eléctricos en diamante.

En la presente contribución, se evidencia el uso del diamante semiconductor como base para un dispositivo de alta potencia con canal activo de diamante, las diversas alternativas de diseño, sus técnicas de estudio y las características eléctricas de los primeros prototipos de los diferentes dispositivos.

Abstract

During the years lapsed on the developing this thesis, worldwide electrical power generation will have increased at an annual average rate of 3.6%, which reflects the growing needs of society in terms of electricity supply, voltage, power density, frequency of use, reliability or working temperature. These needs are becoming more demanding; energy losses must be reduced and performance enhanced. In recent decades, progresses in the field of power electronics are not only due to the introduction of innovative architectures, but also to the evolution of composition of devices. Nowadays, progress is hindered by the inherent limitations of silicon, component of which is manufactured the vast majority of commercially available power electronics components.

Wide band gap semiconductors have properties particularly suited to managing high voltages, high frequencies, and hot environments. As a wide band gap semiconductor, semiconducting diamond devices had become a promising research field, not only for its applications on biological sciences, but because its exceptional electric properties (elevated mobility, high breakdown electric field and outstanding thermal conductivity). After almost fifteen years of research on semiconducting diamond, a great amount of questions have been answered, having allowed the emergence of the first prototypes. This evolution in the know-how has enabled the choice of diamond as the ideal material for the development of high power electronics devices, available for working in high commutation frequency conditions.

Paradoxically, despite the many advantages and the extensive studies on this matter, the spread of diamond based technologies has not reached maturity. This is due, basically, to the bad structural quality on the implementation of the designs for the electronic devices with an active diamond channel. Additionally, limitations in the technological applications of diamond arise from some other of its extreme properties, such as its hardness (that makes cleavage extremely difficult) or the high activation energy of n-type dopants.

However, numerous progresses have been achieved in the growing of diamond structures for electric devices. Particularly, these efforts lead us to minimize dislocation density produced during the growing of multi-layer structures or to optimize the active density of dopants during the growing of doped layers (which have required extensive studies about the incorporation of boron in the diamond lattice). Parallel to the efforts made in the understanding and study of the incorporation of dopants in the diamond lattice, other equally laudable progress in designing optimal structures have been developed to establish the electrical contacts in diamond.

In the present contribution, we feel evident the use of semiconducting diamond as a base for a high power electrical devices with a diamond active channel. The different alternatives on the design, technics for the study and electrical characteristics of the first prototypes of the different devices are shown.

Acronyms

ADF	Annular Dark Field (electron microscopy imaging mode)
Al_2O_3	Aluminum oxide - alumina
ALD	Atomic Layer Deposition
BF	Bright Field (TEM imaging mode)
C	Capacitance [F]
CL	Cathodoluminescence
C_{ox}	Oxide Capacitance [F]
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
D	Drain
DF	Dark field (TEM imaging mode)
D_{it}	Interface state Density [eV-1.cm-2]
E_c	Conduction band energy [eV]
EELS	Electron Energy Loss Spectroscopy
E_F	Fermi level [eV]
E_g	Band Gap Energy [eV]
E_v	Valence band energy [eV]
FET	Field effect Transistor
FIB	Focused Ion Beam
Ga	Gallium
Ga^+	Gallium Ion
HAADF	High Angle Annular Dark Field (electron microscopy imaging mode)
HPHT	High Pressure High Temperature
HREM	High Resolution Electron Microscopy
I_{DS}	Drain-Source Current [A]
I_G	Gate Current leakage [A]
JFET	Junction Field-Effect Transistor
k	Boltzmann constant $=1.3806504 \cdot 10^{-23}$ [J/K]
L	Transistor Channel Length [μm]
MBE	Molecular Beam epitaxy
MESFET	Metal-Semiconductor Field Effect Transistor
MIT	Metal-Insulator transition
MODFET	MOdulation-Doped Field Effect Transistor
MOS	Metal-Oxide-Semiconductor

MOSFET	Metal-Oxide-Semiconductor Field-effect transistor
MPCVD	Microwave-Plasma Chemical Vapour deposition
n_i	Electron concentration
Ni	Nickel
NiD	Non-intentionally doped
N_{it}	Interface trapped charge concentration density [cm^{-2}]
N_{ot}	Oxide trapped charge density [cm^{-2}]
POA	Post Oxidation Annealing
Pt	Platinum
q	Basic Electronic charge [C]
Q_{eff}	Effective charge [cm^{-2}]
Q_m	Mobile ionic charge [cm^{-2}]
Q_{ox}	Oxide trapped charge [cm^{-2}]
Q_{it}	Interface trapped charge [cm^{-2}]
Q_t	Traps charge [cm^{-2}]
SBD	Schottky Barrier Diode
SiC	Silicon Carbide
S	Source
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
V_{DS}	Drain-source Voltage [V]
V_{GS}	Gate-source voltage [V]
W	Gate width [µm]
WBG	Wide Band Gap
WC	Tungsten carbide
W_xC_y	Tungsten semicarbide
Zr	Zirconium
ZrO_2	Zirconium oxide
ε_r	Dielectric permittivity [$F.m^{-1}$]
μ_{eff}	Effective mobility in the inversion channel of a MOS transistor [$cm^2 \cdot V^{-1} \cdot s^{-1}$]
μ_n	Electron mobility [$cm^2 \cdot V^{-1} \cdot s^{-1}$]
μ_p	Hole mobility [$cm^2 \cdot V^{-1} \cdot s^{-1}$]

Index

Chapter I: Introduction to diamond devices

This chapter contextualizes and exposes challenges of diamond as a semiconducting material for power electronic applications. Several approaches aiming to the fabrication of different diamond-based power devices are presented. This introduction is the followed by the motivations of the study of diamond-based power device:

I.1 **Context & history of semiconductor devices:** Here, we introduce the use of semiconductor devices through a brief historical review; we also evaluate the impact of modern electronics and semiconductor devices in the information revolution of the 20^{th} century. Information is organized in the following sections:

- **Early history**
- **Materials & devices**
- **Information revolution**

I.2 **Motivation for diamond in power electronics:** As a consequence of the historical trend presented in I.1, world-wide demand of power supply is increasing and electricity has become a vital resource for human civilization. This fact carries with the consequent problems of power generation and CO_2 emissions, as well as the rising demand of ultra-fast and more efficient technologies. In this section, we will present wide bandgap materials as the next step in the evolution of modern electronic. Finally, diamond will be presented as a wide-bandgap material with outstanding properties.

- **Diamond's electrical applications**

***I.3* Challenges in power electronics** are discussed and summarized in this section. Spotlights on the main challenges such as the increase of the power switch or the frequency are presented.

***I.4* Diamond and its properties:** A brief introduction to semiconducting diamond is here presented together with its most relevant properties for power device applications. Such properties can be compared with those demanded in I.3. This section is presented with the following index:

- **Synthetic industrial diamonds**
- **Diamond doping**
- **Doping-induced metal-to-insulator (MIT) transition**

***I.5* Relevant properties for electronic power devices**: Diamond main properties, useful for power device applications, are here presented by following the next index:

- **Carrier mobility**
- **Saturation velocity**
- **Carrier lifetime**
- **Dielectric breakdown field**
- **Thermal properties**

***I.6* Motivation: impact of the interface configuration in diamond devices**. In this section, we introduce the motivation for the present PhD disertation, by presenting the problematic of the diamond termination and its impact on the behavior of the related final device.

***I.7* Objectives: unipolar devices studied in this work**. Several diamond interfaces (such as diamond-metal or diamond-oxide) will be studied in the present thesis. Here we present a brief discussion of the objectives with this paper.

I.1 Context & history of semiconductor devices

There is no doubt that semiconductors changed the world beyond anything that could have been imagined before them. The history of semiconductors is long and complicated, and one cannot expect it to fit one short introduction. The information contained in this section can be extended by consulting literature [1].

Early history

The term “semiconducting” was first used by Alessandro Volta in 1782 [2]. The first documented observation of a semiconductor effect is that of Michael Faraday (1833), who noticed that the resistance of silver sulfide decreased with temperature, which was different than the dependence observed in metals [3]. In 1874 Karl Ferdinand Braun observed conduction and rectification in metal sulfides [4]. In 1929 Walter Schottky experimentally confirmed the presence of a barrier in a metal-semiconductor junction [5].

Theory

In 1878, Edwin Herbert Hall discovered that charge carriers in solids are deflected in a magnetic field (Hall effect). Shortly after the discovery of the electron by J. J. Thomson, several scientists proposed theories of electron-based conduction in metals. In 1914 Johan Koenigsberger divided solid-state materials into three groups with respect to their conductivity: metals, insulators and “variable conductors”.

In 1928 Ferdinand Bloch developed the theory of electrons in lattices [6]. In 1930, Bernhard Gudden reported that the observed properties of semiconductors were due exclusively to the presence of impurities and, consequently, chemically pure semiconductors did not exist. In 1930, Rudolf Peierls presented the concept of forbidden gaps that was applied to realistic solids by Brillouin that same year.

In 1938, Walter Schottky and Neville F. Mott (Nobel Prize in 1977) independently developed models of the potential barrier and current flow through a metal-semiconductor junction, thanks to the understood of the importance of surface states [7]. A year later, Schottky improved his model including the presence of space charge. In 1942 Hans Bethe developed the theory of thermionic emission (Nobel Prize in 1967).

Materials & devices

In 1945, William Shockley designed the first semiconductor amplifier operating by means of the field-effect principle (unfortunately this effect was not observed experimentally and the device didn’t work). Trying to understand why, while working on the field-effect devices, in December 1947 John Bardeen and Walter Brattain built a germanium-gold point-contact transistor and demonstrated that this device exhibited power gain at all frequencies.

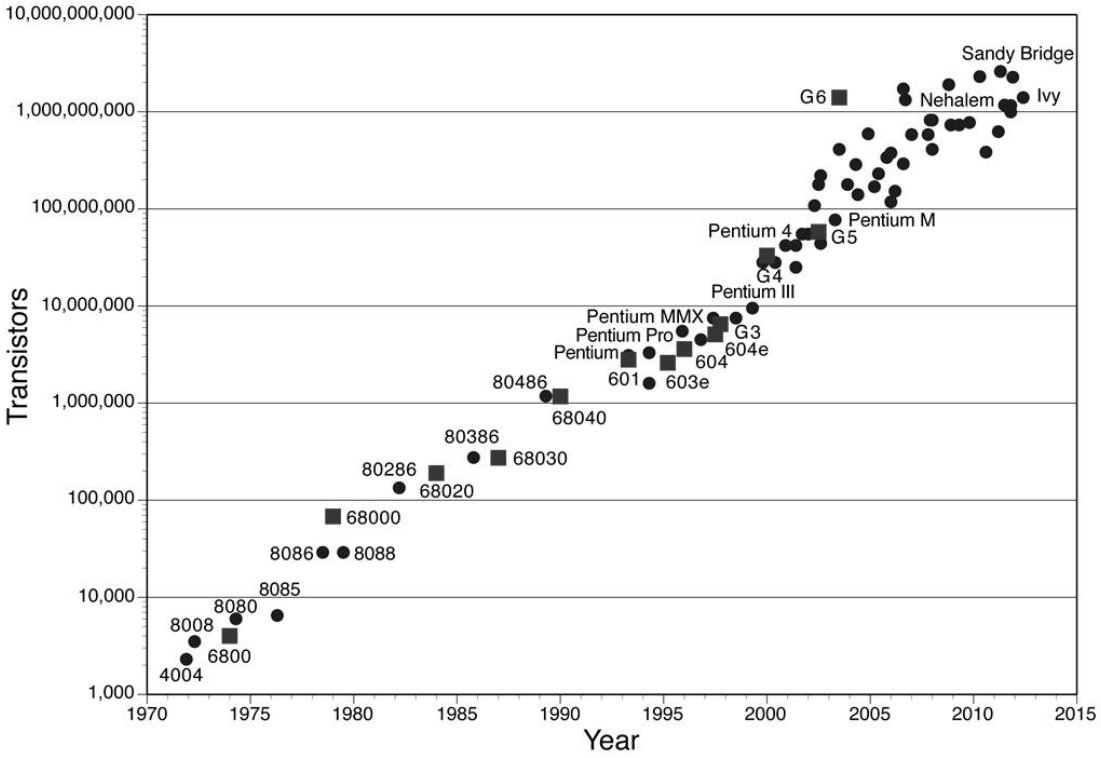

Figure 1: Number of transistors in successive Intel processors as a function of time (Intel website). Take into account that Moore's law doesn't actually consider computing power.

That is, W. Shockley, J. Bardeen and W.H. Brattain had invented the first working solid-state amplifier, being awarded with the Nobel Prize in physics in 1956. Since that moment, the field of semiconducting devices hatches and evolves with the use of new semiconducting materials like Si (1949), GaAs (1962), GaN (1996) or SiC (1990-2000).

Information revolution

Silicon may be considered as the information carrier of our times. In the history of information there were two revolutions (approximately 500 years apart). The first was that of Johannes Gutenberg who made possible the dissemination of information (making it available to many) the other is the invention of the transistor. Currently the global amount of information doubles every year. Many things we are taking for granted (such as, e.g., computers, Internet and mobile phones) would not be possible without silicon microelectronics. Electronic circuits are also present in cars, home appliances, machinery, etc. Optoelectronic devices are equally important in everyday life, e.g., fiber-optic

communications for data transfer, data storage (CD and DVD recorders), digital cameras, etc.

Since the beginning of semiconductor electronics, the number of transistors in an integrated circuit has been increasing exponentially with time. This trend had been first noticed by Gordon Moore [8] and is called Moore's law (here presented in **Figure 1**).

Even though the bipolar technology was largely replaced by CMOS (more than 90 percent of integrated circuits are manufactured in CMOS technology), Moore's law is still true in many aspects of the development trends of silicon microelectronics (obviously, with the appropriate time constant). The MOS transistor has been improved countless times but above everything else it has been miniaturized beyond imagination. The reduction of the feature size is more or less exponential. The number of transistors produced in 2015 I, is anticipated to be approximately ten billion transistors… for every person living on the Earth![2]

I.2 Motivation for diamond in power electronics

Nowadays, electricity is the lifeblood of human civilization. All over the world, it is an essential and a vital resource for all economic sectors (production, manufactures and services). Worldwide electrical power generation rose at an average annual rate of 3.6% from 1971 to 2009[3], greater than the 2.1% growth in total primary energy supply. As an example, the worldwide production of electricity in 2009 was 20053 TWh, which was 11% of the solar energy received by the earth in one hour (174000 TWh). Additional statistics can be found in the web of the International Energy Agency[4].

Power electronics is the branch of electronics specifically dealing with collecting, delivering, and storing energy, including general and local/commodity energy supplies, by conversion and control of electrical power. Specific applications range from power supply systems to motor vehicle drives, photovoltaic and fuel cell converters, inverters, and high-frequency heating, among many others. The impact of power electronics has already been

[2] Hardware components, Intel processor history, http://www.interfacebus.com/intel-processor-types-release-date.html

[3] OECD, library: http://www.oecd-ilibrary.org/economics/oecd-factbook-2013_factbook-2013-en

[4] https://www.iea.org/publications/freepublications/publication/

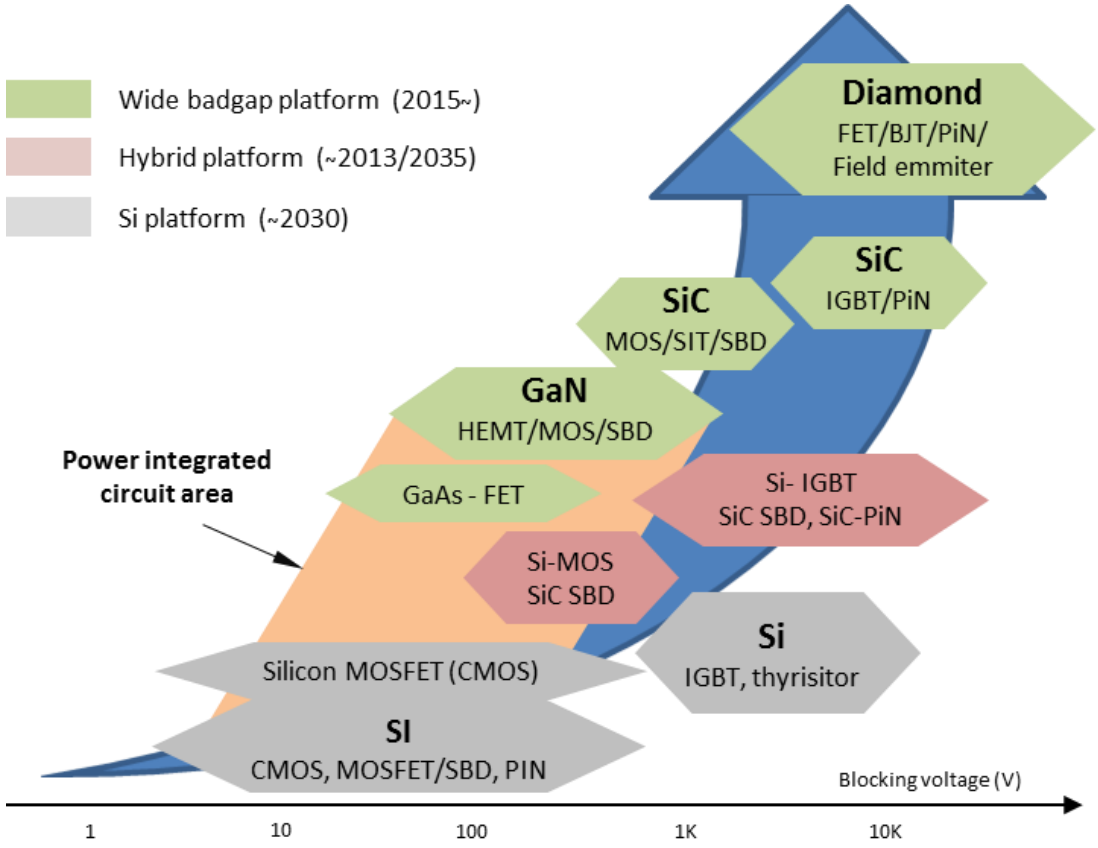

Figure 2: Roadmap of the future advance power devices, showing the predicted evolution in semiconductor use.

significant and is expected to continue increasing in the future optimizing the energy production, energy conversion and management.

Specific devices with efficiencies approaching 98–99%, ultra-fast switching capabilities, and high resiliency to high temperature and other harsh environmental conditions are required for power electronics, which was officially born with the silicon power metal oxide semiconductor field-effect transistor (MOSFET) entering the market in the late 1970s [9]. Indeed, market forecasts predict a strong increase in the next 5–10 years for power electronics technologies and an important contribution is expected to come from the use of wide bandgap semiconductors [10], as highlighted in **Figure 2**.

As in most other electronics areas, silicon has been the predominant semiconductor in power electronics up to date. However, with the emergence of wide bandgap materials power electronic components which are faster, smaller, more efficient, and more reliable than their Si-based counterparts. Moreover, they permit the operation of devices at higher voltages, temperatures, and frequencies, making possible to reduce volume and weight in a

wide range of applications. This could lead to large energy savings in industrial and consumer appliances, accelerate widespread use of electric vehicles and fuel cells, and integrate renewable energy into the electric grid [11].

Significant reductions in cost and CO_2 emissions are expected to result in the long term in an extensive use of power electronics and related automation control technologies anticipated over the coming decades. In fact, the use of wide bandgap materials will result in a greener environment, by eliminating up to 90% of power losses currently occurring during conventional electric conversion. Wide bandgap devices can operate at voltages 10 times higher than Si-based ones, because of their higher maximum electric field and operating temperatures of well over 300°C, twice the maximum operating temperature of Si-based devices [12].

Theoretically, the operating frequency of wide bandgap semiconductors is at least 10 times higher of that of conventional ones, thereby opening up a range of new applications, such as compact radio frequency amplifiers. Once wide bandgap materials and power devices have matured, substrate material and manufacturing costs are expected to decrease, and the devices will be widely used in highly efficient variable speed drives in motors or as compact power supplies in consumer electronics. They can convert direct current (DC) electricity generated from wind and solar energy into alternating current electricity used in medium and high voltage at home and with reduced energy losses conversions.

In addition, the transformer size could be reduced by a factor of 10 or more. These devices will also find applications in efficient high-voltage DC power transmission lines, while for automotive applications the use of wide bandgap materials will considerably reduce electricity loss during vehicle battery recharging. The greater efficiency possible in operating electric traction drives and the ability to tolerate high operating temperatures can also considerably reduce the size of automotive cooling systems.

Application fields in power device technologies are summarized in **Figure 3**, according to literature [13]. An overview of several materials properties is summarized in **Table 1,** which can be used to compare diamond with other semiconductor's properties.

The high electric breakdown field of wide bandgap materials allows these devices to operate at higher voltages and with lower on-resistance while higher electron mobility and electron saturation velocity allow for higher operating frequency.

However, despite its amazing properties for power electronics, some limitations concerning the wafer diameter, the dislocation density and the surface defects in diamond have to be overcome. The successful solution to these limitations will allow diamond to be the next generation material for power electronics, showing strong potential and promising significant advantages over Si-based conventional electronics. Diamond is superior to its

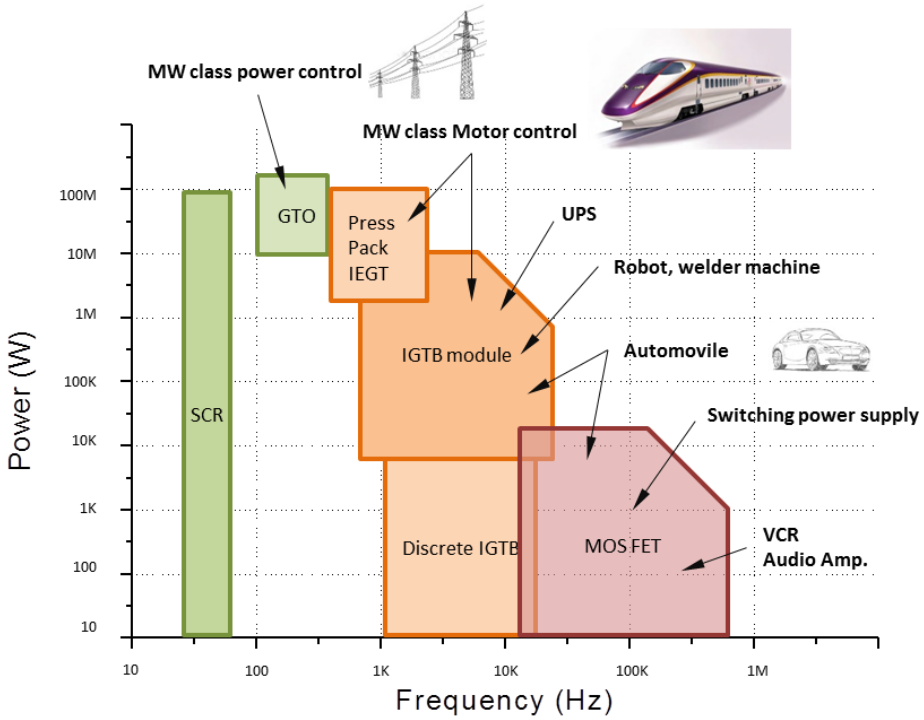

Figure 3: Application fields in power device technologies.

direct competitors from different points of view, and a revolution toward greener and more efficient technologies and devices is anticipated.

On the other hand, there are also significant challenges to consider, including the materials science and technology details and device fabrication. Depending on the proposed solutions, cost reduction plays an important role for effective industrial implementation, production, and market penetration.

It is worth noting that the development of semiconductors, in particular of wide bandgap semiconductors, and progress of their technologies, tends to trigger the development of other materials and new devices and technologies. Initial integration with Si, but in future integration with other materials as well, such as oxides, organics, chalcogenides, and graphene, promises new directions for applied science and technology.

New integrated composite architectures, interfaces, and the utilization of shape and nanoscale synergic effects by using wide bandgap semiconductors could further enhance the electronics revolution, possibly through new physical phenomena.

Table 1: Diamond key properties with respect to that of Si and other wide band gap semiconductors. Grey-background is used to highlight the most relevant values of each parameter.

Property	Symbol (unit)	Si	4H-SiC	GaN	GaAs	Diam.
Band gap	E_G (eV)	1.12	3.23	3.49	1.4	5.45
Breakdown voltage	E_C ($\times 10^{6}$ V.cm^{-1})	0.3	3	3 .5	0.4	10
Electrons mobility	μ_e (cm^{2}.v^{-1}.s^{-1})	1500	980	1250	8500	1000
Holes mobility	μ_h (cm^{2}.v^{-1}.s^{-1})	480	100	200	400	2000
Thermal conductivity	λ (W.cm^{-1}.K^{-1})	1.5	5	1.5	0.46	22
Relative permittivity	ε_r	11.8	9.7	10.4	13.1	5.7
Saturated drift velocity	($\times 10^{7}$ cm^{2}.s^{-1})	1.0	2.0	2.2		1.1
Maximal temperature	T_{max} (K)	410	760	800		1350

To end with this brief introduction, we refer to commercially available Schottky Barrier Diodes (SBD) based in different materials: concerning the blocking voltage of these SBDs, those based on Si are limited to 300V, SiC reach to ≈4kV and GaN-based SBDs are actually working in a 2-6kV range, meanwhile, **extreme dielectric strength** [14] of diamond-based SBDs establishes an operation limit above 10kV(the corresponding values can be consulted in http://www.digikey.es). Finally, the reader is suggested to expand information on the comparison of wide band-gap semiconductors for power electronics devices by consulting literature [15].

Diamond's electrical applications

The use of wide band gap semiconductors in power electronics has been seriously considered since the 80s [16]. **Table 1** lists the main electronic characteristics of silicon, diamond and two other wide band gap materials: silicon carbide (4H-SiC) and gallium nitride (GaN). In addition to its well-known optical and mechanical properties, diamond has exceptional electronic properties. Further information about semiconductor parameters can be found in literature[5].

The maximum voltage difference that can be applied across the material before the insulator breaks down and conduction is related to their bandgap energy. The wide bandgap semiconductor properties offer exceptional breakdown voltage. In addition, a wide band gap induces a low intrinsic carrier density, which allows using devices at higher temperatures without disturbing the properties of the semiconductor material.

[5] http://www.ioffe.ru/SVA/NSM/Semicond/

The excellent mobility of electrons and holes in diamond allows high current densities (which are an important parameter because of the current increase in power) and its high thermal conductivity facilitates the heat dissipation. Finally, the wide band gap ensures greater immunity to radiation, which can be useful in space and nuclear applications, for example. Among the semiconductor considered, diamond has the widest band gap. The combination of these properties makes diamond an ideal candidate for the manufacture of components for power electronics.

The maximal operating temperature is difficult to determine. In the case of silicon, the temperature of use is mainly limited by the increase of intrinsic carrier densities with the temperature. The law describing the variation of the intrinsic carrier density as a function of temperature can be written as:

$$n_i^2 = n \cdot p = N_C \cdot N_V \cdot e^{-E_g/kT} \quad \textbf{Eq. 1}$$

Where n_i is the intrinsic carrier density, n is the number of electrons and p the number of holes. For intrinsic semiconductors at finite temperatures, thermal agitation occurs which results in continuous excitation of electrons from the valence band to the conduction band, and leaving an equal number of holes in the valence band. This process is balanced by recombination of the electrons in the conduction band with holes in the valence band. At steady state, the net result is $n = p = n_i$. With this, the intrinsic carrier concentration at room temperature is $2.4 \cdot 10^{13} cm^{-3}$ in Ge, $1.45 \cdot 10^{10} cm^{-3}$ in Si, $2.1 \cdot 10^{6} cm^{-3}$ in GaAs and $\approx 10^{-27} cm^{-3}$ in diamond. As expected, the larger the bandgap is, the smaller the intrinsic carrier density will be.

The maximum operating temperature of a semiconducting material is that when the calculated intrinsic carrier concentration is $10^{13}\ cm^{-3}$ [17]. This means that intrinsic behavior begins to dominate the extrinsic one. Therefore, there are no more minority and majority carriers and doping do not govern anymore the material behavior. This gives a maximum operating temperature of 290K for Ge, 410K for Si, 588K for GaAs, 760K in SiC, 800K in GaN and 1350K in diamond.

Such intrinsic carrier concentration is not negligible compared with the carrier concentration induced by the low doping of the drift zone of power devices. The values presented are indicative: it is possible, for example, to design silicon components operating at higher temperature. However, if the intrinsic carrier density restricted the use of wide band gap semiconductors at high temperatures, the limitation comes from the environment rather than components that must be adapted to the constraints, including thermo-mechanical.

Silicon is still the dominant material used in electronics, even for high voltage and high power applications. Silicon is a mature, low cost and widely available technology. However, it has significant limitations coming from its moderate thermal conductivity and its small

band gap. Thus its operation is limited at 200°C and a breakdown appears at relatively low electric field. The use of silicon in high power application is followed by relatively high losses and heavy cooling requirements, leading to major costs, space and weight. This is a big disadvantage in key applications such as power conversion, power distribution and transportation. Several groups, either industrial or academic, mainly in Europe, Japan and USA, have recognized and begun to use the huge potentialities of synthetic diamond for implementing electronic devices.

If electronic, thermal and chemical inertness properties of diamond were simultaneously utilized, unprecedented performances would result. Recent progress of epitaxial growth, high boron doping level, surface treatment and improved crystalline quality and availability of synthetic diamond substrates make a solid background for enhancing the development of diamond based applications in several fields like fast and power electronics [18], sensors both in biological media [19] and harsh environment [20], monitoring systems in high radiation beams [21], etc...

Such perspectives have motivated growing industrial developments in England (Element Six Company), Ireland (Diamond Microwave Devices Ltd) and USA (sp3 Diamond Technologies; Appolo Diamond). Recent advances in manufacturing and enlarging synthetic crystalline diamond substrates open a practicable route for growing epitaxially all the layers necessary for building electronic devices. The possibility of p-type doping from traces close to ppb boron concentration up to above one percent, and n-type doping with phosphorus, offers the opportunity of relying only on diamond for elaborating all functionalities.

Diamond electronics holds a fantastic promise. A 10 kV diamond Schottky diode has been reported [22]. Such device exploits the high mobility and power handling properties of diamond. These characteristics would enable individual power devices capable of switching voltage of several kV and kA at temperature beyond 300°C. Kato and co-workers reported a diamond bipolar junction transistor device with phosphorus-doped diamond base layer with a current amplification ratio of around 10 in (111)-oriented diamond at room temperature by utilizing optimized device geometry [23].

Field Effect Transistors for high frequency and high power applications are still in development (this contribution aims to be a step forward in the development of a fully functional device). Structures as hydrogen-terminated diamond FET exhibited a drain-current approaching 80 $mA \cdot mm^{-1}$, with a trans-conductance of 12 $mS \cdot mm^{-1}$, but were unstable at high temperature [24, 25]. A development hetero-junction field effect transistor (HFET) is designed to work at higher temperature. However, a maximum trans-conductance of 0.45 $mS \cdot mm^{-1}$ was reported with AlN/diamond [26].

Using high-quality polycrystalline diamond, MESFET exhibits a maximum transition frequency of 45 GHz, a drain–current density of 550 $mA \cdot mm^{-1}$ and a maximum trans-conductance of 143 $mS \cdot mm^{-1}$. Another kind of transistor, solution gate field effect transistors used the biocompatibility and high frequency properties. Edington et al. shows a maximum gain and a trans-conductance of 3 and 200 $\mu S \cdot mm^{-1}$ respectively [27]. Technological developments were carried out in order to improve the low contact resistance, surface passivation and doping homogeneity.

I.3 Challenges in power electronics

Power electronics is the application of solid-state electronics for the control and conversion of electric power and it also refers to research in electronic and electrical engineering which deals with design, control, computation and integration of nonlinear, time varying energy processing electronic systems with fast dynamics. The capabilities and economy of power electronics system are determined by the active devices that are available. Power electronic devices may be used as switches, or as amplifiers. An ideal switch is either open or closed and so dissipates no power; it withstands an applied voltage and passes no current, or passes any amount of current with no voltage drop. Semiconductor devices used as switches can approximate this ideal property and so most power electronic applications rely on switching devices on and off, which makes systems very efficient as very little power is wasted in the switching devices. By contrast, in the case of the amplifier, the current through the device varies continuously according to a controlled input. The voltage and current at the device terminals follow a load line, and the power dissipation inside the device is large compared with the power delivered to the load.

Several attributes dictate how devices are used. Devices such as diodes conduct when a forward voltage is applied and have no external control of the start of conduction. Power devices such as silicon controlled rectifiers and thyristors (as well as the former mercury valve and thyratron) allow controlling the start of conduction, but relying on periodic reversal of current flow to turn them off. Devices such as gate turn-off thyristors, bipolar junction transistors (BJT), and MOSFET transistors provide full switching control and can be turned on or off without regard to the current flow through them. Transistor devices also allow proportional amplification, but this is rarely used for systems rated more than a few hundred watts. The control input characteristics of a device also greatly affect design; sometimes the control input is at a very high voltage with respect to ground and must be driven by an isolated source. As efficiency is at a premium in a power electronic converter, the losses that a power electronic device generates should be as low as possible.

Semiconductor devices exist with ratings up to a few kilovolts in a single device. Where very high voltage must be controlled, multiple devices must be used in series, with networks to equalize voltage across all devices. Switching speed is a critical factor since the slowest-switching device will have to withstand a disproportionate share of the overall voltage. The current rating of a semiconductor device is limited by the heat generated within the dies and the heat developed in the resistance of the interconnecting leads. Semiconductor devices must be designed so that current is evenly distributed within the device across its internal junctions (or channels); once a "hot spot" develops, breakdown effects can rapidly destroy the device.

The main benefit of the power MOSFET is that the base current for BJT is large compared to almost zero for MOSFET gate current. Since the MOSFET is a depletion channel device, voltage, not current, is necessary to create a conduction path from drain to source. The gate does not contribute to either drain or source current. Turn on gate current is essentially zero with the only power dissipated at the gate coming during switching. Losses in MOSFETs are largely attributed to on-resistance. The calculations show a direct correlation to drain source on-resistance and the device blocking voltage rating, BV_{dss}.

Switching times range from tens of nanoseconds to a few hundred microseconds, depending on the device. MOSFET drain source resistances increase as more current flows through the device. As frequencies increase the losses increase as well, making BJTs more attractive. Power MOSFETs can be paralleled in order to increase switching current and therefore overall switching power. Nominal voltages for MOSFET switching devices range from a few volts to a little over 1000 V, with currents up to about 100 A or so. Newer devices may have higher operational characteristics. MOSFET devices are not bi-directional, nor are they reverse voltage blocking.

We can focus the main challenges in these few points:

- **Drift:** In a p-n junction in the OFF state, the breakdown voltage is determined by the architecture, doping and thickness of the drift zone and by the characteristics of the material (field maximum value which does not trigger the avalanche phenomenon by carrier multiplication). When switching from ON to OFF state (in the case of the bipolar devices) the holes in the n-region must recombine to be effective for blocking. The time required is called recovery time and constitutes the major handicap in bipolar components. In the case of unipolar devices, the time required to switch from ON to OFF state is very short. Switching times result in losing a significant electrical power (switching losses). For high frequency operation, it is thus preferable to use unipolar components.
- **The thermal limitation:** The main types of losses in power electronics are conduction and switching losses. The energy dissipated due to conduction losses

and switching induced heating of the components, and the temperature increased in junction may impair their functioning (even leading to their destruction), so the dissipated energy must be extracted by cooling systems. There are several ways to resolve this issue: with cooling systems, from a research conducted on the components (to limit power thermal losses) or in devices able to operate at higher temperature, to overcome requirements in terms of cooling.

- **Increase the power switched:** Transportation of electric energy, from its production site to its place of use, is a key problem in electronics. This should be made at high voltages and, because electrical losses in the line are due to the Joule effect, it is desirable to increase the voltage of power lines, and so, to reduce the current. The increase in the power spent by the load at constant supply voltage consists, for the power component, to provide a higher current. It can be achieved by increasing the voltage of the current rating of power components.
- **Increase the frequency:** An increase in operating frequency induces a decrease in the value of capacitors an inductors used (in a power electronics module, the value of passive elements surrounding the active one varies inversely with frequency), which results in a decrease in the volume occupied by the capacitors. The diamond transistor presents the function to work at high frequency with low thermal losses being dissipated by the components.

The unique properties of CVD diamond, particularly its large bandgap, high dielectric strength and high thermal conductivity, suggest that the material should be an ideal semiconducting medium for high-voltage and high-power switching applications [18]. If we now consider diamond as an alternative to overcome the difficulties mentioned above, it can be seen in **Table 1** that it has a range of properties that offer the potential to extreme device performance. Even in the group of wide bandgap materials, which includes silicon carbide (SiC) and gallium nitride (GaN), diamond can be considered extreme on its intrinsic electronic properties. It is the unmatched combination of highest bulk thermal conductivity, high carrier mobility and high breakdown voltage that makes diamond a truly

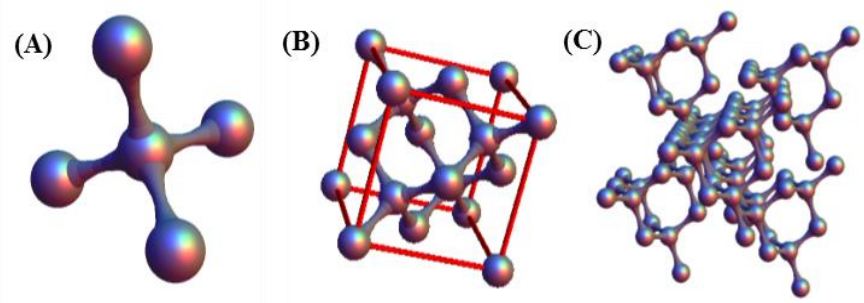

Figure 4: Wolfram's Mathematica simulation of carbon tetrahedron (A), diamond unit cell (B) and diamond crystal fragment (C).

multifunctional material and will allow applications in environments simply too demanding for other materials and devices. As a result, diamond electronic devices, such as power diodes and high frequency field-effect transistors (FETs), can be expected to deliver outstanding performance.

I.4 Diamond and its properties

Diamond is a material composed of the single element carbon. In diamond each carbon atom is tetrahedrally coordinated and covalently bonded to four other carbon atoms. Carbon atoms in diamond can be placed in two crystal lattices, with cubic and hexagonal symmetry respectively. However, the dominant allotrope for both natural and synthetic diamond is the cubic diamond structure. The hexagonal symmetry is rarely found in nature as the mineral *lonsdaleite*.

Diamond owes its hardness to its crystalline organization. The crystal lattice of diamond is one of the most studied ones; it's well known that diamond has the highest hardness and thermal conductivity of any bulk material while remaining an electrical insulator, mainly due to its structure, based on a continuous network of tetrahedrally bonded carbon atoms in which extremely strong covalent bonds are formed between sp^3-hybrid orbitals and low phonon scattering is produced.

The C–C bond length is 154.448 pm. The crystalline structure is of cubic symmetry with unit cell dimension $a = 4/\sqrt{3}\ r_{CC} = 356.682$ pm, containing eight carbon atoms per unit cell, density is established at $\rho = 3.515\ g \cdot cm^{-3}$, mobility at 300K is around 2200 $cm^2/V \cdot s$ for electrons and 1600 $cm^2/V \cdot s$ for holes. The structure can be characterized as two interpenetrating face-centered cubic lattices, displaced by a/4 in each dimension (as spotted in **Figure 4,** where carbon tetrahedron, diamond unit cell and diamond crystal fragment for the idealized crystal structure are shown). On the other hand, natural diamonds are classified as follows:

- **Type Ia** - This is the most common type of natural diamond, containing up to 0.3% nitrogen.
- **Type Ib** - Very few natural diamonds are this type (~0.1%), but nearly all synthetic industrial diamonds are. Type Ib diamonds contain up to 500 ppm nitrogen.
- **Type IIa** - This type is very rare in nature. Type IIa diamonds contain so little nitrogen that it isn't readily detected using infrared or ultraviolet absorption methods.

- **Type IIb** - This type is also very rare in nature. Type IIb diamonds contain so little nitrogen (even lower than type IIa) that the crystal is a p-type semiconductor.

Synthetic industrial diamonds

Synthetic industrial diamonds are usually produced by of High Pressure High Temperature Synthesis (HPHT). In HPHT synthesis, graphite and a metallic catalyst are placed in a hydraulic press under high temperatures and pressures. After a few hours the graphite is transformed into diamond. The resulting diamonds are usually a few millimeters in size and too flawed for use as gemstones, but they are extremely useful as edges on cutting tools and drill-bits and for being compressed to generate very high pressures.

On the other hand, a process called Chemical Vapor Deposition (CVD) is currently used to deposit thin films of polycrystalline diamond. CVD technology makes possible to put 'zero-wear' coatings on machine parts, use diamond coatings to draw the heat away from electronic components, fashion windows that are transparent over a broad wavelength range, and take advantage of other properties of diamonds.

Diamond doping

In contrast with silicon manufacture and with other more common semiconductors, the high compacity of the diamond lattice offers a very small volume to allow impurities to substitute carbon atoms [28]. Few candidates are suitable for diamond doping; principal dopant atoms found are boron, nitrogen, phosphorous, silicon, nickel and sulphur. By ion-implantation techniques, other impurities can be introduced but the compensation resulting from crystal damage is not negligible and complex annealing techniques are required.

If diamond p-type doping is available from traces close to ppb boron concentration up to above one percent, and n-type doping with phosphorus too, some intrinsic problems occur to get high conductive layers. The success of the doping resides in the diamond ability to receive the dopant (depends on crystal orientation), in the compensation ratio (depends of the doping technique and the crystal orientation) and in its ability to incorporate on substitutional sites where the dopant will be active (acceptor and donor ratio).

- n-type diamond has not been found in nature yet. Since the CVD growth technique exists there have been quite a few attempts to dope diamond n-type. Nitrogen is a natural dopant but it doesn't yield any shallow donor. Since 15 years a few groups in the world were able to dope diamond with phosphorus, and different approaches for the n-type doping of diamond are still under research [29, 30].

- Even when, initially, aluminum was supposed to be the main acceptor in p-type diamond, it has been shown that boron is in fact the only the p-type dopant that can be incorporated with high reproducibility [31].

Band diagram for a semiconductor containing acceptor (E_a) and donor (E_d) impurities is shown in **Figure 5** (a); it can be observed that additional energy levels are created inside the forbidden band energy. **Figure 5** (b) shows ideal band diagram of diamond with dopants. Please note that, when doping a semiconductor, the Fermi level is modified as shown in **Figure 5** (a). We will use Boron as main dopant during this thesis, which means p-type diamond due to acceptor impurities (charge carriers will be holes).

An important point in the band diagram is the Fermi level (E_F). The Fermi level of a body is a thermodynamic quantity, and its significance is the thermodynamic work required to add one electron to the body (or equally the work obtained by removing an electron). A precise understanding of the Fermi level (how it relates to electronic band structure in determining electronic properties, how it relates to the voltage and flow of charge in an electronic circuit) is essential to an understanding of solid-state physics.

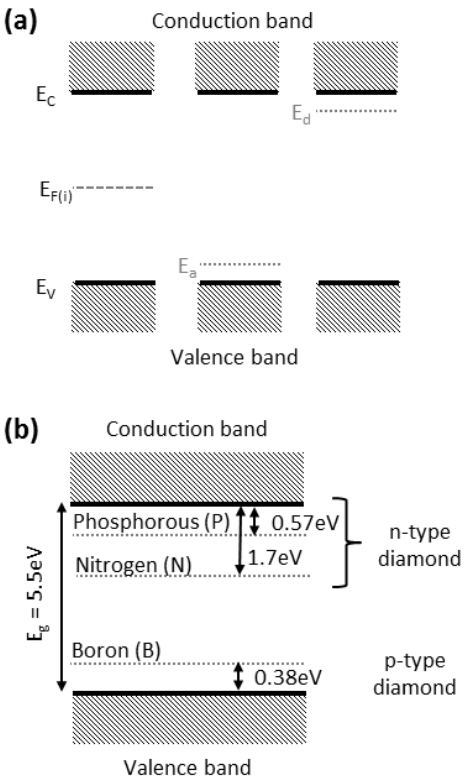

Figure 5: Band diagram of an ideal semiconductor without dopants and with acceptor/donor impurities (a) and band diagram of diamond dopants (b)

In a band structure picture, the Fermi level can be considered to be a hypothetical energy level of an electron, such that at thermodynamic equilibrium this energy level would have a 50% probability of being occupied at any given time, if it does not lie in the forbidden gap. One can summarize the definition of the Fermi level as the top of the available electron energy levels at low temperatures. Such energy level is approximately located in the middle of the forbidden band energy in a semiconductor; please see **Figure 5** (a).

However, this is a very simplified picture of real band structure of semiconductors. Real band diagrams have a dependency on the lattice, the interactions of bonding with antibonding orbitals and depends on the Bloch function solution (in whose calculations, simplified assumptions as a "third parallel neighbor" approach and a Hartree-Fock type

potentials are used). Calculations of real band diagram of diamond, carried out with the previously cited assumptions can be found in literature [32, 33].

To experimentally determine the boron content in real diamond samples, the most commonly used techniques are:

- Secondary Ion Mass Spectrometry: A destructive experiment in which accelerated ions are colliding with the sample, milling it (in a similar way of that of the Focused Ion Beam previously spotted). The sputtered atoms are then "weighted" through spectroscopy techniques, thus making possible to stablish a relation between the milling depth and the type/quantity of atoms present at each defined depth.
- Cathodoluminescence: is a nondestructive technique (please see Annex I) in which an electron beam is used to create light emission from the sample. This light comes from recombination of a variety of particles. Among them, excitons (a bond of an electron-hole pair) are sensitive to variations in the crystal lattice such as defects or active doping.

For high boron doped layers ([B] > 10^{18}cm^{-3}), cathodoluminescence technique cannot be used. However, we successfully applied this technique for low doped diamonds [34]. Usually, dopants are incorporated into the diamond lattice during the growth. However, the variety of doped structures available through this technique is reduced. For this, dopant implantation through ion implantation is attracting more interest at the present time.

Doping-induced metal-to-insulator (MIT) transition

Metal-to-insulator transition in diamond has been widely studied in literature [35, 36], concluding in a critical boron (main p-type dopant in diamond) concentration n_c between 4 and $5\cdot10^{20}$cm^{-3}. It has been found that, in p-type diamond, the critical boron doping of the MIT coincide with that for superconductive transition. Some of the critical exponents of the MIT were determined in [36]. Because diamond has a simple crystallographic structure and does not involve magnetism, it motivates special interest, as far as it can become an attractive model system for the study of superconductivity in low-dimensional structures of controlled dimensions and where disorder can hopefully be restricted to the chemical randomness of an ideal substitutional alloy.

- [B] < ~10^{14} at·cm^{-3} insulator
- ~10^{14} < [B] < ~10^{20} at·cm^{-3} semiconductor
- $4\cdot10^{20}$ < [B] < $5\cdot10^{20}$ at·cm^{-3} superconductor

Critical temperature as a function of the boron content, conductivity vs boron content as a given temperature as well as more detailed calculations and discussion on this topic can be found in literature [36].

I.5 Relevant properties for electronic power devices

Until the advent of single-crystal diamond synthesized by CVD processes, most measurements of electronic properties were made on rare, carefully selected Type IIa natural diamonds (Type IIa diamonds are very rare in nature and have the lowest levels of nitrogen impurity as measured by spectroscopic techniques, below $10^{17}cm^{-3}$, and no specific optical absorptions arising from H or B). These measurements have provided benchmarks against which CVD diamond can be compared.

Additionally, where diamond really scores is that it far outperforms any other material in terms of its ability to insulate very high voltages across very thin layers of the material (see **Figure 6** (a), where ON-resistivity vs **breakdown field** is plotted for various materials). The lower the insulation strength the more base material you need to start with (which is a big issue when wide bandgap semiconductors are already at least 10 times the cost of silicon), but more importantly the slower the device operates - which is why, in the case of power semiconductors, 6,500V appears to be the ultimate practical limit for silicon insulated gate bipolar transistors (IGBTs).

Systems such as power converters and switches are made of silicon or silicon carbide at the moment. Thanks to the superior properties of diamond, the size of such devices could be dramatically reduced while the performances would be improved. For instance, thanks to the weight gain (less elements, reduced cooling system) and efficiency improvement, the use of diamond in public transport sector would allow reducing the losses by a factor of three with respect to the use of Si.

Properties listed in **Table 1** also stablishes a relation between the ON-state resistivity and the breakdown voltage for different semiconductor materials for power device applications, summarized in **Figure 6** (b), it can be observed that there is a limitation between them for the conventional power devices. To expand information about the relationship between the specific ON resistance of the drift region and the maximum achievable breakdown field in different materials, we refer to the plot of [37].

It can be appreciated that diamond presents promising properties that makes it an ideal material for the future power devices. Among these properties, the most relevant for power

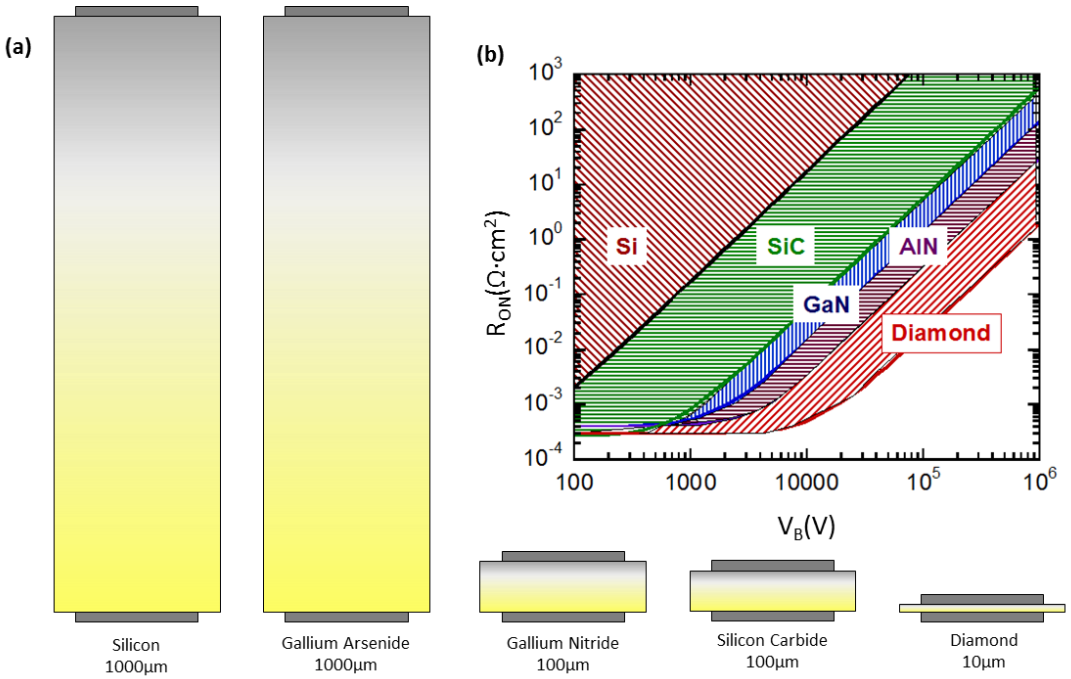

Figure 6: (a) Amount of material needed to isolate 10000V (source: evincetechnology.com) and R_{ON} vs Breakdown voltage for various semiconductors (b). The shape of this graph stablishes the range of operation in which a power device based in different semiconductor can operate properly.

device operations, compared with its direct competitors, are listed below. We do refer to **Table 1** to compare diamond properties with those of other semiconductors.

We can summarize the main advantages of using semiconducting diamond in power devices in three key points, that will be briefly discussed:

- High thermal conductivity
- High carrier mobility
- High breakdown field

Carrier mobility

Single-crystal CVD diamond exhibits both the highest electron and hole mobilities at room temperature of any wide-bandgap semiconductor, which is clearly an immensely attractive property. Electron and hole mobilities of about 4500 $cm^2V^{-1}s^{-1}$ and 3800 $cm^2V^{-1}s^{-1}$, respectively, have been measured in intrinsic, single-crystal CVD diamond at room temperature. Corresponding values for 4H-SiC are 900 $cm^2V^{-1}s^{-1}$ for electrons and 120 $cm^2V^{-1}s^{-1}$ for holes.

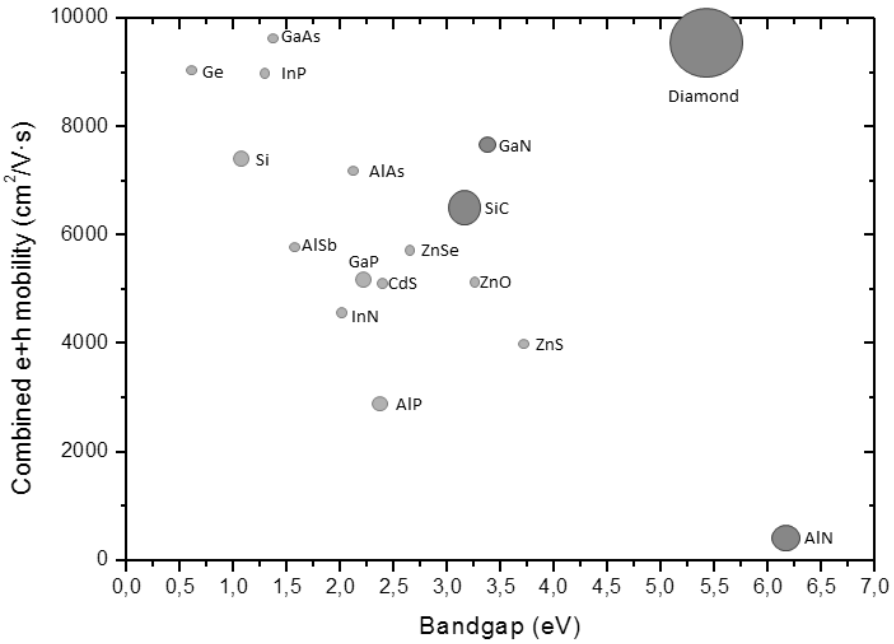

Figure 7: Comparison of diamond's combined carrier mobility, bandgap and thermal conductivity with other semiconductors (area of circle is proportional to the material's thermal conductivity).

Published data [38] indicate that the hole mobility in diamond drops as $T^{-1.5}$ in the interval 300–400 K, which is generally considered to be indicative of acoustic phonon scattering in high crystallographic quality, intrinsic samples as assessed by Isberg et al. [38]. However, Somogyi [39], points out that this reduction in mobility as a function of temperature (in this temperature range) could also be the result of scattering from incomplete ionization of common impurities within the diamond material. At temperatures above about 400 K, hole mobility falls more rapidly with an exponent in the range –2.5 to –3.66.

Even so, mobilities of $\mu_h > 2000$ $cm^2V^{-1}s^{-1}$ at 400 K and $\mu_h > 1000$ $cm^2V^{-1}s^{-1}$ at 500 K have been measured, making high temperature device operation possible. Impurity scattering causes the mobility to drop with increasing dopant concentration. Fox et al.[40] have measured hole mobility dropping from ~1500 $cm^2V^{-1}s^{-1}$ to ~1000 $cm^2V^{-1}s^{-1}$ in B-doped CVD samples with B concentrations in the range $5\cdot10^{16} – 2\cdot10^{18}$ cm^{-3}. Unpublished data on Element Six samples have shown a hole Hall mobility of 450 $cm^2V^{-1}s_{-1}$ for a B concentration of ~10^{19} cm^{-3}. Thus even highly B-doped diamond can exhibit good hole mobility. Of course, in devices where the active region consists of purely intrinsic diamond, the drop in mobility with dopant concentration is not relevant; however, the challenge is then to achieve impurity-free material. **Figure 7** comparison of diamond's combined carrier

mobility, bandgap and thermal conductivity with other semiconductors [18] (area of circle is proportional to the material's thermal conductivity).

Saturation velocity

In high electric fields, the conductivity is determined by the saturation velocity rather than by the mobility. The velocity of charged carriers is saturated at high fields by the generation of optical phonons in the crystal lattice. A high saturation velocity is advantageous for the performance of FETs operating at high frequencies. The saturation velocity, v_s, is given by:

$$v_s = \sqrt{\frac{8E_{opt}}{3\pi m^*} tanh\left(\frac{E_{opt}}{2kT}\right)}$$

…where E_{opt} is the energy of (k = 0) optical phonons and m^* is the effective mass of the charge carriers. High optical phonon energies thus tend to give a high saturation carrier velocity. Diamond has the highest optical phonon energy E_{opt} = 160 meV of any semiconductor. Experimentally determined values of *vs* vary significantly in the literature but most measurements indicate v_s = 0.85–1.2·10^7cm·s^{-1} and v_s = 1.5–2.7·10^7cm·s^{-1} for holes and electrons, respectively.

Of the other wide-bandgap semiconductors, only SiC reaches values comparable to those of diamond. However, diamond has a real advantage in that its saturation velocity is reached in fields of ~10 kV/cm, whereas for SiC, the velocity saturates at fields close to its practical electrical breakdown strength. Such high fields can be very difficult to approach in devices.

Carrier lifetime

Carrier lifetime (τ) is important in designing bipolar (minority carrier) components. It is equally important for devices where electron-hole pairs are generated by radiation, such as radiation detectors. For unipolar devices, the recombination lifetime is of less interest. However, a high carrier lifetime is an indication of a low impurity and defect concentration, and thus an important material quality indicator. Carrier lifetimes of more than 2 μs have been measured in single crystal CVD diamond, which is similar to the best data in 4H-SiC. In natural diamond, lifetimes of less than a nanosecond are typical. The higher τ is, the higher the diffusion length L is, thus improving the detectivity. On the other hand, lower τ values are useful for fast switching applications, like those of high frequency operation devices. Finally, the higher the purity of the material, the higher the τ, dopants makes to decrease the τ value.

Dielectric breakdown field

For many devices, a semiconductor material with a high electric breakdown field is desirable. This is true not only for power devices, such as diodes and switches intended to block several kilovolts, but also for high-frequency FETs. The reason is that, if higher electric fields can be tolerated, the devices can be designed with smaller dimensions, which results in faster switching. Intrinsic breakdown in semiconductors is inherent to the material. It results from impact ionization and subsequent avalanche breakdown.

On the other hand, extrinsic breakdown at defects is dependent on crystalline quality and improves with better quality material. Diamond exhibits the highest predicted breakdown field of any semiconductor with values in the range 5–10 $MV \cdot cm^{-1}$ to be reasonably expected. In contrast, 4H-SiC and GaN exhibit measured breakdown fields of 3 $MV \cdot cm^{-1}$ and 5 $MV \cdot cm^{-1}$, respectively.

Thermal properties

Diamond has the highest thermal conductivity of any material known. High-purity, single-crystal CVD diamond has a thermal conductivity in excess of 2200 $Wm^{-1}K^{-1}$ at room temperature, falling to around 700 $Wm^{-1}K^{-1}$ at 773 K.

The extremely high thermal conductivity of diamond enables diamond-based devices to handle high powers more simply. This is because the first stage of thermal management, getting any heat away from the point at which it is produced, is facilitated by the device itself rather than by an add-on solution. In some integrated circuits, a MOSFET is surrounded by a thick oxide (called the field oxide to distinguish it from the gate oxide) or a trench filled with insulator to electrically isolate if from adjacent devices.

I.6 Motivation: impact of the interface configuration in diamond devices

The carrier flow across the device layers in MOSFETs or diodes, is based on the electrostatic control of the band curvature at the oxide-semiconductor or metal-semiconductor interface. The latter is achieved by modifying the biasing conditions. Thus, bands fitting and band bending at the metal-diamond interface should be precisely controlled. Impurities at this interface modify the band profile and, thus, the device is very sensitive to such aspects.

Nowadays, commercially available Schottky diodes and MOSFETS are based on SiC. Before SiC, commercial MOSFET were formed only with Si, because sufficient electronic passivation of dangling bonds at the semiconductor surface could only be achieved by thermally grown SiO_2 as the gate dielectric. The fact that thermal oxidation of SiC also creates SiO_2 was a significant motivating factor to attempt the development of MOSFET in SiC.

Numerous problems were solved, but one significant problem persisted for a long time: electronic passivation of the SiC-SiO_2 interface, created by either dry or wet oxidation of SiC, remained insufficient because the electrons attracted to the surface of SiC by the gate voltage would be trapped by a very high density of active defects at the interface. This problem was tentatively solved in SiC by nitriding the SiC-SiO^2 interface, either grown or annealed in an NO atmosphere at temperatures above 1000ºC [41]; but still interfacial problems remain to produce reliable SiC MOSFETs.

However, such technological step has not been successfully solved in diamond, mainly because surface properties of diamond are quite different between hydrogen-terminated (H-terminated) and oxygen-terminated (O-terminated) surfaces. H-terminated diamond has p-type surface conductivity even in undoped diamond [42]. Thus, undoped H-terminated diamond has potential for electronic device applications, because of its p-type surface conductivity. On the other hand, O-terminated diamond is insulating. This means that the O-terminated surface has different electrical properties from the H-terminated surface.

The H-terminated surface is positively polarized due to the polar covalent bonding of H-C. In the H-terminated surface, the difference in electronegativity[6] between carbon (2.54) and hydrogen (2.1) partially induces the electron move from hydrogen atoms to carbon atoms. In contrast, the O-terminated surface is negatively polarized, because the electronegativity of oxygen (3.44) is larger than that of carbon [43]. Thus, the termination of the diamond surface is a key parameter that will govern the electrical properties of the interface:

Hydrogen-terminated diamond surfaces:

Diamond hydrogenated surface shows a negative electronic affinity of -0.9eV [44]. Lower potential barriers are implemented on the hydrogen-terminated diamond surfaces, due to the dipole $H^{+\upsilon}$-$C^{-\upsilon}$ [45, 46] responsible for the negative electron

[6] Electronegativity, symbol χ, is a chemical property that describes the tendency of an atom or a functional group to attract electrons (or electron density) towards itself. An atom's electronegativity is affected by both its atomic number and the distance at which its valence electrons reside from the charged nucleus. The higher the associated electronegativity number, the more an element or compound attracts electrons towards it.

affinity of these diamond surfaces (where υ is the averaged fraction of the elementary charge per atom). However, chemical stability is not guaranteed at temperatures as high as in the oxygen-terminated case, and reverse current densities turn out to be hardly weaker than 10^{-7} A/cm^2 at room temperature, still higher than the thermionic limit [47, 48].

Oxygen-terminated diamond surfaces:

Diamond oxygenated surface electronic affinity is reported between 1.0 and 1.7eV [44, 49, 50]. In case of oxygenated diamond surfaces, potential barriers near or higher than 2eV, stable at temperatures higher than 500ºC have been obtained during the development of this thesis, but reverse current densities and ideality factors in Schottky Barrier Diodes were much greater than expected from the thermionic mechanism alone at least at room and moderate temperatures.

Because of an inverted electric dipole at the oxygenated surface of diamond, the largest potential barriers are generally obtained with either noble (Au) or transition metals deposited on this type of surface [51], but some authors shows that thermal treatments up to 500 or 600ºC are able to decrease the barrier height down to 1.2eV [52], probably because of the cancellation of the electric dipole $O^{-\upsilon'}$-$C^{+\upsilon'}$, still preserving a good adhesion of the metallic layer.

In this respect, diamond surface oxygenation is known to be an efficient way to minimize electronic states on diamond surface. Unfortunately, the Schottky barrier height of oxygen-terminated surfaces are generally larger than 2eV, meaning high forward losses. Moreover, these structures can be thermally unstable due to dissociation of oxygen bonds.

For that, we will focus on the of oxygen-terminated diamond/metal and diamond/oxide interfaces as a key problem to be solved. Additional knowledge is required and will help to reduce the density of active defects present in the interface, thus leading to performance improvements in the related power device.

I.7 Objectives: unipolar devices studied in this work

Building well defined interfaces at nanometer scale is especially necessary for electrical rectifiers, which can gain high benefits from the bulk properties of boron doped diamond (like it very high thermal conductivity, hole mobility and electrical breakdown field) if specific properties of the interface are also fulfilled.

These are mainly the good adhesion, thermal and chemical stability at elevated temperatures, compatible with the superior characteristics of diamond and potential barriers ensuring both low electrical losses under forward voltage and minimal reverse currents even at high temperatures. In fact, the main problem to make efficient power devices is the large ionization energies of the acceptor and donor impurities: 380 meV for the boron acceptor and 570 meV for the phosphorus donor. The ionization rate of dopants at room temperature is low and the resulting high series resistance of the active layer is not compatible with some device operation (like metal semiconductor field effect transistor (MESFET), bipolar junction transistor (BJT), or junction field effect transistor (JFET)).

These poor rectifying current-voltage characteristics have been assigned to inhomogeneous and defective interfaces, especially with carbide forming metals [51, 53, 54]. In order to overcome this problem, solutions based on two dimensional (2-D) hole gas are under investigation:

(i) H-terminated diamond field effect transistor (FET) using hole accumulation layer. Such transistors demonstrate high frequency operation but deteriorate under high temperature conditions [55].

(ii) Boron δ-FET consisting on a thin heavily doped (metallic) layer between two intrinsic layers resulting theoretically in high mobility (due to delocalization of carrier away from ionized impurities induced by confinement). However, obtaining a very thin layer (<2 nm needed [56]) is a technological challenge.

(iii) Diamond/nitride heterojunctions FET [57] has been recently proposed and their electronic properties are under investigation at this moment.

In power electronics, the field effect transistor and the Schottky diode are two complementary switches for the commutation cell in a power converter. Recently, in the framework of collaboration between Institut Néel (France) and NIMS (Japan), a 10kV diamond Schottky diode was reported [58].

In order to study the relation between the diamond-interface configuration and the undesired electric behavior, several architectures and metallic stacks are investigated:

a) **Schottky Barrier Diodes:** Oxygen-terminated diamond-metal interfaces are the basic component of power SBDs. Here, we will study the thermal evolution of the oxygen-terminated surface in relation with the contacting metal stack. For that, two different metals will be used:
    a. Zr , that is an easily oxidizable metal, which is expected to be able to hold oxygen at the interface, even at high temperatures.

b. WC which is a carbide-formed metal, and is expected to produce better stability up to 600K, due to the formation of an interfacial bonding between WC and diamond

b) **MOS Al/Al_2O_3/diamond** capacitors are needed for the development of MOSFET structures. Here, we study the effect of the oxygen termination in different diamond MOS capacitors, as well as we evaluate the impact of the oxide thickness variations in the electric response of the related device.

c) **MOS δ-FET** was created once reliable and reproducible diamond MOS structures were improved. Here, we do an attempt for creating a diamond-based FET based in an oxygen-terminated diamond surface and a δ-shaped channel.

We can summarize the main goals to be achieved in this work as follow:

- Contribute to improving the definition of interfaces at nanometer scales in diamond-based power devices.
- Nano-characterize the effect of thermal treatments in a variety of oxygen-terminated diamond-metal interfaces.
- Relating the interface characteristic with the corresponding electrical behavior of the related device.

Chapter II: Materials and methods

In this chapter, we briefly introduce the different samples/devices that have been characterized during this PhD project. A description of the growth process and a review of each final structure will be presented. Later on, we will introduce the some key techniques that have to be used for the nano-characterization of diamond-contact interfaces.

II.1 **Description of the samples:** Here, we present the different specimens and interfaces that have been nano-characterized in this work, structured as follow:

- **Diamond-based Schottky Barrier Diodes**
- **Metal-Oxide-diamond structures**
- **Diamond δ-doped MOSFET**

II.2 **Experimental techniques** used for the chemical and structural nano-characterization of the previously presented interfaces are briefly presented as follows:

- **Focused Ion Beam (FIB)**
- **Damages produced by FIB operations**
- **EELS analysis of the interface**

II.1 Description of the samples

During this work, a variety of diamond-based electric devices will be studied. Here, we summarize the structure of all the studied samples with their respective label. We will also present a brief description of the growth process of each device.

Diamond-based Schottky Barrier Diodes

Diamond-based SBD are composed by an oxygen-terminated diamond surface and a metallic stack, the resulting diamond/metal contact is characterized (structurally and electrically) before and after each annealing step.

To do the oxygen termination in the diamond surface, a Vacuum Ultra-Violet treatment is carried out [59], as illustrated in **Figure 8**. The fabrication process of the SBD structures is produced according to the following sequence:

1. Hydrogen-terminated surface, resulting from the MPCVD growth of the boron-doped homoepitaxial diamond film
2. VUV-light illumination of the oxygen atmosphere. It's difficult to remove hydrogen-termination with the commonly used UV/ozone treatment (based on a low—pressure mercury lamp [43]). The VUV/ozone treatment used here is a convenient and effective mean to form an oxygen-terminated diamond surfaces [59].
3. Oxygenation of the surface
4. WC contact deposition (magnetron sputtering [60]).

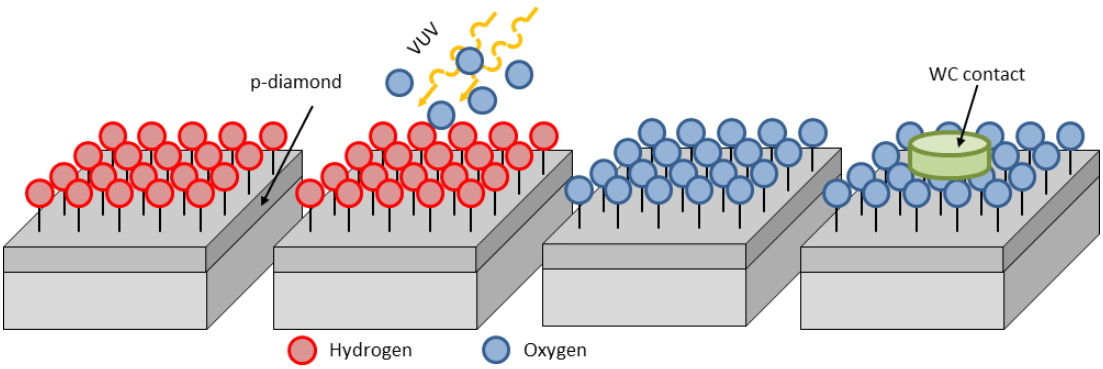

Figure 8: Schematic description of the fabrication process flow of the SBD using VUV/ozone treatment.

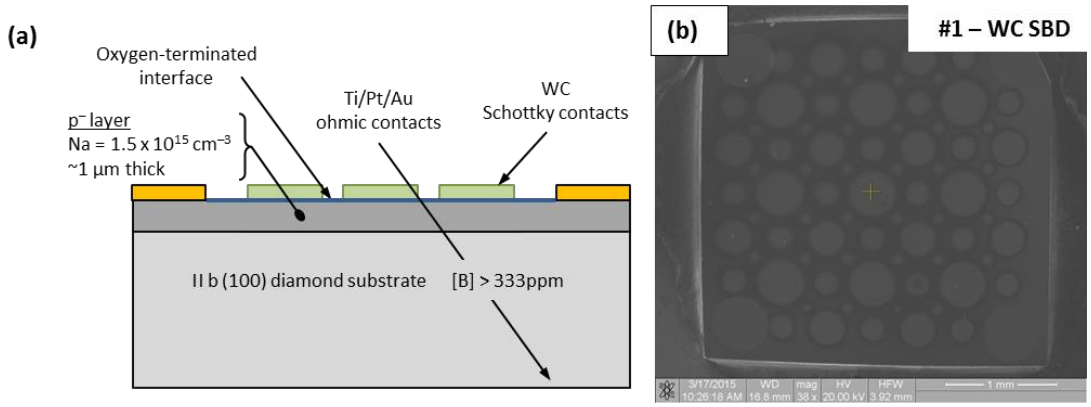

Figure 9: (a) Schematic of the final WC-based SBD structure. (b) SE image of the bulk specimen, WC contacts can be appreciated all over the surface.

The resulting structures are expected to present an oxygen-content layer between the diamond substrate and the metal stack. However, oxygen termination can be altered by the metal sputtering, as will be shown in future chapters.

Note that oxygen termination is expected to have an impact in the electric behavior of the related device, meaning that a nanostructural characterization of the interface is needed. Here, we study two different approaches for SDB structures: WC-based and Zr-based SBDs.

#1. WC-based SBD[7]

To create WC-diamond SBD, a lightly boron-doped diamond layer, with an acceptor concentration of $N_A \approx 10^{15} cm^3$, were grown by microwave plasma-assisted chemical vapor deposition (MPCVD) on $3x3mm^2$ (100)-oriented diamond substrate HPHT type-Ib single crystal. Graphitic phases remaining on diamond after the epitaxy were eliminated by a boiling acids mixture. Ohmic contacts made of Ti/Au were deposited on the four corners of the p-layer surface by E-beam and annealed under vacuum at 600C during one hour.

After the creation of the ohmic contacts, the p-layer surface was oxidized during 30 min by a vacuum-ultraviolet light (VUV)/ozone treatment at room temperature. Finally, a 1:1 stoichiometric WC was deposited through a metallic shadow mask by conventional magnetron sputtering, whose base pressure was less than 10^{-6}Pa, for making Schottky contacts. The resulting structure is presented in **Figure 9**.

[7] WC-based Schottky barrier diodes were designed and fabricated by A. Fiori, T. Teraji and Y. Koide, members of the National Institute for Materials Science. 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan.

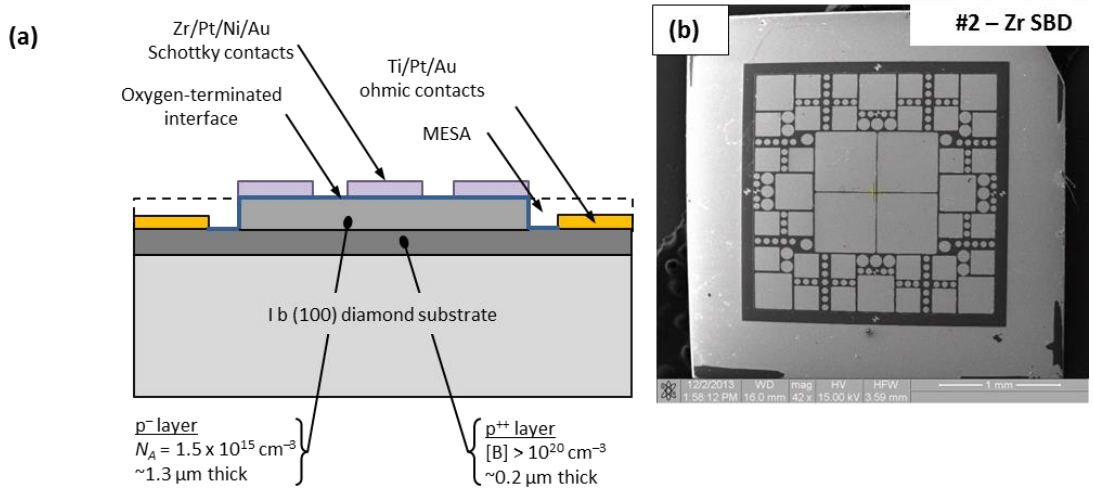

Figure 10: (a) Schematic of the final Zr-based SBD structure. (b) SE image of the bulk specimen, studied Schottky barrier diodes corresponds with the four squared-shaped contacts at the center of the sample.

#2. Zr-based SBD[8]

For the fabrication of the diode, active layer (p^- layer) is grown on a highly conductive epi-layer (p^+ layer) grown on an insulating diamond substrate. This design is generally used in order to get an electrical behavior close to that of the vertical structure, as shown in **Figure 10** (a). The active layer is etched back in order to fabricate the ohmic contact on the top of the highly doped layer, thus delineating the pseudo-vertical structure. This fabrication process involves the epitaxy of active and p^+ layer, the ohmic contact fabrication and the Schottky contact deposition.

This choice was motivated by the current unavailability of commercial electrical grade highly conductive diamond substrates. The latter is, probably, the major obstacle towards vertical diamond Schottky diodes fabrication (even when vertical structures are the optimal geometrical configuration for SBDs).

To do so, heavily boron doped (p^+) and non-intentionally doped (p^-) homoepitaxial diamond layers were grown. First, a 200nm thick p^+ layer with a nominal doping level of 10^{20}at·cm^{-3} was grown in order to use it as a substrate for a 1.3µm thick p^- layer (with an average doping close to 10^{15}cm^3). An Inductively and Capacitively coupled Plasma (ICP) etching step was performed to reduce the p^- layer to a 2x2mm^2 square centered at the middle of the

[8] Zr-based Schottky barrier diodes were designed and fabricated by A. Traoré, P. Muret, A. Fiori, D. Eon, E. Gheeraert and J. Pernot, members of the CNRS, Institute Néel, F-38042 Grenoble, France.

p^+ layer, thus delineating a pseudo vertical Schottky diode structure. Then, an ozone treatment produced by deep UV light was performed to passivate the drift layer surface before Schottky contacts deposition. Finally, an electron beam evaporator was used to deposit Zr contacts and the first metallic material was subsequently covered with different cap layers to obtain the metallic stack.

Table 2: Summary of the Schottky Barrier diodes studied in this work, contacting metal and annealing temperature are presented.

	Contact metal	Annealing temperature (K)
#1A	WC	300
#1B	WC	600
#1C	WC	700
#2A	Zr	300
#2B	Zr	623
#2C	Zr	723

As for the vertical structure, the diode performance will be in part related to the crystal quality of the p^+ layer and furthermore to its doping level. A high quality p^+ layer will favor the minimization of defects inside the ac tive layer (p^- layer). Moreover, this layer has to be sufficiently doped to get a metallic behavior to minimize its contribution to the diode serial resistance and achieve a negligible ohmic contact resistance. The resulting final structure is presented in **Figure 10**.

Metal-Oxide-diamond structures[9]

The studied Al/Al_2O_3/diamond MOS structures were reported by Chicot et al in [61]. Such structures are here characterized by a combination of TEM techniques. In such structures, the Al/Al_2O_3 stack is designed to act as gate electrode on a boron-doped epitaxial diamond layer. The latter were grown in a microwave plasma assisted chemical vapor deposition (MPCVD) reactor on Ib high pressure high temperature (HPHT) (100) diamond substrate.

#3. Oxygen-terminated diamond MOS – 10nm oxide

Structure #3 consists in a B-doped diamond layer with a boron concentration of around $10^{17}cm^{-3}$. The deposition was performed at 910°C with CH_4/H_2=2% and B/C=2 ppm. Then, an ohmic contact (Ti/Pt/Au annealed at 750°C under high vacuum) was evaporated directly on the epitaxial layer to act as reference contact for capacitance measurement. After the creation of the ohmic contacts, diamond surface oxygenation was performed by deep UV ozone treatment [62].

[9] Oxygen-terminated diamond MOS structures were designed and fabricated by G. Chicot, P. Muret, A. Maréchal, E. Gheeraert and J. Pernot, members of the CNRS, Institute Néel, F-38042 Grenoble, France.

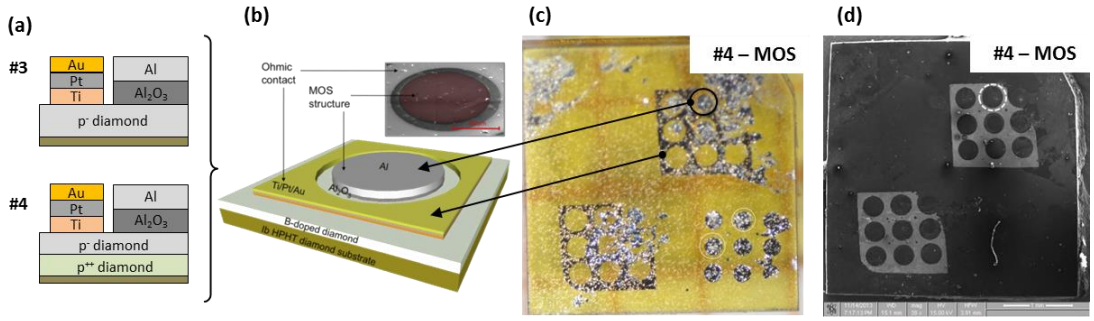

Figure 11: (a) Schematic of the final MOS structures in samples #3 and #4. (b) Schematic view of MOS-Ohmic structure. (c) Optical image of #4 in which MOS and ohmic contacts are highlighted and related with the previously presented schematic. (d) SE image of #4, white-dashed circle is used to highlight one of the studied MOS structure.

Finally, photolithography process was used in order to selectively deposit the dielectric oxide. Then, a 10 nm Al_2O_3 dielectric oxide was deposited by low temperature (100^{o}C) ALD, to preserve the lithography resist. The ALD system used in the present experiments was Savannah 100 from Cambridge NanoTech. The precursor used was trimethylaluminum (TMA), and the oxidant was H_2O. Using the same window in resist, the dielectric has been covered by a 100 nm thick aluminum metal. The final structure is presented in **Figure 11** (a).

#4. Oxygen-terminated diamond MOS – 20nm oxide

Following the same procedure than in sample #3, an oxygen-terminated diamond MOS structure with a 20nm oxide thickness was grown. In this case, a heavily doped layer was grown between the substrate and p-layer with the same technique but with CH_4/H_2=4%, B/C=1200ppm at 830^{o}C. Ohmic contacts were deposited in the same sequence and geometry of #3. The resulting structure is presented in **Figure 11** (b).

Diamond δ-doped MOSFET

To study diamond δ-FETs, we start by characterizing two multilayer structures (samples #5 and #6), containing thin boron doped diamond layers with thickness between 20-60nm. These samples will be used to show the methodology here used to measure thickness and doping of the delta structure.

#5. Stack of thick diamond doped layers

Samples #5 and #6 were growth by MPCVD (Microwave Plasma Chemical Vapor Deposition) in a vertical silica tube reactor as described elsewhere [63] on a (100)-oriented HPHT (high pressure high temperature) type Ib diamond substrate. After a 2 h cleaning with

pure hydrogen plasma at 880ºC, undoped (p^-) and heavily boron-doped (p^{++}) epilayers have been grown alternatively from respectively $H_2/He/CH_4/O_2$ and $H_2/He/CH_4/B_2H_6$ gas mixtures without turning off the plasma.

For the purpose of the related study, the p^{++} epilayers of sample #5 have been labelled from L1 to L4 according to the growth sequence. After the growth of each heavily p^{++} layer, a specific etch-back procedure was performed during 3 min (L2), 6min (L3), and 10 min (L4) using a mixture of hydrogen and oxygen in the plasma. So, #5 consists in a multilayer stack including four thick (nominally 20–60 nm thick) and highly boron doped homoepitaxial diamond layers

#6. Single, thin diamond δ-doped layer

After the characterization of #5, sample #6 was grown. Sample #6 is including only one boron d-doped layer, to evidence the ultimate doping level and thickness that can be reached in the related study.

#7. Multilayer structure of "thick" diamond δ-doped layer

To study boron doping characterization by using TEM, a 001-multi-layer structure have been studied. Diamond films were grown on Ib-type HPHT substrates from Sumitomo Electric on 001-oriented substrate orientation.

A chemical cleaning process was carried out to remove the superficial contamination including non-diamond carbon phases, before growth. Prolonged 0.3–2 h H_2 plasma has been applied to eliminate residual contamination and to etch away the damaged surface layer resulting from the substrate polishing.

Diamond growths were performed in a NIRIM-type Microwave Plasma Chemical Vapor Deposition (MPCVD) reactor, under 50 Torr. Growth parameters were adjusted to achieve high boron doping levels, (0.5% CH_4/H_2, 6000ppm B/C_{gas}).

#8. Single-layer "thin" diamond δ-doped structure

After the characterization of #7, sample #8 was growth. Sample #8 is including only one boron d-doped layer, to evidence the ultimate doping level and thickness that can be reached in the related study (growth parameters are the same used on #7).

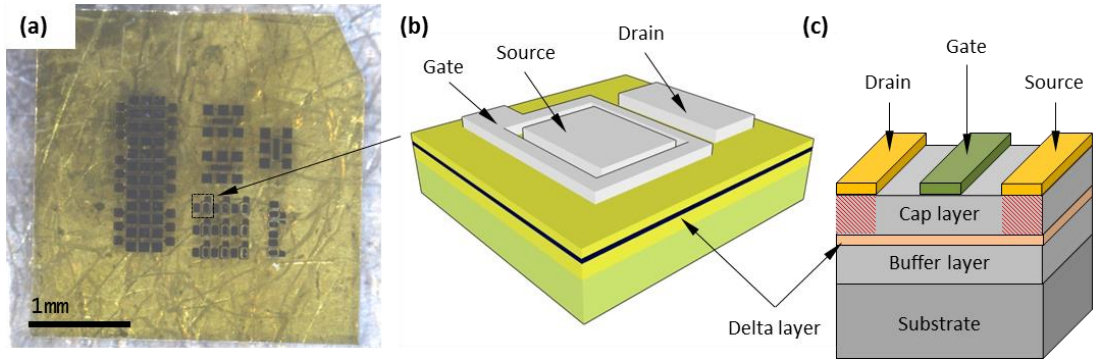

Figure 12: (a) Picture of different FET architectures over a diamond-delta structure and (b) schematic of the structure which shows best electric behavior. (c) Schematic of a diamond delta-FET in its simplest form, red squared region is used to highlight the electric bound between the source-drain contacts and the δ-layer.

#9. Diamond δ-FET[10]

A delta-FET in its simplest for is represented on **Figure 12** (c). In this architecture, the role of the channel is played by the delta layer. This delta layer is grown on a thick NiD layer called buffer layer and covered by a thinner NiD layer called cap layer. The drain and source are ohmic contacts which connect the delta layer channel through the cap layer. For matter of convenience, these contacts are directly deposited on the cap layer before being annealed to reduce the contact resistance by mean of a titanium-carbide formation at the interface. Therefore the drain and source are connected to the delta layer through the cap layer, but, thanks to the low thickness of the cap layer and macroscopic contact size, the induced access resistance is negligible with respect to the resistance of the channel.

Delta structure was growth by using the following recipe:

1. Creation of a non-intentionally-doped (NiD) buffer layer
2. Controlled growing of the delta layer
3. Etching process (to avoid back-edge effects)
4. Growing of a NiD cap layer

Table 3 summarizes the etching and growth steps as well as the different mixtures used for growing the delta. MOS-gate contacts as well as ohmic contacts were fabricated by following the procedure already shown in #3. In this sample, different geometries for δ-FETs were fabricated (as can be appreciated in **Figure 12** (a)) in order to check for an optimum electric response that minimizes edge-related effects and leakages.

[10] Oxygen-terminated diamond δ-FET structures were designed, fabricated and characterized by J. Piñero and A. Maréchal in the facilities of the CNRS, Institute Néel, F-38042 Grenoble, France.

Table 3: Etching and growth rate for different mixtures used for growing (and etching) delta-structures in the surface contact mode (evaluated by ellipsometry)

Step	Press (Torr)	H_2 (sccm)	CH_4/H_2	O_2/H_2	B/C(ppm)	Power (W)	T (ºC)	Duration (min)
1	50	200	0,75	0,32		311	903	50
2	50	2000	0,5		6000	228	830	1
3	50	200		0,25		311	906	5
4	50	200	0,74	0,32		311	915	3

II.2 Experimental techniques

To study chemical and structural properties at nanoscale, Transmission Electron Microscopy (TEM)-related techniques are needed. TEMs are capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons. This enables the instrument's user to examine fine detail (even as small as a single column of atoms, which is thousands of times smaller than the smallest resolvable object in a light microscope).

TEM forms a major analysis method in a range of scientific fields, in both physical and biological sciences and, of course, semiconductor research. Alternate modes of use allow for the TEM to observe modulations in chemical identity, crystal orientation, electronic structure and sample induced electron phase shift as well as the regular absorption based imaging. Further information about electron microcopy-based techniques (scanning and transmission) can be found in Annex I.

In this PhD dissertation, we focus on the study of diamond-related interfaces, whose nanostructure and atomic distribution is expected to explain the

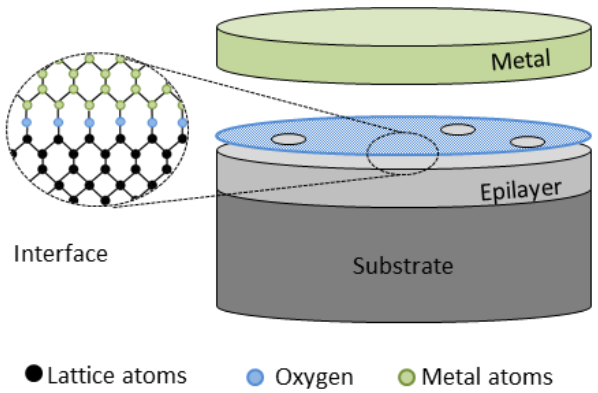

Figure 13: Schematic picture describing the architecture of a diamond Schottky barrier diode, showing a diamond - metal contact and detail of the oxygen-terminated interface, showing oxygen distribution after metal sputtering.

details of the related device behavior. Such interfaces exist between the oxygen-terminated diamond surface and the oxide or metal contact, as spotted in **Figure 13.** In **Figure 13**, a schematic view of a metallic stack over an oxygen-terminated diamond surface (Schottky contact) is presented. On the other hand, detail of **Figure 13** shows diagram of the atomic distribution in the studied interface.

In this sense, to have access to the previously exposed interfaces in all the samples presented in II.1 Description of the samples, specific tools have to be used. Among them, the most important are:

- The Focused Ion Beam, that will be used to prepare electron-transparent diamond specimens
- The Electron Energy Loss Spectroscopy mode of a TEM, that will provide chemical information as well as a mapping of the chemical distribution in a cross-section interface
- The High Angle Annular Dark Field, which will be used to determine the thickness of the δ-layers in diamond-based δ-FET devices.

Focused Ion Beam (FIB)

To analyze diamond using electron microscopy techniques it's necessary, in most of the cases, get electron-transparent samples. It means that we need really thin diamond samples (around 70nm thickness). To get electron-transparent samples as well as to realize a cross section analysis, diamond has to be machined… but this is not so easy. Diamond extreme hardness makes impossible a traditional polish to get electron-transparent specimens! This is the main cause to use Focused Ion Bean techniques when working with diamond.

The Focused Ion Beam (FIB) is a special type of SEM with an additional column. This second column is tilted a specific angle and has a different source to work with Ions (Ga^+ in most of the cases). Gallium irradiation allows nano-milling samples. When high energetic Ga^+ ions impact in the surface of a sample some atoms of the bulk materials are sputtered. This phenomenon combined with an appropriate design of the geometry of the "hole produced" and with different angles of incidence, makes possible the sample preparation. A FIB instrument looks and operates much like a scanning electron microscope (SEM).Both instruments rely on a focused beam to create a specimen image; an ion beam for the FIB and an electron beam for the SEM. For both instruments, the intensity of the secondary electrons produced at each raster position of the beam is displayed to create an image of the sample. In the FIB, secondary ions may also be detected and used to construct an image of the sample. Images having magnifications up to ~ 100 000 times are available using a FIB with a very good depth of field.

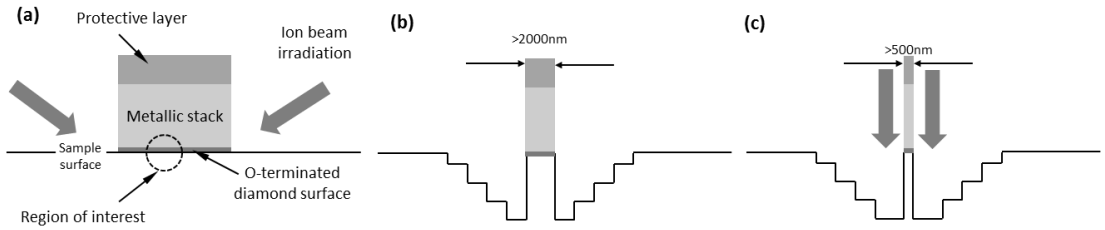

Figure 14: Schematic lateral view of a conventional FIB prepared sample from (a) the initial protective layer deposited, (b) creation of both trenches and (c) reduction of the thickness of the specimen.

In our experimental setup, the operation of a FIB begins with a liquid metal ion source (LMIS). A reservoir of gallium (Ga) is positioned in contact with a sharp Tungsten (W) needle. The Ga wets the needle and flows to the W tip. A high extraction field (>10^8 V/cm) is used to pull the liquid Ga into a sharp cone whose radius may be 5–10 nm. Ions are emitted as a result of field ionization and post-ionization and then accelerated down the FIB column. The use of Ga is advantageous for two reasons:

1. Ga has a low melting point and, therefore, exists in the liquid state near room temperature.

2. Ga can be focused to a very fine probe size (<10 nm in diameter).

FIBs typically operate with an accelerating voltage between 5 and 50 keV. By controlling the strength of the electrostatic lenses and adjusting the effective aperture sizes, the probe current density (and therefore beam diameter) may be altered from tens of pA to several nA corresponding to a beam diameter of ~ 5 nm to ~ 0,5 µm).

Most of the literature listed in the reference section refers to the conventional FIB method of TEM specimen preparation. A detailed description of this method is given in [64-67]. And a schematic of the procedure is spotted in **Figure 14**. **Figure 14** (a) shows a cross section diagram of a Schottky contact (as in **Figure 13**) with a protective layer deposited, region of interest (O-terminated diamond surface/metal interface) is highlighted. **Figure 14** (b) shows the effect of the ion beam irradiation; ion milling is used to reduce the thickness of the specimen till 500nm approximately.

Figure 15 shows SEM images of the whole procedure, from the original sample (#2 was used to illustrate this procedure, see dashed-square in **Figure 15** (a)) to the final specimen. White arrows are used in **Figure 15** (e) to highlight the pre-cut section. As can be noted, a metal line is usually deposited on the area of interest to prevent damage and spurious sputtering of the top portion of the specimen and to also delineate the location of the area of interest. Typical dimensions of the metal line are ~ 1 µm wide, ~ 2 µm high and ~ 30 µm long. Large trenches are sputtered on either side of the area of interest using a high Ga^+ beam current.

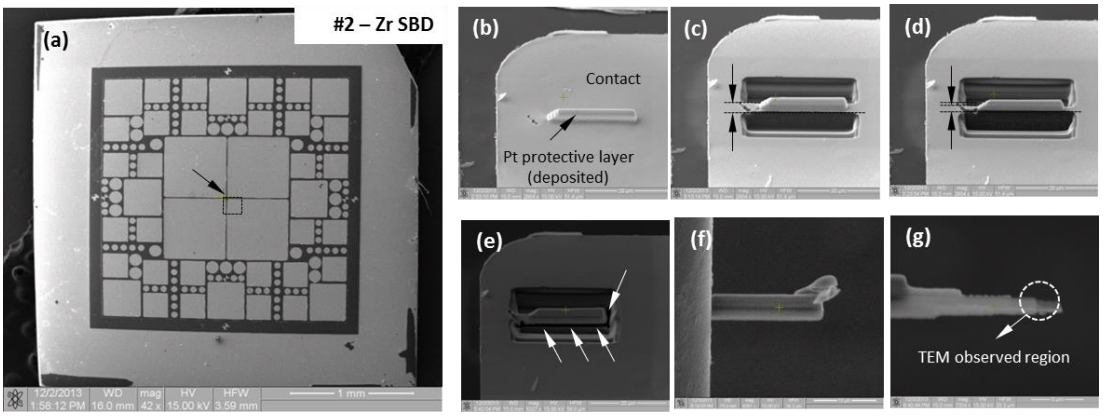

Figure 15: SEM micrography of a conventional FIB procedure. (a) Original sample, (b) deposition of the Pt protective layer, (c) from the initial protective, (c) creation of the trenches, (d) in-sample lamella thickness reduction, (e) pre-cut of the structure, (f) transfer from the bulk to the specimen holder, (g) final thickness reduction.

The beam current is reduced and milling is performed on alternate sides of the specimen to reduce redeposition of sputtered material onto the surface of the specimen. Milling is continued until the membrane is thinned to ~ 100 nm or less (the final thickness of the specimen will depend on the information sought and the density of the material, ~70nm in case of diamond samples). A finished electron transparent portion of the sample is usually ~ 5 µm x ~ 20 µm. An understanding of the sputtering process is important for a knowledgeable operation of the FIB. When a Ga^+ ion is accelerated toward the target sample, it enters the sample and creates a cascade of events which results in the ejection of a sputtered particle (which may be an ion or a neutral atom). This sputtering mechanism thus also results in Ga^+ implantation into the sample. The primary ion penetration depth is ~20 nm for 25 keV Ga^+. The use of enhanced etching may increase the sputtering rate.

Damages produced by FIB operations[11]

Beside its high precision, during FIB operations several undesired phenomena take place: Gallium implantation, surface amorphization and other associated damages can be produced, altering diamond's optical, structural and electrical properties. These phenomena are particularly important in our case, due to the fast tendency of diamond to graphitize and, as can be observed in **Figure 16**, the angle of incidence of ions at the interface is higher than

[11] Influence of the Ga implantation in diamond opto-electronic properties were evaluated by the author in a previous work ("*CL evaluation of the Ga+ implantation on diamond*", HETECH 2013-Glasgow, Scottland).

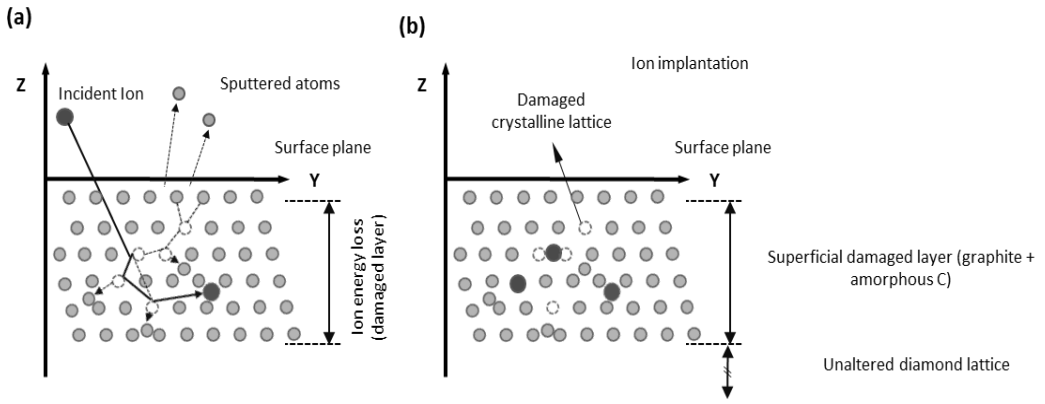

Figure 16: Schematic diagram of a collision cascade generated by an incident ion (a), represented only in 2D. Accelerated Ga^+ atoms can be implanted during the milling process, thus damaging the surface of the semiconductor (b), the latter is revealed as a thick layer with mixture of graphite and amorphous carbon in case of semiconducting diamond.

that of the rest of the lamella due to the difference in hardness between diamond and metal. This induces an increase of amorphous C just at the interface.

To prevent diamond amorphization, low energy, low incident angle ion beam is used during the last steps of the preparation. However, due to the huge difference in the hardness of the diamond bulk substrate and the hardness of the metallic stack, undesired damages (like Ga implantation or C redeposition) are difficult to avoid when studying diamond/contact interfaces. Schematic of a collision cascade, provoking damages in the diamond lattice and Ga implantation is shown on **Figure 17**. Additionally to the previously described diamond-surface amorphization, further artifacts are produced during the FIB manipulation of diamond samples. The most important artifact to be taken into account when studying diamond-metal interfaces is the bottleneck-shaped interface (see **Figure 16**).

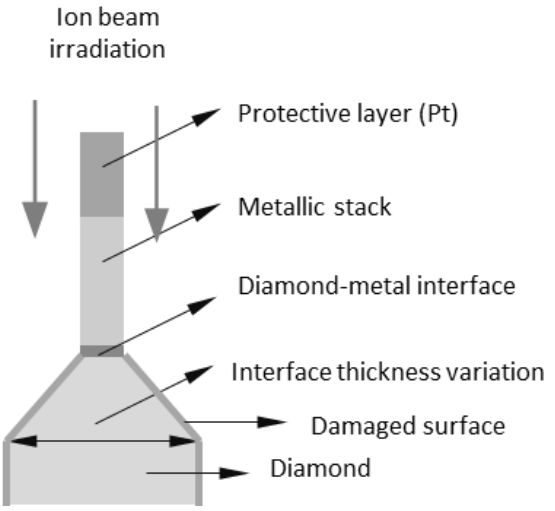

Figure 17: Schematic of a diamond-FIB preparation. Bottleneck-shaped interface is shown as a consequence of the different hardness between the metallic stack and the diamond bulk.

This bottleneck-shaped interface is produced during the last steps of the sample preparation procedure,

and is a consequence of the different hardness between the diamond bulk and the metallic stack.

Both effects (diamond-surface amorphization and bottleneck-shaped interface) have to be taken into account during TEM observations:

- Bottleneck-shaped interface distorts EELS diamond mapping, because the relative content of amorphous C is higher near the interface.
- HREM imaging of diamond/metal interfaces are limited by the FIB nanomachining.

EELS analysis of the interface[12]

In electron energy loss spectroscopy, a material is exposed to a beam of electrons with a known, narrow range of kinetic energies. Some of the electrons will undergo inelastic scattering, which means that they lose energy and have their paths slightly and randomly deflected. The amount of energy loss can be measured via an electron spectrometer and interpreted in terms of what caused the energy loss. Inelastic interactions include phonon excitations, inter and intra band transitions, plasmon excitations, inner shell ionizations, and Cherenkov radiation. The inner-shell ionizations are particularly useful for detecting the elemental components of a material.

Table 3: Main EELS transitions shown in this study, as presented in **Figure 18**

Peak	Energy (eV)	Peak	Energy (eV)	Peak	Energy (eV)
D1	20.7	G1	6.2	C1	4.9
D2	30.9	G2	32.1		
D3	60.9	π*	256.6		
D4	266.9	σ*	263.9		
D5	272.1	G3	267.9		
D6	280.1	G4	274.8		
D7	301.7	G5	278.6		
		G6	299.8		

[12] EELS data of **Figure 18** and **Table 3** were obtained at EELS database (https://eelsdb.eu/)

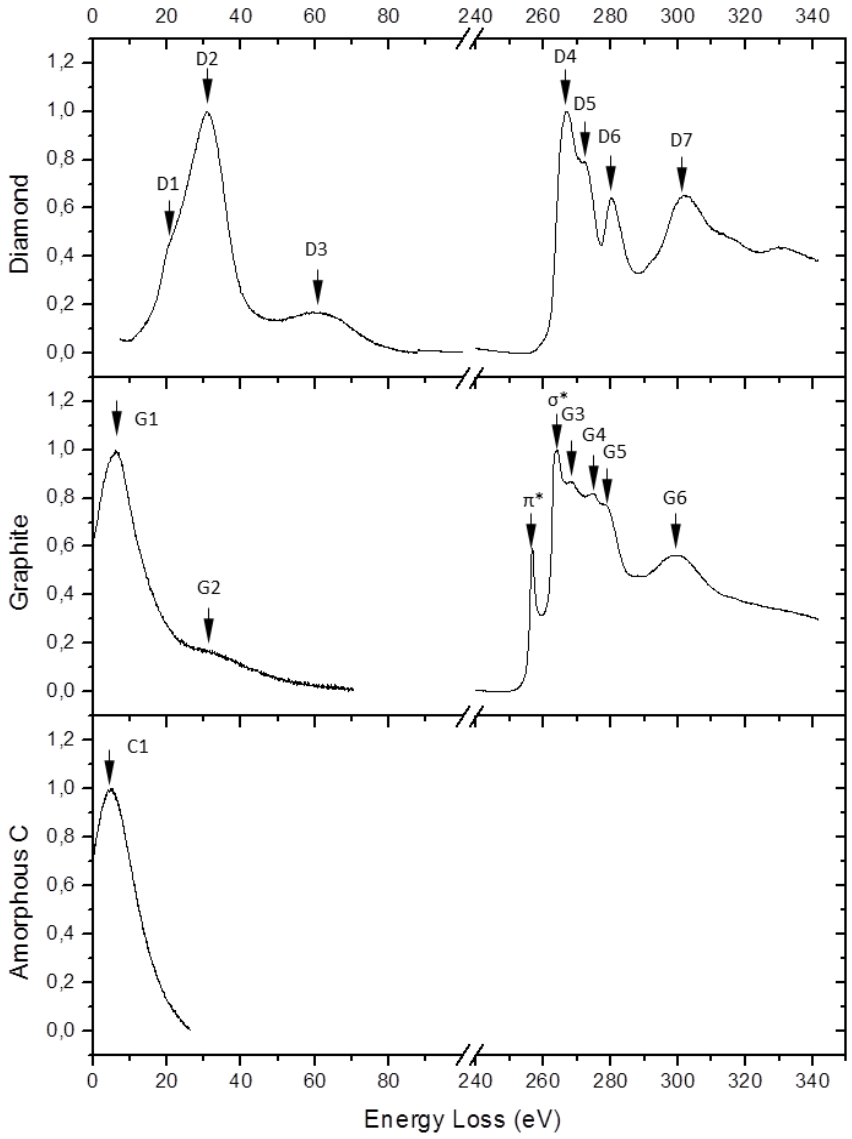

Figure 18: Typical EELS shape of pure diamond, pure graphite and amorphous carbon. Main transitions are labeled and detailed in **Table 3**

For example, one might find that a larger-than-expected number of electrons comes through the material with 285 eV less energy than they had when they entered the material. This is approximately the amount of energy needed to remove an inner-shell electron from a carbon atom, which can be taken as evidence that there is a significant amount of carbon present in the sample. With some care, and looking at a wide range of energy losses, one can determine the types of atoms, and the numbers of atoms of each type, being struck by the beam. The scattering angle (that is, the amount that the electron's path is deflected) can also

be measured, giving information about the dispersion relation of whatever material excitation caused the inelastic scattering.

Finally, typical EELS signature of diamond, graphite and amorphous carbon is shown in **Figure 18**. Main transitions are labeled and summarized in a **Table 4**. In this section, we have focused in the typical diamond, carbon and graphite EELS spectra. However, additional information and generalities about EELS technique is presented in Annex I.

Chapter III: Diamond-based Schottky barrier diodes

Oxygen-terminated diamond-based Schottky diodes for power device applications are analyzed in this chapter. Our purpose is to relate its nanostructure to the behavior of the oxygen-terminated diamond and, in particular, its relationship with the thermal treatment.

III.1 **Introduction**: A brief tour in previous attempts on designing diamond-based SBDs is presented. Oxygen-termination in diamond is introduced and discussed. Role of the contacting metal is also presented by following the next index:

- **The oxygen termination**
- **Conventional vs Schottky diodes for power device applications**
- **Choosing a metal**

III.2 **WC-based diodes [#1]:** WC-based oxygen-terminated diamond SBDs are expected to present an optimum behavior at high temperatures. For this, in this section, WC-based SBDs will be nano-characterized with a novel EELS methodology according to the following index:

- **Current-voltage plot of SBDs**
- **Electrical properties**
- **Structural analysis of the thermal treatment**
- **Interface analysis**

***III.3* Zr-based diodes [#2]:** Zr is an easily oxidizable metal, so, oxygen-terminated Zr-diamond contacts are expected to fix oxygen and then should show good electrical behavior at high temperatures. We will use the EELS methodology (defined in III.2) to evaluate the nanostructure of these interfaces.

- **Electrical properties**
- **TEM-EELS characterization of the metal-semiconductor interface**
- **Variations with thermal treatment**

***III.4* Analysis of WC vs Zr-based Schottky diodes: physical behavior of the interface:** Different behavior of WC-based and Zr-based oxygen-terminated diamond SBDs have been evidenced. In this section, we will discuss and compare the results obtained in both structures by following the next index:

- **Real metal-semiconductor contacts: Interface states**
- **Effect of the thermal treatment on the O-terminated diamond surface**

***III.5* Conclusions:** Main conclusions derived from this chapter are here summarized.

III.1 Introduction

The most common function of a diode is to allow an electric current to pass in one direction (called diode's forward direction), while blocking the current in the opposite direction (reverse direction). The diode unidirectional behavior is called "rectification", and is used to convert alternating current to direct current, including extraction of modulation from radio signals in radio receivers.

However, diodes can have a more complicated behavior than this simple on-off action due to their nonlinear current-voltage characteristics. Semiconducting diodes begin conducting electricity only if a certain threshold voltage or cut-in voltage is present in the forward direction (a state in which the diode is said to be forward-biased). The voltage drop across a forward-biased diode varies only a little with the current, and is a function of temperature. The current-voltage characteristic of a diode can be tailored by the choice of the semiconductor material and doping. Thus, diamond-based diodes are expected to act as excellent rectifiers (due to both, its high breakdown voltage and its high electron/hole mobility).

The different architectures for designing diodes depend on its applications. Among them, the following structures can be mentioned: to regulate voltage (Zener diodes), to protect circuits from high voltage surges (avalanche diodes), to electronically tune radio and TV receivers (varactor diodes), to generate radio-frequency oscillations (tunnel diodes, Gunn diodes, IMPATT diodes), or to produce light (light-emitting diodes).

Diamond Schottky barrier diodes (SBDs) have been intensively studied during the past half-decade, in order to fabricate high-performance rectifiers fulfilling both high-voltage resistance in reverse operation and low on-resistance in forward operation, which are difficult to achieve using common semiconductor materials. In addition, because of the larger band-gap of 5.5 eV and strong mechanical hardness of semiconducting diamond, diamond-based SBDs are expected to be operated under higher temperatures above 200 °C. Most studies consider homoepitaxially grown boron-doped p-diamond (100) films [58].

Several interesting results have been reported up to date for diamond SBDs. Simultaneously, problems that should be solved before practical applications are been clarified gradually. In other words, experimentally obtained device performance has not reached the theoretically expected performance in terms of the physical parameters of semiconducting diamond.

Among the aspects that should be improved, it can be mentioned the larger reverse current and lower breakdown voltage of diamond SBDs present severe obstacles for device applications. In most cases, the reverse current of p-diamond SBDs increased rapidly with the bias voltage increase. Increasing features of reverse current cannot be explained using the standard current transport model, which is represented by Schottky barrier lowering [68] (see A.I Metal – Semiconductor interfaces for more details), even though the acceptor concentration is rather low. Thermionic field emissions and field concentrations at the electrode fringe are possible causes of the enhanced reverse current level [69]. The electric breakdown field of diamond SBDs was experimentally less than 4 MV/cm [70], which is less than one-third of the expected value [71].

Finally, the most important parameters that will govern the behavior of diamond-based SBDs are the diamond termination (as described in I.6 Motivation: impact of the interface configuration in diamond devices) and the choice of the metal contacting the diamond surface. Both parameters will be studied in this chapter.

The oxygen termination

Other key problems to be solved in diamond-based SBDs are dispersion and thermal stability of the diamond Schottky interface. This problem might derive from inhomogeneous

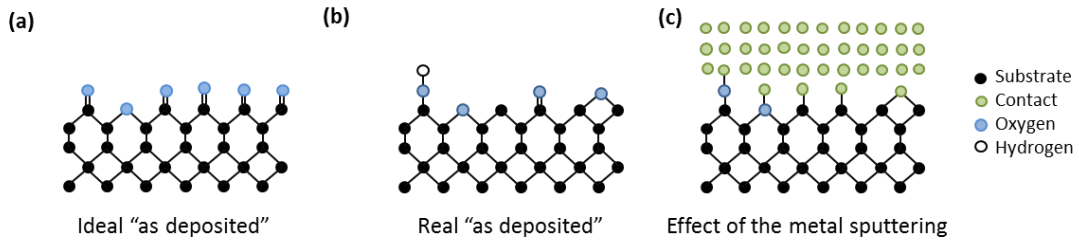

Figure 19: Oxygen-terminated diamond surface after VUV ozone treatment in (a) an ideal situation, (b) a real situation (where some places of the diamond surface are not oxygen-terminated) and (c) oxygen-terminated surface, mixed by metal sputtering.

and unstable oxygen termination of diamond surface. In most common semiconductors, oxygen species at the Schottky interface can be removed to inhibit the degradation of interface properties. However, the oxygen-terminated diamond surface is frequently used [72] for diamond-based SBD fabrication to suppress external leakage current passing through the hydrogen-terminated diamond surface. In addition, the Schottky barrier height of diamond is altered drastically by the condition of surface termination [73]. This fact suggests that the performance of diamond SBD is increased by improving the surface oxidation condition.

The wet-chemically oxidized diamond surface has termination groups of ether (C-O-C), carbonyls (C=O), and hydroxyls (OH) [74]. In the conventional diamond SBD fabrication process, the oxidized diamond samples must be post-annealed (T>800K) after ohmic electrode deposition for the formation of the ohmic contact through an interfacial reaction. Oxygen termination is not stable at such high temperatures. Therefore, non-terminated areas are probably formed on the diamond surface where Schottky electrodes are deposited in the following process step. This behavior is presented in **Figure 19**, where an ideal oxygen-terminated diamond surface is presented (**Figure 19** (a)) together with the probably real oxygen distribution (**Figure 19** (b)). Finally, **Figure 19** (c) shows the effect of the metal sputtering in the oxygen termination. **Figure 19** (b) also shows all the expected configurations for the oxygen termination: C-O-H, C=O, C-O-C and dangling bonds (carbon atoms without oxygen termination).

To obtain better Schottky properties, an alternative diamond surface oxidation process that can be applied with a gas phase reaction after ohmic contact formation is indispensable to fulfill the non-terminated area by oxygen groups without deterioration of the fabricated ohmic contacts. The diamond surface is known to be oxidized by ozone under vacuum ultraviolet (VUV) light irradiation. The surface termination was dominated by hydroxyl groups [75], producing a homogeneously terminated surface. This process is conducted

without intentionally heating of the diamond sample. Therefore, diamond surface oxidation using ozone under VUV irradiation is a promising method for SBD fabrication.

In this work, several diamond surfaces were oxidized through VUV irradiation. The resulting oxygen-terminated diamond SBDs, treated with different annealing processes, will be analyzed and characterized in this chapter.

Conventional vs Schottky diodes for power device applications

In electronics, a diode is a two-terminal electronic component with asymmetric conductance; it has low (ideally zero) resistance to current in one direction, and high (ideally infinite) resistance in the other. A semiconductor diode, the most common type up to date, is a crystalline piece of semiconductor material with a p–n junction connected to two electrical terminals. Nowadays, most diodes are based on silicon, but other semiconductors such as selenium or germanium are sometimes used too.

A schematic band diagram of p-n classic junction is shown in **Figure 20** (a). The subsequent charge carrier diffusion process implies the creation of an electric field and, thus, a potential contact. This structure allows an electric current to pass in one direction (called diode's forward direction), while blocking current in the opposite direction (the reverse direction). This unidirectional behavior is called rectification. Main characteristics of pn-type and Schottky barrier diodes are summarized in **Table 4.**

On the other hand, the Schottky diode is based in a metal/semiconductor interface with a low forward voltage drop and a very fast switching action. When forward current flows

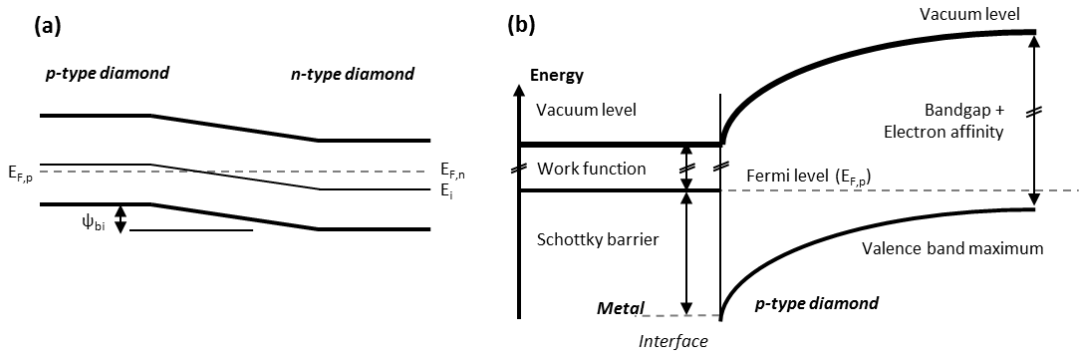

Figure 18: (a) Energy band diagram of a classic p-n diamond junction, Fermi levels are aligned and conduction/valence bands are bended in the interface. (b) Energy band diagram of a metal/p-type semiconducting diamond contact, Schottky barrier is created in the vicinity of the metal/semiconductor interface.

Table 4: Comparison of characteristics of Schottky diode and pn diode, data were obtained from radio-electronics.com

Characteristic	Schottky diode	PN junction diode
Forward current mechanism	Majority transport	Due to diffusion currents, i.e. minority carrier transport
Reverse current	Results from majority carriers that overcome the barrier. This is less temperature dependent than for standard PN junction.	Results from the minority carriers diffusing through the depletion layer. It has strong temperature dependence.
Turn on voltage	Small (around 0.2 V in Si)	Comparatively large (around 0.7V in Si)
Switching speed	Fast - as a result of the use of majority carriers because no recombination is required.	Limited by the recombination time of the injected minority carriers.

through a diode, there is a small voltage drop across the diode terminals. A normal silicon diode has a voltage drop between 0.6–0.7 volts, while a Schottky diode voltage drop is between approximately 0.15–0.45 volts[13]. This lower voltage drop can provide higher switching speed and better system efficiency, which makes them useful in voltage clamping applications and prevention of transistor saturation.

They can also be used as low loss rectifiers[14], although their reverse leakage current is, in general, higher than that of other diodes. Schottky diodes are majority carrier devices and, so, do not suffer from minority carrier storage problems that slow down many other diodes, so they have a faster reverse recovery than p–n junction diodes. They also tend to have much lower junction capacitance than p–n diodes, which provides for high switching speeds and their use in high-speed circuitry and RF devices such as switched-mode power supply, mixers, and detectors [76].

To create a Schottky barrier, a metal–semiconductor junction is formed between a metal and a semiconductor (instead of a semiconductor–semiconductor junction as in conventional diodes). Typical metals are molybdenum, platinum, chromium or tungsten, and certain silicides; the semiconductor typically is n-type silicon. The metal side acts as the anode and n-type semiconductor acts as the cathode of the diode. This Schottky barrier results in both very fast switching and low forward voltage drop.

[13] http://www.datasheetcatalog.com/datasheets_pdf/1/N/5/8/1N5817.shtml

[14] A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction.

The choice of the combination of the metal and semiconductor determines the forward voltage of the diode. Both n- and p-type semiconductors can develop Schottky barriers; the p-type typically has a much lower forward voltage. As the reverse leakage current increases dramatically with lowering the forward voltage, it cannot be too low; the usually employed range is about 0.5–0.7 V and p-type semiconductors are employed only rarely.

With increased doping level of the semiconductor the width of the depletion region drops. Below certain width the charge carriers can tunnel through the depletion region. At very high doping levels the junction does not behave as a rectifier anymore and becomes an ohmic contact.

This can be used for simultaneous formation of ohmic contacts and diodes, as diodes form between the silicide and lightly doped n-type region and ohmic contacts form between the silicide and a heavily doped n- or p-type region. Lightly doped p regions turns into a problem as the resulting contact has too high resistance for a good ohmic contact and too low forward voltage and too high reverse leakage to be a good diode.

As the edges of the Schottky contact are fairly sharp, high electric field gradient occurs around them, limiting the reverse breakdown voltage. Several strategies are used, from guard rings to overlaps of metallization to spread out the field gradient. The guard rings consume valuable die area and are used primarily for large higher-voltage diodes, while overlapping metallization is employed primarily with smaller, low-voltage diodes.

For power Schottky diodes, the parasitic resistances of the buried N+ layer and the epitaxial n-type layer become important. The resistance of the epitaxial layer is more important here than for a transistor as the current has to cross its entire thickness. In comparison with the power p–n diodes, the Schottky diodes are less rugged.

The junction lies in direct contact to the thermally sensitive metallization, a Schottky diode can therefore dissipate less power than an equivalent-size p–n one with deep-buried junction, before failing especially during reverse breakdown. The relative advantage of lower forward voltage of Schottky diodes is diminished at higher forward currents, where the voltage drop is dominated by the series resistance. Unbiased Schottky contact band diagram is shown in **Figure 20** (b).

Compared to other diamond power devices (as bipolar transistor [77], junction field effect transistor [78], Schottky-pn diode [79], etc…) Schottky diode is the most promising because of the highest breakdown voltage reported (2.5kV [80], 6.7kV [81], 10kV [58], 8-12kV [82]) and architectural progress to minimize its serial resistance. Indeed, the high serial resistance of the lightly doped Schottky active layer required to get high breakdown field, is one of the main limitations of such device.

Choosing a metal

As briefly spotted in **Figure 20**, the choice of the metal (and thus, the metal work function and its respective electronegativity) contacting the oxygen-terminated diamond surface will determine key aspects of the related device features. Indeed, Schottky barrier height of metal contacts depends on the diamond termination and the annealing process [45].

According to the nature of the Schottky metal, barrier inhomogeneity may be observed due to partial oxygen desorption [83], meaning that Schottky metal selection and surface pretreatment are crucial to get low enough barrier heights, low defect density at interface, and a thermally stable interface. Two Schottky electrode metals were examined in this study:

- Tungsten carbide (WC) is a carbide preformed metal. Direct bonding between WC and the diamond surface is expected to be formed [59] with breakage of the oxygen termination during deposition. Carbide preformed metal is a good candidate for a high-temperature Schottky contact compared to the carbide forming metal such as tungsten because excess extraction of carbon atoms from diamond accompanied by vacancy formation is expected to be suppressed.
- Zirconium (zr) is an easily oxidizable metal that can be combined with an oxygen-passivated heavily boron doped diamond surface. This procedure could lead to the formation of a very stable and uniform ultra-thin oxide film at the interface, which acts as a chemical and electrical passivation layer.

We labelled WC-based SBD as sample #1, and Zr-based SBD as #2. Information about growing conditions, oxygen termination procedure and metal deposition process of both samples was previously described in II.1 Description of the samples. Such specimens were annealed at different temperatures in order to evaluate the relation of the thermal treatment with the electrical behavior of both SBDs. Here, **Table 5** summarizes the full set of studied samples.

Table 5: Summary of the samples studied in this work with its corresponding annealing temperature

	Contact metal	Annealing temperature (K)
#1A	WC	300
#1B	WC	600
#1C	WC	700
#2A	Zr	300
#2B	Zr	623
#2C	Zr	723

III.2 WC-based diodes [#1]

As first approach to select the Schottky metals, let's remember that the contact has to ensure good adhesion, a thermally and chemically stable interface, and a potential barrier leading to optimum forward losses (a low forward voltage drop) and minimal reverse current even at high temperatures.

Conversely to an ohmic contact where a high density of gap states (or interface states) is promoted by forming a carbide interface layer (titanium carbide is expected to be formed in Ti-diamond ohmic contacts), the main issue towards high performance diodes, fully exploiting the diamond's electrical and thermal properties, is to prevent the carbide formation while minimizing the interface states. Diamond surface oxygenation is known to be an efficient way to minimize electronic states on diamond surface [51], and is known to change the band alignment in the diamond surface. This kind of surface termination was adopted by several research groups as being the first step of the Schottky contacts deposition process.

As Schottky diodes are supposed to be used as rectifiers, they have to be thermally stable. However, thermal dissociation of the oxygen bonds was observed for inter metal such as gold [59] (above 500 K) as well as for easily oxidizable metals (like aluminum) due to the thermal instability of the oxide material. An alternative solution is to use diamond surface oxygenation [59, 84] based in carbide-formed metals, such as tungsten carbide (WC), to improve to contact adhesion. These kinds of interfaces are expected to have a better stability up to 600K, due to the formation of an interfacial bonding between WC and diamond.

Summarizing, WC/diamond contacts performed over diamond oxygen-terminated surfaces are expected to combine both properties:

- Oxygen-terminated diamond interfaces in the metal/semiconductor junction will minimize the electronic states on diamond surface, thus suppressing external leakage currents passing through the hydrogen-terminated diamond surface (diamond surface conduction is known to be caused by hydrogen termination [44]).
- Tungsten carbide metal/semiconductor contact will create WC-diamond bonds in the interface. Carbide preformed metal is a good candidate for a high-temperature Schottky contact compared to the carbide forming metal such as tungsten because excess extraction of carbon atoms from diamond accompanied by vacancy formation is expected to be suppressed.

In our study, after the growing process and the metal deposition (carried out as described in Diamond-based Schottky Barrier Diodes), the resulting SBDs were electrically, chemically and nano-structurally characterized in each subsequent annealing step.

Electric properties of the SBDs (measured at NIMS, Japan) were taken using a micro-probing system with a Pico-ammeter/voltage source unit (6487; Keithley). Measurements were performed under vacuum.

Homemade software for electrical measurements was developed for detailed analyses, carried out at NIMS (Japan). TEM samples were prepared using FIB nanomachining to get electron-transparent specimens by using a Quanta 200 3D FIB dual-beam system. Finally, EELS mapping of the area of interest was carried out by using the beam of a JEOL 2010F transmission electron microscope in STEM mode.

Current-voltage plot of SBDs

Schottky barrier diodes are characterized attending to their current-voltage plots. The key parameters that can be obtained from such plots are:

- The Schottky-barrier heights (Φ_B): Whether a given metal-semiconductor junction is an ohmic contact, or Schottky barrier, depends on the Schottky barrier height, Φ_B, of the junction. For a sufficiently large Schottky barrier height, where Φ_B is significantly higher than the thermal energy kT, the semiconductor is depleted near the metal and behaves as a Schottky barrier. For lower Schottky barrier heights, the semiconductor is not depleted and instead forms an ohmic contact to the metal. The Schottky barrier height is defined differently for n-type and p-type semiconductors (being measured from the conduction band edge and valence band edge, respectively). The alignment of the semiconductor's bands near the junction is typically independent of the semiconductor's doping level, so the n-type and p-type Schottky barrier heights are ideally related to each other. In practice, the Schottky barrier height is not precisely constant across the interface, and varies over the interfacial surface.
- Ideality factor (n): This parameter is used to "weight" how close the real SBD structure to an ideal one is.

Experimentally, Schottky-barrier heights (Φ_B) and ideality factors can be estimated from the fitting of the semi- logarithmic linear region (log-linear region) of forward current density (J) versus voltage (V) characteristics, by mean of the thermionic emission model issued from the SBD theory [85].

According to the latter, the current density behavior follows:

$$J = A^*.T^2.exp\left(\frac{-q.\phi_B}{k_B.T}\right) \times \left[exp\left(\frac{q.V}{n.k.T}\right) - 1\right] \quad \textbf{Eq. 3}$$

Where Φ_B, n, T, q, k_B, and A* are the Schottky barrier height, ideality factor, absolute temperature, elementary charge, Boltzmann constant, and Richardson constant, respectively. In this work, A* is taken as $90 Acm^{-2}K^{-2}$, as widely employed in the literature [86, 87].

According with **Eq. 3**, the shape of the DC current flowing through a Schottky barrier is plotted in **Figure 21**. From a DC current-voltage plot (I-V plot) we can determine:

- the ideality factor n from the slope in forward bias
- the correct model for conduction
    - in thermionic-emission theory, the reverse current saturates (levels off)
    - in diffusion theory, the reverse current depends on the bias
- the saturation current J_0 from the reverse-bias saturation current or the extrapolated-to-zero-volt forward-bias current
- the barrier height Φ_B when the temperature is varied (from a plot of $\ln(J/T^2)$ vs 1/T, which results in a straight line with a slope from which the barrier height can be derived)
- the rectification ratio of a device, this depends (for a fixed voltage) on the J_0, also known as "leakage current"
- For high forward voltages, the current may be limited by the resistivity of the bulk.

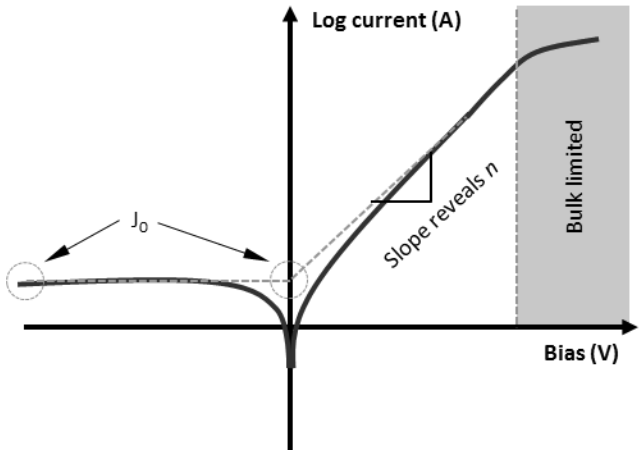

Figure 19: Thermionic-emission theory for the DC current through a Schottky barrier. Positive bias feature is known as the "forward characteristic", while negative bias is known as "reverse characteristic". Ideality factor *n* can be obtained from the slope of the linear section of the forward characteristic, while reverse-bias saturation current J_0 can be extrapolated from the negative bias region of this plot.

In that case, the current doesn't continue rising exponentially with the bias, but only grows linearly. In the semi-log IV curves this is visible as a bending of the curve at strong forward bias. Since the current is limited by the bulk conductivity we can again apply the theory for bulk samples.

Additionally, in view of the particular properties of the Schottky diode there are several parameters that are of key importance when determining the operation of one of these diodes against the more normal PN junction diodes:

- **Forward voltage drop:** In view of the low forward voltage drop across the diode, this is a parameter that is of particular concern. As can be seen from the Schottky diode IV characteristic, the voltage across the diode varies according to the current being carried. Accordingly any specification given provides the forward voltage drop for a given current. Typically the turn-on voltage is assumed to be around 0.2 V.
- **Reverse breakdown:** Schottky diodes do not have a high breakdown voltage. Figures relating to this include the maximum Peak Reverse Voltage, maximum Blocking DC Voltage and other similar parameter names. If these figures are exceeded then there is a possibility the diode will enter reverse breakdown. It should be noted that the RMS value for any voltage will be $1/\sqrt{2}$ times the constant value. The upper limit for reverse breakdown is not high when compared to normal PN junction diodes. Maximum figures, even for rectifier diodes only reach around 100 V. Schottky diode rectifiers seldom exceed this value because devices that would operate above this value even by moderate amounts would exhibit forward voltages equal to or greater than equivalent PN junction rectifiers.
- **Capacitance:** The capacitance parameter is one of great importance for small signal RF applications. Normally the junctions areas of Schottky diodes are small and therefore the capacitance is small. Typical values of a few picofarads are normal. As the capacitance is dependent upon any depletion areas, etc, the capacitance must be specified at a given voltage.
- **Reverse recovery time:** This parameter is important when a diode is used in a switching application. It is the time taken to switch the diode from its forward conducting or 'ON' state to the reverse 'OFF' state. The charge that flows within this time is referred to as the 'reverse recovery charge'. The time for this parameter for a Schottky diode is normally measured in nanoseconds, ns. Some exhibit times of 100 ps. In fact what little recovery time is required mainly arises from the capacitance rather than the majority carrier recombination. As a result there is very little reverse current overshoot when switching from the forward conducting state to the reverse blocking state.

- **Working temperature:** The maximum working temperature of the junction, T_j is normally limited to between 125 to 175°C. This is less than that which can be sued with ordinary silicon diodes. Care should be taken to ensure heatsinking of power diodes does not allow this figure to be exceeded.
- **Reverse leakage current:** The reverse leakage parameter can be an issue with Schottky diodes. It is found that increasing temperature significantly increases the reverse leakage current parameter. Typically for every 25°C increase in the diode junction temperature there is an increase in reverse current of an order of magnitude for the same level of reverse bias.

Further details of the real Schottky contacts, as well as a detailed description of the experimental procedure employed on the electrical characterization of the Schottky structures studied on this thesis can be consulted in literature [88].

Electrical properties[15]

Figure 22 (a) shows the electrical response, taken at various temperatures, for thermally treated WC-based SBD structures. This structure exhibit an improvement of his related electric behavior with the thermal treatment, as revealed by the change of the related slope and the shape of the curves. For a 600K thermal treatment temperature (see dark, thick line in **Figure 22** (a)), this structure shows the optimum operation regime.

The goodness of such regime is quantified evaluating Schottky-barrier heights (Φ_B) and ideality factors. Such parameters are estimated from the fitting of the semi- logarithmic linear region (log-linear region) of forward current density (J) versus voltage (V) characteristics, by mean of the thermionic emission model issued from the SBD theory (see **Eq. 3**).

In **Figure 22** (a), it can be observed that WC SBDs are showing different behaviors depending on the thermal treatment:

- I(V) characteristic acquired at 500K and 600K are far from the ideal SBD behaviour.
- Current density taken at 300K just after the contact deposition is close to the ideal SBD I(V) shape.

[15] WC-based Schottky barrier diodes were electrically characterized by A. Fiori, T. Teraji and Y. Koide, National Institute for Materials Science. 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan.

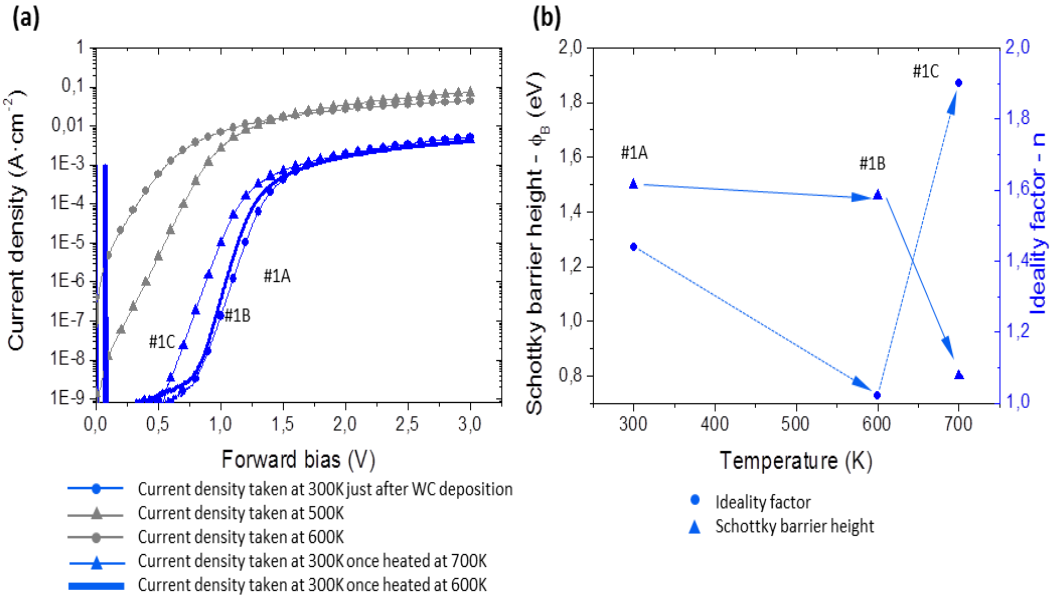

Figure 20: (a) Current density vs bias voltage measured at different temperatures and with different thermal treatments. (b) Evolution of the ideality factor and the SBH with thermal treatment.

- Current density measured at 300K once heated at 600K shows an optimum I(V) behaviour, with an ideality factor close to 1. On the other hand, the Schottky barrier height on this oxygen-terminated surface is not larger than 1.5eV (barriers larger than 2eV can lead to high forward losses).
- Finally, I(V) characteristic (acquired at 300K) of a 700K annealed SBD shows a degradation of the ideality factor.

Thus, SBD electric properties improve with thermal treatment up to an optimum behaviour at 600K annealing. After such point, the structures are presenting certain degradation. So it is established that tungsten carbide (similarly to other carbide-preformed metals) have thermal stability up to 600 K.

An operating temperature higher than 600 K induced a degradation of WC based diamond rectifiers, as can be appreciated by the change in the ideality factor (that goes far from n = 1, rising till n = 1.9). In the same way, Schottky barrier height decreases, this aims to variations in the metal-diamond interface.

Structural analysis of the thermal treatment

To explore the possibility of a relation between the thermal treatment and the interface configuration in WC-based SBD, TEM observations were carried out. TEM study is consisting in a first visual CTEM characterization and EELS probing of the metal/semiconductor interface.

Figure 23(a) shows low magnification 001 BF images of WC-based SBD before (sample #1A) and after (sample #1B) a 600K annealing. Diamond substrate, WC metal layer and Pt protective layer (deposited during FIB preparation II.2 Experimental techniques) are revealed. Grain formation can be appreciated in the 50nm thick WC layer before and after thermal treatment.

Figure 23(a) is used to compare TEM images of WC/diamond interfaces before and after a 600K thermal treatment (corresponding with samples #1A and #1B, respectively, see **Table 6**). Morphological changes in the diamond/metal interface can be appreciated.

To analyze the chemical composition of the diamond/metal contact, EELS profiles were acquired along and across the diamond/oxide/metal interface. EELS mapping of the area of interest was also carried out. White numbered dots in **Figure 23**(b) show location of the recorded EELS spectra.

To easily understand the experimentally acquired EELS spectra, low loss spectra,

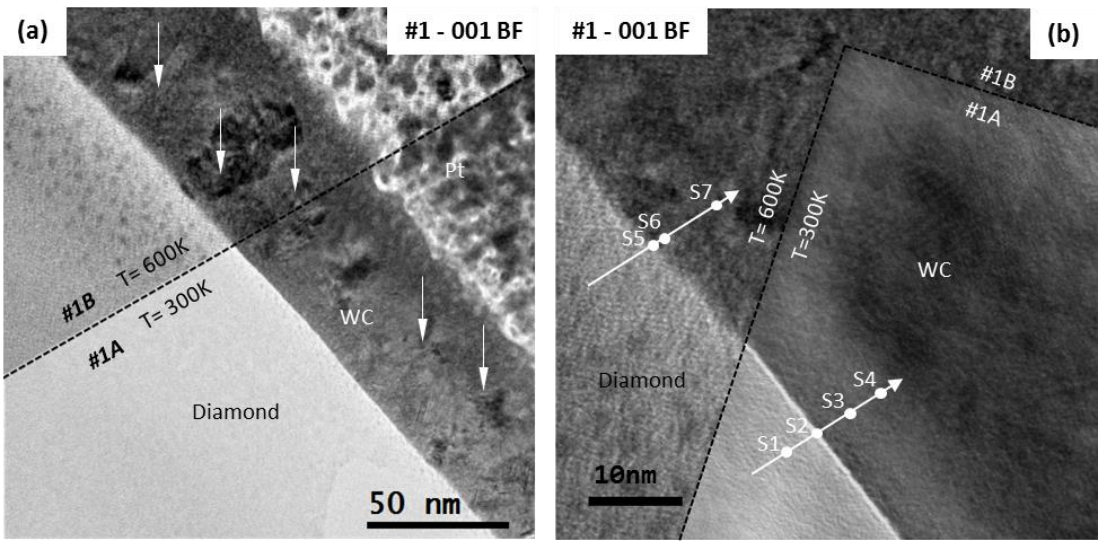

Figure 21: (a) Low magnification 001-Bright Field micrography of the WC/diamond SBD structure before and after a 600K annealing. White arrows are used to highlight grain formation. (b) 001-Bright Field micrograph of the WC/diamond interface before and after a 600K annealing. Numbered dots are used to highlight EELS probe position.

Table 6: Summary of the peak position in low-loss transition in amorphous carbon, pure diamond and pure tungsten.

Carbon		**Diamond**		**Tungsten**	
Label	Energy loss (eV)	Label	Energy loss (eV)	Label	Energy loss (eV)
C1	4.9	D1	20.7	W1	23.2
		D2	30.9	W2	41
		D3	60.9	W3	51.6

corresponding to amorphous carbon, pure diamond and pure tungsten are shown in **Figure 24.** All of them, used as a reference for each pure phase, are picked up from the literature (https://eelsdb.eu/). In **Figure 24** a figure, C1 carbon-related peak is revealed at 4.9eV; diamond-related EELS D1, D2 and D3 peaks are located in 20.7, 30.9 and 60.9 eV respectively (as presented in **Table 3**); finally tungsten-related W1, W2 and W3 peaks, located in 23.2, 41 and 51.6eV respectively, are presented.

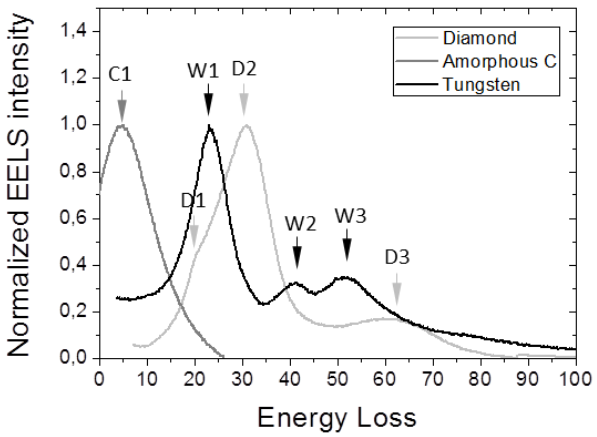

Figure 22: Low-loss EELS spectra for amorphous carbon. pure diamond and pure tungsten, as presented in literature (https://eelsdb.eu/).

Such transitions are summarized and presented in **Table 7**. Experimental EELS spectra, acquired at different locations of the interface of sample #1 are presented in **Figure 25**. **Figure 25** summarizes the results of the EELS analysis acquired across the WC-diamond interface after the 600K annealing.

Table 7: Summary of the experimentally observed EELS peaks right in the diamond-metal interface, compared with those of amorphous carbon, pure diamond and pure tungsten.

	Energy loss (eV)		Energy loss (eV)		Energy loss (eV)		Energy loss (eV)
C1	4.9	D1	20.7	W1	23.2	WC1	13.5
		D2	30.9	W2	41	WC2	23.9
		D3	60.9	W3	51.6	O-K	532

Such results can be compared with EELS spectra of pure diamond and pure tungsten, already presented. EELS spectra of pure diamond and pure tungsten are here used to identify the formation of a possible W-C mixture. Dark line in **Figure 25** is used to plot EELS data of #1A (annealed at 300K), while grey line is used to plot EELS data of #1B (after thermal treatment), spectra were acquired as shown in **Figure 23** (b).

- **S1 spectra, acquired in diamond bulk position of #1A**: low energy loss region shows D2 and D3 diamond-characteristic transitions, while D1 transition almost vanishes. This behavior can be explained by a slight amorphization produced during the FIB nanomachining (see II.2 Experimental techniques).
- **S2 spectra, acquired in the diamond-metal interface of #1A:** Low loss region shows the presence of WC2 peak, which 23.9eV energy is between that of D1 and W1 peak. W2 and W3 peaks are also revealed.
- **S3 spectra, acquired in the metal contact, near the interface of #1A:** Low loss signal shows WC1 peak at 13.5 energy loss. WC2, W2 and W3 peaks are also present.
- **S4 spectra, acquired in metal contact, far from the interface of #1A:** Low loss signal is identical of that of S3 position, while no peak is observed in the oxygen peak position.
- **S5 spectra, acquired in the diamond-metal interface of #1B:** Core loss region shows different carbon signature for the sample annealed at 300K (dark line) and at 600K (grey line). Oxygen peak is revealed at 532eV in both samples (spectra S2 and S5). However, oxygen signal in sample #1B (annealed at 600K, grey line), shows a more defined O-K line.
- **S6 spectra, acquired in metal contact, close of the interface of #1B:** Extremely weak peak, located at the oxygen signal position is detected in #1B.
- **S7 spectra, acquired in metal contact, far from the interface of #1B:** No oxygen-related peak is observed.

Data are summarized in **Table 7**. Both peaks seem to be characteristic of a tungsten semicarbide mixture. Oxygen peak is revealed right at the interface, thus verifying the

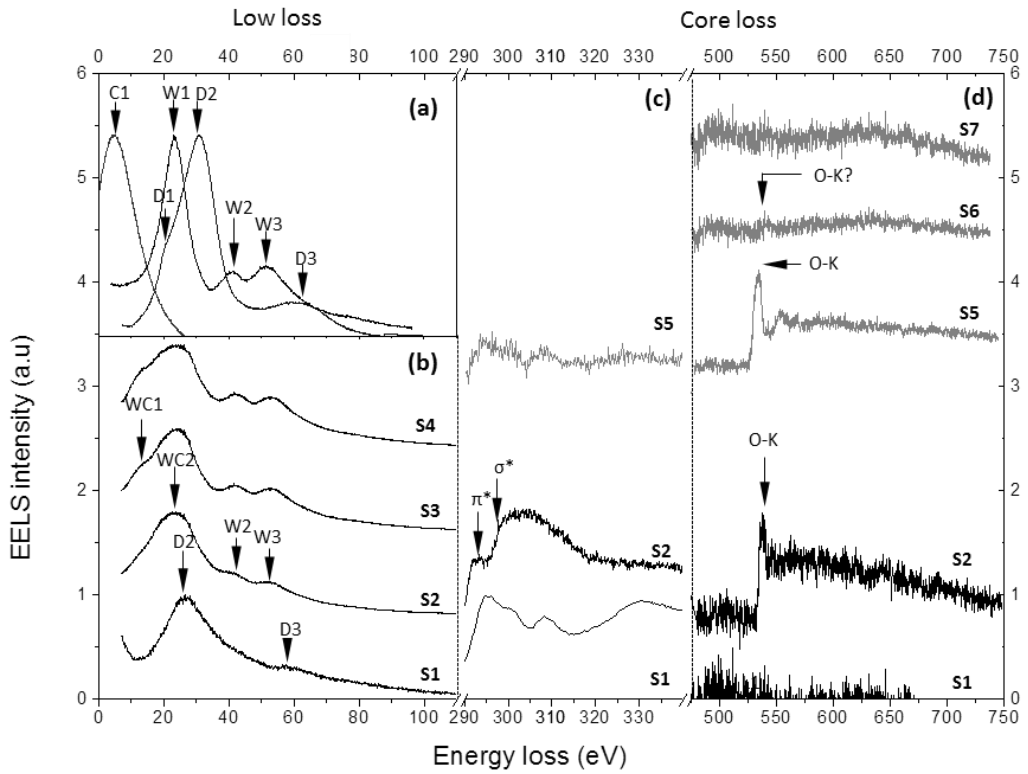

Figure 23: (a) EELS spectra of pure diamond, amorphous carbon and tungsten. (b) Experimentally acquired low-loss EELS spectra, measured across the WC-diamond interface in sample #1A (after 600K annealing). (c) and (d) Core loss EELS spectra measured across the WC-diamond interface in samples #1A and #1B. Dark line is used to plot EELS spectra of WC-SBD annealed at 300K (sample #1A), while grey line is used to plot EELS spectra of sample #1B (annealed at 600K).

presence of a thick oxygen-content layer before and after thermal treatment. However, after thermal treatment, spectra acquired in S6 position shows an extremely weak peak located at oxygen position, that may be related with some oxygen desorption through the WC layer.

On the other hand, spectra acquired in S2 position shows the simultaneous presence of the oxygen-related peak (O-K line, at 538eV) and a W-C mixture in the low loss spectra, as can be observed by the presence of WC1 and WC2 peaks at 13.5 and 23.9eV, respectively.

WC2 peak energy is between W1 and D2 energies, while WC1 is clearly different from D1 peak. W-characteristic peaks W2 and W3 are not shifted in S2-S4 spectra. π^* and σ^* peaks verify the presence of amorphous carbon in the diamond interface, however, this signature clearly changes when annealing at 600K.

Concerning the metal, WC1/WC2 ratio is slightly changing across the contact, meaning that stoichiometry of the W-C mixture is also changing.

Finally, as observed in S5 spectra, weak oxygen signal is still remaining at the WC contact in the vicinity of the diamond-metal interface. The latter can be related with oxygen diffusion from the interface to the contact, an effect that can be related with thermal treatment.

To evaluate this behavior, specific methodology is developed and described in the following section.

Interface analysis by STEM-EELS: oxygen quantification

To study the impact of the O-termination in different diamond devices, atomic composition of oxygen terminated diamond interfaces contacting with metals and oxides have been studied. Experimentally, this can be achieved by means of EELS in a sufficiently thin TEM specimen. The methodology is consisting in:

- A thin specimen, containing the interface, is evaluated by TEM. Sample has to be thin enough to provide High Resolution Electron Microscopy conditions.
- Nano-size EELS probe is located at the diamond/contact interface, as shown in **Figure 26** (a). This allows simultaneously probing the diamond bulk, diamond oxygen termination and first atomic layer of the metallic stack.

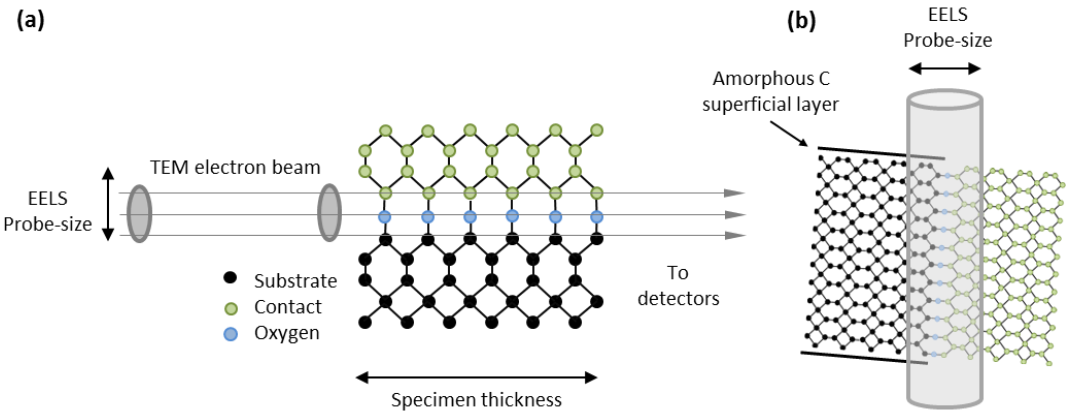

Figure 24: Diagram of the methodology used to evaluate O-terminated diamond/contact interfaces. (a) Ideal conditions for a thin TEM specimen and a perfectly oriented sample. (b) A more realistic situation, containing the relative EELS probe-size, the effect of a slight beam-sample tilt and the creation of a thin amorphous C layer during the FIB process.

- During TEM experiments, sample is positioned in a selected crystallographic orientation (in order to align atomic columns and to have a defined interface with respect to the electron beam), thus avoiding thickness-related effects (see in **Figure 26** (b)).

However, as the EELS probe size has a relatively large spot-size compared to the atomic scale, the atomic probe is not reached and the spot-size slightly averages the chemical quantification. In fact, diamond substrate, interface and contact are probed in the same EELS spectra (nominal size of the EELS probe is 0.19nm). Even though, the latter needs a signal intensity reference as the oxygen peak varies with the sample preparation thickness.

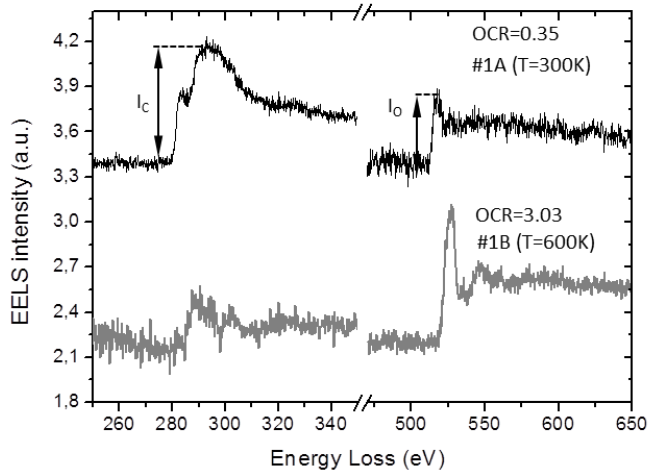

Figure 25: Experimental EELS spectra of O-terminated diamond/WC interfaces before and after thermal treatment and the associated OCR. Oxygen-related signal (O-K line) is revealed at 532 eV while carbon-related signal is revealed at 292eV.

Thus, at any location, comparing it to that of C, allows to avoid thickness effects. For this purpose, the oxygen/carbon intensity ratio is an appropriate parameter to have a relative quantification of the oxygen content. Oxygen-to-Carbon EELS peak intensity ratio (OCR) is defined as follows:

$$OCR = \frac{I_O}{I_C} \qquad \textbf{Eq. 4}$$

Where OCR is the O/C related peaks ratio, while I_O and I_C are the oxygen and carbon peaks intensities respectively. For measuring the carbon signal intensity, we use a 2eV window centered at 292eV in the EELS spectra; while oxygen signal is acquired with a 2eV window centered at 532eV (see details in **Figure 27**). To obtain more accurate data, O/C ratio were

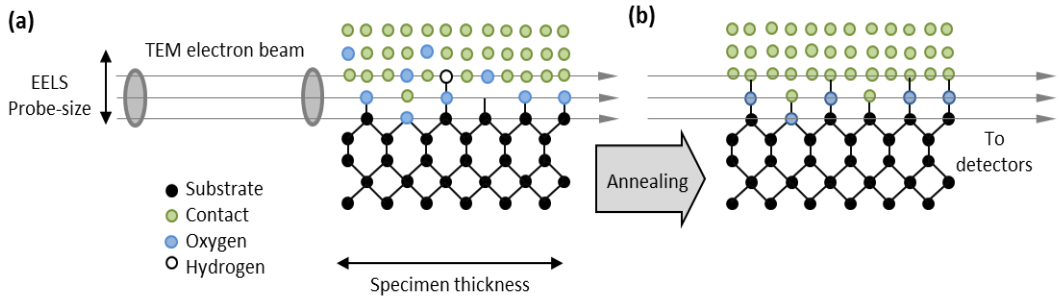

Figure 26: Schematic of the methodology used to study diamond/contact interfaces before (a) and after (b) thermal treatments. (c) Real EELS spectra acquired in a O-terminated diamond/WC SBD interface showing the parameters used in the definition of the Oxygen-to-Carbon EELS peak ratio (OCR).

measured by probing the oxide/diamond interface along a several nanometers linescan, thus allowing to calculate the mean value for each sample.

This procedure allows comparing O-terminated diamond interfaces, and can be used to evaluate the impact of the thermal treatment on this kind of structures (see **Figure 28** (a) and (b)). As the OCR is a mean value, determined over a finite distance of several nm, results will not only depend on the interfacial reaction and sharpness, but also on the interface nm-scale roughness.

In order to quantify the relative oxygen-content at one defined location, O/C ratio analyses were carried out in both SBD structures. As shown in **Figure 27**, O/C ratio (OCR) prior to the annealing (#1A) was around OCR=0.35 along the contact (data were acquired along an 80nm diamond-oxide interface), evolving to an OCR=3.03 value after the 600K annealing (#1B). This reveals an oxide gain of 66%, which can explain the related change in the ideality factor.

Here, we use OCR to evaluate the change on the rugosity of the interface; however, using this methodology, other parameters like the Oxygen-to-Tungsten EELS ratio (OWR) can also be defined. Nevertheless, O and W signals are hardly observable in the same EELS spectra: O low-loss EELS peak is extremely close to zero-loss peak, and O-K line (≈532eV) is far from the Tungsten M4,5 line (≈1840eV). This experimental limitation leads us to use the OCR parameter for this study.

The difference of the oxygen signal before and after vacuum annealing lead us to think in a surface reaction: probably, the oxygen film at the diamond surface is mixed by the collision of heavy W atoms and C during the sputtering by Ar plasma process. This means that some oxygen terminations are probably dissociated during deposition, thus highlighting the fact that WC-SBDs is sensitive to the surface oxidation method, as previously reported by Teraji et al. [59]. Indeed, during the plasma treatment, oxygen deposition probably did not result in

a monoatomic layer, covering the 100% of the surface; but should probably result in small accumulations of several atomic layers in some places, while in other ones, no oxygen is deposited. Thermal treatment and metal deposition are expected to modify this behavior. However, we don't know how the real oxygen-terminated surface is, because oxygen distribution in the diamond surface cannot be evaluated by EELS till the metallic deposition is done. The two possibilities, previously discussed, are expected and presented in **Figure 29**: formation of oxygen clusters (a) and homogeneous oxygen distribution (b).

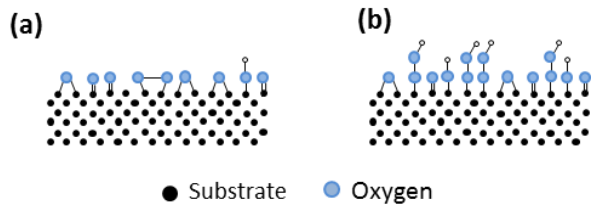

Figure 27: Schematic view used to illustrate different possibilities of oxygen distribution in diamond surface after VUV-ozone treatment (a) with oxygen clusters and (b) without clusters. Dangling bonds are expected in both possibilities.

After the EELS analysis, three facts are revealed in the WC/diamond structure:

- Oxygen atoms in the diamond-metal interface remain after the first annealing step (**Figure 30** (a)).
- The related electric behavior improves after first annealing, showing degradation in the last annealing step.
- O/C ratio improves with first annealing.

This leads to conclude that vacuum annealing makes the oxygen-terminated diamond/metal interface to be more homogeneous. Probably, a tungsten semicarbide (WC_xO_y) is formed in the interface during the 600K annealing [89]. Additionally, diamond oxygen-termination can be dissociated through heating, thus explaining the bad electric behavior at high temperatures; at the present time, additional experiments are required in order to verify these points.

The behavior of the oxygen signal (much weak prior to the thermal treatment) leads us to think in a redistribution of the oxygen atoms with the thermal treatment, as shown in **Figure 30** (a) and (b).

Probably, diamond-termination is mixed by the sputtering **Figure 30** (a)) and then, thermal treatment makes the diamond-oxide-metal interface more homogeneous: oxygen is, then,

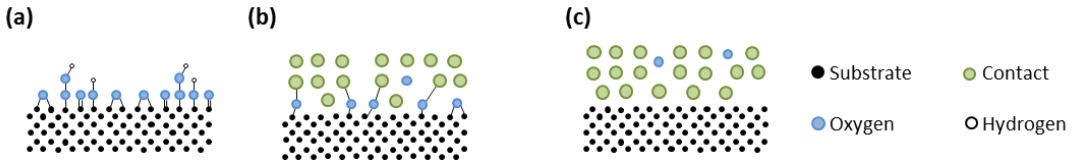

Figure 28: (a) Schematic of the oxygen-terminated diamond surface with the WC contact "as deposited-300K", (b) after first annealing at 600K and (c) after annealing at 700K, when oxygen desorption is expected.

well distributed just at the diamond-metal interface (**Figure 30** (b)). This mechanism explains the change in the related O/C ratio. Finally, high temperature annealing may induce oxygen desorption, as schematically shown in **Figure 30** (c).

III.3 Zr-based diodes [#2]

The fabrication of the pseudo-vertical diode structure of the Zr-based diode was previously described in II.1 Description of the samples. The decision of fabricating a pseudo-vertical diamond SBD was motivated by the fact of that vertical diamond Schottky diode structures suffer from the propagation of defects such as dislocations from heavily doped substrate (highly conductive substrate) in the diode active layer, as a result of epitaxial growth. The best values reported for critical field in vertical structures are 2.1 MV/cm [90] and 2.7 MV/cm [91], which is much lower than that achieved for the lateral diamond Schottky diodes (7.7 MV/cm in [92]). So, for Zr-based diode, a pseudo-vertical structure was adopted.

For the fabrication of the pseudo-vertical diode, active layer (p^- layer) is grown on a highly conductive epi-layer (p^+ layer) grown on an insulating diamond substrate. This design is generally used in order to get an electrical behavior close to that of the vertical structure. As for the vertical structure, the diode performance will be in part related to the crystal quality of the p^+ layer and furthermore to its doping level. A high quality p^+ layer will favor the minimization of defects inside the active layer (p^- layer). Moreover, this layer has to be sufficiently doped to get a metallic behavior to minimize its contribution to the diode serial resistance and achieve a negligible ohmic contact resistance.

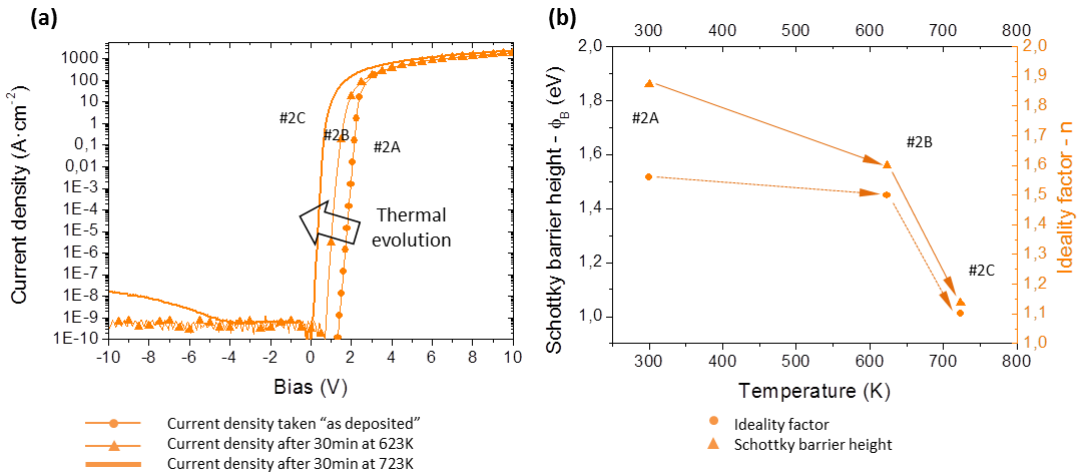

Figure 29: Electrical properties measured on the Zr-based diamond Schottky diode (a) and modifications to the electrical behavior induced by heating. (b) Evolution of the related SBH and ideality factors. Sample #2A is annealed at 300K, #2B at 623K and #2C at 723K.

Electrical properties[16]

Following the same procedure than in the WC-based diode, Zr-based diode was electrically characterized in each step of the thermal treatment. **Figure 31** (a) shows the current density vs voltage behavior of the Zr-based diodes with thermal treatment. As indicated in the figure, the slope of the related I(V) changes with thermal treatment, becoming "more ideal".

The performance of the related electrical behavior of this SBD structures vs the respective thermal treatment was also characterized by the combination of Φ_B and n by fitting **Figure 31** (a) with **Eq. 3**. According to the evolution of such parameters, we can observe that Zr-based SBD is improving till a 700K annealing without thermal degradation. Annealed Zr/p-diamond rectifiers exhibited a better electrical properties than as-deposited electrodes as reflected by the current density about $120A \cdot cm^{-2}$ for 723K annealing (#2C), $19 \cdot cm^{-2}$ for 623K annealing (#2B) and $0.61A \cdot cm^{-2}$ for as-deposited electrodes (#2A) at 2V. Zr-Schottky electrodes annealed at 723K exhibit a barrier height about 1eV, whereas the as-deposited electrodes have a SBH of 1.97eV. Besides the decrease on SBH, the annealing leads to a decrease of the ideality factor, thus suggesting an improvement of the Zr/p-diamond interface. To verify this, TEM measurements were required and are presented in next section.

[16] Electric measurements over #2 were carried out at Institut Néel by Dr. Aboulaye Traoré.

TEM-EELS characterization of the metal-semiconductor interface

Figure 32 shows 001 BF micrography of the SBD metallic stack (before and after a 700K annealing), ending in oxygen terminated diamond-Zr contact. As can be appreciated, prior to the thermal treatment (inset of **Figure 32**, corresponding with #2A, T=300K), different metals of the stack are easily identifiable. However, after a 700K annealing, metals seems to be slightly merged.

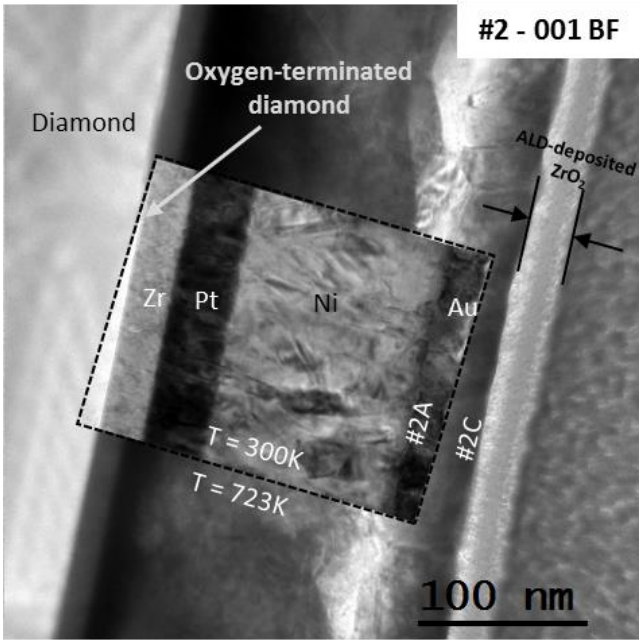

Figure 30: 001-Bright Field micrography of the metallic stack before (inset) and after a 700K annealing. Metal layers can be distinguished before thermal treatment (see inset). After a 700K annealing, layers seems to be slightly merged.

In **Figure 32**, it can also be appreciated an ALD-deposited ZrO_2 layer. Such a layer was deposited after all the electric measurements and thermal treatments. The purpose of this layer was to evaluate the differences between the ALD-deposited ZrO_2 and whatever is produced between the oxygen-terminated diamond interface and the Zr metal. As we will see, EELS spectra of ALD-deposited ZrO_2 will be compared

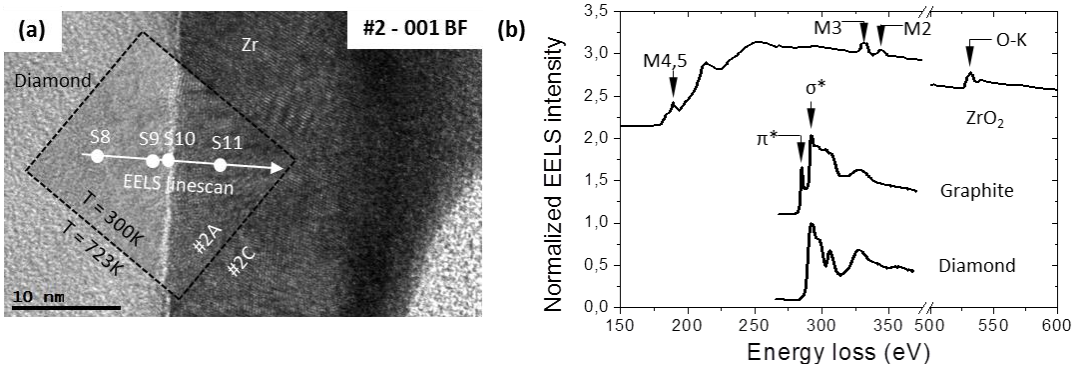

Figure 31: (a) 001-Bright Field micrography of the metallic stack before (inset) and after a 700K annealing. EELS probe positions are highlighted with white numbered dots. (b) EELS spectra for pure diamond, pure graphite and ZrO_2 as presented in literature (https://eelsdb.eu/).

with those spectra acquired right at the oxygen-terminated diamond/Zr interface.

A more detailed Bright-Field TEM image of the interface is shown in **Figure 33** (a). White, numbered dots are used in **Figure 33**(a) to label the probe positions where EELS spectra were carried out. Finally, **Figure 33** (b) shows EELS spectra (data are available in literature, https://eelsdb.eu/), to ease the comparison of the experimentally acquired spectra. EELS peak position of **Figure 33**(b) spectra are summarized in **Table 8.**

Table 8: Summary of the peak position of Zr, graphite and oxygen, as labelled in **Figure 31** (b)**.**

Graphite		**Zirconium**		**Oxygen**	
Label	Energy loss (eV)	Label	Energy loss (eV)	Label	Energy loss (eV)
π*	285	M4,5	189.3	O-K	532
σ*	291.6	M3	331.4		
		M2	343.9		

Figure 34 shows experimentally acquired EELS spectra, measurements were carried out in the "as-deposited" structure (300K, sample #2A) and probe positions are those of **Figure 33.** In **Figure 34**, typical diamond signature of EELS spectra is revealed in S8 position, while

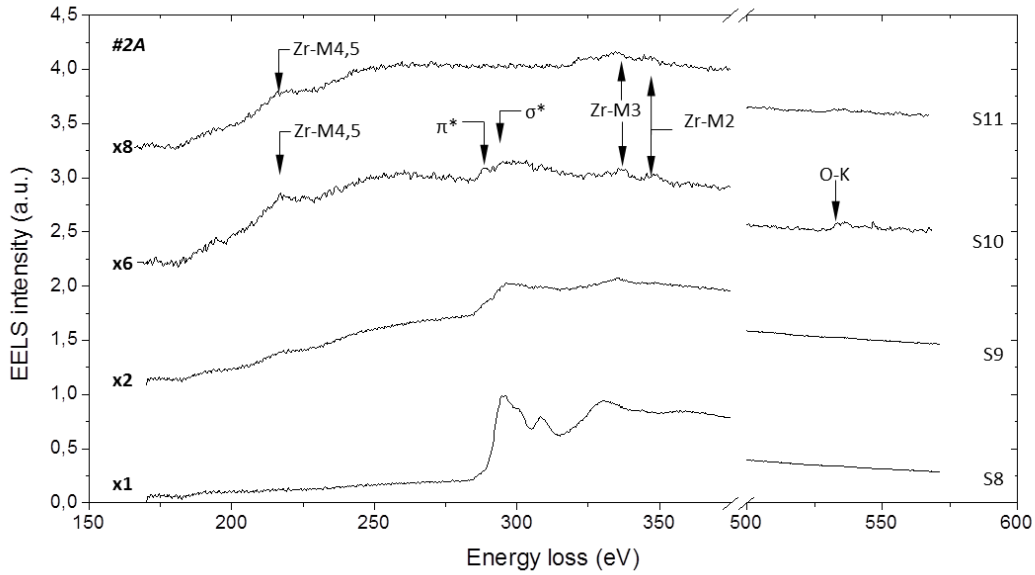

Figure 32: Experimental EELS spectra (sample #2A) acquired across the Zr-diamond interface (in as-deposited contact, 300K) are shown. Dark arrows are used to highlight the main EELS peaks, which can be compared with those of **Figure 31** (b).

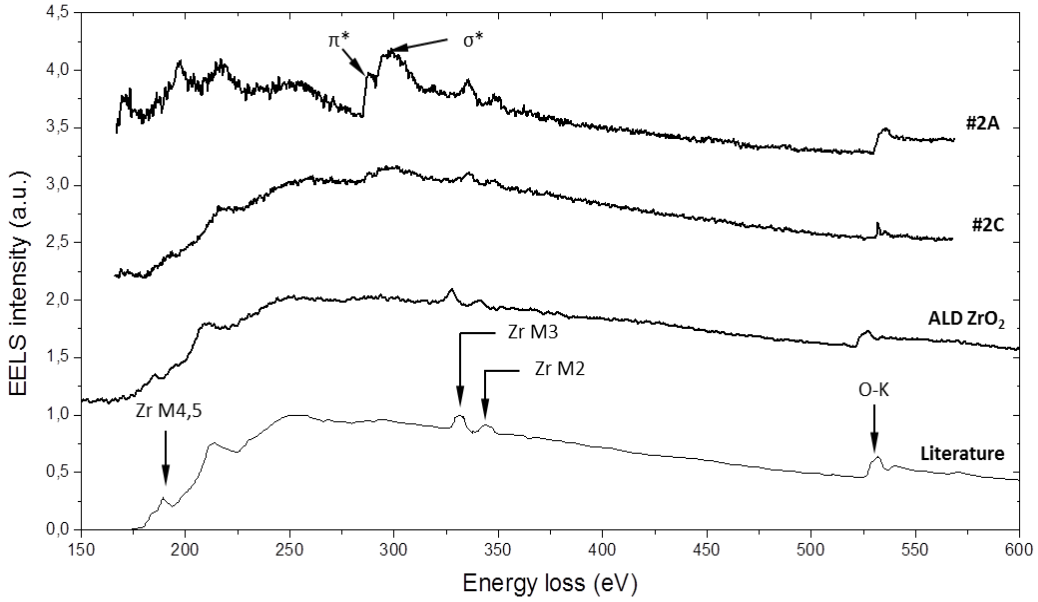

Figure 33: EELS spectra experimentally acquired at diamond/Zr interfaces before (#2A) and after (#2C) annealing. For shake of comparison, ALD-deposited ZrO_2 and EELS spectra of ZrO_2 from EELS database (https://eelsdb.eu/) are also presented.

slight amorphization is observed in the vicinity of the interface (spectrum S9, with carbon-shaped signature), probably due to FIB-related damages (see II.2 Experimental techniques for further details).

Position S10 corresponds with the diamond/metal interface; here we observe the presence of Zr-characteristic peaks and oxygen-related peak at the same time. Finally, no O-related EELS peak is observed in S11 position, confirming the presence of a thick oxygen layer between the metal/semiconductor contacts. Thus, oxygen is detected only at the interface.

Such oxygen layer is observed in all the annealing steps of sample #2, as revealed in **Figure 35**, where EELS spectra experimentally acquired in #2A and #2C interfaces are shown. Before annealing, carbon-related signal, Zr-related signal and O-related signal are present at interface. However, Zr-M4,5 peak seems to be shifted, probably due to a different stoichiometry Zr_xO_y formation (see spectra #2A in **Figure 35**). On the other hand, after a 700K annealing (#2C in **Figure 35**), Zr-M4,5 peak is slightly observed (see arrows) at 189.3eV. In this case, the presence of the O-related peak is recorded, which evidences the existence of an oxygen-content layer even after thermal treatment.

We can compare spectra #2C in **Figure 35** with ZrO_2 spectra acquired in the ALD-deposited and with ZrO_2 spectra from literature, and conclude that a thin zirconia layer is formed

between the oxygen-terminated diamond surface and the Zr metal contact after the thermal treatment.

Variations with thermal treatment[17]

To determine the oxygen distribution in the p-diamond/Zr interface, EELS mapping at the oxygen-peak energy is carried out (see spectrum at position S10 in **Figure 34**). Inset of **Figure 36** shows the EELS map of the oxygen peak intensity (red signal), where most of the oxygen signal is located at the metal/semiconductor interface, even when some weak oxygen signal can be observed in other points (probably due to oxidation or other experimental-related artifacts). This is confirming the confinement of the oxygen layer at the interface. It can also be observed some rugosity in the oxide layer, which can mean oxide thickness variations.

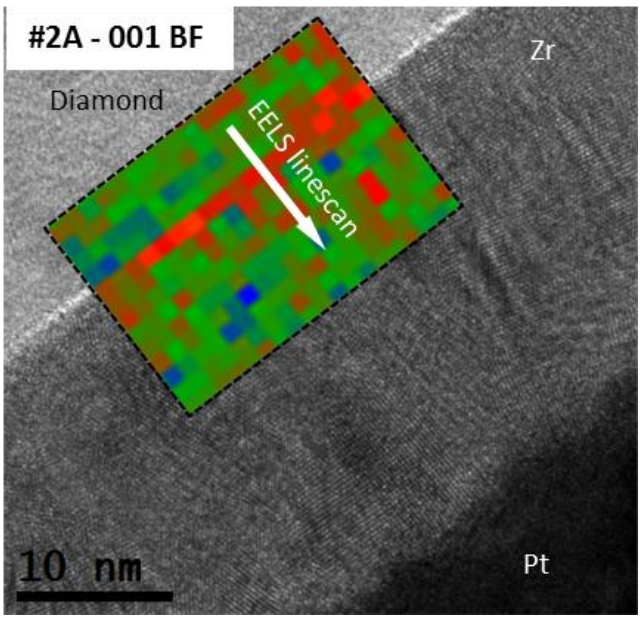

Figure 34: 001-Bright Field micrography of #2A and EELS mapping of the oxygen signal (inset, red signal). Oxygen is shown to be confined in the interface, with slight thickness variations.

To deeper investigate on this O-related layer at the interface, spectra linescans were carried out at the interface, before and after thermal treatment along a 20nm interface. To perform

[17] EELS mapping were obtained in cooperation with D. Méndez (Applications Specialist TEM in FEI company, Eindhoven, Netherlands).

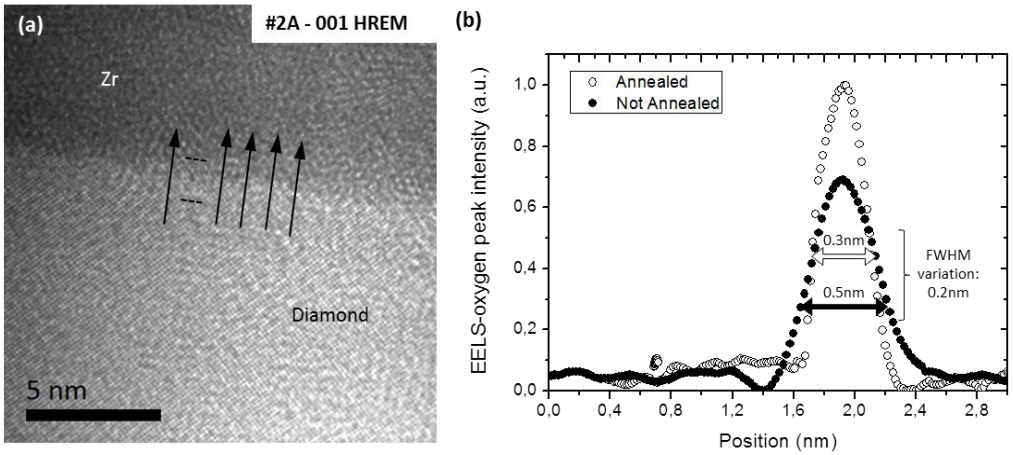

Figure 35: (a) 001- High Resolution Electron Microscopy (HREM) micrography showing the interface of sample #2A. Dark arrows are used to illustrate EELS linescans acquired along the interface. (b) EELS-oxygen signal intensity profiles acquired across the p-diamond/Zr interface before (#2A) and after (#2C) a 723K annealing, oxide thickness variation is revealed

this, an EELS probe of 0.1nm (nominally) was used to do 5nm linescans, crossing the interface along 20nm. Linescans were spaced for 1nm. Oxygen-related EELS peak intensity versus probe position is obtained.

This procedure allows improving the spatial resolution, thus averaging the distribution of the oxygen content along 20nm of the interface, as schematically illustrated in **Figure 37** (a). **Figure 37** (a) shows 001-BF micrography (very close to HREM conditions) of samples #2A and #2C.

In **Figure 37** (b), each point of the EELS linescan profile corresponds to oxygen-signal intensity. To improve the signal to noise ratio, each point is obtained averaging 20 EELS spectra at this defined position. When repeating this procedure in samples #2A and #2C, a variation in the oxygen layer thickness is revealed.

Prior to the annealing (#2A), this layer has a mean thickness of 0.5nm while, after a 723K annealing (#2C), the mean thickness becomes 0.2nm (near the probe-size resolution), thus showing a sharper layer: thinner and with increased oxygen content.

This means that the oxygen layer becomes “sharper” with annealing. Annealed and not annealed EELS profiles at **Figure 37** (b) were normalized by using the O-C ratio as described for the WC-based SBD.

As in the WC-based diode, the behavior of the oxygen signal leads us to think in a redistribution of the oxygen atoms with the thermal treatment. Again, probably, diamond-termination is mixed by the sputtering and then, thermal treatment makes the diamond-

oxide-metal interface more homogeneous (redistributing oxygen atoms in the metal/semiconductor interface).

This procedure could be carried out due to the high intensity of the oxygen signal. However, in the WC-based diode, O-signal intensity wasn't high enough to allow an acceptable resolution. This last fact highlights that the oxygen content in the Zr-based diode is higher than in the WC-based one.

III.4 Analysis of WC vs Zr-based Schottky diodes: physical behavior of the interface

Once the electrical, chemical and structural properties of each specific SBD configuration have been studied, both structures can be compared as competitor devices. **Figure 38** summarizes the obtained current density vs bias behavior. It can be observed that WC-based SBD presents an optimum response for an annealing temperature of around 600K (#1B, thick blue line in **Figure 38**), ideality factor is, then, close to 1. On the other hand, Zr-based SBD is still improving till 700K (#2C, hick orange line in **Figure 38**) and ideality factor remains high till a 700K annealing. WC-SBD shows an excellent rectification ratio of their related electrical properties, as revealed by the fact of that ideality factor value of n=1 is reached at 600K. On the other hand, #2C (Zr/O-terminated diamond, annealed at 723K during 30min, with a previous post annealing at 623K of the same duration) shows n=1.16, high enough to argue for inhomogeneous interface or defects. Differences between both metals yielding in the annealing temperature, and annealing duration are remarkable.

Results obtained in III.2 WC-based diodes and in III.3 Zr-based diodes are summarized in **Table 9**.

Table 9: Summary of the samples studied in this work with its corresponding annealing temperature. The related ideality factors and Oxygen-to-Carbon EELS are also presented for ease of interpretation.

	Contact metal	Annealing temperature (K)	n[a]	ϕ_B (eV)	OCR[b]
#1A	WC	300	1.44	1.36	0.35
#1B	WC	600	1.02	1.61	3.03
#1C	WC	700	1.9	1.58	
#2A	Zr	300	1.58	1.97	0.55
#2B	Zr	623	1.28	1.4	
#2C	Zr	723	1.16	1	1.5

[a]Values of ideality factor n described, see plot in **Figure 36**

[b]Oxygen-to-Carbon EELS ratio obtained by using **Eq. 4**

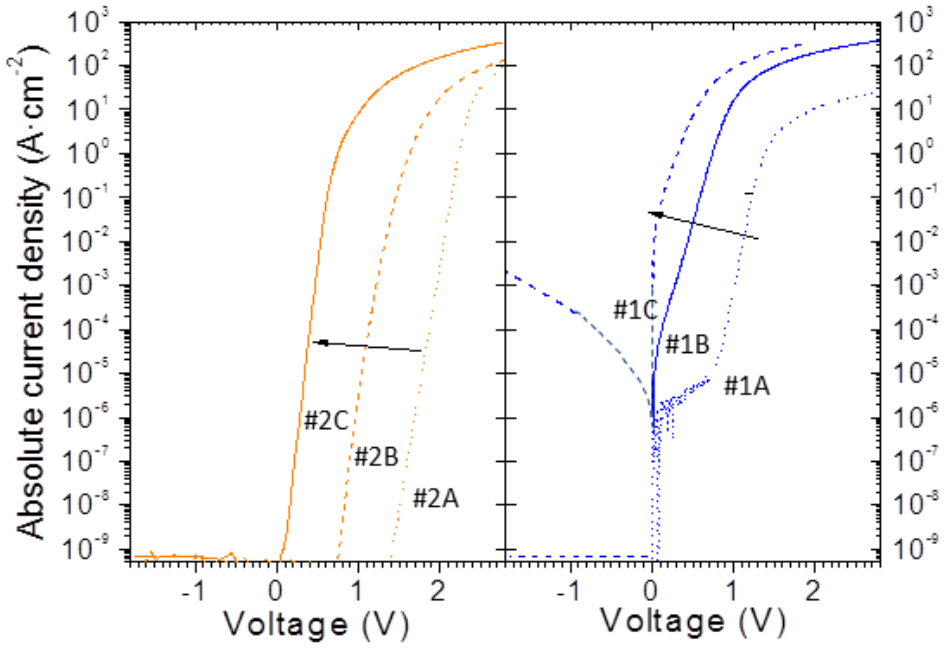

Figure 36: Electrical properties measured in WC and Zr-based diamond Schottky diodes: Modifications to the electrical behavior induced by heating over ZR-based (left) and WC-based (right) diamond Schottky diodes.

As can be appreciated in **Figure 38**, Zirconium Schottky contacts exhibited an extremely good rectification behavior characterized by a high current density 10^3A/cm^2 (at 6V), a reverse current density less than $1 \cdot 10^{-8}$ A/cm^2 up to the maximum voltage ($|V_{max}|$=1000V) available with the measurement set-up of institute Néel [86], and an ideality factor near 1.16 (see plot in **Figure 39**).

On the other hand, WC-based SBD shows degradation of the electrical behavior when annealing at 700K, while Zr-based SBD are still showing a good electrical response. WC-based and Zr-based SBD shows a decreasing of the related SBH in each step of the thermal treatment.

On the other hand, ideality factor becomes closer to 1 after each annealing step. In case of the WC-based SBD, **Figure 38** show an excellent rectification ratio below 700K, but this structure seems to degrade for annealing above 700K. Finally, Zr-diamond SBD shows a slower rectification ratio with the thermal treatment. Besides of that, Zr-diamond SBD structure seems not to degrade after a 700K annealing (see ideality factor value #1C in **Figure 39**).

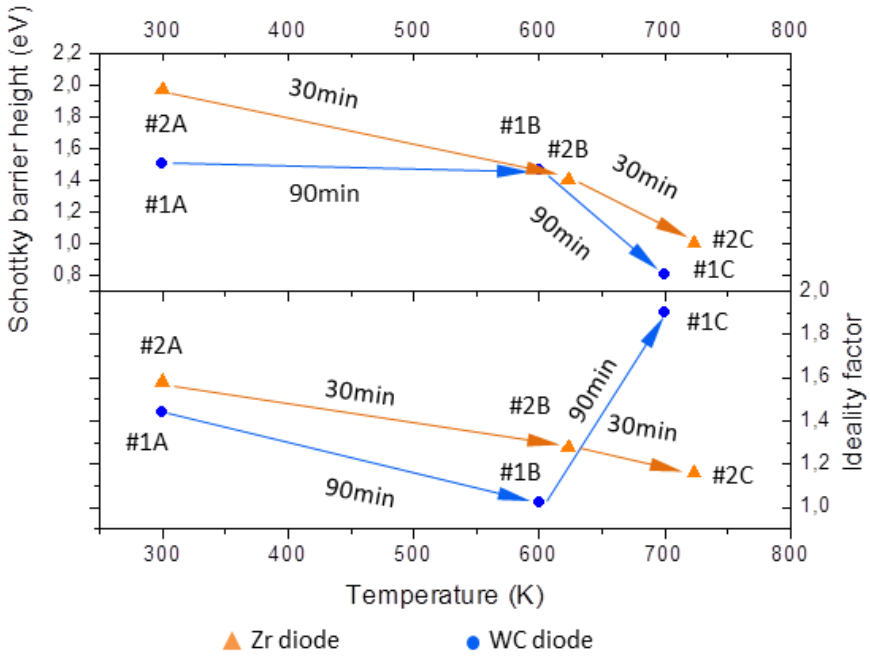

Figure 37: Plot of the evolution of the related Schottky barrier height (up) and ideality factors (bottom) for Zr-based and WC-based SBDs as summarized in **Table 9**

Comparing both structures as competitor devices, one can conclude that:

- Zr-based SBDs are showing lower reverse currents, higher Schottky barrier heights and an adequate electrical performance at high temperatures (>700K).
- WC-based SBDs shows ideality factor close to 1, meaning a more stable interface. However, oxygen desorption is produced at high temperatures (>700K).

Real metal-semiconductor contacts: Interface states

One can compare the experimental results of **Figure 38** with the expected theoretical behavior, issued from the thermionic emission theory already shown in **Figure 21**. For ease of consult, **Figure 40** summarizes both results. Some differences with respect to the ideal behavior can be appreciated in **Figure 40** (a).

The differences between ideal and experimental behaviors can be explained in terms of interfacial states. This is because the barrier heights of a metal-semiconductor contact are, in general, determined by both the metal work function and the interface states.

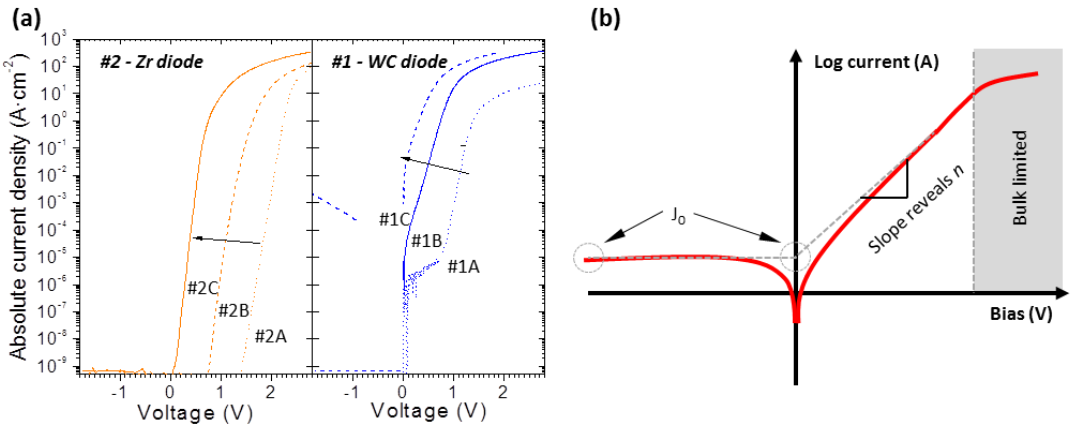

Figure 38: Experimental (a) and theoretical (b) behavior of SBDs.

As previously mentioned, when a metal is deposited onto a semiconductor, even when the metal film is smaller than a single atomic layer, the Fermi levels of the metal and semiconductor must match. This pins the Fermi level in the semiconductor to a position in the bulk gap. Shown to the right is a diagram of band-bending interfaces between two different metals (high and low work functions) and two different semiconductors (n-type and p-type).

A general expression for the barrier heights can be obtained on the bases of the following assumptions:

- With intimate contact between the metal and the semiconductor, and with an interfacial layer of atomic dimensions, this layer will be transparent to electrons but can withdraw potential across it
- The interface states per unit area per energy at the interface are a property of the semiconductor surface and are independent of the metal.

A detailed energy-band diagram of metal-semiconductor contacts (see additional information in Annex II)) is shown in **Figure 41**.

The first quantity of interest in **Figure 41** is the energy level $q\phi_0$ above E_V at the semiconductor surface. It is called the neutral level above which the states are of acceptor type (neutral when empty, negatively charged when full) and below which the states are of donor type (neutral when full of electrons, positively charged when empty). Consequently, when the Fermi level at the surface coincides with this neutral level, the net interface-trap charge is zero. This energy level also tends to pin the semiconductor Fermi level at the surface before the metal contact was formed.

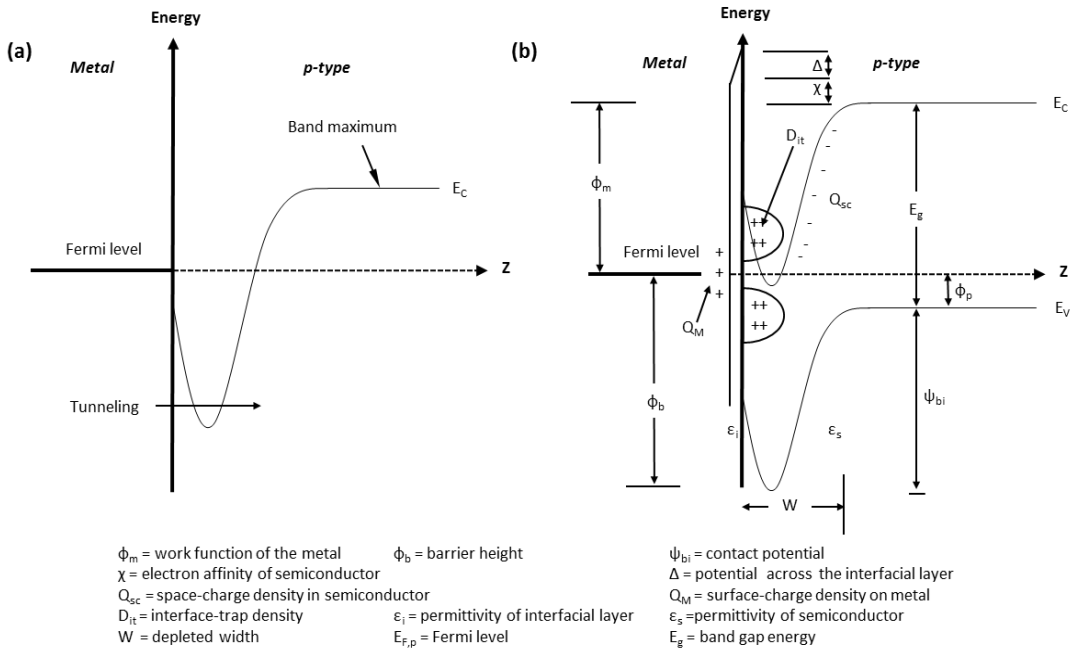

Figure 39: Energy-band diagram for a (a) metal-semiconductor contact and (b) a real metal-semiconductor contact with interface effects

The second quantity is $q\phi_p$, the barrier height of the metal-semiconductor contact; it is this barrier that must be surmounted by electrons/holes flowing from the metal into the semiconductor.

By supposing a potential change across the interfacial layer and using the image-charge model as described in [68], it can be proved that for a high interface trap density D_{it}, the Fermi level at the interface is pinned by the surface states at a given value ($q\phi_0$) above the valence band. The barrier height is independent of the metal work function and is entirely determined by the properties of the semiconductor.

For additional details on the Schottky effects and the barrier lowering phenomena, we emplace the reader to Annex II.

Effect of the thermal treatment on the O-terminated diamond surface

As demonstrated during this chapter, metal-oxygen terminated diamond junctions are known to be highly sensitive to annealing. This sensibility may be reflected in the thermal

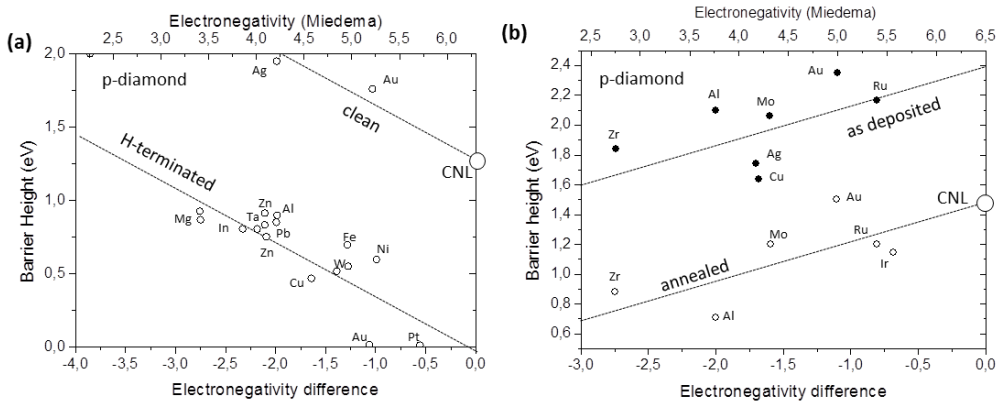

Figure 40: Barrier heights of metals/p-diamond contacts versus the difference of metals and carbon electronegativities reported by Mönch for clean and H-terminated diamond surface (a) and for metal/oxidized diamond for electrodes as-deposited and annealed at temperature ranging from 623 to 723K (b).

stability[18] of the interface existing between the metallic electrodes and oxygen terminated diamond. When the Schottky electrode does not react sufficiently with the oxygen passivation layer (as for noble metals such as Au), induces a posterior desorption of the oxygen termination with the thermal treatment (above 600 K), which degrades the Schottky contact [83].

The main consequences of this desorption process are an increase of the ideality factor (because of the apparition of spatial inhomogeneity) and a decrease of the Schottky barrier height. This diminution is a typical feature of diamond rectifiers based on oxygen-terminated surfaces [69, 93, 94]. This feature has been observed not only in Schottky electrodes that do not react sufficiently with oxygen layers (such as Au, Mo, Ru or Ir), but it has also been observed for easily oxidizable metals, like Al. The latter suggests the requirement of thermally stable interface layers to prevent the oxygen layer desorption when easily oxidizable metals are used. However, results obtained in Zr/oxygen-terminated diamond surfaces seem to provide an stable interface that avoids oxygen desorption. Taking into account the different oxidation features of the metallic electrodes plotted in **Figure 42** (b), it could be assumed that annealing can favor the establishment of chemical bonds between Schottky metals and O-terminated diamond, thus leading to oxide-type interfaces for Zr-electrodes.

A similar behavior can be expected in WC-based SBDs, the value of ϕ_b, 1.85eV, is consistent with the consideration that oxygen termination of diamond was dissociated

[18] The thermal stability of each annealing step is defined by the temperature range in which its barrier height can be considered as constant

through the tungsten-carbon bond formation between WC and diamond. Because of the reaction between WC and diamond during the WC deposition, interfacial bonding forms between WC and diamond. Here, most of the oxygen termination is probably dissociated during the deposition.

This result can be linked to the fact of ϕ_b is sensitive to the surface oxidation method (termination can be mixed by sputtering). This partially remaining oxygen-termination at the interface can lead to a more homogeneous interface when heating, till the point in which diamond-oxygen termination will be dissociated through the heating.

According with electronegativity theory, absorbed atoms at diamond surface induce a dipole layer [50] that can affect the diamond electron affinity (EA), as illustrated in "I.6 Motivation: impact of the interface configuration in diamond devices", thus inducing a negative (hydrogen, -1.3eV) and a positive (oxygen, 1.7eV) electron affinity. This explains the formation of a high SBH (above 2eV) for SBDs on oxygen-terminated diamond, whereas for hydrogen-terminated diamond surfaces, the barrier height is below 1eV.

In 1994, Mönch [45] demonstrates the correlation between the barrier height observed for metals/H-terminated diamond rectifier and C-H dipoles using MIGS-and-Electronegativity concept. Heine's MIGS concept defines a continuum virtual gap states in junction area due to the metal's electron wave functions tailing in semiconductor.

These virtual states are defined by their neutral level ϕ_0 (Charge-Neutrality Level CNL) inducing a Fermi level pinned even for ideal junction, thus predicting a linear correlation between SBH and the difference χ_m-χ_s of the metal and the semiconductor electronegativities. Zero bias SBH is, then:

$$\phi_b^0 = \phi_0^* - S_x(\chi_m - \chi_s) \qquad \textbf{Eq. 5}$$

… where ϕ_0^* is the Charge Neutrality Level (CNL) at the metal-semiconductor interface. The slope parameter S_x is calculated from the expression $A_x/S_x\text{-}1=0.1(\varepsilon_r\text{-}1)^2$, where ε_r is the electronic part of the static dielectric constant of semiconductor and A_x=0.86 (when Miedema's electronegativity scale is used [45]). According to the data presented in [45], the following slopes are deduced for the zero-bias SBH:

- Metal/clean surface diamond junctions $\phi_b^0 = 1.4 - 0.3(\chi_m - \chi_s)$
- Metal/hydrogen terminated diamond junction $\phi_b^0 = 0.017 - 0.37(\chi_m - \chi_s)$.
- Metal/oxygen terminated diamond junction $\phi_b^0 = 2.33 + 0.21(\chi_m - \chi_s)$
- Annealed metal/oxygen terminated diamond junction $\phi_b^0 = 1.45 + 0.23(\chi_m - \chi_s)$

Combining this result with the data reported in literature ([83, 94, 95]) **Figure 42** has been built. **Figure 42** (a) corresponds with clean diamond/H-terminated diamond surfaces, data were extracted from [45]. **Figure 42** (b) shows SBHs for metal/O-terminated diamond surfaces in "as deposited" and annealed electrodes. It can be noticed that the SBH diminution due to annealing is a common feature of easily oxidizable metals (Zr, Al) as well as for noble metals (IR, Au, Ru). Such a SBH diminution seems not to happen for Ag and Cu electrodes (even when they were stable up to 873K [95]). In case of Zr, Mo and Ru electrodes, a good electrical behavior and reproducibility were reported even after a 673K annealing, with a SBH dropping by approximately 1 eV.

Finally, additionally to the fact that diamond surface could be not entirely covered by oxygen layer, oxygen adsorption on diamond surface give rise to several terminations such as carbonyl (C=O), hydroxyl (COH), Carboxyl (O=COH group, and eventually epoxide (COC). It was demonstrated through theoretical calculations that these different terminations may induce different electron affinities [49]. Thus, according to the geometrical distribution of these different bonds, the SBH of a metal/O-terminated diamond junction could be spatially inhomogeneous. By annealing, a final state where an almost homogeneous interfaces with an ideal behavior can be reached (by cancelling the interface dipoles). Several mechanisms linked to the presence of an oxide layer can produce this effect (see [96]):

a) Effective disappearance of the oxygen-carbon dipole layer due to a new bonding arrangement at the diamond interface after annealing.
b) Compensation of the initial dipole layer by positive charges in the oxide, as usually due to extrinsic deep levels, often related to oxygen vacancies.
c) Intrinsic gap states within the oxide layer resulting in a new dipole induced by the alignment of the charge neutrality levels in the oxide and diamond.
d) A combination of these mechanisms or a change in the oxide properties which eventually promoted one of them after annealing

Figure 42 summarizes the picture for both SBD structures. In **Figure 42** (a), VUV/ozone

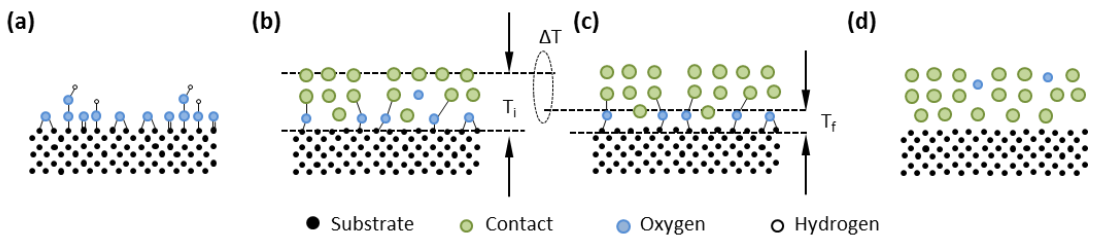

Figure 41: Schematic model of the O-terminated diamond interface after the VUV/ozone treatment, (a) as-deposited contact, (b) annealed, (c) annealed once annealed at 700K in the Zr diode and (d) annealed at 700K

treatment creates an O-terminated diamond surface. C-OH, C-O-C and other terminations are expected. Deposition of the metallic stack can lead to mixtures or O dissociation in the interface, as shown in **Figure 42** (b). Initial thickness of the oxide layer (T_i) of 0.5nm could be measured in case of the Zr diode. Once the samples are annealed a thin, sharp oxide layer is formed at the interface (see **Figure 43** (c)). Final thickness of the oxide layer (T_f) could be measured in the Zr diode. Finally, in case of the WC/diamond diode, oxygen desorption is produced at high temperature annealing (see **Figure 43** (d)); thus leading to the bad electrical behavior already shown. Probably, oxygen-termination is missed in some points of the diamond/metal interface just after the metal deposition. After thermal treatment atoms in the interface are locally displaced, thus contributing to the formation of a sharper interface (here, appreciated as an improvement of the OCR). For higher annealing temperatures, oxygen-termination is not stable and oxygen desorption leads to the disappearance of the O interface.

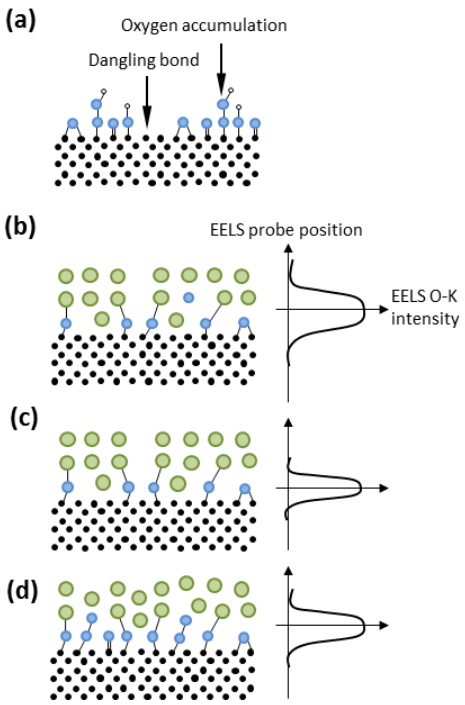

Figure 42: Schematic model of the O-terminated diamond interface (a) after the VUV/ozone treatment, (b) as-deposited contact, (c) annealed with ideality factor close to n =1 (case of the WC diode) and (d) annealed with a higher ideality factor but also with a higher oxygen content.

III.5 Conclusions

TEM-based techniques, particularly EELS-related ones, allow detecting and quantifying the oxygen content at oxygen-terminated diamond/metal interfaces. By using these techniques, we have demonstrated the following facts:

- VUV-ozone treatment of the diamond surface followed by metal deposition, leads to the formation of an oxygen-content layer both in WC/ and Zr/based diodes.
- Thermal treatment of such structures leads to oxygen redistribution in the interface, thus making a “more defined” interface (as evidenced by the oxygen-to-carbon ratio). This fact is also supported by the behavior of the ideality factor.

- Probably, diamond surface is not fully covered by oxygen after the ozone treatment. Additionally, oxygen accumulations can formed in the surface as presented in **Figure 42** (a).
- In WC-based diodes, thermal treatment at 600K leads to an ideality fact close to ideality (which means a clear and sharp interface). However, by heating up to 700K, such structures seem to degrade: ideality factor rises and oxygen desorption is expected. See **Figure 42** (b).
- In Zr-based diodes, thermal treatment at 623 and 723 leads to an improvement in the ideality factor. However, ideality factor of 1.16 is still high enough to argue for interfacial defects (see **Figure 42** (c)). On the other hand, no degradation is observed at 700K, and oxygen layer is evidenced to exist even at such high temperatures.

One can conclude that WC-based diodes leads to lower interface-states defects and more defined oxygen-terminated interfaces, but electronegativity of WC makes impossible to hold the oxygen-termination at high temperatures. On the other hand, Zr is an easily oxidizable metal, whose electronegativity allows holding diamond oxygen-termination even at high temperatures, even when such an interface is still defective.

Chapter IV: Diamond MOS structures

Metal-Oxide-Semiconductor structures, as part of the MOS Field-Effect-Transistor, are key structures of the modern electronics. MOS structures are needed to implement capacitors and to control the channel of a MOSFET.

IV.1 **Introduction:** An overview on the previous attempts on designing diamond-based MOS structures is presented. Atomic layer deposition (ALD) is used to create oxide-metal stacks over oxygen-terminated diamond surfaces. Classic Diamond MOS structures

- **MOS operation regimes**
- **Si vs diamond for MOSFETs**
- **Controlling the active channel**

IV.2 **Functional vs structural behavior of diamond-MOS structures [#3] &** [#4]**:** Diamond MOS structures were electrically characterized by capacitance/voltage (C(V)) and current/voltage measurements. To explain such behavior, diamond-MOS structures were characterized by a variety of TEM techniques. Particularly, EELS mapping of the oxygen-related peak allows an accurate measurement of the oxide thickness, as well as to explore oxygen distribution inside the oxide layer.

- **Experimental details**
- **Electrical properties**
- **Structural characterization of [#3] & [#4]**

***IV.3* Interface effects:** The observed nanostructure and electric behavior is here related with the surface states in the semiconductor.

- **Band bending**
- **Fermi level pinning**
- **Spotlight on interface traps**

***IV.5* Oxide charges:** Oxide defects, other than interface-related effects, were detected by TEM and C(V) measurements. Here, we summarize the evidences for the presence of oxide-related charges, following the next index:

- **TEM evidences of oxide charges**
- **Electric evidences of oxide charges**

IV.*6* Conclusions: Partial conclusions of this chapter are summarized here.

IV.1 Introduction

MOS structures are needed to store energy (acting as capacitors) [97] and also to control the channel in MOSFET devices [68]. The designs of practical capacitors vary widely, but all of them contains at least two electrical conductors (plates) separated by a dielectric (i.e. an insulator that can store energy by upon polarization). The conductors can be thin films, foils or sintered beads of metal or conductive electrolyte, etc. The non-conducting dielectric acts to increase the capacitor's charge capacity. A dielectric can be glass, ceramic, plastic films, air, vacuum, paper, mica, oxide layer etc.

MOS capacitors are widely used as parts of electrical circuits in many common electrical devices. Unlike a resistor, an ideal capacitor does not dissipate energy. Instead, a capacitor stores energy in the form of an electrostatic field between its plates. Capacitors are also used in electronic circuits for blocking direct current while allowing alternating current to pass. In analog filter networks, they smooth the output of power supplies. In resonant circuits they tune radios to

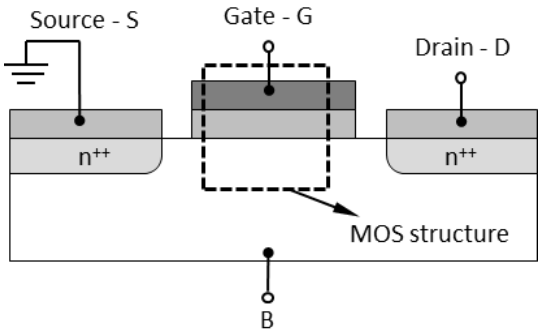

Figure 43: Schematic of a MOS-FET device, designed for n-type channel. MOS structure highlighted in dashed-square region.

particular frequencies. In electric power transmission systems, they stabilize voltage and power flow.

The metal oxide semiconductor (MOS) structure is a specific case of metal insulator semiconductor (MIS) structure where the insulator is an oxide. The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of oxide on top of a semiconducting substrate and depositing a layer of metal. As the oxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor.

When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a p-type semiconductor (being N_A the density of acceptors, p the density of holes; $p = N_A$ in neutral bulk), a positive voltage, V_{GB}, from gate to body creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions. If V_{GB} is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface in the semiconductor.

Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. When the voltage between transistor gate and source (V_{GS}) exceeds the threshold voltage (V_{th}), it is known as overdrive voltage.

Concerning the MOS-FET, its insulating behavior of a metal-oxide-semiconductor field effect transistor (as schematically presented in **Figure 44**) is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. In theory, this effect should allow to overcome the high ionization energy of diamond dopants in the channel. Carriers would then flow with a high mobility in the channel, opening the way for fast switching MOSFET able to withstand high voltage and to get rid efficiently of the heat, thanks to diamond material.

This structure with p-type body is the basis of the n-type MOSFET, which requires the addition of an n-type source and drain regions. We refer to Annex II for a brief introduction to the background of MOS and MOSFET structures.

MOS operation regimes

As its name implies, a metal-insulator-semiconductor (MIS) structure is composed of a stack of a metal, an insulator (generally, an oxide) and a semiconductor. An ohmic contact acting as a reference is necessary for applying a voltage on the metal gate. Here, we use energy-band diagram to introduce and highlight the capacitance behavior of these structures under different bias. In section A.2 Metal – Oxide – Semiconductor interfaces, different operations regimes, depending on the applied bias. Such operations regimes are schematically shown in **Figure 44**.

- V < 0 Accumulation: At this interface, the valence band is now closer to the Fermi level than further in the semiconductor when the bands are flat. This band bending causes an accumulation of majority carriers (here holes) in the semiconductor near the SC/oxide interface, giving its name to the regime called accumulation.
- V = 0 Flat band
- V > 0 Depletion: When a positive voltage is applied, the bands bend and a space

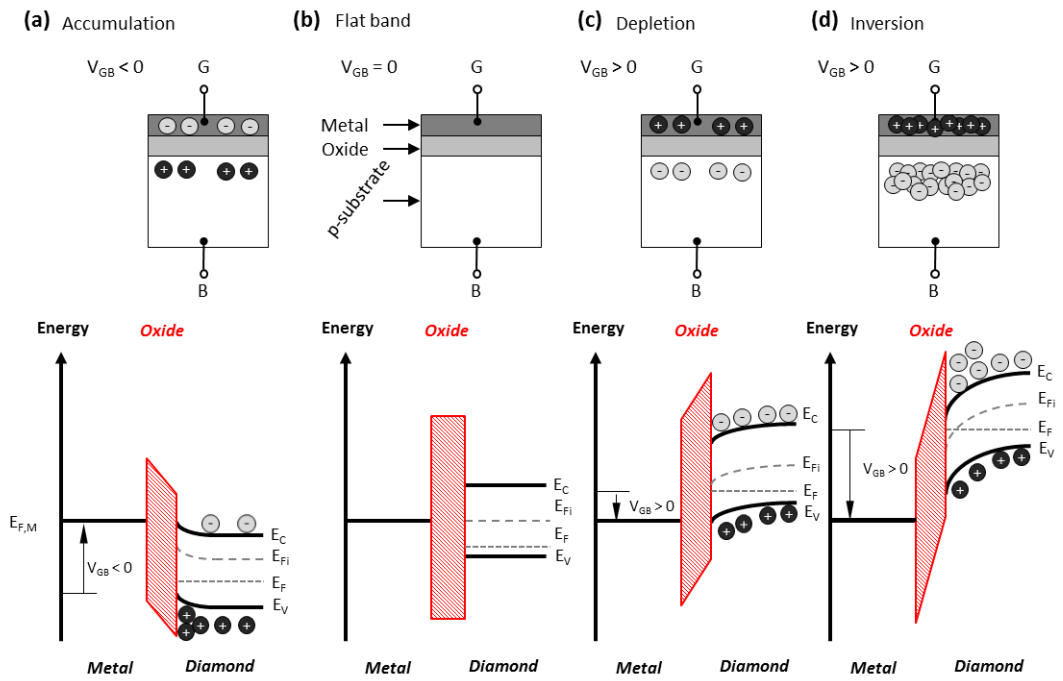

Figure 44: Band diagrams and charge carrier distributions at different regimes of a MOS capacitor (p-type substrate, n-type channel) showing: (a) accumulation, (b) flat band condition, (c) depletion and (d) inversion. Electrons, provided by the semiconductor without thermal generation are appreciated in inversion mode.

charge region appears where the majority carriers are depleted. This means those majority carriers are repulsed away from interface by the generated electrical field. This is the depletion regime.

- V >> 0 Weak inversion of charge carriers: When a larger positive voltage is applied, the bands bend downward more and more, until the Fermi level E_F crosses the intrinsic Fermi level E_i (E_i is the Fermi level for an intrinsic semiconductor, it lies at ~$E_g/2$ in the gap far from the oxide/semiconductor interface). Conduction at the SC/oxide interface is no longer carried out by the holes but by the electrons which are more numerous than the holes in this region. The semiconductor is said locally inverted (as more minority than majority carriers are present at the interface) and this regime is called the weak inversion.
- V >>> 0 Strong inversion: By increasing further the voltage, the strong inversion regime is reached. The sheet density of electrons in the inversion layer is now larger than the density of holes in the neutral part of the semiconductor. Usually, no distinction is made between weak and strong inversion regime and what is often called inversion regime corresponds to the strong inversion case described here.

Si vs diamond for MOSFETs

The conducting or insulating behavior of the MOSFET is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. Unfortunately, the physical properties of Si semiconductor do not allow building efficient MOSFET for power electronics applications (generally insulated gate bipolar transistor are preferred but also limited to 4k V).

MOSFET based on other semiconductors, like III-V compounds or SiC [98, 99], are improving but the performances of such devices are still not competitive with Si devices and, anyway, will be always lower than those expected for a diamond based MOSFET.

The first successful MIS structure made of SiO_2 on Si led immediately to the report of the famous Si MOSFET which is now ubiquitous in analog and digital electronics. Thanks to sufficiently clean SiO_2/Si interfaces (we do refer to I.6 Motivation: impact of the interface configuration in diamond devices), the inversion regime can be reached in silicon.

On the contrary, in the case of most semiconductors this regime has never been reached; mainly due to interface impurities that avoid a clean control of the interface band-bending.

Controlling the active channel

So, the main problem to fabricate a metal oxide semiconductor (MOS) structure is to achieve a high-quality semiconductor oxide interface (it means: sufficiently clean) in order to control the different regimes of the MOS: accumulation of majority carriers, depletion, deep depletion or inversion of carriers. This oxide/diamond interface is highly related to both the oxide and the diamond surfaces quality. Thus, the choice of the oxide as well as the diamond surface treatment is of the uttermost importance.

To address this challenge, taking into account the most common values reported in literature [61, 100], an aluminum oxide layer deposited by atomic layer deposition (ALD) on an oxygenated-diamond surface was the chosen option for the MOS structure, because of the expected match of the oxide with the diamond band gap as shown on **Figure 45** for a low doped diamond (values were taken from literature [50]). Moreover, the reaction leading to ALD aluminum oxide is known to be well initialized on hydroxyl (-O-H) terminated surfaces such as the oxygen terminated diamond one [101].

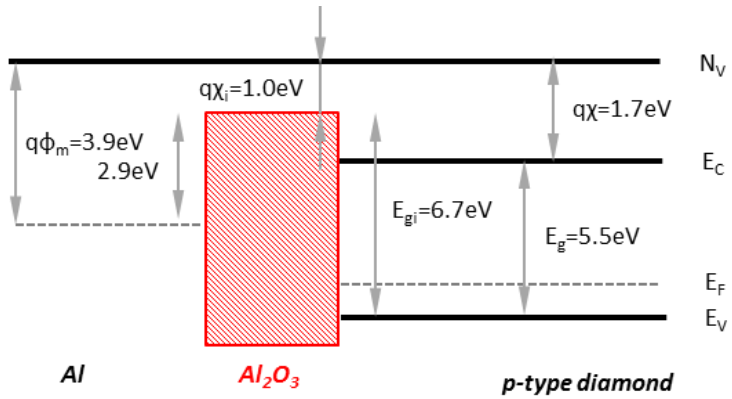

Figure 45: Theoretical band diagram of a MOS structure composed of a stack of Al/Al_2O_3/p-type diamond before Fermi level alignment.

The electrostatic control of the band curvature is a possible solution to solve the issue of the low ionization rate of the diamond dopants, but requires clean and low defect interfaces between oxide and semiconductor to avoid the Fermi level pinning at the interface. Therefore, MOS structures made of diamond as a semiconductor must be studied first, before fabricating the MOSFET device, in order to answer questions such as:

- Can a diamond MOS structure allow an electrostatic control of the channel to be achieved?
- If achieved, will the interface oxide/diamond be good enough (sufficiently clean) to avoid the Fermi level pinning and to allow reaching the inversion layer in a MOSFET?

IV.2 Functional vs structural behavior of diamond-MOS structures [#3] & [#4]

Literature shows that previous MOS structures performed on diamond [26, 102, 103] exhibited accumulation regime, but no deep depletion or inversion regimes. More recently, investigations of Al_2O_3 with hydrogen-terminated [104, 105] and oxygen-terminated diamond [61] demonstrate that such MOS capacitors could undergo accumulation, depletion and deep depletion. However, some structures in [61] are still presenting some undesired electric behavior. In this chapter, we will focus on the latter structures, exploring the relation between the thermal treatment of ALD growth conditions (ALD cycle of Al_2O_3 is briefly presented in **Figure 46**) and the oxide layer modifications in Al/Al_2O_3/diamond MOS structures. Oxide layer properties are expected to have an impact on the electrical response of such MOS structures.

Experimental details

The growth procedure of the studied Al/Al_2O_3/diamond MOS structures was presented in II.1 Description of the samples, as previously reported by Chicot et al. in [61] (in such contribution, the studied interfaces were labelled as #1 and #4). In such structures, the Al/Al_2O_3 stack is designed to act as gate electrode on a boron-doped epitaxial diamond layer. Gate electrodes are here characterized by a combination of TEM techniques.

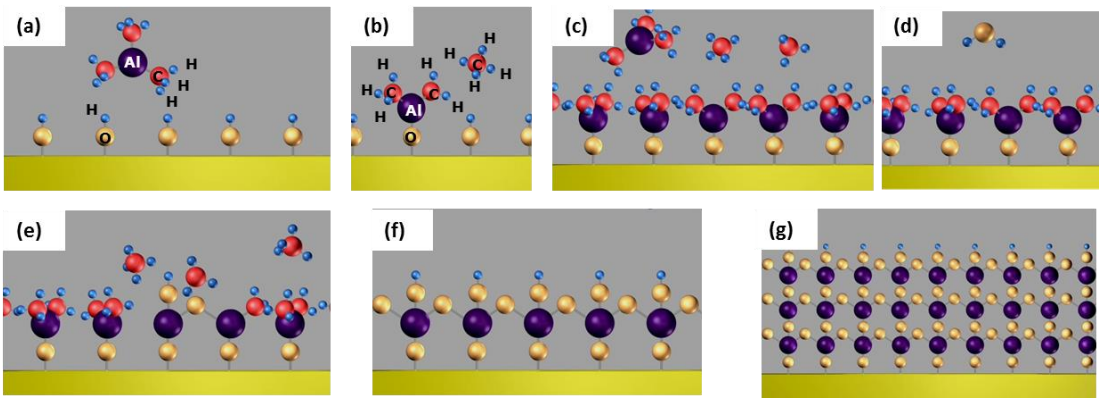

Figure 46: ALD cycle of Al_2O_3. Surface reacts with trimethyl aluminum (TMA) producing methane as reaction product (a), (b). TMA reacts with the adsorbed hydroxyl groups until the surface is passivated (c). H_2O pulsed into chamber (d) reacts with the new surface, forming Al-O bridges (e), (f). Again, methane is pumped and surface becomes passivated. Several cycles of TMA and H_2O pulses creates the layer Al_2O_3 (g).

Structure of samples #3 and #4 consists in a B-doped diamond layer with a boron concentration of around $10^{17}cm^{-3}$, on each; an ohmic contact (Ti/Pt/Au annealed at 750°C under high vacuum) was evaporated directly on the epitaxial layer to act as reference contact for capacitance measurement. After the creation of the ohmic contacts, diamond surface oxygenation was performed by deep UV ozone treatment [62]. Finally, photolithography process was used in order to selectively deposit the dielectric oxide.

Then, a 10 nm thick for sample #3 and 20 nm for #4 of Al_2O_3 dielectric oxide have been deposited by low temperature (100°C) ALD (see **Figure 46**), to preserve the lithography resist. The ALD system used in the present experiments was Savannah 100 from Cambridge NanoTech. The precursor used was trimethylaluminum (TMA), and the oxidant was H_2O. Using the same window in resist, the dielectric has been covered by a 100 nm thick aluminum metal using an electron beam evaporator. The resulting structures and further details are well described in [61].

Electrical properties[19]

Electrical properties of MOS capacitors have been measured using a Keithley 6517B source-electrometer apparatus for the static current/voltage I(V) characteristics and a Agilent E4980A Precision LCR Meter for the capacitance/voltage C(V) measurements. The measurements reported in this chapter were done with frequencies in the range of 50kHz to 220kHz by Chicot et al., details of the capacitance measurements can be consulted in literature [61]. To understand this plot, as well as to have a direct comparison between these data and the theoretical behavior, we refer to "A.I Metal – Semiconductor interfaces". In sample #3, different regimes can be observed on C(V) measurements (**Figure 49** (a)). For negative voltage ($V \leq -5V$), hole accumulation is observed.

This phenomenon was analyzed by Chicot et al., being is partially attributed to the presence of interface states or/and deep levels in the diamond layer close to the Al_2O_3/diamond interface (compensating levels in the first hundred nanometers under the Al_2O_3/diamond interface in a diamond growth without oxygen in the gas phase [62, 93, 106].

While the voltage increases, a space charge region begins to appear in the semiconductor. Then, for voltage increasing values ($V \geq 3V$), the capacitance starts to increase again (see arrow in **Figure 47** (a)). Usually, this kind of increase is characteristic of the strong inversion regime, where majority carriers are locally inverted; meaning that electron concentration at the oxide/diamond interface is larger than the hole density in the p-type diamond region.

[19] Electric measurements over #3 and #4 were carried out at Institut Néel by Dr. Gauthier Chicot.

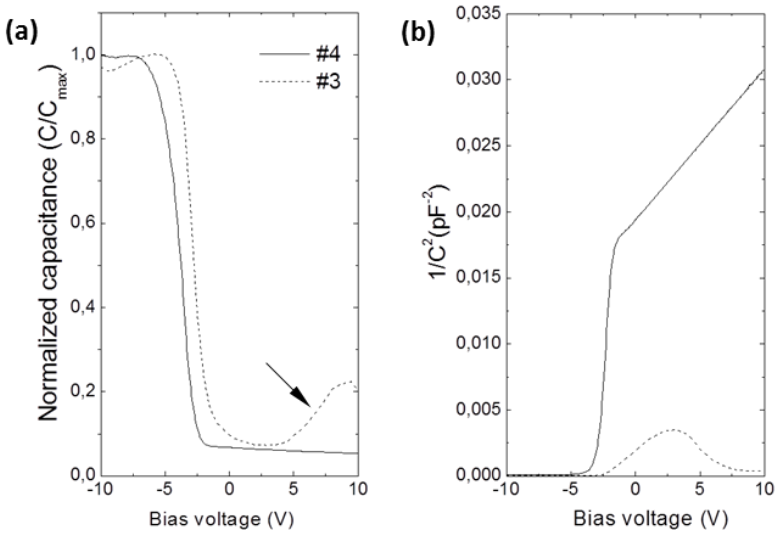

Figure 47: Experimentally acquired electrical properties of capacitors labelled as #3 and #4. (a) Capacitance C/C_{max} versus voltage measurement, and (b) $1/C^2$ versus voltage.

This behavior was explained in [61] by the fact of that diamond p-layer of sample #3 shows a large amount of defects such as hillocks. These defects are generally passing through the whole depth of the layer (it means: from the bottom to the surface of diamond), and can act as a mechanism to provide electrons from neutral regions through these defects up to the oxide/semiconductor interface. However, a measurement artifact due to the high oxide leakage current or impedance due to deep levels couldn't be discarded.

To clarify this, sample #4 was designed and fabricated. In this sample, hole accumulation and depletion are also observable. But, instead of increasing again the positive voltage range, the capacitance continues decreasing, as shown in **Figure 47** (a). This decrease is typical of the deep depletion regime. In fact, applying a linear fit to the $1/C^2$ vs voltage (**Figure 47** (b)), the effective doping of the p-diamond can be deduced. The good agreement of this fitting with the SIMS measurements confirms that the whole area of the capacitor is active.

In **Figure 48** the static I(V) measurements of both structures are shown. In sample #4, a quite high current density flowing across the "insulating" Al_2O_3 layer, and a not symmetrical behavior in the I(V) characteristic can be observed. The latter reveals more current flowing in the negative voltage (hole accumulation) than in the positive voltage (depletion). Moreover, for sample #4, the current is lower under positive voltage than under the negative ones. Assuming a very small barrier for holes when the structure is in deep depletion, the current is only limited by the insulating space charge region.

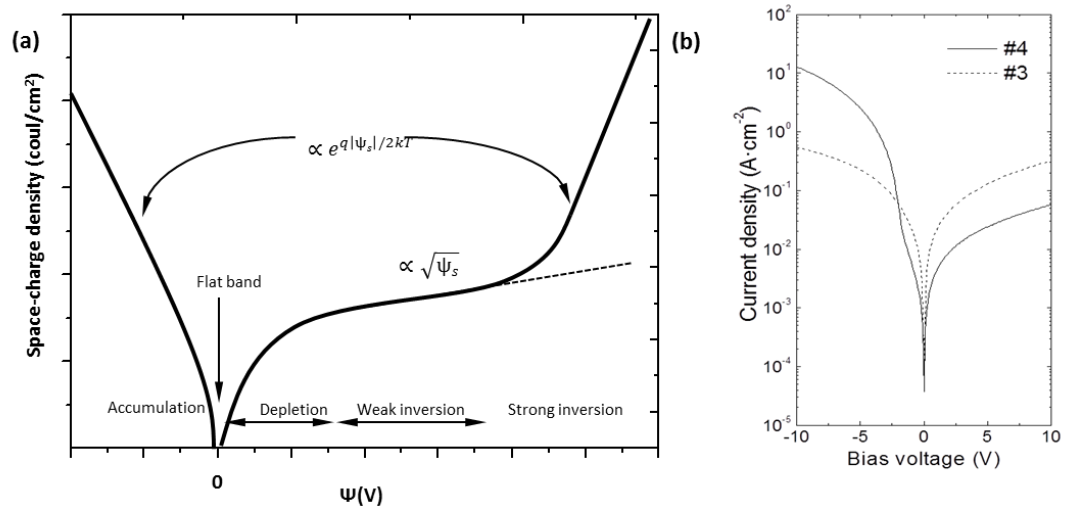

Figure 48: (a) Theoretical variation of space-charge density in a semiconductor as function of the surface potential for a p-type low-doped semiconductor. (b) Experimentally measured electrical properties of #3 and #4 capacitors, here static current versus voltage is shown.

On the contrary, for sample #3, the almost symmetrical current may be due to a parallel leakage path inside the depletion zone, as previously mentioned to explain the capacitance anomalies. The latter may be related with different oxygen content between metal and semiconductor, thus leading to bandgap fluctuations along the interface.

Structural characterization of [#3] & [#4]

To understand the differences in the electric behavior of #3 and #4, structural and chemical characterization of both MOS structures is carried out by combining CTEM and EELS experiments. **Figure 49** shows 001-BF micrography acquired in both samples.

Figure 49 has been composed to show both interfaces at the same magnification, #3 is shown in left/upper side and #4 is shown in bottom/right side. Arrows in **Figure 49** are used to guide the reader's eyes along the Al_2O_3 layer, white arrows are used for #3, while black arrows are used to identify the oxide layer in #4. It can be observed that the diamond/oxide interfaces of both samples are well defined, while the oxide/metal interface in #3 seems to be modified from point to point. Indeed, white arrows in **Figure 49** (oxide layer in #3) reveal variations in the oxide thickness.

On the other hand, black arrows in **Figure 49** are used to highlight diamond/oxide and oxide/metal interfaces of #4. It can be observed that both interfaces have a sharp transition and that the oxide thickness at #4 is remaining nearly constant.

To highlight oxide variations in #3, **Figure 50** was prepared. In **Figure 50**, a 001 BF micrography of #3 diamond/Al_2O_3/Al stack is shown. White arrows are used to label oxide thickness variations, revealing the following phenomena:

(1) 5nm stable oxide thickness
(2) bottlenecks with oxide thickness below 5nm
(3) oxide thickness over the expected 10nm ALD-growth oxide thickness

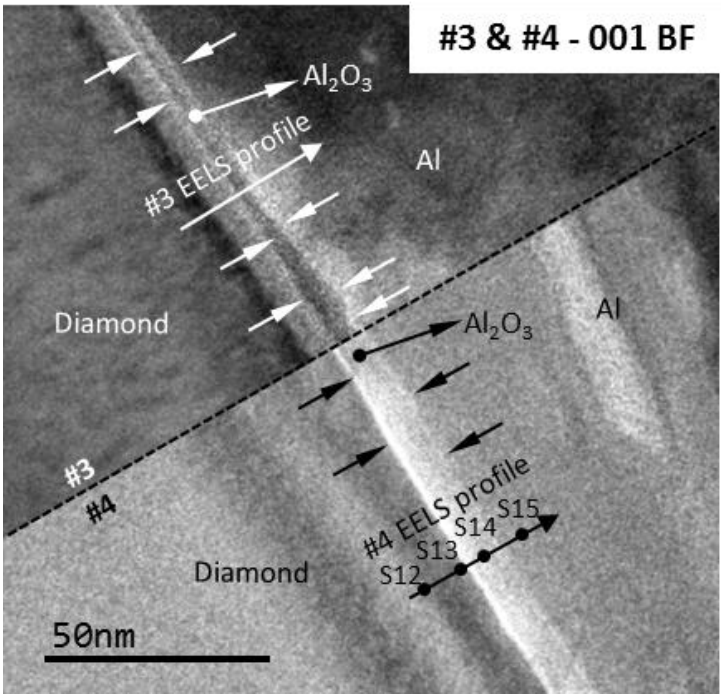

Figure 49: Bright Field micrography of the diamond MOS interfaces #3 and #4 and location of the EELS profiles

To get an accurate determination of the oxide thickness of samples #3 and #4, EELS analyses were carried out in both specimens. This technique allows acquiring structural and chemical information simultaneously. So that EELS spectra were acquired along the arrows indicated in **Figure 49**. EELS spectra, recorded at positions S12 to S15 of MOS structure #4, as indicated in **Figure 49**, are shown in **Figure 51**. The latter reveals Al_2O_3 formation (position S14) due to the presence of the oxygen-related O-K peak simultaneously with Al-related Al-K peak. This allows identifying the Al_2O_3 layer and, thus, measuring the oxide thickness along the MOS structure. On the other hand, positions S12 and S13 show a typical diamond

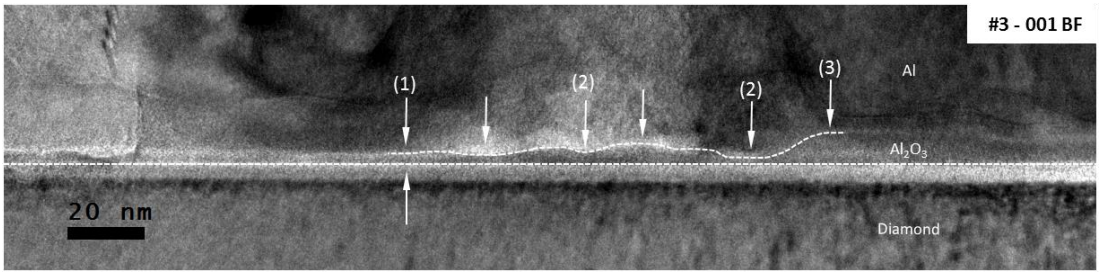

Figure 50: 001 BF micrography of #3 diamond/Al_2O_3/Al stack. White arrows are used to label oxide thickness variations: (1) 5nm stable oxide thickness, (2) bottlenecks with oxide thickness below 5nm and (3) oxide thickness over the expected 10nmALD-growth oxide thickness

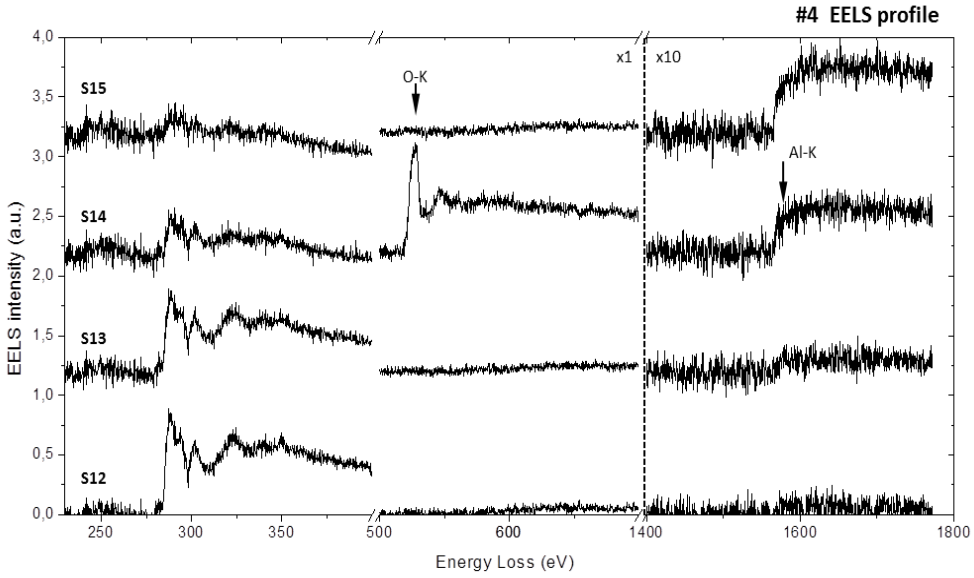

Figure 51: EELS spectra acquired in #4, following the linescan indicated in **Figure 49**. A: diamond substrate, B: diamond substrate near the interface, C: oxide layer and D: metal layer

shape EELS spectra. Some carbon signal is still remaining at positions S14 and S15, probably due to carbon redeposition produced during the ion milling of the FIB sample preparation procedure.

Once the presence of the oxide layer has been evidenced, EELS maps of the oxygen distribution in both structures were acquired. This allows evaluating the homogeneity of the oxygen distribution in the oxide layer, as well as an accurate measurement of the oxide thickness; oxide thickness variations and oxide thickness mean value.

Figure 52 shows oxygen map (green-blue scale) of #3 (a) and #4 (b) diamond-MOS structures. EELS maps were acquired by performing a 20x20 pixels mapping, with a 3nm EELS probe size and the same exposure time pixel by pixel. Inset of **Figure 52** (a) shows oxygen mapping of #3; it can be appreciated that oxygen signal is present on the Al_2O_3 layer, but also at some points of the metal layer, as spotted by label (3). In fact, **Figure 52** (a) shows an oxygen island inside the metal layer (upper-left side of inset, labelled as (1)). This is attributed to the presence of Al_2O_3 in the Al layer.

Probably, thickness's inhomogeneities in the ALD-deposited Al_2O_3 layer lead to the formation of vertical and curved structures. During a cross section study, these structures are appreciated as islands, with no apparent connection with the Al_2O_3 layer. On the other hand,

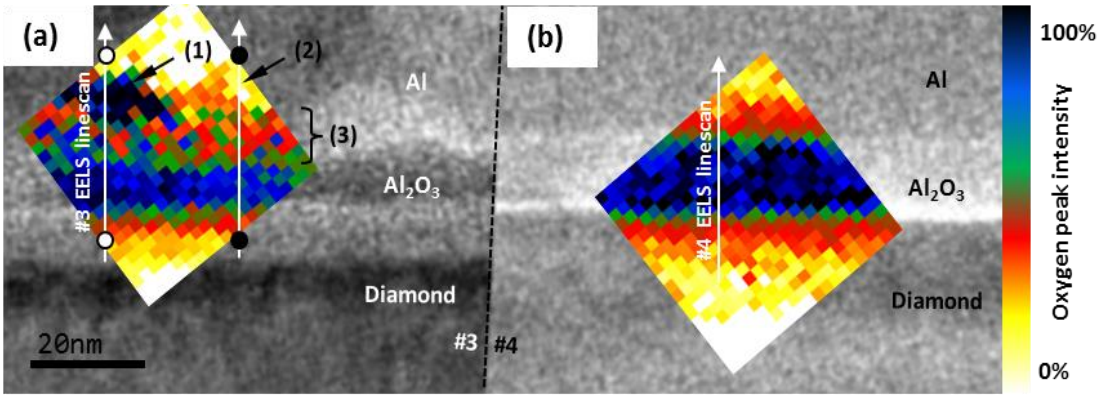

Figure 52: EELS mapping (insets) of the oxygen signal (blue color) in oxide layer of samples #3 (a) and #4 (b). In sample #3, oxygen signal could be observed inside the AL metal layer, revealing inhonogeneities in the oxide thickness. Figure also shows the position where EELS linescans were acquired in both samples.

oxygen map on #4 is shown in **Figure 52** (b); an homogeneous oxygen distribution and sharp transitions at both sides of the interfaces can be observed.

EELS mapping for #4 (presented at inset of **Figure 52** (b)) reveals an oxide mean thickness value of around15nm (20nm thick oxide layer was expected by the growing procedure). However, sample #3 shows a 5nm thick oxide layer, with thickness variations in the same order of magnitude than the width of the oxide layer. Indeed, an oxide thickness between 3 and 15nm was evidenced by EELS in #3. Furthermore, it can be appreciated that in **Figure 52** (a), oxygen distribution in #3 is not homogeneous inside the oxide layer. The latter can be related with oxide/metal mixtures.

Oxygen inhomogeneities can be revealed by profiling the EELS oxygen-peak intensity across the oxide layer. **Figure 53** shows the EELS oxygen-peak intensity profiles, acquired at the positions highlighted in **Figure 52**; grey rectangle is used to mark the position of the diamond bulk. A 0.1 nm probe size was used for oxygen-intensity EELS profiling.

Oxygen distribution in samples #3 and #4 are revealed, in **Figure 53**, by:

- Unfilled dots are used to plot EELS linescan corresponding with label (1) in **Figure 52** (a)
- Filled dots are used to plot EELS linescan corresponding with label (2) in **Figure 52** (a)
- Thick black line is used to plot EELS linescan corresponding to **Figure 52** (b)

Note that data shown in **Figure 53** are presenting higher resolution than those presented in **Figure 52** mapping. This is because EELS profiles in **Figure 53** were averaged over 5nm (so, each profile in **Figure 53** corresponds to the averaged value of 5 linescans).

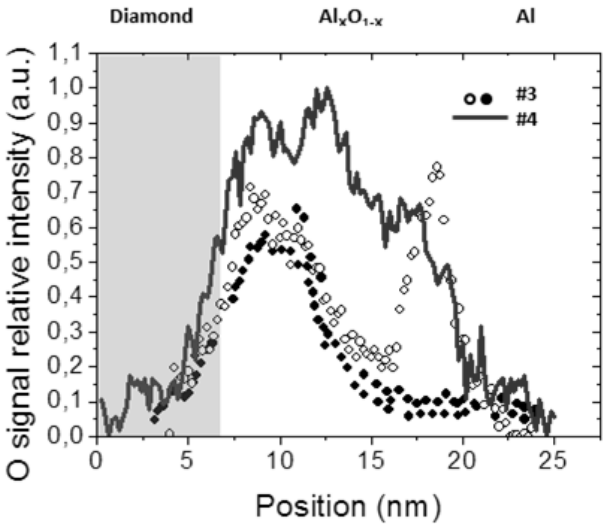

Figure 53: EELS oxygen-intensity profiles of samples #3 and #4 acquired along the linescans shown in **Figure 49.** Second peak in unfilled dot line plot corresponds with an "oxide island" inside the Al layer, as shown in inset of **Figure 52** (a)

Back to discussion, **Figure 53** evidences that oxide layer in #3 is presenting inhomogeneities: oxygen seems to be concentrated in the vicinity of the diamond bulk. A similar behavior is observed in sample #4 (black thick line in **Figure 53**), with a higher oxygen content near the diamond-side of the contact. Finally, oxide island revealed in inset of **Figure 52** ((a), label (1)) is also presented in **Figure 53** as a second peak in de unfilled dot-line plot. This behavior can lead to Al/diamond shortcuts, explaining the electrical behavior discussed in the last section.

For an accurate comparison of both oxide layers, O/C ratios were acquired as described in Chapter III (see **Eq. 4)**: "Interface analysis". The latter allows measuring OCR values of 0.96 for #3 and 3.85 for #4. This means that the oxygen signal is almost four times higher in #4 if compared with the carbon signal. This result allows a direct comparison of the oxide gain in both samples, thus allowing to determine the relative efficiency of the oxygen incorporation in both structures.

Table 10 summarizes the key results obtained in this section. Oxide thickness variations in #3 have been evidenced and oxygen distribution in the oxide layer varies in both samples.

Table 10: Summary of the samples studied in this chapter with its corresponding experimentally measured oxide parameters obtained by combining CTEM and EELS techniques

Sample	Nominal oxide thickness (nm)	Measured oxide max. thickness (nm)	Measured oxide min. thickness (nm)	Measured oxide mean thickness (nm)	OCR
#3	10	15±1	≈3±1	5	0.96±0.02
#4	20	15±1	15±1	15±1	3.85±0.02

Even though the ALD experimental procedure is identic in both samples, strong differences in terms of electrical behavior and nanostructure are revealed. It can be tentatively attributed to some substrate differences as much or to a partial passivation of the oxide layer during the ALD-growth.

The difference in OCR may be related with the presence of oxygen vacancies (V_O) in #3. The shape indicates that oxygen atoms migrate toward the metallic contact (Al), probably as a consequence of the electrical measurements (samples are electrical strained). Indeed, polarization can drive the electrically charged vacancies (V_O) to one side of the oxide layer.

IV.3 Interface effects

The previously presented electric behavior of #3 and #4 (**Figure 47** and **Figure 48**) differs from that of the ideal MOS structure. Here, we explain these differences according to the theory of real metal-oxide-semiconductor structure. Further information can be found in literature [68, 107].

Surface states

Due to the interruption of the periodic lattice structure at the surface of the crystal, interface traps Q_{it} (historically also called “interface states”, “fast states” or “surface states”) exists within the forbidden gap. Surface states are electrically active states, resulting from the disruption of the periodicity of the lattice at the semiconductor surface, formed due to the sharp transition from solid material that ends with a surface and are found only at the atom layers closest to the surface.

The termination of a material with a surface leads to a change of the electronic band structure from the bulk material to the vacuum. In the weakened potential at the surface, new electronic states can be formed, so called surface states. On the other hand, an interface trap is an electrically active defect, located at the interface between oxide and

semiconductor, capable of trapping and de-trapping charge carriers. Interface traps have an adverse effect on device performance.

We conclude that, when the periodic pattern of chemical bonds in the crystal is interrupted at the surface, it results in unsaturated (dangling) bonds, which can rearrange themselves (surface reconstruction) and/or which might be saturated by a (mono) layer of atoms (sometimes oxygen). This results in a change of both the surface crystal structure and the allowed energies that depend sensitively on the materials and bulk crystal structures involved. Often, the electronic surface structure has little to do with the bulk structure. The surface states can be probed, for example with scanning tunneling techniques or with photo emission spectroscopy.

The number of surface states per area is essentially given by the number of atoms per area at the surface. These states can be comprised of states that in the infinite, boundary less crystal would have contributed to either the conduction or the valence bands and can be an admixture of both types of bands. Due to charge neutrality, in the case of the intrinsic semiconductor the number of filled surface states is equal to the number of electrons that were removed from the bulk valence band due to surface formation, resulting in a neutral, uncharged surface. The remaining surface states are empty.

Filled surface states have electrons that in principle could be given into empty available states and can therefore be considered donor-like states. Vice-versa: empty surface band states are called acceptor-like. The energy up to which the surface states (within the surface band) are filled in the intrinsic, un-doped semiconductor is dictated by charge neutrality and is sometimes referred to as the charge neutrality level or charge neutrality chemical

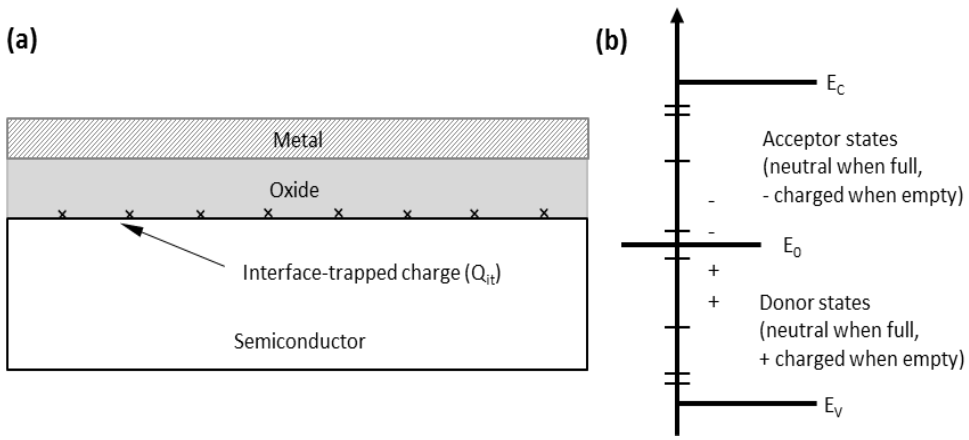

Figure 54: (a) diagram of a MOS stack where interface-trap region is highlighted and (b) interpretation of a system with both acceptor and donor states with a neutral level E_0 above which the states are of acceptor type and below which of donor type. When E_F is above/below E_0, net charge is – /+.

potential.

Similar to bulk impurities, an interface trap/surface state is considered a donor if it is neutral, and can become positively charged by donating (giving up) an electron. An acceptor interface trap is neutral and becomes negatively charged by accepting an electron. Presumably, every interface has both kinds of traps. A convenient notation is to interpret the sum of these by an equivalent distribution D_{it}, with an energy level called neutral level E_0 above which the states are of acceptor type, and below which are of donor type (see diagram in **Figure 56** (b)). Note that, when a voltage is applied, the Fermi level moves up or down with respect to the interface-trap levels and a change of charge in the interface traps occurs. This change of charge affects the MIS capacitance and alters the ideal MIS curve

Band bending

For a bit more quantitative consideration, let z_{dep} denote the extent of the depletion region into the bulk starting from the surface at z = 0, and N the dopant density (per m^3). All donors are ionized in the depletion region, giving a space charge density of ρ = eN. The Poisson equation for the z-dependence of the potential V(z) within the depletion region $0 \leq z \leq z_{dep}$ is [107]:

$$\frac{d^2V}{dz^2} = -\frac{e^2N}{\epsilon\epsilon_0} \Rightarrow V(z) = -\frac{e^2N}{2\epsilon\epsilon_0}(z - z_{dep})^2 \qquad \textbf{Eq. 6}$$

Where the normalization of V was chosen as V = 0 in the bulk (for $z > z_{dep}$) and the constant of integration was chosen to match $V(z_{dep}) = 0$ accordingly. According to **Eq. 6**, the bands are therefore bending quadratically, with a total shift of V ($z \rightarrow 0^+$) = $-e^2Nz^2_{dep}/2\epsilon\epsilon_0$. More generally, the local curvature of a band is proportional to the local space charge density. At the surface Z = 0, V(z) will jump (over the narrow extent of the surface charge accumulation layer), due to the charge accumulated strongly localized at the surface n_s.The surface accumulation charge is of equal size but opposite sign as the local depletion region charge $n_s = -N\ z_{dep}$ (charge neutrality) and creates a further change in V that we neglect. I this approximation, the bands have bent by a total amount of ΔV = V (0).

At the surface, the chemical potential[20] is in the surface band, since that band is partly filled for sufficiently low doping density; and the surface band energy and width depends on

[20] In thermodynamics, the chemical potential is a form of potential energy that can be absorbed or released during a chemical reaction, the chemical potential of a system of electrons at a temperature of zero Kelvin is known as the Fermi energy.

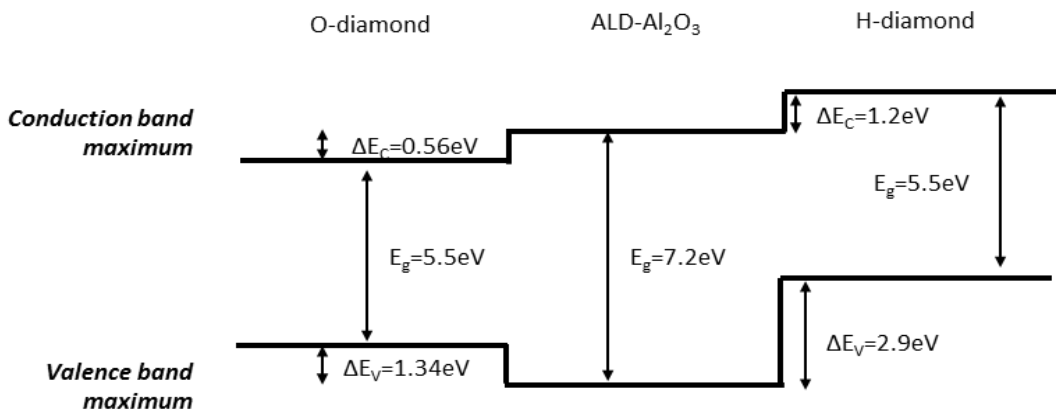

Figure 55: Theoretical band diagram in a diamond/ALD-Al_2O_3 interface in the case of an oxygen-terminated diamond surface and an hydrogen-terminated diamond surface.

material properties. In the bulk, the chemical potential is in the gap, usually closer to the conduction band (again, depending of the doping density). However, in equilibrium, the chemical potential has to be the same everywhere, and in particular needs to be the same at the surface and in the bulk. This condition therefore dictates the value of ΔV, i.e. the amount by which the bands need to bend, originating from the material dependent surface properties, and therefore determines the depletion depth z_{dep}

Fermi level pinning

To make an example, let's assume that the surface band is centered in the middle of the gap, with a width of a fraction of the gap size, and is half filled in the intrinsic material. Doping will fill the surface band slightly more. Let's take the case of diamond MOS structure #3, with a band gap of E_g = 5.45eV (**Table 1**), and a nominal doping of N = 10^{17}at/cm^{-3} = 10^{23}at/m^{-3} (here we use the value reported for #3, as described in II.1 Description of the samples, Metal-Oxide-diamond structures). Then, $\Delta V \approx E_g/2$, and with $\epsilon \approx 5.7$ (**Table 1**) and using:

$$z_{dep} = \sqrt{\frac{2\epsilon\epsilon_0 \Delta V}{e^2 N}} \qquad \textbf{Eq. 7}$$

It follows that $z_{dep} \approx 130$nm, we can compare this quantity with diamond lattice constant $a_0 = 0.35$nm[21]. This result in a surface charge of $n_s = N\, z_{dep} \approx 3.71 \cdot 10^{16} m^{-2}$, much smaller than the total surface density of states ($\approx 2/a^2_0 \approx 16.3 \cdot 10^{18} m^{-3}$)[22] with the previously presented lattice constant. Therefore, the chemical potential at the surface is essentially independent of the doping level (at least, for typical doping densities as above). One says that *the Fermi level is pinned at the surface*. Particularly considering that the surface atoms make up a very small fraction of the total number of atoms in the crystal, the role of the surface is quite important. Also, note that the depletion depth z_{dep} can be changed with the dopant density, as formulated in **Eq. 7**.

Spotlight on interface traps

When a voltage is applied, the Fermi level moves up or down with respect to the interface-trap levels and a change in the interface traps occurs. This change of charge affects the MOS capacitance and alters the ideal MOS curve. Capacitance measurements can be used to evaluate the interface-trap density, because the input capacitance of the equivalent circuit contains information about the interface traps (see **Figure 56**). The basic equivalent circuit incorporating the interface-trap effect is shown in **Figure 56** (a).

In **Figure 56**, C_i and C_D are the insulator and the semiconductor depletion-layer capacitance, respectively. C_{it} and R_{it} are the capacitance and resistance associated with the interface traps and, thus, are also functions of energy. The product $C_{it} \cdot R_{it}$ is defined as the interface-trap lifetime τ_{it}, which determines the frequency behavior of the interface traps. The parallel branch of the equivalent circuit in **Figure 56** (a) can be converted into a frequency-dependent capacitance C_p in parallel with a frequency dependent conductance G_p as shown in **Figure 58** (b) and according with the expressions:

$$C_p = C_D + \frac{C_{it}}{1 + \omega^2 \tau_{it}^2} \qquad \textbf{Eq. 8}$$

$$\frac{C_p}{\omega} = C_D + \frac{C_{it} \omega \tau_{it}}{1 + \omega^2 \tau_{it}^2} \qquad \textbf{Eq. 9}$$

[21] http://www.semiconductors.co.uk/propiviv5431.htm

[22] Further information about the total surface density of states can be found in literature: K. NG. Kwok S. M. Sze, Physics of semiconductor devices, 2nd ed. Wiley, New York (1981)

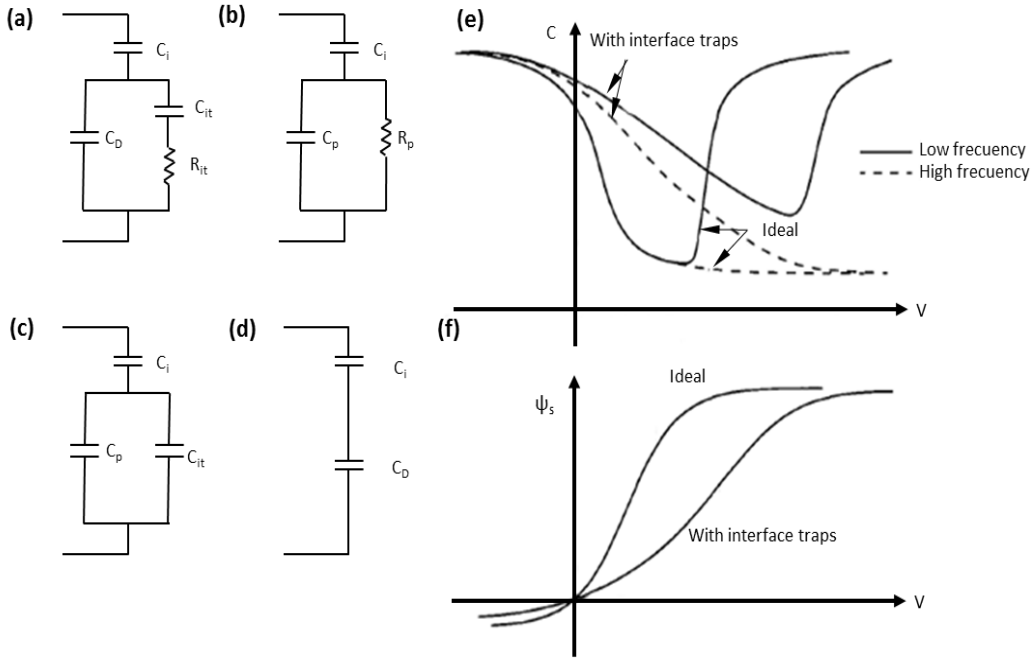

Figure 56: (a), (b) Equivalent circuits including interface-trap effects. (c) Low frequency limit. (d) High frequency limit. (e) and (f), influence of interface traps on high frequency and low frequency C-V curves in a p-type semiconductor.

Also of particular interest are the equivalent circuits in the low-frequency and high frequency limits included in **Figure 56** (c) and (d) (deduced from the previous equations). Physically, it means that the traps are not fast enough to respond to the fast signal. **Figure 56** (e) shows qualitatively the high-frequency and low-frequency C-V characteristics with and without interface traps.

A very noticeable effect on the interface traps is that the curves are stretched out in the voltage direction. This is due to the fact that extra charges has to fill the traps, so it takes more total charge or applied voltage to accomplish the same surface potential ψ_s (or band bending). This is demonstrated more clearly in **Figure 56** (f), where ψ_s is plotted against the applied voltage directly, with and without traps. This means that interface traps affects the total capacitance in two ways:

- Through the extra circuit elements C_{it} and R_{it}
- Indirectly, on C_D: for a fixed bias, since some charge will be needed to fill the interface traps, the remaining charge to be put in the depletion layer is reduced and this will reduce the surface potential or band bending. But since the relationship between C_D and ψ_s is fixed, changing ψ_s means changing C_D also.

IV.5 Oxide charges

Oxide-related charges, other than that of the interface traps, include the fixed oxide charge Q_f, the mobile ionic charge Q_m and the oxide-trapped charge Q_{ot}, as shown in **Figure 57**. In general, unlike interface-trapped charges, these oxide charges are independent of bias, so they cause parallel shift in the gate-bias direction.

The effect on the voltage shift is weighted according to the location of the charge, i.e., the closer to the oxide-semiconductor interface, the more shifts it will cause.

Positive charge is equivalent to an added positive gate bias for the semiconductor so it requires a more negative bias to achieve the same original semiconductor band bending. Notice that in the new flat band condition, the oxide field is no longer zero. The fixed oxide charges Q_f, has the following properties:

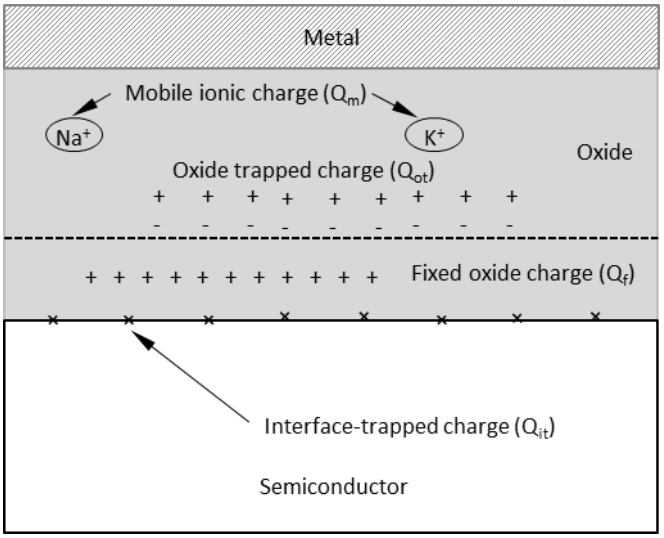

Figure 57: Terminology for charges associated with a standard thermally oxidized MOS structure.

- They are located very close to the oxide-semiconductor interface
- They are generally positive
- Their density is not greatly affected by the oxide thickness or by the type or concentration of impurities in semiconductor
- They depend on oxidation and annealing conditions
- They depend on semiconductor surface orientation

It can be regarded as a charge sheet located at the interface: $\Delta V_f = -Q_f/C_i$ Mobile ionic charges can move back and forth through the oxide layer, depending on biasing conditions, and thus rise to voltage shifts. The shift is usually enhanced at elevated temperatures.

Oxide trapped charge is associated with defects in the oxide. The oxide traps are usually initially neutral and are charged by introducing electrons and holes into the oxide layer. This can occur from any current passing through the oxide layer.

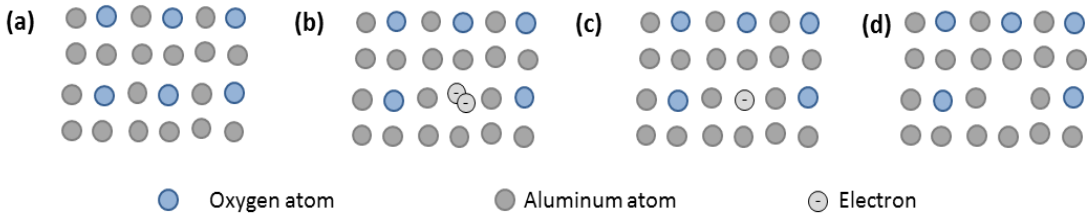

Figure 58: Oxygen vacancies in an Al_2O_3 oxide. (a) No oxygen vacancy, (b) V_O, (c) V_O^+ and (d) V_O^{++} vacancy types.

On the other hand, charged oxygen vacancies in Al_2O_3 oxide layer are usual. Indeed, different kinds of oxygen vacancies [108] can be produced (see **Figure 58**) when:

(b) V_O: Oxygen is removed from the Al_2O_3 lattice, 2 electrons remains.
(c) V_O^+: Oxygen is removed from the Al_2O_3 lattice, 1 electron remain.
(d) V_O^{++}: Oxygen is removed from the Al_2O_3 lattice, no electron remaining.

Concerning native point defects in Al_2O_3, it's generally believed that they have their full normal charges: V_O^{2+}, O_i^{2-}, V_{Al}^{3-}, Al_i^{3+}. On the other hand, defects in pure alumina can only form in charge neutral combinations as follow:

- Schottky (vacancies) and anti-Schottky (interstitials): 3 V_O^{2+} + 2 V_{Al}^{3-} and 2 Al_i^{3+} + 3 O_i^{2-}
- Cation Frenkel (Al^{3+} ions) and anion Frenkel (O^{2-} ions): V_{Al}^{3-} + Al_i^{3+} and V_O^{2+} + O_i^{2-}

Point defects [108] in alumina can diffuse particularly, oxygen vacancy diffusion has been investigated by other authors [109], resulting in three distinct classes of diffusion jumps. Charged oxygen vacancies in the oxide can be moved from its site to an adjacent one in a biased MOS structure [109], even in amorphous alumina [110], thus leading to oxide-charge related effects in the C-V curve.

TEM evidences of oxide charges

EELS measurements, carried out in the oxide layer of sample #4, reveal some differences in the oxygen distribution inside the oxide layer. Sample #4 presents a variety of diamond MOS capacitors, some of them were electrically characterized, while some others were not. This means that some MOS structures were "electrically strained", while some others remains "as deposited". For that, an EELS study of the oxygen distribution in the oxide layer depending on the "on duty" operation was considered of interest.

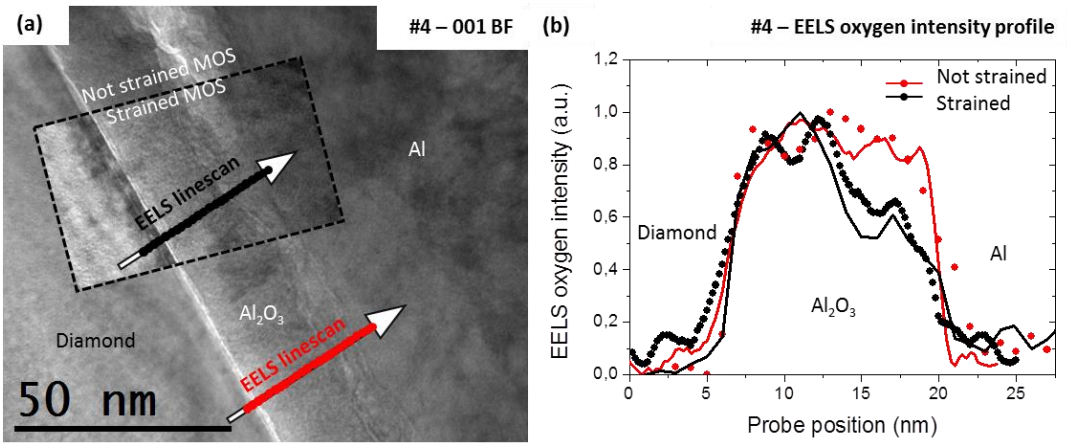

Figure 59: (a) 001-BF image of diamond MOS structures electrically strained (inset) and not strained. (b) EELS oxygen-intensity profiles measured across the oxide layer in strained (black line) and not strained (red line) diamond-MOS structures. Different oxygen distribution, depending on the electric strain, are evidenced.

Two #4 structures were studied: one before and one after the electrical characterization. The results are summarized in **Figure 59**. **Figure 591** (a) shows 001-BF image of both structures, white arrows are accompanied by red/black spots to highlight the points where EELS data were acquired. It can be observed that EELS oxygen-related signal is higher in the vicinity of the diamond interface in electrically characterized samples. On the other hand, MOS capacitors that were not electrically characterized are showing a more homogeneous oxygen distribution in the oxide layer. This was revealed by EELS profiling of the oxygen-related peak (O-K line, at 532 eV) over the oxide layer (see **Figure 61**(b)).

Note that oxygen-EELS intensity profiles presented on insets of **Figure 61**(b), were acquired by averaging several profiles over a 5nm interface. The previously described behavior is here tentatively attributed to oxide charges, which may be induced by oxygen migration. Such migration may lead to oxygen inhomogeneities in the oxide layer.

Electric evidences of oxide charges

In the previously described electrical behavior (see IV.2 Functional vs structural behavior of diamond-MOS structures [#3] & [#4]), an horizontal shift on the C(V) curve of both samples can be observed. Indeed, **Figure 47** (a) shows that flat band condition is modified (look at the 0V position of **Figure 47** (a)).

This is explained in terms of the presence of oxide charges, as schematically presented in **Figure 60**. **Figure 60** (a) shows the impact of positive charges in the oxide, horizontally displacing the shape of the related C(V) feature. **Figure 60** (b) shows an schematic view of

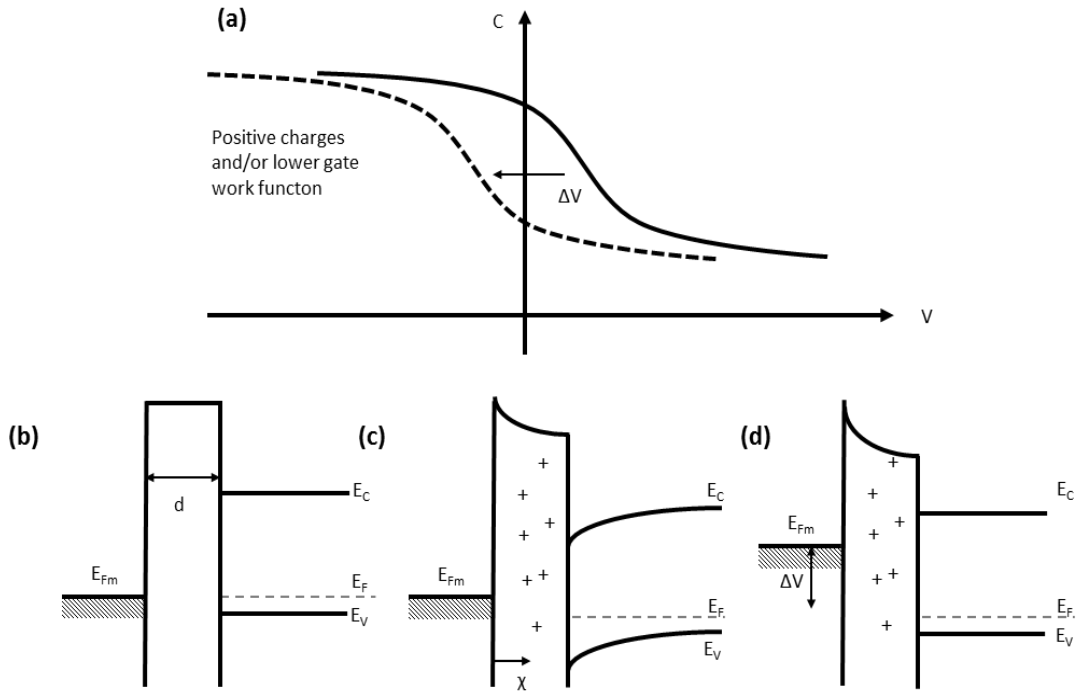

Figure 60: (a) High frequency C-V curve (p-type semiconductor) shifted along the voltage axis due to positive oxide chares. Band diagram at flat band (b), original, (c), with positive oxide charges and (d) new flat band bias.

the original flat band condition, once the structure is polarized (c) the new flat band condition remains as indicated in **Figure 60** (d).

IV.6 Conclusions

Taking into account the previously exposed phenomena, a variety of conclusions can be extracted:

- Shift in the C-V plot (see **Figure 47** (a)) can be explained by two factors:
  - In terms of oxide charges in the Al_2O_3 layer
  - Additionally, interface states also modify the shape of the C-V curve with respect to the ideal behavior.
- Oxygen distribution inside both oxide layers is not homogeneous. Even when the oxide thickness in #4 remains constant, a not homogeneous oxygen distribution inside the oxide layer can be observed. This can be due to the formation of oxygen

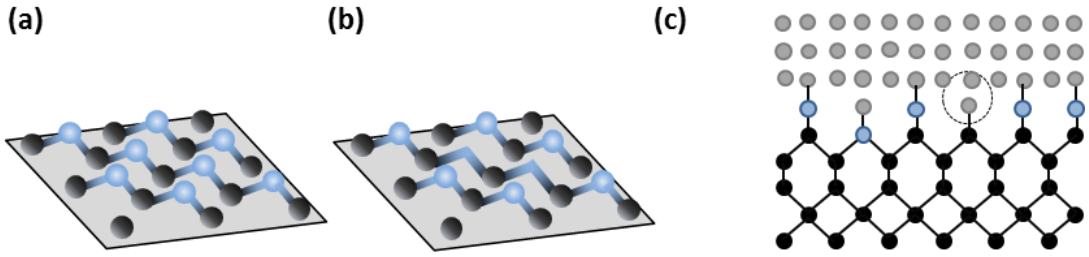

Figure 61: Diagram of the diamond surface after the VUV-ozone treatment (a) fully covered of oxygen and (b) with oxygen vacancies. (c) Direct diamond-oxide contact or "dangling bond", that leads to charges in the interface.

vacancies in the oxide, induced by the applied voltage. Additional measurements are required in order to verify this point.

- Thickness variations of the Al_2O_3 layer in #3 respect to #4 have been evidenced. Such variations could be related with the ALD process, and are shown to have a clear impact in the electric response of the related device.

These facts allow us to identify the real problems and, thus, to design more reliable structures in the future. As spotted, the main sources of the bad behavior of the diamond MOS structures are the oxide thickness variations, the interface states and the oxide charges. Concerning the interface states, diamond's covalent semiconductor surface is expected to have a high density of surface states or defects near the neutral level (which is expected to be about one-third of the bandgap from the valence-band edge). Indeed, the theoretical calculation by Pugh [111] for (111) diamond surfaces, gives a narrow band of surface states slightly below the center of the forbidden gap.

Such interface states are minimized when VUV-ozone treatment of the diamond surface is carried out. However, probably the oxygen atoms are not covering the whole diamond surface ("size" of the oxygen atoms makes it very difficult). This will lead to direct diamond-oxide contacts, which means surface charges (see **Figure 63**). Direct diamond-oxide contacts or "dangling bonds" leads to undesired charge carriers along the interface, modeled as interface states, which are not completely avoided after the ozone treatment.

Chapter V: Diamond δ-FETs

In the previous chapter, diamond-MOS structures were characterized in order to build reliable MOSFETs devices. However, diamond-based traditional MOSFET architecture presents the problem of the n-type doping of drain and source (needed to supply carriers to the active channel as well as for the manufacture of reliable p-n junctions [112, 113]). Additionally, diamond-oxide interface states still prohibit a good control of the field expansion in the diamond material. Nevertheless, despite the progress in n-type doping of diamond [30, 114, 115], n-type doping still carries some technological difficulties as growing in an specific CVD reactor or by implantation. C. Saguy et al. [116] demonstrated that [P-V] complexes are not broken even after high temperature annealing, explaining the difficulty of n-type doping by P ion implantation in diamond. Moreover, n-type diamond with phosphorous impurities leads to a very deep donor level (0.6eV below the band minimum [117]), so boron still remains as the most commonly employed dopant in diamond.

In this sense, p-type diamond is more easily obtained either by MPCVD growth or by using boron ion-implantation followed by annealing [118, 119]. Boron is known as an efficient dopant for diamond because of its 0.37eV acceptor level above the valence band. So, to achieve a Field Effect Transistor in diamond, δ-FET architecture seems to be an ideal first approach in which charge carriers (created in the δ -doped structure) can move through the diamond lattice without requiring n-type doping.

In this chapter, we will focus on the architecture of diamond δ-FETs as well as in our efforts to fabricate it, following the next index:

V.1 Introduction: Basic concepts and fundamentals behind a δ-FET architecture are introduced. Simulations of charge carrier confinement in δ -doped diamond structures, carried out by various authors in literature, are also presented and discussed.

- **Charge carrier confinement**

V.2 Boron concentration profiling: For the manufacturing of reliable δ-doped diamond devices, an accurate control of the doping process is needed, together with specific methods for the characterization (both in terms of doping level and localization of boron acceptors). Here, an STEM-based methodology is developed to quantify the boron distribution in diamond δ -doped structures.

- **Experimental details**
- **Z-contrast for boron profiling of δ-doped layers (STEM-HAADF)**
- **HAADF corrected profiles**

V.3 Diffraction contrast for boron doping profiling of δ-doped layers by TEM : An accurate characterization of the thickness and doping of the δ -layer is mandatory, in order to reach an optimum configuration of the device.

- **Experimental details**
- **Contrast in TEM**
- **Methodology**
- **δ-FET characterization (#9**)

V.4 Diamond δ-FET [#9]: The configuration of the samples used in this work to fabricate δ-FETs is described. The previously presented structures were electronically and TEM-characterized, main results are summarized here.

- **δ-doped diamond FETS**
- **MOSFET electrical properties**

V.5 Conclusions: Final consideration about the several attempts of fabricating operative diamond-based δ-FET devices

- **Conclusions on δ-layers characterization**
- **δ-FET fabrication**
- **General conclusions**

V.1 Introduction

Doping distributions with high peak concentrations and narrow distribution widths are advantageous for many device applications. A δ-like function in doping distributions minimizes potential fluctuations originated from random doping atom distributions,

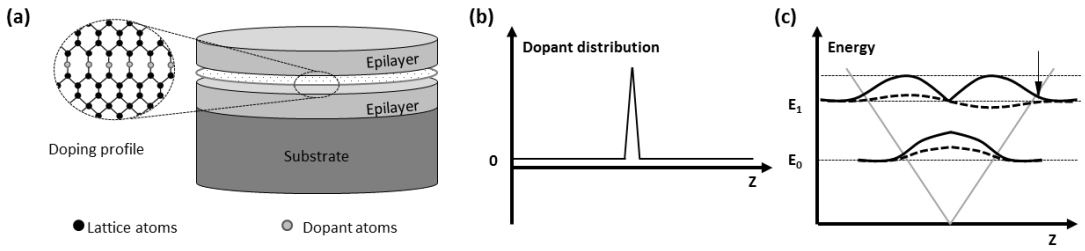

Figure 62: (a) Schematic illustration of a semiconductor substrate and an epitaxial film containing a δ-doped layer. A schematic lattice with the impurity atoms being confined to a single atomic plane is also shown. (b) Delta-like function doping distribution and (c) V-shaped potential well (grey line) created by a δ-function-like charge distribution. Also shown are the energy levels (black-dashed line), wavefunctions (dashed, thick black line) and squared wavefunctions (squared modulus of the wavefunction means probability density of measuring a particle, thick black line) of a quantized free-carrier system in a V-shaped well. Dark arrow is used to highlight that probability of presence of charge carriers outside of the V-shaped potential is not zero.

resulting in a significant improvement of the optical properties of doping supperlatices. Quantum confined interband transitions have been widely observed in absorption measurements and luminescence emission experiments [120].

The free-carrier distribution in semiconductors depends on the distribution of ionized impurities. The free-carrier distribution is instrumental for many properties of semiconductors, including recombination and transport properties. In semiconductors with "smooth" changes of doping concentration, the free-carrier profile follows the doping profile with a good approximation.

However, in δ-doped semiconductors which exhibit abrupt doping concentration variations along short distances, the free-carrier distribution is spread out much further than the doping distribution in the quantum-mechanical picture. These δ-like distribution is modelled by the Dirac δ-function, δ(z), which is a mathematical distribution whose width is infinitely narrow. The magnitude of δ(z) is zero for $z \neq 0$ and infinite for $z = 0$. The integral of the function has a value of unity. The employment of the δ(z) for semiconductor doping profiles implies that the width of the one-dimensional profile is much narrower than all other relevant length scales.

These relevant length scales includes the screening length, the free-carrier diffusion length and the De Broglie's wavelength of a quantized carrier system. In the ideal situation, this implies a very thin doped layer (one atomic layer in the lattice), as schematically shown in **Figure 62** (a). **Figure 62** also shows a simplified δ-like distribution (b), whose simplified V-shaped potential is presented in (c) by using grey line.

Strictly speaking, the use of the δ(z) function for any real physical quantity is problematic. Thus, the Gaussian function can be alternatively used to describe very narrow 1D doping

distributions. Mathematically, the simplest way to model this distribution is to define a 2D dopant distribution (assuming that the dopant distribution depends on the z coordinate only): $N_D(z)$, that can be a δ-like or a Gaussian-like function.

Next is to assume that all dopants are ionized (which is not entirely correct at room temperature, as k_BT=0.0257eV and E_B=0.370eV [121, 122] at T = 300K). Then, the electrostatic potential created by the dopants can be calculated using the Poisson's equation:

$$\nabla^2 V = \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right) V(x,y,z) = \frac{\rho(x,y,z)}{\varepsilon} \qquad \textbf{Eq. 10}$$

where ∇^2 is the Laplace operator in the Euclidean space, V(x,y,z) is the potential function, ρ(x,y,z) is the spatial distribution of the dopants and ε the electrostatic permittivity. In a rigorous calculation of the free-carrier distribution in δ-doped semiconductors, size-quantization of the electron gas must be taken into account; that is, the Schrödinger and Poisson equations must be solved simultaneously. Ideally, the free-carrier density equals the ionized dopant concentration. The contribution of the free carriers to band-bending cannot be neglected and the potential well will not be strictly V-shaped. Whereas still V-shaped in the vicinity of the notch of the potential, the band edges become flat (horizontal) when far enough from the doping sheet. The entire dopant-free-carrier system is neutral and, as a consequence, the band edges are flat at large distances from the dopant sheet.

A self-consistent solution of the spatial and energetic structures of δ-doped semiconductors requires simultaneous solutions of the Schrödinger's and Poisson's equations. The solution is usually obtained in an iterative way. Initially a "reasonable" free-carrier distribution is assumed, from which, using Poisson's equation, a potential is deduced. A new set of wavefunctions is calculated from the potential using the Schrödinger's equation. A second iteration of the potential is then calculated using the new free-carrier distribution. This procedure is continued until calculation converges, that is, wavefunctions and potential do not change with further iterations. Further information on efficient solutions of the Schrödinger-Poisson equations in semiconductor device simulations can be found in literature [123].

Thick black line in **Figure 62** (c) shows that wavefunction amplitude is not zero outside of the V-shaped potential (see dark arrow). In Born's statistical interpretation, the squared modulus of the wave function, $|\psi|^2$, is a real number interpreted as the probability density of measuring a particle's being detected at a given place, or having a given momentum, at a given time, and possibly having definite values for discrete degrees of freedom. So, this waveform extension means that there is a probability of having charge-carriers outside of the δ layer; these are known as "delocalized carriers".

Charge carrier confinement

The striking diamond properties highlighted in the first chapter should allow developing new electric switches with low losses. FET channel conductance needs a certain carrier confinement obtained either by a surface band binding (MOSFETs) or a quantum well (MODFETs). Here, this effect is carried out by the incorporation of δ-doped layers.

To improve switching velocity, high carrier mobilities are required, which is impossible in highly doped material [124]. Thus, a δ-doped configuration allows, on one hand, to have carriers and on the other one, to get them partially out of the doped region, allowing higher mobilities.

However, because of the high energy of the p-type dopant (boron), the equilibrium carrier concentration is low at room temperature and the on-state resistivity is very high. This activation energy decreases with the doping level, but this trend is accompanied with a decrease in the hole mobility in the bulk crystal.

One way to overcome this difficulty is to create free holes in a certain location of the device (the δ-layer) and to delocalize the charge carriers in order to allow current flow in a channel with a low ionized impurity concentration. This delocalization is induced by quantum confinement of a very thin δ layer (as previously explained).

Then a bias on a gate on the surface parallel to the 2D hole gas will allow to cast out carriers (by modulating the delocalization), and more important, to switch the FET in ‘‘on’’ or ‘‘off’’ state. A diamond field effect transistor (FET) based on this δ-doping combines high speed commutation and low “on” resistance. The critical parameters to get such 2D hole gas in diamond, in particular the doping level and the δ-layer thickness, were reported by Fiori et al. [56].

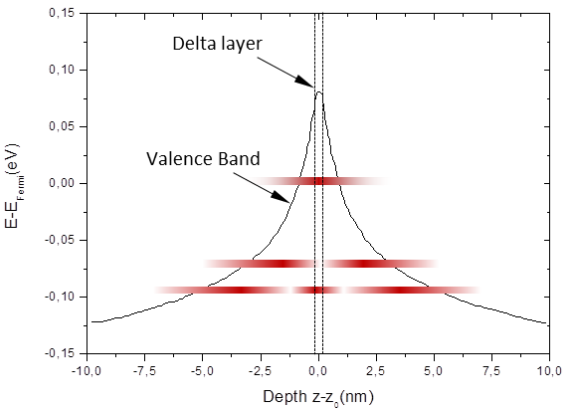

Figure 63: Heavy holes probability density (colored) for δ=0.36nm ($[B]_\delta=5\cdot10^{20}$ cm^{-3}) in an infinite diamond structure (ground state and four excited states only). The vertical position of the energy level indicates its energy relative to the Fermi level, the horizontal position its spatial extension, and the color contrast its probability density.

In the case of an infinite structure (it means, a sufficiently large distance between the δ layer and the surface), the delta layer lies on a symmetry axis. This symmetry acts on the valence band and on the presence probability density of

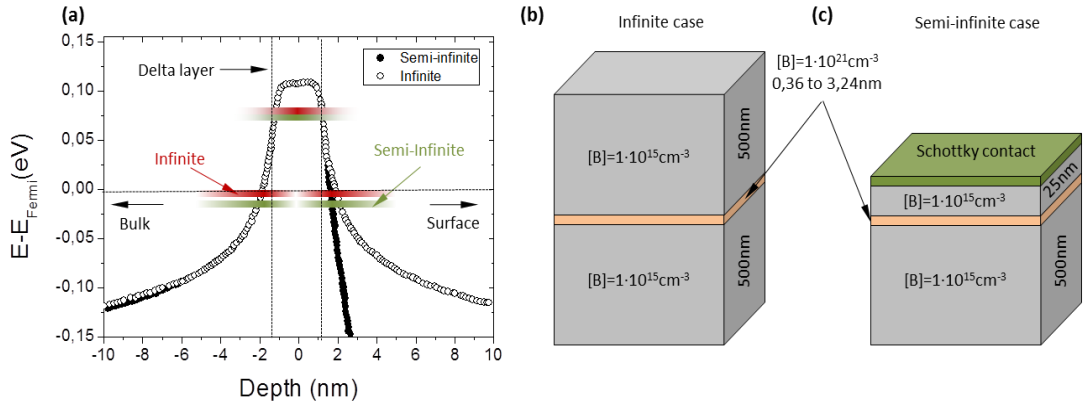

Figure 64: (a) Heavy holes probability density for δ=2.52nm in an infinite (red) and semi-infinite (green) diamond. Peaks of heavy holes probability density are localized by wide arrows. Only the ground state and first excited state are represented to simplify the drawing. Schematic of the delta-boron-doped diamond stacks used in the calculations by Fiori et al. (b) and (c).

holes, as shown in **Figure 63**. Such spread carrier distribution is shown in **Figure 63**, where red color intensity variation is used to illustrate the charge carrier distribution in a diamond δ-layer [56].

In the semi-infinite diamond structure (**Figure 64**), a Schottky barrier (here located at 25nm from the delta layer) reproduces the effect of a gate on the diamond surface, as in the case of a FET. The Schottky contact induces a slight shift of wave-functions towards the bulk of the device; this spatial shift was accompanied by an energy shift toward lower energies. The latter is more deterious, as it will reduce the occupation density at a constant temperature. The fraction of delocalized holes was reduced by 3% (in this case of δ=2,5nm [56]).

The calculations of the effect of quantum confinement of holes in diamond carried out by Fiori et al. [56] indicates that a 3nm-thick delta-layer would induce the delocalization of 30% of the free holes outside of the doped region. For a 1nm-thick delta-layer, around 60% of holes are delocalized, meaning that the doping level is high enough to ensure metallic conductivity.

The difference between the case of a delta-layer deeply buried into the diamond, and a delta-layer neat a Schottky barrier at the surface is a small reduction of the fraction of delocalized holes (conductivity should also be wakened). This study establish a value of 2-3nm thick for the delta layer in diamond.

V.2 Boron concentration profiling (#5 & #6)

For the fabrication of reliable δ-doped diamond devices, an accurate control of doping level and thickness is needed, together with specific characterization methods (both in terms of doping level and localization of boron acceptors). Although early secondary ion mass spectroscopy (SIMS) profiles did not meet such requirements [18], recently, Elastic Recoil Detection profiles have shown that the values obtained by SIMS could be measured over a wide area [125], probably due to beam-related effects.

The large dynamical doping range is a key advantage of SIMS to characterize δ-doped layers; in turn it presents two important limitations [126]:

- To avoid ion mixing inside diamond crystal during SIMS operation, a complicated DRF (depth resolution function) deconvolution analysis is required, which strongly depends on the species at stake.
- The probed region extension averaged the deduced boron related profile.

Doping level evaluation over micrometer-scale can also be carried out by optical methods as Raman and FTIR. Among these techniques, cathodoluminescence is clearly the most sensitive [106] while ensuring a high spatial resolution since cross sectional analysis can be also carried out on FIB preparations. However, the signal is too weak in heavily doped diamond to image the spatial distribution of dopants. The need of an imaging method able to quantify boron content and layer thickness becomes obvious when δ-doped devices are being developed. For this reason, high angle annular dark field (HAADF [127] or Z-contrast mode) in STEM mode is here applied to thin homoepitaxial multilayers in order to determine the thickness, interface sharpness, and boron content of these doped structures. Recently, boron doping was also observed using this technique(with different methodology) on nanocrystalline diamond [128].

Here, a modified method is applied to the case of boron δ-doped layers in order to avoid FIB-lamella thickness effects. Comparison to SIMS experimental profile has demonstrated the power of the method and showed that such layers are now close to reach the requirements for carrier delocalization, as theoretically demonstrated in [56].

Experimental details

Two samples were studied: one multilayer stacks including four thin (nominally 20–60 nm thick) and highly boron doped homoepitaxial diamond layers (labelled sample #5) to first show the method, and another one including only one boron δ-doped layer (labelled sample

#6) to evidence the ultimate doping level and thickness that can be reached. The samples have been grown by MPCVD in a vertical silica tube reactor as described elsewhere [63] on a (100)-oriented HPHT type Ib diamond substrate. After a 2 h cleaning with pure hydrogen plasma at 880ºC, undoped (p^-) and heavily boron-doped (p^{++}) epilayers have been grown alternatively from respectively $H_2/He/CH_4/O_2$ and $H_2/He/CH_4/B_2H_6$ gas mixtures without turning off the plasma. For the purpose of this study, the p^{++} epilayers of sample A have been labelled from L1 to L4 according to the growth sequence (that is, from substrate to surface).

After the growth of each heavily p^{++} layer, a specific etch-back procedure was performed during 3 min (L2), 6min (L3), and 10 min (L4) using a mixture of H_2 and O_2 in the plasma. The HAADF-STEM experiment was carried out in a Jeol 2010F microscope equipped with an annular dark field (ADF) detector. To ensure high angle detection (HAADF), the camera length was fixed at 8 cm leading to minimum so that maximum detector collection angles of 38.5 mrad and 99.8 mrad, corresponding to spatial frequencies *s* around 4 and 1.5$Å^{-1}$, respectively, are reached. The detector should be sensitive only above a s_{min}=1.55$Å^{-1}$ threshold to avoid Bragg scattering effects. Because diamond is the hardest known material, specimen preparation for cross-section TEM observation was undertaken using a Focused Ion Beam in a Dual Beam Scanning electron microscope (FIB-Dual Beam, lift-off method).

Z-contrast for boron profiling of δ-doped layers (STEM-HAADF)

The use of the Z-contrast or HAADF-STEM mode is well known to allow atomic resolution [129]. For example, individual atoms at interfaces as isolated boron atoms in carbon nanostructures or concentration profiles in nanostructures have been demonstrated [130]. So far, the method has yielded either concentrations in the alloying range or individual atoms identification at atomic resolution, but seemed insufficiently sensitive for doping level determination in Si or III-V compounds. The low Z-number of carbon and the difference between the scattering cross sections of C and B at higher angles (which depends on Z^2 [131] and is about 30% at 100 mrad in our setup) makes possible detecting and imaging boron in the heavy doping range as shown in the following. Moreover such layers are visible by diffraction contrast or even in bright field condition with some slight defocus, but boron quantification is then very difficult.

Figure 65 (a) shows a HAADF-STEM micrograph with the four heavily boron doped p^{++} layers embedded in an undoped (p^-) diamond layer. The darker tone at the right hand of the micrograph is due to a gradual reduction in thickness of the FIB lamella preparation, which is more pronounced close to the right-hand side (surface). The convolution of thickness and chemical effects is well revealed in the intensity profile of **Figure 65** (b), recorded along the

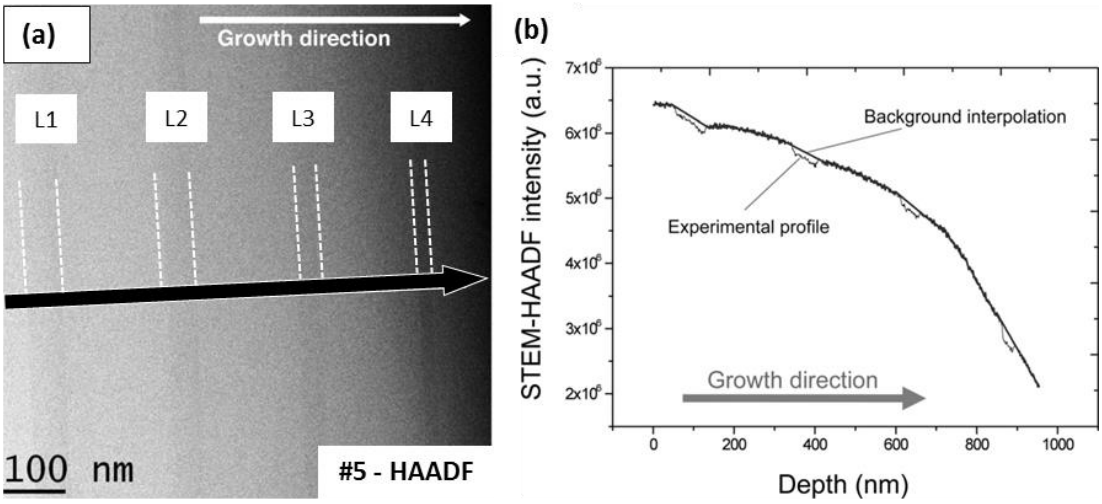

Figure 65: Sample #5 results: (a) HAADF-STEM micrograph recorded on four δ-doped layers. White, dashed lines are used to guide the eyes along the different boron doped diamond layers (b) Intensity profile recorded along the line indicated in the micrograph (black line) and the interpolation without taking into account the δ -doped layers (bold curve). Difference between experimental values and interpolated ones allow avoiding the lamella TEM preparation thickness effects. To reduce signal-noise, an average of 100 profiles was carried out over the width of the line.

10 nm-wide line indicated on the micrograph. To separate both effects and to analyze only the chemical concentration-related variation of the HAADF-STEM current intensity I^{HAADF}, an interpolation was performed using the data obtained only on the undoped region (in bold, i.e., taking off data of the heavily doped layers), and thus the ratio of the $I^{HAADF}(x)$ and $I^{HAADF}(0)$ where x is the boron content (i.e., current measured on the doped region and the corresponding current obtained by interpolation at the same position respectively) could be calculated at each position along the experimental profile.

Then, at one specified position, the intensity difference between the doped (experimental value: $I^{HAADF}(x)$) and undoped (interpolated value: $I^{HAADF}(0)$) material was deduced independent of the sample preparation thickness, allowing determine the boron doping, thanks to the following simple modelization of I^{HAADF}.

According to the wave behavior of keV electrons across a thin solid lamella, the ratio of scattered electrons depends on the square of the atomic scattering factor. In addition, interaction with phonons reduces the coherent intensity, and incoherent electrons are diffracted at high angles. Low angle scattering is dominated by elastic scattering as it results from Bragg reflections in the crystal, "Bragg scattering (BS)", while high angle scattering is dominated by inelastic scattering, i.e., incoherent scattering, which gives diffuse intensity distribution, "thermal diffuse scattering (TDS)". Thus at sufficiently high angles there are no diffraction effects, and the scattered intensity depends directly on the square of the

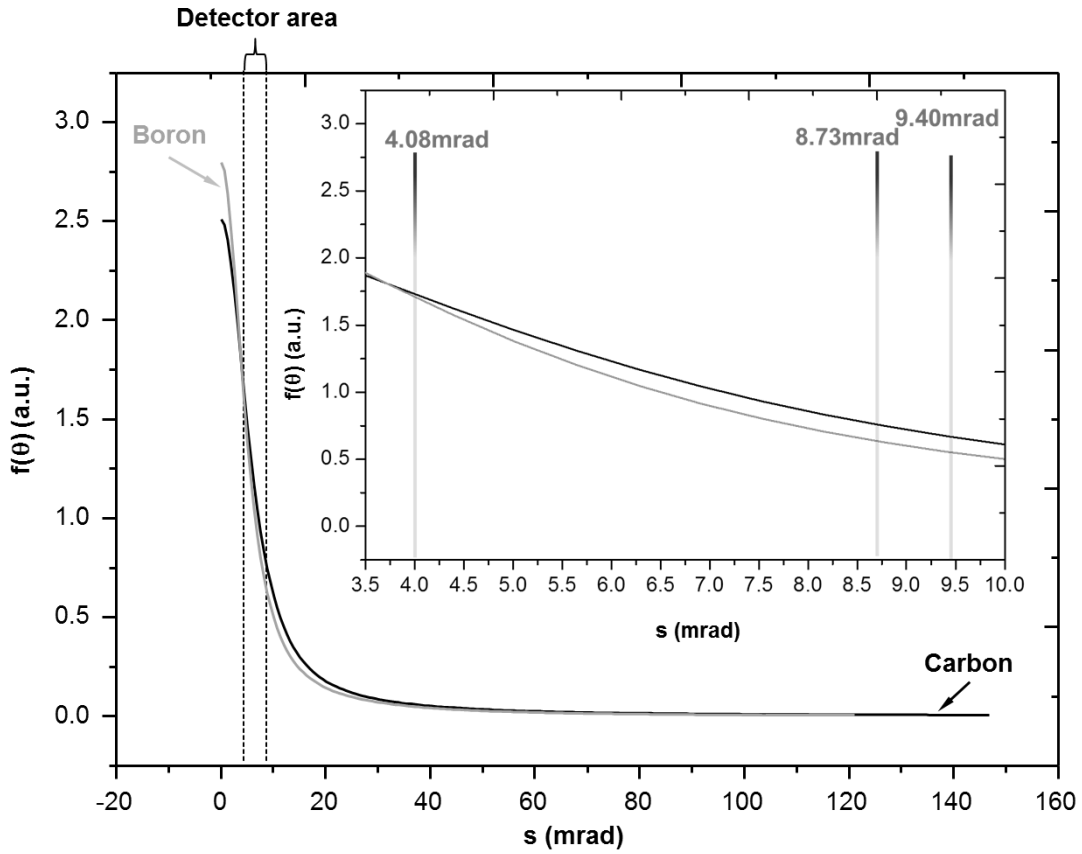

Figure 66: Atomic scattering factors for Carbon and Boron atoms, as a function of the collection semiangle. Inset shows intensity values for collecting semiangles corresponding to g = 111, g =220 and g = 004 at 120keV

atomic scattering factor, *f(θ)*, which gives the amplitude of the electron wave after scattering on one isolated atom. Then, the angular dependence of the electron emission is presented in **Figure 66**, and writes:

$$I^{HAADF}(s) = I_0\left[\sum_i |f_i(s)|^2\right] = I_0\left[\sum_{carbon} |f_{carbon}(s)|^2 + \sum_{boron} |f_{boron}(s)|^2\right] \qquad \textbf{Eq. 11}$$

where I_0 is the incident electron beam intensity, $f_i(s)$ is the atomic scattering factor for the atom i that depends on the scattering angle θ (=s/2) and have units of Å. For one species (i.e., sub index "carbon" or "boron" in **Eq. 11**), using the atomic scattering factor published by Kirkland [132] and integrating over the detector area in the reciprocal space (spatial frequencies *s*, units of $Å^{-1}$).

$$I_i^{HAADF} = \int_{s_{min,detector}}^{s_{max,detector}} [I_i^{HAADF}(s)]ds = I_0 N \sum_{s_{min,detector}}^{s_{max,detector}} f_{i,Kirkland}(s)^2 2\pi s \Delta s = D_i I_0 N \quad \textbf{Eq. 12}$$

where N is the number of atoms irradiated by the incident electron beam. The dependence of $f_{i,Kirkland}(s)$ over the range of the detector angle detection can be directly deduced from the values published by Kirkland [132] for either boron or carbon. In the case of the present experimental collection geometry, the calculation of sums labelled D_i in **Eq. 12** yielded for diamond and boron, values of D_{carbon}=0.214 and D_{boron}=0.0153. This corresponds to the probability for one incident electron to be scattered in the direction of the annular detector when scattering occurs either by a carbon or boron atom respectively.

Considering that here a boron doped layer is observed, the electronic current scattered in the direction of the annular detector by a doped layer (I_x^{HAADF}, with x the boron content) is:

$$I_x^{HAADF}(s) = I_0 N[(1-x)D_{carbon} + xD_{boron}] \quad \textbf{Eq. 13}$$

With *x* being the atomic proportion of boron in the diamond crystal. As the e-beam spot has a Gaussian shape, in addition to have a not easily measurable current, it is difficult to determine precisely I_0N (tentatively a value around 10^4 nA was estimated). To deduce *x*, the ratio, *R*, between the current in the doped and undoped regions is evaluated:

$$R = \frac{I_x^{HAADF}}{I_0^{HAADF}} = (1-x) + \frac{D_{boron}}{D_{carbon}} x \quad \textbf{Eq. 14}$$

Then, the relative boron content writes as:

$$x = \frac{1-R}{1-\frac{D_{boron}}{D_{carbon}}} = \frac{1-R_{measured}}{1-\frac{D_{boron}}{D_{carbon}}} C \quad \textbf{Eq. 15}$$

Therefore, the boron content can be determined by the ratio of electrons collected by the detector coming from doped and undoped regions. However, the factor R corresponds to the ratio of the electron currents scattered onto the detector and not on the current delivered by the detector ($R_{measured}$). In order to take into account this response, an experimental calibration of the used equipment has been carried out using a thick (4µm) diamond homoepitaxial single layer, with a well-known doping level (obtained from a previous calibrated SIMS measurements [127]) at different thicknesses (controlled by the FIB related sample preparation) and different condenser apertures to vary the electron beam current.

Brightness and contrast controls were kept at a fixed value (0 and 9, respectively) so that the correction factor C could be estimated for these experimental conditions.

HAADF corrected profiles (#5 & #6)

Figure 69 shows the result of applying **Eq. 15** with this correction factor at each point of the profile shown in **Figure 67** (b). The resulting doping profile indicates that boron is incorporated more easily close to undoped interfaces (see arrows). Since no extended defects could be detected by TEM on this preparation, this feature is tentatively attributed to the lattice strain gradient by the incorporation of boron. Indeed, a lattice expansion around 0.1% has been measured for a boron doping level of $10^{21}cm^{-3}$ [133].

As the observed noise was in the range of $10^{20}cm^{-3}$, the dynamical range was limited to about one order of magnitude, so that the trend to obtain sharper interfaces upon longer etch-back steps [63], although qualitatively confirmed, could not be interfered quantitatively from data shown in **Figure 67**.

A more detailed comparison of the HAADF boron concentration profile of layers to SIMS profiles of the same sample confirmed the relevance of this (independent) calibration procedure for absolute concentrations, the agreement between SIMS and HAADF values being rather striking as shown in the inset for layer L1. Some local variations are revealed by the HAADF-STEM while SIMS averages the profile.

Another result was that the typical exponential profiles observed by SIMS over various orders of magnitude at the interfaces of the multilayer under study were probably an artefact, resulting from the ion-mixing generally involved in SIMS measurements [134], leading

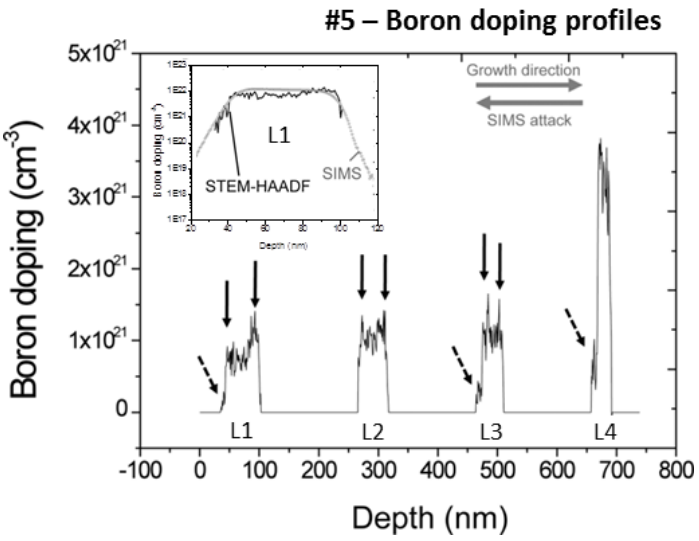

Figure 67: #5 doping profile derived from **Eq. 15** using the ratio between the measured and interpolated HAADF-STEM intensity along the experimental profile of **Figure 63** (b). In the inset, comparison between the SIMS and HAADF-STEM profiles on layer L1 is represented. Note that the boron scale is logarithmic to show the sensitivity of SIMS.

to systematic overestimation of the real width.

If this is the case, it is legitimate to ask how the layer thickness should be estimated from broadened SIMS profiles. Based on the comparison between the SIMS and HAADF-STEM profiles of several epilayers within various samples, the use of the extrema of the first derivative of the SIMS profile with respect to depth gives the layer thickness: the distance between these two extrema is usually within a few % of the thickness of the heavily doped epilayer as determined by HAADF-STEM.

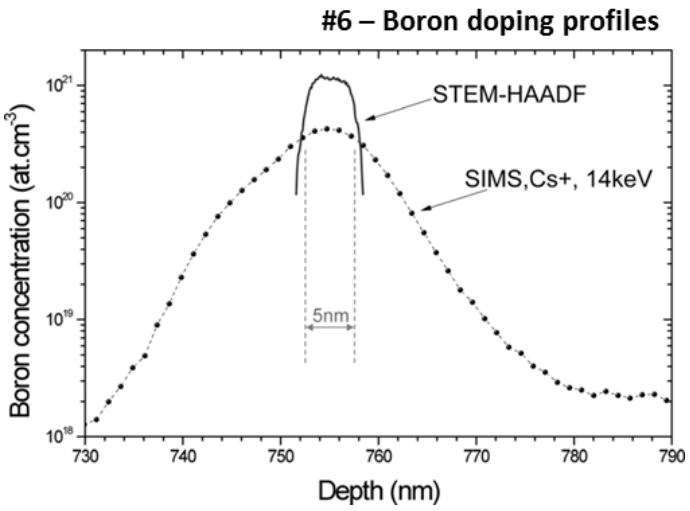

Figure 68: Boron profiles in logarithmic scale obtained from SIMS and HAADF-STEM techniques on sample #6. Ion-mixing is shown to broaden the SIMS profile. A 5 nm thick δ-doped layer is demonstrated by the HAADF-STEM profile.

The fact that the latter profiles do not show any systematic broadening on one of the sides of the doped epilayers pointed to another probable consequence of ion mixing: the ubiquitous enhancement of the width of the interface analyzed after sputtering the p^{++} region, which is apparent in most of the published SIMS profiles, is independent of how the samples were grown or whether the plasma was interrupted or not.

To illustrate the difference between both techniques on a very thin doped layer, HAADF-STEM and SIMS profiles are compared in **Figure 68** on a δ-doped layer (sample #6).

Integration over a wider line allowed reducing the HAADF-STEM noise with respect to that in **Figure 67**. A logarithmic scale is used to show the high sensitivity of the SIMS, but, in contrast, ion-mixing is shown to broaden the recorded boron profile. Note that for thicker layers (L1, L2 and L3 layers in sample #5) the difference is not so critical in contrast to thinner layers (L4 in #5 and δ-layer of sample #6).

Such behavior motivated other authors to use complementary techniques to improve the SIMS profile; Chicot et al.[135] calculated this broadening to correct the experimental data while Balmer et al. [136] complete the SIMS data with elastic recoil detection analysis (ERDA) to estimate boron-doping thickness.

Here, as a first result, a 5 nm-thick layer is demonstrated directly by the HAADF-STEM profile, showing that the growth technology is now close to reach quantum confinement enhancement of mobility.

V.3 Diffraction contrast for boron doping profiling of δ-doped layers by TEM (#7, #8 & #9)

Here, a methodology proposed by M. P. Alegre et al. [137] is used to evaluate the boron content in boron doped diamond layers. This iterative and auto-consistent methodology for the doping quantification of highly boron-doped diamond layers will consider two reflections "g", and the dependency of the TEM contrast with the effective thickness of the sample.

For this, the intensity quotient, attenuated by a factor s_{eff} will be evaluated among highly doped layers (p^{++}) and low doped layers (p^{-}). We will use dark field (DF) imaging in g= 004 and g = 220 reflections on a FIB-prepared sample, which experimental thickness will be previously evaluated via SEM. The acquisition of the TEM imaging was carried out in a variety of TEM microscopes: JEOL 1200EX and JEOL 2100 LaB_6, operating at 120 and 200keV, respectively.

Experimental details

Three samples were studied: #7, a multilayer stacks including four "thick" boron doped layers; #8, single, thin boron doped diamond layer structure and #9, containing a δ-layer with ultimate thickness (expected to be suitable for developing FET devices). The characteristics of the growing procedure of samples #7, #8 and #9 were described in II.1 Description of the samples.

Contrast in TEM

In conventional TEM (CTEM) using diffraction contrast mode, the registered intensity for a given reflection with Miller index "hkl" [131] is:

$$I_{hkl} = A(t)B\left(\frac{\pi t}{\xi_{hkl}}\right)^2 \frac{sin^2(\pi t s_{eff})}{(\pi t s_{eff})^2} \qquad \textbf{Eq. 16}$$

where *t* is the sample thickness, A(t) is a function used to track the attenuation of the wave intensity with the thickness variations (see **Figure 69**), B is a constant which depends on the detector gain, ξ_{hkl} the extinction distance and s_{eff} the effective excitation deviation, defined as:

$$s_{eff} = \sqrt{s^2 + \frac{1}{\xi_{hkl}^2}} \qquad \textbf{Eq. 17}$$

Where s is the deviation parameter (measured with respect to the Bragg conditions), ξ_{hkl} is the extinction distance for a given reflection and for a given doping (see **Figure 71**), defined in our system as:

$$\xi_{hkl} = \frac{\pi V_C \cos(\theta_{bragg})}{\lambda F(\theta_{hkl})} \qquad \textbf{Eq. 18}$$

V_C is the unit cell volume in the studied system, θ_{Bragg} is the Bragg angle, λ is the wavelength of the electron beam ($\lambda=3.35\cdot10^{-12}$m for a 120keV beam) and $F(\theta_{hkl})$ is the structure factor of the system for a given reflection (main contribution to the compositional sensibility in dark field images obtained in high boron doped diamond).

Methodology

A FIB-prepared sample (350±20nm thick, determined by SEM) was obtained from a multilayer structure whose boron content reaches levels close to the 0.01% atomic percent. Once the FIB lamella is obtained, TEM micrographies are carried out in the conventional CTEM mode.

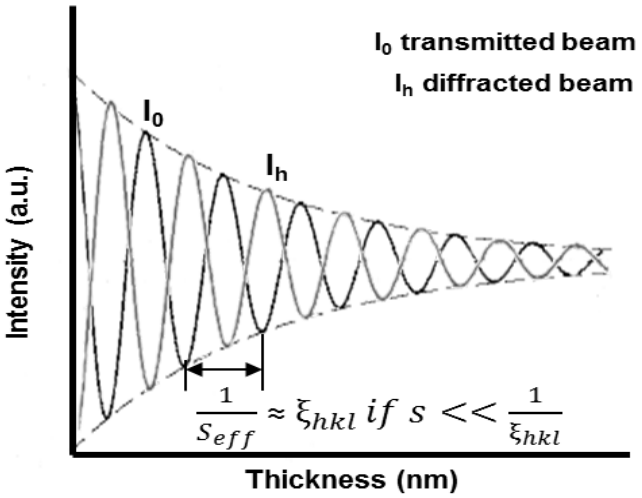

Figure 67: Dependency of the transmitted and diffracted beams (in two-beam conditions) with respect to the thickness of a crystal with an specific absorption coefficient and for a given reflection.

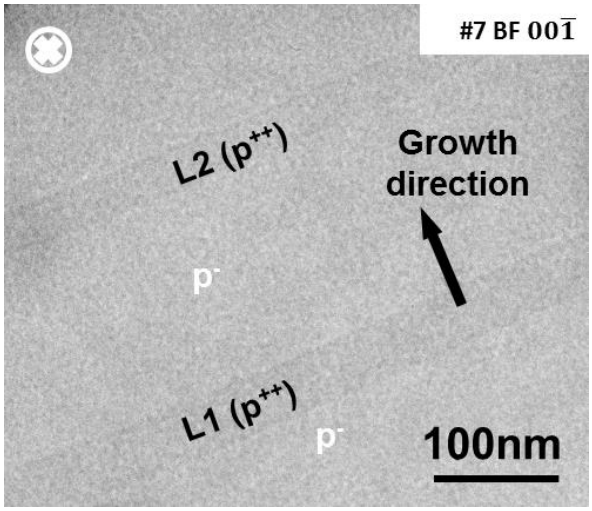

Figure 68: Bright field micrography of the multilayer structure of #7. A slight variation in the contrast of both boron doped layers is observed.

In the zone axis [00$\bar{1}$], BF mode, the previously cited sample reveals a slight difference between layers L1 and L2 (see **Figure 70**). An exhaustive analysis makes evident a layer thickness of 48±5nm for L2 and 60±5 for layer L1 (deviation evaluated over the CTEM micrography).

The different contrast between highly doped regions vs low doped regions depends on the chemical composition of the system (it means: the boron doping level).

However, to carry out an accurate evaluation of the boron content, it's not enough with evaluating the difference between a high doped region and a low doped region by BF. We will take into account (i) DF conditions, (ii) two different reflections, (iii) the thickness dependency (see **Figure 69**) and (iv) the influence of the S_{eff} parameter. Taking this into account, we carry out a DF study on the L2 layer.

Micrographies of the two considered reflections (g = 004 and G = 220) are compared, an inversion of the associated contrast is appreciated. The p^{++} area presents a clear contrast in g = 004, while it becomes a dark contrast in g = 220. With respect to the low-doped regions

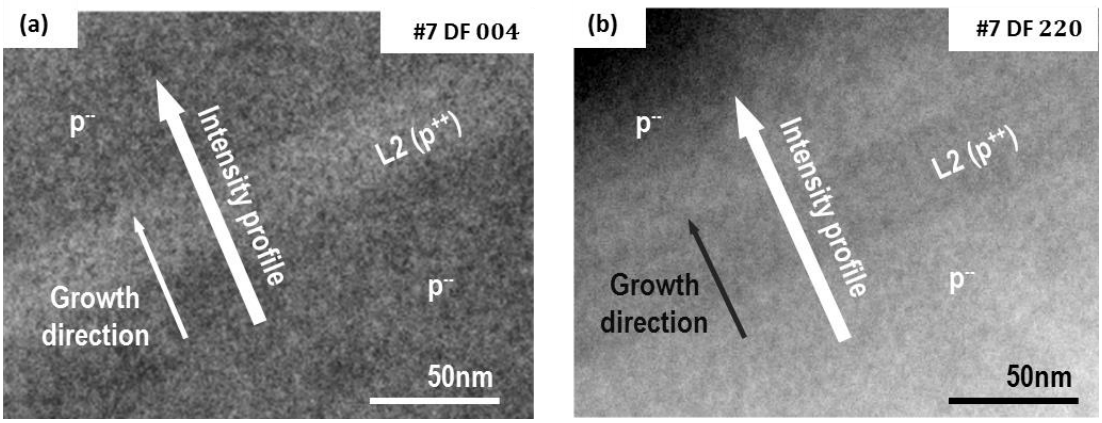

Figure 69: DF micrographies of L2 in (a) g = 004 and (b) g = 220 reflections. Both images were acquired with the same optimized conditions of bright-contrast which guaranties a lineal behavior.

(p^{-}), a reverse behavior is revealed: dark contrast on the first reflection and clear on the second one.

To evaluate this fact, an intensity profile (100 lines over a 200nm-size area along the growth direction) is carried out for both reflections at the same place of the sample (see thick lines in **Figure 71**).

An exhaustive analysis of these intensity profiles (here labelled as I_{004} and I_{220}) highlights the variations in the specimen's thickness along the profile. Grey line in **Figure 72** is used to plot experimentally acquired CTEM intensity values (measured averaging 100 lines over 200nm, as presented in **Figure 71**). Dark line in **Figure 72** is used to plot the CTEM intensity profile once the effect of the different thickness along the specimen has been removed. Once the "normalized intensity profiles" were acquired, **Eq. 19** (BDI or boron doping intensity) was used to determine the values of boron concentration and specimen thickness:

$$BDI_{hkl}(z) = \frac{\left(f_{eff}(z)\right)^2 \frac{sin^2(\pi \cdot t \cdot s_{effdoped})}{(\pi \cdot t \cdot s_{effdoped})^2}}{(f_0)^2 \frac{sin^2(\pi \cdot t \cdot s_{effundoped})}{(\pi \cdot t \cdot s_{effundoped})^2}} \qquad \textbf{Eq. 19}$$

Where f_{eff} is the effective scattering factor (that changes with the position (z), as the boron content also changes), S_{eff} the effective deviation parameter (definition of both parameters can be consulted in literature [131]) and *t* the sample thickness.

This procedure allows to overcome the problem of the wave intensity attenuation, because the A(t) parameter, already shown in **Eq. 16**, it's discarded by making the ratio. On the other hand, f_{eff} is defined [131] as:

$$f_{eff} = 8[xf_B + (1-x)f_C] \qquad \textbf{Eq. 20}$$

where *x* is the atomic percentage of boron inside the doped layer, while f_B and f_C are the effective scattering factors of boron and carbon, respectively. Note that, as these factors are dependent on the specific reflection, their values will be a function of the semiangle, as was presented in **Figure 66**. Here, we are not deriving **Eq. 19** nor **Eq. 20**, we instead refer the reader to the work of M.P. Alegre et al [137] for further information.

Please note that, at this point, we have one equation (**Eq. 19**) with two unknown parameters (*BDI* and f_{eff}). To solve this problem we will use two different crystalline orientations (that will be [004] and [220] for sample #7, as shown in **Figure 71**).

Iterative procedure

Once these experimental profiles are acquired, and by means of **Eq. 19**, an iterative and auto-consistent procedure is applied. For this, the theoretical BDI_{hkl} values for g = 004 are plotted with respect to the boron values in the range of interest (0-0.4% atomic). BDI, for a given reflection, depends on two quantities that we aim to determine here: (i) the thickness of the lamella *t* and (ii) the boron content.

To obtain a boron doping profile, the diffracted intensity should be considered at each position of the intensity profile of **Figure 72**. In **Figure 72**, black line corresponds to the original intensity profile while red line plots the corrected intensity profile. We will label the background intensity as I_0 and the boron doped layer intensity as I_C.

For this, we will first consider positions 1 (corresponding with I_C value) and 2 (I_0 value) in **Figure 72** (a): z = 99, I_C^{004} = 84 and I_0^{004} = 78; then $BDI(1)_{004}$ = 1.08. In the same way, in **Figure 72** (b): z = 56, I_C^{220} = 160 and I_0^{220} = 174; thus $BDI(1)_{220}$ = 0.92.

We introduce a mathmatic routine in which the SEM-measured sample thickess is taken into acount in the BDI theoretical values vs [B] plot. Both values were acquired from the intensity quotient of the values labelled as 1-4 in **Figure 72**. Then, the goal is to find a pair lamella thickness values t_f and boron concentration x_f that allows fitting the experimental values to BDI_{004} and BI_{220}.

Then, the values of concentration and thickness are sequentially calculated as shown in **Figure 73**. Indeed, **Figure 73** (a) shows output figure of the theoretical calculation of BDI_{004},

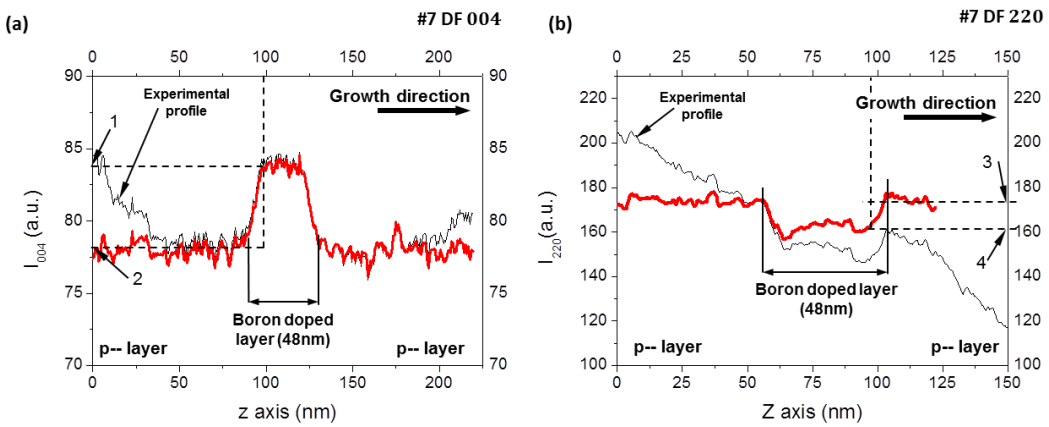

Figure 70: Sample #7, L2 experimentally acquired CTEM intensity profiles (averaging 150 lines over a 150nm length as described in **Figure 71**) for (a) g = 004 and (b) g = 220. Black lines are used to plot original experimental profiles; red lines are used to plot experimental profiles once the effect of the sample's thickness has been removed.

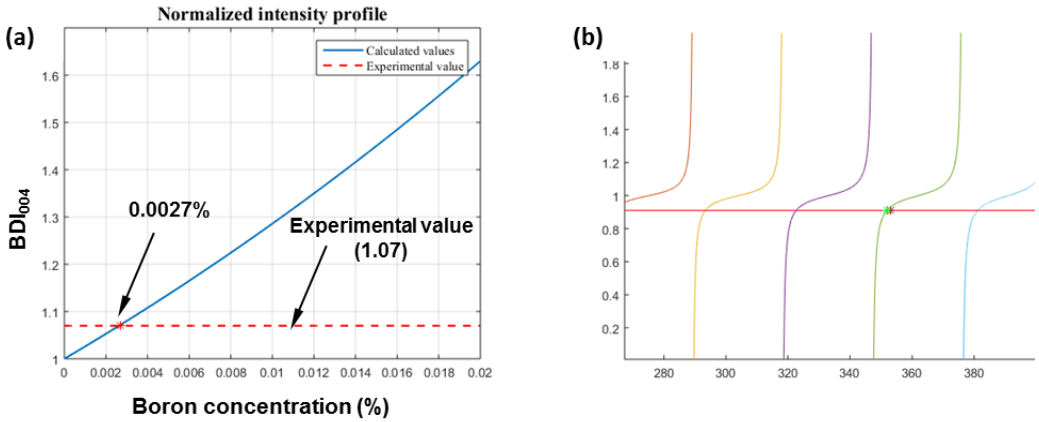

Figure 71: (a) Plot of the theoretical calculation of BDI_{004} for a 0<[B]<0.02% range. Dashed line mean lamella thickness of t_1 = 350nm. (b) Theoretical plot of BDI_{220} (0.91) vs thickness range between 275 and 400nm with a boron concentration of 0.0027% (value obtained from (a)).

leading to a boron concentration of 0.0027%, which is used as input for the plot of **Figure 73** (b): BDI_{220} vs lamella thickness.

So, the procedure consists in:

1. Lamella thickness is measured by SEM/FIB, then, experimentally measured BDI is plotted vs [B] for an specific pole (for example BDI_{calc}^{004})
2. [B] is deduced from BDI_{exp}
3. Using the latter [B] value BDI_{calc}^{220} is plotted vs thickness.
4. Repeat the procedure till iteration converges

After the first iteration, a new thickness of t_2=366nm is obtained and used again till this procedure converges to an stable value. Following this procedure, boron content of L2 was found to be ≈ $\underline{0.1 \cdot 10^{21} \text{at/cm}^3}$ and a lamella thickness value of 353 nm after 3 iterations.

By comparing this result with the corresponding SIMS measurements for the same structure, we observe several similarities: both profiles lead to thin highly doped diamond layers and with boron content that are compatible with the analyzed layer. Parameters used for this simulation were:

- Wavelength of electron, taking into account the relativistic correction at 120kV: λ = 0.00335nm
- Carbon structure factor: f_C = 0.1587802532 [131]
- Boron structure factor: f_B = 0.1446313502 [131]

- Diamond lattice parameter: a = 0.3567nm [138]

To evaluate the applicability of this methodology, additional studies on thinner diamond δ structures were carried out. Same procedure on sample #8 (**Figure 74**) reveals a δ-layer thickness of 4.7 0±0.5nm and a experimental boron concentration of $1.2\cdot10^{20}$at/cm^3 ($2.0\cdot10^{20}$at/cm^3 was obtained by SIMS).

The resulting intensity profiles as well as the boron concentration profile (obtained by using the previously described methodology) are presented in **Figure 74** (a) and (b). Secondary Ion Mass Spectroscopy (SIMS) provided a dopant depth profile for each sample, being the resultant average boron concentrations presented in **Table 11.**

Table 11: Summary of boron doping levels, obtained by SIMS, on the studied structures.

Sample	Layer	Layer thickness (nm)	$[B]_{exp}$ ($\cdot10^{20}$at/cm^3)	$[B]_{SIMS}$ ($\cdot10^{20}$at/cm^3)
#7	L1	60±5		0.02
	L2	48±5	0.1	0.3
	L3			1.8
	L4			4.5
#8		4.7±0.5	1.2	2.0
#9		1.4±0.2	5	---

Finally, the previously described procedure is used on sample #9. In this case, by using both reflections (g = 004 and g = 220) on sample #9, TEM micrographies reveals the highly

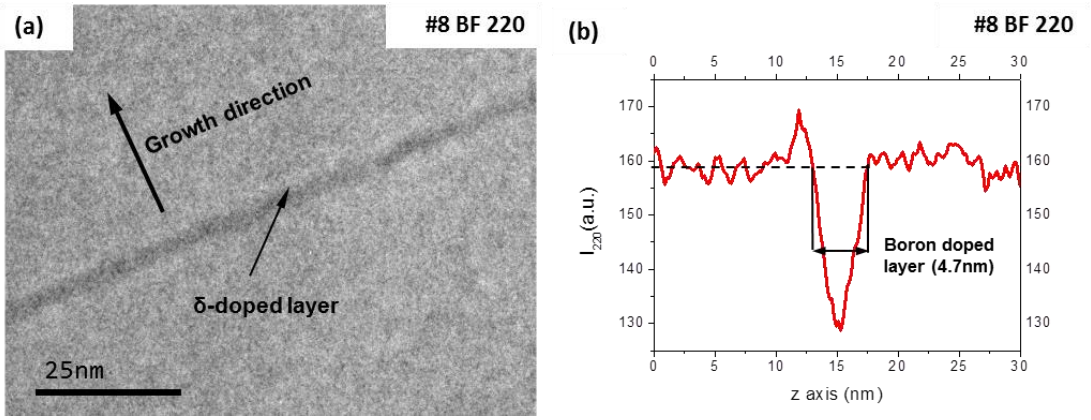

Figure 72: (a) Bright field micrography of thin diamond boron-doped δ layer on sample #8. Contrast variations between the highly doped regions and the non-doped ones are observed. (b) Intensity profile of the delta layer (sample #8) for g = 220 reflection.

doped δ-layer, as presented in **Figure 75**, whit a layer thickness of ≈1.4nm. Simulations provided a value of [B] = $5 \cdot 10^{20}$at/cm^3.

As can be appreciated, no SIMS measurements were done on #9, to preserve the specimen suitable for the δ-FET fabrication.

δ-FET characterization (#9)

Electrical properties of the δ-FET should depend, mainly, on the δ structure. For that, TEM studies of the related boron delta-doped layer were carried out, as shown in **Figure 75** (a). Thickness of the delta-layer was estimated from the intensity profile shown in **Figure 75** (b).

Thickness of the boron delta-doped layer was measured to be 1.4nm once the contribution of the background and the specimen thickness were removed [139]. **Figure 75** (a) shows TEM micrography of gate 2 in a δ3 structure from a CVD substrate (see **Figure 78**). A 15nm thick Al_2O_3 layer is observed over a 100nm thick Al layer. Boron delta-doped layer is located at 18nm from the oxygen-terminated surface.

Such a layer is expected to be heavily boron doped ([B]>10^{20}cm^{-3}), but, since Secondary Ion Mass Spectroscopy measurements were not carried out (because is a destructive technique) doping content was estimated from the fitting, presented in V.3 Diffraction contrast for boron doping profiling of δ-doped layers by TEM (#7, #8 & #9), resulting in a [B] ≈ $5 \cdot 10^{20}$cm^{-3} for the delta layer. A [B] ≈ $1 \cdot 10^{16}$cm^{-3} is expected for the buffer and cap layers (as obtained from Cathodoluminescence measurements). For ease of consult, key

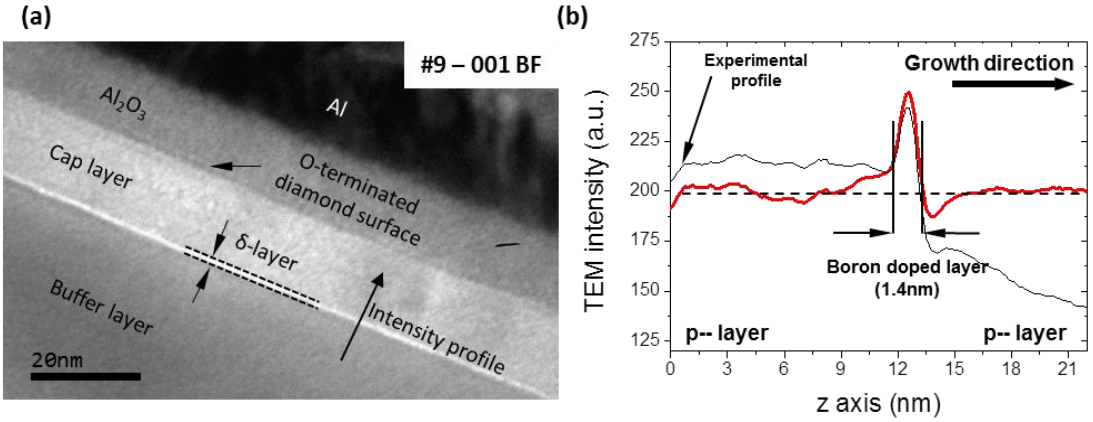

Figure 73: (a) BF micrography of thin diamond boron-doped δ layer on sample #9. Contrast variations between the highly doped regions and the non-doped ones are observed. (b) Intensity profile of the delta layer (sample #9) for g = 001 reflection. Thickness of the boron doped diamond layer of sample #9 shows a narrow doping profile, this sample will be used for the δ-FET device fabrication.

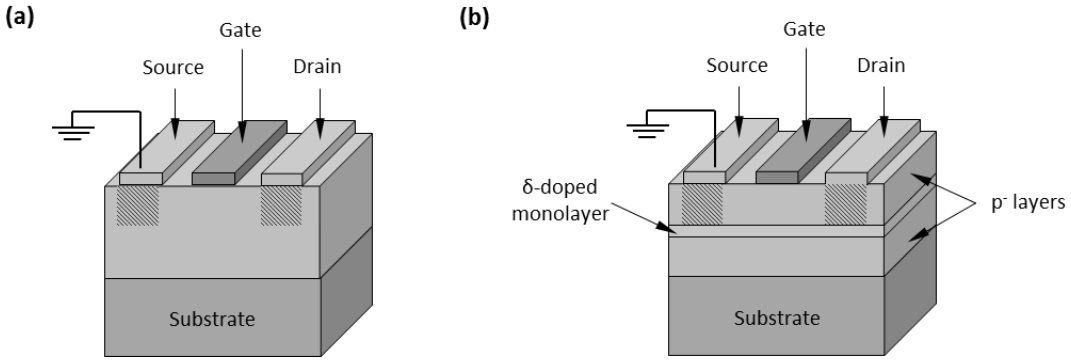

Figure 74: (a) Schematic diagram of the architecture of a conventional MOSFET and (b) a δ-doped FET (sample #7 was used to fabricate this structure).

parameters of this device are summarized here:

- δ-layer thickness: ≈ 1.4 nm
- Al_2O_3 layer thickness: 15nm
- $[B]_\delta \approx 5 \cdot 10^{20} cm^{-3}$

Even when these conditions are the ideal ones for a diamond-based δ-FET, the corresponding device did not yield any improved performance, as will be shown in next section. Some authors have demonstrated that, even for delta layers only a couple of nanometers thick, the mobility enhancement expected if holes were quantum confined was not observed [135].

V.4 Diamond δ-FET [#9]

The most evident limitations of Schottky diodes are the relatively low reverse voltage ratings for silicon-metal Schottky diodes (typically 50 V and below) and a relatively high reverse leakage current. Some higher-voltage designs are available; 200 V is considered a high reverse voltage. Reverse leakage current, because it increases with temperature, leads to thermal instability. This often limits the useful reverse voltage to well below the actual rating. While higher reverse voltages are achievable, higher forward voltage drops are registered, comparable to other types; such a Schottky diode would have no advantage unless great switching speed is required.

When less power dissipation is desired a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and a control circuit can be used instead of, in an operation mode known as active rectification. MOSFET is a more conventional semiconductor device whose conducting or insulating behavior is based on the electrostatic control of the band curvature at the oxide/semiconductor interface. The classic MOSFET structure consists in a 4-terminal device (as shown in **Figure 76** (a)) composed by:

- Gate and Source, ohmic contacts usually deposited over a doped region.
- Bulk contact in the substrate semiconductor.
- Gate contact, consisting in a semiconductor substrate, with a thin oxide layer and a top metal contact.

δ-doped diamond FETS

In order to fabricate well controlled thickness delta-layer, growth rates and etching rates must be known, so the recipe for the growing of diamond delta-layer structures presented by Chicot et al. [100] is here followed. A δ-FET in its simplest for was represented in **Figure 76** (b). In this architecture, the role of the channel is played by the delta layer. This delta layer is grown on a thick NiD (non-intentionally doped) layer called buffer layer and covered by a thinner NiD layer called cap layer. The drain and source are ohmic contacts which connect the delta layer channel through the cap layer.

For matter of convenience, these contacts are directly deposited on the cap layer before being annealed to reduce the contact resistance by forming a titanium-carbide at the

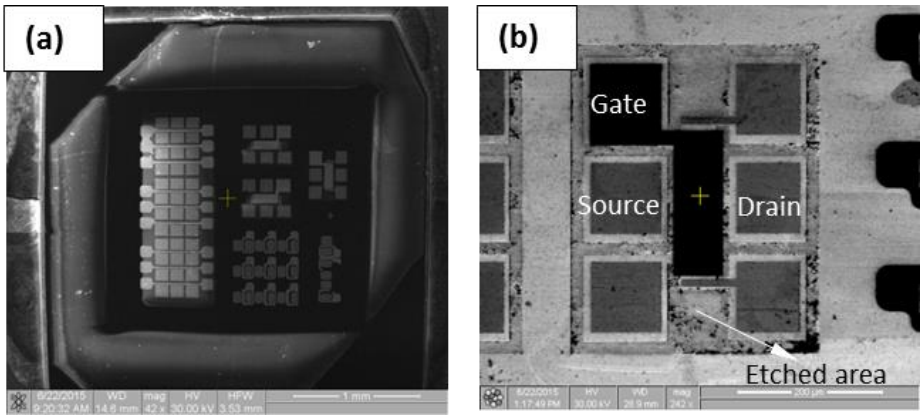

Figure 75: Different FET architectures deposited over δ-structures in (a) a 001-oriented HPHT substrate. (b) Detail of one of the FET architectures where gate, source and drain contacts are shown. Etched area, surrounding the FET structure is also presented in (b).

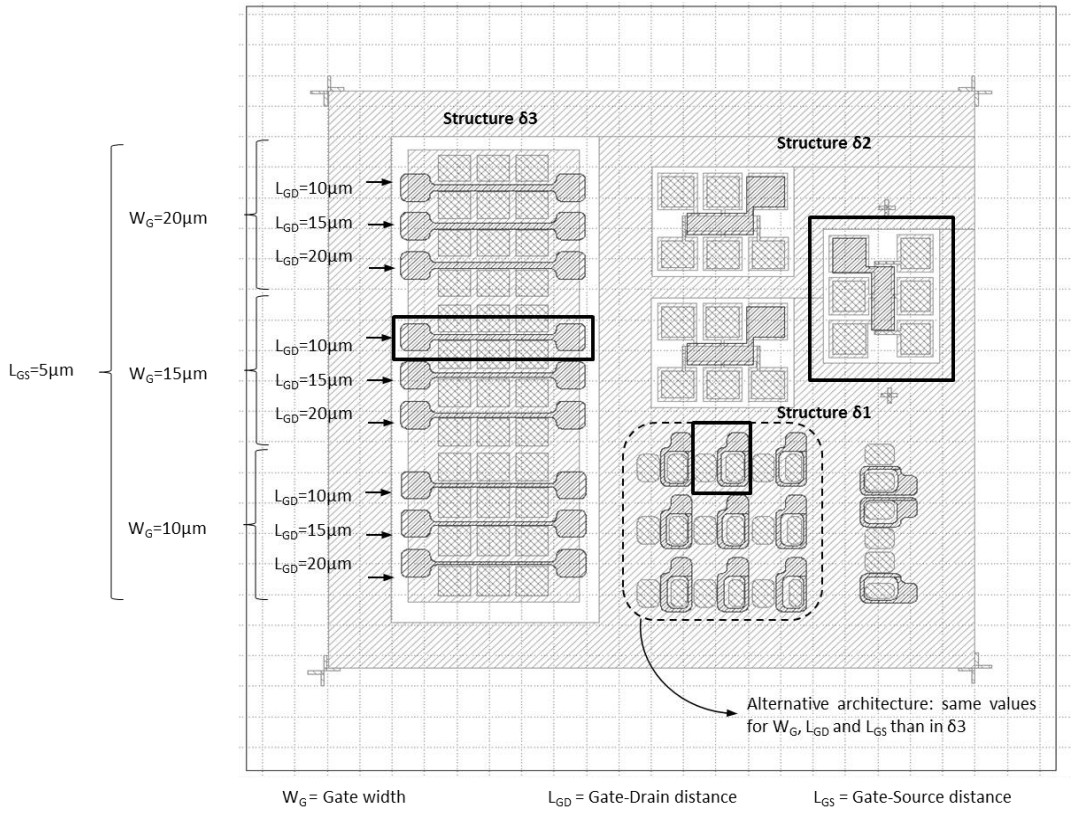

Figure 76: Picture of different FET architectures used in this work. δ1 structure shows an asymmetric design with different channel lengths and gate widths. δ2 structure shows a symmetric design with a constant channel length and gate width. An alternative δ3 structure was designed, by following the same channel lengths and gate widths, in order to test the effect of surrounding the source contact with the gate contact. Squares with thick-black lines are used to highlight the specific contacts that will be electrically characterized.

interface. Therefore, the drain and source are connected to the delta layer through the cap layer, but, thanks to the low thickness of the cap layer and macroscopic contact sizes, the induced access resistance is negligible with respect to the resistance of the channel.

The conduction of the channel is controlled by a gate which is a Schottky contact deposited on NiD cap layer. If sufficiently thin delta layers are obtained, delta-FET combining high carrier concentration and high mobility could be achieved. Such a transistor would be on in the normal state when no voltage is applied on the gate and off for an applied positive voltage.

In fact, if the cap layer and the delta layer are depleted of charge carriers under the gate, the current should not flow anymore between the drain and source electrodes. This voltage must

be high enough to completely deplete the channel in order to have a good off state. Even if the breakdown field in diamond is higher than in other semiconductors, the large amount of charges needed to create a metallic delta layer (with [B] > $N_{crit(3D)}=5\cdot10^{20}cm^{-3}$) counterbalances this high value. Therefore, the breakdown field of diamond will introduce a limitation for the sheet charge density that can be depleted in the channel.

Once the delta-layer is grown, gate (made in Al/Al_2O_3), source and drain (made in Ti/Pt/Au) contacts are deposited following different architectures. The latter are shown in **Figure 77**, were the FET structures are presented. Finally, **Figure 77** (b) shows a detail of a one of the structures, where the etching process, surrounding the FET area, can be appreciated (etching of the surrounding area of the FET is necessary to isolate the studied structure).

A detailed schematic of the FET proposed architectures is presented in **Figure 78**. Such designs are labelled as δ1, δ2 and δ3 and they were designed for testing different MOSFET architectures and parameters:

- δ1 structure shows an asymmetric drain-gate-source design. Different channel lengths and gate widths can be tested in this device.
- δ2 is a symmetric drain-gate-source design. Single gate length.
- δ3 gate contact is used to surround source contact; this can reduce channel leakage effects. Corners of the contacts are rounded, in order to avoid sharp corners that could induce bad electrical behavior at high voltages. Channel lengths and gate widths are those of δ1.

MOSFET electrical properties

There are many ways to categorize the versions of FETs. When channels are formed by electrons (n-type channel), it results on a more conductive channel with a more positive gate bias. That is, the source-drain current increases if the gate bias increases (positive bias). On the other hand, p-type channels are formed by holes and are more conductive with more negative gate bias; this occurs when the gate bias decreases in the negative range. Furthermore, it is important to describe the state of the transistor with zero gate bias. FETs are called enhancement-mode, or normally-off, if at zero gate bias the channel conductance is very low and a gate voltage to form a conductive channel must be applied.

The counterpart is called depletion-mode, or normally-on, when the channel is conductive with zero gate bias and a gate voltage to turn the transistor off (see **Figure 79**) must be applied.

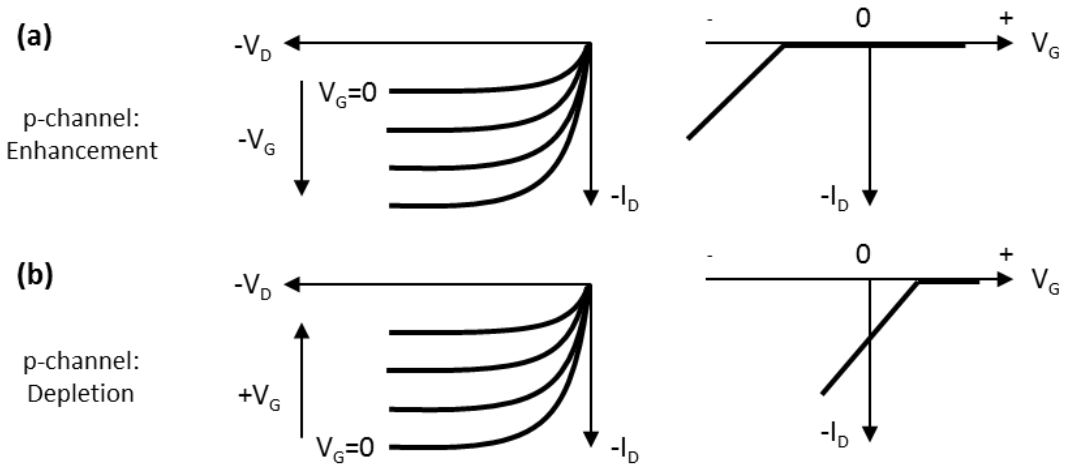

Figure 77: V_D vs I_D for various gate voltages and V_G vs I_D in case of a MOSFET with p-channel in (a) enhancement-mode (normally-off) and depletion-mode (normally-on)

It is also important to point out the nature of the channel in more details. A channel can be formed by a surface inversion layer (as in conventional MOSFET) or a bulk buried layer (see **Figure 80**). The surface inversion channel is a two-dimensional charge sheet of thickness in the order of 5 nm. The buried channel is much thicker, comparable to the depletion width since when the transistor is turned off; the channel is totally consumed by the surface depletion layer. In the FET family, MESFETs and JFETs are always buried-channel

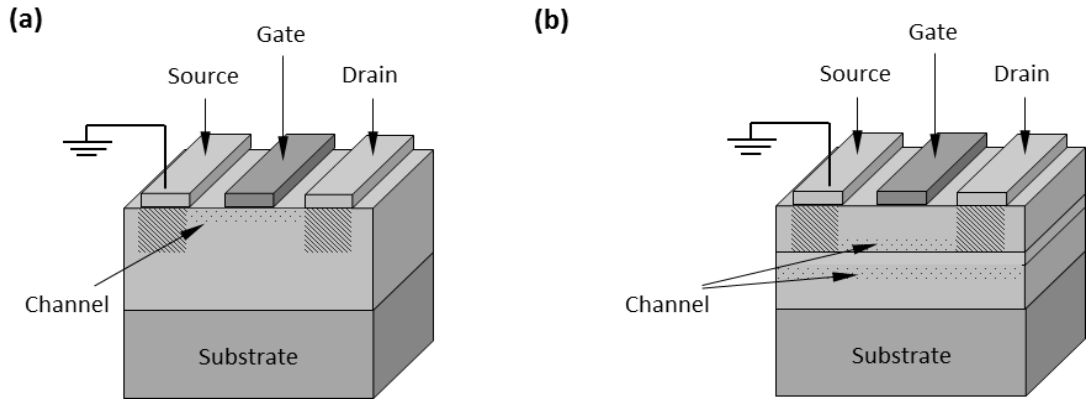

Figure 78: FET channels: (a) surface inversion channel and (b) buried channel. Take into account that a common MOSFET is a four-terminal device that consists of a p-type semiconductor substrate into two n^+-regions (the source and drain) that are formed, usually, by ion implantation.

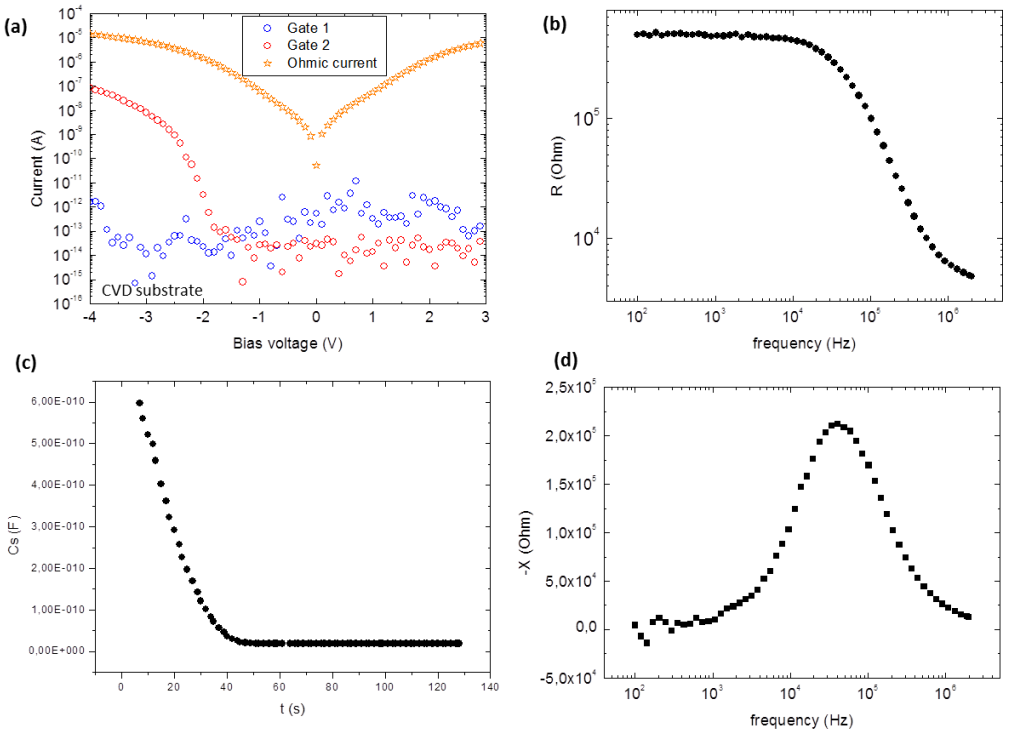

Figure 79: Electric measurements carried out in δ3 structure of #5 showing (a) I(V) characteristic in gates 1 and 2, (b) ohmic resistance vs frequency in gate 2, (c) capacitance vs frequency in gate 2 and (c) impedance vs frequency in gate 2. Measurements were carried out in vacuum at 300K.

devices, while MODFETs are surface-channel devices. MOSFETs and MISFETs can have both kinds of channels in parallel, but in practice, they are mostly surface-channel devices.

These two kinds of channels offer advantages of their own. Buried channels are based on bulk conduction and, thus, are free of surface effects such as scattering and surface defects, resulting in better carrier mobility. On the other hand, the physical distance between the gate and the channel is larger and also dependent on gate bias, leading to a lower and variable transconductance.

Note that for depletion-mode devices, it is common to use buried channels, but theoretically, one can achieve the same goal by choosing a gate material with a proper work function to shift the threshold voltage to a desirable value. In our case, boron doped diamond delta layers are used to delocalize charge carriers; charge carriers can move through the undoped diamond lattice, where mobility is higher. This means that our transistor will be "normally on", and we have to apply a gate voltage in order to reach the different operation regimes.

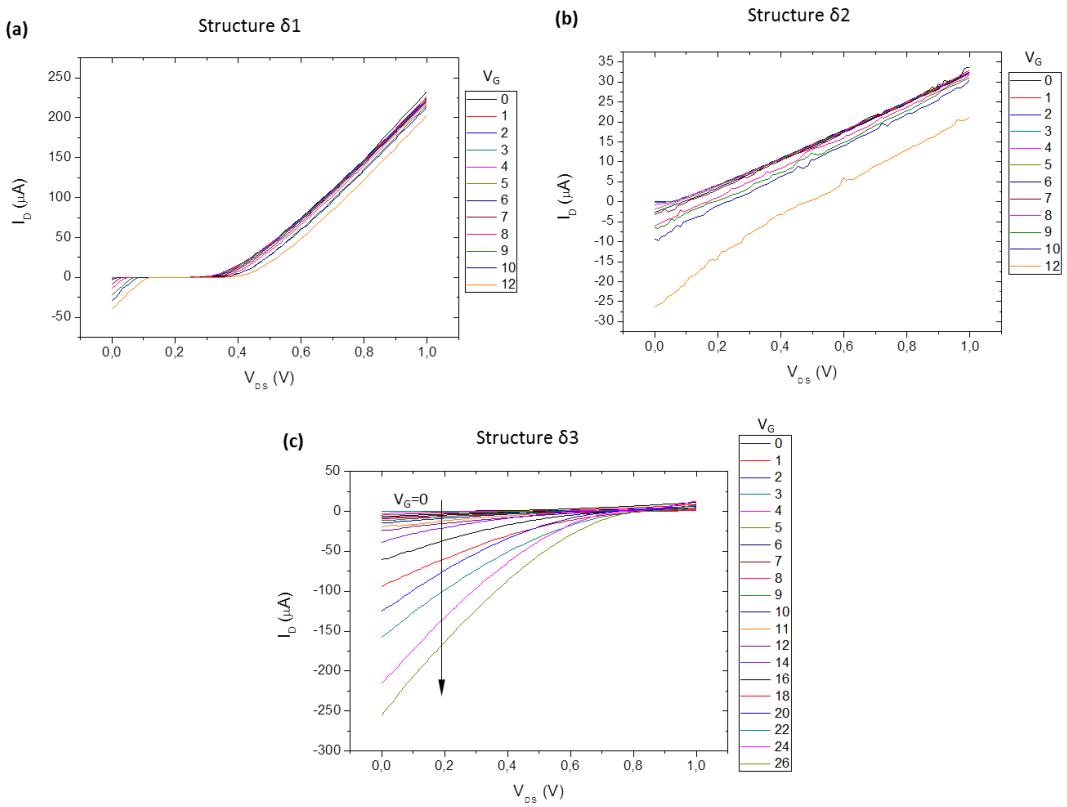

Figure 80: I_{DS} vs V_{DS} characteristics (for various gate voltages) of the δ-FET structures presented in **Figure 76** over (a) δ1 structure, (b) δ2 structure and (c) δ3 structure.

Experimentally[23], electrical properties of Gate, Source and Drain contacts were studied by 2 probe measurements. Electric characteristics of such contacts are presented in **Figure 81**. Particularly **Figure 81** (a) shows 2 probe measurements of a δ1-type structure. As can be observed, ALD-deposited oxide (T = 250ºC) seems to give good oxide in some structures, insofar that no leakage current through the gate is observed (Gate 1, blue signal in **Figure 81** (a)). However, some other structures are still showing leakages, as can be appreciated in red color of **Figure 81** (a) (Gate 2).

Moreover, current between the two ohmic contacts is at least two orders of magnitude higher than leakages. Higher leakages were observed in other structures, which mean that δ3-type structure is the most efficient among the whole sample.

[23] Electric characterization was carried out by J. Piñero, F. Lloret and A. Maréchal at Institut Néel (Grenoble, France) facilities.

Once the contacts of the related device were characterized, 3 probe measurements were carried out to obtain I_{DS} vs V_{DS} features for a variety of gate voltages (V_G). Comparing the experimental results shown in **Figure 82**, with the theoretically expected shape (see **Figure 79**), we found that

- δ1 structure shows voltage shifts, and is not reaching saturation region. We just observe linear behavior.
- δ2 structure shows bad electrical behavior, even in linear region. This may be caused to the device architecture, in which leakages can be produced.
- δ3 structure also shows voltage shift (as in δ1 structure). Linear region is observed, and no saturation region is reached.

We can conclude that no channel modulation is produced by modifying gate voltage. This could be explained by the fact of that, unfortunately, the Al/Al_2O_3/diamond capacitor is not reaching inversion regime, thus making impossible the modulation of the channel that is essential for the MOSFET behavior. Additionally, voltage shifts are appreciated in all structures.

- Focusing in δ3 structure (the one showing better electrical behavior), we observe that, when increasing the gate voltage, the shape of the $I_{DS}(V_{DS})$ moves from top to bottom (see arrow in **Figure 82**). The latter is the opposite of the expected characteristic of a normally-ON device, based on a p-type channel (see **Figure 79** (b)). Several phenomena can explain this behavior:
- Oxide-related leakages (as studied in Chapter IV).
- Probably, no "normally ON" behavior is produced, which also means that no charge carrier delocalization occurs in the sample.

We can conclude that, probably, no channel was formed during our experiments, and that ALD growth of the oxide is a parameter that has to be improved in order to get reliable structures.

V.5 Conclusions

Conclusions on δ-layers characterization

In V.2 Boron concentration profiling (#5 & #6), boron content in-depth profiles of homoepitaxially grown heavily doped diamond epilayers were measured quantitatively by HAADF-STEM down to 10^{20} B/cm^3 at nanometric resolution (layers of 48, 4.7 and 1 nm

thick were measured). Boron was shown to locate preferentially at undoped/doped interface, and the broader SIMS profile of the deeper interface of p^{++} layers is shown to be an artefact related to ion mixing processes. The experiments highlighted the potential of HAADF-STEM for characterizing, with a nanometric resolution, the boron content of diamond based delta-doped layers. Extremely thin δ-doped layers down to 5 nm thick are demonstrated in boron concentration edges steep enough to expect that even slightly thinner epilayers would induce some carrier delocalization.

δ-FET fabrication

Beside the efforts in fabricating reliable δ-FET devices, no field effect or enhancement of the mobility was observed. This can be attributed to a variety of facts:

1. δ-layer is not thin enough to induce carrier delocalization.
2. Oxide of the MOS stack leads to leakages and shortcuts.
3. No ohmic contact is produced between source, drain and the delta layer.

1. δ-layer thickness:

As said before, some authors have reported that δ-layers in boron doped diamond have to achieve a thickness value below 2nm [56]. In fact, the working zone in which this kind of devices device can operate, can be obtained by considering a planar capacitance composed by gate/cap-layer/delta layer. Following this reasoning, Chicot et al. [100] summarizes the operating area in **Figure 83** for a diamond breakdown voltage of 10MV/cm [140]. The breakdown field is reached for a sheet hole density equal or later than $3.2 \cdot 10^{13} cm^{-2}$.

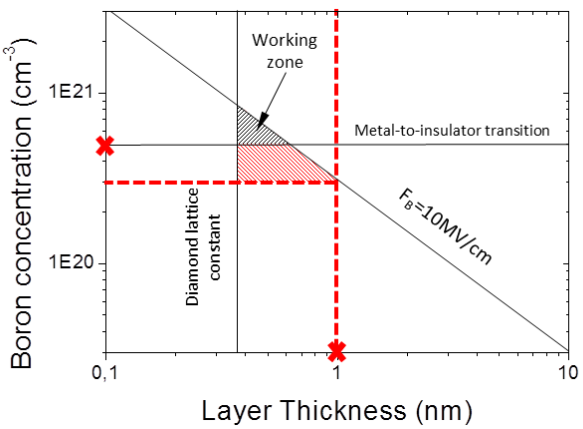

Figure 81: Boron concentration versus thickness map with diamond breakdown field. Triangle named "working zone" shoes the range of doping level and thickness eligible for a delta FET where the channel can be closed by applying a voltage without reaching the breakdown voltage. Red crosses are used to highlight the boron concentration and layer thickness of sample #9 (δ-FET device).

This diagram shows that the working zone where a diamond delta-doped FET channel can be closed without reaching the maximum breakdown field is very

limited. In fact, in addition to the electric field limitations, low limitation in terms of thickness (by the lattice constant) and in term of doping (by the metal-to insulator transition MIT) will restrain further this working zone.

However, the "working zone" of **Figure 83** was calculated by making some assumptions (see [100] for details), so this "working zone" is useful to obtain an order of magnitude for the thickness and doping level of the delta layer to be incorporated in a delta FET for which the channel could be closed.

In our case, the calculated boron content of $\approx 5 \cdot 10^{20} cm^{-3}$, seems to be sufficiently high to reach the metal-to-insulator transition. However, measured layer thickness of ≈1nm seems not to be thin enough to reach the theoretical working zone (even when this thickness is expected to be enough for inducing carrier delocalization). Working zone of our δ-FET device (sample #9) is presented in **Figure 83** with a red mesh, it can be appreciated that our device is close to the theoretical working zone.

To summarize, delta-layers thinner than 0.64nm and doped between $5 \cdot 10^{20} cm^{-3}$ and $1 \cdot 10^{21} cm^{-3}$ have to be aimed at. A delta-layer theoretically suitable for these requirements was simulated, results can be seen in **Figure 64**, where it can be observed that an important part of the holes are delocalized out of the delta-layer, which would entail a significant improvement of the mobility if such a layer could be grown.

Nevertheless, if a high mobility value can be achieved in such a structure, even if it is not possible to close the channel in the corresponding delta-FET, such a device could be used for radio-frequency applications.

2. Oxide quality:

In Chapter IV, we show the importance of an optimum oxide layer in the MOS behavior. Probably, MOS stacks of sample #9 are presenting oxide failures that couldn't be appreciated by TEM (because a very reduced area of the sample is studied by TEM).

3. Contacting the δ:

Probably, source and drain contacts can be improved by using boron implantation. In our experiment, we expect the δ to be electrically contacted with source and drain. However, the use of ion implantation of ≈ 20nm depth and rapid annealing could be used to create p^+ islands before depositing the ohmic contacts.

General conclusions

A variety of δ-structures have been studied and characterized by a various TEM techniques, among them:

- HAADF, used to characterize the thickness of the δ-layers
- CTEM (in BF and DF modes), used to estimate the boron content of the specific δ-layers

Delta layers were fabricated aiming at obtaining abrupt interfaces, a sufficiently high boron doping level insuring a metallic conduction in the delta layer and low doped NiD cap and buffer layers suited for high mobility. Nanometer thick delta layers were obtained and characterized by TEM. The latter confirmed the nanometric thickness for metallic delta layers thinner than 2 nm, but showed no enhancement of mobility.

Several indications of scattering mechanisms due to ionized impurity are pointed out in literature [135, 136], aiming to firstly though that two dimensional scattering mechanism must be responsible of the low mobility value measured in metallic delta-layers.

These δ-FET structures have been recently studied and have attracted special interest [136], because of the expected high performance at high frequencies if the numerous carriers from the delta layer could effectively flow in a high mobility region. This transistor should be normally ON without applied bias, but this effect was not observed (meaning that no hole delocalization is achieved).

This fact is confirmed by other authors [141], who didn't observe the full activation of boron impurities, the presence of weak delocalization and verify the absence of any mobility enhancement. Chicot et al. [141] reports a constant mobility value of 3.6 ± 0.8 $cm^2/V \cdot s$, measured independently of the thickness or substrate type.

Within the usual approximations such as that of a parabolic valence band, the bulk mobility which was calculated by these authors, taking into account quantitatively the scattering by ionized impurities, was a factor four higher than the experimental mobility value.

To summarize, a thin diamond-metallic layer was reported with growth conditions similar to that of [100]. Unfortunatelly, the related electrical behavior was not enough to consider that high frequency field effect transistors in diamond using delta-doped structures could be one day able to compete with the present AlGaN/GaN HEMTs (showing mobilities of 2200 $cm^2/V \cdot s$), even when the measured thickness of the delta structure was below 1.5nm

Furthermore, it seems challenging to grow thinner metallic diamond layers and even if achieved, there is no guarantee that such layers would exhibit a higher mobility than

reported in the previously cited literature. Therefore other architectures such as diamond MOSFET have to be investigated. However, even if the initially target of a delta-field effect transistor seems to not be promising due to the too low mobility measured in the delta-structures, this investigation of the delta layer electrical properties allows us to understand and to progress a lot on both diamond growth and electrical characterization techniques.

One of the important results of this work is to highlight that, with the present knowledge and with an optimum design (in terms of delta-layer thickness, delta-layer depth, gate design) and with different architectures, no field effect and no enhancement of the mobility are achieved.

Chapter VI: Conclusions and perspectives

In this work, interfaces of zirconium, tungsten semicarbide and aluminium oxide with oxygenated diamond surfaces before and after a variety of thermal treatments anneal have been characterized on the one hand by TEM imaging and EELS spectroscopy at University of Cádiz (Spain), and on the other hand by through electrical measurements made on Institut Néel (France) and in the National Institute of Materials Science (NIMS – Japan). The knowledge accumulated through these studies was used to design a δ-doped diamond FET device, such device was also electrically and structurally characterized.

Conclusions – Schottky barrier diodes

In Chapter III: diamond-based Schottky barrier diodes, evidences of an oxide interlayer of approximately two atomic layers have been obtained in case of the oxygen-terminated diamond-based Schottky barrier diodes. Current-voltage characteristics, EELS mapping and TEM micrographies have been collected at several temperatures in some diodes and analyzed in order to investigate the detailed shape of the current density behavior with applied voltage.

Existent physical models, taking the barrier height and current density inhomogeneities, have been applied and brought face to face with experimental results. From these comparisons, several physical phenomena have been revealed. Among them:

- the existence of a thin oxygen-content layer in oxygen terminated diamond-metal contacts
- the evolution of such a layer with:
    - the thermal treatment
    - the Schottky metal
- the possibility of direct diamond/metal bounds has been highlighted

The effect of different shapes of barrier fluctuations has been spotted, this phenomena is here related with local barrier enhancements or local barrier lowering due to the variations in the interfacial oxygen content. This behavior has been related, by other authors [88], with fixed repulsive charges close to the interface.

In the near future, barrier inhomogeneities would be characterized by a variety of TEM techniques. Concerning these characterization techniques, a procedure for the TEM evaluation of diamond interfaces has been established.

Because of the known inhomogeneity of the oxygen terminations and enhancement of the electron affinity by also 1.4 eV on the initial oxygenated diamond surface, EELS data strongly suggests that these oxygen terminations vanished after high temperature annealing. Then, the more general issue of barrier height determination and Fermi level pinning has been addressed by means of an analysis of the experimental data collected in the present work and in recent literature, eventually reassessed with the help of the methods presented before.

The test of other metals after annealing confirms the disappearance of oxygen terminations, irrespective of the presence of an oxide interlayer or not, and the electron affinity of the diamond surfaces as a relevant quantity for barrier height description.

The next steps for developing reliable diamond Schottky diodes could be:

Improving the total diamond surface covered by oxygen: As evidenced in Chapter III, dangling bonds are created because of the lack of oxygen termination in some points of the diamond surface. Indeed, large areas of the diamond surface could be not covered by oxygen. This lack of oxygen termination may not only be a consequence of the deposition process of the metal stack, but also related with the VUV-ozone treatment. Further investigations in this area may lead to a significant improvement of the oxygen-terminated diamond surface.

The metal choice: Different metals were tested in order to build diamond-based Schottky diode, evidencing a different device behavior with the thermal operations. Searching an appropriate metal that manages to hold the oxygen termination at high

temperatures (more than 700K actually) is a key step in the performance improvement of these devices.

Interface bandgap tracking: An accurate control of Schottky and MOS devices could be achieved if a deeper knowledge of the energy-band diagram configuration of the oxygen-terminated diamond/metal interface is reached (as recently highlighted in [142]). To do so, different techniques such as XPS or STEM-EELS may be used for future investigations of oxygen-terminated diamond interfaces.

Conclusions - MOS

In Chapter IV: diamond-MOS structures, we demonstrated the fabrication of metal oxide diamond structures where different regimes are controlled by the gate bias: accumulation of holes, depletion and deep depletion. In accumulation regime (negative voltage), a frequency dispersion of capacitance value was measured and attributed to the high series resistance of diamond but also to defects involved in non-ideal MOS structures. In the positive voltage range where the inversion or deep depletion (depending on measurement frequency) regimes are expected, a capacitance increase was observed and has been attributed to a possible inversion regimes allowed by electrons flowing through diamond layer defects. On the contrary, the observation of the capacitance decrease attributed to the deep depletion regime in the other samples is consistent with the high measurement frequency (and the fast sweeping rate) used, which does not allow generation of any minority carrier.

UV illumination of a sample showing deep depletion, did not lead to the detection of minority carriers. The frequency measurement and the bias voltage sweeping rate are certainly still too high to create inversion, even if minority carriers are optically generated. Nevertheless, the observation of a deep depletion regime in sample #4 opens the route for the fabrication of diamond MOSFET.

This requires that the gate insures the electrostatic control of the channel and so, the on state (inversion) and the off state of the device. Such a transistor would be normally in off state because of a channel in depletion regime when no bias is applied to the gate, since the flat band voltage is not strongly negative. This case is indeed achieved in sample #1 as it can be seen on band C(V) measurements in **Figure 50**, while the more negative flat band voltage in sample #4, which might induce weak inversion, deserves future investigations.

Electrical measurements enabled us to investigate band offsets of the diamond MOS structures and show that for samples #1 and #4, only a small barrier for holes exists, which would be an issue during MOSFET operation. In fact, the oxide must be more insulating to avoid current flowing between source (or drain) and gate, otherwise the control of the

different states would not be effective. Therefore, future work on MOS structure has to focus on oxide improvement and defects (interface states and charges in the oxide) investigations.

Some roads that can be followed to continue the investigations initiated in this work are:

Oxide improvement: An improvement of the aluminum oxide is probably the next crucial step to avoid the possibility of C(V) hysteresis). This can be achieved by using active ozone instead of water precursor during the growth of the oxide [143], this would help for instance to reduce hydrogen contamination in the oxide. Another parameter which can be tuned is the temperature: using an approach in which the oxide is deposited on the whole surface of the sample and then patterned by an etching step (to avoid the limitation of the temperature resistance of the resistor). Oxide post annealing can be also an option, to desorb unused precursors (including water) which could be at the origin of mobile charges in the oxide or to crystallize the oxide itself. Finally, the use of other oxides has to be considered to obtain a larger barrier for holes in accumulation and to tune the flat band voltage in such a way that the MOS structure is in depletion at 0 V to yield a normally off-MOSFET.

Interface states investigation: The fact that some MOS capacitors shows an almost inexistent frequency dependence, opens the way for more accurate and systematic interface states studies. Further measurements, especially using the conductance method, transient capacitance measurements and very low frequencies, must be performed in order to obtain more reliable quantification of interface states. A multi samples study, where oxide deposition, surface treatment or diamond growth parameters are varied could help to distinguish the contribution of interface states from the one of mobile charges in the oxide (or even defects from the diamond active layer).

Conclusions δ – FETs

In Chapter V, we demonstrate the fabrication of a thin, highly boron doped diamond layer. We introduce a variety of techniques to characterize its thickness and its doping content. Different FET designs over the diamond δ-structure were studied. Even when such a thickness and doping were the optimum values for a δ-FET architecture, no charge channel was formed in the FET.

This could be due to inexistent charge carrier delocalization (even when the δ configuration is the optimum one). As the MOS-gate configuration is not able to work properly, this acts as a second bottleneck for this kind of devices.

The same evolution the oxygen-terminated surface is observed in oxygen-terminated diamond MOS structures, also showing the possibility of dangling bonds, thus altering the normal MOS behavior.

Finally, a set of δ-FET architectures have been tested in order to check for transistor-like behavior. Here, we confirm the observation of a less than 1.5nm thick boron doped layer, which was insufficient to delocalize carriers. The impossibility to reach thicker delta-layers reaches to a dead way in which no improvement of the mobility was observed.

However, improvements in this field could be achieved by solving the next problems:

MOS stack improvement: as a key part of the FET device, MOS stack has to be controlled and oxide-related defects has to be fixed.

Optimizing the deep of the δ-layer: here, we use a 1.5nm thick diamond boron doped layer, located at 20nm deep from the diamond surface. Ohmic contacts are expected to be electrically contacted with the δ-layer, but this possibility could not be confirmed. Alternative architectures, allowing a physical contact between the δ-layer and the ohmic contacts may lead to significant improvements.

Reaching thinnest δ-layers: Although this point is obvious, reaching δ-layer thickness of less than 1.4nm in diamond is a technological challenge. If diamond δ-layers of less than 1nm could be reached, a well-designed device δ-FETs should be operative and competitive.

Beside of these not positive results on diamond δ-FET development, promising results both in Schottky barrier diodes and diamond-based MOS structures have been obtained. All these concerns have been presented and discussed with the help of new experimental results, improved models and recent high quality experimental works in the purpose of fostering new advances in the old problem of potential barrier at metal-covalent semiconductor interfaces.

ANNEX I: Electron Microscopy techniques

A.1 Scanning Electron microscopy (SEM)

In a scanning electron microscope (SEM), an electron beam, with energy typically comprised between 1 and 30 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter on the surface of a sample. The re-emitted secondary electrons are collected by an Everhart-Thornley detector, which roughly consists of an anode polarized with a potential of a few hundreds volts.

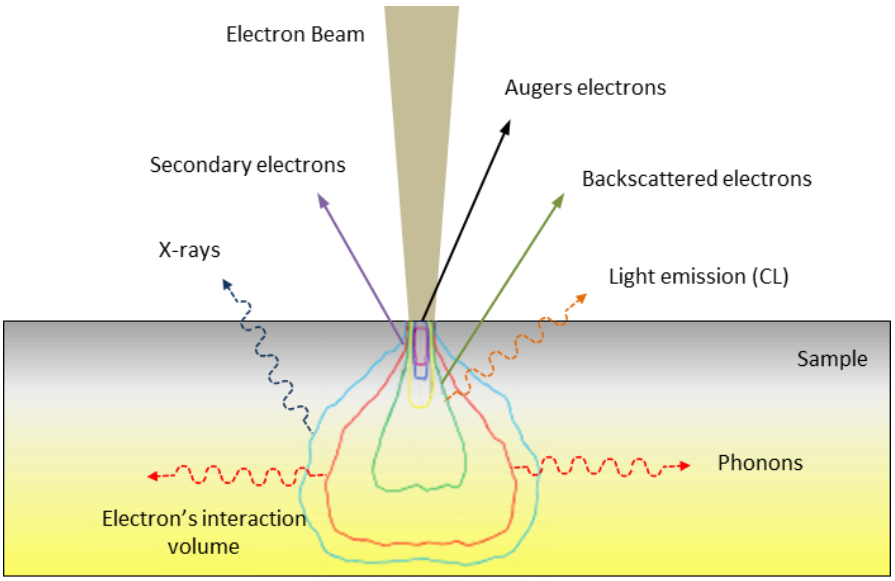

Figure 82: Electron beam interaction diagram and brief resign of the types of signals produced by an SEM

Unlike the TEM, where electrons of the high voltage beam form the image of the specimen, the SEM produces images by detecting low energy secondary electrons which are emitted from the surface of the specimen due to excitation by the primary electron beam. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition and other properties such as electrical conductivity. The types of signals produced by an SEM include secondary electrons, back scattered electrons (BSE), characteristic x-rays, light (cathodoluminescence), specimen current and transmitted electrons as shown in **Figure 84**. These types of signal all require specialized detectors for their detection that are not usually all present on a single machine.

The SEM micrographs have a very large depth of field yielding a characteristic three-dimensional appearance useful for understanding the surface structure of a sample. Because the SEM uses electromagnets rather than lenses, the researcher has much more control in the degree of magnification.

For conventional imaging in the SEM, specimens must be electrically conductive, at least at the surface, and electrically grounded to prevent the accumulation of electrostatic charge at the surface. Metal objects require little special preparation for SEM except for cleaning and mounting on a specimen stub. Nonconductive specimens tend to charge when scanned by the electron beam, and especially in secondary electron imaging mode, this causes scanning faults and other image artifacts. They are therefore usually coated with an ultrathin coating of electrically-conducting material, commonly gold, deposited on the sample either by low vacuum sputter coating or by high vacuum evaporation. Conductive materials in current use for specimen coating include gold, gold/palladium alloy, platinum, osmium, iridium, tungsten, chromium and graphite. Coating prevents the accumulation of static electric charge on the specimen during electron irradiation.

In a SEM, a beam of electrons is produced at the top of the microscope by an electron gun. The electron beam follows a vertical path through the microscope, which is held within a vacuum. The beam travels through electromagnetic fields and lenses, which focus the beam down toward the sample. Once the beam hits the sample, electrons and X-rays are ejected from the sample. Detectors collect these X-rays, backscattered electrons, and secondary electrons and convert them into a signal that is sent to a screen similar to a television screen. This produces the final image.

Depending on the position of the detector with respect to the orientation of the sample surface, the number of collected electrons varies. In a naïve view, we therefore have access to the topography of the surface of a sample by scanning it with the electron beam and collecting in parallel the emitted secondary electrons. The spatial resolution of this

technique is given by the spatial extension of the volume emitting secondary electrons and is of the order of a few nm.

Cathodoluminescence (CL)

When an energetic (several keV) electron beam is delivered on a solid, the incident electrons are scattered, elastically or not, by the atoms of the solid and are then re-emitted. The emitted electrons presenting an energy comparable with the primary electrons are called backscattered electrons. On the contrary, electrons emitted after several inelastic scatterings and of energy of typically few eV are called secondary electrons.

The particles excited by an inelastic electron / atom scattering can cover a wide range of energies. When the energy of the incoming electron is sufficiently high, it can promote an electron of the atom from a deep energy level to a higher energy one (for instance from K to L orbital). The excited electron will then relax by emitting X-ray. When the energy loss of the incident electron is only of a few eV, it only excites an electron from the valence to the conduction band. In the case of semiconductors, the excited electron relaxes toward the bottom of the conduction band and then recombines. The light emission subsequent to the excitation by an electron beam is called cathodoluminescence (CL).

In order to collect the cathodoluminescence signal, a parabolic mirror is introduced between the sample and the polar piece (objective lens) of the microscope. The two main drawbacks yielded by the presence of the mirror are: (*i*) reduction of the number of secondary electrons reaching the Everhart-Thornley detector, thus decreasing the signal-to-noise ratio of the

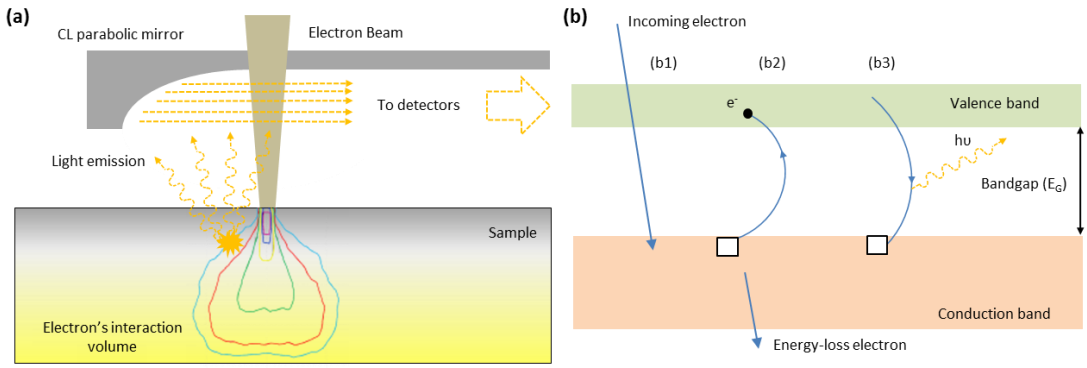

Figure 83: Experimental CL setup diagram in a conventional system (a) and schematic process of the physic phenomena (b). Figure B shows a brief scheme of the process whereby an incoming electron (b1) promotes to to another one from the valence to the conduction band (b2), relaxation of this second electron allows the production of a photon (b3) of energy E= hυ

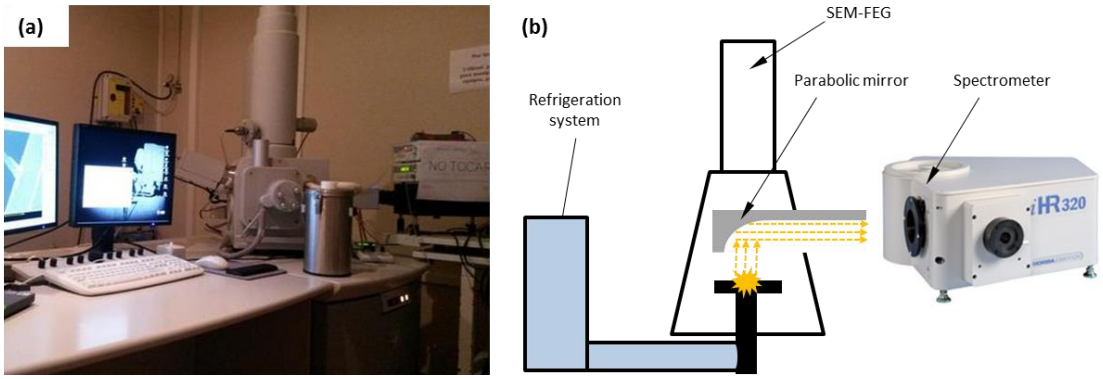

Figure 84: Experimental CL setup diagram in our home-made system (a) photography of our system in a FEI-Sirion SEM-FEG and (b) simple schematic of the whole experimental system including the refrigeration system (by liquid nitrogen), SEM, parabolic mirror and spectrometer.

secondary electron mapping, (*ii*) increase in the working distance and therefore decreasing the spatial resolution of the set-up.

The CL signal is then sent to a monochromator followed by a photomultiplier tube or a CCD. As is the case for SE mappings, CL mappings are obtained by scanning the electron beam on the surface of the sample while detecting in parallel the emitted CL.

However, the spatial resolution of CL is more difficult to estimate, as one has to care not only for the extension of the generation volume, but also for the diffusion of charge carriers. Let us finally note that the penetration depth of the electron beam inside the material increases with the acceleration voltage. It is thus for instance possible to distinguish by depth-resolved CL the emission of near surface-states from that of the underlying material.

As shown in **Figure 85**, CL signal is produced by an electron-hole recombination; it's possible to estimate the density of electron-hole pairs generated in a semiconductor by an electron beam. It is usually admitted that, to create an electron hole pair of energy equal to the bandgap, an energy of the order of two times the bandgap is lost through different inelastic scattering mechanisms. Consequently, from the acceleration and the intensity of the incident electron beam, we know approximately the number of injected charge carriers.

In order to access the density of charge carriers, we must determine the spatial extension of the volume in which electron-hole pairs are created, *i.e.* the generation volume. This can be done analytically or numerically by Monte- Carlo simulation, in this thesis we have used CASINO software for this purpose [144].

A.2 Transmission Electron microscopy (TEM)

Transmission electron microscopy (TEM) is a microscopy technique whereby a beam of electrons is transmitted through an ultra-thin specimen, interacting with the specimen as it passes through. An image is formed from the interaction of the electrons transmitted through the specimen; the image is magnified and focused onto an imaging device, such as a fluorescent screen, on a layer of photographic film, or to be detected by a sensor such as a CCD camera.

TEMs are capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons. This enables the instrument's user to examine fine detail (even as small as a single column of atoms, which is thousands of times smaller than the smallest resolvable object in a light microscope). TEM forms a major analysis method in a wide range of scientific fields, in both physical and biological sciences. TEMs find application in cancer research, virology, materials science as well as pollution, nanotechnology, and semiconductor research.

TEM image contrast is due to absorption and/or crystallographic diffraction of electrons in the material which vary with thickness and composition of the material. Alternate modes of use allow for the TEM operator to observe modulations in chemical identity, crystal orientation, electronic structure and sample induced electron phase shift as well as the regular absorption based imaging.

From the top down, the TEM consists of an emission source, which may be a tungsten filament or a lanthanum hexaboride (LaB_6) source. For tungsten, this will be of the form of either a hairpin-style filament, or a small spike-shaped filament. LaB_6 sources utilize small single crystals. By connecting this gun to a high voltage source (typically ~100–300 kV) the gun will, given sufficient current, begin to emit electrons either by thermionic or field electron emission into the vacuum. This extraction is usually aided by the use of a Wehnelt cylinder. Once extracted, the upper lenses of the TEM allow for the formation of the electron probe to the desired size and location for later interaction with the sample.

Other possibility is to use a Field Emission Gun (FEG) to produce an electron beam that is smaller in diameter, more coherent and with up to three orders of magnitude greater current density or brightness than can be achieved with conventional thermionic emitters such as tungsten or lanthanum hexaboride. A field emission gun is a type of electron gun in which a sharply pointed Müller-type emitter is held at several kilovolts negative potential relative to a nearby electrode, so that there is sufficient potential gradient at the emitter surface to cause field electron emission. Emitters are either of cold-cathode type, usually made of single crystal tungsten sharpened to a tip radius of about 100 nm, or of the Schottky type, in

which thermionic emission is enhanced by barrier lowering in the presence of a high electric field. Schottky emitters are made by coating a tungsten tip with a layer of zirconium oxide, which has the unusual property of increasing in electrical conductivity at high temperature.

Manipulation of the electron beam is performed using two physical effects. The interaction of electrons with a magnetic field will cause electrons to move according to the right hand rule, thus allowing for electromagnets to manipulate the electron beam. The use of magnetic fields allows for the formation of a magnetic lens of variable focusing power, the lens shape originating due to the distribution of magnetic flux. Additionally, electrostatic fields can cause the electrons to be deflected through a constant angle. Coupling of two deflections in opposing directions with a small intermediate gap allows for the formation of a shift in the beam path, this being used in TEM for beam shifting, subsequently this is extremely important for STEM. From these two effects, as well as the use of an electron imaging system, sufficient control over the beam path is possible for TEM operation. The optical configuration of a TEM can be rapidly changed, unlike that for an optical microscope, as lenses in the beam path can be enabled, have their strength changed, or be disabled entirely simply via rapid electrical switching, the speed of which is limited by effects such as the magnetic hysteresis of the lenses.

The lenses of a TEM allow for beam convergence, with the angle of convergence as a variable parameter, giving the TEM the ability to change magnification simply by modifying the amount of current that flows through the coil, quadrupole or hexapole lenses. The quadrupole lens is an arrangement of electromagnetic coils at the vertices of the square, enabling the generation of a lensing magnetic fields, the hexapole configuration simply enhances the lens symmetry by using six, rather than four coils.

Typically a TEM consists of three stages of lensing. The stages are the condensor lenses, the objective lenses, and the projector lenses. The condensor lenses are responsible for primary beam formation, whilst the objective lenses focus the beam that comes through the sample itself (in STEM scanning mode, there are also objective lenses above the sample to make the incident electron beam convergent). The projector lenses are used to expand the beam onto the phosphor screen or other imaging device, such as film. The magnification of the TEM is due to the ratio of the distances between the specimen and the objective lens' image plane. Additional quad or hexapole lenses allow for the correction of asymmetrical beam distortions, known as astigmatism.

It is noted that TEM optical configurations differ significantly with implementation, with manufacturers using custom lens configurations, such as in spherical aberration corrected instruments, or TEMs utilizing energy filtering to correct electron chromatic aberration. Much deeper understanding of all the knowledge and phenomena associated with TEM can

be obtained in literature, we do strongly recommend reading the textbook of D.B. Williams & C.B. Carter [131].

In this work, we will extensively use TEM-related techniques for the nano-structural and chemical analysis of diamond interfaces in a variety of devices. A brief introduction of the previously mentioned TEM-related techniques will be presented by following the next index:

TEM is a tool that provides a wide variety of techniques; this field is so extensive that we decide to present just a few key ideas. We refer to the previously mentioned literature [131] to expand knowledge in each specific technique.

High Resolution Electron Microscopy (HREM)

HREM is a TEM imaging mode that allows for direct imaging of the atomic structure of the sample consisting, mainly, in the imaging of an object by recording the 2D spatial wave amplitude distribution in the image plane (in analogy to a "classic" light microscope), the technique is also known as phase contrast TEM. At present, the highest point resolution realized in phase contrast TEM is around 0.05nm. At these small scales, individual atoms of a crystal and its defects can be resolved.

One of the difficulties with HRTEM is that image formation relies on phase contrast. In phase-contrast imaging, contrast is not necessarily intuitively interpretable, as the image is influenced by aberrations of the imaging lenses in the microscope. The largest contributions for uncorrected instruments typically come from defocus and astigmatism. The latter can be estimated from the so-called Thon ring pattern appearing in the Fourier transform modulus

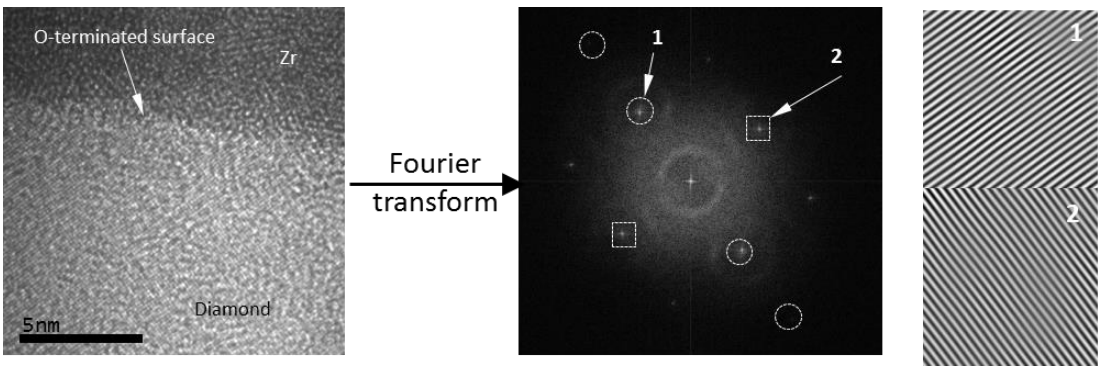

Figure 85: Diagram of the procedure for filtering HREM images from the original micrography (here, a diamond/Zr diode, directly obtained in a FEI Titan S/TEM). Fourier transform of image and inverse Fourier transform of spots labeled as 1 and 2 are also shown.

of an image of a thin amorphous film.

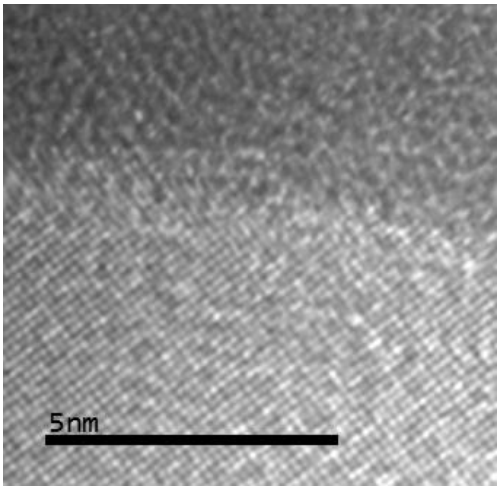

Figure 86: HREM-filtered image of **Figure 85**. The resulting final image is less noisy.

HREM images are formed by the confluence of electron beams scattered in different directions. To illustrate this, **Figure 87** shows an HREM image "as acquired" in a TEM. Fourier transform (an expression the image as a "sum" of frequencies; is the frequency-domain representation of the image) also show in **Figure 87**. If we do select the spots that are corresponding with an specific plane and we do the inverse Fourier transform, we obtain images that are consisting in an array of lines (that matches with the crystallographic planes we previously selected by choosing a pair of spots). To illustrate this, **Figure 87** shows inverse Fourier transforms of different couples of diffraction spots. Finally, if we select all the spots of the diffraction pattern (and proceed with the inverse Fourier transform) we obtain the HREM-filtered image as shown in **Figure 88**. This image is said to be filtered because white background that appears in **Figure 87** has been removed.

The contrast of a HRTEM image arises from the interference in the image plane of the electron wave with itself. Due to our inability to record the phase of an electron wave, only the amplitude in the image plane is recorded.

However, a large part of the structure information of the sample is contained in the phase of the electron wave. In order to detect it, the aberrations of the microscope (like defocus) have to be tuned in a way that converts the phase of the wave at the specimen exit plane into amplitudes in the image plane.

The interaction of the electron wave with the crystallographic structure of the sample is complex, but a qualitative idea of the interaction can readily be obtained. Each imaging electron interacts independently with the sample. Above the sample, the wave of an electron can be approximated as a plane wave incident on the sample surface. As it penetrates the sample, it is attracted by the positive atomic potentials of the atom cores, and channels along the atom columns of the crystallographic lattice. At the same time, the interaction between the electron wave in different atom columns leads to Bragg diffraction.

The exact description of dynamical scattering of electrons in a sample not satisfying the weak phase object approximation (WPOA), which is almost all real samples, still remains the holy grail of electron microscopy. However, the physics of electron scattering and

electron microscope image formation are sufficiently well known to allow accurate simulation of electron microscope images.

Scanning Transmission Electron Microscopy (STEM)

STEM is a TEM imaging mode distinguished from conventional transmission electron microscopes (CTEM) by focusing the electron beam into a narrow spot which is scanned over the sample in a raster. The rastering of the beam across the sample makes these microscopes suitable for analysis techniques such as mapping by energy dispersive X-ray (EDX) spectroscopy, electron energy loss spectroscopy (EELS) and annular dark-field imaging (ADF). These signals can be obtained simultaneously, allowing direct correlation of image and quantitative data.

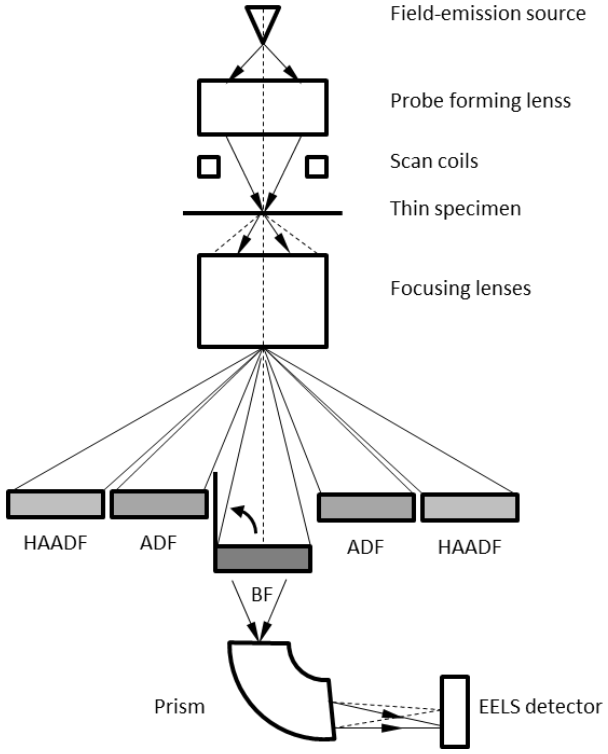

Figure 87: Scheme of the procedure for TEM-based ADF, HAADF and energy-loss spectroscopy in scanning-transmission (STEM).

By using a STEM and a high-angle detector (see **Figure 89**) it is possible to form atomic resolution images where the contrast is directly related to the atomic number (z-contrast image). This is in contrast to the conventional high resolution electron microscopy technique, which uses phase-contrast, and therefore produces results which need interpretation by simulation.

Annular Dark Field & High Angle Annular Dark Field (ADF-HAADF)

An annular dark field detector collects electrons from an annulus around the beam, sampling far more scattered electrons than can pass through an objective aperture. This gives an advantage in terms of signal collection efficiency and allows the main beam to pass to an EELS detector, allowing both types of measurement to be performed simultaneously. Annular dark field imaging is also commonly performed in parallel with Energy-dispersive X-ray spectroscopy acquisition, and can be also done in parallel to bright-field (STEM) imaging.

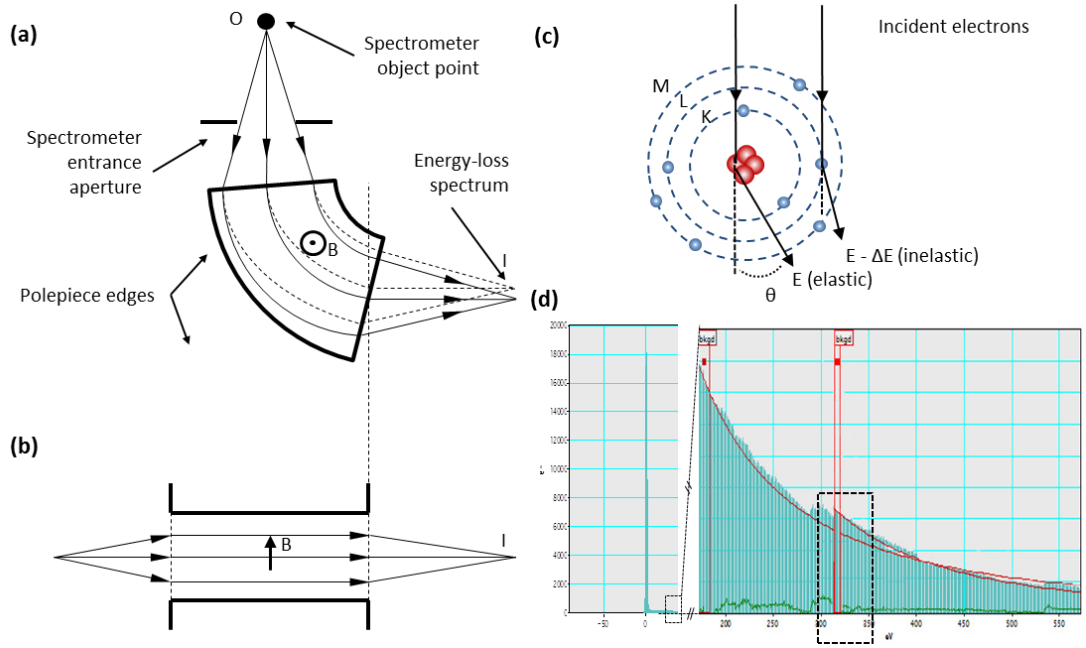

Figure 88: Dispersive and focusing properties of a magnetic prism (a) in a plane perpendicular to the magnetic field and (b) parallel to the field. Solid lines represent zero-loss electrons (E=0); dashed lines represent those that have lost energy during transmission. (c) Basic diagram of the physical nature of EELS spectra. (d) EELS spectra of diamond, used to compare the intensity of the EELS signal near the zero loss peak (left) with respect to the core loss region (right)

An annular dark field image formed only by very high angle, incoherently scattered electrons — as opposed to Bragg scattered electrons — is highly sensitive to variations in the atomic number of atoms in the sample (Z-contrast images).

Electron Energy Loss Spectroscopy (EELS)

In electron energy loss spectroscopy (EELS) a material is exposed to a beam of electrons with a known, narrow range of kinetic energies. Some of the electrons will undergo inelastic scattering, which means that they lose energy and have their paths slightly and randomly deflected. The amount of energy loss can be measured via an electron spectrometer and interpreted in terms of what caused the energy loss.

Inelastic interactions include phonon excitations, inter and intra band transitions, plasmon excitations, inner shell ionizations, and Cherenkov radiation. The inner-shell ionizations are particularly useful for detecting the elemental components of a material (see **Figure 90** (c)). For example, one might find that a larger-than-expected number of electrons comes through the material with 285 eV less energy than they had when they entered the material. This is approximately the amount of energy needed to remove an inner-shell electron from a carbon

atom, which can be taken as evidence that there is a significant amount of carbon present in the sample. With some care, and looking at a wide range of energy losses, one can determine the types of atoms, and the numbers of atoms of each type, being struck by the beam.

The scattering angle (that is, the amount that the electron's path is deflected) can also be measured, giving information about the dispersion relation of whatever material excitation caused the inelastic scattering.

Figure 90 (a) and (b) shows schematic diagram of dispersive and focusing properties of a magnetic prism, here used to illustrate EELS experiments. A typical electron energy loss spectrum is shown in **Figure 92** (d), it consists of three parts:

- **Zero-loss peak at 0 eV:** It mainly contains electrons that still have the original beam energy E_0, i.e., they have only interacted elastically or not at all with the specimen. In thin specimens, the intensity of the zero-loss beam is high, so that damage of the CCD chip can occur. Since there is no useful information in it, the zero-loss beam is often omitted during spectrum collection.
- **Low-loss region (< 100eV):** Here, the electrons that have induced plasmon oscillations occur. Since the plasmon generation is the most frequent inelastic interaction of electron with the sample, the intensity in this region is relatively high. Intensity and number of plasmon peaks increases with specimen thickness.
- **High-loss or core loss region (> 100eV):** For the ionization of atoms, a specific minimum energy, the critical ionization energy E_C or ionization threshold, must be transferred from the incident electron to the expelled inner-shell electron, which leads to ionization edges in the spectrum at energy losses that are characteristic for an element. Thus, EELS is complementary to X-ray spectroscopy, and it can be utilized for qualitative and quantitative element analysis as well. In particular, the detection of light elements is a main task of EELS.

Compared to the plasmon generation, the inner-shell ionization is a much less probable process, leading to a low intensity of the peaks. In the high-loss region, the amount of inelastically scattered electrons drastically decreases with increasing energy loss, thus small peaks are superimposed on a strongly decreasing background (s. spectrum). Because of the low intensity, the representation of the high-loss region is often strongly enhanced (here: intensity gap at about 220 eV).

The critical ionization energy E_C is sensitive to the chemical situation of the element: e.g., dashed-squared area on **Figure 90** (d) shows amorphous C shape, whose peaks are shifted in respect to that of graphite. Moreover, the ionization process may take more energy than E_C, and therefore there also is intensity located after the corresponding edge. Actually, this

region, designated as ELNES (Energy-Loss Near-Edge Structure), mirrors the DOS and provides information about the bonding situation. Modulations further away from the ionization edge contain information about interatomic distances and coordination (EXELFS, Extended Energy-Loss Fine Structure).

A lot of information is present in EELS spectrum. The energy resolution (below 1 eV) is much better than in X-ray spectroscopy, and as a result more structural information can be obtained from the fine structure in EELS. For many questions, it is important to get this information with a high local resolution. Such mappings can be done with two different methods:

1. STEM with EELS

In STEM mode, a region of the sample is selected, and an EELS is measured on each spot of the defined grid (serial measurement).

2. EFTEM using an energy filter

An energy range is selected, and an energy-filtered image is recorded with electrons of this energy (parallel measurement).

Some EEL spectra are available in [145].

ANNEX II: Semiconductor interfaces

A.I Metal – Semiconductor interfaces

When metal makes contact with a semiconductor, a potential barrier is generated at the metal-semiconductor interface (see **Figure 91**). In **Figure 91**, the "metal work function" $q \cdot \phi_m$ is the energy difference between the vacuum level and the Fermi level E_F. This quantity is equal to $q \cdot (\chi + \phi_{sc})$ in the semiconductor, where $q\chi$ is the electron affinity[24] measured from the bottom of the conduction band E_C to the vacuum level and $q\,\phi_{sc}$ is the energy difference between E_C and the Fermi level (note that this value can change with doping). The potential difference between two work functions is called the "contact potential" $\phi_m - (\chi + \phi_{n,p})$.

As the gap distance decreases, the electric field in the gap increases and an increasing charge is built up at the metal surface. An equal and opposite charge must exist in the semiconductor depletion region (this is similar to the academic case of a p-n junction). When the gap is small enough to be comparable to interatomic distances, it becomes transparent to electrons and we obtain the limiting case. The barrier height is simply the difference between the metal work function and the electron affinity of the semiconductor.

The shape of this barrier is responsible for controlling the current conduction as well as its capacitance behavior. Because of their importance in direct current and microwave applications and as intricate parts of other semiconductor devices, metal-semiconductor

[24] In solid state, electron affinity is defined as the energy obtained by moving an electron from the vacuum just outside the semiconductor to the bottom of the conduction band just inside the semiconductor. Electron does depend on the surface termination (crystal face, surface chemistry, etc) and, in certain circumstances, may become negative. This means that the material is an efficient cathode that can supply electrons to the vacuum with little energy loss.

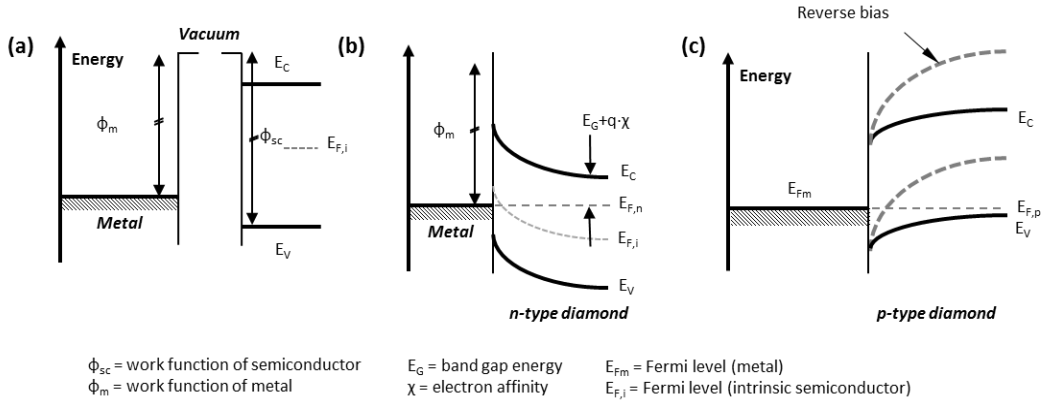

Figure 89: Energy-band diagrams of metal-semiconductors contacts. Metal and semiconductor in electrically isolated systems for an intrinsic semiconductor, (a) metal and n-type semiconductor, (b) Metal and p-type (dashed line means reverse bias)

contacts have been studied extensively. Specifically, they have been used as photodetectors, solar cells, gate electrode for MESFET, etc. Specially, the metal contact on heavily doped semiconductors forms an ohmic contact that is required for every semiconductor and device in order to pass current in and out of the device.

In practice, simple expressions for barrier heights, like $q\cdot\phi_{Bp0}=E_g- q(\phi_m-\chi)$, are never realized experimentally. This is mostly because the electron affinity of the semiconductor and the work function of the metal have to be established; additionally the values of $q\phi_m$ are generally very sensitive to surface contamination.

According to the difference of work functions, a Metal-Semiconductor (MS) junction will be an ohmic contact or a Schottky contact (acting as rectifier). In the case of a p-type semiconductor (boron-doped diamond), an ohmic contact is formed when the metal work function is higher than the semiconductor one, whereas a Schottky contact is obtained when the metal work function is lower. This is well explained by the Schottky-Mott theory stating that the band alignment of a MS junction is related to a charge transfer from one side to other aiming to force the Fermi levels to coincide.

To simplify the discussion, we will assume that the metal work function is equal to the semiconductor work function (the flat band condition is satisfied for a zero bias voltage). We will also assume that the semiconductor is p-type, as we will work only with p-type diamond. It will not be the case for low doped diamond. Finally, the voltage V is positive when the gate metal is positively biased using the ohmic contact as a reference.

The band alignment of a metal/semiconductor (p-type in our case) interface will depend on the relative height of ϕ_m and ϕ_{sc} as follows:

- **$\phi_m > \phi_{sc}$:** in this case, the band alignment at thermal equilibrium leads to an upward semiconductor band bending at the interface (related to a hole accumulation). If such junction is biased (V) so that holes flow from the semiconductor to the metal, they encounter no barrier. Moreover, in reverse direction, the upward band bending related to hole accumulation in the interface, behaves like an anode (holes source), which will provide a copious supply of holes. The resistance (R) of the semiconductor will therefore determine the electrical current via the ohmic law V = I·R, thus conforming an ohmic contact.
- **$\phi_m < \phi_{sc}$:** here, the band alignment gives rise to a build-in potential barrier, the so-called "Schottky barrier" ϕ_b at the interface and a downward semiconductor band bending. So, that when a metal is brought into full contact with a semiconductor, the conduction and valence bands of the semiconductor at the surface are brought into a definite energy relationship with the Fermi level in the metal. This is similar to the depletion layer of a metal-semiconductor contact that of the one-sided abrupt p-n junction.

Once this relationship is established, it serves as a boundary condition to the solution of the Poisson equation (**Eq. 25**) in the semiconductor, which proceeds in exactly the same manner as in a p-n junction.

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon} \qquad \textbf{Eq. 21}$$

Figure 94 shows the energy-band diagrams for metal on p-type material under different biasing conditions. In this case, and as stated by the Schottky-Mott theory, the potential barrier arises because of a charges transfer from the semiconductor (higher Fermi level) to the metal. The charges transferred (holes, in boron-doped diamond) leave behind uncompensated acceptor atoms and furthermore a positive charges accumulation on the surface of the metal (extra conduction carrier contained within a Thomas-Fermi screening distance of around 0.5Å [85]), the band alignment involves a downward semiconductor band bending (diffusion potential V_{d0}) related to the negatively charged acceptor atoms in the depletion region and an abrupt barrier in the metal side ϕ_b.V_{d0} is the potential barrier that encounters free carrier diffusing towards the metal whereas ϕ_b inhibits carrier injection from the metal to the semiconductor. The ideal Schottky Barrier Height (SBH) is defined by the Mott equation as $\phi_b = E_g/\ q-(\phi_m-\chi)$:

- Under zero bias and for a slightly doped semiconductor (Fermi level close to acceptor level), $qV_{d0} \approx q\ \phi_b - E_a$, where E_a is the acceptor ionization energy (**Figure 92** (a))

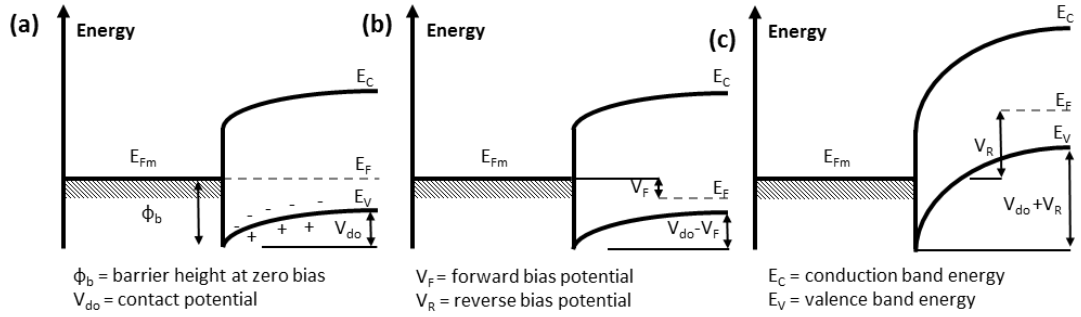

Figure 90: Energy-band diagrams of metal-semiconductors contacts (for p-type semiconductor). Metal and semiconductor (a) in thermal equilibrium (b) forward bias (decrease the barrier) and (c) reverse bias (increase the barrier).

- Under applied bias V, this potential becomes $qV_d = qV_{d0} + qV$. Accordingly, the barrier V_d is lower under forward bias, thus favoring a carrier injection from the semiconductor to the metal (**Figure 92** (b))
- Reverse situation occurs when diffusion potential increases versus reverse bias V_r. The electrical current in this case is induced by a carrier injection from the metal to the semiconductor (**Figure 92** (c)).

The Schottky effect

A simple analytic model for the metal-semiconductor junction is based on the full depletion approximation, obtained by assuming that the semiconductor is full depleted over a distance W (called the depletion region). Such depletion width can be expressed as a function of the applied voltage. As the semiconductor is depleted of mobile carriers within the depletion region, the charge density in that region is due to ionized impurities, this yield to a charge density in the semiconductor that has to be balanced by the charge in the metal (Q_M). We can assume full ionization, so that the ionized impurities density equals the acceptor density N_A (please, take into account that we are focusing in p-type diamond). So, if charges in the semiconductor are exactly balanced by charges in the metal, no electric field exists except around the metal-semiconductor interface (it is limited to the depletion region).

If we now assume that the density of free carriers is very high in a metal, the thickness of the charge layer in the metal is very thin. Therefore, the potential across the metal is several orders of magnitude smaller than across the semiconductor (even though the total amount of charges is the same in both regions). The total potential difference across the semiconductor equals the built-in potential in thermal equilibrium and is further reduced or increased by the applied voltage. This provides the following expression for the depletion layer width:

$$W = \sqrt{\frac{2\varepsilon_s(\psi_{bi} - V)}{qN_A}} \qquad \textbf{Eq. 22}$$

This kind of structure also has an associated capacitance that can be calculated by taking the derivative of the charge with respect of the applied voltage.

This picture implies that image charges builds up in the metal electrode of a M-S junction as carriers approach the M-S interface. The potential associated with these charges reduces the effective barrier height. This barrier reduction tends to be rather small compared to the barrier height itself. Nevertheless this barrier reduction is of interest since it depends on the applied voltage and leads to a voltage dependence of the reverse bias current. Note that this barrier lowering is only experienced by a carrier while approaching the interface and will therefore not be noticeable in a capacitance-voltage measurement. If we include the barrier lowering in a n-type semiconductor, the plot of **Figure 93** is obtained.

Figure 93 shows the energy band diagram obtained using the full-depletion approximation, the potential reduction experienced by electrons, which approach the interface and the resulting conduction band edge. A rounding of the conduction band edge can be observed at the metal semiconductor interface as well as a reduction of the height of the barrier.

The calculation of the barrier reduction assumes that the charge of an electron close to the metal-semiconductor interface attracts an opposite surface charge, which exactly balances

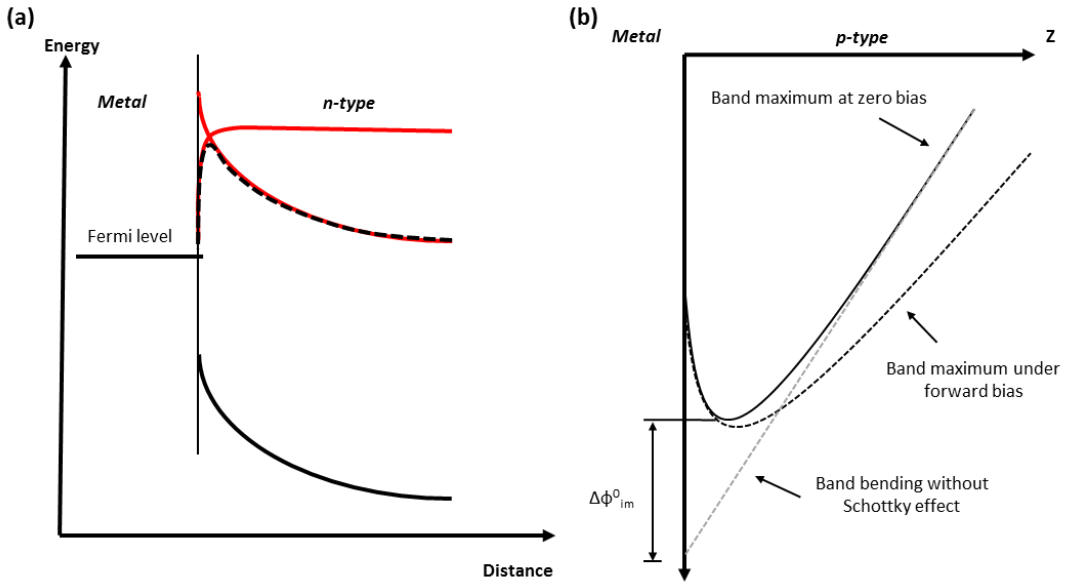

Figure 91: Energy band diagram for a metal/n-type semiconductor contact including the barrier lowering (a) and detail of the M-S interface for a p-type semiconductor.

the electron's charge so that the electric field surrounding the electron does not penetrate beyond this surface charge. The time to build-up the surface charge and the time to polarize the semiconductor around the moving electron are assumed to be much shorter than the transit time of the electron. This scenario is based on the assumption that there are no mobile or fixed charges around the electron as it approaches the metal-semiconductor interface.

Schottky barrier height and ideality factor

As previously spotted, when metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. The barrier heights of a metal-semiconductor system are, in general, determined by both: the metal work function and the interface states. A general expression of the barrier height can be obtained by following two assumptions:

(1) with intimate contact between the metal and the semiconductor, and with an interfacial layer of atomic dimensions, this layer will be transparent to electrons but can withstand potential across it.
(2) the interface states per unit area per energy at the interface are property of the semiconductor surface and are independent of the metal.

The interfacial layer will be assumed to have a thickness of a few angstroms and, therefore, will be essentially transparent to electrons.

With these assumptions, and with the requirement that the electric field in a metal-semiconductor interface must be perpendicular to the metal, since its surface is an equipotential, the "Schottky effect" appears as a consequence. Let's consider Coulomb interaction (force attraction) between a charge carrier located at a distance x in semiconductor and its mirror image charge at –x. This consideration affects the carrier injection from one side to the other by inducing a barrier variation and, accordingly, the SBH is reduced even at zero bias. Then, the Schottky barrier height (SBH) changes once a bias voltage is applied (even for an ideal junction) because of intrinsic mechanisms such as the image-force and furthermore due to the influence of imperfections in the junction area. Following the latter assumptions, the zero bias SBH $\phi^0{}_b$ is given by [68]:

$$\phi_b^0 = \phi_{b0} - \Delta\phi_{im}^0 \approx \phi_{b0} - \left(\frac{2q^3 N_A}{(4\pi)^2 \epsilon_S^3} V_{d0}\right)^{1/4} \quad \textbf{Eq. 23}$$

On the other hand, when the electric field increase in the junction area i.e. under a reverse bias, the built-in potential barrier is reduced thus favoring the carrier injection from the metal to the semiconductor. Note that in this situation, the carrier injection from the

semiconductor to the metal is inhibited by a high potential barrier (diffusion potential). Under forward bias V_f, the SBH is still bias-dependent and conversely to reverse case, it is higher than ϕ^0_b and the electrical current is defined by a carrier emission from the semiconductor to the metal. The bias dependence of SBH in the forward state is generally expressed as:

$$\phi_b(V_f) = \phi_{b0} + (1 - 1/n_{if})V_f \qquad \textbf{Eq. 24}$$

Where V_f is the voltage drop across the depletion layer, and n_{if} is a bias-independent parameter called "ideality factor" related to the Schottky effect only:

$$n_{if} = \left(1 - \frac{\Delta\phi^0_{im}}{4qV_{d0}}\right)^{-1} \approx \left[1 - \frac{1}{4q}\left(\frac{2q^3N_A}{(4\pi)^2\epsilon_s^3}\right)^{1/4}(V_{d0})^{-3/4}\right]^{-1} \qquad \textbf{Eq. 25}$$

The ideality factor tends towards unity for a high zero-bias diffusion potential and so for a high SBH. It has to be noticed that even for a low SBH, n_{if} is generally close to 1 for most of semiconductors. As example, for a p-type diamond doped at 10^{16}cm^{-3}, n_{if} is expected to be 1.005, 1.008, and 1.009 for respectively 2 eV, 1 eV, and 0.9 eV zero-bias barrier heights. Thus, the SBH should be less sensible (quasi constant barrier) to forward applied bias voltage if the image force is only considered.

However, the image force effect is generally not enough to explain the bias dependence of SBH. Indeed, the static dipoles and the states linked to the imperfections at MS interface also contribute to lower the SBH. The forward state is still described by the linear bias dependence mentioned above but the ideality factor is no longer related to the Schottky effect only. Under reverse bias, the SBH lowering is generally defined using the empirical expression:

$$\phi_b(V_r) = \phi_b^0 - \Delta\phi_{im} - \alpha E_m =$$

$$= \phi_b^0 - \left[\frac{2q^3N_A}{(4\pi)^2\epsilon_s^3}(V_{d0} + V_r)\right]^{\frac{1}{4}} - \alpha\left[\frac{2qN_A}{\epsilon_s}(V_{d0} + V_r)\right]^{1/2} \qquad \textbf{Eq. 26}$$

Where α is a constant supposed to be related to the density and depth of interface states. The bias dependence of the SBH mainly alters the reverse state since it increases the reverse current by continuously reducing the Schottky barrier height. However, a high reverse electric field in junction area induces carrier tunneling in the semiconductor, which can be the limiting transport mechanism and then define the electrical current.

A.2 Metal – Oxide – Semiconductor interfaces

As its name implies, a metal-insulator-semiconductor (MIS) structure is composed of a stack of a metal, an insulator (generally, an oxide) and a semiconductor. An ohmic contact acting as a reference is necessary for applying a voltage on the metal gate.

The **Figure 95** shows the band diagram of an ideal MIS structure with a 0V applied voltage. As specified above, metal and semiconductor have been chosen in order that the bands are flat. The different regimes of this ideal MIS capacitor can be described as a function of the applied bias voltage:

- When a negative voltage (V < 0) is applied to the metal gate, the bands (valence and conduction bands) of the semiconductor bend upward at the edge of the semiconductor. At this interface, the valence band is now closer to the Fermi level (see **Figure 95** (b)) than further in the semiconductor when the bands are flat. This band bending causes an accumulation of majority carriers (here holes) in the semiconductor near the SC/oxide interface, giving its name to the regime called accumulation.
- When a positive voltage (V > 0) is applied, the bands bend downward (see **Figure 95** (c)), a space charge region appears where the majority carriers are depleted. This is the depletion regime.
- When a larger positive voltage is applied, the bands bend downward more and

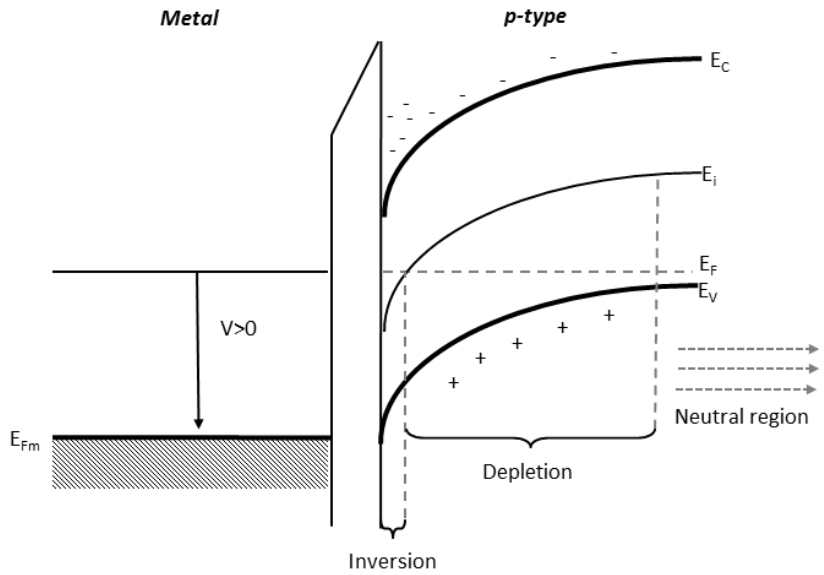

Figure 92: Band diagram of an ideal MOS capacitor under strong inversion.

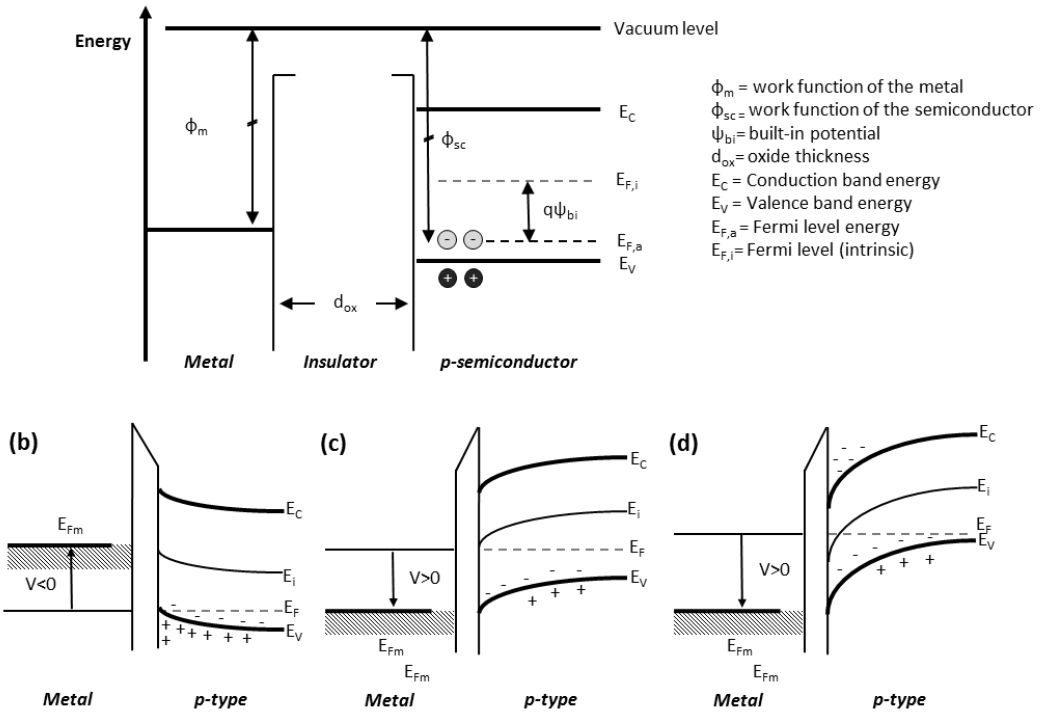

Figure 93: (a) Ideal metal-insulator energy band diagram in flat condition (0V applied voltage) for a p-type semiconductor. Same energy-band diagram under different operation regimes: (b) accumulation, (c) depletion) and (d) strong inversion.

more, until the Fermi level E_F reaches the intrinsic Fermi level E_i (E_i is the Fermi level for an intrinsic semiconductor, it lies at ~ $E_g/2$ in the gap far from the oxide/semiconductor interface). Conduction at the SC/oxide interface is no longer carried out by the holes but by the electrons which are more numerous than the holes in this region. The semiconductor is said locally inverted and this regime is called the weak inversion.

- By increasing further the voltage, the strong inversion regime is reached (see **Figure 95** (d)). The sheet density of electrons in the inversion layer is now larger than the density of holes in the neutral part of the semiconductor. Usually, no distinction is made between weak and strong inversion regime and what is often called inversion regime corresponds to strong inversion case defined here.

Here, we use energy-band diagram to introduce and highlighting the capacitance behavior of these structures under different bias. We have described different operations regimes, depending on the applied bias:

- V < 0 Accumulation
- V = 0 Flat band

- V > 0 Depletion
- V >> 0 Weak inversion of charge carriers
- V >>> 0 Strong inversion

A detail of the ideal band-diagram of a p-type semiconductor under strong inversion regime is presented in **Figure 94**. However, this is a simplified picture.

For a deep understanding of these interfaces, we have to introduce additional concepts (the surface space-charge region and the surface potential).

We also have to introduce the real phenomena that affects to the C(V) properties of MOS structures. Among them, the most critical are the interface traps and the oxide charges.

Surface space-charge region

For the sake of the simplicity, let's assume that the difference between the metal work function and the semiconductor work function is zero, $\phi_{ms} = 0$ In the particular case of Al metal and low-doped diamond substrate, this assumption is close to the real (ϕ_{Al} = 4.28eV, ϕ_{diam} = 3,9eV [146]), this is the case in previous chapters of this PhD dissertation.

With this condition, for a diamond Metal-Oxide-Semiconductor configuration, the following relation can be stablished with the help of **Figure 94**:

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{q} - \phi_p\right) = 0 \qquad \textbf{Eq. 27}$$

Being χ the diamond electron affinity and ϕ_p the Fermi potential with respect to the midgap and band edges. Now, by following the diagram of **Figure 95**, the hole concentration is given by:

$$p_p(x) = p_{p0} e^{\frac{-q\psi_p}{kT}} \qquad \textbf{Eq. 28}$$

To simplify, let's take $\beta = \frac{q}{kT}$. The potential $\psi_p(x)$ can be obtained by solving the one-dimensional Poisson equation $d^2\psi_p/dx^2 = -\rho(x)/\varepsilon$ where the total space-charge density is given by: $\rho(x) = q(N_D^+ - N_A^- + p_p - n_p)$ far from the surface, the charge neutrality must exist and: $N_D^+ - N_A^- = -p_{p0} + n_{p0}$ The resultant Poisson equation to be solved can be integrated, thus giving the relation between the electric field and the ψ_p potential.

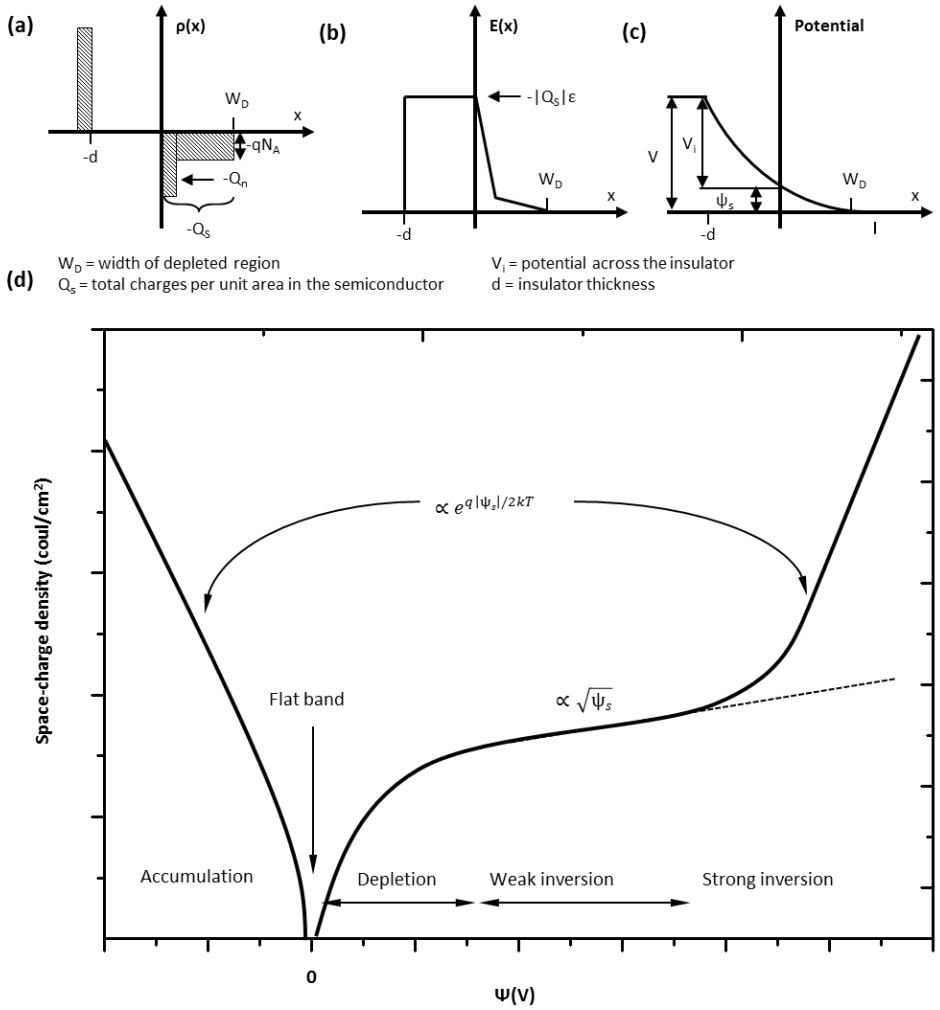

Figure 94: Charge distribution (a), electric-field distribution (b) and potential distribution relative to the bulk (c) of an ideal MOS capacitor (d) Schematic of the variation of space-charge density in a semiconductor as function of the surface potential for a p-type low-doped semiconductor

$$E^2 = \left(\frac{2kT}{q}\right)\left(\frac{qp_{p0}\beta}{2\varepsilon_s}\right)\left\{\left[e^{-\beta\psi_p} + \beta\psi_p - 1\right] + \frac{n_{p0}}{p_{p0}}\left[e^{\beta\psi_p} - \beta\psi_p - 1\right]\right\} \qquad \textbf{Eq. 29}$$

To simplify, we define the following abbreviations:

$$F = \sqrt{\left[e^{-\beta\psi_p} + \beta\psi_p - 1\right] + \frac{n_{p0}}{p_{p0}}\left[e^{\beta\psi_p} - \beta\psi_p - 1\right]} \geq 0 \qquad \textbf{Eq. 30}$$

And the Debye length of holes, defined as $L_D = \sqrt{\varepsilon_s / q p_{p0} \beta}$. Thus, the electric field at the surface is:

$$E = \pm \frac{\sqrt{2}kT}{qL_D} F \qquad \textbf{Eq. 31}$$

From this surface field, we can deduce the total space charge per unit area by applying Gauss law: $Q_s = -\varepsilon E$, the resulting curve is plotted in **Figure 96**, where a typical variation of the space-charge density Q_s as a function of the surface potential ψ_s for a low doped p-type semiconductor at room temperature is shown. Note that, for negative ψ_s, Q_s is positive and it corresponds to the accumulation region. The function F is dominated by first term of **Eq. 30**, that is, $Q_S \propto e^{q|\psi_s|/2kT}$. For ψ_s = 0, we have the flat-band condition and Q_s = 0. For increasing ψ_s, Q_s is negative and we have depletion and weak-inversion cases. The function F is now dominated by the second term, that is $Q_S \propto \sqrt{\psi_s}$. For higher values, we have the strong inversion case with the function F dominated by the fourth term, that is $Q_S \propto e^{q|\psi_s|/2kT}$.

Surface potential and C(V) regimes on MOS structures

Several parameters are involved in the MOS structure operating, such as doping and thickness of the semiconductor, thickness, permittivity and charge of the oxide, as well as temperature. We will use the approach proposed by Gilbert Vicent [147], very useful to understand MOS operation as well as the influence of each fore-mentioned parameter on the MOS polarization, more details and fundamentals of the qψ theory can be found in literature [148].

Figure 97 (a) summarizes the mentioned MOS parameters and shows the energy-band diagram at the interface of a p-type semiconductor/insulator. The potential $q\psi_p(x)$ is measured with respect to the intrinsic Fermi level in the bulk at a distance x from the insulator-semiconductor interface. The surface potential $\psi_s=\psi_p(0)$ is the potential at the interface, corresponding to the band curvature.

As the metal/oxide/semiconductor (MOS) structure acts as a capacitor, the C(V) characteristic reveals the operating regimes that can be reached. An overview of the general trend of capacitance versus gate voltage characteristic of a perfect MOS structure is shown in **Figure 97** (b). When applying a negative voltage, the MOS structure is under accumulation

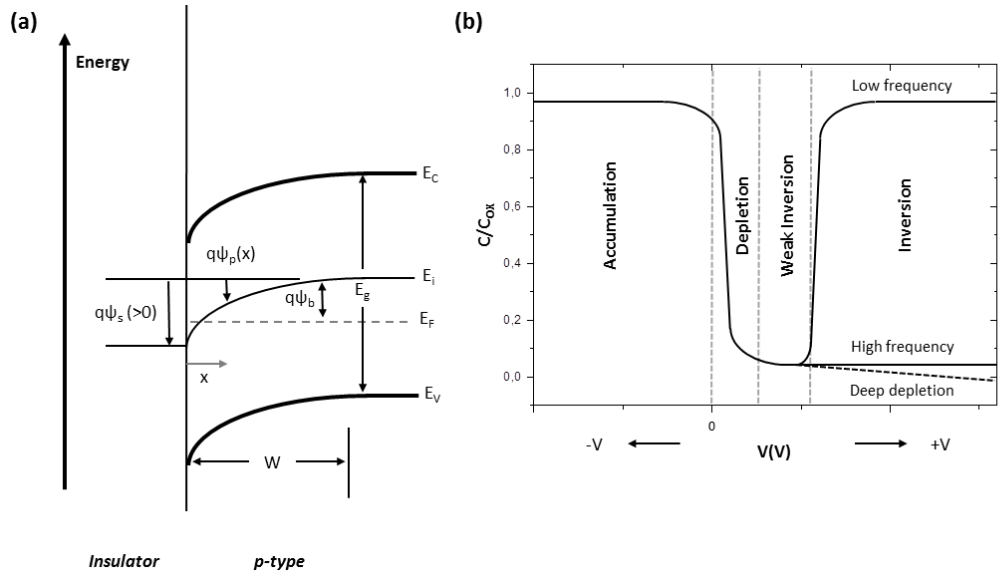

Figure 95: (a) qψ diagram for a real insulator-semiconductor (p-type) contact and (b) theoretical MOS capacitor C(V) characteristic showing the different operating regimes.

regime and can be compared to a planar capacitor composed of metal/oxide/accumulation layer. In this regime, the capacitance is almost flat and equal to the oxide capacitance: $C = C_{ox} = \varepsilon_{ox}S/d_{ox}$, where S is the MOS capacitor area.

When applying a small positive voltage, a depleted region starts to appear in the SC from the oxide interface: the structure is in the depletion regime. While the voltage is increasing, the width of the space charge region (WSCR) of the depleted region increases and so, the corresponding capacitance C_D decreases. The resultant capacitance of the whole structure is composed of the oxide capacitance C_{ox} in series with the depleted region capacitance CD such as: $1/C(V) = 1/C_{ox} + 1/C_D(V)$.

Consequently, as C_{ox} is a constant value, the total capacitance C(V) decreases as the voltage bias increases. If a larger positive voltage is applied, the structure should be theoretically in weak inversion and then in strong inversion. Three cases can be distinguished:

- *Low frequency case of inversion:* In strong inversion regime (called usually inversion), the measured capacitance versus bias voltage increases until reaching the oxide capacitance value due to the presence of minority carriers at the interface. In fact, the structure is again comparable to a planar capacitance composed of the metal/oxide/inversion layer. For a MOS capacitor, this regime needs a minority carriers (here, electrons) generation mechanism to be present. This can be provided by thermal (or optical) generation of electron-hole pairs in the neutral part of the

semiconductor by intrinsic level or by mid gap deep level. Besides, thermal generation depends on the band gap value (which is large for diamond). The measurement frequency must therefore be very low, typically lower than 1 Hz for silicon (which is a small band gap SC compared to diamond), in order that the charges could follow the a.c signal. This is the low frequency case.

- *High frequency case of inversion:* If the frequency is too high, the recombination-generation rates of minority carriers can not follow the a.c signal variation and lead to charge exchange with the inversion layer. This last stays unchanged and no increase of the capacitance is observed. Instead the capacitance measured stays constant: this is the high frequency case of inversion.
- *Deep depletion:* If a high measurement frequency is combined with a quick V_G sweeping rate (it is commonly admitted that 1 hour, to sweep from accumulation to inversion, can be quick for a good semiconductor), the inversion layer cannot be formed and instead, the depletion layer continues to extend in the semiconductor (even if ψ_s is larger than $2\psi_b$). In this case, the capacitance will continue to decrease. This regime is a non-equilibrium state.

Thus, particular attention has to be paid to the measurement frequency depending on the semiconductor used. In the case of diamond, due to its wide band gap, very low frequency (<<< 1Hz) will be necessary to observe low frequency inversion, if no other minority carrier generation source is used. Therefore, only deep depletion is expected in diamond. Finally, charges and interfaces states affects experimental C(V) characteristics:

- Difference between the work function of metal/SC and fixed charges in the oxide will shift the C(V) characteristic.
- Mobile charges in the oxide are responsible for an hysteresis behavior.
- Interface states can affect C(V) characteristic in several ways, depending on the interface state density.

Further details of the C(V) regimes and MOS characterization techniques employed during this thesis can be consulted in literature [100].

A.3 MOS Field Effect Transistors

A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If

dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a "+" sign after the type of doping.

Structure and channel formation

If the MOSFET is an n-channel or nMOS FET, then the source and drain are "n^+" regions and the body is a "p" region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are "p^+" regions and the body is a "n" region. The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

The occupancy of the energy bands in a semiconductor is set by the position of the Fermi level relative to the semiconductor energy-band edges. As described above, and shown in the figure, with sufficient gate voltage, the valence band edge is driven far from the Fermi level, and holes from the body are driven away from the gate. At larger gate bias still, near the semiconductor surface the conduction band edge is brought close to the Fermi level, populating the surface with electrons in an inversion layer or n-channel at the interface between the p region and the oxide. This conducting channel extends between the source and the drain, and current is conducted through it when a voltage is applied between the two electrodes. Increasing the voltage on the gate leads to a higher electron density in the inversion layer and therefore increases the current flow between the source and drain.

For gate voltages below the threshold value, the channel is lightly populated, and only a very small subthreshold leakage current can flow between the source and the drain.

Modes of operation

When a negative gate-source voltage (positive source-gate) is applied, it creates a p-channel at the surface of the n region, analogous to the n-channel case, but with opposite polarities of charges and voltages. When a voltage less negative than the threshold value (a negative voltage for p-channel) is applied between gate and source, the channel disappears and only a very small subthreshold current can flow between the source and the drain.

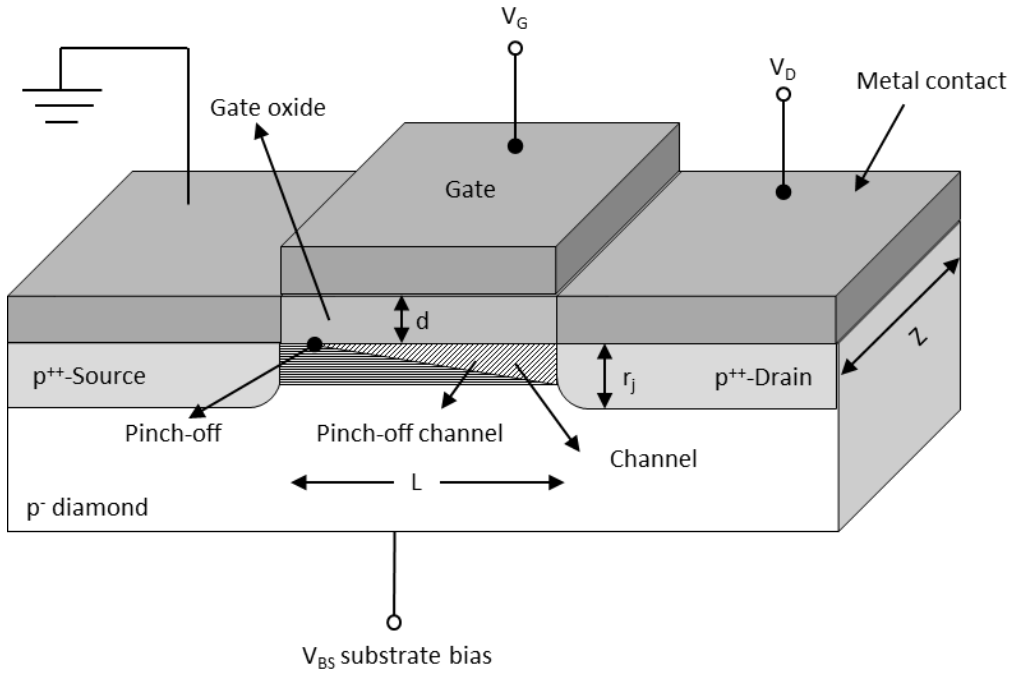

Figure 96: Schematic diagram of the architecture of a conventional MOSFET. In the particular case of diamond, Source and Drain are p++ doped while substrate is p- doped. This schematic is also showing two channel cases: conventional lineal channel and pinch-off channel.

The device may comprise a Silicon On Insulator (SOI) device in which a buried oxide (BOX) is formed below a thin semiconductor layer. If the channel region between the gate dielectric and a BOX region is very thin, the very thin channel region is referred to as an ultrathin channel (UTC) region with the source and drain regions formed on either side thereof in and/or above the thin semiconductor layer. Alternatively, the device may comprise a semiconductor on insulator (SEMOI) device in which semiconductors other than silicon are employed. Many alternative semiconductor materials may be employed.

When the source and drain regions are formed above the channel in whole or in part, they are referred to as raised source/drain (R_{SD}) regions.

The gate contact is, in fact, a MOS capacitor that shows three different operation regimes depending on the Gate-to-Bulk voltage (V_{GB}). In the conventional case of p-type substrate (n-type conductivity), these regimes are known as:

> **Accumulation ($V_{GB}<0$):** Accumulation occurs when one applies a voltage less than the flat-band voltage ($V_{GB}=0$). The negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Only a small amount of band

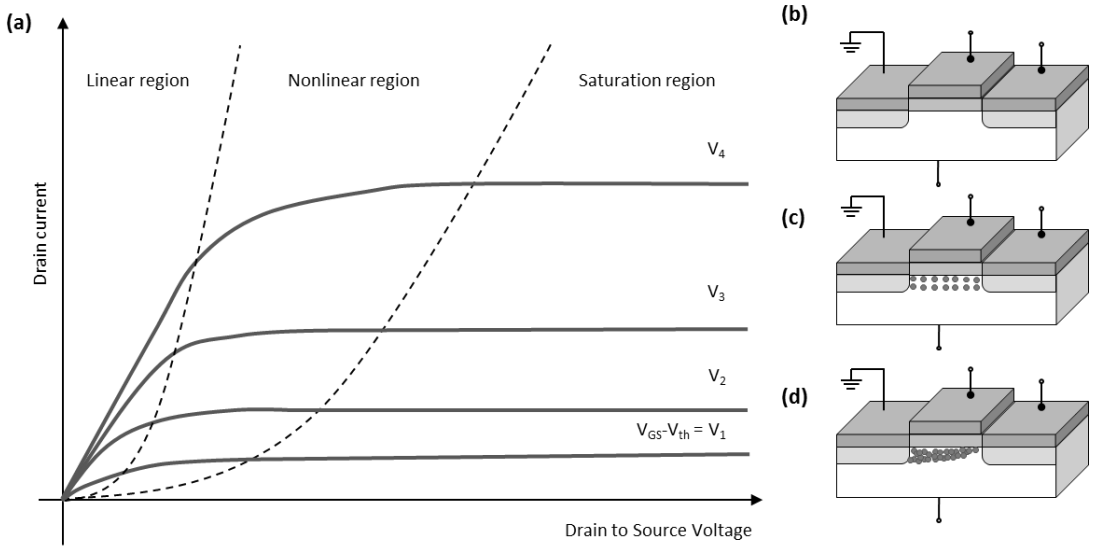

Figure 97: Shape of typical I_D-V_{DS} curves in a MOSFET for different V_{GS}-V_{th} values (a) and schematic of a MOSFET in cut-off (b), linear (c) and saturation region (d).

bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide.

Depletion (V_{GB}>0): As a more positive voltage than the flat-band voltage is applied, a negative charge builds up in the semiconductor (but it was p-type semiconductor!). Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage.

Inversion (V_{GB}>>0): As the potential across the semiconductor increases beyond twice the bulk potential, another type of negative charge emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increases the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential.

The electronic channel created by using this structure can be controlled with source and drain contacts, thus conforming a classic MOSFET structure. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate. In

the less common depletion mode MOSFET, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and conductivity is decreased by application of a field that depletes carriers from this surface layer.

For now, let's assume the channel carriers are electrons (n-channel device). A common MOSFET is a four-terminal device that consists of a p-type semiconductor substrate into which two n^+-regions, the source and drain, are formed, usually by ion implantation. The gate dielectric is formed by thermal oxidation and the metal contact on the insulator is called gate. The basic device parameters are the channel length L (which is the distance between the two metallurgical junctions), the channel width Z, the insulator thickness d, the junction depth r_j, and the substrate doping N_A (N_D if p-doping).

The source contact will be used as the voltage reference throughout this thesis. When ground or a low voltage is applied to the gate, the main channel is shut off, and the source-to-drain electrodes correspond to two p-n junctions connected back to back. When a sufficiently large positive bias is applied to the gate so that a surface inversion layer (or channel) is formed between the two n^+-regions, the source and the drain are then connected by a conducting surface n-channel through which a large current can flow. The conductance of this channel can be modulated by varying the gate voltage. The back-surface contact (or surface contact) can be at the reference voltage or reverse biased; this substrate voltage will also affect the channel conductance.

When a voltage is applied across the source-drain contacts, the MOS structure is in a nonequilibrium condition; that is, the minority-carrier (electron in this case) quasi-Fermi level E_F is lowered from the equilibrium Fermi level, which leads the MOSFET to operate various regions:

> **Linear region:** in which the channel acts as a resistor, so drain current is proportional to drain voltage. Strong inversion of the substrate.
>
> **Nonlinear region:** by increasing the drain voltage, the current deviates from a linear relationship, it eventually reaches to a point at which the inversion charge at the drain is reduced to nearly zero (this location is called the "pinch-off" point).
>
> **Saturation region/active mode:** beyond the previously discussed drain bias, the drain current remains essentially the same. Charge carriers are strongly attracted, which provokes channel deformation.

Concerning the bulk semiconductor, physical properties of Si do not allow building efficient MOSFET for power electronics applications (generally insulated gate bipolar transistor is preferred but also limited to 4 kV). MOSFET based on other semiconductors, like III-V compounds or SiC, are progressing but the performances of such devices are not

competitive with Si devices and anyway will be always lower than that expected for diamond based MOSFET [94]. The main problem to fabricate a MOS structure is to achieve the semiconductor oxide interface with a sufficiently low interface states density. In that case, the different regimes of the MOS can be controlled: accumulation of majority carriers, depletion, deep depletion, or inversion of carrier (minority carrier density larger than majority carrier density at the interface).

Bibliography

1. Jakubowski, L.Ł.a.A., *History of Semiconductors.* Journal of telecommunications and information technology, 2010. **1**.
2. Busch, G., *Early history of the physics and chemistry of semiconductors – from doubts to fact in a hundred years".* Eur. J. Phys., 1989. **10**: p. 254-263.
3. F. Laeri, F.S., U. Simon, and M. Wark, *Host-Guest-Systems Based on Nanoporous Crystals.* Weinheim: Wiley, 2003: p. 435-436.
4. T. K. Sarkar, R.M., A. A. Oliner, M. Salazar-Palma, and D. L. Sengupta, *The History of Wireless.* Hoboken: Wiley, 2006.
5. Mönch, W., *Semiconductor Surfaces and Interfaces.* Berlin-Heidelberg: Springer, 2001.
6. L. Hoddeson, E.B., J. Teichmann, and S. Weart, *Out of the Crystal Maze: Chapters in the History of Solid State Physics.* New York: Oxford University Press, 1992.
7. Lojek, B., *History of Semiconductor Engineering.* Berlin-Heidelberg: Springer, 2007.
8. Moore, G.E., *Progress in digital integrated electronics.* Proc. IEDM Tech. Dig., 1975: p. 103.
9. Bose, B.K., IEEE Trans. Ind. Electron, 2012. **60**: p. 2638.
10. Ohashi, H., *Power devices now and future, strategy of Japan.* In 2012 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2012: p. 9-12.
11. Iacopi, F., et al., *Power electronics with wide bandgap materials: Toward greener, more efficient technologies.* Mrs Bulletin, 2015. **40**(5): p. 390-398.
12. Shikata, S., et al., *Recent Progress of Diamond Device toward Power Application*, in *Silicon Carbide and Related Materials 2008*, A. PerezTomas, et al., Editors. 2009, Trans Tech Publications Ltd: Stafa-Zurich. p. 999-1002.
13. A. Nakagawa, Y.K., K. Nakamura, *Silicon Limit Electrical Characteristics of Power Devices and ICs* 2008.
14. P.N. Volpe, P.M., J. Pernot, F. Omnès, T. Teraji, Y. Koide, F. Jomard, D. Planson, P. Brosselard, N. Dheilly, B. Vergne, S. Scharnholz, *Extreme dielectric strength in boron doped homoepitaxial diamond.* Applied Physics Letters, 2010. **97**.
15. B. Ozpineci, L.M.T., *Comparison of wide-bandgap semiconductors for power electronics applications.* 1996.
16. Baliga, B.J., *Semiconductos for high-voltage, vertical channel field-effect transistors.* Journal of Applied Physics, 1982. **53**(3): p. 1759-1764.
17. Semiconductor, A., *Defining Maximum Operating Junction Temperature.* Application Note. **AN-1011**.

18. Balmer, R.S., et al., *Unlocking diamond's potential as an electronic material.* Philosophical transactions of the Royal Society A - Mathematical, Physical and Engineering Sciences, 2008. **366**(1863): p. 251-265.
19. Nebel, C.E., et al., *Diamond for bio-sensor applications.* Journal of Physics D-Applied Physics, 2007. **40**(20): p. 6443-6466.
20. Brambilla, A., et al., *CVD diamond gamma dose rate monitor for harsh environment.* Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment, 2001. **458**(1-2): p. 220-226.
21. Morse, J., et al., *Single crystal CVD diamond as an X-ray beam monitor.* Diamond and Related Materials, 2007. **16**(4-7): p. 1049-1052.
22. P. N. Volpe, P.M., J. Pernot, F. Omnes, T. Teraji, F. Jomard, D. Planson, P. Brosselard, N. Dheilly, B. Vergne, S. Scharnholtz, *High breakdown voltage Schottky diodes synthesized on p-type CVD diamond layer.* Physica Status Solidi (a), 2010. **207**(9): p. 2088-2092.
23. Kato, H., et al., *Diamond bipolar junction transistor device with phosphorus-doped diamond base layer.* Diamond and Related Materials, 2012. **27-28**: p. 19-22.
24. Moran, D.A.J., et al., *Processing of 50 nm gate-length hydrogen terminated diamond FETs for high frequency and high power applications.* Microelectronic Engineering, 2011. **88**(8): p. 2691-2693.
25. Moran, D.A.J., et al., *Scaling of Hydrogen-Terminated Diamond FETs to Sub-100-nm Gate Dimensions.* IEEE Electron Device Letters, 2011. **32**(5): p. 599-601.
26. Imura, M., et al., *Development of AlN/diamond heterojunction field effect transistors.* Diamond and Related Materials, 2012. **24**: p. 206-209.
27. Edgington, R., et al., *Boron delta-doped (1 1 1) diamond solution gate field effect transistors.* Biosensors & Bioelectronics, 2012. **33**(1): p. 152-157.
28. Zunger, A., *Practical Doping Principles.* Applied Physics Letters, 2003.
29. Chevallier, J., et al., *Different approaches for the n-type doping of diamond*. Proceedings of the 2007 International Workshop on the Physics of Semiconductor Devices: Iwpsd-2007, ed. K.L. Narasimhan and D.K. Sharma2007, New York: Ieee. 813-818.
30. Araujo, D., et al., *Study of the phosphorus incorporation in n-doped diamond films by cathodoluminescence.* Journal of Physics-Condensed Matter, 2004. **16**(2): p. S287-S292.
31. Lagrange, J.P., A. Deneuville, and E. Gheeraert, *Activation energy in low compensated homoepitaxial boron-doped diamond films.* Diamond and Related Materials, 1998. **7**(9): p. 1390-1393.
32. Cohan, N.V., D. Pugh, and R.H. Tredgold, *Band structure of diamond.* Proceedings of the Physical Society of London, 1963. **82**(525): p. 65-&.
33. Cohan, N.V., *Band Structure of Diamond.* Proc. Phys. Soc., 1963. **82**.
34. Araujo, D., et al., *Influence of the substrate type on CVD grown homoepitaxial diamond layer quality by cross sectional TEM and CL analysis.* Diamond and Related Materials, 2011. **20**(3): p. 428-432.

35. Klein, T., et al., *Metal-insulator transition and superconductivity in boron-doped diamond.* Physical Review B, 2007. **75**(16).
36. Bustarret E, A.P., Sacepe B , Chapelier C, Marcenat C, Ortega L, Klein T, *Metal-to-insulator transition and superconductivity in boron-doped diamond.* Philosophical transactions of the Royal Society A - Mathematical, Physical and Engineering Sciences, 2008. **366**.
37. S. Dimitrijev, J.H., D. Haasmann, H.A. Moghadam, A. Aminbeidokhti, *Power-switching applications beyond silicon: The status and future prospects of SiC and GaN devices.* International Conference on Microelectronics, 2014: p. 43.
38. J. Isberg, J.H., E. Johansson, T. Wikstrom, D.J. Twitchen, A. J. Whitehead, S. E. Coe, and G. A. Scarsbrook, *High carrier mobility in single-crystal plasma-deposited diamond.* Science, 2002. **297**(5587): p. 1670-1672.
39. Somogyi, K., *Classical approximations for ionised impurity scattering applied to diamond monocrystals.* Diamond and Related Materials, 2002. **11**(3-6): p. 686-691.
40. Fox, B.A., et al., *Diamond devices and electrical properties.* Diamond and Related Materials, 1995. **4**(5-6): p. 622-627.
41. H. F. Li, S.D., H. B. Harrison, D. Sweatman, Applied Physics Letters, 1997. **70**: p. 2028.
42. Maki, T., et al., *Hydrogenating effect of single-crystal diamond surface.* Japanese Journal of Applied Physics Part 2-Letters, 1992. **31**(10A): p. L1446-L1449.
43. Sakai, T., et al., *Ozone-treated channel diamond field-effect transistors.* Diamond and Related Materials, 2003. **12**(10–11): p. 1971-1975.
44. Muret, P. and C. Saby, *Band bending, electronic affinity and density of states at several (100) surfaces of boron-doped homoepitaxial diamond thin films.* Semiconductor Science and Technology, 2004. **19**(1): p. 1-7.
45. Monch, W., *Barrier heights of metal contacts on H-terminated diamond - explanation by metal-induced gap states and interface dipoles.* Europhysics Letters, 1994. **27**(6): p. 479-484.
46. Humphreys, T.P., et al., *The role of atomic hydrogen and its influence on the enhancement of secondary electron emission from C(001) surfaces.* Applied Physics Letters, 1997. **70**(10): p. 1257-1259.
47. Uppireddi, K., et al., *Thermionic emission energy distribution from nanocrystalline diamond films for direct thermal-electrical energy conversion applications.* Journal of Applied Physics, 2009. **106**(4).
48. Kataoka, M., et al., *Thermionic electron emission from nitrogen-doped homoepitaxial diamond.* Diamond and Related Materials, 2010. **19**(2-3): p. 110-113.
49. Sque, S.J., R. Jones, and P.R. Briddon, *Structure, electronics, and interaction of hydrogen and oxygen on diamond surfaces.* Physical Review B, 2006. **73**(8).
50. Maier, F., J. Ristein, and L. Ley, *Electron affinity of plasma-hydrogenated and chemically oxidized diamond (100) surfaces.* Physical Review B, 2001. **64**(16).

51. Teraji, T., et al., *Low-leakage p-type diamond Schottky diodes prepared using vacuum ultraviolet light/ozone treatment.* Journal of Applied Physics, 2009. **105**(12).
52. Ikeda, K., et al., *Thermally Stable Schottky Barrier Diode by Ru/Diamond.* Applied Physics Express, 2009. **2**(1).
53. Evans, D.A., et al., *Diamond-metal contacts: interface barriers and real-time characterization.* Journal of Physics-Condensed Matter, 2009. **21**(36).
54. Baumann, P.K. and R.J. Nemanich, *Electron affinity and Schottky barrier height of metal-diamond (100), (111), and (110) interfaces.* Journal of Applied Physics, 1998. **83**(4): p. 2072-2082.
55. Makoto, K., S. Hisashi, and H. Kazuyuki, *Thermal Stabilization of Hole Channel on H-Terminated Diamond Surface by Using Atomic-Layer-Deposited Al 2 O 3 Overlayer and its Electric Properties.* Applied Physics Express, 2012. **5**(2): p. 025701.
56. A. Fiori, J.P., E. Gheeraert, E. Bustarret, *Simulations of carrier confinement in boron d-doped diamond devices.* Physica Status Solidi (a), 2010. **207**: p. 2084-2087.
57. Imura, M., et al., *Demonstration of diamond field effect transistors by AlN/diamond heterostructure.* Physica Status Solidi (RRL) – Rapid Research Letters, 2011. **5**(3): p. 125-127.
58. P.N. Volpe, P.M., J. Pernot, F. Omnès, T. Teraji, Y. Koide, F. Jomard, D. Planson, P. Brosselard, N. Dheilly, B. Vergne, S. Scharnholz., *Extreme dielectric strength in boron doped homoepitaxial diamond.* Applied Physics Letters, 2010. **97**(22).
59. Teraji, T., Y. Koide, and T. Ito, *Schottky barrier height and thermal stability of p-diamond (100) Schottky interfaces.* Thin Solid Films, 2014. **557**: p. 241-248.
60. Liao, M., Y. Koide, and J. Alvarez, *Crystallographic and electrical characterization of tungsten carbide thin films for Schottky contact of diamond photodiode.* Journal of Vacuum Science & Technology B, 2006. **24**(1): p. 185-189.
61. Chicot, G., et al., *Metal oxide semiconductor structure using oxygen-terminated diamond.* Applied Physics Letters, 2013. **102**: p. 242108.
62. Pierre Muret, J.P., Tokuyuki Teraji, Toshimichi Ito, *Deep levels in homoepitaxial boron-doped diamond films studied by capacitance and current transient spectroscopies.* Physica Status Solidi (a), 2008. **205**.
63. A. Fiori, T.N.T.T., G. Chicot, F. Jomard, F. Omnès, E. Gheeraert, E. Bustarret, *In situ etching-back processes for a sharper top interface in boron delta-doped diamond structures.* Diamond and Related Materials, 2012. **24**: p. 175-178.
64. L.A. Giannuzzi, F.A.S., *A review of focused ion beam milling techniques for TEM specimen preparation.* Micron, 1999. **30**: p. 197-204.
65. Jin, H.H., et al., *Modified preparation technique of TEM sample for various TEM analyses of structural materials.* Materials Letters, 2012. **89**: p. 133-136.
66. Schaffer, M., B. Schaffer, and Q. Ramasse, *Sample preparation for atomic-resolution STEM at low voltages by FIB.* Ultramicroscopy, 2012. **114**: p. 62-71.
67. Chen, Y.Q., F.Z. Tang, and L.C. Zhang, *A preparation method of diamond specimens using an advanced FIB microscopy for micro and nanoanalysis*, in *Materials Science*

and Nanotechnology I, C.L. Zhang and L.C. Zhang, Editors. 2013, Trans Tech Publications Ltd: Stafa-Zurich. p. 592-595.
68. S. M. Sze, K.N.K., Physics of semiconductor devices, 2nd ed. Wiley, New York, 1981.
69. Ikeda, K., et al., *Fabrication of a field plate structure for diamond Schottky barrier diodes.* Diamond and Related Materials, 2009. **18**(2-3): p. 292-295.
70. Umezawa, H., et al., *Increase in Reverse Operation Limit by Barrier Height Control of Diamond Schottky Barrier Diode.* Electron Device Letters, IEEE, 2009. **30**(9): p. 960-962.
71. Landstrass, M.I., et al., *Device properties of homoepitaxially grown diamond.* Diamond and Related Materials, 1993. **2**(5–7): p. 1033-1037.
72. Gaowei, M., et al., *Annealing dependence of diamond-metal Schottky barrier heights probed by hard x-ray photoelectron spectroscopy.* Applied Physics Letters, 2012. **100**(20): p. 201606.
73. Kiyota, H., et al., *Electrical properties of Schottky barrier formed on as-grown and oxidized surface of homoepitaxially grown diamond (001) film.* Applied Physics Letters, 1995. **67**(24): p. 3596-3598.
74. Boukherroub, R., et al., *Photochemical oxidation of hydrogenated boron-doped diamond surfaces.* Electrochemistry Communications, 2005. **7**(9): p. 937-940.
75. Ohta, R., et al., *Organosilane self-assembled monolayers directly linked to the diamond surfaces.* Journal of Vacuum Science & Technology A, 2004. **22**(5): p. 2005-2009.
76. Gurbuz, Y., et al., *Diamond semiconductor technology for RF device applications.* Solid-State Electronics, 2005. **49**(7): p. 1055-1070.
77. H. Kato, K.O., T. Makino, M. Ogura, D. Takeuchi, and S. Yamasaki, Diamond and Related Materials, 2012. **27-28**: p. 19.
78. T. Iwazaki, Y.H., K. Tsuzuki, H. Kato, T. Makino, M. Ogura, D. Taekuchi, T. Matsumoto, H. Okushi, S. Yamasaki, and M. Hatano, Applied Physics Express, 2012. **5**: p. 091301.
79. T. Makino, S.T., Y. Hayashi, H. Kato, N. Tokuda, M. Ogura, D. Takeuchi, K. Oyama, H. Ohashi, H. Okushi, and S. Yamasaki, Applied Physics Letters, 2009. **94**: p. 262101.
80. Twitchen, D.J., et al., *High-voltage single-crystal diamond diodes.* IEEE Transactions on electron devices, 2004. **51**(5): p. 826-828.
81. Butler, J.E., et al., *Exceptionally high voltage Schottky diamond diodes and low boron doping.* Semiconductor Science and Technology, 2003. **18**(3): p. S67-S71.
82. T. P. Chow, W.H., J. Yang, and J. E. Butler, Int. J. High Speed Electron. Syst. , 2004. **14**: p. 872.
83. Teraji, T., Y. Koide, and T. Ito, *High-temperature stability of Au/p-type diamond Schottky diode.* Physica Status Solidi-Rapid Research Letters, 2009. **3**(6): p. 211-213.
84. Fiori, A., T. Teraji, and Y. Koide, *Thermal stabilization and deterioration of the WC/p-type diamond (100) Schottky-barrier interface.* Physica Status Solidi (a), 2014. **211**(10): p. 2363-2366.

85. Rhoderick, E.H., *Metal semiconductor contacts.* Oxford Unuversity Press, 1978., 1978.
86. Traoré, A., et al., *Zr/oxidized diamond interface for high power Schottky diodes.* Applied Physics Letters, 2014. **104**: p. 052105.
87. Ueda, K., et al., *High-temperature characteristics of Ag and Ni/diamond Schottky diodes.* Diamond and Related Materials, 2013. **38**(0): p. 41-44.
88. Traore, A., *High power diamond Schottky diode.* PhD disertation - Institut Néel, 2014.
89. Brillo, J., H. Kuhlenbeck, and H.J. Freund, *Interaction of O-2 with WC(0001).* Surface Science, 1998. **409**(2): p. 199-206.
90. Umezawa, H., Y. Kato, and S. Shikata, *1 Omega On-Resistance Diamond Vertical-Schottky Barrier Diode Operated at 250 degrees C.* Applied Physics Express, 2013. **6**(1).
91. Kumaresan, R., H. Umezawa, and S. Shikata, *Vertical structure Schottky barrier diode fabrication using insulating diamond substrate.* Diamond and Related Materials, 2010. **19**(10): p. 1324-1329.
92. Volpe, P.N., et al., *Extreme dielectric strength in boron doped homoepitaxial diamond.* Applied Physics Letters, 2010. **97**(22).
93. Liao, M.Y., J. Alvarez, and Y. Koide, *Thermal stability of diamond photodiodes using tungsten carbide as Schottky contact.* Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers, 2005. **44**(11): p. 7832-7838.
94. Umezawa, H., et al., *High temperature application of diamond power device.* Diamond and Related Materials, 2012. **24**: p. 201-205.
95. Kenji, U., K. Keita, and A. Hidefumi, *High-temperature characteristics and stability of Cu/diamond Schottky diodes.* Japanese Journal of Applied Physics, 2014. **53**(4S): p. 04EP05.
96. Muret, P., et al., *Potential barrier heights at metal on oxygen-terminated diamond interfaces.* Journal of Applied Physics, 2015. **118**(20): p. 204505.
97. Wang, B., *Mechanics of advanced Functional Materials.* Zhejiang University Press, 2013.
98. Morkoç, H., et al., *Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies.* Journal of Applied Physics, 1994. **76**(3): p. 1363-1398.
99. Dimitrijev, S., et al., *Power-switching applications beyond silicon: Status and future prospects of SiC and GaN devices.* Mrs Bulletin, 2015. **40**(05): p. 399-405.
100. Chicot, G., *Field effect in boron doped diamond.* PhD disertation - Institut Néel, 2013.
101. George, S.M., *Atomic Layer Deposition: An Overview.* Chem. Rev., 2010. **110**: p. 111-131.
102. Kasu, M., H. Sato, and K. Hirama, *Thermal Stabilization of Hole Channel on H-Terminated Diamond Surface by Using Atomic-Layer-Deposited Al2O3 Overlayer and its Electric Properties.* Applied Physics Express, 2012. **5**(2).

103. Yokota, T., *Origin of the metallic properties of heavily boron-doped superconducting diamond.* Nature, 2005. **438**: p. 647-650.
104. A. Hirawira, A.D., S. Kurihara, Y. Yokoyama, and H. Kawarada, J. Appl. Phys., 2012. **112**: p. 124504.
105. J. W. Liu, M.Y.L., M. Imura, H. Li, and Y. Koide, Applied Physics Letters, 2012. **101**: p. 232907.
106. Omnes, F., et al., *Study of boron doping in MPCVD grown homoepitaxial diamond layers based on cathodoluminescence spectroscopy, secondary ion mass spectroscopy and capacitance-voltage measurements.* Diamond and Related Materials, 2011. **20**(7): p. 912-916.
107. Mönch, P.D.W., *Semiconductor Surfaces and Interfaces.* Springer-Verlag Berlin Heidelberg, 2001.
108. N.D.M. Hine, K.F., M.W. Finnis, W.M. Foulkes, A.H. Heuer, *Point defects and diffusion in alpha-alumina.* International Conference on QMC in the Apuan Alps, 2009.
109. Aschauer, U., P. Bowen, and S.C. Parker, *Oxygen vacancy diffusion in alumina: New atomistic simulation methods applied to an old problem.* Acta Materialia, 2009. **57**(16): p. 4765-4772.
110. Novikov, Y.N., V.A. Gritsenko, and K.A. Nasyrov, *Charge transport mechanism in amorphous alumina.* Applied Physics Letters, 2009. **94**(22).
111. Pugh, D., *Surface states on (111) surface on diamond.* Physical review Letters, 1964. **12**(14): p. 390-&.
112. Tajani, A., et al., *Homoepitaxial {111}-oriented diamond pn junctions grown on B-doped Ib synthetic diamond.* Physica Status Solidi (a), 2004. **201**(11): p. 2462-2466.
113. Araujo, D., et al., *Excitonic emission and N- and B-incorporation in homoepitaxial CVD-grown diamond investigated by cathodoluminescence.* Physica Status Solidi (c), 2005. **2**(4): p. 1336-1341.
114. Barjon, J., F. Jomard, and S. Morata, *Arsenic-bound excitons in diamond.* Physical Review B, 2014. **89**(4).
115. Koizumi, S., T. Teraji, and H. Kanda, *Phosphorus-doped chemical vapor deposition of diamond.* Diamond and Related Materials, 2000. **9**(3–6): p. 935-940.
116. Saguy, C., E. Baskin, and R. Kalish, *Electrical properties of undoped and ion-implanted type IIa diamonds measured by photo-Hall.* Diamond and Related Materials, 2005. **14**(3-7): p. 344-349.
117. Gheeraert, E., et al., *Low temperature excitation spectrum of phosphorus in diamond.* Diamond and Related Materials, 2001. **10**(3-7): p. 444-448.
118. Vogel, T., J. Meijer, and A. Zaitsev, *Highly effective p-type doping of diamond by MeV ion implantation of boron.* Diamond and Related Materials, 2004. **13**(10): p. 1822-1825.
119. Ratnikova, A.K., et al., *Homoepitaxial single crystal diamond grown on natural diamond seeds (type IIa) with boron-implanted layer demonstrating the highest mobility of 1150 cm(2)/V s at 300 K for ion-implanted diamond.* Diamond and Related Materials, 2011. **20**(8): p. 1243-1245.

120. Schubert, E.F., *Delta doping of III-V compound semiconductors - fundamentals and device applications.* Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films, 1990. **8**(3): p. 2980-2996.
121. J.W. Ager, W.W., M. McCluskey, M.A. Plano, M.I. Lansdtrass, Applied Physics Letters, 1995. **66**: p. 616.
122. Thonke, K., *The boron acceptor in diamond.* Semicond. Sci. Technol., 2003. **18**: p. S20.
123. Alex Trellakis, T.A., and Peter Vogl, *Efficient Solution of the Schrödinger-Poisson Equations in Semiconductor Device Simulations.*
124. Volpe, P.N., et al., *High hole mobility in boron doped diamond for power device applications.* Applied Physics Letters, 2009. **94**(9).
125. H. El-Hajj, A.D., A. Bergmaier, G. Dollinger, M. Kubovic, E. Kohn, *Characteristics of boron δ-doped diamond for electronic applications.* Diamond and Related Materials, 2008. **17**: p. 409-414.
126. Groner, M.D., et al., *Low-Temperature Al2O3 Atomic Layer Deposition.* Chemistry of Materials, 2004. **16**(4): p. 639-645.
127. D. Araujo, P.A., R. El Bouayadi, A.J. Garcia, M.P. Alegre, M. P. Villar, F. Jomard, E. Bustarret, *Local boron doping quantification in homoepitaxial diamond structures.* Diamond and Related Materials, 2010. **19**(7-9): p. 972-975.
128. Lu, Y.G., et al., *Direct visualization of boron dopant distribution and coordination in individual chemical vapor deposition nanocrystalline B-doped diamond grains.* Applied Physics Letters, 2012. **101**(4).
129. Pizarro, J., et al., *Simulation of high angle annular dark field scanning transmission electron microscopy images of large nanostructures.* Applied Physics Letters, 2008. **93**(15).
130. D. Araujo, P.A., R. El Bouayadi, A.J. Garcia, M.P. Alegre, M. P. Villar, F. Jomard, E. Bustarret, *Local boron doping quantification in homoepitaxial diamond structures.* Diamond and Related Materials, 2010. **19**(7–9): p. 972-975.
131. Carter, D.B.W.a.C.B., *Transmission Electron Microscopy, a textbook for Materials Science.* 1996-2009.
132. Kirkland, E.J., R.F. Loane, and J. Silcox, *Simulation of annular dark field STEM images using a modified multislice method.* Ultramicroscopy, 1987. **23**(1): p. 77-96.
133. Fiori, A., T. Teraji, and Y. Koide, *Diamond Schottky diodes with ideality factors close to 1.* Applied Physics Letters, 2014. **105**(13).
134. Hofmann, S., *Depth resolution in sputter profiling.* Applied physics, 1977. **13**(2): p. 205-207.
135. G. Chicot, T.N.T.T., A. Fiori, F. Jomard, E. Gheeraert et al., *Hole transport in boron delta-doped diamond structures.* Applied Physics Letters, 2012. **101**.
136. Balmer, R.S., et al., *Transport behavior of holes in boron delta-doped diamond structures.* Journal of Applied Physics, 2013. **113**(3).
137. Alegre, M.P., *Calidad cristalina e incorporación de boro en homoepitaxias de diamante.* PhD disertation - Universidad de Cádiz, 2014.

138. Brazhkin, V.V., et al., *Lattice parameters and thermal expansion of superconducting boron-doped diamonds.* Physical Review B, 2006. **74**(14): p. 140502.
139. Araújo, D., et al., *Boron concentration profiling by high angle annular dark field-scanning transmission electron microscopy in homoepitaxial.* Applied Physics Letters, 2013.
140. Wort, C.J.H. and R.S. Balmer, *Diamond as an electronic material.* Materials Today, 2008. **11**(1–2): p. 22-28.
141. Chicot, G., et al., *Electronic and physico-chemical properties of nanometric boron delta-doped diamond structures.* Journal of Applied Physics, 2014. **116**(8): p. -.
142. Maréchal, A., et al., *Energy-band diagram configuration of Al2O3/oxygen-terminated p-diamond metal-oxide-semiconductor.* Applied Physics Letters, 2015. **107**(14): p. 141601.
143. Hirama, K., et al., *Characterization of diamond metal-insulator-semiconductor field-effect transistors with aluminum oxide gate insulator.* Applied Physics Letters, 2006. **88**(11).
144. D. Drouin, A.R.C., R. Gauvin, P. Hovington, P. Homy, H. Demers CASINO, www.gel.usherbrooke.ca/casino.
145. database, E., https://eelsdb.eu/.
146. Diederich, L., et al., *Electron affinity and work function of differently oriented and doped diamond surfaces determined by photoelectron spectroscopy.* Surface Science, 1998. **418**(1): p. 219-239.
147. Vincent, G., *All the physical and electrical parameters of the MOS transistor on a single graph (QΨ)*.* Eur. Phys. J. Appl. Phys., 2005. **32**(3): p. 155-158.
148. Vincent, G., *Metal oxide semiconductor structure and transistor behaviour using a single and simple graph (Qψ) which takes into account all the physical and electrical parameters.* Journal of Applied Physics, 2008. **103**(7): p. 074505.

José Carlos Piñero Charlo

C/Teresa de Calcuta, nº 58. Puerto Real (Cádiz, España).
CP - 11510
Phone number: +34 660 58 48 95
E-mail: josecarlos.pinero@uca.es
Date of birth: 10 – 11 – 1984
NIF: 44965997P

Featured publications

1. P. Muret, A. Traoré, A. Maréchal, D. Eon, J. Pernot, D. Araujo, J. Piñero. "Potential Barrier Heights at Metal on Oxygen-Terminated P. Muret, A. Traoré, A. Maréchal, D. Eon, J. Pernot, D. Araujo, J. Piñero. "Potential Barrier Heights at Metal on Oxygen-Terminated Diamond Interfaces." *Journal of Applied Physics* 118, no. 20 (2015): 204505.
2. Navas, Javier, Antonio Sanchez-Coronilla, Juan Jesus Gallardo, Norge Cruz Hernandez, Jose Carlos Pinero, Rodrigo Alcantara, Concha Fernandez-Lorenzo*, et al.* "New Insights into Organic-Inorganic Hybrid Perovskite Ch3nh3pbi3 Nanoparticles. An Experimental and Theoretical Study of Doping in Pb^{2+} Sites with Sn^{2+}, Sr^{2+}, Cd^{2+} and Ca^{2+}." *Nanoscale* 7, no. 14 (2015): 6216-29.
3. De los Santos, Desiré M., Javier Navas, Teresa Aguilar, Antonio Sánchez-Coronilla, Concha Fernández-Lorenzo, Rodrigo Alcántara, Jose Carlos Piñero, Ginesa Blanco, and Joaquín Martín-Calleja. "Tm-Doped TiO_2 and $Tm_2Ti_2O_7$ Pyrochlore Nanoparticles: Enhancing the Photocatalytic Activity of Rutile with a Pyrochlore Phase." *Beilstein Journal of Nanotechnology* 6 (2015): 605-16.
4. Piñero, J. C., D. Araujo, A. Traoré, G. Chicot, A. Maréchal, P. Muret, M. P. Alegre, M. P. Villar, and J. Pernot. "Metal–Oxide–Diamond Interface Investigation by Tem: Toward MOS and Schottky Power Device Behavior." *Physica Status Solidi (a)* 211, no. 10 (2014): 2367-71.
5. A. Vo-Ha, M. Rebaud, D. Carole, M. Lazar, A. Tallaire, V. Soulière, J. C. Pinero, D. Araujo, G. Ferro. "3c-Sic Seeded Growth on Diamond Substrate by Vls Transport." *Materials Science Forum* 778-780 (2014): 234-37
6. V. Soulière, A. Vo-Ha, D. Carole, A. Tallaire, O. Brinza, J.C. Pinero, D. Araujo, G.Ferro. "Heteroepitaxial Cvd Growth of 3c-Sic on Diamond substrate." *Materials Science Forum* 778-780 (2014): 226-29.
7. Lloret, F., J. Piñero, D. Araujo, M. P. Villar, E. Gheeraert, A. Vo-Ha, V. Soulière*, et al.* "Diamond as Substrate for 3c-Sic Growth: A Tem Study." *Physica Status Solidi (a)* 211, no. 10 (2014): 2302-06.
8. Chicot, G., A. Fiori, P. N. Volpe, T. N. Tran Thi, J. C. Gerbedoen, J. Bousquet, M. P. Alegre*, et al.* "Electronic and Physico-Chemical Properties of Nanometric Boron Delta-Doped Diamond Structures." *Journal of Applied Physics* 116, no. 8 (2014): -.
9. Alegre, M. P., D. Araújo, A. Fiori, J. C. Pinero, F. Lloret, M. P. Villar, P. Achatz*, et al.* "Critical Boron-Doping Levels for Generation of Dislocations in Synthetic Diamond." *Applied Physics Letters* 105, no. 17 (2014): -
10. Araújo, D., M. P. Alegre, J. C. Piñero, A. Fiori, E. Bustarret, and F. Jomard. "Boron Concentration Profiling by High Angle Annular Dark Field-Scanning Transmission Electron Microscopy in Homoepitaxial." *Applied Physics Letters* (2013).
11. J. C. Piñero, D. Araújo, A. Fiori, A. Traoré, M. P. Villar, D. Eon, P. Muret, J. Pernot, and T. Teraji, Applied Surface Science (accepted for publication on 27 - April - 2016).

Featured contributions to congress

A total of 24 contributions at international conferences during the interval 2012-2015. Among them, we highlight:

- **Title:** HREM of Diamond Related MOS Structures **Congress:** Materials Research Society 2014 **Date:** 2014 (Noviembre) **Place:** Boston,- MASSACHUSETTS; ESTADOS UNIDOS DE AMERICA **Authors:** Piñero-Charlo, José Carlos; Araújo-Gay, Daniel; Villar Castro, Maria Del Pilar
- **Title:** Thermal treatment and interface-related effects on WC/ and Zr/O-terminated diamond Schottky diodes by TEM **Congress:** SURFINT-SREN IV **Date:** 2015 (Noviembre) **Place:** Florencia (Italia) **Authors:** J. Piñero, D. Arauj, P.Villar, A. Traoré, D. Eon, P. Muret, A. Fiori, J. Pernot, T. Teraji

Other qualifications	
International experience (scolarships and awards)	
Best young researcher (SURFINT-SREN 2015)	Scolarship “training staff researcher” (BES-2010-039524)
Stage at EPFL 2013 (three months)	Stage at Institut Néel 2013 (three months)
Stage at EPFL 2012 (three months)	Stage at Attolight 2012 (three months)