A 0.18µm CMOS Low-Noise Elliptic Low-Pass Continuous-Time Filter

Juan Francisco Fernández-Bootello, Manuel Delgado-Restituto and Ángel Rodríguez-Vázquez
Instituto de Microelectónica de Sevilla, Centro Nacional de Microelectrónica
Avda. Reina Mercedes s/n, 41012-Sevilla (España), Tel: +34 - 95 505 6666
E-mails: bootello@imse.cnm.es, mandel@imse.cnm.es, angel@imse.cnm.es

***Abstract*— This paper presents a seventh order low-pass continuous-time elliptic filter for use in a high-performance wireline communication receiver. As an additional attribute, the filter provides programmable boost in the pass-band to counteract high frequency components attenuation. The filter shows a nominal cutoff frequency of f_c = 34 MHz, less than 1dB ripple in the pass-band, and a maximum stop-band rejection of 65dB. The filter also exhibits low noise feature (peak root spectral noise density below 56nV/$\sqrt{\text{Hz}}$) and high linearity (more than 64dB of MTPR for a DMT signal of $0.5V_{pp}$ amplitude). It has been designed in a 0.18µm CMOS technology and it is compliant with industrial operation conditions (-40 to 85ºC temperature variation and ±5% power supply deviation). Simulations show a typical power consumption of 450 mW @ 1.8V supply.**

***Index Terms*— Analog Filters, Continuous-Time Filters, G_m-C Filters, Low-noise, High-linearity.†**

I. Introduction

Modern high-performance receivers, particularly those used in communications through hostile transmission media, usually require large Dynamic Range (DR) filtering stages before A/D conversion, in order to reduce the number of bits that the digital processor and the converter itself must resolve [1]. In these cases, filter requirements are not only tailored from anti-alias criteria, due to the sampled-data nature of the conversion stage, but also by accounting that unwanted signals, which may be even larger than the desired information, must be sufficiently attenuated to avoid data converter overloads. Moreover, filters at the Analog Front-End (AFE) of the receiver must be linear enough so not to create intermodulation distortion components which fall in the desired channel. This is, indeed, a major requirement in systems based on Digital Multi-Tone (DMT) signalling [2].

In this paper, we describe an integrated seventh-order low-pass filter to be used at the AFE of a high-performance broadband Power-Line Communication (PLC) receiver. As an additional signal conditioning feature, the filter can be digitally programmed for boosting the high-frequency components of the passband. Main specifications for the filter are 34 MHz of cutoff frequency, more than 40dB of stopband rejection (corner at 46 MHz), less than 1dB ripple in the passband, and programmable boosting from 0 to 12dB at 2dB steps. By far, the most demanding specifications concern noise and distortion. The filter must exhibit less than 60nV/$\sqrt{\text{Hz}}$ of peak root spectral density in the passband, and more than 60dB of MTPR for different patterns of DMT signals of $0.5V_{pp}$ amplitude.

The paper is organized as follows. Sec. II describes the design considerations taken to define the filter structure in order to comply with specifications as well as to reduce as much as possible the power and area consumptions. Sec. III focuses on the transconductor block, as the main building element of the architecture, and Sec. IV shows the circuitry used for tuning. Finally, Sec. V presents simulations of the filter and transconductor block, and Sec. gives some concluding remarks.

II. Filter Structure

Owing to the superior performance of doubly terminated LC ladder filter structures with regard to its low sensitivity to components variation, their emulation by active circuits very often constitute the candidates of choice for silicon realization [3]. This is also favoured by the availability of algorithms which, by simple matrix manipulations, are able to map the original LC structure to its equivalent active representation using integrators as elementary building blocks [4]. In the proposed design, also based on LC emulation, the ladder filter (illustrated in Fig. 1) has been implemented with G_m-C (or transconductor-C) open-loop integrators given the high frequency characteristic of the filter, that makes unreliable other alternatives such as active-RC or MOSFET-C [6].

The active structure of the filter must be scaled in order to achieve the smallest possible area and power consumptions for a given set of specifications [6]. The optimization algorithm used in the design of the proposed filter has been described in [7] and takes into account design aspects, such as limited quality factor of integrators, internal peak amplitudes, noise (they are evaluated by simple matrix methods), linearity (using Volterra series), as well as area and power estimations. The optimizer uses simulated annealing techniques and explores the design space of all those filter configurations de-

†. **Acknowledgement**: This work has been partially funded by the spanish MCyT under Project TIC2003-02355 (RAICONIF).

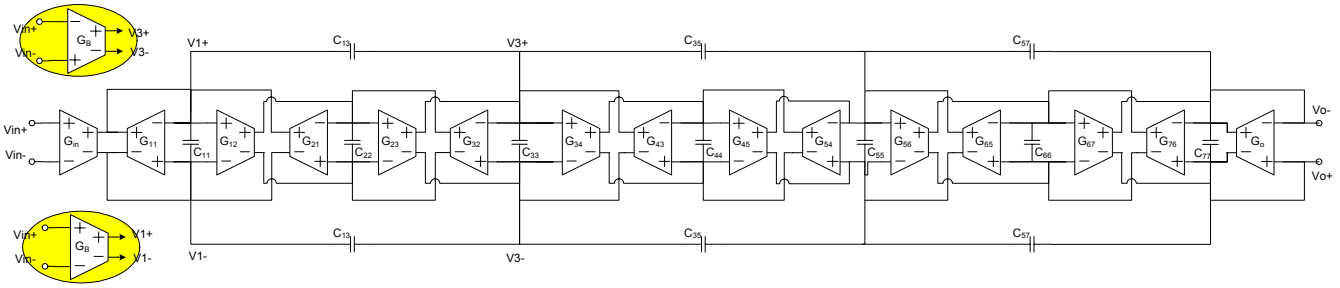

Fig. 1. Simplified schematic of the filter. Programmable feedforward transconductors G_B at the insets provide transfer boosting at high frequencies.

rived from a single LC prototype, with integer ratios among transconductors. This is done to reduce mismatch effects (all transconductors are made as multiples of a single unitary element), as well as to simplify the tuning strategy and speed-up the design process.

In order to satisfy system requirements, it was found after optimization that the unitary transconductor must exhibit a transconductance of $G_{mu} = 425\ \mu A/V$, a noise excess factor below 10 and an IM_3 component better than 70dB for two tones of $140mV_{pp}$ separated 1MHz along the filter passband. On the other hand, Table 1 and 2 show, respectively, the number of unitary elements composing the transconductors of Fig. 1, and the value of the filter capacitances

Table 1: Number of unitary elements per transconductor.

G_{in}	G_{11}	G_{12}	G_{21}	G_{32}	G_{23}	G_{43}	G_{34}
16	16	16	16	10	16	24	12
G_{54}	G_{45}	G_{65}	G_{56}	G_{76}	G_{67}	G_o	G_B
9	18	18	9	6	12	4	0-32

Table 2: Filter capacitances.

C_{11}	C_{22}	C_{33}	C_{44}	C_{55}
34.9 pF	26.1pF	59.7pF	44.2pF	29.6pF
C_{66}	C_{77}	C_{13}	C_{35}	C_{57}
29.6pF	31.2pF	3.68pF	14.02pF	13.85pF

III. Transconductor

Fig. 2(a) shows the schematic of the transconductor employed in the filter. Transistors M_1, M_3 and M_2, M_4 (enhanced by the feedback action of M_5, M_7 and M_6, M_8, respectively) ideally transfer with unity gain the input voltage of the transconductor to the pair of nominally identical degeneration resistors R_1 and R_2. The generated incremental current, which is ideally proportional to the input voltage as long as resistors R_1 and R_2 are perfectly linear, flows through the loop formed by transistors M_5-M_8 and it is replicated at the output by M_9-M_{12}. It can be found that the transconductance amounts

$$G_m = \frac{g_{m9}}{g_{m5}}\left[\frac{Ag_{m1}}{1+Ag_{m1}R}\right] \approx \frac{g_{m9}}{g_{m5}} \cdot \frac{1}{R} \quad (1)$$

where g_{mj} is the transconductance of transistor M_j, R is the resistance of R_1 and R_2, and A is the gain of the amplifier composed by M_1 and M_3

$$A = \frac{g_{m1}}{g_{ds1}+g_{ds3}} \quad (2)$$

and g_{dsj} is the output conductance of transistor M_j. Approximation in (1) applies for large enough A values and reveals that the transconductance is inversely proportional to the degeneration resistance and can be scaled by the aspect ratio of transistors M_9-M_5 (or M_{10}-M_4). On the other hand, the nonlinearity of the transconductor can be modelled, assuming perfect matching among equivalent elements, by a third order intermodulation coefficient given by

$$IM_3 \approx \frac{3}{32}\left(\frac{1}{Ag_{m1}R^3I^2}\right)v^2 \quad (3)$$

where I is the current provided by the tail transistor M_p and v is the differential input voltage. According to (3), in order to reduce IM_3 for a given transconductance, I and/or A must be increased. Whatever design strategy is used for improving linearity care must be taken to not severely degrade the current efficiency of the transconductor or its high-frequency performance (parasitics at nodes ⓐ must be kept low).

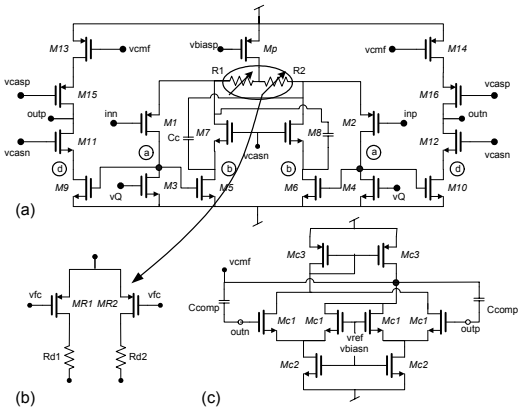

Fig. 2. (a) Schematic of the transconductor; (b) tunable resistor; and (c) common-mode feedback circuit.

Resistors R_1 and R_2 are implemented as shown in Fig. 2(b), where transistors M_{R1} and M_{R2} are operated in the ohmic region by means of the analogue control signal v_{fc}. This allows to continuously vary the resistance R (and thereafter, the transconductance G_m), what is exploited to correct variations in the cut-off frequency of the filter, as explained later on.

In the structure of the Fig.2 (a), the noise excess factor ξ is given by,

$$\xi \approx \frac{2}{3}\left(g_{m9} + g_{m5} + g_{m13}\frac{g_{m9}}{g_{m5}}\right)R + \frac{g_{m9}}{g_{m5}} \quad (4)$$

and, hence, it can be reduced, for a given G_m value, by lowering the transconductances of M_5, M_9 and M_{13}. This can be done by increasing their overhead voltages, taking into account the limited power supply (1.8V) and speed requirements.

A small-signal analysis of Fig.2 (a) reveals that the structure presents poles and zeros approximately given by

$$\omega_{p1} \approx \frac{g_{m7}}{C_b} \qquad \omega_{p2} \approx \frac{g_{m11}}{C_d} \qquad \omega_{p3} \approx \frac{g_{m1}}{C_a}\frac{g_{m5}}{G} \qquad \omega_z \approx \frac{G}{C_c} \quad (5)$$

where C_a, C_b, C_d are the capacitances associated to corresponding nodes in Fig.2 (a), and C_c is a compensation capacitor which aims to counteract the phase lag produced by the poles. Note from (4) and (5), that by decreasing g_{m5} the noise excess factor is reduced but the frequency response of the transconductor worsens. Thus, there is a trade-off between speed and noise. Phase response of the transconductor can be modified (Q-tuned) by controlling the current through transistors M_1, M_3 (and M_2, M_4), using terminal v_Q.

Fig.2 (c) shows the common-mode feedback circuit of the transconductor. Indeed, this circuit is shared by all the paralleled transconductors connected to the same nodes of the filter in Fig.1. To avoid stability problems, two compensation capacitors connect the output nodes of the transconductors to the control node, v_{cmf}.

IV. Tuning Circuit

Fig.3 shows the circuitry used to tune the cut-off frequency and quality factor of the (slave) filter of Fig.1. It is based on a voltage-controlled biquad externally driven by a precise clock reference. Transconductors in the biquad and slave filter are matched and controlled by the same tuning variables obtained from the circuit of Fig.3. At the angular frequency $\omega_c = nG_{mu}/C$, the band-pass output voltage of the biquad (labelled *obp* in Fig.3) is in phase with the input and have the same amplitudes. At the same frequency, the low-pass output voltage of the biquad (labelled *olp* in Fig.3) also shows the same amplitude than the external reference, but they are in quadrature. By comparing the phase of *olp* with that of the external clock, and integrating the error signal in a capacitor, the feedback loop determines a control voltage v_{fc} such that the transconductance becomes $G_{mu} = (2\pi/n)f_{clk}C$, where f_{clk} is the frequency of the external reference. Because integrating

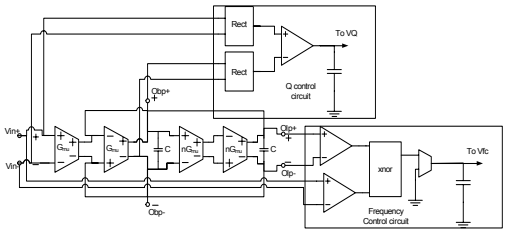

Fig. 3. Tuning circuit.

capacitors in the biquad and the slave filter are also matched, the feedback loop allows to define the cut-off frequency of the filter in terms of f_{clk}. Similarly, by comparing the amplitude of *obp* and the external reference and integrating the errors in a capacitor, the feedback loop determines a control voltage v_Q that tunes the quality factor of the slave filter. The biquad has a quality factor $Q = n = 8$, which is close to the worst case Q of the poles of the filter.

V. Simulation Results

Simulation results from extracted layout (Fig.4) are presented in this section. Fig. 5 (a) shows the transfer characteristics of the filter (no boosting applied), and a detail of the passband, for most representative corners of the process, supply voltage and temperature range. Passband ripple remains below 1dB as specified. Fig. 5 (b) illustrates the programmability of the filter for different cutoff frequencies and boosting settings. For the maximum value of G_B (see Fig. 1), the gain boost amounts 12dB at the cut-off frequency. In time domain simulations, no instability is observed regardless of the boost amplitude. Fig. 5(c) illustrates the root spectral density in the passband for different corners (its peak value remains below 56 nV/$\sqrt{Hz}$ and the integrated in-band noise is 155μV_{rms}). Fig. 6 (a) shows the intermodulation of the transconductor for different corners when it is excited by two tones of 140mV_{pp} of amplitude separated 1MHz. This simulation has been made in the frequency range of interest. As expected, the distortion decreases as the frequency increases. Fig. 6(b) shows the frequency response to a 0.5V_{pp} DMT transient signal at the worst case distortion corner. As can be seen, the multi-tone power ratio (MTPR) is 64 dB.

In order to compare the filter with others in the literature, the third order distortion (HD_3) has been simulated with an input frequency of 5 MHz. In this conditions the filter achieves a HD_3 of -49 dB @ 1.2 V_{pp} differential input thus showing a DR of 69 dB. Table 3 shows the main characteristics of the compared filters where FOM denotes the power per

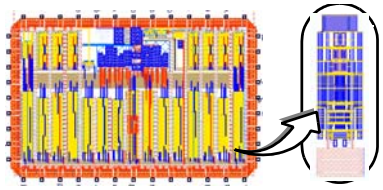

Fig. 4. Layout of the filter

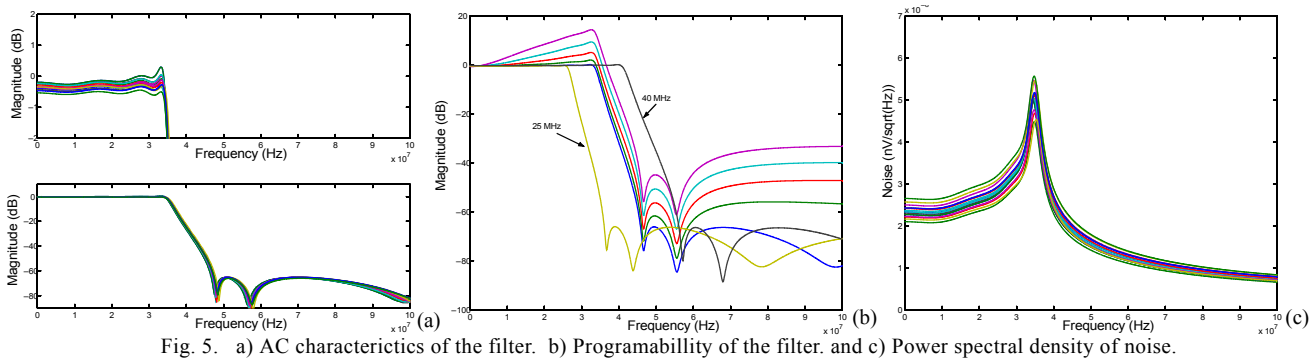

Fig. 5. a) AC characterictics of the filter. b) Programabillity of the filter. and c) Power spectral density of noise.

pole per edge frequency [6]. Fig. 5 (c) shows the FOM vs DR of those filters where the filter proposed is in the best adjustment line.

VI. Conclusions

In this paper, a seventh order elliptic-low pass filter with gain boosting and on-chip tuning has been presented. It has been designed in a 0.18µm CMOS process and occupies an active area of 13mm^2. The filter consumption is 450 mW (without boosting) from a power supply of 1.8V , and exhibits a dynamic range of 69dB . The filter also features very low-noise properties.

Table 3: Comparison of several filter designs

Reference	Silva [8]	Chen [8]	Mehr [10]	Yang [11]	Rezzi [12]	This work
Technology	0.35 CMOS	0.35 CMOS	0.6 CMOS	BiCMOS	BiCMOS	0.18 CMOS
Order	7	4	7	7	7	7
Power supply (V)	3.3	2.3	5	2.5	5	1.8
Edge frequency	200 MHz	150 MHz	25 MHz	600 KHz	50 MHz	34 MHz
HD_3 (dB)	-44 @ 500 mV_{pp} f_{in}=30 MHz	-44 @ 2 V_{pp} f_{in}=20 MHz	-40 @ 640 mV_{pp} fin=2 MHz	-49 @ 2 V_{pp} fin=100 KHz	-40 @ 700 mV_{pp}	-49 @ 1.2 V_{pp} fin= 5 MHz
Noise rms	397 µV	1.69 mV	-	198 µV	650 µV	155 µV
DR (dB)	51	52	60	77	52	69
Power (mW)	60	90	60	26	40	450
FOM (J)	$4,29x10^{-11}$	$1,50x10^{-10}$	$5,14x10^{-10}$	$6,19x10^{-9}$	$1,14x10^{-10}$	$1,89x10^{-9}$

VII. References

[1] F. Behbahani et al. “Adaptive Analog IF Signal Processor for a Wide-Band CMOS Wireless Receiver”, *IEEE J. Solid-State Circ.*, Vol. 36, pp. 1205-1217, Aug. 2001.

[2] Z.-Y. Chang, D. Haspeslagh, and J. Verfaillie, “A highly linear CMOS Gm-C bandpass filter with on-chip frequency tuning”, *IEEE J. Solid-State Circ.*,Vol. 32 , pp. 388 - 397, Mar. 1997.

[3] Y. P. Tsividis, and J.O. Voorman, *Integrated Continuous-time Filters*, IEEE Press, New York, 1993.

[4] N. P. J. Greer et al. “Matrix methods for the design of transconductor ladder filters”, *IEE Proc. Circ., Dev. and Sys.*, Vol. 141, pp. 89-100, 1994.

[5] Y. P. Tsividis, “Integrated Continuous-Time Filter Design– An Overview”, *IEEE J. Solid-State Circ.*, Vol. 29, pp. 166-176, Mar. 1994.

[6] G. Groenewold.”The Design of High Dynamic Range Continuous-Time Integratable Bandpass Filters”, *IEEE Trans. Circuits and Systems,* Vol. 38, pp. 838-852, Aug. 1991.

[7] J.F. Fernández-Bootello, M. Delgado-Restituto, A. Rodríguez-Vázquez, “System-Level Optimization of Baseband Filters for Communication Applications”. *Microetechnologies for the New Millennium 2003*, Maspalomas, Spain, May 2003.

[8] J. Silva-Martinez et al. "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system," *Solid-State Circuits, IEEE Journal of*, Vol. 38, Iss. 2, pp. 216-225, 2003.

[9] M. Chen et al. "A 2-V/sub pp/ 80-200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *Solid-State Circuits, IEEE Journal of*, Vol. 38, Iss. 10, pp. 1745-1749, 2003.

[10] I. Mehr and D. R. Welland, "A CMOS continuous-time G_m-C filter for PRML read channel applications at 150 Mb/s and beyond," *Solid-State Circuits, IEEE Journal of*, Vol. 32, Iss. 4, pp. 499-513, 1997.

[11] F. Yang and C. C. Enz, "A low-distortion BiCMOS seventh-order Bessel filter operating at 2.5 V supply," *Solid-State Circuits, IEEE Journal of*, Vol. 31, Iss. 3, pp. 321-330, 1996.

[12] F. Rezzi et al. "A 70-mW seventh-order filter with 7-50 MHz cutoff frequency and programmable boost and group delay equalization," *Solid-State Circuits, IEEE Journal of*, Vol. 32, Iss. 12, pp. 1987-1999, 1997

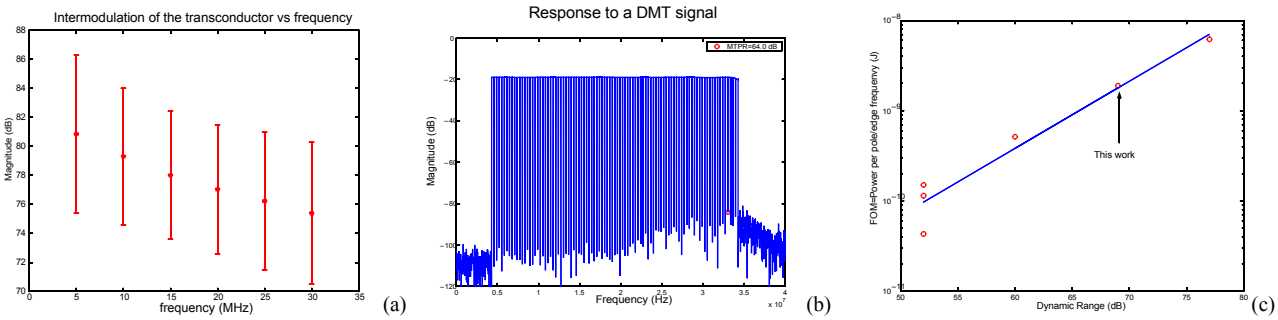

Fig. 6. a) Intermodulation of the transconductor vs frequency. b) Response of the filter to a DMT signal. and c) Comparison of several filter design