

# SOFT-SWITCHED STEP-UP MEDIUM VOLTAGE POWER CONVERTERS

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A DISSERTATION SUBMITTED TO  
THE FACULTY OF GRADUATE STUDIES  
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS  
FOR THE DEGREE OF  
DOCTOR OF PHILOSOPHY

GRADUATE PROGRAM IN  
ELECTRICAL ENGINEERING AND COMPUTER SCIENCE  
YORK UNIVERSITY  
TORONTO, ONTARIO

August 2019

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## Abstract

With a ten-year average annual growth rate of 19 percent, wind energy has been the largest source of new electricity generation for the past decade. Typically, an offshore wind farm has a medium voltage ac (MVac) grid that collects power from individual wind turbines. Since the output voltage of a wind turbine is too low (i.e., typically 400 – 690 V) to be connected to the MVac grid (i.e., 20 – 40 kV), a heavy line-frequency transformer is used to step up the individual turbine's output voltage to the MV level. To eliminate the need for bulky MVac transformers, researchers are gravitating towards the idea of replacing the MVac grid with a medium voltage dc (MVdc) grid, so that MV step-up transformers are replaced by MV step-up power electronic converters that operate at the medium frequency range with much lower size and weight.

This dissertation proposes a class of modular step-up transformerless MV SiC-based power converters with soft-switching capability for wind energy conversion systems with MVdc grid. This dissertation consists of two parts: the first part focuses on the development of two novel groups of step-up isolated dc-dc MV converters that utilize various step-up resonant circuits and soft-switched high voltage gain rectifier modules. An integrated magnetic design approach is also presented to combine several magnetic components together in the modular high voltage gain rectifiers. The second part of this dissertation focuses on the development of several three-phase ac-dc step-up converters with integrated active power factor correction. In particular, a bridgeless input ac-dc rectifier is also proposed to combine with the devised step-up transformerless dc-dc converters (presented in the first part) to form the three-phase soft-switched ac-dc step-up voltage conversion unit. In each of the presented modular step-up converter configurations, variable frequency control is used to regulate the output dc voltage of each converter module. The operating principles and characteristics of each presented converter are provided in detail. The feasibility and performance of all the power converter concepts presented in this dissertation are verified through simulation results on megawatts (MW) design examples, as well as experimental results on SiC-based laboratory-scale proof-of-concept prototypes.

*to my parents,  
my lovely wife, Farnaz,  
and my sister*

## **Acknowledgment**

There are no appropriate words to convey my deep gratitude and respect to my supervisor, Dr. John Lam. His invaluable guidance, encouragement and strong technical insights were instrumental in completing this work. I appreciate all his contributions of time, ideas, and financial support to make my Ph.D. experience productive and stimulating.

I also wish to express my thanks to the members of the dissertation examining committee: Dr. Ali Hooshyar, Dr. Hany Farag, Dr. S. Ali Khajehoddin, Dr. Sebastian Magierowski, and Dr. Paul G. O'Brien. I am grateful for their valuable advice and feedback.

I would like to offer my thanks to all graduate students in the Power Electronics Laboratory for Sustainable Energy Research (PELSER) for many productive discussions over the past few years.

I deeply thank my parents for giving me strength, love, and support to reach for the stars and chase my dreams. Words cannot express how grateful I am to my mother and father for the countless sacrifices they have made for me. Without you, I would not be the person I am today. My sister, Maryam, also deserves my wholehearted thanks. Without her supports, love, and encouragement, I would not be able to pursue my studies in the PhD level and begin this journey. Also, I express my gratitude to my parents-in-law for their unconditional support.

Above all, I owe thanks to a very special person, my wife, Farnaz, for her continued and unfailing love, support, and understanding during my pursuit of Ph.D. degree that made the completion of thesis possible. Thank you for your unwavering belief in me to get through the tough times. To have a woman of such infinite talent and dynamism, put her own professional career on hold to be with me, and support me, is my most precious possession. I owe you everything.

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# List of Abbreviations

<b>AC</b>	Alternating Current
<b>APWM</b>	Asymmetrical Pulsewidth Modulation
<b>BCM</b>	Boundary Conduction Mode
<b>CAGR</b>	Compound Annual Growth Rate
<b>CCM</b>	Continuous Conduction Mode
<b>DAB</b>	Dual Active Bridge
<b>DC</b>	Direct Current
<b>DCM</b>	Discontinuous Conduction Mode
<b>DFIG</b>	Doubly-Fed Induction Generator
<b>DSP</b>	Digital-Signal Processing
<b>EDF</b>	Extended Describing Function
<b>EMF</b>	Electromotive Force
<b>EMI</b>	Electromagnetic Interference
<b>FHA</b>	First Harmonic Approximation
<b>GaN</b>	Gallium Nitride
<b>GWEC</b>	Global Wind Energy Council
<b>HFT</b>	High Frequency Transformer
<b>HGR</b>	High Gain Rectifier
<b>HV</b>	High Voltage

<b>HVac</b>	High Voltage AC
<b>HVdc</b>	High Voltage DC
<b>ICS</b>	Input Current Sharing
<b>IGBT</b>	Insulated-Gate Bipolar Transistor
<b>IPOP</b>	Input Parallel Output Parallel
<b>IPOS</b>	Input Parallel Output Series
<b>ISOP</b>	Input Series Output Parallel
<b>ISOS</b>	Input Series Output Series
<b>KCL</b>	Kirchhoff's Current Law
<b>KVL</b>	Kirchhoff 's Voltage Law
<b>LFT</b>	Low Frequency Transformer
<b>LPF</b>	Low Pass Filter
<b>LV</b>	Low Voltage
<b>MFT</b>	Medium Frequency Transformer
<b>MOSFET</b>	Metal Oxide Semiconductor Field Effect Transistor
<b>MPPT</b>	Maximum Power Point Tracking
<b>MV</b>	Medium Voltage
<b>MVac</b>	Medium Voltage AC
<b>MVdc</b>	Medium Voltage DC
<b>OCS</b>	Output Current Sharing
<b>OVS</b>	Output Voltage Sharing
<b>PFC</b>	Power Factor Correction
<b>PI</b>	Proportional Integral
<b>PID</b>	Proportional Integral Derivative
<b>PMSG</b>	Permanent Magnet Synchronous Generator

<b>PWM</b>	Pulsewidth Modulation
<b>RMS</b>	Root Mean Square
<b>SC</b>	Switched Capacitor
<b>SCIG</b>	Squirrel-Cage Induction Generator
<b>Si</b>	Silicon
<b>SiC</b>	Silicon Carbide
<b>SSA</b>	State Space Averaging
<b>VCO</b>	Voltage Controlled Oscillator
<b>VMR</b>	Voltage Multiplier Rectifier
<b>WBG</b>	Wide-Bandgap
<b>WECS</b>	Wind Energy Conversion Systems
<b>WRIG</b>	Wound Rotor Induction Generator
<b>WRSG</b>	Wound Rotor Synchronous Generator
<b>ZCS</b>	Zero Current Switching
<b>ZVS</b>	Zero Voltage Switching

## Chapter 1 Introduction

The global reliance on clean renewable power generation is increasing. The share of renewables in the growth of electricity generation capacity has increased from about 25% in 2001 to 63% in 2018 [1]. In particular, wind energy is one of the fastest-growing renewable energy sources in the world. According to the Global Wind Energy Council (GWEC), the total installed wind power capacity worldwide reached 519 GW in 2018 with 568 GW onshore and 23 GW offshore installations [2]. Figure 1.1 shows the global cumulative installed wind capacity from the years 2001 to 2018.

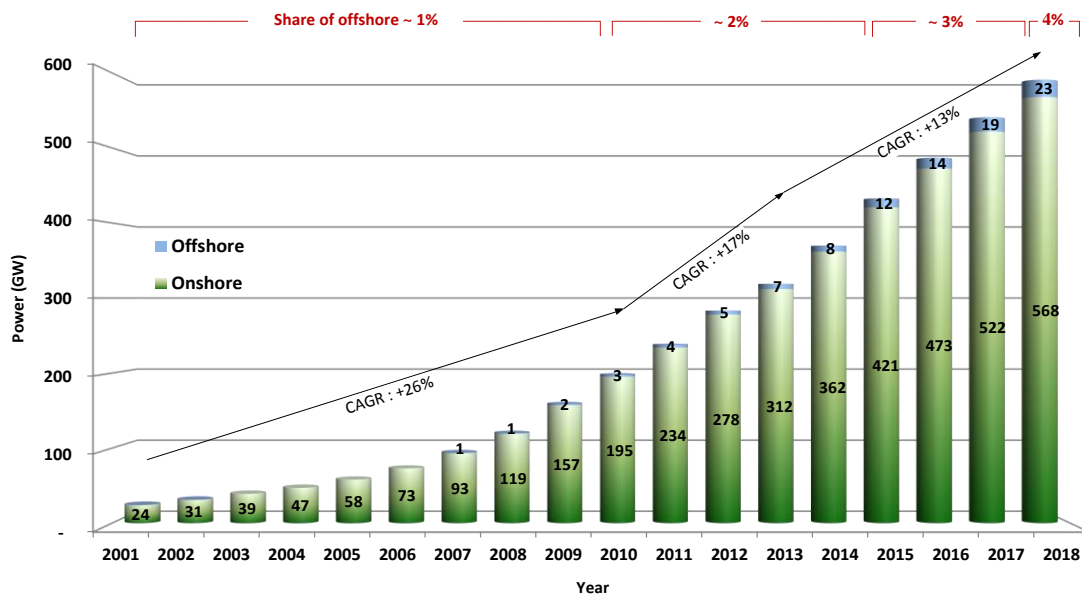


Figure 1.1– Global cumulative installed wind capacity

The performance of wind energy system can be greatly enhanced with the use of a full-scale power converter in Type IV turbine. A list of some recent multi-megawatt commercial wind turbines is given in Table 1.1 [3]–[5]. The table shows that today, Type IV turbine with PMSG is the dominant technology in the market. It can be also observed that the most standard generator voltage level is 690 V even for up to 8 MW wind turbines.

Table 1.1– List of Commercial Type 3 and Type 4 Megawatt Wind Turbines

Manufacturer, Country	Model Number	Power	Generator Type, Rated Voltage	Hub Height Rotor Diameter
GE Energy USA	Haliade-X	12.0MW	PMSG, 6.6kV	150m 220m
	Haliade 150	6.0MW	PMSG, 900V	100m 150.8m
	GE4.1-113	4.1MW	PMSG, 690V	85m 113m
	GE3.6S	3.0MW	DFIG, 690V	80m 104m
	GE2.5XL	2.5MW	PMSG, 690V	75/85/100m 100m
Siemens Germany	SWT-8.0-154	8.0MW	PMSG, 690V	site-specific 154m
	SWT-7.0-154	7.0MW	PMSG, 690V	site-specific 154m
	SWT-6.0-154	6.0MW	PMSG, 690V	120 154m
	SWT-3.3-130	3.3MW	PMSG, 690V	85/110/120/135m 130m
Enercon GmbH Germany	E126/7580	7.58MW	WRSG, 690V	135m 127m
	E126/6000	6.0MW	WRSG, 690V	135m 126m
	E112/6000	6.0MW	WRSG, 440V	124m 114m
	E112/4500	4.5MW	WRSG, 440V	120m 114m
Vestas Denmark	V112	3.3MW	PMSG, 650V	84/140m 112m
	V100	2.5MW	PMSG, 690V	100m 99.8m
	V80	2.0MW	DFIG, 690V	60/100m 80m
Goldwind China	GW136	4.2MW 4MW	PMSG, 690V	100/110m 136m
	GW140/3000	3.0MW	PMSG, 690V	100/120m 140m
	GW70/1500	1.5MW	PMSG, 690V	85m 70m

## 1.1 Wind Farm Configurations

A wind farm consists of tens or hundreds of wind turbines, which increase the produced electricity and minimize the required land area. Many configurations have been introduced in the literature, but considering the cost, efficiency, reliability, and performance of the wind farm, only a few of them have been implemented practically. Parallel and series topologies are the most practical and promising wind farm configurations that are presented in this section. While the series connection increases the voltage and power rating, the parallel connection of wind turbines offer more reliable and robust technology with increasing the current and power capacity [6]. The current wind farms mainly use the parallel connection. In terms of the transmission systems, the high voltage ac (HVac) systems are mainly used for low power wind farms, which are located close to the utility grid. For power ratings and distances greater than 400 MW and 60 km, the high voltage dc (HVdc) transmission is the most preferable choice [5], [7], [8].

### 1.1.1 Parallel AC Configuration with HVac Transmission

The parallel ac power architecture of a wind farm consists of a medium voltage ac (MVac) grid and HVac transmission as shown in Figure 1.2. The most standard voltage range for the current wind turbine generators is 400 – 690 V. This range of generator output voltage is too low to be directly connected to the high voltage transmission lines. Therefore, each wind turbine consists of a medium voltage (MV) transformer to step-up the turbine's output to the medium voltage level (i.e., 11–34.5 kV, with the most common collection point voltages being 34.5 and 33 kV in North America and Europe, respectively [5]). To form an MVac collection system, the three-phase

output terminals from the step-up transformers are connected in parallel. The MVac is then stepped up to HVac in the range of 60–245 kV by the HV transformer in a wind farm substation [7], [8]. All types of wind turbines can be used to form this wind farm configuration as the step-up transformers are a common element in all these configurations. The previous offshore wind farms located near to shore also used parallel ac with HVac architecture. The advantages of this configuration are simplicity and low initial cost for the wind farm substation. However, it has a few disadvantages. As the power ratings of commercial wind turbines increase [9], the ac cables connecting the turbine and the MV transformer will have to carry more current as the output voltage of the turbine is low. These cables are expensive and suffer substantial amounts of power loss [10].

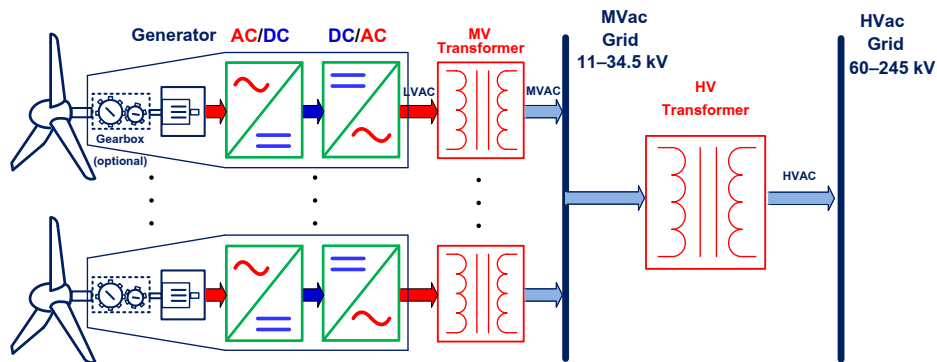


Figure 1.2– Parallel ac with HVac based onshore wind farm configuration

### 1.1.2 Parallel AC Configuration with HVdc Transmission

Parallel ac configuration of a wind farm with HVdc transmission is shown in Figure 1.3. This is the most typical power architecture for distant offshore wind farms with high power capacity. Similar to the previous structure, it consists of an MVac grid that is connected to a high turns-

ratio transformer to step up the voltage to HVac. The HVac is then converted to HVdc through ac-dc converters. The bulky HV transformer and ac-dc converter are located in an offshore platform that is connected to the onshore substation through submarine HVdc cables [11]. This technology is robust and reliable. However, it requires high maintenance and initial cost. The high number of the stages also causes a considerable increase in weight and volume, which leads to higher installation cost [12]. A high-power density can be obtained by replacing the bulky 50/60 Hz transformers with high-frequency transformers [13]–[15]. But high-frequency transformers with high turns-ratio are difficult to design at high voltages and megawatt power levels due to the high cost of the magnetic material, core and dielectric losses [16], [17].

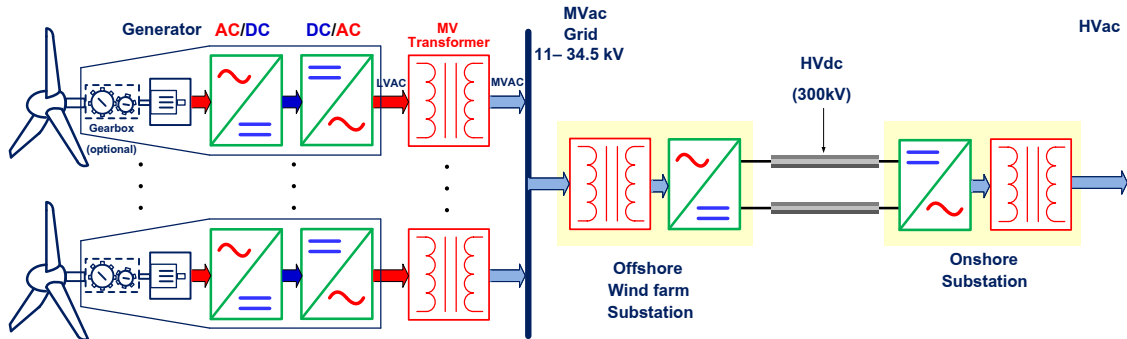


Figure 1.3– Parallel ac with HVdc based offshore wind farm configuration

### 1.1.3 Series DC Configuration with HVdc Transmission

Figure 1.4 shows the series dc configuration of a wind farm with HVdc transmission [18], [19]. In this architecture, the output dc voltages of the ac-dc converters are connected in series to achieve an HVdc level. An example of an offshore wind farm employing this interconnection approach is Nordsee Ost offshore wind farm in Germany, where 60 wind turbines, with 5 kV output voltage each, are connected in series to reach a transmission HVdc voltage of 300 kV [5].

As illustrated in Figure 1.4, the dc-ac converters and the offshore platform are not required in this configuration. Compared to the parallel connection, the length of cable is shorter and the number of converters is less, leading to an improvement in the efficiency, and reduction in the weight and cost. To isolate a wind turbine from the dc network during maintenance or down times, a bypass switch is usually connected across the dc-link of each ac-dc converter. One challenge of this structure is that the variation in wind speed results in fluctuations in output voltage and consequently output power. Moreover, if large numbers of wind turbines are bypassed due to the unexpected problems, the entire wind farm may have to be shut down as the transmission dc voltage falls below the threshold limit [5]. The insulation in the nacelle is also another challenge as it's directly connected to HVdc line [6].

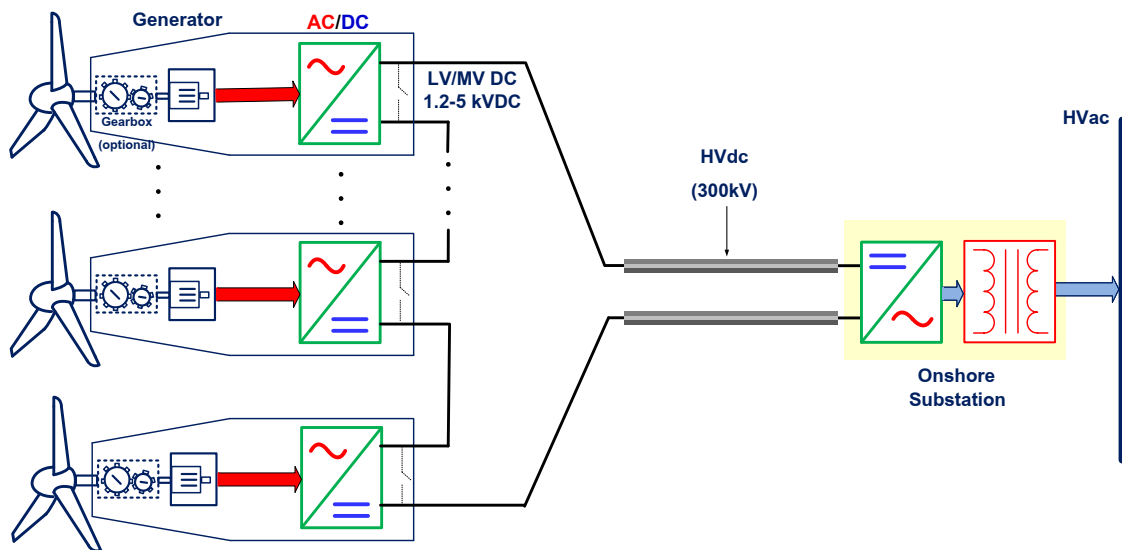


Figure 1.4– Series dc with HVdc based offshore wind farm configuration

### 1.1.4 Parallel DC Configuration with HVdc Transmission

Figure 1.5 shows the power system configuration with a medium voltage dc (MVdc) grid, where the MV transformers are replaced by MV step-up dc-dc converters [20]–[22]. The intermediate dc-dc converter steps up the dc voltage to (MVdc) and the parallel connections of the output MVdc voltages build the MVdc collection system. A central step-up dc-dc converter is then used to step-up the MV to high voltage (e.g. >300 kV) for high voltage dc (HVdc) power transmission. The configuration of HVdc transmission and receiving-end substation are similar to the previous configuration.

By operating the MVdc converter at medium frequency, the weight, and the size of a converter is becoming much smaller than the MV step-up transformer. Therefore, the overall system size and weight as well as the construction and installation cost of the wind turbine and substation platform reduce significantly, compared to parallel ac configurations in sections 1.1.1 and 1.1.2.

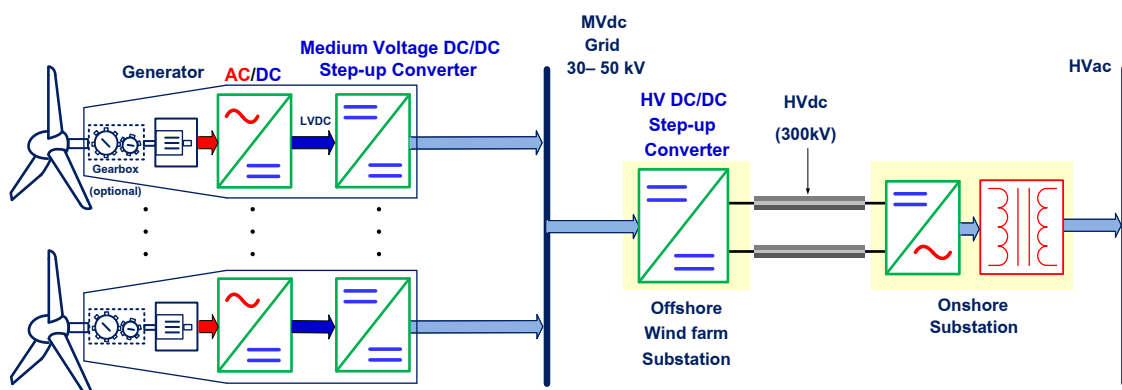


Figure 1.5– Parallel dc with HVdc based offshore wind farm configuration

Another reason to support the concept of an MVdc grid is that the offshore wind farms are increasingly being located further from shore [23]. As an example, German's Global Tech II farm, with a capacity of 486 MW, is nearly 100 km out to sea [24]; or Hornsea, the largest offshore wind farm in the world, with the entire capacity of up to 6 GW is planning to be located 120 km from shore in England [25]. This far distance to the shore has made high voltage dc (HVdc) a necessity in transporting offshore wind energy to customers on shore to eliminate reactive power requirements and reduce cabling cost and complexity [11], [26].

## **1.2 Technical Challenges and Possible Solutions**

To integrate the wind turbine generators into a medium voltage grid (e.g., 11–34.5 kV), a high turns-ratio transformer is commonly used to step up the voltage, as discussed in section 1.1. The power transformer operated at the frequency of 50/60 Hz is heavy, large, and inefficient, and is typically located either inside the nacelle of the turbine or at the tower base, as shown in Figure 1.6. If located inside the nacelle, which is the case in offshore wind turbines, the bulky dry-type transformer increases the weight and volume of the nacelle and imposes a significant mechanical stress to the tower. For example, the weight and volume of a 0.69/33 kV, 2.6 MVA dry-type transformer is typically in the range of 6–8 t and 5–9 m<sup>3</sup>, respectively [27]. In the latter scenario, where a transformer is placed near or within the tower base, multiple high current three-phase ac cables are required. These cables are expensive and they can suffer a substantial amount of power loss that reduces the overall efficiency. Ground-mounted transformers in this case, are typically liquid-filled and used for onshore wind farm applications. Several vendors

have been developing special transformers for wind energy applications aiming to reduce the size and weight with the consideration of environmental concerns. For instance, the SLIM transformers developed by Pauwels are compact in size and have low no-load losses [28]. Unlike the conventional liquid-filled transformers that use cellulose and mineral oil, SLIM transformers use a high temperature aramid insulation material called NOMEX and silicone liquid with a high degree of fire safety. But a high volume of liquid in step-up transformers requires regular monitoring and replacement. These challenges are critical in offshore and remote area applications where the costs of installation and regular maintenance are extremely high [29]. Table 1.2 compares the specifications of various 0.69/33 kV transformers used in the wind industry [28], [30], [31].

One way to solve the aforementioned drawbacks is to employ a modular converter system approach, where multiple low voltage rating converter modules are connected in series to achieve the required MV output [10], [32]. In [5], [33], [17] different types of multilevel and modular multilevel converter configurations have also been presented for this application. However, due to the large amount of

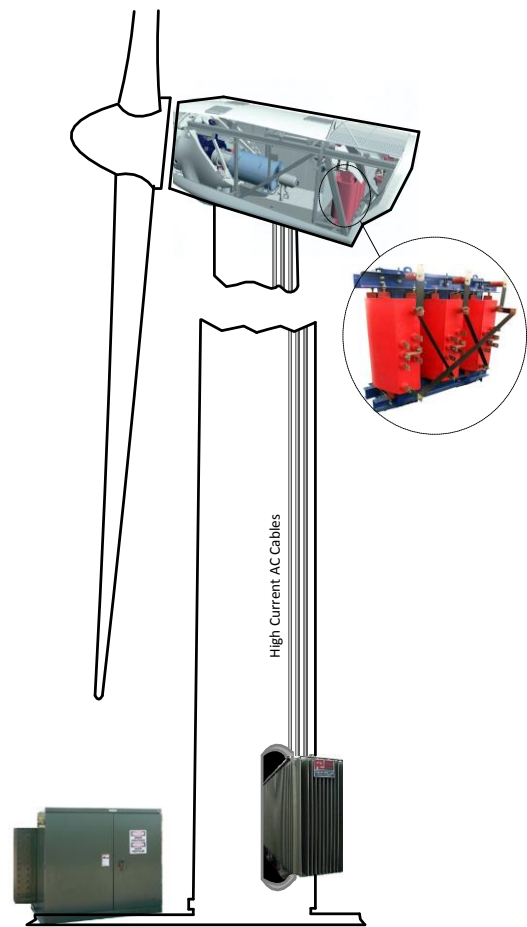


Figure 1.6– Housing of power transformer in wind turbine

components, multilevel converters are relatively heavy, bulky and expensive. Moreover, their efficiency deteriorates as the number of levels increase. Multilevel converters will be discussed further in section 1.4.1.4.

Table 1.2– Summary of Transformers Specifications

Transformer type	Vendor	Rating (MVA)	Size (m <sup>3</sup> )	Weight (kg)	No-load loss (kW)	Full-load loss (kW)	Liquid (kg)
Dry-type	ABB	2.5	8.50	6,200	5.80	25.00	–
Liquid filled	ABB	2.00	5.70	4,530	3.20	21.00	870
SLIM	Pauwels	2.30	4.00	5,040	2.60	22.50	900

As discussed in section 1.1.4, the use of an MVdc grid has been presented as an alternative and attractive power architecture so that medium-to-high frequency MV converters can be used to replace the bulky low frequency MV transformers. As individual wind turbine size as well as overall wind farm size increases, there is a corresponding increase in the cable lengths within the wind farm collection grid, introducing more conduction power losses. The use of a MVdc grid also offers the advantage of not requiring any ac reactive power compensation within the grid [34]. The growing inter turbine spacing, combined with the necessity of using an HVdc link to shore makes use of an MVdc collection grid architecture more suitable for aggregating wind turbine energy compared to the traditional MVac alternative. The typical MVdc power converter configurations, as shown in Figure 1.5 consist of two stages: the front-end ac-dc stage and the step-up dc-dc voltage conversion stage. The generator side ac-dc converter can be unidirectional or bidirectional; as the synchronous generators does not need reactive power compensation. The MV step-up dc-dc converter is a key component in offshore wind systems with an MVdc grid, as

it needs to be highly efficient and be able to provide high voltage gain to step-up the turbine output voltage. Several works on MV step-up dc-dc converter have been presented for this application [12], [17], [22], [26], [35]–[40].

### **1.3 Semiconductor Devices Advancement**

Since the invention of the bipolar junction transistor, Silicon (Si)-based power semiconductor devices have gone through many generations of development in the past 50 years. However, they have many limitations in terms of blocking voltage capability, operation temperature, conduction and switching losses, and switching frequency [41]. Due to the limited performance, the cooling system, larger filter and passive components, and series connections of Si semiconductors are required in the power converters. Recently, wide-bandgap (WBG) switching devices have emerged with promising characteristics. In general, WBG refers to electronic energy bandgaps significantly larger than one electron volt (eV). The term is mostly a way of distinguishing other semiconductors from Silicon with 1.1 eV. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most-well known and commercially available wide-bandgap devices that can offer exceptional characteristics, such as low turn-ON resistance, fast switching speed, high operating temperature, and high breakdown electric field. Figure 1.7 highlights the key electrical characteristics of Si, SiC, and GaN materials. According to this figure, GaN material presents low ON-state loss, better high frequency, and high voltage capability; however, compared to SiC, its thermal conductivity is lower.

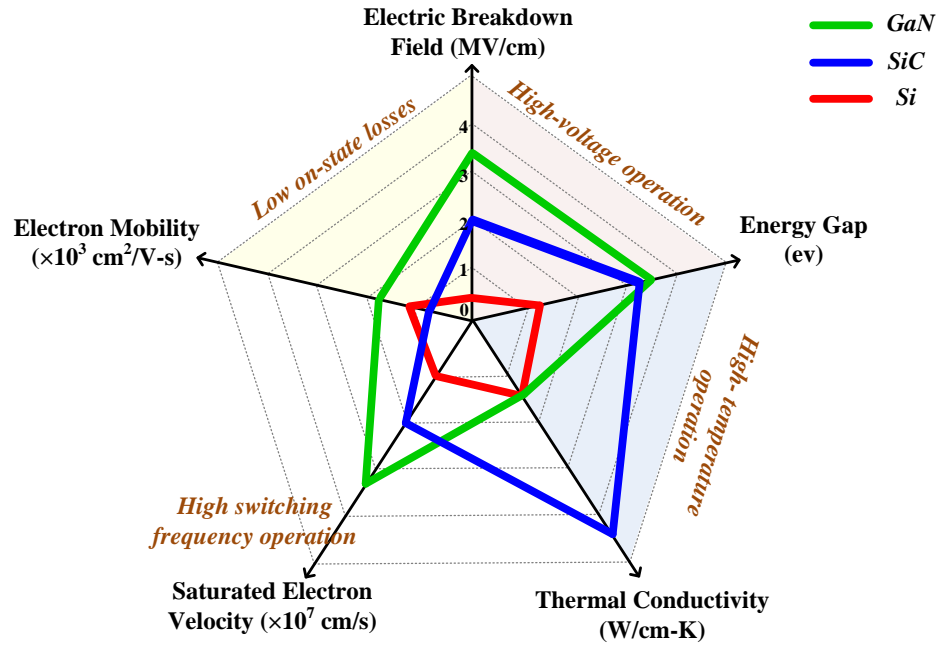




Figure 1.7– Summary of Si, SiC, and GaN relevant materials properties

A summary of Si, SiC and GaN-based applications status with different frequency ranges and rated power is shown in Figure 1.8. It can be observed that for medium voltage applications, such as wind turbines, IGBT devices are currently being used for 600 V to 6.5 kV with operating frequencies of up to 10 kHz [42]. The highest voltage rating of the commercially available IGBTs is 6.5 kV, which is suitable for 2.88 kV or lower voltage converter systems with traditional two-level converters [29]. With further increase in voltage, other solutions, such as the series or cascaded connections of IGBTs or using SiC modules, should be considered. Although the series connections of IGBTs can reduce the stress of voltage across each switch, the need for extra snubber circuits for voltage balancing, control complexity, low efficiency, and high volume restrict the performance of this approach. On the other side, SiC IGBTs and

MOSFETs are gaining increasing attention in high voltage high power applications. SiC power devices with their higher voltages ( $>6.5$  kV), higher switching frequencies, and higher operating temperatures ( $200^{\circ}\text{C}$ ) compared to their Si IGBT counterparts, have had a major impact on medium voltage applications. The use of high voltage rated devices may increase the switching and conduction losses of the converter. Moreover, the price of power semiconductor devices increases rapidly with their voltages and power ratings. Therefore, reducing the stress of voltage across each semiconductor device offers using low-rated WBG devices that improve performance and reduce cost. Table 1.3 shows a comparison between 1.2 kV and 1.7 kV SiC half-bridge modules. It can be seen that the price of the 1.7 kV SiC MOSFET is two times higher than the 1.2 kV module with the same rated current.

Table 1.3– A Comparison Between 1.2kV and 1.7kV SiC Half-bridge Modules [43]

Part Number	Manufacturer	FET Type	$V_{\text{dss}}$ <sup>1</sup>	$I_{\text{d}}$ <sup>2</sup>	$R_{\text{ds(on)}}$	$C_{\text{iss}}$ <sup>3</sup>	Price per unit
 APTSM120AM14CD3AG	Microsemi	SiC MOSFET 2 N-Channel	1.2 kV	337 A	11 m $\Omega$	23 nF	612 CAD
 CAS300M17BM2	Cree/Wolfspeed	SiC MOSFET 2 N-Channel	1.7 kV	325 A	10 m $\Omega$	20 nF	1,213 CAD

<sup>1</sup> Drain to source voltage

<sup>2</sup> Current - continuous drain ( $I_{\text{d}}$ ) @  $25^{\circ}\text{C}$

<sup>3</sup> Input capacitance ( $C_{\text{iss}}$ ) (Max) @  $V_{\text{ds}}$

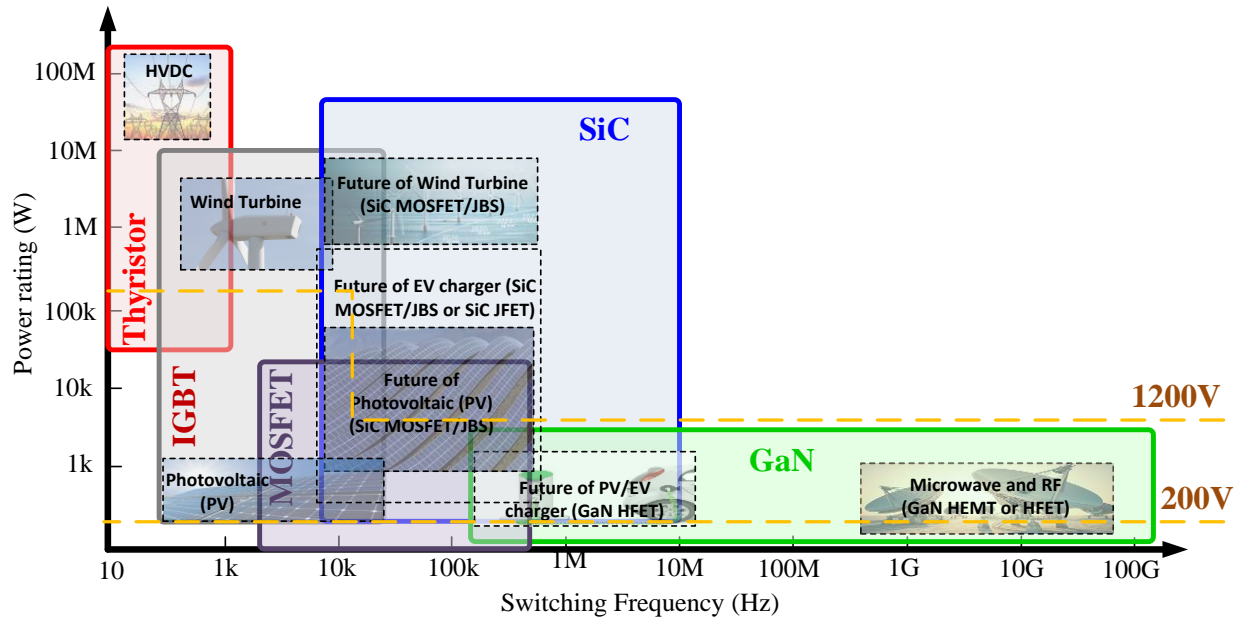


Figure 1.8–Summary of Si, SiC and GaN-based applications status [42]

## 1.4 Power Converters for Medium Voltage DC (MVdc)

Typical power converters for the MW medium voltage dc (MVdc) consist of two stages: the front-end ac-dc rectifier and the dc-dc step-up converter. The generator side ac-dc rectifier can be unidirectional or bidirectional, as the synchronous generator does not need reactive power compensation. The maximum power point tracking (MPPT) is implemented at the front-end rectifier stage and the dc-dc grid side converter performs the output voltage (MV) regulation. The key function of the dc-dc converter is to provide step-up voltage conversion. Different types of MV step-up dc-dc converters are discussed in the following sections.

### 1.4.1 Existing MV Step-Up DC-DC Converter

Various voltage boosting techniques in dc-dc converters have been presented in the literature. These step-up converters can be classified into 4 major techniques: switched capacitor based step-up converters, resonant converters, high frequency step-up transformers, and converters with multi stage/level structures [40]. In the following section, the general structures of these techniques are illustrated and their major merits and drawbacks are presented.

#### 1.4.1.1 Switched Capacitor Based Converters

Switched capacitor (SC) is a well-known boosting technique that has been employed for MVdc grid applications [12], [35], [44], [45]. A basic switched capacitor voltage doubler is shown in Figure 1.9. In the first phase, capacitor  $C_1$  is charged to the input voltage. In the second phase, capacitor  $C_1$  is placed in series with the input source, which ideally doubles the output voltage level [46]. For higher voltage gains, the basic switched capacitors can be connected in series, series-parallel or ladder connection. For instance, based on a ladder connection, a resonant switched capacitor was presented in [35]. Figure 1.10 shows the circuit configuration of the switched capacitor based resonant converter that can step up the voltage  $m+n+1$  times. The converter has the advantage of achieving zero current switching (ZCS) for all the semiconductor devices. However, the magnitude of the transistor current is dependent on the number of cells used in the topology. As the number of cells increases to provide the required output MV level, the switches suffer more and more conduction loss. This converter can achieve high voltage gain and soft switching operation only when the duty ratio is 0.5, which decreases the degree of

control freedom. As a result, the resonant switched capacitor presented in the literature does not provide output voltage regulation at the MVdc grid. Instead, the output voltage regulation is performed by the cascaded HVdc stage. In order to regulate the output voltage against the load variation, a low power buck-boost converter has been suggested in [47] which can be connected in series with the switched capacitor converter. Adding an extra conversion stage for the purpose of merely voltage regulation, however, does not seem to be an efficient method.

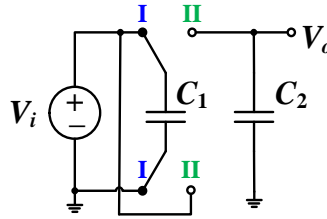


Figure 1.9– Basic switched capacitor

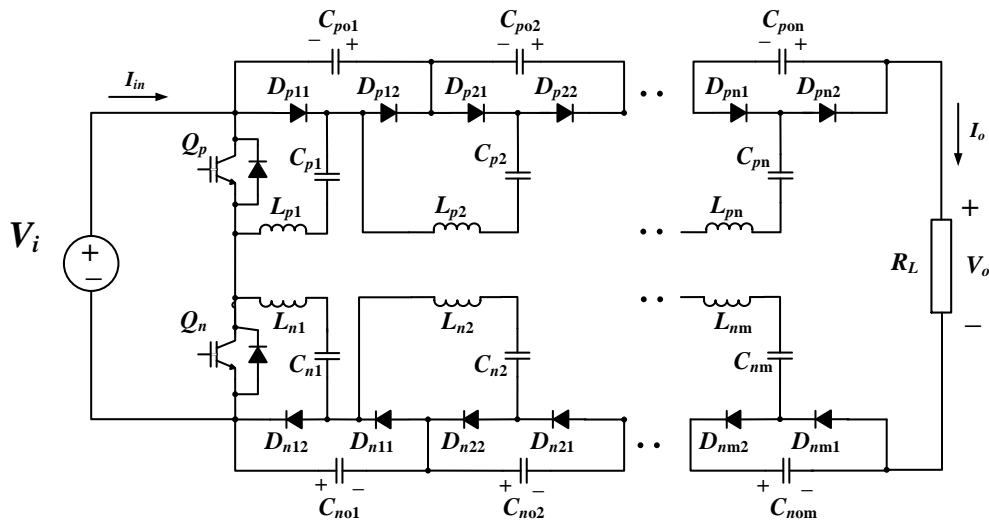


Figure 1.10– ZCS resonant switched capacitor converter

### 1.4.1.2 Resonant Converters

Because of their soft-switching capability, resonant converters are attractive for use in MVdc systems with reduced switching power losses [48]–[51]. Different resonant circuit structures can be used to achieve step-up voltage conversion. A standard dc-dc resonant converter is illustrated in Figure 1.11. The switch network generates a square-wave voltage  $v_s(t)$  with a switching frequency of  $f_s$ . This voltage is applied to the input terminals of a resonant tank network that consists of passive circuit components, such as inductors ( $L$ ) and capacitors ( $C$ ). In some cases, a resonant tank network will also include a transformer. The output of the resonant tank network is then rectified into a dc voltage or current by the diode rectifier and a low-pass-filter (LPF) circuit. By changing the switching frequency of the resonant tank network, the magnitudes of output voltage (or output current) can be controlled.

The three basic resonant circuits are  $LC$  series resonant,  $LC$  parallel resonant and  $LCC$  series-parallel resonant. The voltage gain plots of these resonant circuits are shown in Figure 1.12. Figure 1.12(a) shows the voltage gain of  $LC$  series-resonant converter as a function of relative operating frequency ( $f_s/f_0$ ), where  $f_0$  is the corner frequency of the resonant circuit and is given by (1.1). It can be observed that the maximum voltage gain in series resonant converters is always equal to one, regardless of any changes in the quality factor ( $Q$ ).

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (1.1)$$

The main disadvantage of  $LC$  series-resonant converters is that the output voltage cannot be regulated at light load conditions. The voltage gain characteristic of an  $LC$  parallel resonant

circuit is shown in Figure 1.12(b). Compared to the series resonant circuit, the parallel resonant topology does not require a wide range of switching frequencies to maintain output voltage regulation. However, high circulating energy at light load conditions is the main drawback of a parallel resonant converter as it significantly reduces the light load efficiency. In addition, the circulating current increases as the input voltage increases. Hence, this converter is not suitable for applications with a high input voltage range [52]. To overcome the shortcomings of *LC* series and parallel resonant circuits, resonant tank circuits with a third circuit element (either an inductor or a capacitor) were presented [53]–[55]. Among the 26 possible topologies, the *LCC*, *LLC*, and *CLL* are the most well-known three-element resonant converters [55]. Figure 1.12(c) shows the voltage gain of series-parallel or *LCC* resonant converters as a function of the relative operating frequency ( $f_s/f_0$ ). This converter combines the properties of both series and parallel resonant converters by absorbing their merits and mitigating their drawbacks. However, the *LCC* resonant converter is dominated by parallel resonant frequency and subsequently presents the same shortcomings. High circulating current in *LCC* resonant converters may lead to lower converter efficiency and increase the current stress. In addition, *LCC* resonant converters cannot achieve zero current switching (ZCS) on the rectifier network.

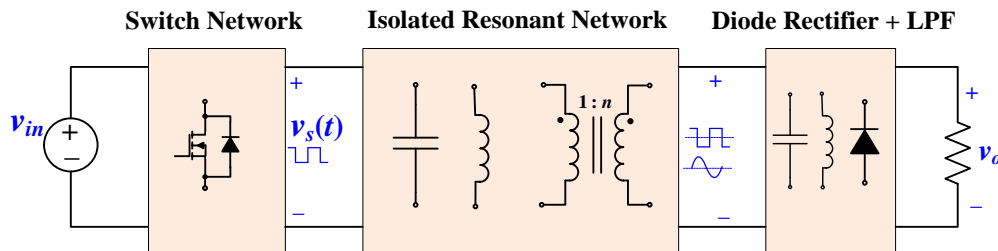
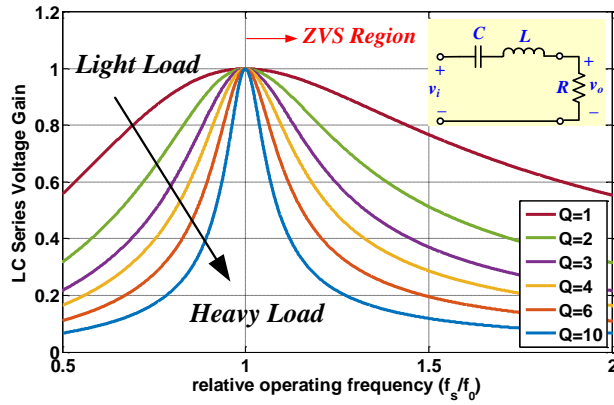
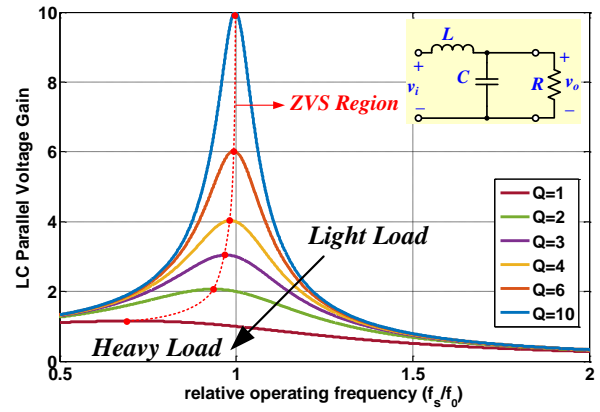


Figure 1.11– Conventional resonant converter structure



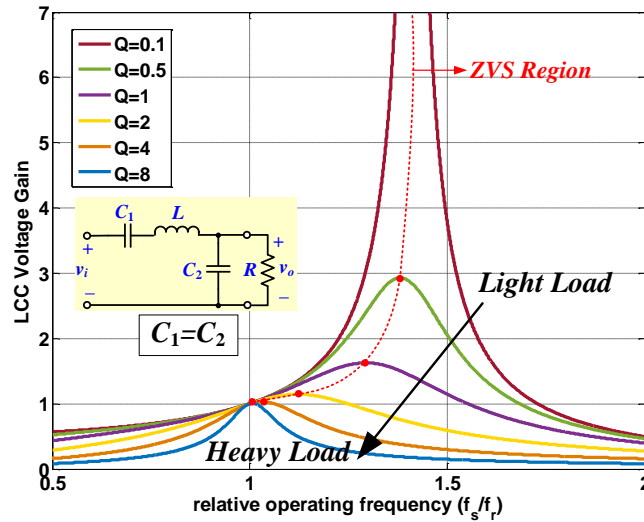
$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{1 + Q^2 \left( \omega_r - \frac{1}{\omega_r} \right)^2}} \quad \text{where; } Q = \frac{L\omega_0}{R}$$

a) LC series resonant converter voltage gain



$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{(1 - \omega_r^2)^2 + \left( \frac{\omega_r}{Q} \right)^2}} \quad \text{where; } Q = \frac{R}{L\omega_0}$$

b) LC parallel resonant converter voltage gain



$$\left| \frac{v_o}{v_i} \right| = \frac{1}{\sqrt{(2 - \omega_r^2)^2 + Q^2 \left( \omega_r - \frac{1}{\omega_r} \right)^2}} \quad \text{where; } Q = \frac{L\omega_0}{R}$$

c) LCC series-parallel resonant converter voltage gain

Figure 1.12– Voltage gain characteristics of the basic resonant circuits

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### 1.4.1.3 High Frequency Step-Up Transformers

High frequency transformer (HFT)-based dc-dc converters are the subject of increasing research interest due to their compact size and ability to provide high voltage gain. There are several types of dc-dc converters that incorporate high frequency transformers in their switching network layouts. An active-bridge step-up converter, as shown in Figure 1.13, is a very well-known topology that steps up the input voltage by using a medium-to-high frequency step-up transformer [17]. By operating the dc-dc converters with a medium frequency transformer (MFT) in the range of a few kilo-Hz, the overall size of the system is reduced. However, designing a medium frequency transformer at high power levels with high turns-ratio has some inherent limitations in terms of isolation and coupling effect. The high insulation layer requirement between the LV and HV windings of a medium-to-high frequency step-up transformer reduces magnetizing inductance and increases leakage inductance, compared to a conventional low frequency transformer (LFT). This leakage energy is considered the main drawback of utilizing high frequency transformers [56]. Furthermore, the winding parasitic capacitance cannot be ignored due to the large number of turns in the secondary winding. In high voltage modular applications, the output voltage sharing is sensitive to the parasitic parameters of the step-up HFT. Moreover, in step-up applications, where the voltage amplitudes of the primary side and secondary side do not match, the circulating current becomes much higher and the efficiency reduces significantly [57]. Figure 1.14 shows some practically developed high power MFTs.

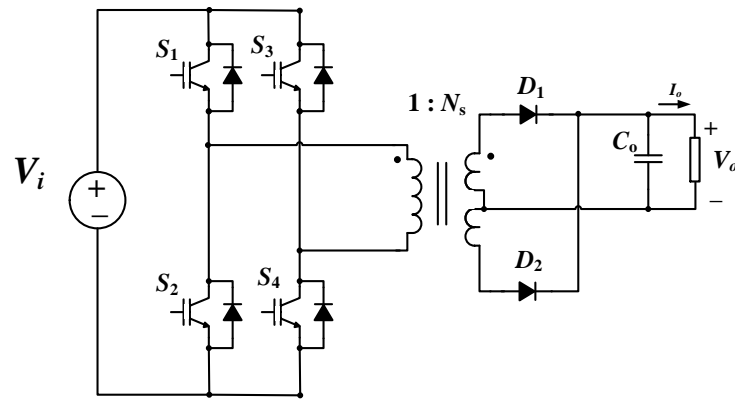
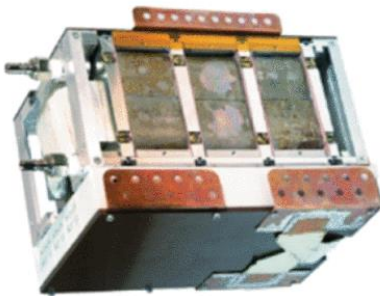


Figure 1.13– Active bridge converter



(a)



(b)



(c)

Figure 1.14– High power medium frequency transformers

(a) 450 kW, 3.6/3.6-kV, 5.6 kHz by UEN; (b) 166 kW, 1/0.4-kV, 20 kHz by ETHZ [58]; (c) 240 kW, 0.6/0.9-kV, 10 kHz by ABB.

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#### 1.4.1.4 Multi Stage/Level Converters

One well-known method for increasing the voltage gain of a dc-dc converter is to employ several stages of converter modules connected in various ways. This can be realized by implementing several identical or different converter modules combined with various voltage boosting techniques. This method is thoroughly investigated in [40].

Cascading connection of converters is a simple approach for increasing the voltage gain. The multiple-module cascaded boost configuration is shown in Figure 1.15. In this approach, the rectified wind turbine output voltage is connected to the cascaded boost converters to step up the voltage. The voltage stress on the first stage is relatively low, and it can be operated at high frequencies. However, the voltage stress of the switch and diode in the second boost converter are equal to the output voltage. The average diode current also equals to the load output current [17]. The multiple module approaches take advantage of modularity, due to the ease of interleaving techniques. For example, a multiple module series hybrid converter is shown in Figure 1.16. The device count in this converter is less than that of the active bridge converter. The reduced active component count is associated with merits, such as simplifying the driver circuits, and fewer snubbers and balancing network components. However, due to the lower voltage gain of this converter, an ac transformer should be added before the rectifying stage. Diode reverse recovery losses are also a drawback in these approaches due to the inherent effect of continuous conduction mode (CCM) operation of the boost converter [17].

Multilevel dc-dc converters are gaining attention in both industry and academia for their capability in high-power high-voltage applications. A schematic of single input multilevel

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structure with several sub-modules is shown in Figure 1.17. There are various types of multilevel converters, such as diode-clamped and flying capacitor converters that can be used in step-up dc-dc converters. A five-level multilevel modular diode clamped converter is shown in Figure 1.18 (a). However, diode-clamped converters require a large number of diodes that suffer the unbalancing issue [39]. A five-level multilevel modular capacitor clamped (flying capacitor) converter is also shown in Figure 1.18 (b). This converter uses many capacitors connected in series. The total series capacitance is much smaller than that of a single one. Therefore, the total volume of capacitors required is quite high [59]. Generalized multilevel converters can be also used for step-up dc-dc conversions [60]; but the weight and volume of the entire system increase dramatically as the step-up ratio becomes high. In general, the main advantages of multilevel converters are simplicity, modularity, and flexibility [40]. However, multilevel converters usually require a complicated balancing control scheme to maintain the voltage levels; and because of the high component count, the efficiency deteriorates as the number of stages/levels increases.

Table 1.4 provides a comparative summary of various voltage-boosting techniques in terms of their major characteristics: power level, cost, reliability, efficiency, power density, weight, integration, and complexity [40].

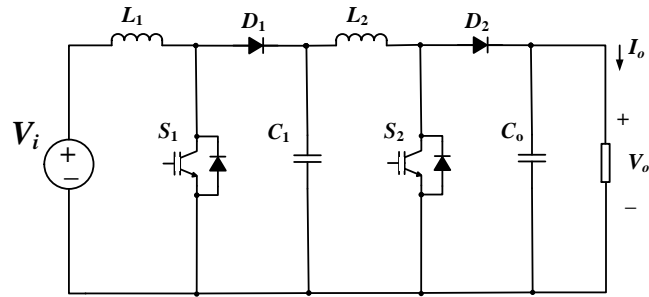


Figure 1.15– Multiple-module cascaded boost configuration

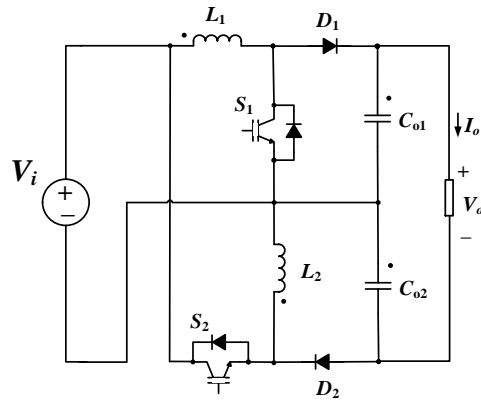


Figure 1.16– Multiple-module hybrid converter

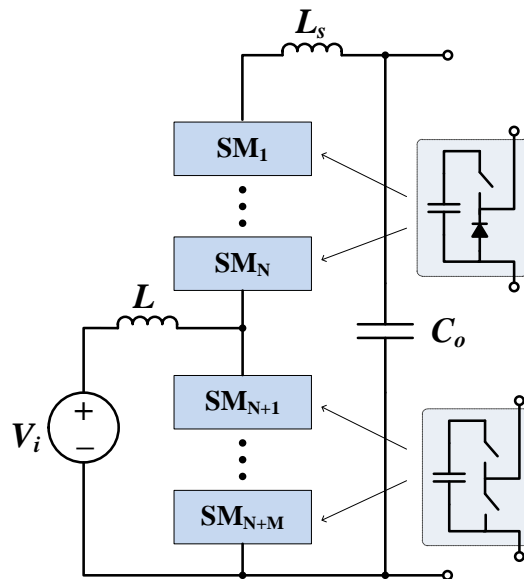


Figure 1.17– General structure of dc-dc multilevel modular converter (MMC)

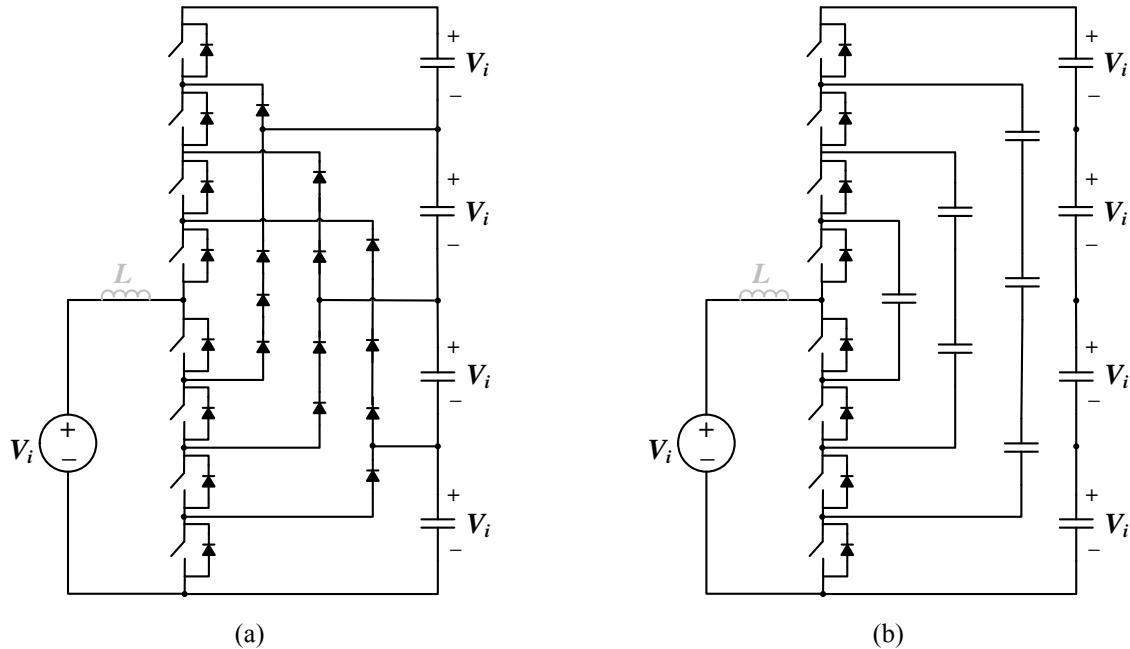


Figure 1.18– (a) five-level multilevel modular diode clamped converter ; (b) five-level multilevel modular capacitor clamped (flying capacitor) converter

Table 1.4– Summary of Boosting Techniques in MVdc Step-Up Converters

Voltage boosting techniques	Advantageous	Disadvantageous
Switched capacitor based converters	<ul style="list-style-type: none"> <li>✓ Low cost and lightweight circuits.</li> <li>✓ Small size and high power density.</li> <li>✓ Easy to be integrated.</li> <li>✓ Fast dynamic response.</li> </ul>	<ul style="list-style-type: none"> <li>✗ Inrush current at start-up.</li> <li>✗ Sensitive to ESR of capacitors.</li> <li>✗ Lack of output voltage regulation.</li> <li>✗ Only discrete output voltage.</li> </ul>
Resonant converters	<ul style="list-style-type: none"> <li>✓ Achieve soft-switching.</li> <li>✓ Medium-to-high frequency operation</li> <li>✓ Small size and light weight</li> <li>✓ High efficiency.</li> </ul>	<ul style="list-style-type: none"> <li>✗ Having a very high quality factor when very high voltage gain is required.</li> <li>✗ Current and voltage stress of the resonant components at high gain.</li> </ul>
High-frequency step-up transformers	<ul style="list-style-type: none"> <li>✓ Versatile in boost ability due to the tunable turns-ratio of transformer.</li> <li>✓ Switches can be place in low voltage side, helping to reduce conduction loss.</li> </ul>	<ul style="list-style-type: none"> <li>✗ Isolation and coupling effect problems.</li> <li>✗ Negative effect of parasitic components, such as large voltage spike due to the leakage inductance.</li> <li>✗ Complex design.</li> <li>✗ Relatively bulky.</li> </ul>
Multi stage/level converters	<ul style="list-style-type: none"> <li>✓ Modular structure.</li> <li>✓ High power capability.</li> <li>✓ Reliability.</li> </ul>	<ul style="list-style-type: none"> <li>✗ Large amount of components.</li> <li>✗ Relatively heavy, bulky and costly.</li> <li>✗ Efficiency deteriorates with number of stages</li> </ul>

### 1.4.2 Generator-Side AC-DC Converter

In type IV wind turbine, active power flows unidirectionally from the permanent magnet synchronous generators (PMSG/WRSG) to the grid. So, for the front-end rectifying stage both active rectifier and passive rectifier can be utilized [61]–[63]. A three-phase ac-dc active rectifier is shown in Figure 1.19. While active rectifiers provide power factor correction (PFC) in the input, diode-bridge rectifiers offer low cost, less footprint, light weight, simple configuration with more reliability. However, with the lack of control system in passive rectifiers, MPPT operation or regulation of the dc-link voltage cannot be performed. To address this issue, a boost converter can be employed as an intermediate dc-dc stage. This configuration is shown in Figure 1.20. The boost converter can (1) step up the unregulated dc-link voltage; (2) perform maximum power point tracking and as a result enables a variable speed operation for the PMSG/WRSG; and (3) implement power factor correction.

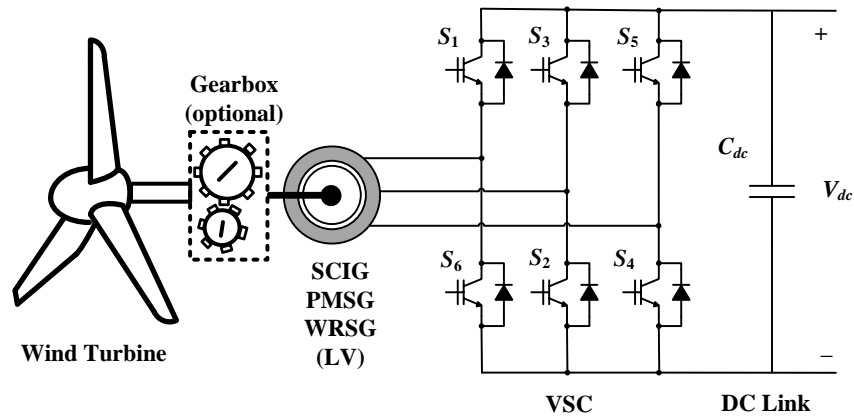


Figure 1.19– Three-phase ac-dc active rectifier

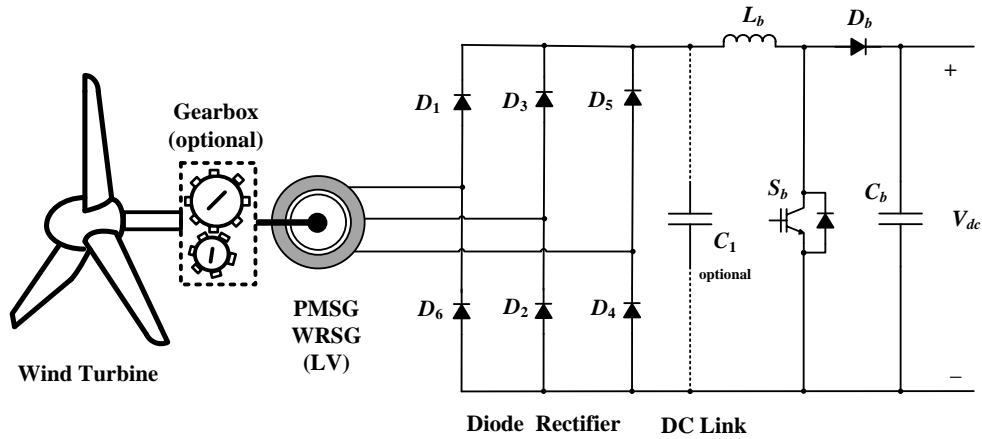


Figure 1.20– Three-phase ac-dc diode rectifier + boost converter

Another solution to eliminate the heavy low frequency transformer is to use medium frequency transformers (MTFs) in a cascaded back-to-back H-bridges structure. This configuration is shown in Figure 1.21. By operating the dc-dc converters with medium frequency transformers in the range of a few kilo-Hz, the overall size of the system reduces. However, the converter requires isolated dc sources, which are generated by an open winding generator. The generator design is complex as it contains multiple sets of two-phase windings. Moreover, as discussed in section 1.4.1.3, medium frequency transformers with high turns-ratio for high power applications in wind energy systems have some inherent limitations in terms of isolation and coupling effect.

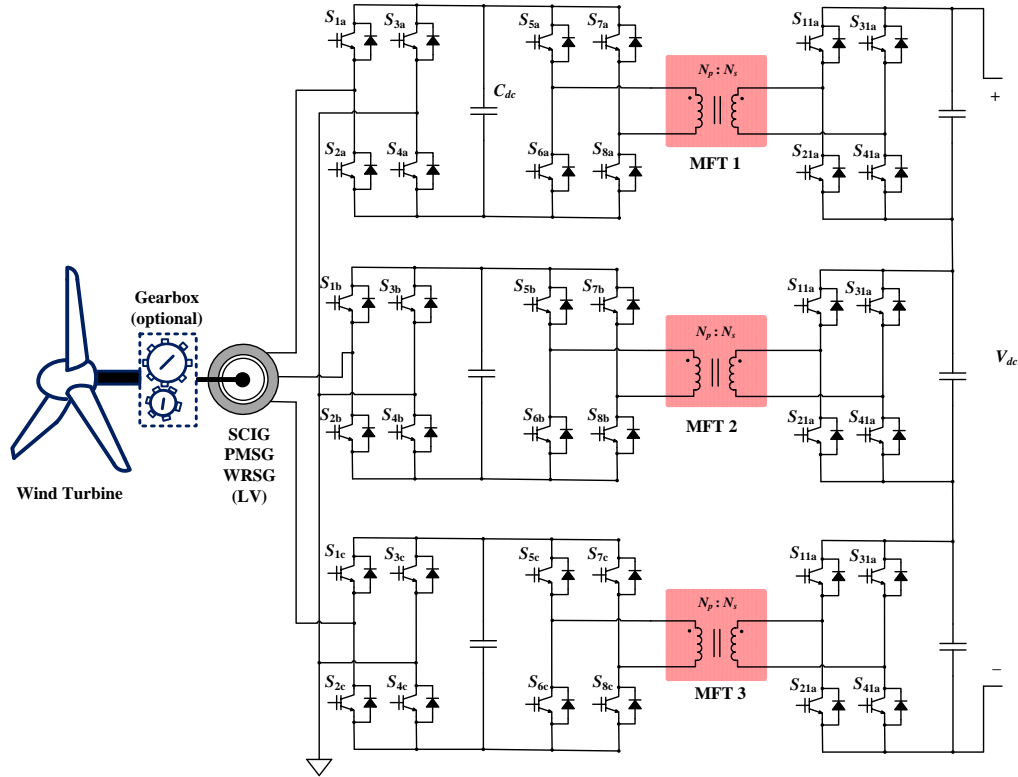


Figure 1.21– Cascaded H-bridge back-to-back converter for wind turbines with medium frequency transformer

## 1.5 Research Objectives

In summary, different types of power converter topologies capable of stepping up the voltage for MVdc application have been reported. However, existing MV step-up converter systems suffer from one or more of the following challenges:

- The need for a high-frequency step-up transformer (with high turns-ratio)
- Restricted soft-switching condition or hard-switching
- High voltage stress across the power switches
- Complicated balancing techniques in the modular converter structure

- Low-to-medium frequency operation
- Multiple power conversion stages

The proposed research is aimed at developing a novel class of highly efficient step-up transformerless MV power converters to address all the aforementioned challenges. In particular, the objectives of this thesis are:

1. To develop a new class of high frequency soft-switched dc-dc step-up converters that utilize step-up resonant circuit modules with high-gain, high-frequency output rectifiers.
2. To develop a new integration technique that combines the normal front-end ac-dc converter stage with the newly devised dc-dc step-up converter to form different types of single-stage three-phase ac-dc step-up converters for MVdc power conversion systems.
3. To integrate various magnetic components and further reduce the size and cost of the overall power converter system.
4. To achieve soft-switching and to reduce the voltage stress of semiconductor devices to be able to employ lower-rated WBG semiconductor devices in all the devised converter topologies with high frequency operation in the range of tens of kHz.

## **1.6 Dissertation Outline**

This dissertation can be classified into two main parts: Chapter 2 and Chapter 3 describe various types of the proposed step-up transformerless dc-dc converter topologies. Chapter 4 presents and discusses a new class of ac-dc step-up converter system with an integrated active power factor correction. In particular, the organization of this thesis is as follows:

In Chapter 1, a review of different types of MV power architectures for wind energy conversion systems was presented. In particular, the emerging MVdc grid structure that utilizes MV step-up dc-dc converter was discussed in detail. Different types of existing MV step-up converters, including their advantages and design challenges have been addressed. Then, different types of semiconductor devices, including the latest WBG switching devices, have been discussed in this chapter. Towards the end, the research motivations of this thesis, as well as its organization are highlighted in this chapter.

In Chapter 2, a new class of modular MV step-up dc-dc resonant converters that do not require any high-frequency step-up transformers is proposed. In each converter module, the proposed approach combines a step-up resonant circuit with at least one soft-switched high-frequency high-gain output rectifier module. When multiple high-gain output rectifier modules are used in each converter module, an integrated magnetic technique is presented to combine several magnetic components to reduce the overall size of the power conversion unit. The current-driven structure of the high-gain output rectifier guarantees smooth performance of the high frequency rectifying diodes. In addition, at the input inverter side of each converter module, a multistring configuration of the switches reduces the voltage stress across each switch to half of the input voltage. The feasibility of the proposed converters is then verified through simulation results and experimental works on proof-of-concept prototypes.

In Chapter 3, two different step-up transformerless dc-dc resonant converter modules that extend the works proposed in Chapter 2 are presented to further reduce the number of magnetic components. Each of the proposed converter modules utilizes only one isolating magnetic

component with coupled high-gain high-frequency rectifiers. In the first topology, two coupled high-gain rectifier modules are connected to the step-up resonant circuit via a three-winding high frequency transformer. As a result, the output voltage of each high-gain rectifier is balanced due to the presence of the coupled-inductor. In the second topology, a new step-up converter module that consists of three resonant sub-modules interconnecting with a unity turns-ratio multiphase transformer and coupled high-gain rectifier modules is presented. The presence of three resonant circuit sub-modules connecting via a multiphase transformer is able to fully utilize all the switch networks at the input inverter to transfer power. The feasibilities of both converter topologies are verified through simulation results and experimental works on proof-of-concept prototypes.

In Chapter 4, a new class of modular ac-dc step-up transformerless high voltage gain converters with integrated active power factor correction is presented. In the proposed approach, the three-phase boost rectifier is integrated with the step-up resonant converter modules presented in Chapter 2 and Chapter 3 to form various single-stage ac-dc step-up MV converters. Soft-switching operations are achieved in all the semiconductor devices to maintain high circuit efficiency.

To reduce the number of diodes required for the front-end rectifier, a new bridgeless ac-dc rectifier is also proposed and it is combined with the step-up dc-dc converter modules presented in previous chapters to form various modular bridgeless ac-dc three-phase step-up converters for MV step-up conversion. The performance of all developed three-phase ac-dc converter topologies is verified through simulation results and experimental works on proof-of-concept prototypes.

In Chapter 5, the contributions of this thesis are summarized. It also suggests some future works related to this thesis.

## **Chapter 2    Proposed DC-DC Converters with Modular Resonant Circuits and High- Gain Rectifiers**

To reduce the price and overall size of the power interface in renewable energy systems, the current research trend is to replace line-frequency, heavy, and large-size passive components with much lighter power electronic systems that utilize high frequency semiconductor devices.

The first part of this chapter focuses on the development of a step-up dc-dc converter with a unity turns-ratio (1:1) medium-to-high frequency transformer to address the drawbacks of high turns-ratio high frequency transformers, discussed in Chapter 1. The second part of this chapter focuses on the development of several high-frequency voltage-boosting techniques using a modular approach. In particular, the proposed converter configuration will use both modular step-up resonant circuits and high-frequency voltage-multiplier rectifier circuits to achieve step-up voltage conversion function. Finally, to improve the volume and number of magnetic components, the third part of this chapter focuses on the development of coupled magnetics in the proposed converter topologies.

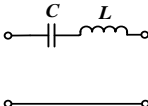
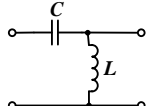
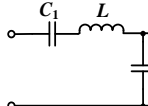
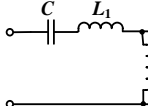
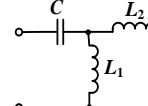
## 2.1 Resonant Converter Topology

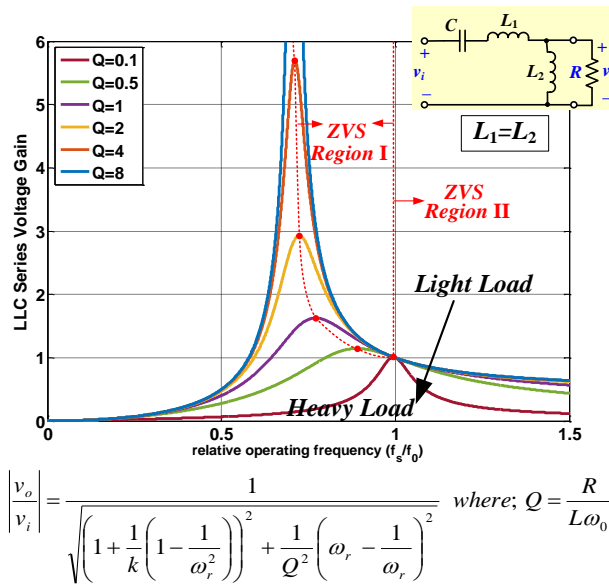
Many resonant networks have been proposed in literature, but only a few of them have made their way to the practical implementation. To overcome the shortcomings of *LC* series, parallel and series-parallel topologies discussed in section 1.4.1.2, this section investigates the most practical and well-known three-element resonant converters which are *LLC* and *CLL* resonant circuits. *LLC* and *CLL* resonant circuits, shown in Figure 2.1(a) and (b), are the most promising candidates in front-end dc-dc applications with comparatively similar behavior and shortcomings. Unlike *LCC* resonant circuit, *LLC* and *CLL* resonant converters can build a current-driven rectifier network with ZCS capability. While *LLC* offers lower circulating energy and component stress, *CLL* circuit reduces the size and volume of the converter with placing the series inductor ( $L_2$ ) on the secondary side of the transformer. Figure 2.1 shows that higher voltage gain can be achieved for a *CLL* resonant circuit under the similar condition that  $L_1=L_2$ . On the other hand, *LLC* circuits can incorporate both leakage and magnetizing inductances of the HF transformer into the resonant network [53]. Table 2.1 highlights the key features of the most well-known resonant converters [53].

To achieve high voltage gain without using a high turns-ratio transformer, modular resonant circuits are utilized in the proposed converter. Although resonant circuits are able to provide high voltage gain, they suffer the drawback of having a very high quality factor when very high voltage gain is required. It is known that having a high value of quality factor in the resonant circuit subsequently increases the current and voltage stress of the resonant circuit components.

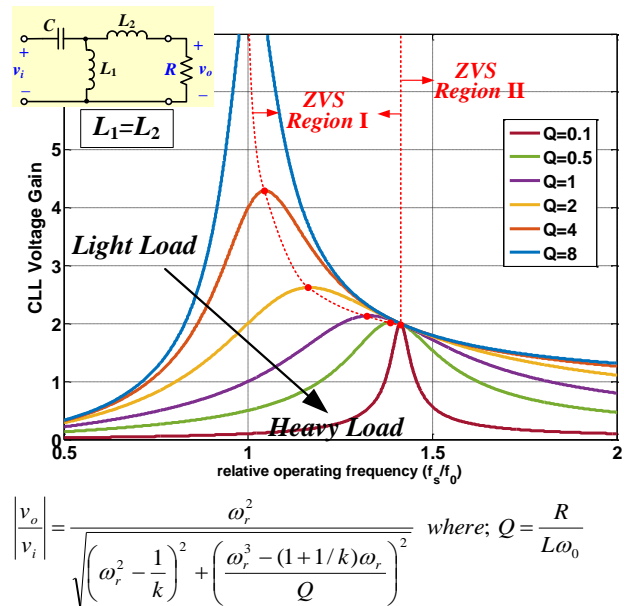
Hence, relying solely on resonant circuits to achieve very high voltage gain in step-up power converters is not a long-term solution.

Table 2.1– Comparison of Different Resonant Topologies

	<i>LC Series</i>	<i>LC Parallel</i>	<i>LCC</i>	<i>LLC</i>	<i>CLL</i>
					
Frequency Variation	Wide	Wide	Narrow	Moderate	Moderate
Voltage/Current Stress	Lowest	High	Highest	Low	High
ZVS (on switch network)	✓	✓	✓	✓	✓
ZCS (on rectifier network)	✗	✗	✗	✓	✓



a) *LLC* resonant converter voltage gain



a) *CLL* resonant converter voltage gain

Figure 2.1– Voltage gain characteristics of most practical resonant circuits

## 2.2 DC-DC Converters with Modular Resonant Circuits

The general block diagram of the proposed modular MV dc-dc converter configuration is shown in Figure 2.2. The proposed converter consists of a high frequency inverter with the power switches arranged in multiple strings configuration to reduce the voltage stress across the switches; and multiple resonant circuits with high frequency rectifying stages to step up the voltage, as shown in Figure 2.3. Different topologies can be derived from the proposed structure. Figure 2.4 shows two different topologies that can be employed using the proposed structure: (a) *CL* resonant converters with voltage-fed full-bridge rectifiers, (b) *LLC* resonant converters with current-fed full-bridge rectifiers. In this section, *CL* resonant converter with voltage-fed bridge rectifier will be discussed.

The proposed converter has the following features: 1) the multistring arrangement of the switches allows much lower voltage stress across each transistor; 2) the modular step-up resonant circuits are able to achieve high voltage gain so that transformer with high turns-ratio is not required; 3) zero voltage switching (ZVS) turn-ON and zero current switching turn-OFF are achieved in all the switches; 4) the output MVdc level is controlled by variable frequency control of the step-up converter; 5) unlike multilevel inverters, the output of the inverter in the proposed converter produces an asymmetrical square waveform that does not require voltage balancing control; and 6) circulating energy in all the resonant circuit modules is minimized through close-to-resonant operation for different load conditions.

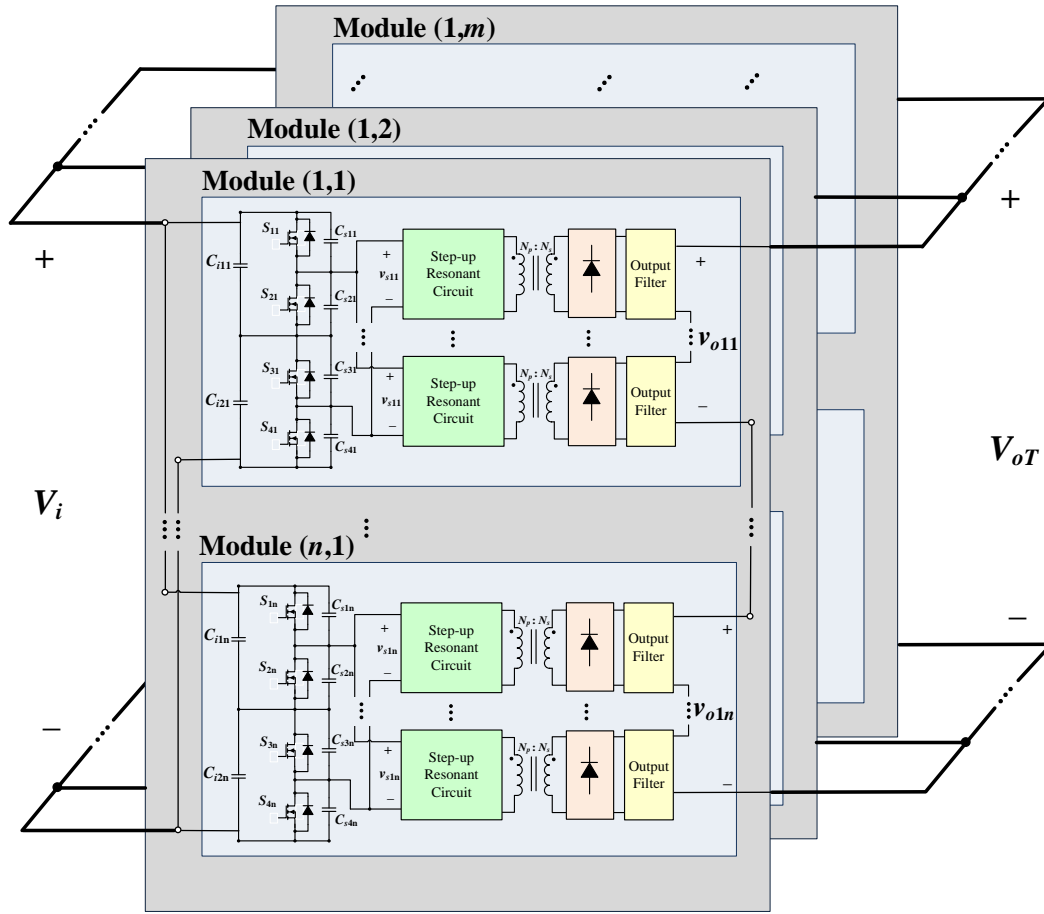


Figure 2.2– Proposed modular MV step-up dc-dc converter structure

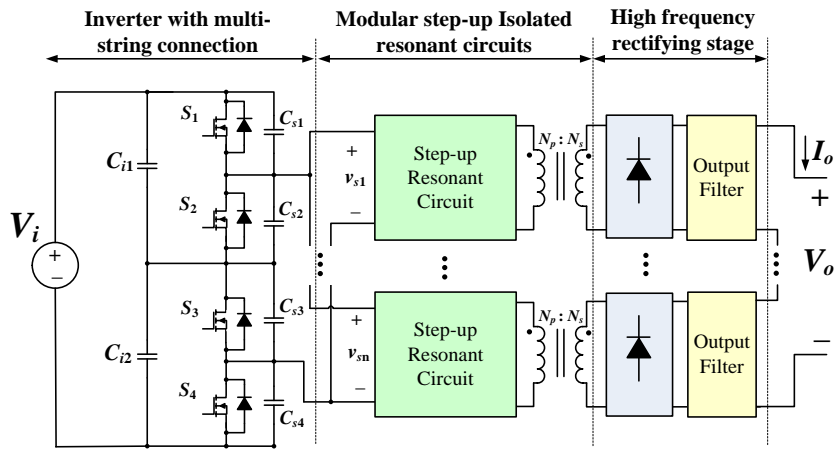


Figure 2.3– One module of proposed MV step-up dc-dc converter

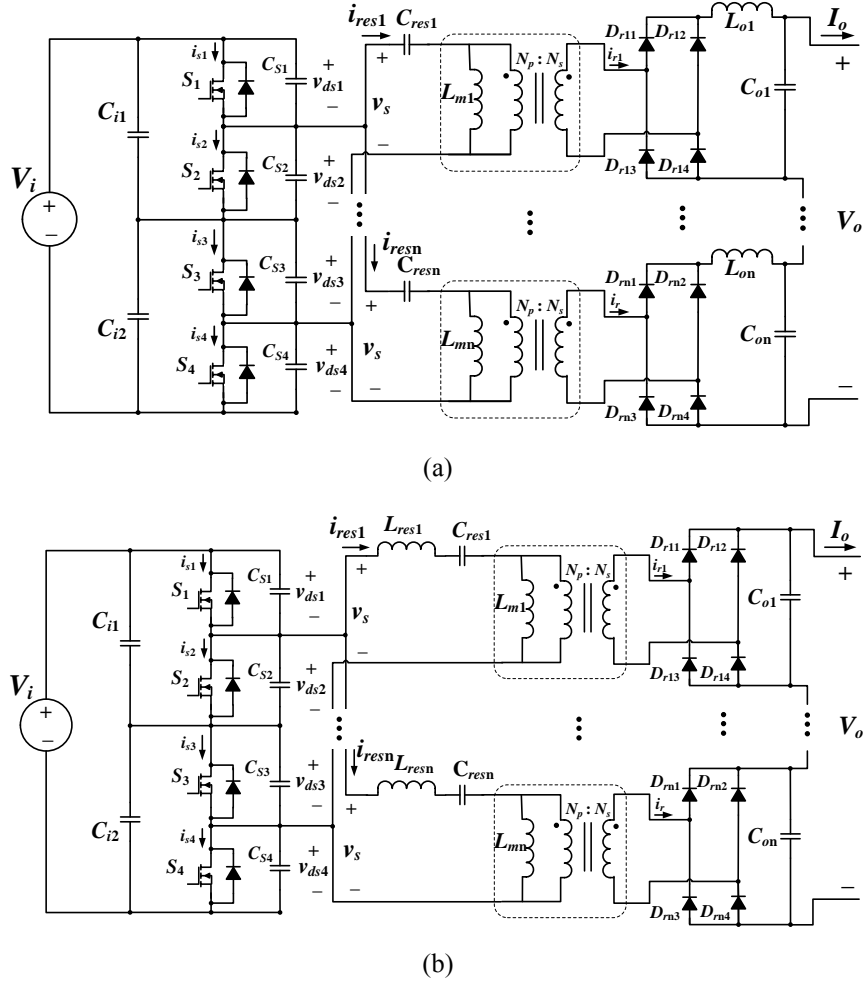


Figure 2.4– Modular step-up converters, relying on resonant circuits to step-up the voltage.

(a) *CL* resonant converter with voltage-fed bridge rectifier, (b) *LLC* resonant converter with current-fed bridge rectifier

### 2.2.1 Multistring Configuration of Semiconductor Devices

One of the objectives of this thesis is to reduce the stress of voltage across each semiconductor device to be able to employ lower-rated WBG devices for medium voltage applications. The proposed multistring connection of the semiconductor devices is illustrated in Figure 2.5. This circuit consists of four switches,  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  which are controlled by two compensating

gating signals. Switches ( $S_1, S_4$ ) and switches ( $S_2, S_3$ ) operate in complementary fashion. In state I switches ( $S_1, S_4$ ) turn ON during the interval  $dT_s$ , while in state II switches ( $S_2, S_3$ ) turn ON during the interval  $(1-d)T_s$ . This configuration can effectively reduce the voltage stress of the devices by half. The operating principles of the proposed inverter with multistring connection of semiconductor devices are shown in Figure 2.6.

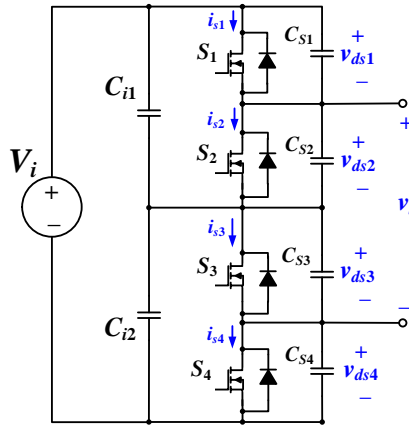


Figure 2.5– Proposed multistring connection of semiconductor devices

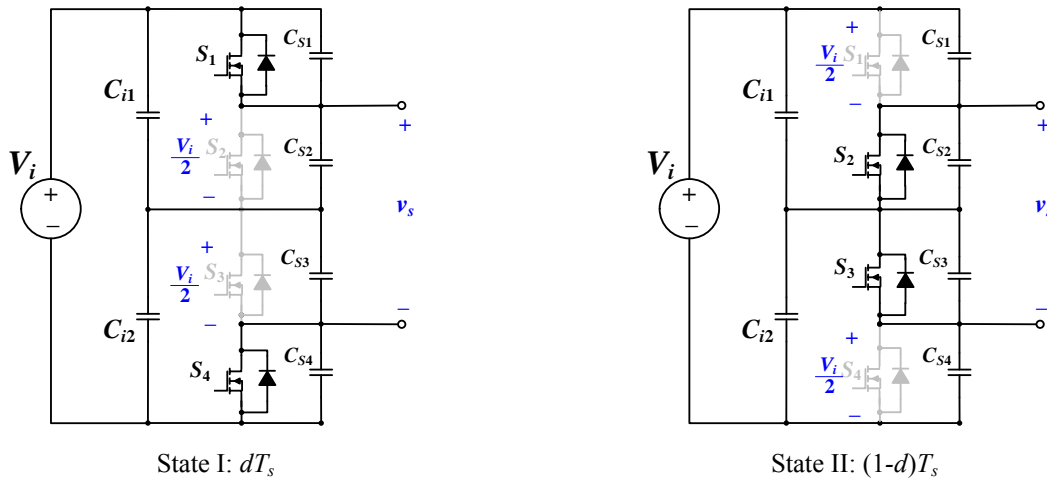


Figure 2.6– Operating states of the proposed multistring connection of semiconductor devices

### 2.2.2 Proposed Topology with *CL* Step-Up Resonant Circuits

The proposed converter structure is derived by employing multiple modules of resonant converters cascaded with high frequency rectifiers with an inductive output filter. In order to reduce the voltage stress across the primary side power transistors, as in the case in the conventional full-bridge or active bridge step-up converters, the proposed converter structure consists of utilizing “multiple string” of switches on the primary side of the converter. Figure 2.7 shows the proposed MV step-up converter structure, which consists of a leg of two switch pairs and two modules of step-up resonant circuits with their output rectifying stages. As discussed in previous section (2.2.1), voltage stress across each switch is equal to  $\frac{1}{2}$  of  $V_i$ .

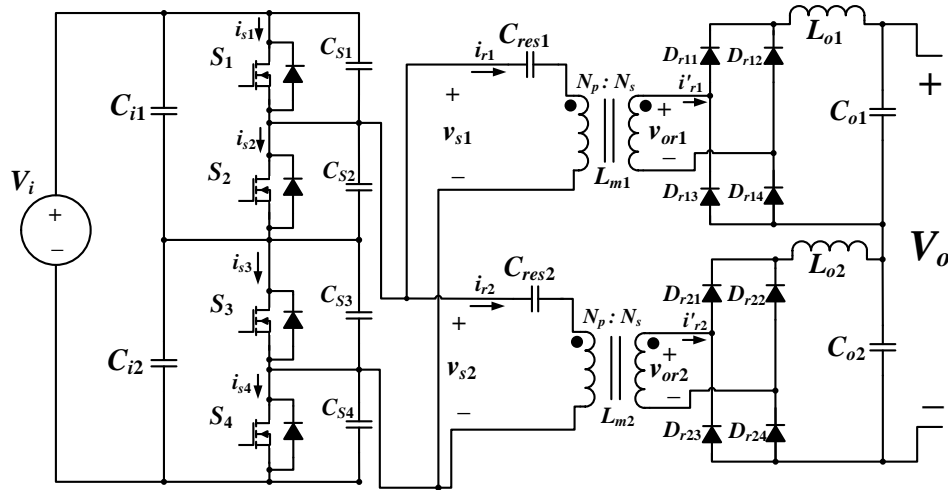


Figure 2.7– Proposed converter with two modules of resonant circuit

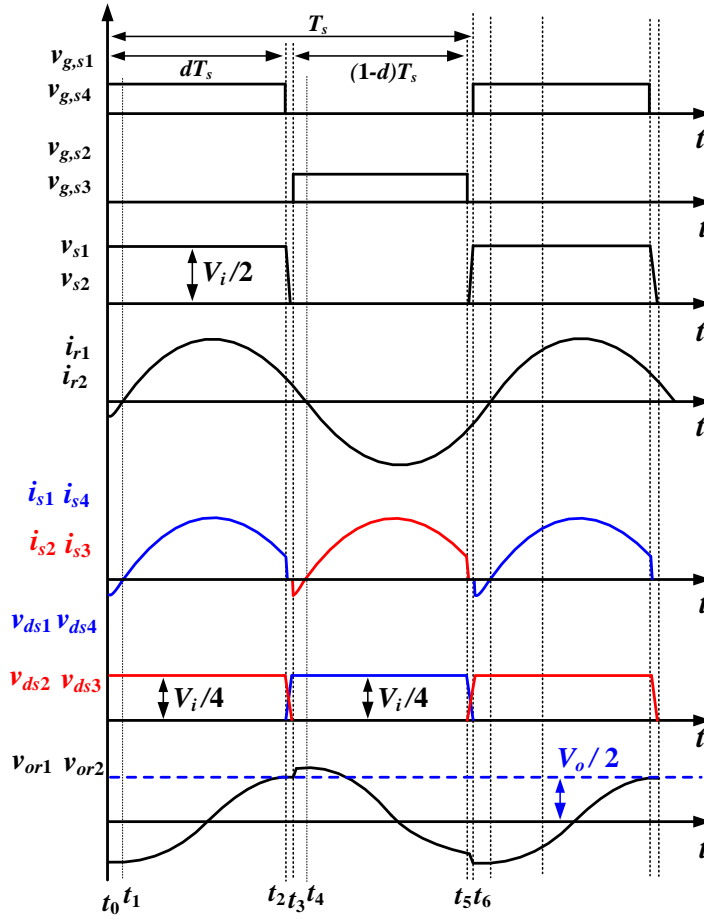


Figure 2.8– Key operating waveforms of the converter

### 2.2.3 Converter Operating Principles

The operating principles of the proposed converter can be analyzed according to the operating waveforms shown in Figure 2.8. The equivalent circuit at each stage within a switching period is also shown in Figure 2.9. As mentioned earlier,  $(S_1, S_4)$  turn ON during the interval  $dT_s$ , whereas  $(S_2, S_3)$  turn ON during the interval  $(1-d)T_s$ . In the following analysis, the switches and diodes are assumed to be ideal components.

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**$[t_0 < t < t_1]$ :** The gate signals are applied to  $S_1$  and  $S_4$ . Due to the negative resonant current in both resonant circuits, the antiparallel diodes of  $S_1$  and  $S_4$  are forced to turn ON. Meanwhile, the voltage across  $S_2$  and  $S_3$  are clamped to capacitor ( $C_{i1}$  and  $C_{i2}$ ) voltage, which is equal to  $V_i/2$ .

**$[t_1 < t < t_2]$ :** The gate signals are still applied to  $S_1$  and  $S_4$ ; the negative resonant currents in the previous stage now become positive, making  $S_1$  and  $S_4$  to be turned ON under ZVS condition.

**$[t_2 < t < t_3]$ :** The gate signals that were applied to  $S_1$  and  $S_4$  are now removed. Due to the snubber capacitors ( $C_{s1}$  and  $C_{s4}$ ), the voltages across  $S_1$  and  $S_4$  rise slowly from zero. Hence, voltage slowly increases from zero after the gate signals are removed from  $S_1$  and  $S_4$ . As a result,  $S_1$  and  $S_4$  are turned OFF with ZCS.

**$[t_3 < t < t_4]$ :** The gate signals that were applied to  $S_1$  and  $S_4$  are removed prior to this stage and are now applied to  $S_2$  and  $S_3$ . Since the resonant current in both resonant circuits are positive, the antiparallel diodes of  $S_2$  and  $S_3$  are forced to turn ON. At the same time, the output voltages of the resonant circuits reverse their polarities.

**$[t_4 < t < t_5]$ :** At  $t_4$ , the positive resonant currents in the previous stage become negative, so  $S_2$  and  $S_3$  are turned ON under ZVS at  $t_4$ .

**$[t_5 < t < t_6]$ :** The gate signals that were applied to  $S_2$  and  $S_3$  are now removed. Due to the snubber capacitors ( $C_{s2}$  and  $C_{s3}$ ), the voltage across  $S_2$  and  $S_3$  rises slowly from zero and ZCS is achieved. This stage ends when the gate signals are applied to  $S_1$  and  $S_4$  again.

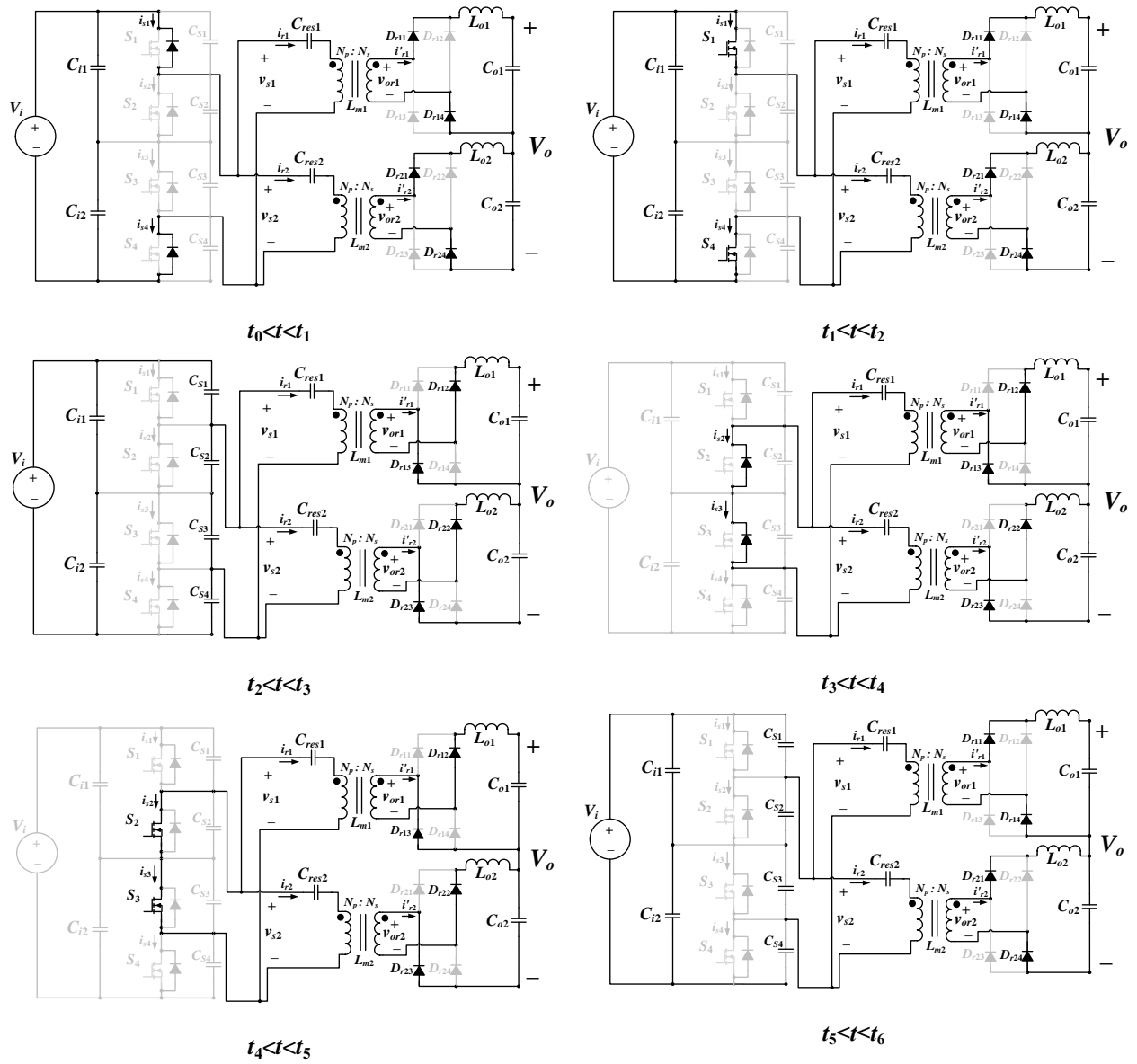


Figure 2.9—Equivalent circuit in each operating stage within a switching period

### 2.2.4 Analysis of Each Converter Module with *CL* Resonant Circuit

This section will provide an in-depth analysis of the proposed step-up dc-dc converter. To simplify the analysis of the proposed circuit characteristics, only one module with single resonant circuit and rectifier is considered, as shown in Figure 2.10. The input voltage to the resonant circuit of module  $k$  is described by (2.1), where  $d$  represents the duty cycle;  $\theta_n$  is the phase angle that is given by (2.2); and  $n$  represents the  $n$ th harmonic. Since the harmonics content in the resonant circuits can be assumed to be negligible, fundamental approximation is then used in the following calculations.

$$v_{sk}|_{k=1,2} = V_i d + \sum_{n=1}^{\infty} \left( \frac{\sqrt{2}V_i}{n\pi} \sqrt{1 - \cos(2n\pi d)} \sin(2\pi n f_s t + \theta_n) \right) \quad (2.1)$$

$$\theta_n = \tan^{-1} \left( \frac{\sin(2\pi n d)}{1 - \cos(2\pi n d)} \right) \quad (2.2)$$

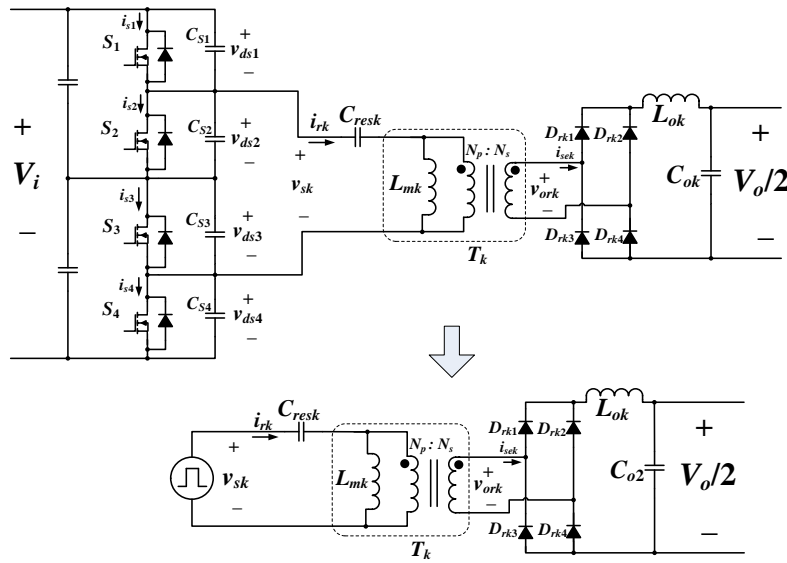


Figure 2.10– Equivalent circuit of one of the modules in the proposed converter

### 2.2.4.1 Resonant Current Analysis ( $i_{rk}$ )

The resonant current ( $i_{rk}$ ) in each module is derived from the ac components in (2.1). Hence,  $i_{rk}$  is given by (2.3), where  $|Z_{ik}|$  is the magnitude of the input impedance of the resonant circuit;  $\phi_{Zi}$  is the phase angle of the input impedance.

$$i_{rk}|_{k=1,2} = \sum_{n=1}^{\infty} \left( \frac{\sqrt{2}V_i}{n\pi|Z_{ik}|} \sqrt{1 - \cos(2n\pi d)} \sin(2\pi n f_s t + \theta_n - \phi_{Zi}) \right) \quad (2.3)$$

$$|Z_{ik}|_{k=1,2} = R_{eqk} \sqrt{\frac{(1 - \omega_r^2)^2 + \left(\frac{\omega_r}{Q_k}\right)^2}{\omega_r^2(\omega_r^2 + Q_k^2)}} \quad (2.4)$$

$$\phi_{Zi} = \tan^{-1}\left(\frac{\omega_r}{Q_k(1 - \omega_r^2)}\right) - \tan^{-1}\left(\frac{Q_k}{\omega_r}\right) \quad (2.5)$$

where  $Q_k$  represents the quality factor of the resonant circuit which is given by (2.6);  $R_{eqk}$  represents the equivalent load resistance at the output of resonant circuit module  $k$ ; and  $\omega_{0k}$  is the angular corner frequency of module  $k$  given by (2.7). The relative angular operating frequency ( $\omega_{rk}$ ) is given by (2.8), where  $\omega_s$  represents the angular operating frequency. The angular resonant frequency ( $\omega_{resk}$ ) of the  $CL$  resonant circuit can be determined by setting  $\phi_{Zi}$  equal to zero, which results in the relationship shown in (2.9). It can be observed from (2.9) that when  $Q_k$  is high,  $\omega_{resk} = \omega_{0k}$ . In other words, the resonant frequency is equal to the corner frequency. Hence, the corner frequency equation will be used in the design example.

$$Q_k = \frac{R_{eqk}}{\omega_0 L_{mk}} \quad (2.6)$$

$$\omega_{0k}|_{k=1,2,3 \text{ or } 4} = \frac{1}{\sqrt{L_{mk} C_{resk}}} \quad (2.7)$$

$$\omega_{rk}|_{k=1,2} = \frac{\omega_s}{\omega_{0k}} \quad (2.8)$$

$$\omega_{resk}|_{k=1,2} = \omega_{0k} \sqrt{1 - \frac{1}{Q_k}} \quad (2.9)$$

From (2.3), the peak value of the fundamental resonant current and the rms resonant current can be obtained as given by (2.10) and (2.11), respectively.

$$I_{rk\_max} = \frac{\sqrt{2}V_i}{\pi} \frac{\sqrt{1 - \cos(2\pi d)}}{|Z_{ik}|} \quad (2.10)$$

$$I_{rk} = \frac{V_i}{\pi} \left[ \sum_{n=1}^{\infty} \left( \frac{1 - \cos(2\pi nd)}{(n|Z_{ik}|)^2} \right) \right]^{1/2} \quad (2.11)$$

To explain the characteristics of the resonant current, only the fundamental component is considered. Considering the input voltage  $V_i$  and the equivalent ac resistance  $R_{eqk}$  as the base values, a plot of normalized rms resonant current as a function of  $\omega_r$  for various  $Q_k$  with  $d=0.5$  is shown in Figure 2.11.

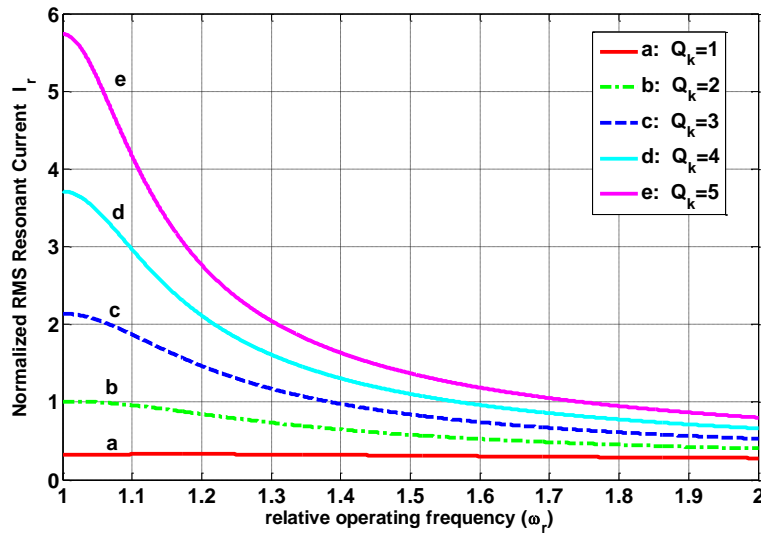


Figure 2.11– Per unit rms value of the fundamental resonant current at  $d_k=0.5$

### 2.2.4.2 Voltage Gain

The voltage gain of each *CL* resonant circuit between  $v_{sk}$  and  $v_{ork}$  is given by (2.12) as a function of  $\omega_r$  and  $Q_k$ .

$$\left| \frac{v_{ork}}{v_{sk}} \right|_{k=1,2} = \frac{1}{\sqrt{\left(1 - \frac{1}{\omega_r^2}\right)^2 + \left(\frac{1}{\omega_r Q_k}\right)^2}} \quad (2.12)$$

The series capacitor in each resonant circuit module ( $C_{resk}$ ) blocks the dc component of voltage  $v_{sk}$ , and hence, the rms value of resonant voltage  $v_{sk\ ac}$  is given by (2.13).

$$v_{sk\ ac} = \frac{V_i}{\pi} \left[ \sum \frac{1 - \cos(2n\pi d)}{n^2} \right]^{1/2} \quad (2.13)$$

From (2.13), it can be observed that the maximum rms voltage occurs at  $d=0.5$ , (2.14) shows the maximum voltage gain of  $v_{skac}/V_i$ .

$$\frac{v_{sk\ ac}}{V_i} = \frac{\sqrt{2}}{\pi} \left[ \sum_{n=odd} \frac{1}{n^2} \right]^{1/2} = \frac{1}{2} \quad (2.14)$$

The voltage gain of the current-source rectifier, considering the series connection of the rectifiers, is given by (2.15). By multiplying the aforementioned voltage gains, the total gain of the proposed converter with  $d=0.5$  is given by (2.17), where  $m$  is the transformer turns-ratio ( $m = N_s/N_p$ ). A plot of (2.17) is shown in Figure 2.12. It shows that high voltage gain can be achieved between  $V_o$  and  $V_i$  by designing a relatively high  $Q_k$  value in the resonant circuit. The phase angle ( $\phi_{Zi}$ ) equation given in (2.5) is plotted in Figure 2.13, where the operating region to achieve high voltage gain and to maintain ZVS turn-ON for all the switches is highlighted in red.

$$\frac{V_o}{V_{or1}} = 2 \times \frac{2\sqrt{2}}{\pi} \quad (2.15)$$

$$\frac{V_o}{V_i} = \frac{V_o}{V_{or1}} \times \frac{V_{or1}}{V_{s1}} \times \frac{V_{s1}}{V_i} \quad (2.16)$$

$$\left| \frac{V_o}{V_i} \right| = \frac{2m\sqrt{2}}{\pi} \frac{1}{\sqrt{\left(1 - \frac{1}{\omega_r^2}\right)^2 + \left(\frac{1}{\omega_r Q_k}\right)^2}} \quad (2.17)$$

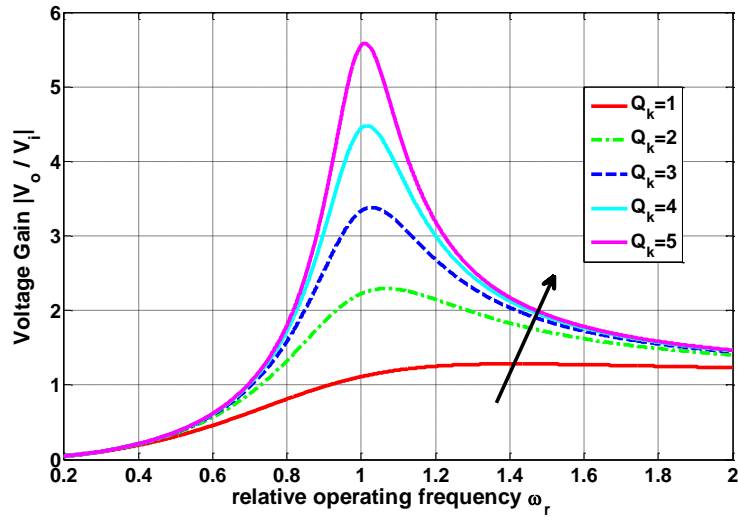


Figure 2.12– Voltage gain plot of the proposed step-up converter

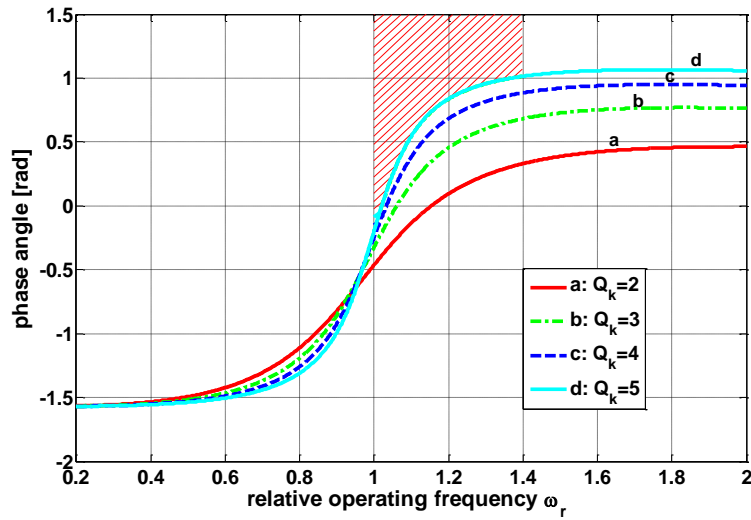


Figure 2.13– Phase plot of the *CL* resonant circuit

### 2.2.4.3 RMS Switch Current

The rms current in the switches is illustrated by (2.18) and (2.19), where  $\phi_{zi}$  is given by (2.5). Since the harmonics components are negligible in the switching losses, only the fundamental component is considered for the calculation of the rms switch current. With  $d=0.5$ , (2.18) and (2.19) are equal and are plotted in Figure 2.14 as a function of  $\omega_r$ .

$$I_{sw1} = I_{sw4} = \sqrt{\frac{1}{T_s} \int_0^{dT_s} [i_{r1}]^2 dt} = \frac{V_i}{\pi |Z_i|} \sqrt{(1 - \cos(2\pi d)) \left( d + \frac{\sin(2\pi d) \cos(2\phi_{zi})}{2\pi} \right)} \quad (2.18)$$

$$I_{sw2} = I_{sw3} = \sqrt{\frac{1}{T_s} \int_{dT_s}^{T_s} [i_{resk}]^2 dt} = \frac{V_i}{\pi |Z_i|} \sqrt{(1 - \cos(2\pi d)) \left( 1 - d_k - \frac{\sin(2\pi d) \cos(2\phi_{zi})}{2\pi} \right)} \quad (2.19)$$

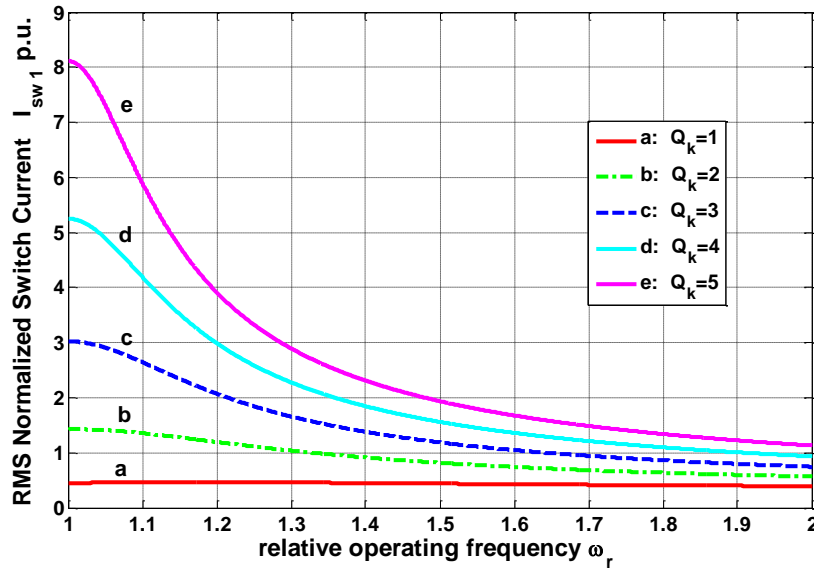


Figure 2.14– Per unit rms value of the fundamental switching current at  $d=0.5$

#### 2.2.4.4 Turn-OFF Currents of $S_1$ and $S_4$

To turn ON  $S_2$  and  $S_3$  under ZVS, as shown in Figure 2.8, the resonant current should force the antiparallel diodes to conduct prior to the turn-ON instants of the switches. Hence,  $I_1$  and  $I_4$  must be positive. The turn-OFF currents of  $S_1$  and  $S_4$  can be found by evaluating the resonant current at  $t = dT_s$  and can be determined from

$$I_1 = I_4 = \sum_{n=1}^{\infty} \left( \frac{\sqrt{2}V_i}{n\pi|Z_i|} \sqrt{1 - \cos(2n\pi d)} \sin(2\pi n d + \theta_n - \phi_{Zi}) \right) \quad (2.20)$$

#### 2.2.4.5 Turn-OFF Currents of $S_2$ and $S_3$

Similarly, the turn-OFF currents of switches  $S_2$  and  $S_3$  are obtained as shown in (2.21). To attain ZVS for  $S_1$  and  $S_4$ , as shown in Figure 2.8,  $I_2$  should be positive. This allows current to flow through the inverse parasitic diode of the switch. Since the converter operates above resonance and the quality factor  $Q_k$  is of relatively high value,  $S_1$  and  $S_4$  will always experience ZVS turn-ON for different loading conditions. Figure 2.15 shows the per unit turn-OFF current of all the switches as a function of relative operating frequency at  $d=0.5$ . From the figure, it is evident that by operating the converter above resonance and choosing a relatively high quality factor  $Q_k$ , the switches are able to experience ZVS.

$$I_2 = I_3 = \sum_{n=1}^{\infty} \left( \frac{-\sqrt{2}V_i}{n\pi|Z_i|} \sqrt{1 - \cos(2n\pi d)} \sin(\theta_n - \phi_{Zi}) \right) \quad (2.21)$$

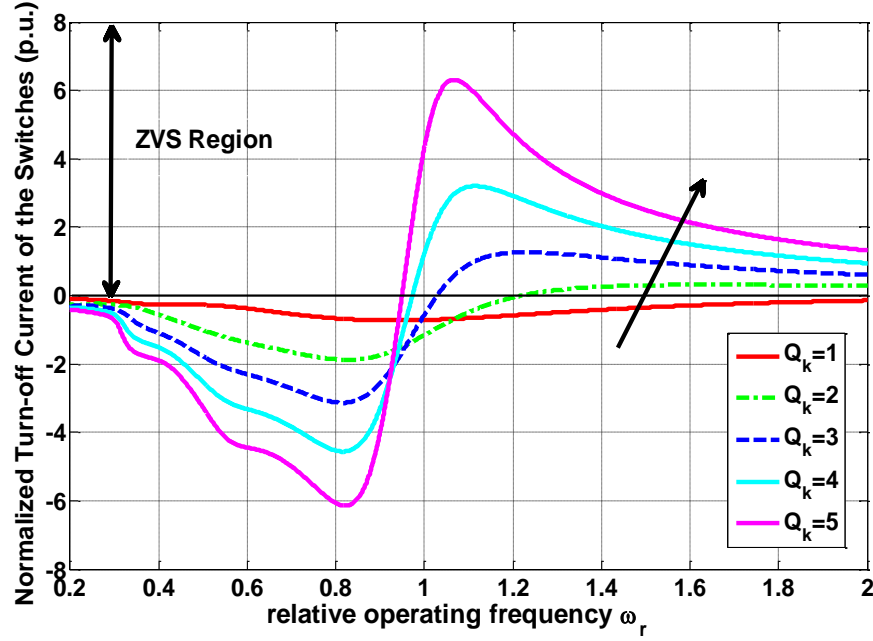


Figure 2.15— Normalized turn-OFF current of all the switches at  $d_k=0.5$

#### 2.2.4.6 Output Filter Inductors $L_{o1}$ and $L_{o2}$

The high frequency rectifier at the output of each resonant circuit module consists of an  $LC$ -type output filter. The inductor of the output filter plays an important role in determining the current flowing through each of the high frequency rectifying diodes. Figure 2.16 shows the high frequency rectifier and its equivalent circuit, where the input voltage  $v_{or}$  is assumed to be a close-to-sinusoidal voltage source as given by (2.22) as fundamental approximation was used in this analysis. With a sufficiently large output capacitor ( $C_{ok}$ ), the output voltage ( $V_{ok}$ ) can be modeled as a constant voltage dc source. Figure 2.17 shows the operating waveforms of the high frequency rectifier, with the assumption that  $L_{ok}$  is not large enough to filter all the harmonics. The current ( $i_{Lok}$ ) is then given by (2.23). From Figure 2.17, it is evident that the average value

of  $i_{Lok}$ , which is given by output current  $I_o$  is given by (2.24). The high frequency diode currents, such as  $i_{Drk1}$  and  $i_{Drk2}$ , can be observed from Figure 2.17 that they are able to achieve ZCS turn-ON and OFF.

$$v_{ors} = \sqrt{2}v_{or,rms} \sin(\omega t) \quad (2.22)$$

$$i_{Lok}(\theta) = \frac{1}{\omega L_{ok}} \int_{\theta_1}^{\theta} [\sqrt{2}v_{or,rms} \sin(\omega t) - V_{ok}] d(\omega t) \quad (2.23)$$

$$I_o = \frac{\int_{\theta_1}^{\theta_3} \left( \frac{1}{\omega L_{ok}} \int_{\theta_1}^{\theta} [\sqrt{2}v_{or,rms} \sin(\omega t) - V_{ok}] d(\omega t) \right) d\theta}{\pi} \quad (2.24)$$

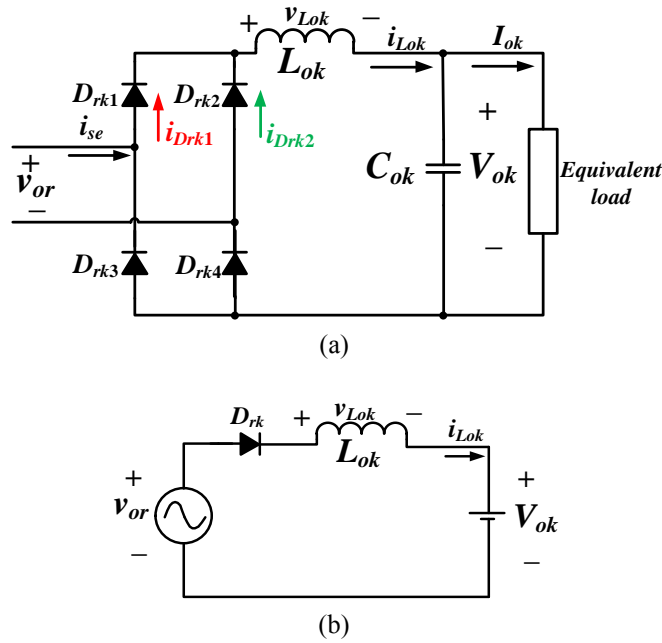


Figure 2.16– Equivalent circuit of the high frequency rectifier

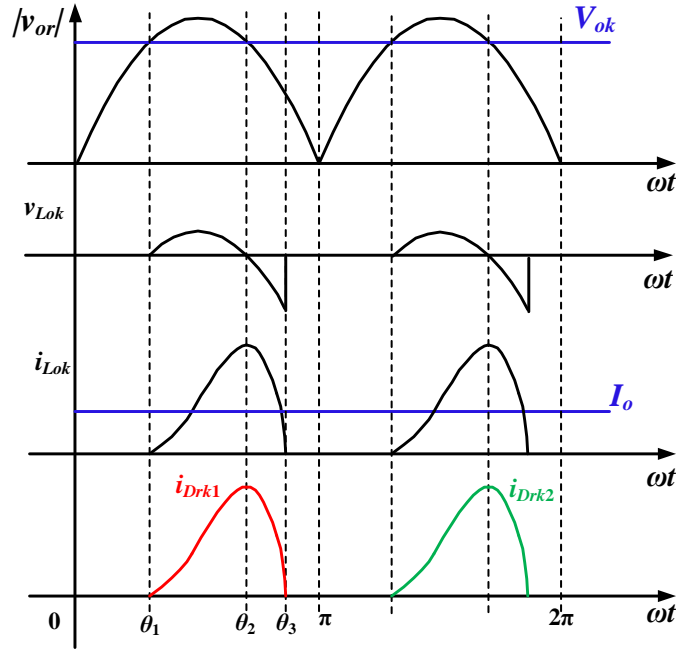


Figure 2.17– Operating waveforms of the high frequency rectifier

### 2.3 Proposed DC-DC Converters with Modular Resonant Circuits and High-Gain Rectifiers

As discussed earlier, step-up resonant converters rely on the high frequency step-up transformers or step-up resonant tank circuits, such as the *CL* (section 2.2) or *LLC* [64] to provide high voltage gain by designing a proper quality factor for the resonant circuit. The topology proposed in section 2.2 demonstrates the case of using modular *CL* resonant converter with current-source type rectification. *LLC* step-up resonant converter with a voltage-fed rectifier [64] is also shown in Figure 2.4(b). However, both converters rely only on resonant circuit modules to provide step-up voltage function. Hence, step-up resonant circuits suffer the drawback of highly sensitive frequency control to regulate the output voltage when a high step-up ratio is required. This

makes variable frequency control not very practical when a high voltage step-up ratio is required. In order to solve the above drawback, and to provide high voltage gain without using high turns-ratio transformers, the proposed converter presented in this section utilizes high-gain rectifiers (also called voltage multipliers) besides the step-up resonant circuits.

### **2.3.1.1 High-Gain Rectifiers**

High-gain rectifiers (HGRs) are an efficient voltage boosting technique that can be utilized at the output stage of a converter to rectify and step up the ac or pulsating dc input. Since only consisting of different combination of diodes and capacitors, voltage multiplier rectifiers (VMRs) are easy to implement with low cost and weight. In this subsection different voltage multiplier rectifiers are discussed and compared with each other. Basically, voltage multiplier rectifiers can be classified into two categories: half-wave and full-wave. The most well-known half-wave and full-wave voltage multipliers are shown in Figure 2.18 and Figure 2.19, respectively. Figure 2.18(a) shows the well-known Greinacher voltage doubler rectifier that can be used at the output of transformer-based dc–dc converters [65]. The main disadvantage of this type of voltage multiplier rectifier is the high voltage stress on the diodes and the output capacitor, which is equal to the high output voltage. To improve the high voltage stress of the components, the improved Greinacher voltage doubler was introduced in [66]. This rectifier is shown in Figure 2.18(b). The voltage stress of all the components is half of the output voltage which facilitates the use of lower voltage rating components. Cockcroft–Walton (CW) is also another well-known voltage multiplier and is shown in Figure 2.18(c). The main advantage of this rectifier is that it can be simply cascaded to boost the voltage in a high level.

Full-wave voltage multipliers are also another well-known type of rectifiers than can be used at the output stage of transformer-based converters. Figure 2.19 (a) illustrates a full-wave voltage doubler rectifier. In this rectifier, the stress of voltage across the diodes and capacitors is half of the output voltage. The voltage multiplier in Figure 2.19(b) is a voltage quadrupler rectifier, formed by a stacked combination of two voltage doublers. The voltage quadrupler rectifier is employed in modern step-up converters due to its balanced voltage stress on the capacitors and diodes.

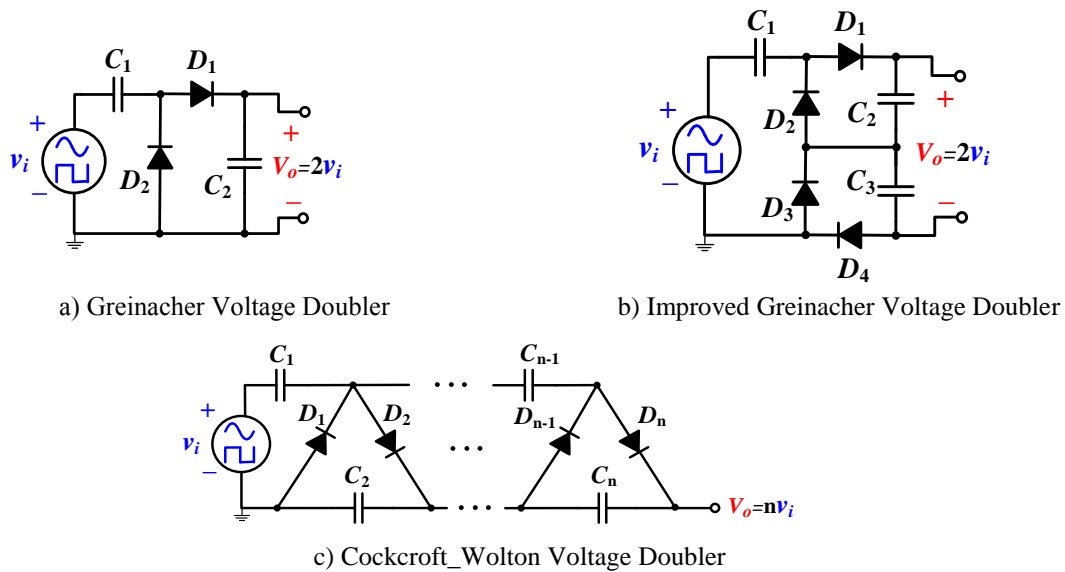


Figure 2.18– Well-known half-wave voltage multiplier rectifiers

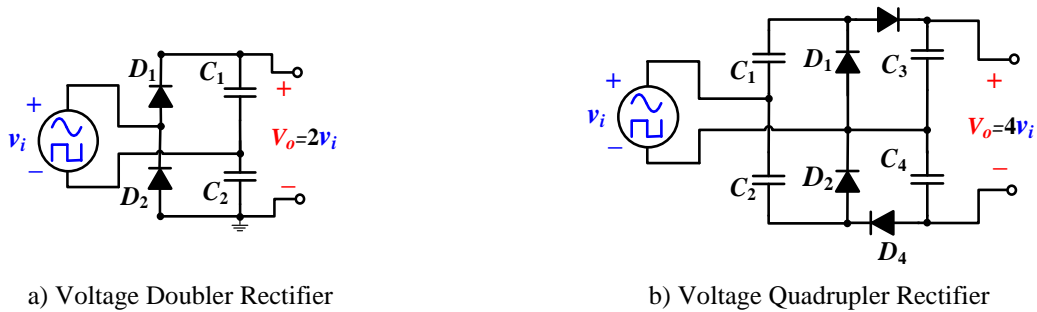


Figure 2.19– Well-known full-wave voltage multiplier rectifiers

The main advantages of full-wave VMRs over the half-wave is the reduced voltage stress on output capacitors (half of the output voltage) and the balanced voltage stress on output capacitors and diodes. Table 2.2 summarizes the voltage stresses on the diodes and capacitors and the component counts of various VMRs.

Table 2.2– Comparison of Different Voltage Multiplier Rectifiers

	Voltage Multiplier Rectifier	Output Voltage $V_o$	Output Diode Voltage Stress	Output Capacitor Voltage Stress	Number of Diodes	Number of capacitors
Half-wave	Greinacher Voltage Doubler	$2 V_{in}$	$V_o$	$V_o$	2	2
	Improved Greinacher Voltage Doubler	$2 V_{in}$	$V_o/2$	$V_o/2$	4	3
	Cockcroft_Wolton Voltage Doubler	$n \cdot V_{in}$	$V_o$	$V_o$	$n$	$n$
Full-wave	Voltage Doubler Rectifier	$2 V_{in}$	$V_o$	$V_o/2$	2	2
	Voltage Quadrupler Rectifier	$4 V_{in}$	$V_o/2$	$V_o/2$	4	4

### 2.3.2 Different Topologies Employing Modular Resonant Circuits and High-Gain Rectifier

The structure of the proposed modular MV step-up dc-dc converter with high-frequency high-gain rectifier modules is shown in Figure 2.20. Different topologies can be derived by employing different voltage multiplier rectifiers. Figure 2.21 shows different topologies that can be employed using the proposed structure: *LLC* step-up resonant modules cascaded with voltage quadrupler modules is shown in Figure 2.21(a); the topology shown in Figure 2.21(b) consists of *LLC* step-up resonant modules and voltage doubler rectifying modules. However, both topologies (Figure 2.21(a) and (b)) require high current resonant inductors. A new *CLL* resonant

converter cascaded with voltage doubler modules is shown in Figure 2.21(c). This topology alleviates the current stress and the inductor size problem, as the resonant inductor  $L_s$  is placed on the secondary side of the isolating transformer. The performance region of the proposed converter compared to the other voltage boosting techniques is shown in Figure 2.22.

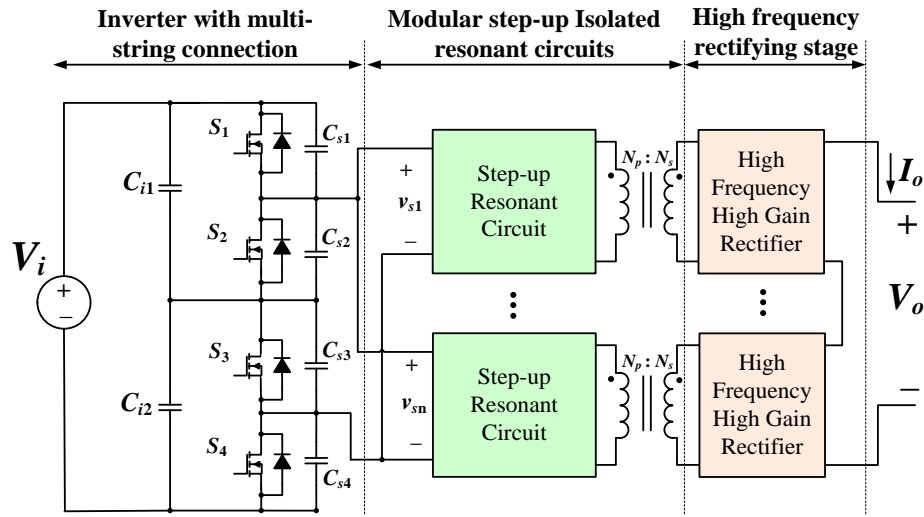
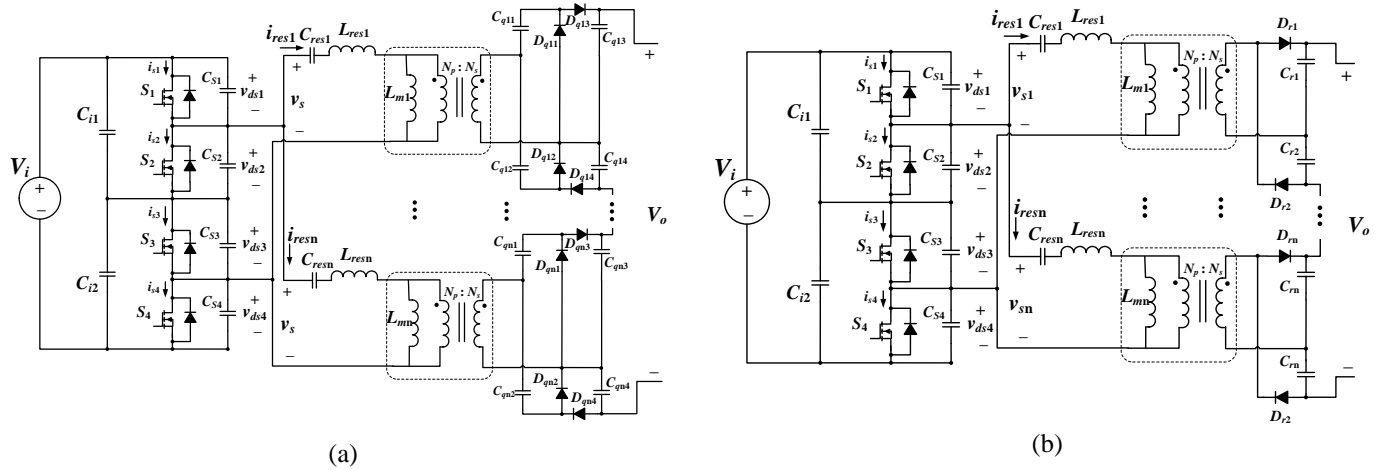


Figure 2.20– Proposed modular MV step-up dc-dc converter with high-frequency high-gain rectifiers



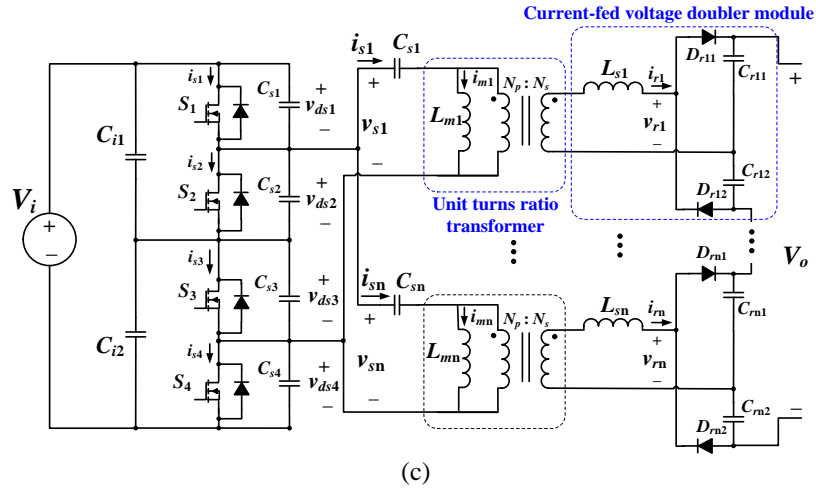


Figure 2.21– Multiple circuit configurations based on the proposed converter structure

- (a) *LLC* step-up resonant converters with HF voltage quadruplers, (b) *LLC* Step-up resonant converters with HF voltage doublers, (c) *CLL* step-up resonant converter with voltage doubler

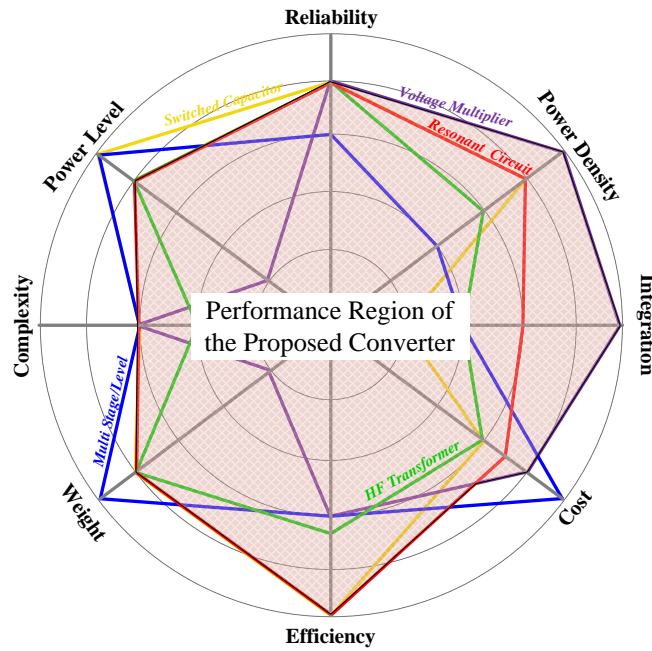


Figure 2.22– Performance region of the proposed converter

## **2.4 Step-Up Resonant Converter with Internally Coupled High Voltage-Gain Modules**

In this section, a fully soft-switched silicon carbide (SiC)-based modular step-up resonant converter with magnetically integrated zero current switching voltage doublers is proposed for medium voltage dc (MVdc) conversion in wind energy systems. The proposed converter configuration utilizes both modular step-up resonant circuits and magnetically integrated voltage doublers to achieve the step up voltage conversion function.

Since the magnetic components are often the heaviest and bulkiest components in the converters, coupled inductors are employed in the proposed converter to reduce the size and weight of the power conversion system. By magnetically integrating the voltage doublers in the output rectifying stage, the output dc voltage balancing of all the converter modules can be achieved much easier without using a complicated balancing control scheme. Moreover, the number of required magnetic components will also be reduced, compared to the individual module's approach with separate components.

The output voltage of each module of the dc-dc step-up converter is regulated through variable frequency control, whereas asymmetrical pulsewidth modulation (APWM) control is utilized to balance all the resonant currents in all the resonant circuits in each converter module. Since APWM control is utilized in the proposed design to balance all the resonant currents in each module, a simple passive auxiliary circuit is included in each converter module to extend soft-switching operation.

### 2.4.1 Circuit Description of the Proposed Converter

The proposed modular dc-dc step-up converter configuration is shown in Figure 2.23, where the input terminals are connected in parallel and the output terminals are connected in series, which is a well-known approach for high input current, high output voltage applications. The proposed converter module consists of multiple step-up resonant circuit modules that are cascaded with magnetically-integrated current-fed voltage doublers. In each of the proposed converter modules, the inverter side consists of multiple strings of switches to reduce the voltage stress across each switch to half of the input voltage. For the  $n$ th module (shown in Figure 2.24), switch pair  $(S_{n1}, S_{n4})$  and switch pair  $(S_{n2}, S_{n3})$  operate in complementary fashion, with switch pair  $(S_{n1}, S_{n4})$  turn ON during the interval  $D_n T_s$ , and switch pair  $(S_{n2}, S_{n3})$  turn ON during the interval  $(1-D_n)T_s$ , where  $D_n$  is the duty ratio and  $T_s$  is the switching period. The passive auxiliary circuit, as highlighted in green, is used to assist switch pair  $(S_{n2}, S_{n3})$  to achieve zero voltage switching turn-ON when  $D_n$  is controlled to a lower value. In general, the proposed topology alleviates the current stress and inductor size problem seen in [53], [64], as the series resonant inductors  $L_{sn1}$ ,  $L_{sn2}$ , and  $L_{sn3}$  (note that  $L_{sn1}$ ,  $L_{sn2}$  and  $L_{sn3}$  will be grouped as  $L_{sn}$  for the rest of this chapter) are placed on the secondary side of the HF isolating transformers. This arrangement enhances the overall circuit efficiency by reducing the winding losses associated with  $L_{sn}$ .

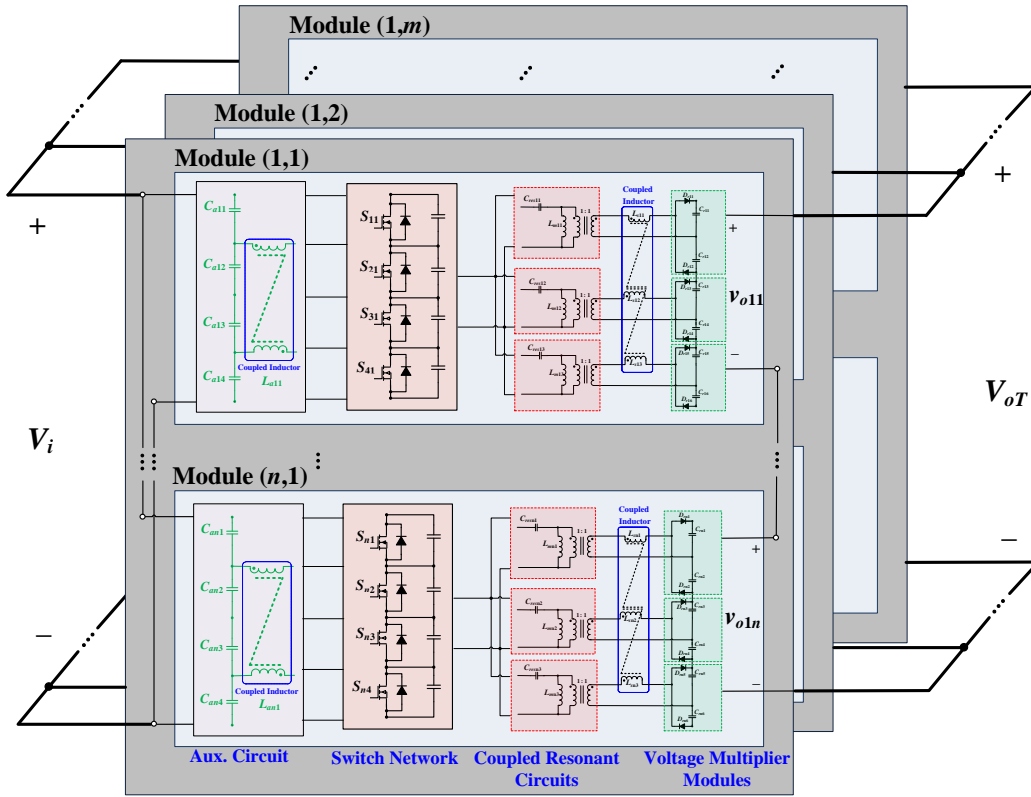


Figure 2.23– Modular structure of the proposed step-up transformerless dc-dc step-up converter

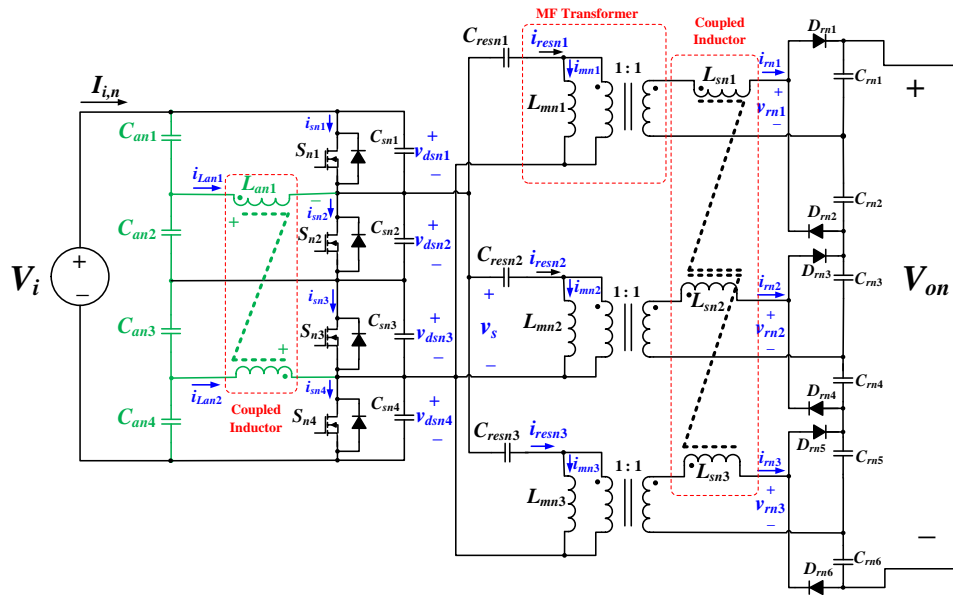


Figure 2.24– Proposed dc-dc step-up converter configuration with magnetically-integrated voltage doublers (per module)

### 2.4.2 Operating Principles of the Proposed Step-up Converter

To simplify the steady-state analysis of the proposed converter, only one module is considered. The operating principles of the proposed converter with one module can be analyzed according to the operating waveforms shown in Figure 2.25. The key operating stages of the circuit within a switching cycle are shown in Figure 2.26.

**$[t_0 < t < t_1]$ :** Prior to this interval,  $C_{sn1}$  and  $C_{sn2}$  have been discharged to the resonant circuit and the voltage across these capacitors have reached zero. At the beginning of this stage at  $t_0$ , the gate signals are applied to  $S_{n1}$  and  $S_{n4}$ . Due to the negative portion of the resonant current  $i_{resn1}$ , currents  $i_{sn1}$  and  $i_{sn4}$  are negative. Hence, the antiparallel diodes of  $S_{n1}$  and  $S_{n4}$  are turned ON. Meanwhile, the voltage across  $S_{n2}$  and  $S_{n3}$  are clamped to dc-link capacitors ( $C_{an2}$ ,  $C_{an3}$ ) voltage, which is half of the input voltage ( $V_i/2$ ).

**$[t_1 < t < t_2]$ :** At  $t_1$ ,  $i_{resn1}$  becomes positive and the negative current flowing through the antiparallel diodes of  $S_{n1}$  and  $S_{n4}$  in the previous stage, now becomes positive. As a result  $S_{n1}$  and  $S_{n4}$  are turned ON under zero voltage condition, implying zero turn-ON losses for  $S_{n1}$  and  $S_{n4}$ .

**$[t_2 < t < t_3]$ :** At the beginning of this interval all the switches are OFF.  $C_{sn1}$  and  $C_{sn4}$  are already discharged into the resonant circuit. This allows using comparatively large snubber capacitors. As a result, voltage across  $S_{n1}$  and  $S_{n4}$  begin to rise slowly and near ZCS turn-OFF is achieved for  $S_{n1}$  and  $S_{n4}$  at  $t_2$ .

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**[ $t_3 < t < t_4$ ]:** At  $t_3$ , the gate signals are applied to  $S_{n2}$  and  $S_{n3}$ ; and the positive  $i_{resn1}$  flows through the antiparallel diodes of  $S_{n2}$  and  $S_{n3}$ . While voltages across  $S_{n1}$  and  $S_{n4}$  remain at  $V_i/2$ , the output voltages of the resonant circuits reverse their polarities.

**[ $t_4 < t < t_5$ ]:** At  $t_4$ , the positive  $i_{resn1}$  in the previous stage becomes negative, the antiparallel diodes of  $S_{n2}$  and  $S_{n3}$  stop conducting, forcing the  $S_{n2}$  and  $S_{n3}$  to be turned ON under ZVS.

**[ $t_5 < t < t_6$ ]:** At  $t_5$ , the gating signals of  $S_{n2}$  and  $S_{n3}$  are removed; and  $C_{sn2}$  and  $C_{sn3}$  start to charge. This allows the voltages across  $S_{n2}$  and  $S_{n3}$  to rise slowly, which means a close to ZCS turn-OFF is achieved for  $S_{n2}$  and  $S_{n3}$ . Due to the negative current of  $i_{resn1}$ , the snubber capacitors  $C_{sn1}$  and  $C_{sn4}$  begin to discharge into the resonant circuit. This stage ends when the gate signals are applied to  $S_{n1}$  and  $S_{n4}$  again.

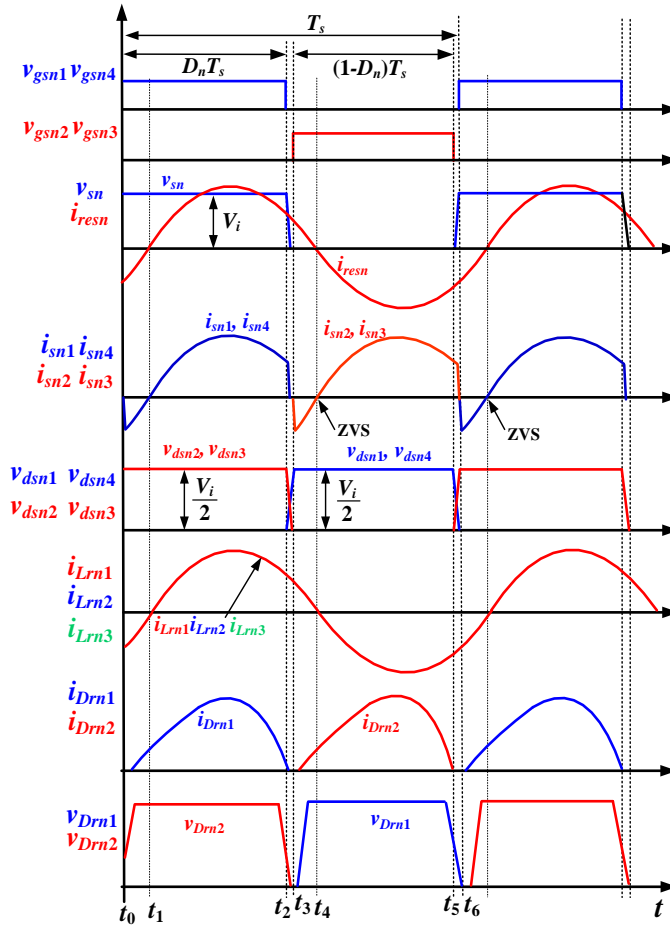


Figure 2.25– Key operating waveforms of the converter (per module)

### 2.4.3 Theoretical Analysis of the Proposed Converter (Per Module)

The equivalent circuit of one module, shown in Figure 2.27, was used to complete the steady state analysis of the proposed topology with the following assumptions.

- 1) All the components, including semiconductor switches and diodes, are ideal.
- 2) The delay between the switches gating signals is neglected.
- 3) The effect of snubber capacitors is neglected.

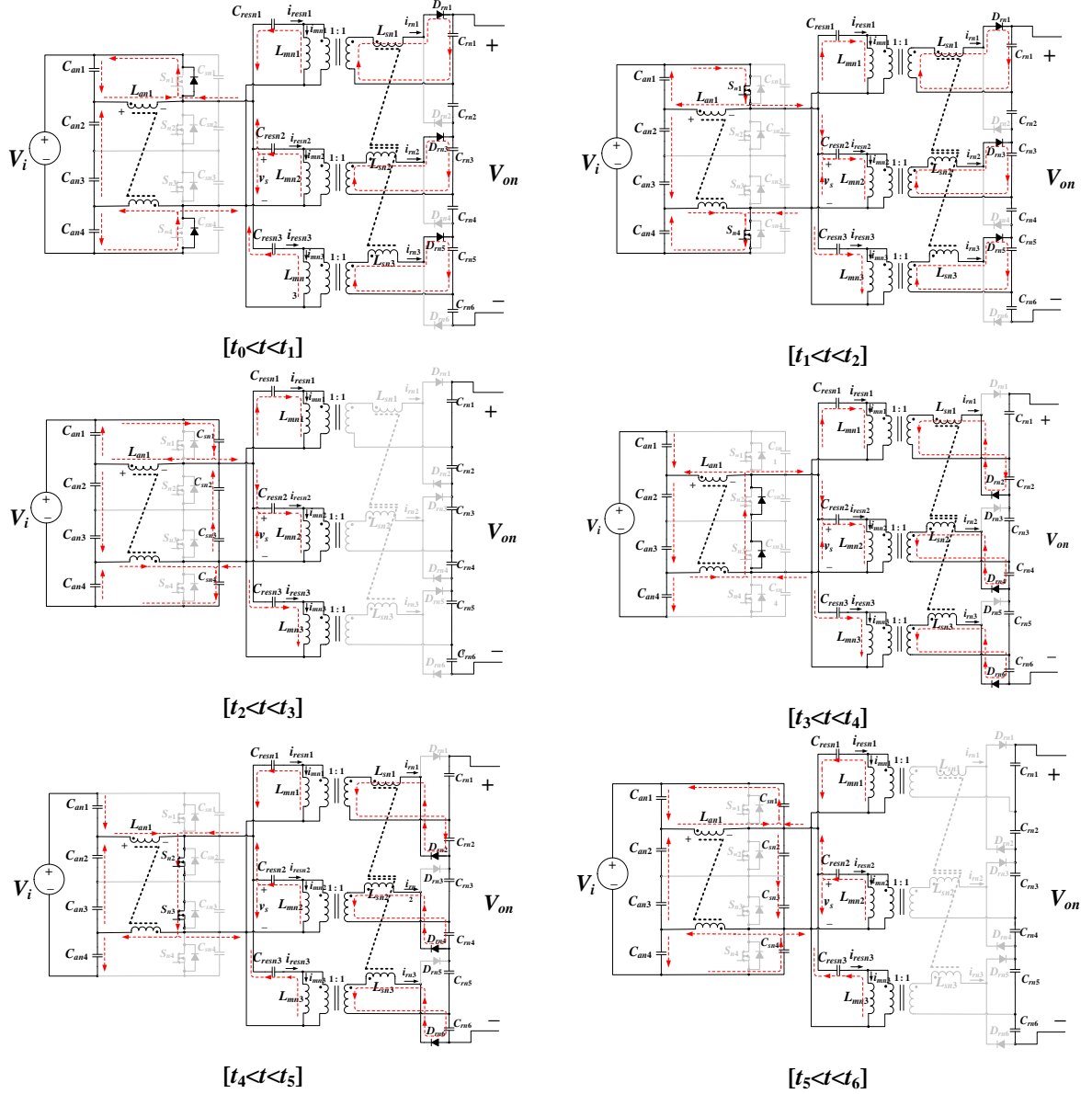


Figure 2.26– Operating stages of the proposed converter within a switching period (illustrated with one module)

The Fourier series representation of the input voltage to the resonant circuit  $v_s$  is given by (2.25). Due to the dc blocking function of  $C_{resn}$ , only ac components of  $v_s$  ( $v_{s(ac)}$ ) is applied to the resonant circuit which is given by (2.26), where  $D_n$  represents the duty cycle;  $\theta_h$  is the phase

angle that is given by (2.27);  $f_s$  is the operating switching frequency; and  $h$  represents the  $h$ th harmonics.

$$v_s = V_i D_n + v_{s(ac)} \quad (2.25)$$

$$v_{s(ac)} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_s t + \theta_h) \right) \quad (2.26)$$

$$\theta_h = \tan^{-1} \left( \frac{\sin(2\pi h D_n)}{1 - \cos(2\pi h D_n)} \right) = \frac{\pi}{2} - \pi D_n \quad (2.27)$$

Since each module consists of three sub-modules of *CLL* resonant circuits and voltage multiplier rectifiers (VMRs), one-third of the output voltage ( $\frac{1}{3} \cdot v_{on}$ ) appeared in the equivalent circuit shown in Figure 2.27.  $R_{ac}$  represents the equivalent load resistance at the output of the resonant circuit (2.28), and the ratio of resonant to magnetizing inductance is  $k = L_{sn}/L_{mn}$ .

$$R_{ac} = \frac{2R}{3\pi^2} \quad (2.28)$$

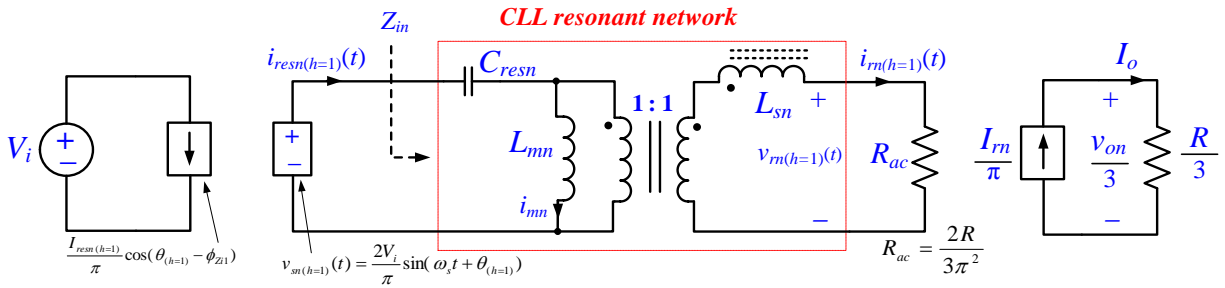


Figure 2.27– The steady state equivalent circuit of the proposed topology

As the output power increases,  $R_{ac}$  approaches zero. At full-load, the resonant frequency is determined by  $C_{resn}$  and the equivalent inductance  $L_{eq}$ , which is the parallel combination of resonant and magnetizing inductances.

$$\omega_{FL} = \frac{1}{\sqrt{L_{eq} C_{resn}}} \quad (2.29)$$

$$L_{eq} = \frac{L_{sn} L_{mn}}{L_{sn} + L_{mn}} = \frac{k}{k+1} L_{mn} \quad (2.30)$$

At no-load,  $R_{ac}$  will be open-circuit, and the resonant frequency is defined by  $C_{resn}$  and  $L_{mn}$  as follows:

$$\omega_{NL} = \frac{1}{\sqrt{L_{mn} C_{resn}}} \quad (2.31)$$

The full-load and no-load relative angular operating frequencies are presented by  $\omega_f$  (2.32) and  $\omega_n$  (2.33), respectively, where  $\omega$  represents the angular operating frequency.

$$\omega_f = \frac{\omega}{\omega_{FL}} \quad (2.32)$$

$$\omega_n = \frac{\omega}{\omega_{NL}} = \omega_f \sqrt{\frac{k+1}{k}} \quad (2.33)$$

The relative operating frequency at no-load in (2.33) shows that  $\omega_n$  is always higher than  $\omega_f$ . Considering the fact that the circuit always operates at switching frequencies above resonance, (2.33) implies that at full-load, the resonant frequency  $\omega_f$  is closer to the switching frequency.

### 2.4.3.1 Resonant Current

In the proposed circuit, the resonant current ( $i_{resn}$ ) expression is given by (2.34), being derived from the ac component of the input voltage to the resonant circuit  $v_{sn}$  in (2.26), where  $|Z_{in}|$  is the magnitude of the input impedance of the resonant circuit, and  $\phi_{Zi}$  is the phase angle of the input impedance [54].

$$i_{resn} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_s t + \theta_h - \phi_{Zi}) \right) \quad (2.34)$$

$$|Z_{in}| = R_{ac} \frac{\sqrt{\alpha^2 + [h\omega_r Q(1/k + \alpha)]^2}}{h\omega_r \sqrt{[h\omega_r(1 + 1/k)]^2 + Q^2}} \quad (2.35)$$

$$\phi_{Zi} = \tan^{-1} \left( h\omega_r Q \left( \frac{1}{k\alpha} + 1 \right) \right) - \tan^{-1} \left( \frac{Q}{-h\omega_r(1 + 1/k)} \right) \quad (2.36)$$

To simplify the equations, the variable  $\alpha$  is defined by (2.37)

$$\alpha = 1 - \frac{(h\omega_r)^2}{k} \quad (2.37)$$

The relative angular operating frequency ( $\omega_r$ ) is given by (2.38), where  $\omega_0$  represents the angular resonant frequency (2.39), and  $Q$  is the quality factor which is given by (2.40).

$$\omega_r = \frac{\omega}{\omega_0} \quad (2.38)$$

$$\omega_0 = \frac{1}{\sqrt{L_{sn} C_{resn}}} \quad (2.39)$$

$$Q = \frac{R_{ac}}{L_{sn}\omega_0} \quad (2.40)$$

From (2.34), the rms resonant current ( $I_{resn}$ ) and the peak value of the fundamental resonant current ( $I_{resn1\_max}$ ) can be determined from the following equations, respectively.

$$I_{resn} = \frac{V_i}{\pi} \left[ \sum_{h=1}^{\infty} \left( \frac{1 - \cos(2\pi h D_n)}{(h|Z_{in}|)^2} \right) \right]^{1/2} \quad (2.41)$$

$$I_{resn1\_max} = \frac{\sqrt{2}V_i}{\pi} \frac{\sqrt{1 - \cos(2\pi D_n)}}{|Z_{in}|} \quad (2.42)$$

The ratio of the coupled inductor magnetizing current,  $i_{mn}$  to  $i_{rn}$  can be given by

$$\frac{I_{mn}}{I_{rn}} = k \left[ 1 - j \frac{Q}{h\omega_r} \right] \quad (2.43)$$

$$\left| \frac{I_{mn}}{I_{rn}} \right| = k \sqrt{1 + \frac{Q^2}{(h\omega_r)^2}} \quad (2.44)$$

(2.44) shows that increasing the switching frequency and decreasing  $k$  and quality factor can reduce the circulating current in the circuit, resulting in lower conduction loss. This equation can be examined with respect to  $k$ . It can be seen that as  $k$  approaches zero (by having  $L_{mn} \rightarrow \infty$ ), the circuit can be approximated as a series-resonant converter and the current through the parallel branch ( $I_{mn}$ ) becomes zero. Hence, circulating current and conduction losses will decrease as the size of  $L_{mn}$  increases. Conversely, the efficiency suffers with a small  $L_{mn}$  as more current will flow through the parallel branch.

### 2.4.3.2 Voltage Gain

The voltage gain of each *CLL* resonant circuit is given by (2.45) as a function of  $\omega_r$ ,  $k$  and  $Q$ .

$$\frac{V_{rn}}{V_{sn}} = \frac{-\omega_r^2}{k\alpha + j\omega_r Q(1+k\alpha)} \quad (2.45)$$

$$\left| \frac{V_{rn}}{V_{sn}} \right| = \frac{\omega_r^2}{\sqrt{(k\alpha)^2 + (\omega_r Q(1+k\alpha))^2}} \quad (2.46)$$

The maximum rms voltage of  $V_{sn}$  occurs at  $D_n=0.5$ . Hence, the voltage conversion ratio of the entire converter can be found based on the equivalent circuit in Figure 2.27:

$$\left| \frac{V_{on}}{V_i} \right| = \left( \frac{V_{on}}{I_o} \right) \times \left( \frac{I_o}{I_{rn(h=1)}} \right) \times \left( \frac{I_{rn(h=1)}}{V_{rn(h=1)}} \right) \times \left( \frac{V_{rn(h=1)}}{V_{sn(h=1)}} \right) \times \left( \frac{V_{sn(h=1)}}{V_i} \right) \quad (2.47)$$

$$\left| \frac{V_{on}}{V_i} \right| = (R) \times \left( \frac{1}{\pi} \right) \times \left( \frac{1}{R_{ac}} \right) \times \left( \frac{\omega_r^2}{\sqrt{(k\alpha)^2 + (\omega_r Q(1+k\alpha))^2}} \right) \times \left( \frac{2}{\pi} \right) = \frac{3\omega_r^2}{\sqrt{(k\alpha)^2 + (\omega_r Q(1+k\alpha))^2}} \quad (2.48)$$

A plot of the voltage gain as a function of  $\omega_r$  and  $k$  has been shown in Figure 2.28. It is shown that each curve peaks at a different value of  $k$ . This value is  $k_{critical}$  and represents the point where  $\phi_{zi}=0$ . To achieve ZVS, the operating frequency should always be above the resonant frequency. This means that  $k$  should be selected above  $k_{critical}$ . It also can be seen from Figure 2.28 that higher voltage gain can be achieved by higher  $k$ . On the other hand, according to (19), increasing  $k$  can increase the circulating current. Therefore, there should be a trade-off between the voltage-gain and the achieved efficiency. A plot of (2.48) for a constant  $k$  ( $k=0.5$ ) and as a function of  $\omega_r$  for different loading conditions is shown in Figure 2.29.

The next step in designing the converter is to ensure that ZVS will be maintained for all load conditions with a minimized circulating current. To do this, the turn-OFF currents of the switches should be analyzed. For example, the turn-OFF currents of switches  $S_{n1}$  and  $S_{n4}$  provide information whether  $S_{n2}$  and  $S_{n3}$  are turned ON under zero voltage.

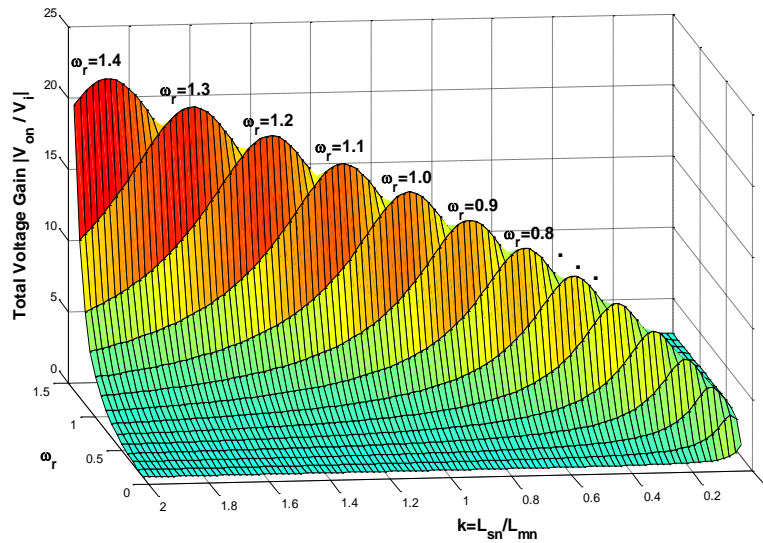


Figure 2.28– Converter voltage gain as a function of  $\omega_r$  and  $k$  for  $Q=3$

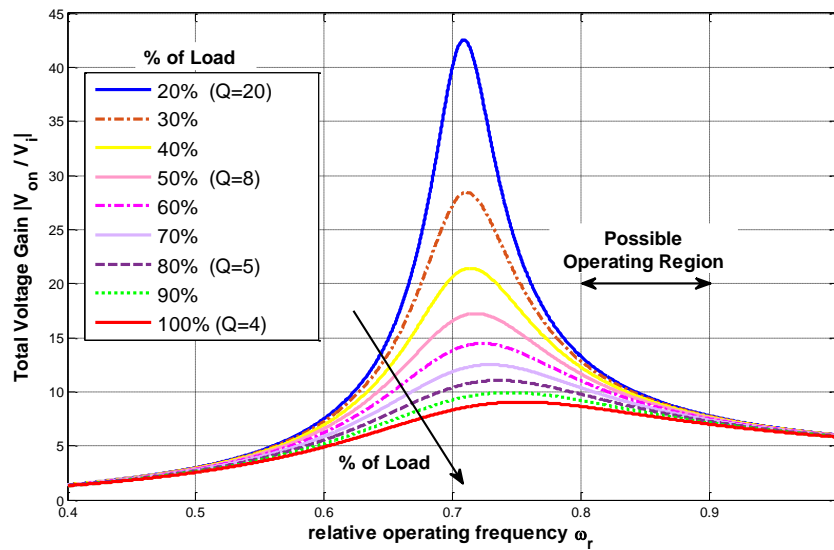


Figure 2.29– Converter voltage gain as a function of  $\omega_r$  for  $k=0.5$

### 2.4.3.3 Turn-OFF Currents of $S_{n1}$ , $S_{n4}$ ( $I_1$ , $I_4$ )

The turn-OFF current of  $S_1$  is the resonant current  $i_{resn}$  at  $t = D_n T_s$ , given by

$$I_1 = I_4 = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h D_n + \theta_h - \phi_{Zi}) \right) \quad (2.49)$$

To turn ON  $S_{n2}$  and  $S_{n3}$  under zero voltage switching, as shown in Figure 2.26, the resonant current should force the antiparallel diodes to conduct prior to the turn-ON instant of the switches. Hence,  $I_1$  and  $I_4$  must be positive. The normalized turn-OFF currents of  $S_{n1}$  and  $S_{n4}$  ( $I_1$  and  $I_4$ ) as a function of duty cycle ( $D_n$ ) and  $k$  is shown in Figure 2.30, for  $\omega_r=2$  and  $Q=4$ . The equivalent ac resistance  $R_{ac}$ , the dc input voltage  $V_i$ , and the angular resonant frequency  $\omega_0$  are chosen as the base values. The figure illustrates that as  $k$  increases, the hard-switching region occurs for a wider range of duty ratio  $D_n$ . This figure also shows that the curves with higher  $k$  have the greatest magnitudes, resulting in higher conduction loss.

### 2.4.3.4 Turn-OFF Currents of $S_{n2}$ , $S_{n3}$ ( $I_2$ , $I_3$ )

Similarly, the turn-OFF currents of switches  $S_{n2}$  and  $S_{n3}$  are found by evaluating (10) at  $t=0$ , given as follows:

$$I_2 = I_3 = \sum_{h=1}^{\infty} \left( \frac{-\sqrt{2}V_i}{h\pi|Z_i|} \sqrt{1 - \cos(2h\pi d)} \sin(\theta_h - \phi_{Zi}) \right) \quad (2.50)$$

The same reasoning can be applied to  $S_{n2}$  and  $S_{n3}$ . To allow current flow through the antiparallel diodes and achieving zero voltage switching for  $S_{n1}$  and  $S_{n4}$ ,  $I_2$  and  $I_3$  must be positive. A plot of (2.50) for different sets of parameters ( $k$  and  $D_n$ ) is also shown in Figure 2.31.

It can be seen from this figure that with increasing  $k$ , the soft-switching operation of  $S_{n1}$  and  $S_{n4}$  is lost at high duty ratios.

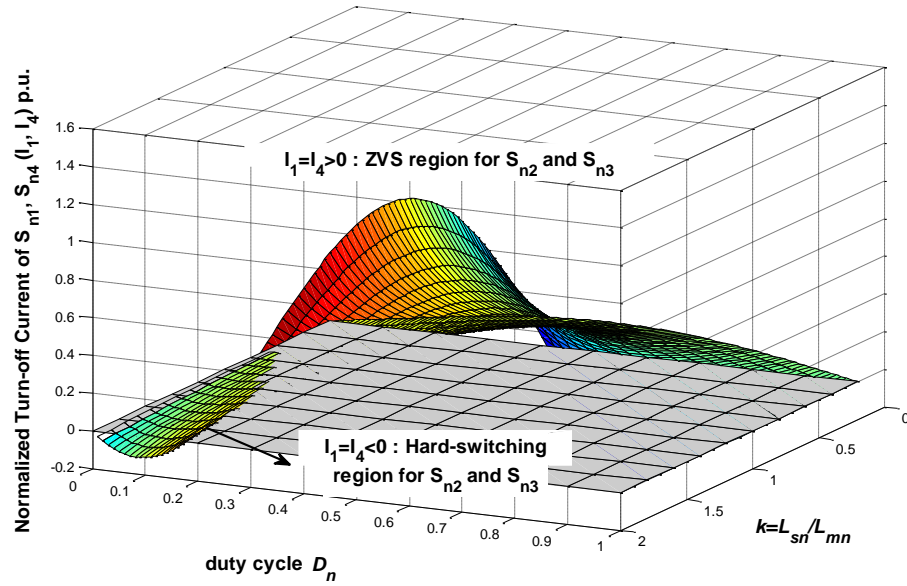


Figure 2.30– Normalized turn-OFF current of  $S_{n1}$  and  $S_{n4}$  ( $I_1$  and  $I_4$ ) as a function of duty cycle  $D_n$  and  $k$  for  $\omega_r=2$  and  $Q=4$

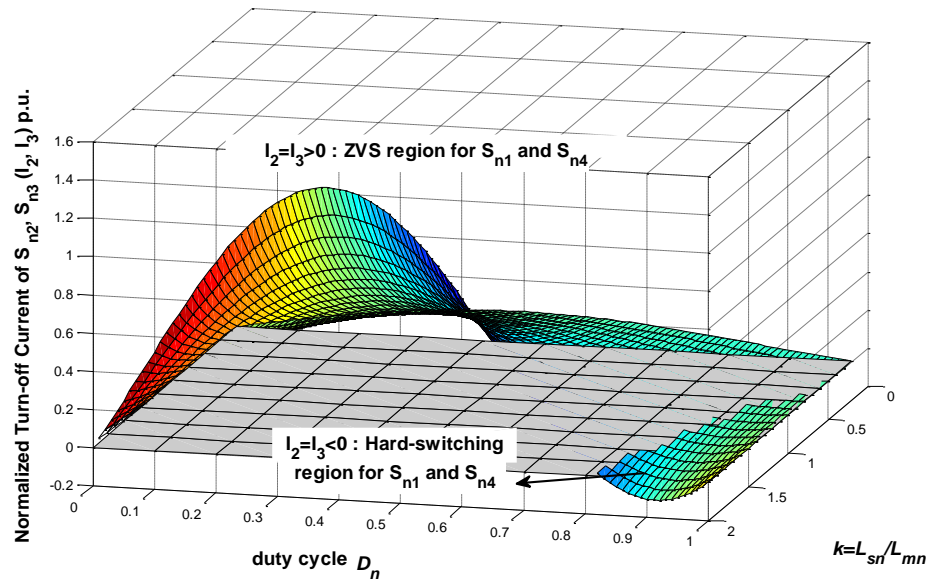


Figure 2.31– Normalized turn-OFF current of  $S_{n2}$  and  $S_{n3}$  ( $I_2$  and  $I_3$ ) as a function of duty cycle  $D_n$  and  $k$  for  $\omega_r=2$  and  $Q=4$

### 2.4.3.5 Resonant Current Balancing in Each Module

Due to the modular resonant circuit structure in the proposed converter, variations in the resonant circuit components can lead to discrepancies in the resonant currents as well as variations in the output voltages of the resonant circuits. To ensure that the resonant currents ( $i_{resn1}$ ,  $i_{resn2}$  and  $i_{resn3}$ ) are balanced in each converter module, the control principle shown in Figure 2.32 is used, where the errors among these currents are regulated through adjusting the duty ratio of the switches with APWM control. A low-pass filter is used before the control signal is fed to the PID compensator for the inner control loop. The outer voltage control loop will be used to regulate the output dc voltage of each module ( $V_{on}$ ). However, using APWM control method will potentially affect the soft-switching operation of one switch pair in each module of the proposed converter, under some operating conditions. Hence, a passive auxiliary circuit, highlighted in green in Figure 2.23, is employed to ensure that soft-switching operation over a wide range of operating points is provided. Details about the operating principles of the auxiliary circuit will be discussed next.

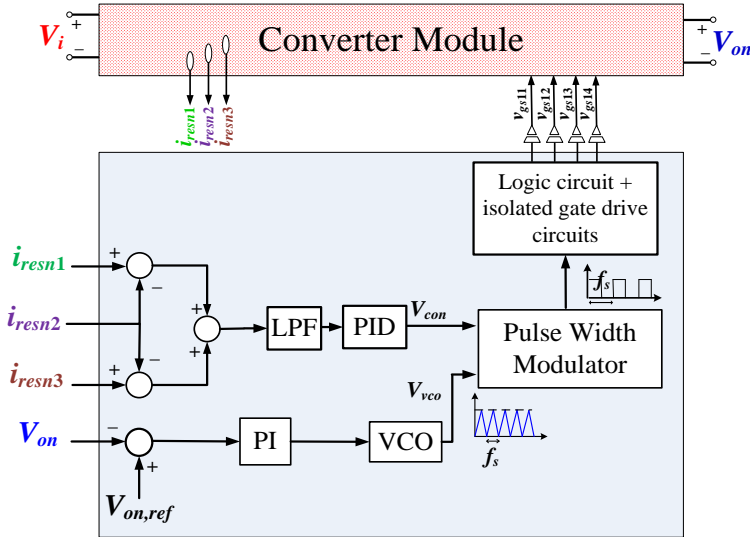


Figure 2.32– Control block diagram for balancing resonant currents in each converter module

### 2.4.3.6 Extended Soft-Switching Operation

Since APWM control is used to ensure all three resonant currents are balanced in each converter module, one switch pair (i.e.,  $S_{n2}$ ,  $S_{n3}$ ) in the inverter may lose ZVS turn-ON when  $D_n$  is reduced. The auxiliary circuit shown in Figure 2.24 consists of a network of four capacitors and a coupled inductor ( $L_{an1}$ ). The coupled inductor provides compensating current to maintain ZVS when  $S_{n2}$  and  $S_{n3}$  in the inverter operates with much reduced  $D_n$ ; and the input capacitors ( $C_{an1}$ ,  $C_{an2}$ ,  $C_{an3}$ ,  $C_{an4}$ ) split the dc-link voltage. The two key operating states of the auxiliary circuit in one converter module are shown in Figure 2.33.

The voltage across the auxiliary inductors and the current through them are shown in Figure 2.34. From the voltage across the auxiliary capacitors ( $V_{ca1}$  and  $V_{ca2}$ ), the voltage across the auxiliary inductor  $v_{La1}$  is calculated. Considering the inductor volt-second balance over one switching period ( $D_n T_s V_{ca1} = (1 - D_n) T_s V_{ca2}$ ), and the fact that  $C_{a1}$  and  $C_{a2}$  split the half of dc input

voltage ( $V_{ca1}+V_{ca2}=V_i/2$ ), the steady state voltage of the auxiliary capacitors can be given by (2.51) and (2.52), respectively. Hence, the time variation of  $v_{Lan1}$  and  $i_{Lan1}$  can be obtained as shown in (2.53) and (2.54), respectively.

$$V_{ca1} = (1 - D_n) \frac{V_i}{2} \quad (2.51)$$

$$V_{ca2} = D_n \frac{V_i}{2} \quad (2.52)$$

$$v_{Lan1} = \frac{V_i}{\pi} \sum_{h=1,3,5,\dots}^{\infty} \left( \frac{1}{n} \sin[h\pi(1 - D_n)] \cos[2\pi h f_s t - h\pi(1 + D_n)] \right) \quad (2.53)$$

$$i_{Lan1} = \frac{V_i}{\pi \omega L_{an1}} \sum_{h=1,3,5,\dots}^{\infty} \left( \frac{1}{n^2} \sin[h\pi(1 - D_n)] \sin[2\pi h f_s t - h\pi(1 + D_n)] \right) \quad (2.54)$$

(2.55) represents the peak value of  $i_{Lan1}$  which occurs at  $t=t_2$  and  $t=t_5$  when the switches are turned OFF (see Figure 2.25).

$$i_{Lan1\_pk} = \frac{1}{L_{an1}} \int_{(1-d)T_s/2} V_{ca2} dt = \frac{D_n(1-D_n)}{4f_s L_{an1}} V_i \quad (2.55)$$

With introducing  $m$  that relates  $L_s$  to  $L_{an1}$  as  $m = L_{an1}/L_s$ ,  $i_{Lan1}$  can be normalized to its per unit expression given by the following equation:

$$i_{Lan1\_pk} = \frac{1}{L_{an1}} \int_{(1-d)T_s/2} V_{ca2} dt = \frac{D_n(1-D_n)}{4f_s L_{an1}} V_i \quad (2.56)$$

Since the peak value of the auxiliary inductor occurs at turning-OFF instants and provides extra lagging current, ZVS can be achieved over a wide range of operating points. The calculation for  $(I_1, I_4)$  and  $(I_2, I_3)$  with the auxiliary circuit is represented by

$$I_1 = I_4 = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h D_n + \theta_h - \phi_{zi}) + \frac{\pi d(1 - D_n)Q}{2m(h\omega_r)} \right) \quad (2.57)$$

$$I_2 = I_3 = \sum_{h=1}^{\infty} \left( \frac{-\sqrt{2}V_i}{h\pi|Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \sin(\theta_h - \phi_{zi}) + \frac{\pi d(1 - D_n)Q}{2m(h\omega_r)} \right) \quad (2.58)$$

The normalized turn-OFF currents of  $S_{n1}$  and  $S_{n4}$  ( $I_1$  and  $I_4$ ), and the ZVS region for the circuit with the passive auxiliary circuit as a function of duty cycle  $D_n$  and  $k$  for  $\omega_r=2$ ,  $Q=4$  and  $m=7$  are shown in Figure 2.35. Compared to Figure 2.31, it can be seen that the circuit with the auxiliary circuit is able to achieve ZVS over a wider range of operating points and duty ratios.

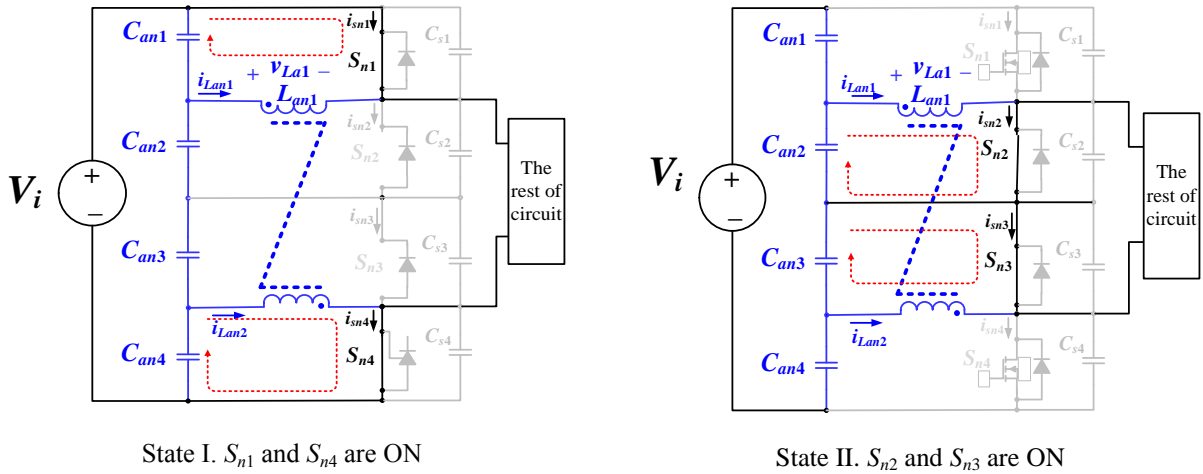


Figure 2.33– Key operating stages of the auxiliary circuit in the proposed converter (one module illustrated)

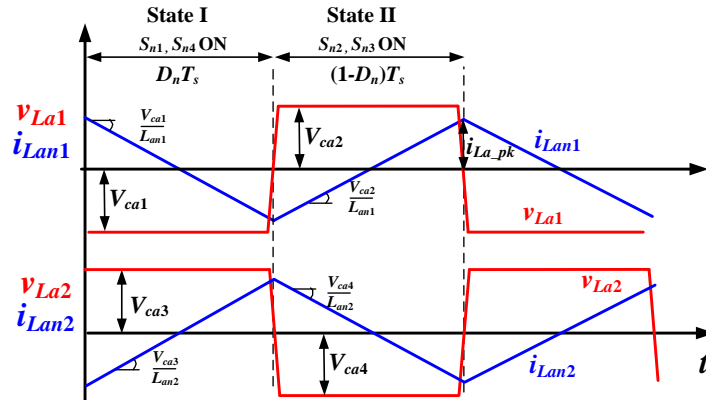


Figure 2.34– Key operating waveforms of the auxiliary circuit in the proposed converter

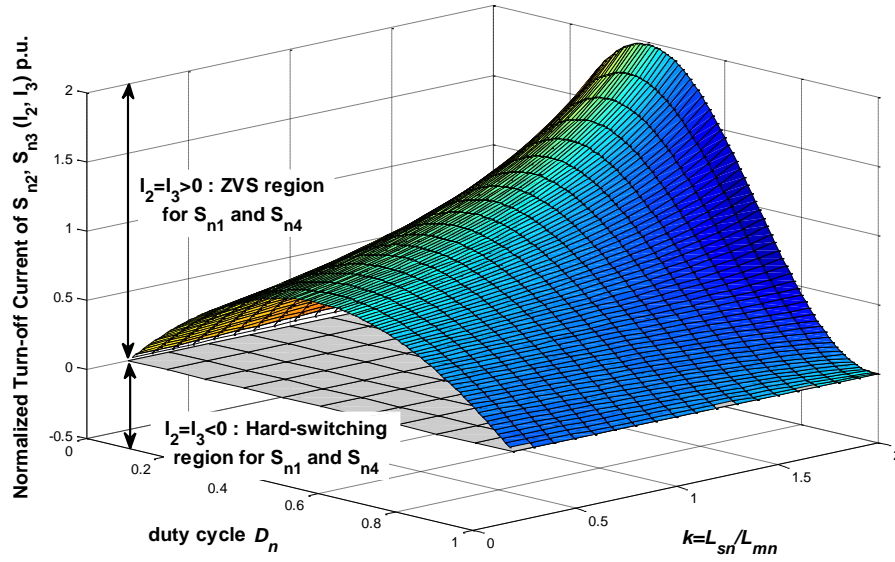


Figure 2.35– Normalized turn-OFF current of  $S_{n2}$  and  $S_{n3}$  ( $I_2$  and  $I_3$ ) with the auxiliary circuit as a function of duty cycle  $D_n$  and  $k$  for  $\omega_r=2$ ,  $Q=4$  and  $m=7$ .

#### 2.4.3.7 Voltage Balancing Technique across Input Capacitors

In the proposed step-up converter, snubber capacitors ( $C_{sn1} \sim C_{sn4}$ ) play an important role in reducing the turn-OFF switching loss in each switch by allowing the switch voltage to rise slowly from zero, after the switch is turned OFF. However, in a practical circuit, variation in these capacitances can introduce voltage unbalance across input capacitors ( $C_{an1} \sim C_{an4}$ ), which will subsequently affect the switch voltages by introducing voltage unbalance among the switch voltages. To ensure that the voltage across each input capacitor is always balanced, a simple passive balancing circuit is used at the input of each resonant circuit module as shown in Figure 2.36. The use of an auxiliary circuit to provide input capacitor voltage balancing has been discussed for symmetrical half-bridge inverters in [67]. To apply similar technique to the proposed converter, each auxiliary circuit consists of a capacitor  $C_{aux}$  connected in series to the

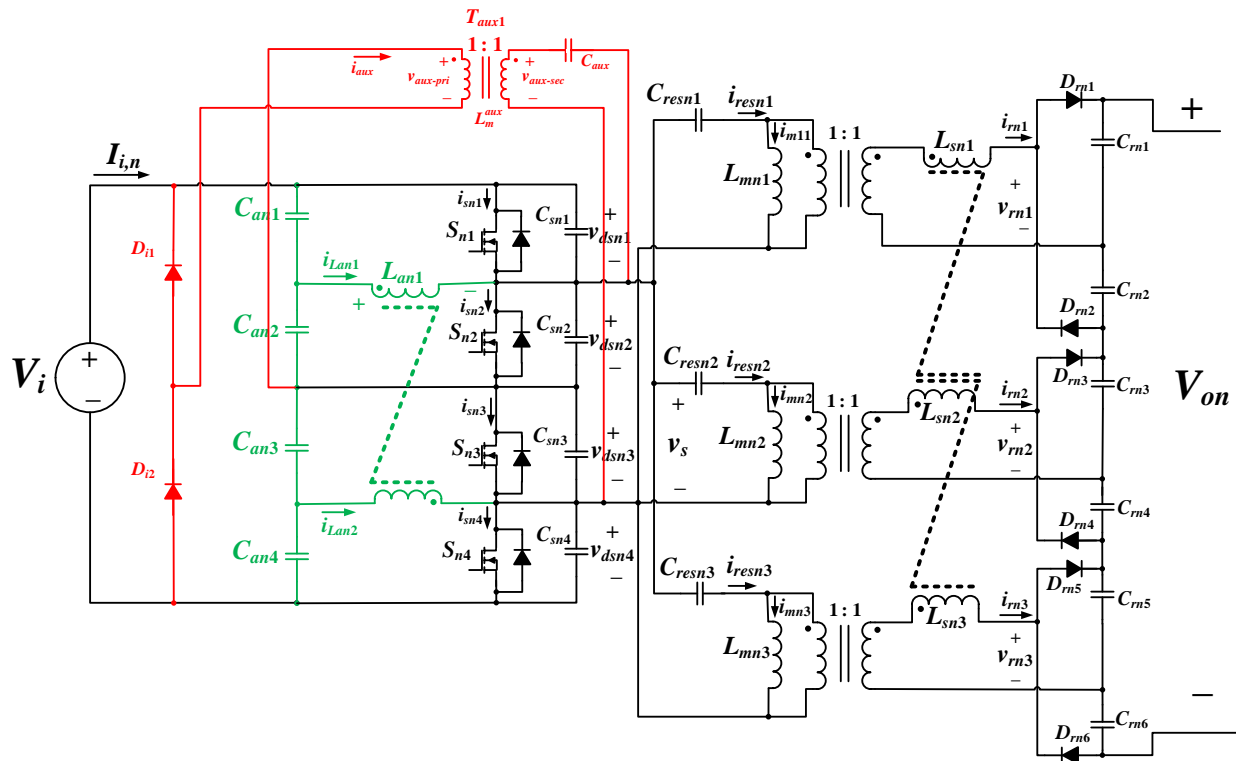


Figure 2.36– Voltage balancing technique with auxiliary circuit in the proposed converter (with only one module)

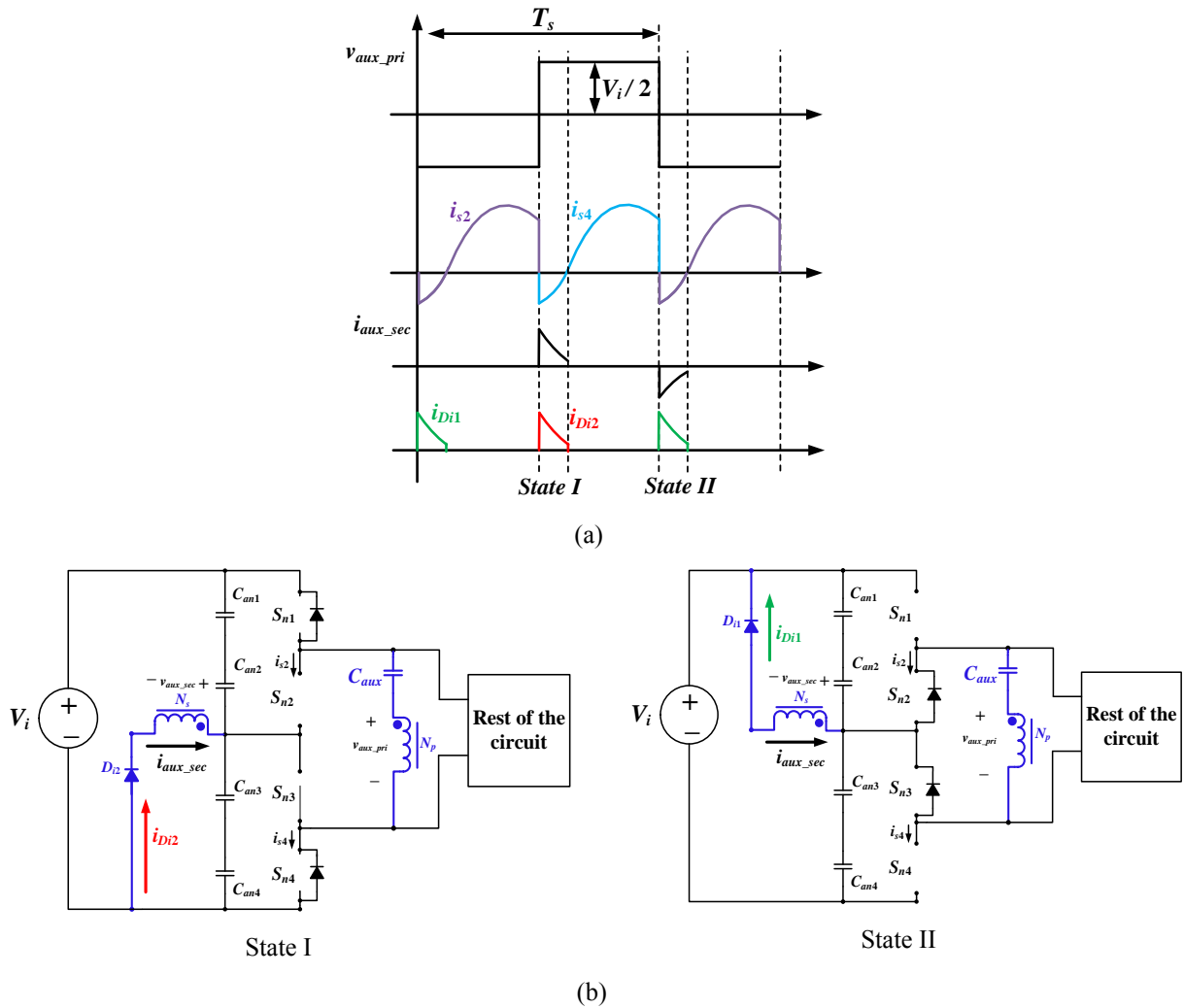
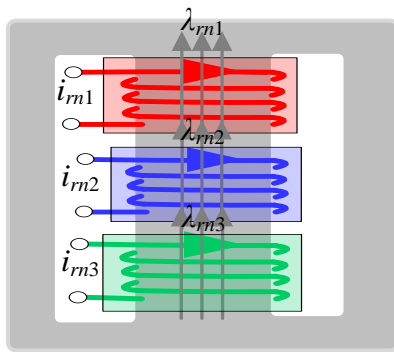


Figure 2.37– Operating waveform and stages with the auxiliary voltage balancing circuit

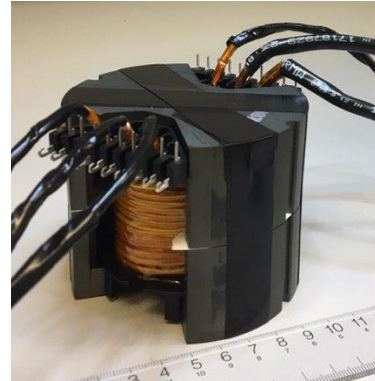
### 2.4.3.8 Design of the Coupled Inductor

Since the proposed converter utilizes coupled inductors to balance the current sharing of the three high-frequency and high-gain rectifiers, this section will briefly describes the structure of the coupled inductor. It has been highlighted in literature that in high power applications, magnetic components account for a considerable proportion of the weight and size of the entire

system [68]. This is particularly critical in offshore wind turbines, where the volume and weight of the system is of great importance. By using magnetic integration in the proposed converter, the total volume of magnetic core and copper usage can be reduced, which will result in a significant reduction in the system weight and volume. The structural diagram of the three coupled inductors is shown in Figure 2.38(a). The flux passes across the midleg, enabling three separate inductors to be integrated into a single core. Two types of magnetic cores that can be suitable for the proposed converter design are: ferrite N87 and nanocrystalline core material. To reduce the skin effect and mitigate proximity effect, parallel high-frequency Litz wire bundles are also utilized for each winding. As a result, lower volumes of conductive material are required. Figure 2.38(b) shows a picture of the designed coupled inductor.



(a)



(b)

Figure 2.38– (a) Structural diagram of the coupled inductor, (b) a picture of the implemented coupled inductor

#### 2.4.4 Converter Modeling

To analyze the control algorithm, the small-signal model and the control-to-output transfer functions are obtained in this section using extended describing function (EDF).

State-space averaging (SSA) techniques are well-known approaches in effective modeling of switching circuits, but only when the variations of ac signals is much smaller than their quiescent operating points. In the resonant converters, however, the sinusoidal variations are large in magnitude and the coupling between ac and dc state variables is nonlinear. Hence SSA and circuit averaging methods cannot be applied for the resonant converter modeling [69], [70]. Sampled data modeling can also provide an accurate model of power electronic circuits in which a steady state trajectory can be obtained by solving piece-wise linear state equations [71]. However, its analytical expressions cannot provide physical insight behavior of the circuit.

In order to derive accurate large signal and small signal models of the resonant circuits, the extended describing function (EDF) method, which can handle multistate variables, such as resonant inductor currents, resonant capacitor voltages, and other non-sinusoidal variables has been successfully adopted in some papers, including [69], [72]–[74].

This section presents an accurate analysis of the frequency characteristics of the variable frequency control *CLL* resonant converter, based on EDF method. The small-signal model and control-to-output transfer functions are obtained by linearizing each nonlinear element in the vicinity of the steady state operating point.

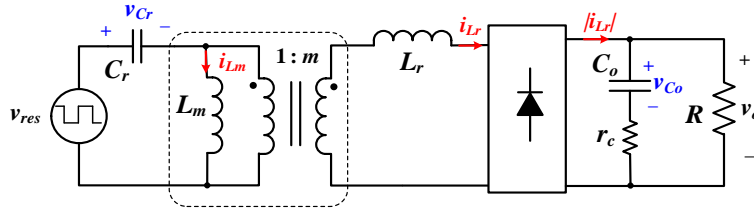


Figure 2.39– Equivalent circuit of the *CLL* resonant converter for modelling

The equivalent circuit of the *CLL* resonant converter is shown in Figure 2.39. To simplify the analysis, only one module of the resonant circuit has been considered in the modeling. As discussed in section 2.4.3, the switch network generates a square wave voltage  $v_{res}$  (2.26) that applies to the resonant circuit. Based on the first harmonic approximation (FHA) and the assumption of  $d=0.5$ ,  $v_{res}$  can be simplified as

$$v_{res} = \frac{2V_g}{\pi} \sin(h\omega_s t) \quad (2.59)$$

#### 2.4.4.1 Nonlinear State Equations and Harmonic Approximation

By applying KVL and KCL to the circuit, shown in Figure 2.39, the nonlinear state equations can be given by

$$\frac{di_{L_r}}{dt} = -\frac{\text{sign}(i_{L_r})v_o}{L_r} - \frac{mv_{cr}}{L_r} + \frac{mv_{res}}{L_r} \quad (2.60)$$

$$\frac{di_{L_m}}{dt} = \frac{v_{res}}{L_m} - \frac{v_{cr}}{L_m} \quad (2.61)$$

$$\frac{dv_{cr}}{dt} = \frac{mi_{L_r}}{C_r} + \frac{i_{L_m}}{C_r} \quad (2.62)$$

$$\frac{dv_{co}}{dt} = \frac{R}{(R+r)C_o} \left[ |i_{Lr}| - \frac{v_{co}}{R} \right] \quad (2.63)$$

where  $i_{Lr}$ ,  $i_{Lm}$ ,  $v_{cr}$ , and  $v_{co}$  are state variables. Under the assumption that the voltage and current inside the *CLL* resonant network are quasi-sinusoidal, the fundamental approximation method can be applied to  $i_{Lr}$ ,  $i_{Lm}$ ,  $v_{cr}$ .

$$i_{Lr}(t) = i_{Lrs}(t) \sin(\omega_s t) + i_{Lrc}(t) \cos(\omega_s t) \quad (2.64)$$

$$i_{Lm}(t) = i_{Lms}(t) \sin(\omega_s t) + i_{Lmc}(t) \cos(\omega_s t) \quad (2.65)$$

$$v_{cr}(t) = v_{crs}(t) \sin(\omega_s t) + v_{crc}(t) \cos(\omega_s t) \quad (2.66)$$

The derivatives of  $i_{Lr}$ ,  $i_{Lm}$ ,  $v_{cr}$ , and  $v_{co}$  are given by

$$\frac{di_{Lr}}{dt} = \left[ \frac{di_{Lrs}}{dt} - \omega_s i_{Lrc} \right] \sin(\omega_s t) + \left[ \frac{di_{Lrc}}{dt} + \omega_s i_{Lrs} \right] \cos(\omega_s t) \quad (2.67)$$

$$\frac{di_{Lm}}{dt} = \left[ \frac{di_{Lms}}{dt} - \omega_s i_{Lmc} \right] \sin(\omega_s t) + \left[ \frac{di_{Lmc}}{dt} + \omega_s i_{Lms} \right] \cos(\omega_s t) \quad (2.68)$$

$$\frac{dv_{cr}}{dt} = \left[ \frac{dv_{crs}}{dt} - \omega_s v_{crc} \right] \sin(\omega_s t) + \left[ \frac{dv_{crc}}{dt} + \omega_s v_{crs} \right] \cos(\omega_s t) \quad (2.69)$$

#### 2.4.4.2 Extended Describing Function (EDF), Perturbation and Linearization

By employing the EDF modelling technique stated in the literature, the nonlinear terms in equations (2.60)–(2.63) can be approximated either by the fundamental harmonic terms or the dc terms, to yield:

$$v_{res} \approx F_1(v_g) \sin(\omega_s t) \quad (2.70)$$

$$\text{sign}(i_{Lr})v_o \approx F_2(i_{Lrs}, v_{co})\sin(\omega_s t) + F_3(i_{Lrc}, v_{co})\cos(\omega_s t) \quad (2.71)$$

$$|i_{Lr}| \approx F_4(i_{Lrs}, i_{Lrc}) \quad (2.72)$$

$$i_g \approx F_5(i_{Lms}, i_{Lrs}) \quad (2.73)$$

where  $F_1 \sim F_5$  are extended describing functions (EDFs) that can be calculated by making Fourier expansions of nonlinear terms, given by

$$F_1(v_g) = \frac{2V_g}{\pi} \quad (2.74)$$

$$F_2(i_{Lrs}, v_{co}) = \frac{4}{\pi} \frac{i_{Lrs}}{\sqrt{i_{Lrs}^2 + i_{Lrc}^2}} v_{co}, \quad F_3(i_{Lrc}, v_{co}) = \frac{4}{\pi} \frac{i_{Lrc}}{\sqrt{i_{Lrs}^2 + i_{Lrc}^2}} v_{co} \quad (2.75)$$

$$F_4(i_{Lrs}, i_{Lrc}) = \frac{2}{\pi} i_p = \frac{2}{\pi} \sqrt{i_{Lrs}^2 + i_{Lrc}^2} \quad (2.76)$$

$$F_5(i_{Lms}, i_{Lrs}) = \frac{2}{\pi} \sin\left(\frac{\pi d}{2}\right)(i_{Lms} + m i_{Lrs}) \quad (2.77)$$

After finding the steady state solutions, the complete linearized small-signal models can be established by perturbing the system around operating points:  $v_g = V_g + \hat{v}_g$  and  $\omega_s = \Omega_s + \hat{\omega}_s$ . After obtaining the equations, the small signal transfer function can be derived on the basis of the state-space method.

$$\begin{cases} \frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} \\ \hat{y} = C\hat{x} + D\hat{u} \end{cases} \quad \begin{aligned} \hat{x} &= (\hat{i}_{Lrs}, \hat{i}_{Lrc}, \hat{i}_{Lms}, \hat{i}_{Lmc}, \hat{v}_{crs}, \hat{v}_{crc}, \hat{v}_{co})^T \\ \hat{u} &= (\hat{v}_g, \hat{\omega}_{sn})^T, \quad \hat{y} = (\hat{v}_o, \hat{i}_g)^T \end{aligned} \quad (2.78)$$

where

$$\begin{aligned}
A &= \begin{bmatrix} -\frac{R_{ac}}{L_r} \cdot \frac{\beta^2}{(\alpha^2 + \beta^2)} & \frac{R_{ac}}{L_r} \cdot \frac{\alpha\beta}{(\alpha^2 + \beta^2)} + \Omega_s & 0 & 0 & -\frac{m}{L_r} & 0 & -\frac{2}{\pi L_r} \cdot \frac{\alpha}{\sqrt{\alpha^2 + \beta^2}} \\ \frac{R_{ac}}{L_r} \cdot \frac{\alpha\beta}{(\alpha^2 + \beta^2)} - \Omega_s & -\frac{R_{ac}}{L_r} \cdot \frac{\alpha^2}{(\alpha^2 + \beta^2)} & 0 & 0 & 0 & -\frac{m}{L_r} & -\frac{2}{\pi L_r} \cdot \frac{\beta}{\sqrt{\alpha^2 + \beta^2}} \\ 0 & 0 & 0 & \Omega_s & -\frac{1}{L_m} & 0 & 0 \\ 0 & 0 & -\Omega_s & 0 & 0 & -\frac{1}{L_m} & 0 \\ \frac{m}{C_r} & 0 & \frac{1}{C_r} & 0 & 0 & \Omega_s & 0 \\ 0 & \frac{m}{C_r} & 0 & \frac{1}{C_r} & -\Omega_s & 0 & 0 \\ \frac{R}{R+r} \frac{2}{\pi} \frac{\alpha}{C_o \sqrt{\alpha^2 + \beta^2}} & \frac{R}{R+r} \frac{2}{\pi} \frac{\beta}{C_o \sqrt{\alpha^2 + \beta^2}} & 0 & 0 & 0 & 0 & \frac{-1}{(R+r)C_o} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{2m}{\pi L_r} & \frac{\omega_0 \gamma \beta}{\alpha^2 + \beta^2} \\ 0 & \frac{-\omega_0 \gamma \beta}{\alpha^2 + \beta^2} \\ \frac{2}{\pi L_m} & \omega_0 I_{Lmc} \\ 0 & -\omega_0 I_{Lms} \\ 0 & \omega_0 V_{crc} \\ 0 & -\omega_0 V_{crs} \\ 0 & 0 \end{bmatrix} \quad (2.79) \\
C &= \begin{bmatrix} r \frac{R}{R+r} \frac{2}{\pi} \frac{\alpha}{\sqrt{\alpha^2 + \beta^2}} & r \frac{R}{R+r} \frac{2}{\pi} \frac{\beta}{\sqrt{\alpha^2 + \beta^2}} & 0 & 0 & 0 & 0 & \frac{R}{R+r} \\ \frac{m}{\pi} & 0 & \frac{1}{\pi} & 0 & 0 & 0 & 0 \end{bmatrix}, \quad D = 0
\end{aligned}$$

where  $\alpha = 1 - k\Omega_r^2$ ,  $\beta = \mathcal{Q}\Omega_r(\alpha + k)$ ,  $k = \frac{L_m}{L_r}$  and  $\gamma = \frac{2V_g km\Omega_r^2}{\pi R_{ac}}$ .

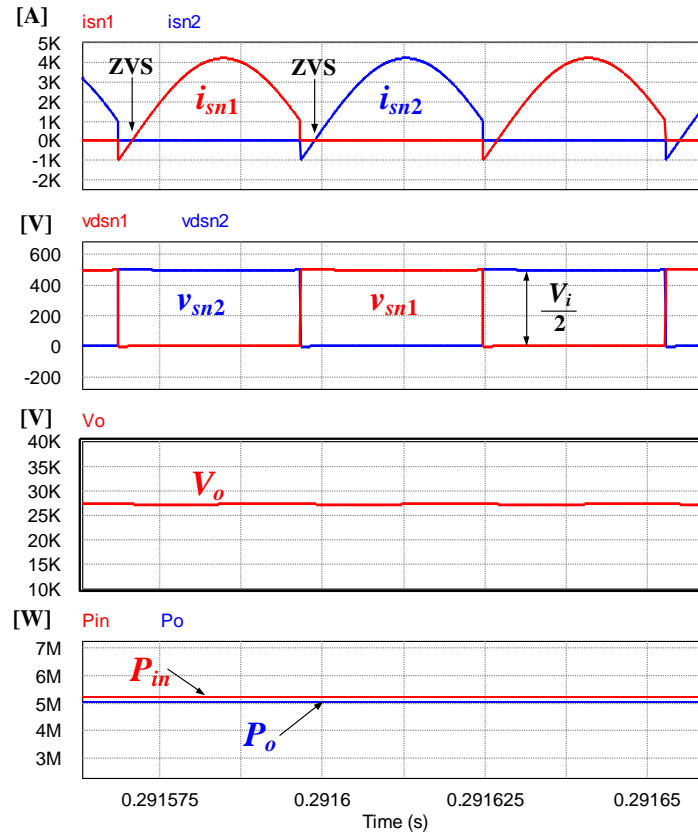
Hence, the control to output transfer function can be expressed as

$$G_{v\omega}(s) = \left. \frac{\hat{v}_o(s)}{\hat{\omega}_{sn}(s)} \right|_{\hat{v}_g(s)=0} = C(1,:)(sI - A)^{-1}B(2,:) \quad (2.80)$$

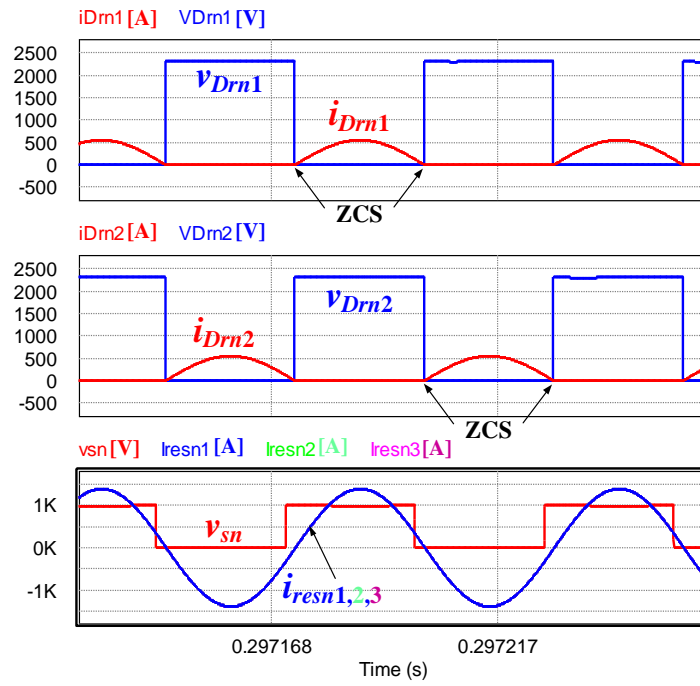
## 2.4.5 Simulation Results

To demonstrate the functionality of the proposed converter, a 5-MW wind turbine system with an output dc voltage of 28 kV was simulated in PSIM. The input voltage is selected to be 1 kV to reflect the output dc voltage of the front-end ac-dc rectifier of a wind turbine (typically between 400 V and 690 V). The simulated converter consists of four modules of the proposed circuit. SiC MOSFET half-bridge modules from Semikron (SKM500MB120SC) are used. Note that the design procedure of the proposed circuit will be given for the proof-of-concept experimental circuit, which will be discussed in section 2.4.7. Figure 2.40 shows the key

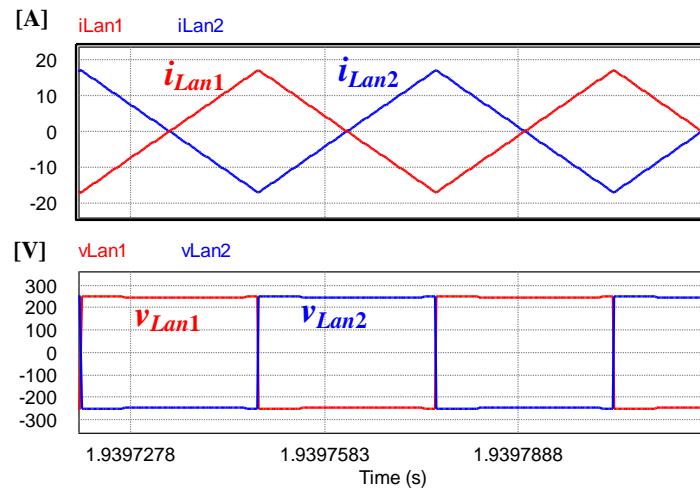
simulation results at full-load condition. As illustrated in Figure 2.40(a), ZVS turn-ON and close to ZCS turn-OFF are achieved. Figure 2.40(b) shows the switching waveforms of one module of the output voltage doubler, which demonstrates that ZCS turn-ON and turn-OFF are achieved for all the diodes. Figure 2.40(c) shows the auxiliary inductor currents; each auxiliary inductor (i.e.,  $L_{an1}$ ) is 100  $\mu\text{H}$ . The efficiency at full-load condition is 98.8%.



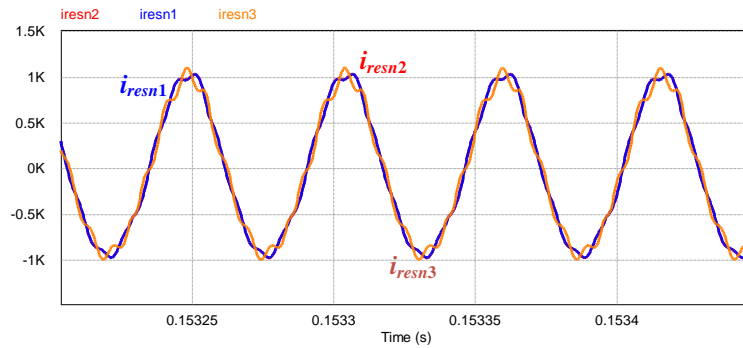
(a) switching waveforms of the switches and output voltage



(b) voltage doubler diodes waveforms



(c) auxiliary magnetism current waveforms



(d) resonant currents in one converter module

Figure 2.40– Simulation results for full-load condition

Figure 2.40(d) shows all three resonant currents within one module, where a component tolerance of 20% has been introduced to obtain the results. It shows that all the resonant currents are well-balanced within one circuit modules.

## 2.4.6 Controller Design

The control block diagram of the circuit is shown in Figure 2.32. The output of the discrete-time PI controller is fed to the voltage-controlled oscillator (VCO) to adjust the switching frequency of the MV converter, using a TMS320F28335 Delfino Microcontroller. As discussed, the small-signal model and control-to-output transfer functions of the resonant circuit and high-gain rectifier modules are obtained by employing extended describing function (EDF). The derived model is then used to design the controller.

The LPF used in the proposed controller system design is a simple first-order low-pass filter. The transfer function is given below

$$LPF(s) = \frac{1}{\frac{s}{2\pi f_c} + 1} \quad (2.81)$$

where  $f_c$  represents the cut-OFF frequency and is chosen to be relatively low to ensure that the high frequency components obtained from the error among the resonant currents are eliminated, as a higher cut-OFF frequency can potentially affect the steady-state response. To best highlight the selection of the cut-OFF frequency, the output voltage response against low-pass filter cut-OFF frequency variations (50 Hz, 100 Hz, and 150 Hz) are obtained. In this design, a cut-OFF frequency of 150Hz was selected. Figure 2.41 shows the dynamic performance of the output voltage with different cut-OFF frequencies for a step change in the load. Note that under different variations of  $f_c$ , the output voltage regulation is still functioning.

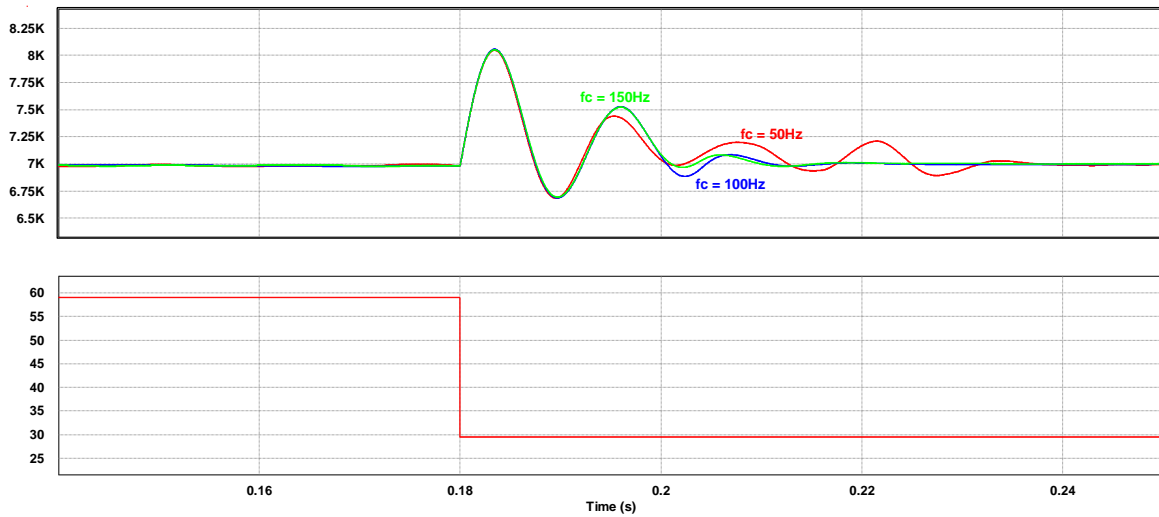


Figure 2.41– The output voltage response against low-pass filter cut-OFF frequency variations (50Hz, 100Hz, 150Hz)

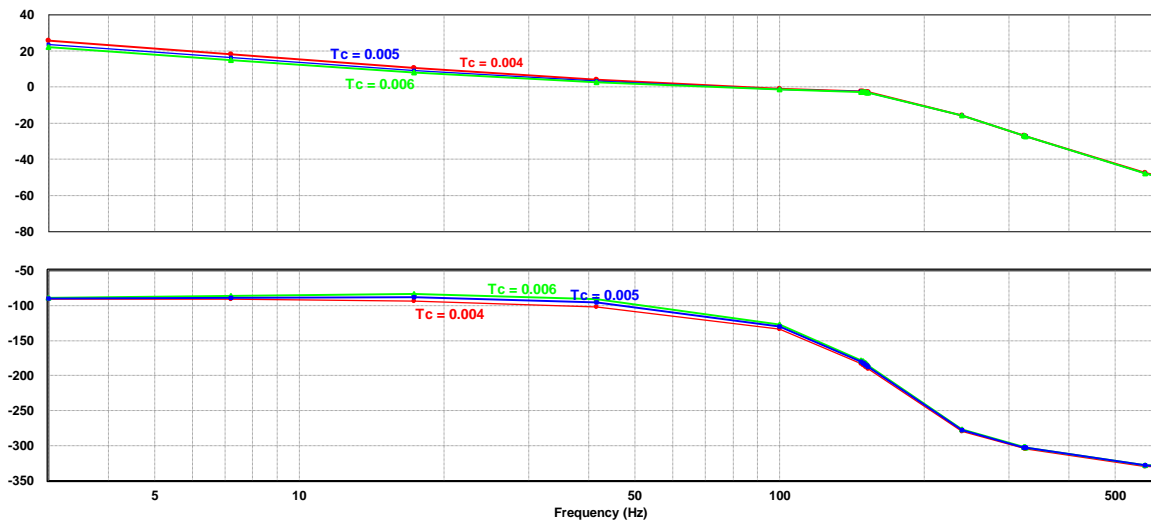
Top traces: output voltage (with different cut-OFF frequencies for LPF)

Lower trace: output load current (step change from full-load to 50% load condition)

In order to increase the low-frequency loop gain, eliminate steady-state error, and minimize the response time of the converter with the variable frequency feedback controller, a PI controller in the form of (2.82) is used.

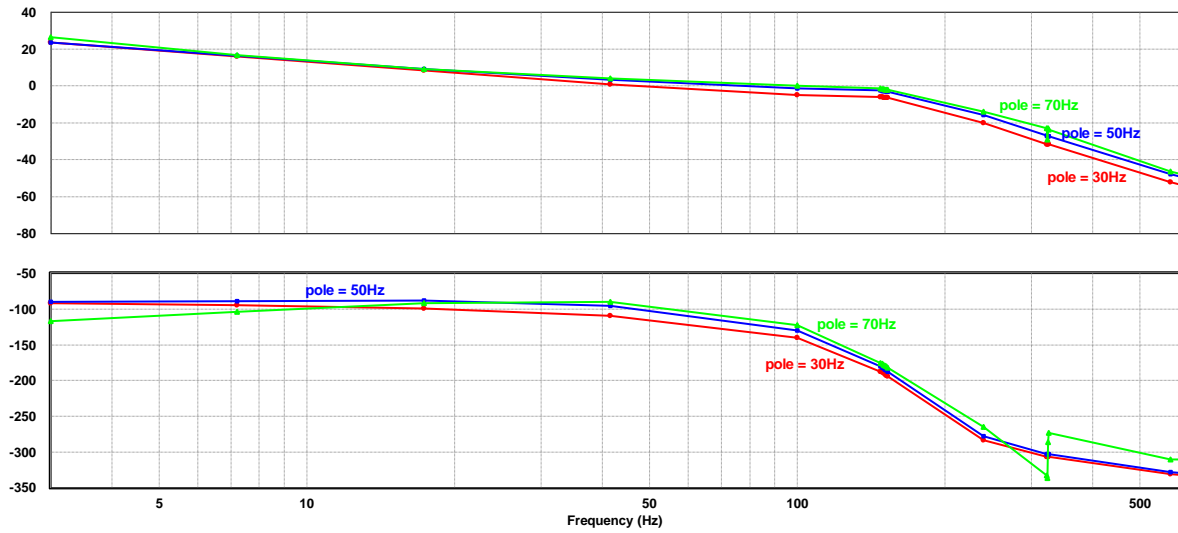
$$PI = K_c \left( \frac{1 + sT_c}{sT_c} \right) \left( \frac{1}{1 + s * pole} \right) \quad (2.82)$$

This PI compensator is the modified type II compensator, where  $T_c$  is the time constant;  $K_c$  is the gain; and  $pole$  is the second pole of the PI compensator. To highlight the performance of the PI compensator used in the proposed design, the closed-loop bode plots for various values of  $T_c$ ,  $K_c$  and  $pole$  were obtained as shown in Figure 2.42, Figure 2.43, and Figure 2.44, respectively. It can be observed that the obtained phase margins all meet the stability criteria (The phase margin values are given in each figure caption). Figure 2.45 shows the closed-loop bode plot of the design under different loading conditions. The minimum phase margin for this design is  $59.4^\circ$ .



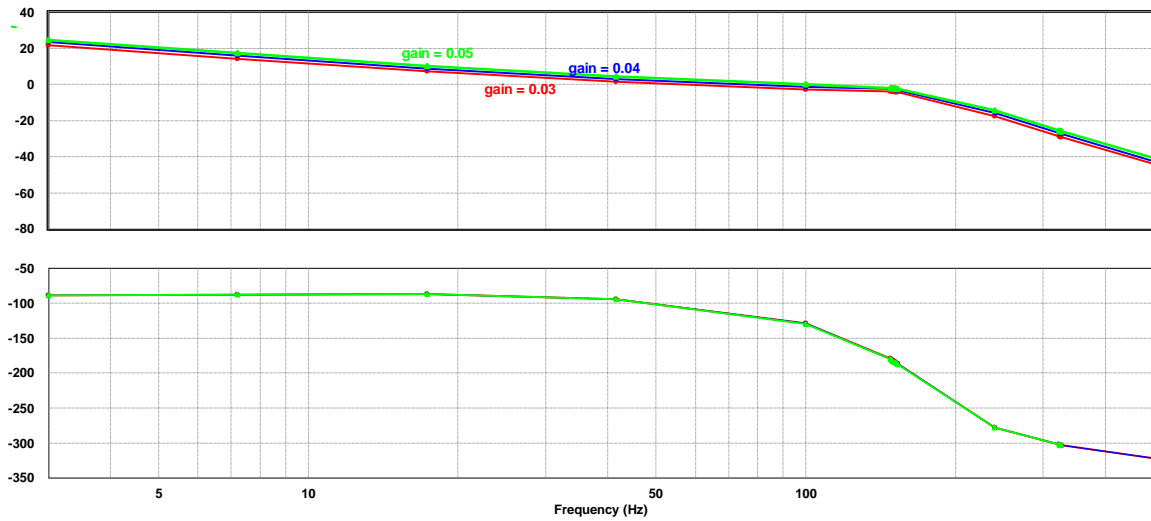
$$[(T_c = 0.004) \text{ PM} = 52^\circ, (T_c = 0.005) \text{ PM} = 59.1^\circ, (T_c = 0.006) \text{ PM} = 64.4^\circ]$$

Figure 2.42– Bode plot with various “Time constant (i.e.,  $T_c$ )” in the PI transfer function (with  $V_i = 1\text{kV}$  at full-load)



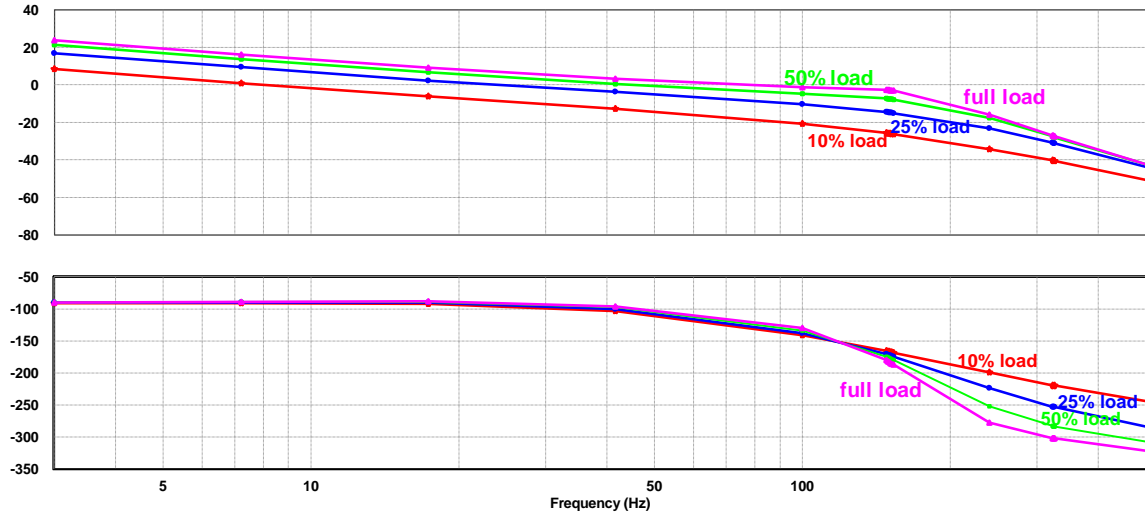
[(pole = 30Hz) PM = 67.3°, (pole = 50Hz) PM = 59.23°, (pole = 70Hz) PM = 52.8°]

Figure 2.43– Bode plot with various “pole placements” in the PI transfer function (with  $V_i = 1\text{kV}$  at full-load)



[(gain = 0.03) PM = 73.8°, ( $T_c = 0.04$ ) PM = 60.3°, ( $T_c = 0.05$ ) PM = 45.8°]

Figure 2.44– Bode plot with various “gain values (i.e.,  $K_c$ )” in the PI transfer function (with  $V_i = 1\text{kV}$  at full-load)



[(10% load) PM = 89.8°, (25% load) PM = 86.5°, (50% load) PM = 79°, (full-load) PM = 59.4°]

Figure 2.45– Closed-loop Bode plot performance with different loading (i.e., power) conditions (with  $V_i = 1\text{kV}$ )

## 2.4.7 Experimental Results and Design Procedures

To further verify the performance of the proposed step-up converter topology, a 5.6-kW, 0.3/4.8-kV proof of concept prototype was built in the laboratory. The prototype consists of two modules. The design steps of the converter's circuit components are given in the following.

- 1) The equivalent output ac resistance can first be obtained as shown in the following equation:

$$R_{ac} = \frac{2}{3\pi^2} \frac{V_o^2}{P_o} = \frac{2}{3\pi^2} \frac{V_o^2}{P_o} = 139\Omega \quad (2.83)$$

- 2) The switching frequency is assumed to be around 17.5 kHz. To achieve a voltage gain of eight for each module, according to Figure 2.28 and Figure 2.29,  $k$  and  $Q$  are chosen to be

0.5 and 4, respectively. With respect to the duty ratio  $D_n$ , the maximum voltage gain occurs at  $D_n=0.5$ . Hence according to (2.38),  $\omega_r$  is calculated to be 0.84.  $L_{sn}$  is then calculated accordingly from (2.85)

$$\omega_0 = \frac{2\pi f_{sw}}{\omega_r} = 1.3 \times 10^5 \text{ rad / sec} \quad (2.84)$$

$$L_{sn} = \frac{R_{ac}}{Q\omega_0} = 267 \mu H \quad (2.85)$$

- 3)  $L_{sn}$  is selected to be 305uH. With  $k = 0.5$ ,  $L_{mn}$  is then equal to 610μH with a turns-ratio of 1:1,  $C_s$  is then obtained as shown in the following equation:

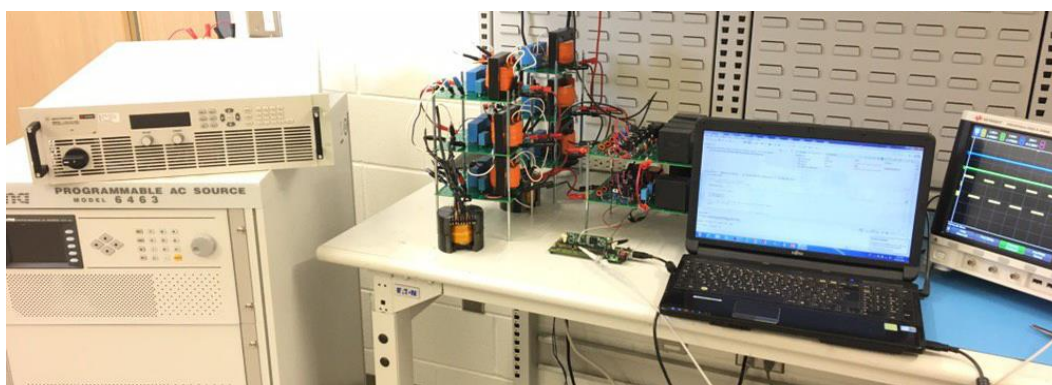
$$C_s = \frac{1}{(2\pi f_0)^2 L_{sn}} = 195 \text{ nF} \quad (2.86)$$

A list of the final circuit parameters of the prototype and the simulation are summarized in Table 2.3. In the proof-of-concept experimental prototype, SiC MOSFETs of model number: SCT3030AL from ROHM Semiconductor and SiC Schottky fast recovery diodes from STMicroelectronics are used. A picture of the experimental prototype is shown in Figure 2.46. The key waveforms per module obtained from the prototype under full-load condition are shown in Figure 2.47. As illustrated in Figure 2.47(a) and (b), ZVS turn-ON and ZCS turn-OFF are achieved for all the switches. Figure 2.47(c) shows the voltage doubler diode's waveforms. It can be observed that ZCS condition is achieved. Figure 2.47(d) shows all the resonant currents and the inverter output voltage in one module, illustrating that all the resonant currents are completely balanced. The output voltage per module is shown in Figure 2.47(e). This plot also

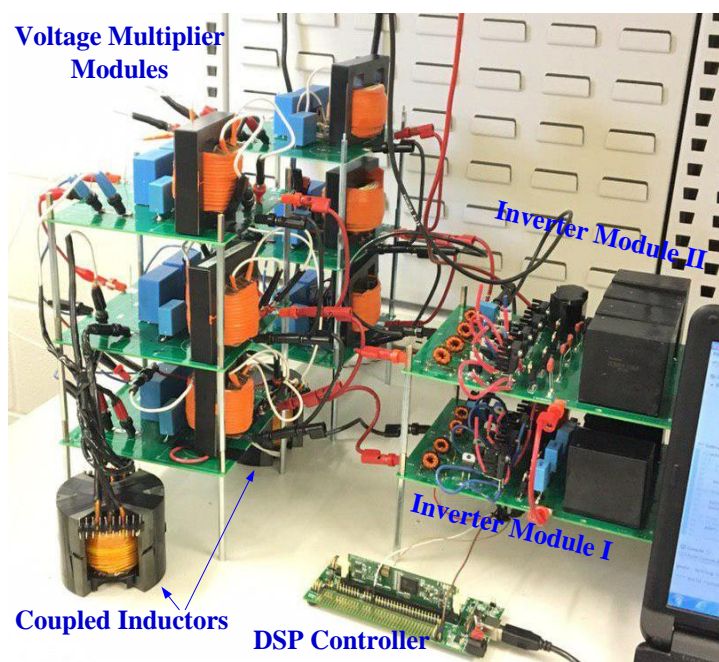
shows that the measured efficiency is 99.3% for module 1. Also, the measured efficiency for module 2 at full-load condition is 99.1%.

Table 2.3– Circuit Components (Per Module) in Simulation and the Experimental Prototype

Specifications		
	Simulation	Prototype
Rated Power	5MW	5.6kW
Rectified dc Input Voltage $V_i$	1kV <sub>DC</sub>	300V <sub>DC</sub>
Output Medium Voltage $V_o$	28kV <sub>DC</sub>	4.8kV <sub>DC</sub>
Number of Modules $n$	4	2
Per Converter Module Output Voltage $V_{on}$	7kV <sub>DC</sub>	2.4kV <sub>DC</sub>
Circuit Components per Module		
	Simulation	Prototype
SiC MOSFETs $S_{n1} \sim S_{n4}$	SKM500MB120SC, SEMIKRON 1200V, 541A (three in parallel)	SiC SCT3030AL (650V, 70A)
Snubber Capacitors $C_{sn1} \sim C_{sn4}$	MKP385362125JFM2B0 0.062μF, 1.25kV <sub>DC</sub>	0.039μF, 300V
Input Capacitors $C_{an1} \sim C_{an4}$	947D591K132DJRSN 590μF, 1.3kV <sub>DC</sub>	EZP-E50107MTA (100μF, 500V)
Resonant Capacitors $C_{resn1} \sim C_{resn3}$	B25835K2224K27 (TDK) 0.22μF, 3.7kV <sub>AC</sub>	200nF, 1kV
High Frequency Coupled Magnetics $L_{mn1} \sim L_{mn3}$	600μH (1:1)	610μH (1:1), 22mΩ
Coupled Inductor $L_{sn1} \sim L_{sn3}$	300μH (1:1)	305μH (1:1), 36mΩ N87, Ferrite Core, PM 87/70 (TDK)
SiC High Frequency Rectifier Diodes $D_{rn1} \sim D_{rn6}$	MSC030SDA120B SiC Schottky Diode (1.2kV, 65A)	SiC STPSC15H12D (1.2kV, 15A)
Output Capacitors $C_{rn1} \sim C_{rn6}$	B25856K2405K3 (4μF, 4kV <sub>DC</sub> )	B32774D4106K, (1μF, 1.3 kV <sub>DC</sub> )

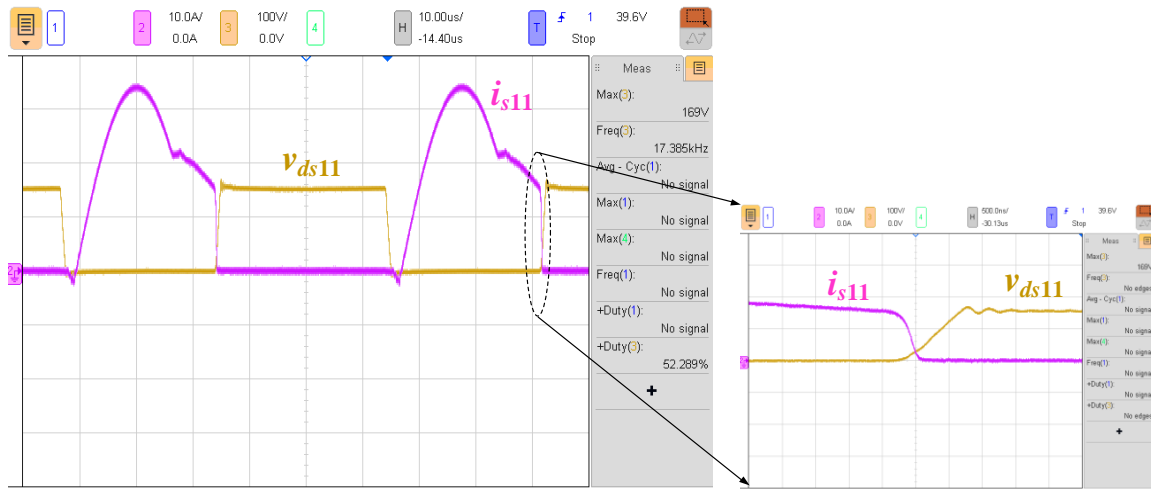


(a)



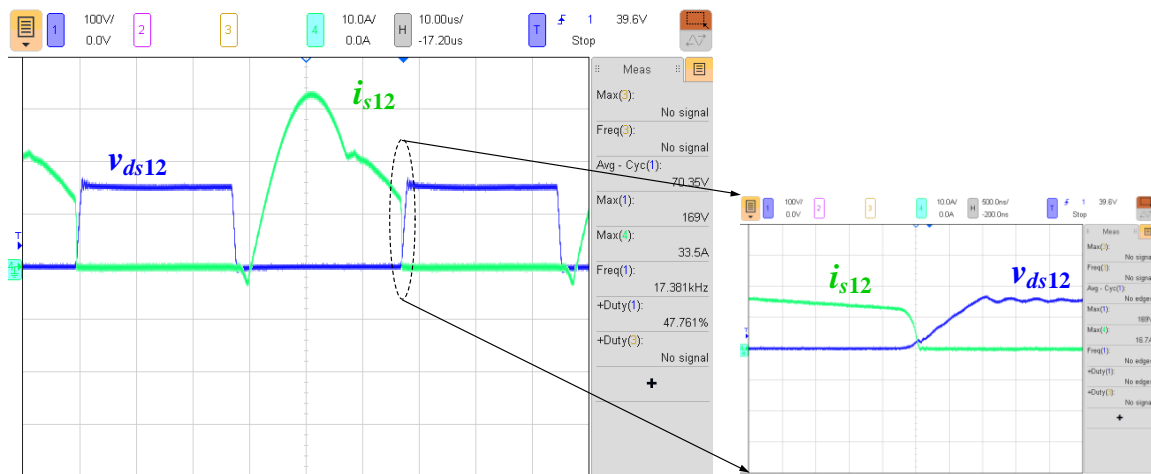
(b)

Figure 2.46– (a) Experimental platform (b) prototype picture



(a)

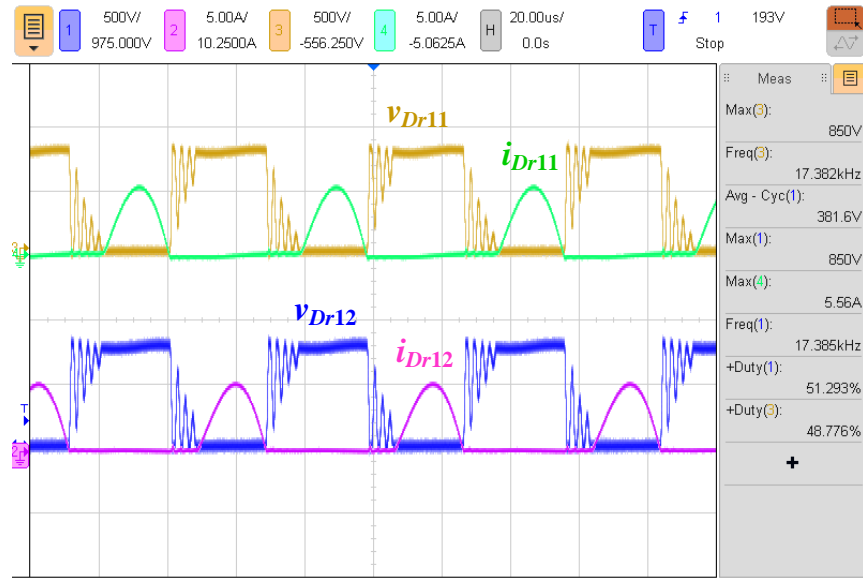
(a')

(a) [ $v_{ds11}$ : 100V/div;  $i_{s11}$ : 10A/div; time: 10 $\mu$ s/div](a') [ $v_{ds11}$ : 100V/div;  $i_{s11}$ : 10A/div; time: 500ns/div]

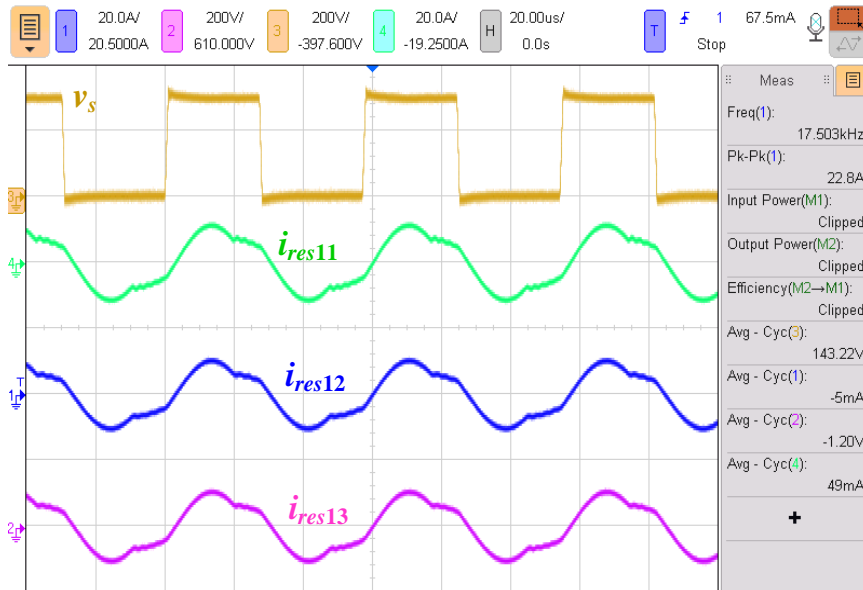
(b)

(b')

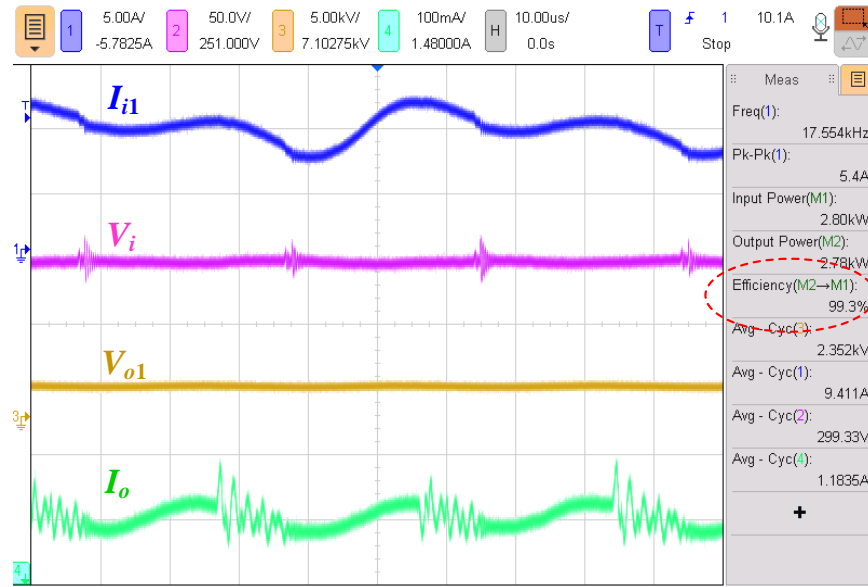
(b) [ $v_{ds12}$ : 100V/div;  $i_{s12}$ : 10A/div; time: 10 $\mu$ s/div](b') [ $v_{ds12}$ : 100V/div;  $i_{s12}$ : 10A/div; time: 500ns/div]



(c) [ $i_{Dr11}$ ,  $i_{Dr12}$ : 5A/div;  $v_{Dr11}$ ,  $v_{Dr12}$ : 500V/div; time: 20 $\mu$ s/div]



(d) [ $i_{res11}$ ,  $i_{res12}$ ,  $i_{res13}$ : 20A/div,  $v_s$ : 200V/div; time: 20 $\mu$ s/div]



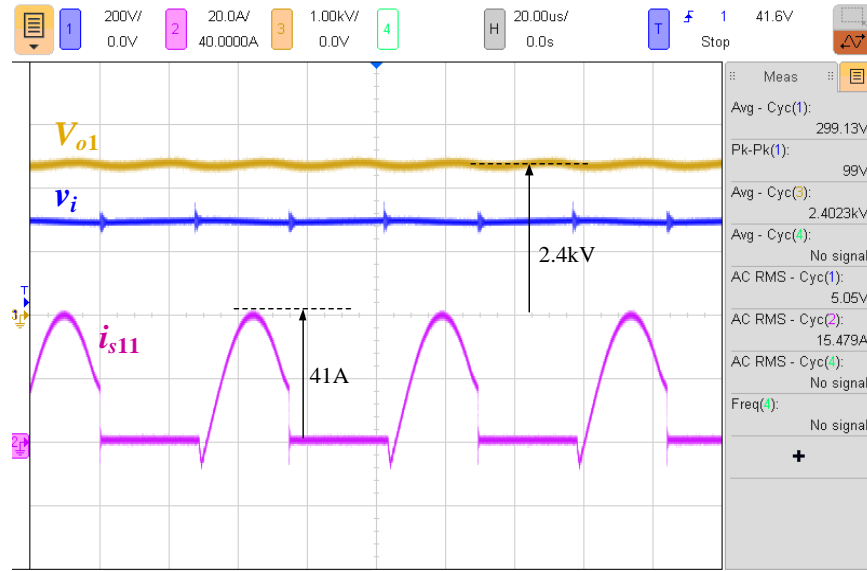
(e) [ $I_{i1}$ : 5A/div;  $I_o$ : 0.1A/div;  $V_i$ : 50V/div;  $V_{o1}$ : 5kV/div; time: 10 $\mu$ s/div]

Figure 2.47– Experimental waveforms at rated power condition with 99.3% measured efficiency per module

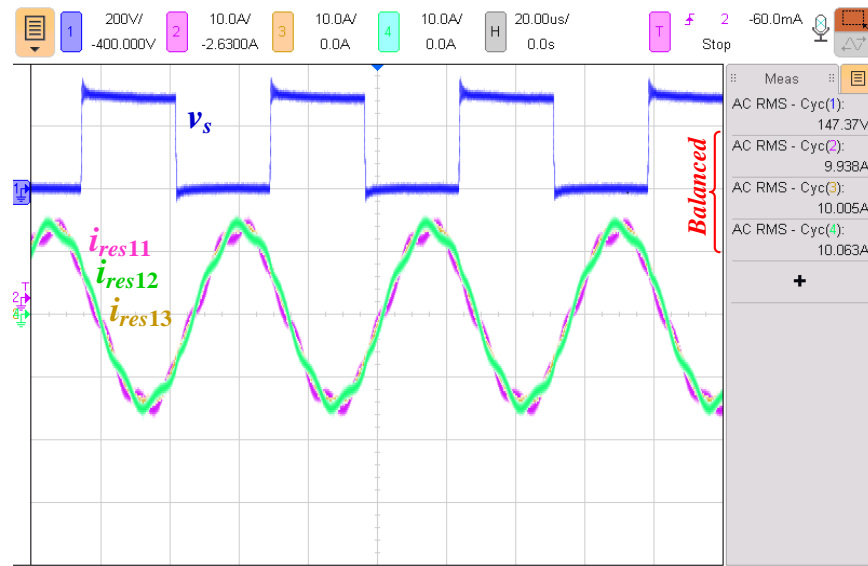
Figure 2.48 and Figure 2.49 show the performance of the proposed converter when the  $CLL$  parameters change by 20% rated value. Results verify the performance of the proposed converter with completely balanced current and voltage sharing. The balancing voltage across the switches can verify the balanced voltage across the dc-link capacitors and snubber capacitors. It can be also observed from all operating conditions of the simulation and experimental results that stress of voltage across each switch is half of the DC-link voltage ( $V_i/2$ ).

Figure 2.50 illustrates the balanced voltage across the capacitors in the switch network at full-load condition. In regard to the output capacitors voltage sharing, it can be observed from Figure 2.51 that using coupled inductor can significantly reduce the unbalanced voltage degree without any additional components and control efforts. The figure shows the voltages across the

output capacitors ( $v_{Cr1n}$  and  $v_{Cr2n}$ ) are almost identical. Figure 2.52 and Figure 2.53 show the performance of the proposed converter with the step changes in the load and input voltage, respectively. As can be seen, the variable frequency control circuit can maintain the output voltage at 2.4kV. Finally, Figure 2.54 shows the efficiency of the experimental prototype and simulation results.

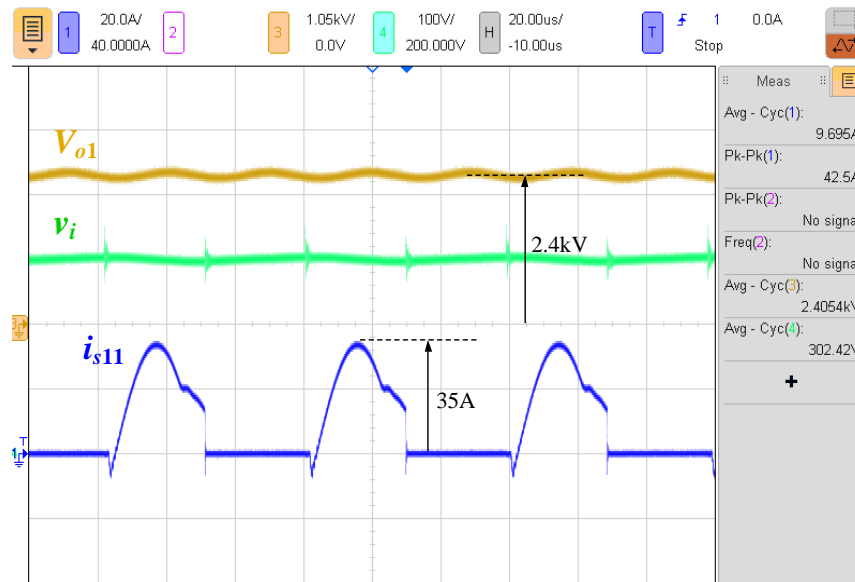


(a) [ $V_{o1}$ : 1kV/div,  $v_i$ : 200V/div,  $i_{s11}$ : 20A/div; time: 20 $\mu$ s/div]

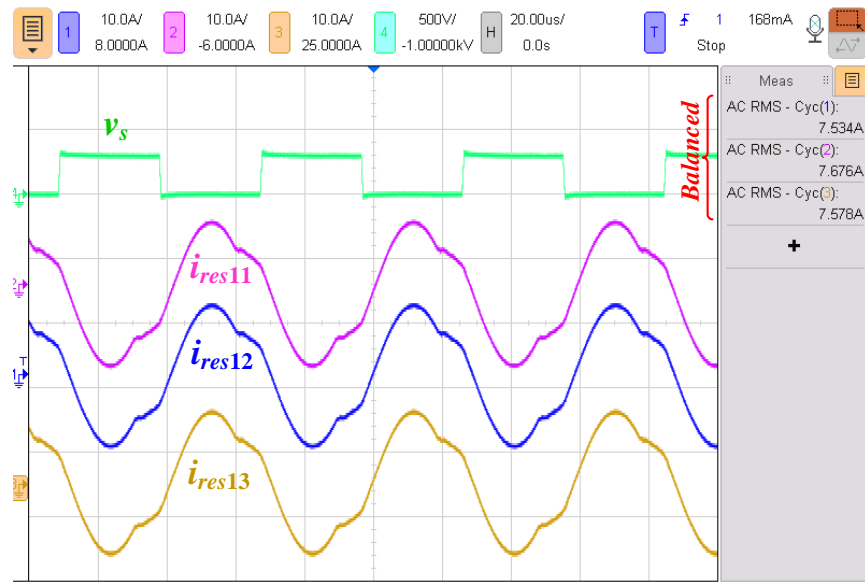


(b) [ $i_{res11}, i_{res12}, i_{res13}$ : 10A/div,  $v_s$ : 200V/div; time: 20 $\mu$ s/div]

Figure 2.48– Experimental waveforms at 20% reduction in the coupled inductance ( $L_{sn}$ ) (per module)

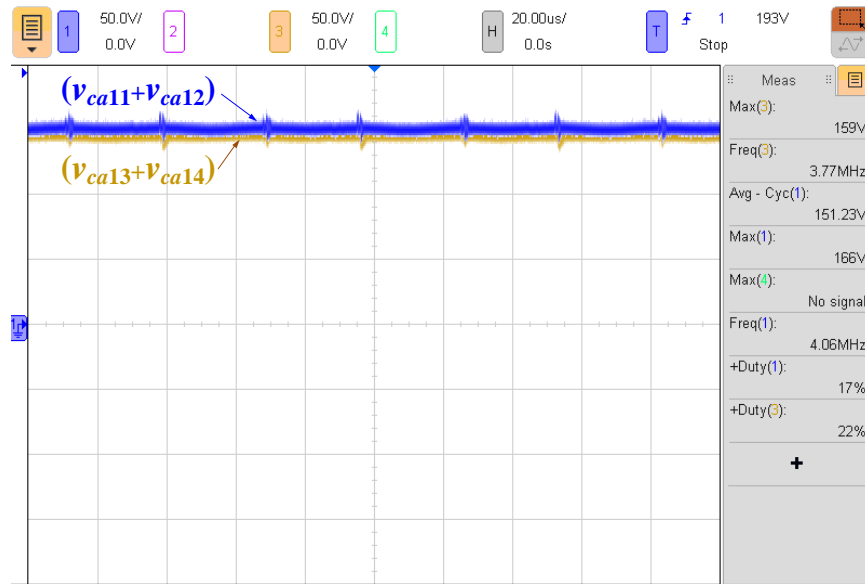


(a) [ $V_{o1}$ : 1kV/div,  $v_i$ : 200V/div,  $i_{s11}$ : 20A/div; time: 20 $\mu$ s/div]

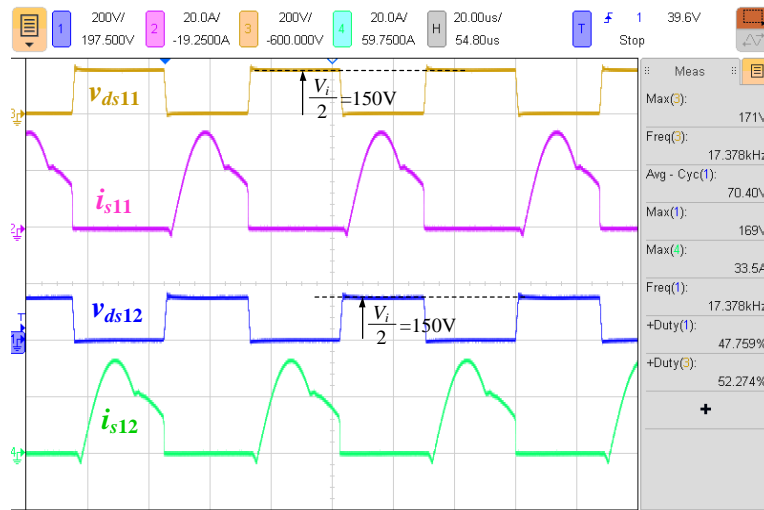


(b) [ $i_{res11}, i_{res12}, i_{res13}$ : 10A/div,  $v_s$ : 500V/div; time: 20 $\mu$ s/div]

Figure 2.49– Experimental waveforms at 20% increase in the resonant capacitance ( $C_{resn}$ ) (per module)

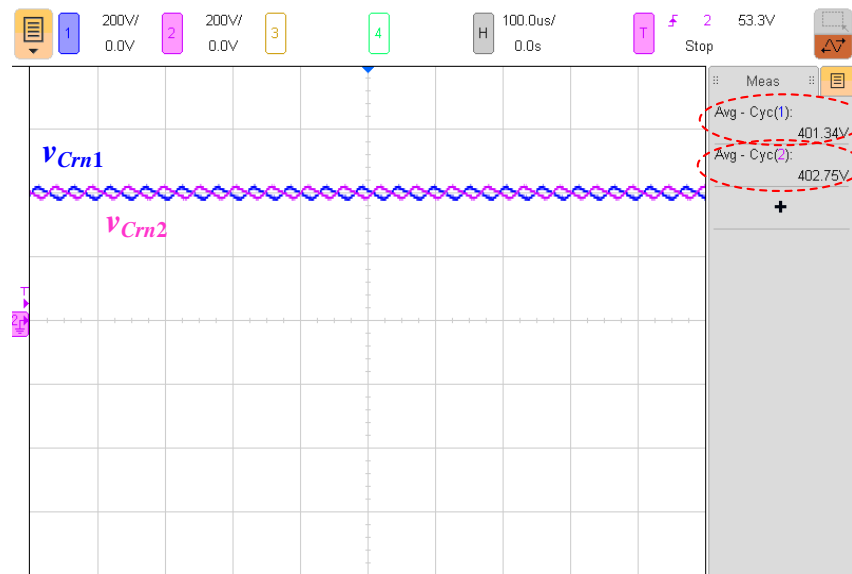


(a) [ $(v_{ca11} + v_{ca12})$ : 50V/div,  $(v_{ca13} + v_{ca14})$ : 50V/div; time: 20 $\mu$ s/div]



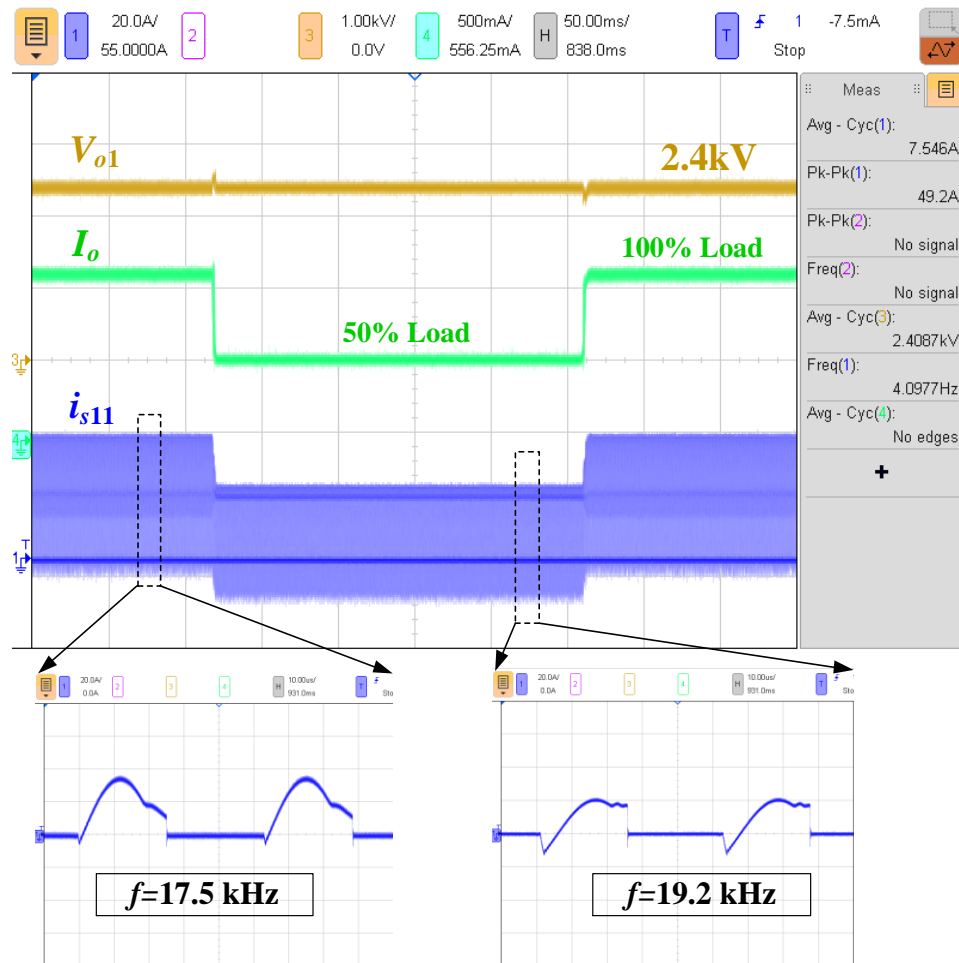
(b) [ $v_{ds11}, v_{ds12}$ : 200V/div,  $i_{s11}, i_{s12}$ : 20A/div; time: 20 $\mu$ s/div]

Figure 2.50– Balanced voltage across the capacitors in the switch network at full-load condition; (a) across the dc-link capacitors; (b) across snubber capacitors



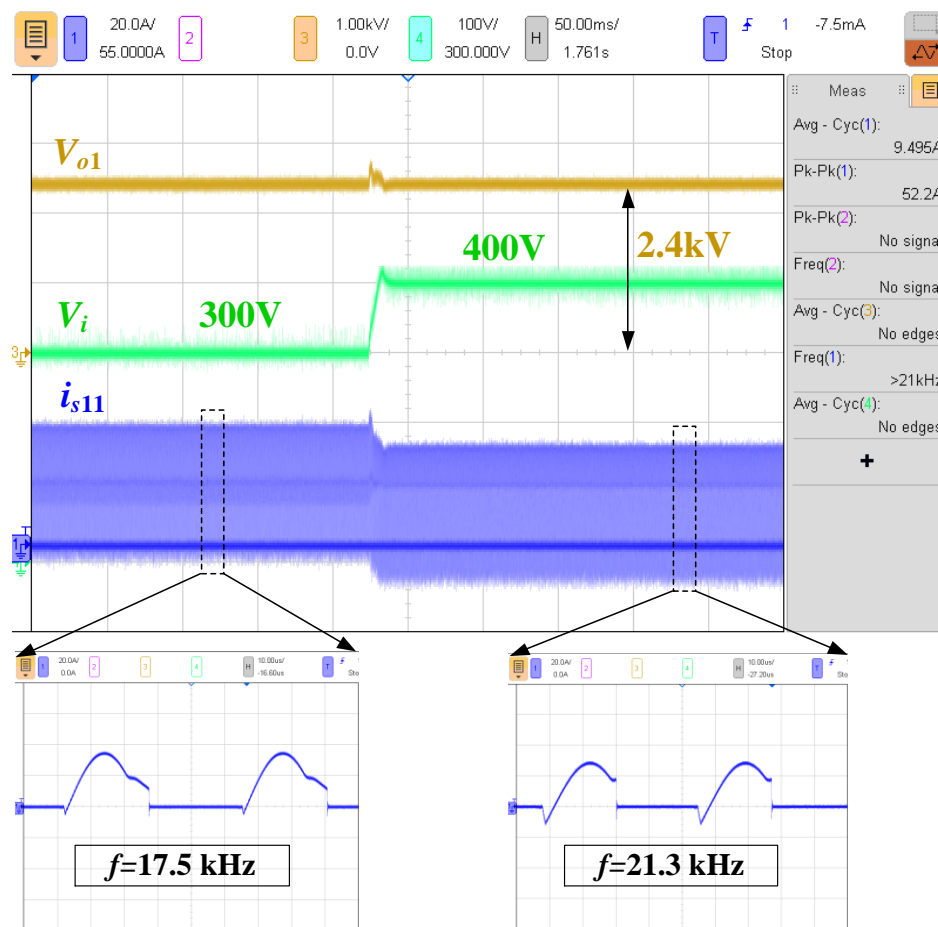
[ $v_{cr1n}$ : 200V/div,  $v_{cr2n}$ : 200V/div; time: 100 $\mu$ s/div]

Figure 2.51– Balanced voltage across the output capacitors



[ $V_{o1}$ : 1kV/div,  $I_o$ : 500mA/div,  $i_{s11}$ : 20A/div; time: 50ms/div]

Figure 2.52– Dynamic response with the step change in the load



[ $V_{o1}$ : 1kV/div,  $V_i$ : 100V/div,  $i_{s11}$ : 20A/div; time: 50ms/div]

Figure 2.53– Dynamic response with the step the input voltage

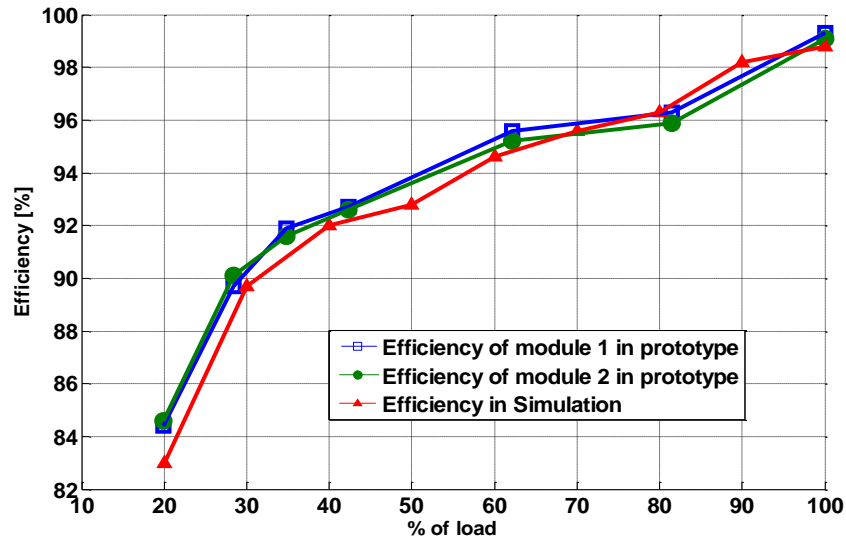


Figure 2.54 – Measured efficiency of the experimental prototype and simulation results for different power level

## 2.5 Chapter Summary

This chapter describes the proposed solution in MV dc-dc step-up converters in wind energy applications. In the first two sections of this chapter, a novel high-gain converter based on modular resonant converters is proposed. The semiconductor devices can obtain soft switching with a reduced voltage stress (half of the dc-link voltage). However, since the proposed converter only relies on the resonant circuits to step-up the voltage, it suffers the drawback of having a highly sensitive frequency control to regulate the output voltage. To address this problem, a new class of SiC-MOSFETs based, soft-switched modular step-up dc-dc resonant converter, utilizing magnetically coupled high-gain output rectifier modules, has been presented. In addition, a simple coupled auxiliary circuit that employs only passive circuit components has also been added to each of the proposed converter modules to extend ZVS turn-ON for all switches over a wide range of operating conditions. The output voltage was regulated via variable frequency

control, whereas all the resonant currents within one converter module were balanced with duty ratio control.

To verify the performance of the proposed modular converter configuration, simulation results have been provided on a 5-MW wind turbine system with an output voltage of 28 kV. Results demonstrated that soft-switching operation is guaranteed for all the active devices in the converter circuit with an overall efficiency of 98.8% obtained at full-load condition. The stability and robustness of the control loop have also been verified. Finally, experimental results on a SiC-implemented modular 0.3/4.8 kV, 5.6 kW proof-of-concept prototype have been given to further verify the theoretical concept and to highlight the features of the proposed circuit. The final results confirmed that an efficiency of at least 99% is obtained for each module in the hardware prototype at full-load condition. The dynamic performance of the converter prototype has also been given to highlight the effectiveness of the control scheme, as well as the soft-switching operation for different loading conditions.

## **Chapter 3    Proposed DC-DC Converters with Single Isolation Magnetic and Coupled High-Gain Rectifiers**

In Chapter 2, several step-up transformerless dc-dc soft-switched converter topologies based on a high-gain output rectifier approach were presented for MVdc applications. The proposed approach did not require high turns-ratio high frequency step-up transformers, and was able to achieve soft-switching conditions for all the switching devices. With respect to MV converter design, modular circuit configuration is commonly used. Since the resonant circuit and the high-gain rectifier module in each of the presented converter modules were inter-connected via a high frequency transformer, multiple unity turns-ratio transformers were then required in the presented modular design approach.

In an effort to further reduce the size and cost of the magnetic components used in the devised converter configurations presented in Chapter 2, two different types of MV dc-dc converter modules, where each will utilize only a single magnetic structure with magnetically coupled high-gain rectifiers, are presented in this chapter. Section 3.1 presents the first topology, where a step-up resonant circuit module is connected to a doubly coupled-voltage-quadrupler via

a 1:1:1 three-winding transformer for MVdc conversion. Since the coupled voltage-quadruplers are able to achieve step-up voltage conversion, high turns-ratio step-up high frequency transformers are not required in the proposed design, while at the same time, the output voltage of each voltage-quadrupler can be well-balanced without using complicated controller, due to the use of the three-winding transformer. All the primary side switches in the proposed converter are still able to achieve ZVS turn-ON and ZCS turn-OFF.

The second topology is presented in section 3.2. To fully capture the power from all the multistring inverter side switching circuits, a new step-up dc-dc converter module that utilizes three resonant sub-module circuits interconnecting with unity turns-ratio multiphase transformer and a doubly coupled voltage doubler modules is presented in section 3.2. In each topology presented in this chapter (section 3.1 and 3.2), a single magnetic core component is used to transfer all the power from the multistring inverter side to the output high frequency high-gain rectifiers. The detailed descriptions of each circuit's operating principles and its characteristics are presented in this chapter. The performance of both dc-dc topologies are verified through simulation results and experimental works on proof-of-concept prototypes.

### **3.1 Step-Up Converter Module Configuration with 1:1:1 Transformer**

Magnetics are often the bulkiest components in the layout [75]. One way to decrease the volume and weight of the magnetics is to increase the switching frequency of the converter, as the size of the magnetic components is inversely proportional to the switching frequency. It was discussed

in previous chapter that increasing the switching frequency leads to an increase in switching losses, which in turn reduces the converter efficiency. Hence, resonant converters, as the most promising soft-switching techniques, were employed in the proposed dc-dc converters to reduce the switching losses and electromagnetic interference (EMI).

### 3.1.1 Circuit Description of the Proposed Converter

The general block diagram of the first proposed dc-dc step-up converter configuration that utilizes only a single magnetic component, linking the resonant circuit module and the coupled high-gain rectifier modules, is shown in Figure 3.1. The proposed converter configuration consists of dc-link capacitors, a switch network, a *CLL* resonant circuit connected to coupled high-gain rectifiers (HGRs) through a three-winding transformer. To maximize the voltage gain of the converter, two voltage-quadruplers are used for the high-gain rectifying stages. The switch network comprises multistring connection of switches to reduce the voltage stress across the switches to half of the dc-link voltage. This circuit consists of four switches,  $S_{11}$ ,  $S_{21}$ ,  $S_{31}$  and  $S_{41}$  which are controlled by two compensating gating signals. Switches ( $S_{11}$ ,  $S_{41}$ ) and switches ( $S_{21}$ ,  $S_{31}$ ) operate in complementary fashion, with switches ( $S_{11}$ ,  $S_{41}$ ) turned ON during the interval  $DT_s$ , and switches ( $S_{21}$ ,  $S_{31}$ ) turned ON during the interval  $(1-D)T_s$ . The isolated *CLL* resonant circuit consists of a resonant capacitor ( $C_{r11}$ ), a coupled inductor ( $L_{c11}$ ) which has been isolated by a unity turns-ratio three-winding transformer ( $T_{11}$ ) with the magnetizing inductance of  $L_{m11}$ . The converter incorporates transformer nonidealities (i.e., leakage and magnetizing inductances) into the basic operation of the *CLL* resonant circuit. The proposed circuit also benefits from implementing a dc-blocking capacitor (i.e., resonant capacitor  $C_{r11}$ ) in series with the primary

winding of the HF transformer to avoid core saturation. ZVS turn-ON can be achieved for all the switches by the energy stored in the magnetizing and coupled inductors which flows through the switches antiparallel diodes. Near ZCS turn-OFF can also be obtained by discharging the snubber capacitors ( $C_{s11} \sim C_{s41}$ ) across each switch prior to the rising edge of the gate signal. The proposed circuit can maintain ZVS over a wide range of operating points while minimizing the conduction-loss penalty. By employing a *CLL* resonant circuit, the proposed topology takes on the inherent characteristics of a series resonant converter at full-load, introducing less circulating current. And as the load decreases further, the converter exploits the characteristics of the parallel resonant converter to maintain ZVS for a wider range of operating points. Analysis of the converter will be presented and validated with experimental results.

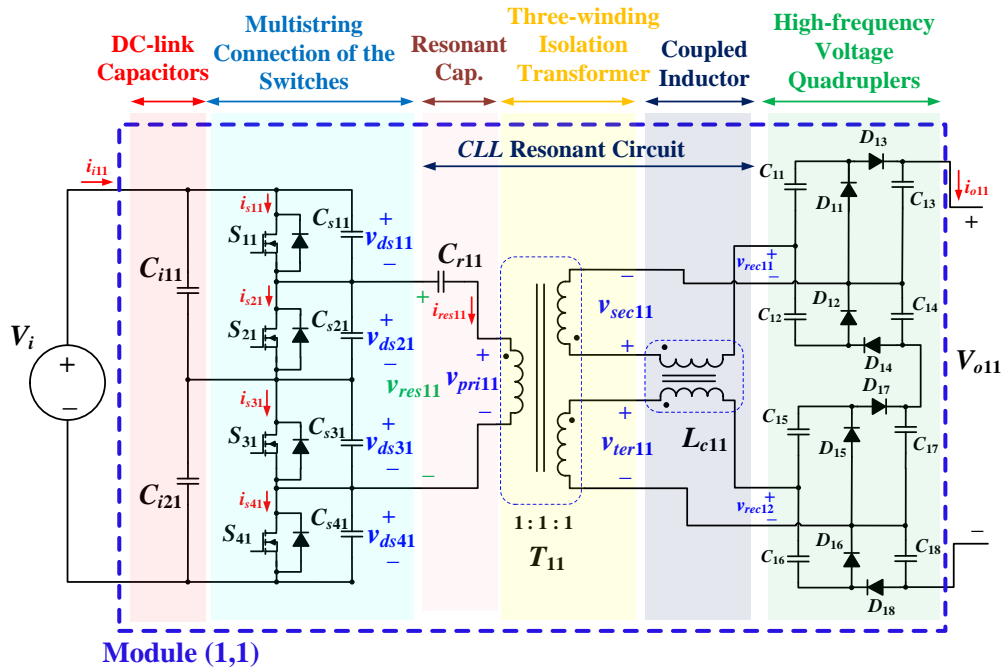


Figure 3.1– Proposed MV coupled-voltage-quadruplers based step-up converter with 1:1:1 Transformer

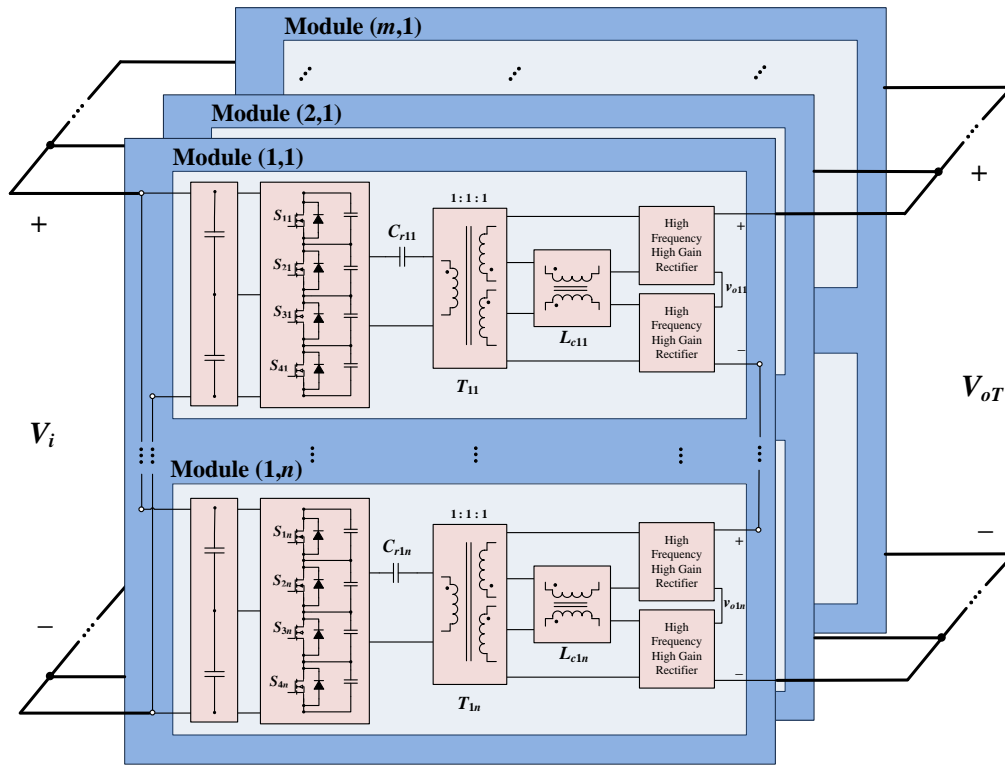


Figure 3.2– Modular structure of the proposed converter

The proposed converter utilizes coupled inductors at the input of the high frequency rectifying stages to form a current-fed high-gain rectifier. The current-driven structure of the high-gain rectifiers guarantees smooth performance of the diodes. Hence, the diode reverse recovery losses are eliminated. By magnetically-integrating the voltage-quadruplers in the output rectifying stage, the output dc voltage balancing of the two voltage multiplier modules can be achieved much easier without using a complicated balancing control scheme. Moreover, the number of required magnetic components can be reduced, compared to the individual module approach with separate components. In the proposed circuit, full-bridge voltage-quadrupler rectifiers are employed at the output stage of the converter. The main advantages of this full-wave voltage multiplier rectifier (VMR) over the half-wave VMR is the reduced voltage stress

on output capacitors (half of the output voltage) with a balanced voltage stress on output capacitors and diodes [40].

The modular structure of the proposed converter is shown in Figure 3.2. The proposed topology utilizes a combination of input-parallel-output-parallel (IPOP) and input-parallel-output-series (IPOS) systems. According to [76], input parallel systems are superior to input series systems. Assuming that the converter modules have identical topology and specifications, for IPOP and IPOS systems, the modules are connected in parallel at the input side, and the input voltages of the modules are thus equal. Therefore, we need to make the module output currents equal for IPOP systems, and the output module voltages equal for IPOS systems. This means that output current sharing (OCS) and output voltage sharing (OVS) should be ensured for IPOP and IPOS systems, respectively. For input-series-output-parallel (ISOP) and input-series-output-series (ISOS) systems, since the modules are connected in series at the input side, we not only have to ensure OCS and OVS for ISOP and ISOS systems, respectively, but also input voltage sharing (IVS) for both ISOP and ISOS systems. In other words, both IVS and OCS are needed for ISOP systems, and both IVS and OVS are needed for ISOS systems. In practice, as the topologies of the modules are identical, the mismatches in the power stages, such as the power devices, transformers, inductors, and capacitors, are not so large, so that the difference among the module efficiencies is negligible. Thus, the module output currents or the module output voltages will be almost evenly shared for IPOP and IPOS systems, respectively. In other words, achieving input current sharing (ICS) implies OCS for IPOP systems and OVS for IPOS systems. The sharing of voltages and currents for different dc-dc modular systems are shown in

Table 3.1 [76]. Hence, in the proposed modular topology with IPOP/IPOS structure, input current control can guarantee a balanced voltage and current sharing, and consequently a balanced power sharing for the entire system.

Table 3.1– Voltage and Current Sharing of Different DC-DC Modular Systems

	IPOP	IPOS	ISOP	ISOS
Input Voltage Sharing (IVS)	Equal by connection	Equal by connection	Required	Required
Input Current Sharing (ICS)	Required	Required	Equal by connection	Equal by connection
Output Voltage Sharing (OVS)	Equal by connection	ICS implies OVS	Equal by connection	Required
Output Current Sharing (OCS)	ICS implies OCS	Equal by connection	Required	Equal by connection

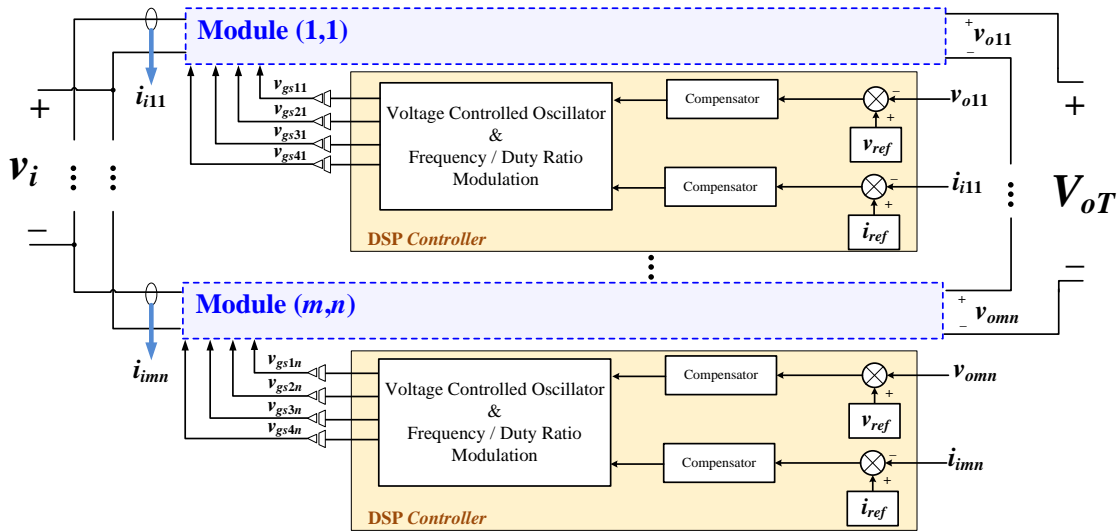


Figure 3.3– Modular control scheme for the proposed converter

In the proposed converter there are two sets of control parameters, switching frequency and duty ratio. In this work variable frequency control is selected to regulate the output voltage and duty ratio can provide a current control through asymmetrical pulse-width modulation (APWM) to ensure balanced currents at the input of each module. The block diagram of the control scheme is shown in Figure 3.3.

### 3.1.2 Operating Principles of the Proposed Step-up Converter

The operating principles of the proposed converter can be analyzed according to the operating waveforms shown in Figure 3.4, where  $D$  represents the duty cycle of  $S_{11}$  and  $S_{41}$ , with  $S_{21}$  and  $S_{31}$  operate with a duty ratio of  $(1-D)$ ; and  $T_s$  is the switching period. The key operating stages of the proposed circuit within a switching cycle are analyzed as shown in Figure 3.5, with the red arrows indicating the flow of the currents.

**$[t_0 < t < t_1]$ :** Prior to this interval  $C_{s11}$  and  $C_{s21}$ , have been discharged to the resonant circuit and the voltage across these capacitors have reached zero. At the beginning of this stage  $t_0$ , the gate signals are applied to  $S_{11}$ ,  $S_{41}$ . Due to the negative portion of the resonant current  $i_{res11}$ , currents  $i_{s11}$  (and  $i_{s41}$ ) are negative. Hence, the antiparallel diodes of  $S_{11}$  and  $S_{41}$  are turned ON. Meanwhile, the voltage across  $S_{21}$  and  $S_{31}$  are clamped to dc-link capacitor ( $C_{i11}$ ,  $C_{i21}$ ) voltages, which are half of the input voltage ( $V_i/2$ ).

**$[t_1 < t < t_2]$ :** At  $t_1$ ,  $i_{res11}$  becomes positive and the negative current flowing through antiparallel diodes of  $S_{11}$  and  $S_{41}$  in the previous stage, now become positive; so  $S_{11}$  and  $S_{41}$  are turned ON under zero voltage conditions. This implies zero turn-ON losses for  $S_{11}$  and  $S_{41}$ .

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**$[t_2 < t < t_3]$ :** At the beginning of this interval all the switches are OFF.  $C_{s11}$  and  $C_{s41}$  are already discharged into the resonant circuit. This allows using comparatively large snubber capacitors. As a result, voltage across  $S_{11}$  and  $S_{41}$  begin to rise slowly and near ZCS turn-OFF is achieved for  $S_{11}$  and  $S_{41}$  at  $t_2$ .

**$[t_3 < t < t_4]$ :** at  $t_4$ , the gate signals are applied to  $S_{21}$  and  $S_{31}$ , and the positive  $i_{res11}$  flows through the antiparallel diodes of  $S_{21}$  and  $S_{31}$ . The voltage across  $S_{11}$  and  $S_{41}$  remain at  $V_i/2$ . At the same time, the output voltages of the resonant circuits reverse their polarities.

**$[t_4 < t < t_5]$ :** at  $t_4$ , the positive  $i_{res11}$  in the previous stage become negative, the antiparallel diodes of  $S_{21}$  and  $S_{31}$  stop conducting.  $S_{21}$ ,  $S_{31}$  are then turned ON under ZVS.

**$[t_5 < t < t_6]$ :** at  $t_5$ , the gating signal of  $S_{21}$  and  $S_{31}$  ( $v_{gs21}$  and  $v_{gs31}$ ) are removed and  $C_{s21}$  and  $C_{s31}$  start to charge. This allows the voltage across  $S_{21}$  and  $S_{31}$  to rise slowly, allowing close to ZCS turn-OFF transition to be achieved for  $S_{21}$  and  $S_{31}$ . Due to the negative resonant current ( $i_{res11}$ ), the snubber capacitors and  $C_{s11}$  and  $C_{s41}$  begin to discharge into the resonant circuit. This stage ends when the gate signals are applied to  $S_{11}$  and  $S_{41}$  again.

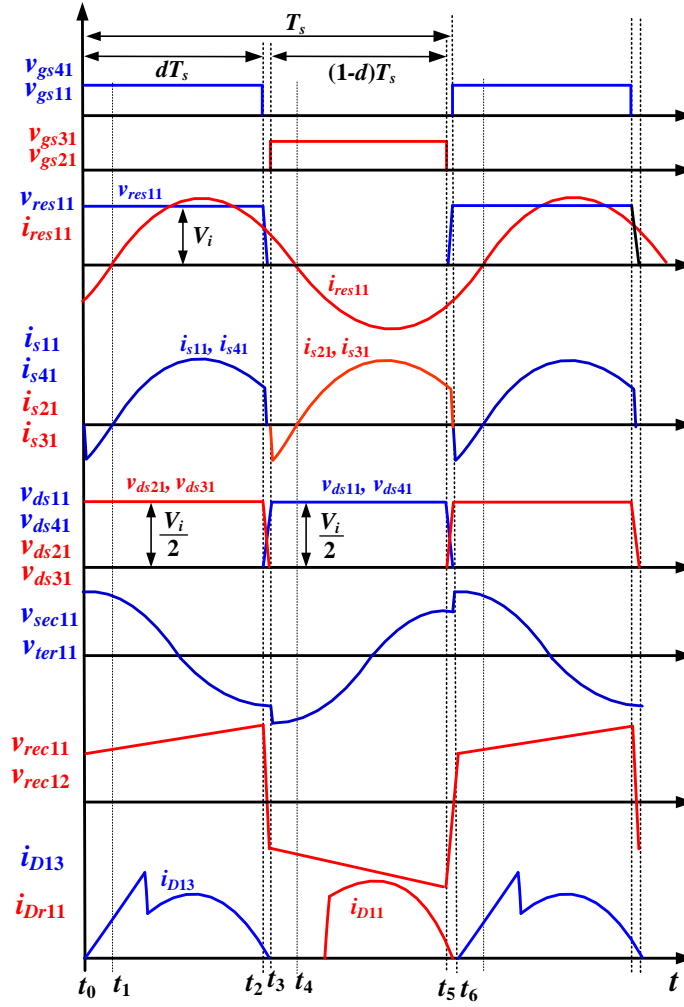


Figure 3.4— Key operating waveforms of the converter for one module

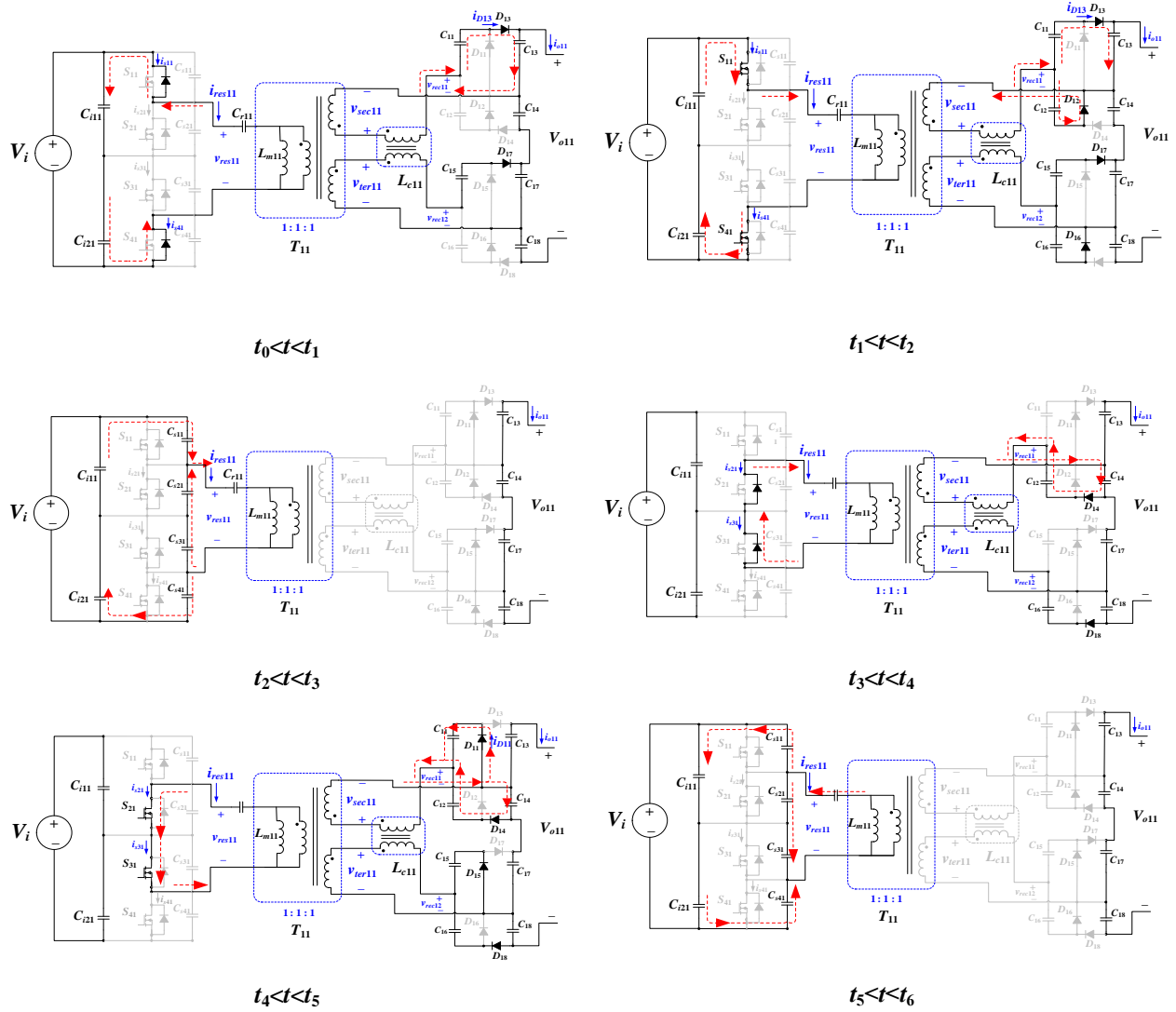


Figure 3.5– Operating stages of the proposed converter within a switching period (illustrated with one module)

### 3.1.3 Converter Analysis

Per module equivalent circuit, shown in Figure 3.6, was used to complete the steady state analysis of the proposed topology. The Fourier series representation of the input voltage to the resonant circuit  $v_{res11}$  is given by (3.1), where  $v_{res11(ac)}$  represents the ac component and is given

by (3.2); where  $D$  represents the duty cycle;  $\theta_h$  is the phase angle that is given by (3.3);  $f_s$  is the operating switching frequency; and  $h$  represents the  $h$ th harmonics. Since the harmonics contents in the resonant circuits can be assumed to be negligible, fundamental approximation is used in the following calculations.

$$v_{res11} = V_i D + v_{res11(ac)} \quad (3.1)$$

$$v_{res11(ac)} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi} \sqrt{1 - \cos(2h\pi D)} \sin(2\pi n f_s t + \theta_h) \right) \quad (3.2)$$

$$\theta_h = \tan^{-1} \left( \frac{\sin(2\pi h D)}{1 - \cos(2\pi h D)} \right) \quad (3.3)$$

To simplify the analysis of the resonant circuit, the following equations are used. The ratio of coupled inductance to magnetizing inductance is given by (3.4);  $R_{ac}$  in Figure 3.6 represents the equivalent load resistance at the output of the resonant circuit.

$$k = \frac{L_{c11}}{L_{m11}} \quad (3.4)$$

As the output power increases,  $R_{ac}$  approaches zero. At full-load, the resonant frequency is determined by  $C_{r11}$  and the equivalent inductance  $L_{eq}$ , which is the parallel combination of resonant and magnetizing inductances.

$$\omega_{FL} = \frac{1}{\sqrt{L_{eq} C_{r11}}} \quad (3.5)$$

$$L_{eq} = \frac{L_{c11} L_{m11}}{L_{c11} + L_{m11}} \quad (3.6)$$

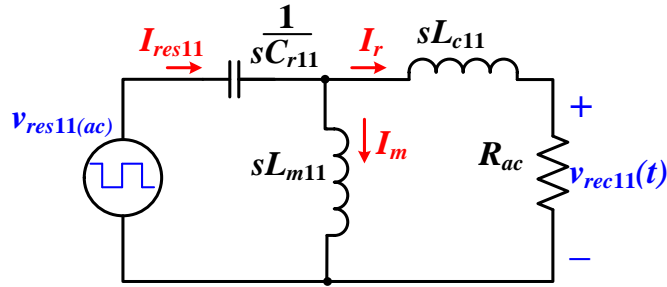


Figure 3.6– The equivalent circuit of the proposed topology

At no-load,  $R_{ac}$  will be open-circuit, and the resonant frequency is defined by  $C_{r11}$  and  $L_{m11}$ :

$$\omega_{NL} = \frac{1}{\sqrt{L_{m11}C_{r11}}} \quad (3.7)$$

The full-load and no-load relative angular operating frequencies are presented by  $\omega_f$  (3.8) and  $\omega_n$  (3.9), respectively, where  $\omega$  represents the angular operating frequency.

$$\omega_f = \frac{\omega}{\omega_{FL}} \quad (3.8)$$

$$\omega_n = \frac{\omega}{\omega_{NL}} = \omega_f \sqrt{\frac{k+1}{k}} \quad (3.9)$$

The relative operating frequency at no-load  $\omega_n$  in (3.9) shows that it is always higher than  $\omega_f$ . Considering the fact that the circuit always operates at a switching frequency above resonance, (3.9) implies that at full-load, the resonant frequency  $\omega_f$  is closer to the switching frequency.

#### A. Resonant current of the inverter ( $i_{res11}$ )

The resonant current ( $i_{res11}$ ) is derived from the ac components of the input voltage to the resonant circuit  $v_{res11(ac)}$  in (3.2), and hence is given by (3.10), where  $|Z_i|$  is the magnitude of the input impedance of the resonant circuit; and  $\phi_{Zi}$  is the phase angle of the input impedance.

$$i_{res11} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_i|} \sqrt{1 - \cos(2h\pi D)} \sin(2\pi hf_s t + \theta_h - \phi_{Zi}) \right) \quad (3.10)$$

$$|Z_{in}| = R_{ac} \frac{\sqrt{\alpha^2 + [h\omega_r Q(1/k + \alpha)]^2}}{h\omega_r \sqrt{[h\omega_r(1 + 1/k)]^2 + Q^2}} \quad (3.11)$$

$$\phi_{Zi} = \tan^{-1} \left( h\omega_r Q \left( \frac{1}{k\alpha} + 1 \right) \right) - \tan^{-1} \left( \frac{Q}{-h\omega_r(1 + 1/k)} \right) \quad (3.12)$$

To simplify the equations, the variable  $\alpha$  is defined by (3.13)

$$\alpha = 1 - \frac{(h\omega_r)^2}{k} \quad (3.13)$$

The relative angular operating frequency ( $\omega_r$ ) is given by (3.14), where  $\omega_0$  represents the angular resonant frequency (3.15).  $Q$  is the quality factor and is given by (3.16).

$$\omega_r = \frac{\omega}{\omega_0} \quad (3.14)$$

$$\omega_0 = \frac{1}{\sqrt{L_{c11}C_{r11}}} \quad (3.15)$$

$$Q = \frac{R_{ac}}{L_{r11}\omega_0} \quad (3.16)$$

From (3.10), the rms resonant current and the peak value of the fundamental resonant current can be given by (3.17) and (3.18), respectively. The ratio of the transformer magnetizing current,  $i_m$  to  $i_r$  is then given by (3.19). It can be inferred from (3.20) that increasing the switching frequency and decreasing  $k$  and quality factor can reduce the circulating current in the circuit, resulting in lower conduction loss. This equation can be examined with respect to  $k$ . It can be seen that as  $k$  approaches zero (by having  $L_m \rightarrow \infty$ ), the circuit can be approximated as a

series-resonant converter and the current through the parallel branch ( $I_m$ ) becomes zero. Hence, circulating current and conduction losses will decrease as the size of  $L_{m11}$  increases. Conversely, the efficiency suffers with a small  $L_{m11}$  as more current will flow through the parallel branch.

$$I_{res11} = \frac{V_i}{\pi} \left[ \sum_{n=1}^{\infty} \left( \frac{1 - \cos(2\pi hD)}{(h|Z_i|)^2} \right) \right]^{1/2} \quad (3.17)$$

$$I_{res11\_max} = \frac{\sqrt{2}V_i \sqrt{1 - \cos(2\pi D)}}{\pi |Z_i|} \quad (3.18)$$

$$\frac{I_m}{I_r} = k \left[ 1 - j \frac{Q}{h\omega_r} \right] \quad (3.19)$$

$$\left| \frac{I_m}{I_r} \right| = k \sqrt{1 + \frac{Q^2}{(h\omega_r)^2}} \quad (3.20)$$

### B. Voltage Gain

The voltage gain of each *CLL* resonant circuit (Figure 3.6) is given by (3.21) as a function of  $\omega_r$ ,  $k$ , and  $Q$ .

$$\frac{V_{rec11}}{V_{res11(ac)}} = \frac{-\omega_r^2}{k\alpha + j\omega_r Q(1 + k\alpha)} \quad (3.21)$$

$$\left| \frac{V_{rec11}}{V_{res11(ac)}} \right| = \frac{\omega_r^2}{\sqrt{(k\alpha)^2 + (\omega_r Q(1 + k\alpha))^2}} \quad (3.22)$$

The series capacitor in the resonant circuit ( $C_{r11}$ ) blocks the dc component of voltage  $v_{res11}$ .

From (3.2), the rms value of resonant voltage  $v_{res11(ac)}$  is given by

$$V_{res11(ac)} = \frac{V_i}{\pi} \left[ \sum \frac{1 - \cos(2h\pi D)}{h^2} \right]^{1/2} \quad (3.23)$$

Then, the total voltage gain of the converter, considering the voltage-quadrupler rectifiers, can be given by

$$\left| \frac{V_{o11}}{V_i} \right| = \frac{8h^2\omega_r^2 \left[ \sum \frac{1 - \cos(2h\pi D)}{n^2} \right]^{1/2}}{\pi \sqrt{(k\alpha)^2 + [h\omega_r Q(1 + k\alpha)]^2}} \quad (3.24)$$

The maximum rms voltage of  $V_{res11(ac)}$  occurs at  $D=0.5$ .

$$\frac{V_{res11(ac)}}{V_i} = \frac{\sqrt{2}}{\pi} \left[ \sum_{h=odd} \frac{1}{h^2} \right]^{1/2} = \frac{1}{2} \quad (3.25)$$

$$\sum_{h=odd} \frac{1}{h^2} = \frac{\pi^2}{8} \quad (3.26)$$

Hence, the total voltage gain of the converter at  $D=0.5$  can be given by (3.27), where  $k$  is given by (3.4).

$$\left| \frac{V_{o11}}{V_i} \right| = \frac{4h^2\omega_r^2}{\sqrt{(k\alpha)^2 + [h\omega_r Q(1 + k\alpha)]^2}} \quad (3.27)$$

A plot of the voltage gain as a function of  $\omega_r$  and  $k$  has been shown in Figure 3.7. It is shown that each curve peaks at a different value of  $k$ . This value is  $k_{critical}$  and represents the point where  $\phi_{zi}=0$ . To achieve ZVS, the operating frequency should always be above the resonant frequency. This means that  $k$  should be selected above  $k_{critical}$ . It also can be seen from Figure 3.7 that higher voltage gain can be achieved by higher  $k$ . On the other hand, according to (3.19), increasing  $k$  can increase the circulating current. Therefore, there is a trade-off between the voltage-gain and the achieved efficiency. A plot of (3.27) for a constant  $k$  ( $k=0.5$ ) and as a function of  $\omega_r$  and  $Q$  is shown in Figure 3.8.

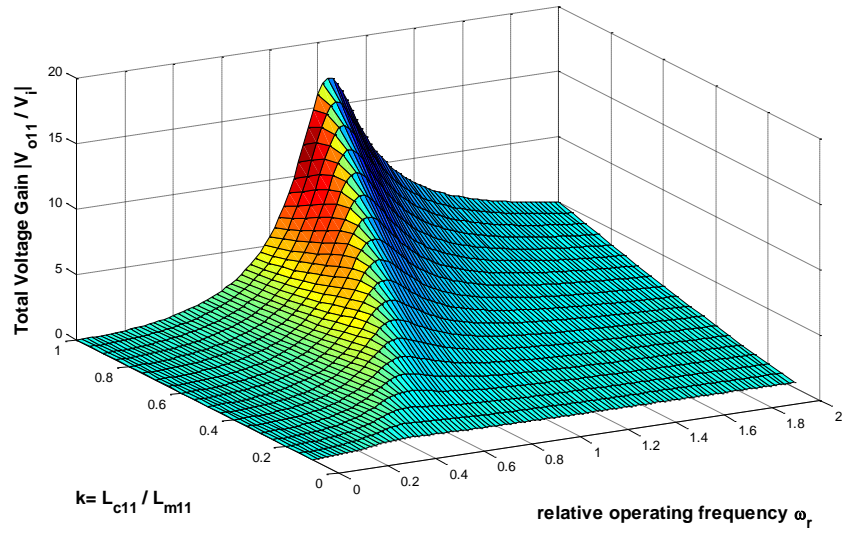


Figure 3.7– Converter voltage gain as a function of  $\omega_r$  and  $k$  for  $Q=4$

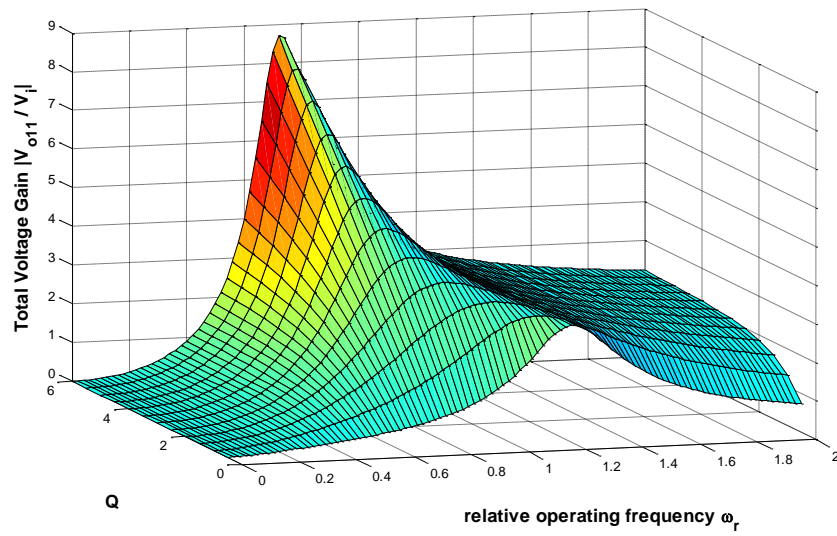


Figure 3.8– Converter voltage gain as a function of  $\omega_r$  and  $Q$  for  $k=0.5$

The next step in designing the converter is to ensure that ZVS will be maintained for all load conditions with a minimized circulating current. To do this, the turn-OFF currents of the switches should be analyzed. For example the turn-OFF switch currents of  $S_1$  and  $S_4$  provides information about whether  $S_2$  and  $S_3$  are turned ON under zero voltage condition.

*C. Turn-OFF currents ( $I_1, I_4$ ) of  $S_{11}, S_{41}$*

The turn-OFF currents of  $S_{11}$  and  $S_{41}$  can be found by the resonant current  $i_{res11}$  at  $t = DT_s$

$$I_1 = I_4 = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_i|} \sqrt{1 - \cos(2h\pi d)} \sin(2\pi h D + \theta_h - \phi_{Z_i}) \right) \quad (3.28)$$

To turn-ON  $S_{21}$  and  $S_{31}$  under zero voltage switching conditions, as shown in Figure 3.4, the resonant current should force the antiparallel diodes to conduct prior to the turn-ON instants of the switches. Hence,  $I_1$  and  $I_4$  must be positive. The normalized turn-OFF current of  $S_{11}$  and  $S_{41}$  ( $I_1$  and  $I_4$ ) as a function of duty cycle  $D$  for  $\omega_r=2$  and  $Q=5$  is shown in Figure 3.9. The equivalent ac resistance  $R_{ac}$ , the dc input voltage  $V_{in}$ , and the angular resonant frequency  $\omega_0$  are chosen as the base values. It is shown that the curves with higher  $k$  have the greatest magnitudes, resulting in higher conduction loss.

*D. Turn-OFF currents ( $I_2, I_3$ ) of  $S_{21}$  and  $S_{31}$*

Similarly, the turn-OFF currents of switches  $S_{21}$  and  $S_{31}$  are found by evaluating (3.10) at  $t=0$  as shown in (3.29). A plot of (3.29) for different sets of parameters is also shown in Figure 3.10.

$$I_2 = I_3 = \sum_{n=1}^{\infty} \left( \frac{-\sqrt{2}V_i}{n\pi|Z_i|} \sqrt{1 - \cos(2n\pi d)} \sin(\theta_n - \phi_{Z_i}) \right) \quad (3.29)$$

The same reasoning can be applied to  $S_{21}$ ,  $S_{31}$ . To allow current flow through the antiparallel diodes and achieving zero voltage switching for  $S_{11}$ ,  $S_{41}$ ,  $I_2$  and  $I_3$  must be positive.

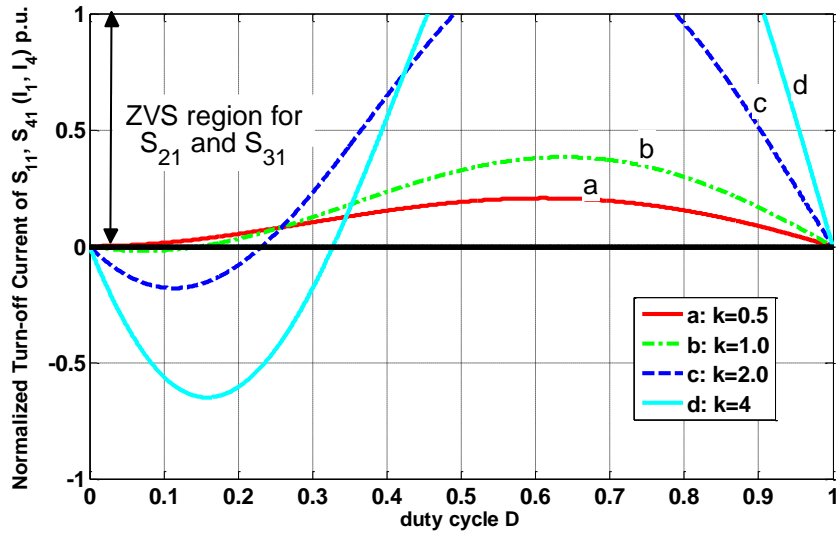


Figure 3.9– Normalized turn-OFF current of  $S_{11}$  and  $S_{41}$  ( $I_1$  and  $I_4$ ) as a function of duty cycle  $d$  for  $\omega_r=2$  and  $Q=5$

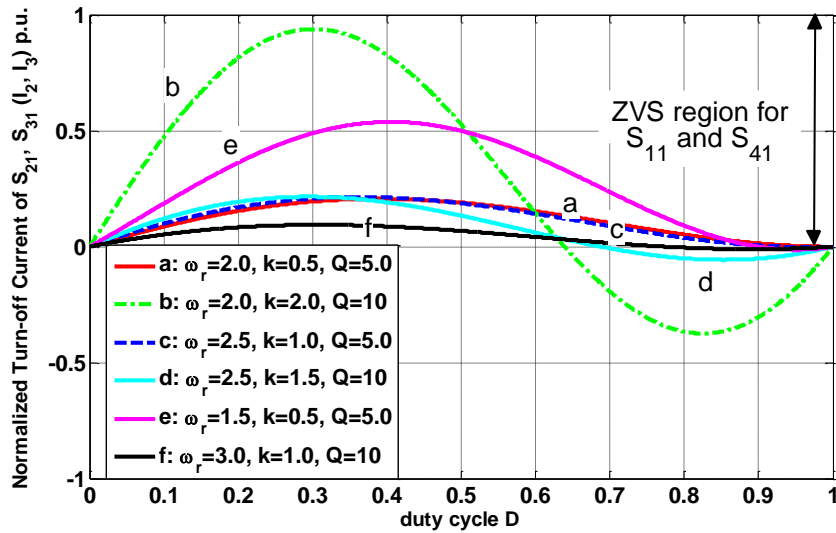


Figure 3.10– Normalized turn-OFF current of  $S_{21}$  and  $S_{31}$  ( $I_2$  and  $I_3$ ) as a function of duty cycle  $D$

### E. Snubber capacitor selection

To achieve ZVS turn-ON, the snubber capacitors should be completely discharged into the resonant circuit within the dead time period, which allows using comparatively large snubber capacitors. As a result, voltage across the switches begins to rise slowly and ZCS turn-OFF can be achieved. The slowest charging and discharging occurs at light-load and high-line. Therefore, the upper limit of the snubber capacitor value is dictated at light load and high line. At light load, it was assumed that all currents flow through  $L_{m11}$ . The  $C_{eq}$  can also be given by a series connection of two snubber capacitors and  $C_{r11}$  (3.30).

$$C_{eq} = \left[ \frac{2}{C_{snubber}} + \frac{1}{C_{r11}} \right]^{-1} \quad (3.30)$$

$$\omega_{snubber} = \frac{1}{\sqrt{L_{m11}C_{eq}}} = \sqrt{\frac{2}{L_{m11}C_{snubber}} + \frac{1}{L_{m11}C_{r11}}} \quad (3.31)$$

As a general rule of thumb to achieve reasonable zero-voltage turn-OFF for all conditions, the MOSFET snubber capacitors should charge in no less than  $2t_{fi}$ , where  $t_{fi}$  is the fall time of the switch current at turn-OFF, and  $t_d > 2t_{fi}$ .

$$t_d \geq \frac{2\pi}{4\omega_{snubber}} \geq 2t_{fi} \quad (3.32)$$

Moreover, the magnetizing inductance  $L_m$  must store enough energy to completely discharge the two snubber capacitors.

$$\frac{1}{2}L_{m11}I_2^2 \geq \frac{1}{4}C_{snubber}V_{in}^2 \quad (3.33)$$

### 3.1.4 Simulation, Experimental Results and Performance

To demonstrate the functionality of the proposed converter, a 4-MW wind turbine system with an output dc voltage of 18 kV was simulated in PSIM for the proposed modular converter shown in Figure 3.2. The input voltage is selected to be 3.3 kV and to transfer this amount of power, six modules were employed, with two in series ( $n=2$ ) and three in parallel ( $m=3$ ). Note that in the proposed topology the voltage stress across each switch is half of the dc-link voltage, due to the multistring arrangement of the power SiC MOSFETs. Hence, half-bridge SiC MOSFET modules from CREE (CAS300M17BM2) were utilized for a 4 MW modular converter. Experimental results on two 3.7 kW, 0.5/2.7 kV modules are also provided. Per module system specifications and components parameters for both simulation and prototype are summarized in Table 3.2.

#### 3.1.4.1 Design Procedure

The design steps of the simulation and prototype components are as follows:

##### 1. Resonant Tank Values

The equivalent output ac resistance can first be obtained by

$$R_{ac} = \frac{2}{\pi^2} \frac{V_o^2}{P_o} = 100\Omega \quad (3.34)$$

The switching frequency is assumed to be around 17 kHz. To achieve a voltage gain of 5.4 for each module, according to Figure 3.7 and Figure 3.8,  $k$  and  $Q$  are chosen to be 0.5 and 3.5, respectively. With respect to the duty ratio  $D$ , the maximum voltage gain occurs at  $D=0.5$ . Hence according to (3.27),  $\omega_r$  is calculated to be 1.2.  $L_{c11}$  is then calculated accordingly:

$$L_{c11} = \frac{R_{ac}}{Q\omega_0} = 346\mu H \quad (3.35)$$

Table 3.2– Specifications and Components Used in the Simulation and the Laboratory-Scale Prototype

Per Module Converter Specifications		
	Simulation	Prototype
Per module rated power ( $P_{o11}$ )	670kW	3.7kW
DC-link voltage ( $V_i$ )	3.3kV <sub>DC</sub>	500V <sub>DC</sub>
Per module output dc voltage ( $V_{o11}$ )	18kV <sub>DC</sub>	2.7kV <sub>DC</sub>
Per module voltage gain	~5.4	~5.4
Switching freq. $f_s$ (at full-load)	~16.8kHz	~17.4kHz
Circuit Components Parameters (Per Module)		
	Simulation	Prototype
SiC MOSFETs $S_{11} \sim S_{41}$	CAS300M17BM2 (CREE) (1.7kV, 325A, 8.0mΩ)	SCT3022AL (ROHM) (650V, 93A, 22mΩ)
Snubber capacitors $C_{s11} \sim C_{s41}$	BFC237894243 (Vishay) (24nF, 2kV <sub>DC</sub> )	ECQ-E6153KF (Panasonic) (15nF, 630V <sub>DC</sub> )
Input capacitors $C_{i11} \sim C_{i21}$	C20AZGR5220AASK (KEMET) (22μF, 2.3kV <sub>DC</sub> )	EZP-E50107MTA (Panasonic) (100μF, 500V <sub>DC</sub> )
Resonant capacitors $C_{r11}$	2 × B25856K2204K3 (EPCOS) 2 × 0.2μF, 4kV <sub>DC</sub>	2 × BFC238330204 (Vishay) 0.2μF, 1000V <sub>DC</sub>
Three-winding transformer $L_{mn}$	720μH (1:1:1)	720μH (1:1:1), 32mΩ, L <sub>Leakage</sub> :12 μH N87 Ferrite Core
Coupled inductor $L_{cn}$	335μH (1:1)	335μH (1:1), 48mΩ L <sub>Leakage</sub> :66μH N87 Ferrite Core
SiC diodes $D_{1n} \sim D_{4n}$	MSC030SDA120B SiC Schottky Diode (1.2kV, 65A) (4 in Series)	GP2D005A170B SiC Schottky Diode (1.7kV, 5A)
Output capacitors $C_{11} \sim C_{22}$	T50W1NR-F (CDE) (1μF, 5kV <sub>DC</sub> )	B32774D4106K (EPCOS) (1μF, 1.3kV <sub>DC</sub> )

With  $k = 0.5$ ,  $L_{m11}$  is then equal to 692  $\mu\text{H}$  with a turns-ratio of 1:1, and  $C_{r11}$  is obtained by

$$C_{r11} = \frac{1}{(2\pi f_0)^2 L_s} = 400 \text{ nF} \quad (3.36)$$

The snubber capacitors are calculated according to (3.31) – (3.33):  $C_{s11} \sim C_{s41} = 24 \text{ nF}$ ; so that close to ZCS turn-OFF are realized for all switches in the circuit.

## 2. High-Frequency Transformer

### a) Choice of material

According to the properties of magnetic materials, illustrated in Table 3.3, with the range of switching frequency of around 20 kHz and availability of the core types, MnZn Ferrite core with the material of N87 from TDK is selected.

### b) Choice of inductance factor; $A_L = L/N^2$ value

The relative temperature coefficient  $\alpha_F$  of N87 according to the table of material properties is on average about  $4 \times 10^{-6}/\text{K}$ . Since the required temperature coefficient of effective permeability ( $\alpha_e$ ) value of the ungapped PM core is about  $64 \times 10^{-5}/\text{K}$  [77], the effective permeability can be found

$$\alpha_F = \frac{\alpha_e}{\mu_e} \Rightarrow \mu_e = \frac{\alpha_e}{\alpha / \mu_i} = \frac{64 \times 10^{-5}}{4 \times 10^{-6}} = 160 \quad (3.37)$$

Hence, with the core type PM 87/70 and  $\mu_e = 160$ , inductance factor can be found from datasheet:  $A_L = 1250 \text{ nH}$ .

*c) Choice of winding material*

Litz wire with 1000 strand of AWG44 wires (i.e., 1000×0.05 mm) covered by natural silk is used. The total cross section of the Litz wire is calculated 1000×0.002 mm<sup>2</sup>=2 mm<sup>2</sup>. The dc resistance of this aforementioned Litz wire can be found by (3.38) [78].

$$R_{DC} = \frac{R_s \cdot (1.015)^{N_B} \cdot (1.025)^{N_C}}{N_s} = \frac{2873 \times 1.015 \times 1.025}{1000} = 2.99 \text{ ohm}/1000 \text{ ft} \quad (3.38)$$

where  $R_s$  is the maximum dc resistance of the individual strands and for AWG44 is 2873 ohms/1000 ft.  $N_B$  is the number of bunching operations and  $N_C$  is the number of cabling operations which in this case both are 1; and finally  $N_s$  is the number of individual strands. The ac to dc resistance ratio is then given by

$$\frac{R_{AC}}{R_{DC}} = 1 + K \left( \frac{N_s D_1}{D_o} \right)^2 G = 1 + 2 \left( \frac{1000 \times 0.002}{0.085} \right)^2 \times 5.4 \times 10^{-7} = 1.0006 \quad (3.39)$$

where  $K$  is constant and depends on  $N_s$ . For  $N_s=1000$ ,  $K$  is 2.  $D_1$  is the diameter of the individual strands over the copper and  $D_o$  is the diameter of the finished cable over the strands.  $G$  is the eddy-current basis factor and is given by

$$G = \left( \frac{D_1 \sqrt{f_{sw}}}{10.44} \right)^4 = \left( \frac{0.002 \sqrt{20 \times 10^3}}{10.44} \right)^4 = 5.4 \times 10^{-7} \quad (3.40)$$

*d) Number of turns and current density*

For an  $A_L$  value of 1250nH and a desired inductance of 720 μH, the equation  $N=(L/A_L)^{0.5}$  yields 24 turns. The current density is selected to be 4 A/mm<sup>2</sup> [79]. The rms current of the transformer primary winding is 17 A. Hence, two parallel Litz wire (1000×0.05mm) is used to achieve a

current density of  $4.2 \text{ A/mm}^2$ . The secondary and tertiary windings consist of only one Litz wire. The detailed specifications of the high frequency transformer are presented in Table 3.4. A picture of the high frequency transformer is also shown in Figure 3.11.

Table 3.3– Properties of Magnetic Properties

Magnetic Material Properties				
Material Name	Trade Name Composition	Initial Permeability $\mu_i$	Flux Density (Tesla) $B_s$	Typical Operating Frequency
Permalloy	80-20 NiFe	25000	0.66-0.82	1k-25k
Amorphous	Nanocrystalline	30,000	1.0-1.2	250k
Ferrite	MnZn	0.75-15k	0.3-0.5	10k-2M
Ferrite	NiZn	0.20-1.5k	0.3-0.4	0.2M-100M

Table 3.4– Specifications of the High Frequency Transformer Utilized in the Proposed Converter

Core	Flux density ( $B$ )	Relative effective permeability ( $\mu_e$ )	Effective magnetic cross section $A_e$	Turns	Litz wire	Magnetizing Inductance	Parasitic Resistance	Leakage Inductance
N87 (TDK) Ferrite Core PM 87/70	300mT	160	$910 \text{ mm}^2$	24/24/24	0.050mm $\times 1000$ strands	720 $\mu$ H	32m $\Omega$	12 $\mu$ H

Table 3.5– Specifications of the Coupled Inductor utilized in the Proposed Converter

Core	Flux Density ( $B$ )	Effective Magnetic Cross Section $A_e$	Turns	Litz Wire	Magnetizing Inductance	Parasitic Resistance	Leakage Inductance
N87 Ferrite Core two stacked E 65/32/27	280mT	$910 \text{ mm}^2$	12/12	0.050mm $\times 1000$ strands	350 $\mu$ H	58m $\Omega$	43 $\mu$ H

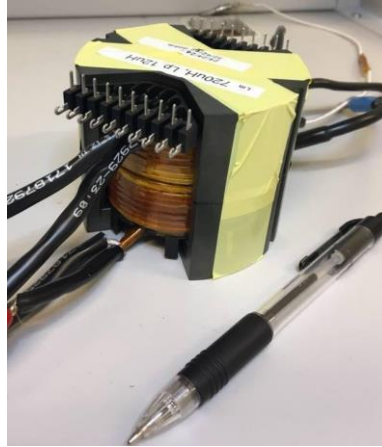


Figure 3.11– A picture of HF three-winding 1:1:1 transformer (weight 1.3kG, height: 70mm, diameter: 87mm)

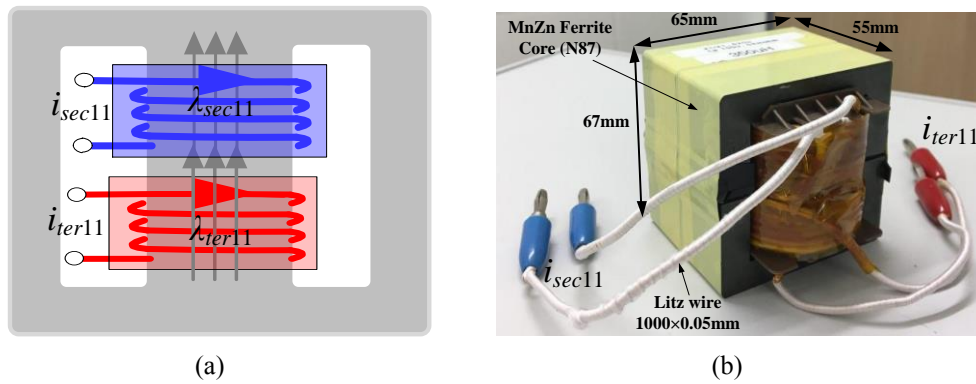


Figure 3.12– (a) Structure of the coupled inductor (b) a picture of experimental coupled inductor

### 3. Coupled Inductor

The coupled inductor was designed based on the approach used for the high frequency transformer. Two ferrite E core (65/32/27) form TDK were stacked together to meet the design criteria as it is shown in Table 3.5. To reduce the skin effect and mitigate the proximity effect, high-frequency Litz wire was also used for each winding. The structure of the coupled inductor and a picture of the implemented coupled inductor are shown in Figure 3.12.

#### ***4. Voltage Quadrupler Rectifier***

According to section 2.3.1.1, the stress of the voltage across the diodes and capacitors in the voltage quadrupler is  $V_o/2$ . The current going through the diodes in the voltage quadrupler is also equal to the dc output current. Hence, the diodes and capacitors voltage ratings can be selected accordingly. For design and selection of voltage quadrupler rectifier components and other components refer to Table 3.2.

#### **3.1.4.2 Simulation Results**

Figure 3.13 shows the key simulation results for full-load condition, where the duty ratio is  $D=0.5$ . As illustrated, ZVS turn-ON and close to ZCS turn-OFF are achieved for all the switches. The rms current going through each switch module is 212 A and the stress of voltage across each switch is 1.65 kV which makes it possible to utilize new 1.7 kV CREE SiC MOSFETs. Figure 3.14 shows the measured current and voltage waveforms across the diodes in one of the high frequency voltage-quadrupler modules. It can be observed that soft switching is achieved for all the diodes. The balanced output voltages of the three-winding HF transformer at full-load condition is also shown in Figure 3.15. Figure 3.16 shows the total 18 kV<sub>DC</sub> output voltage, input voltage of 3.3 kV<sub>DC</sub> and the balanced input voltages to the voltage-quadruplers. A peak efficiency of 98% was measured in the simulated system.

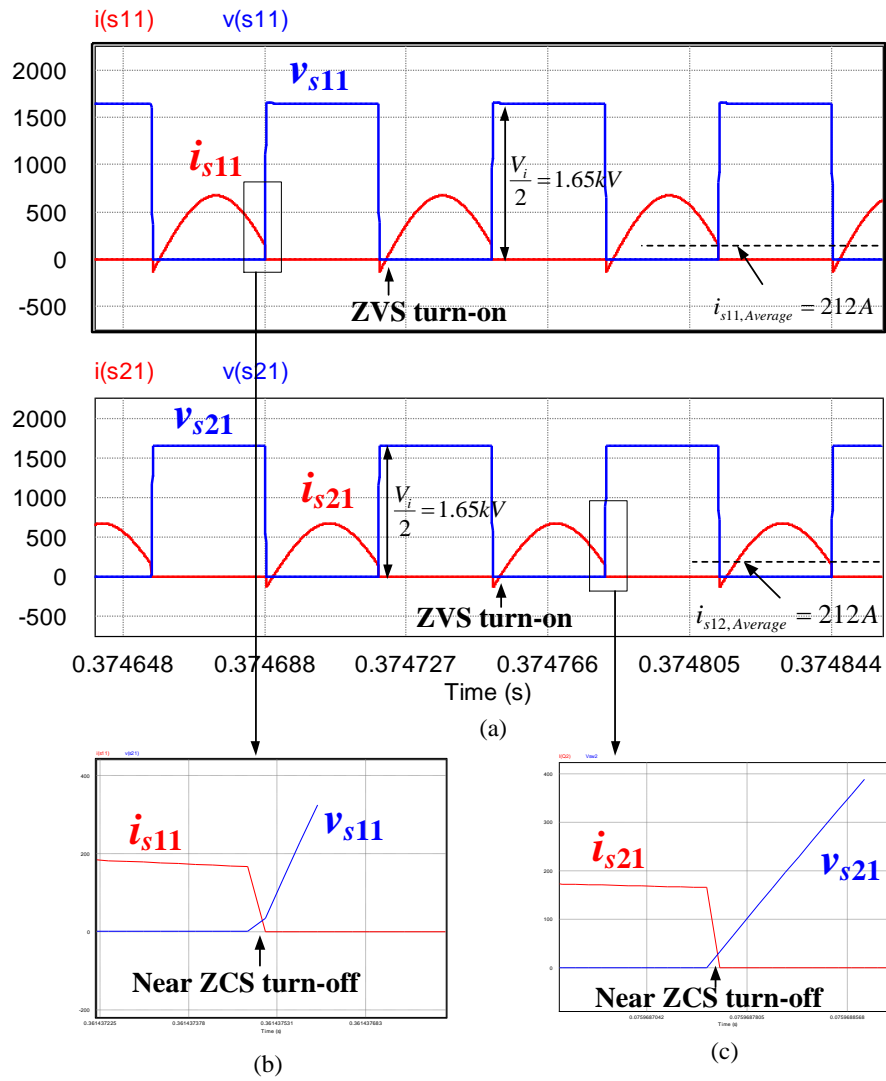


Figure 3.13– Per module switching waveforms at full-load simulation

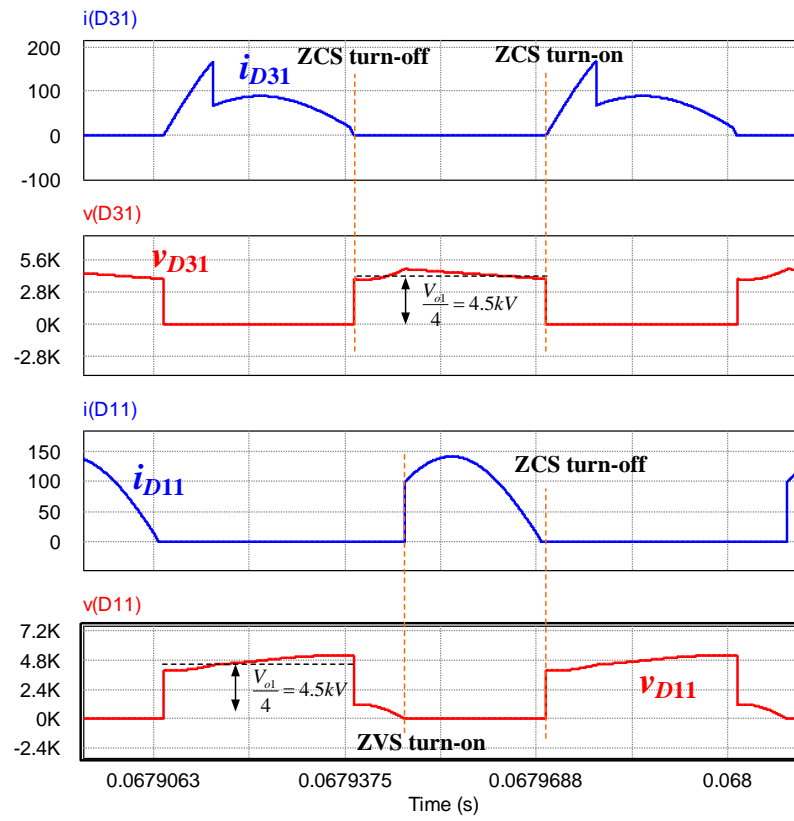


Figure 3.14– Voltage-quadrupler diodes waveforms at full-load simulation

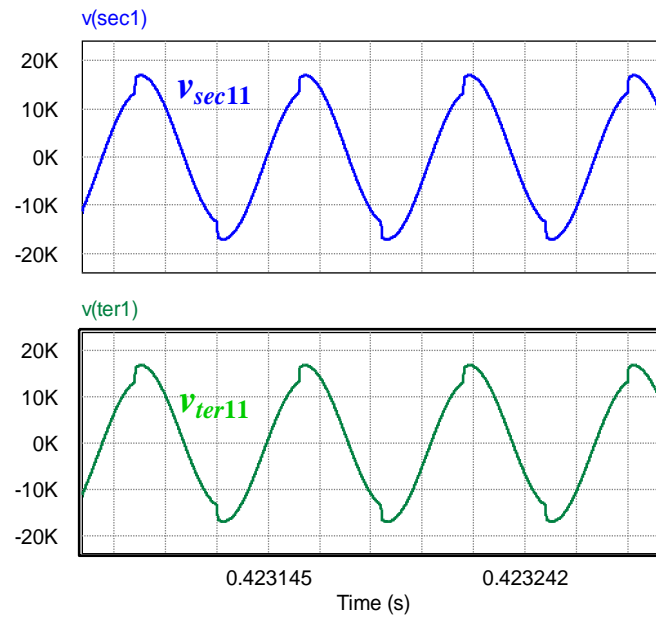


Figure 3.15– Three-winding HF transformer voltages at full-load simulation

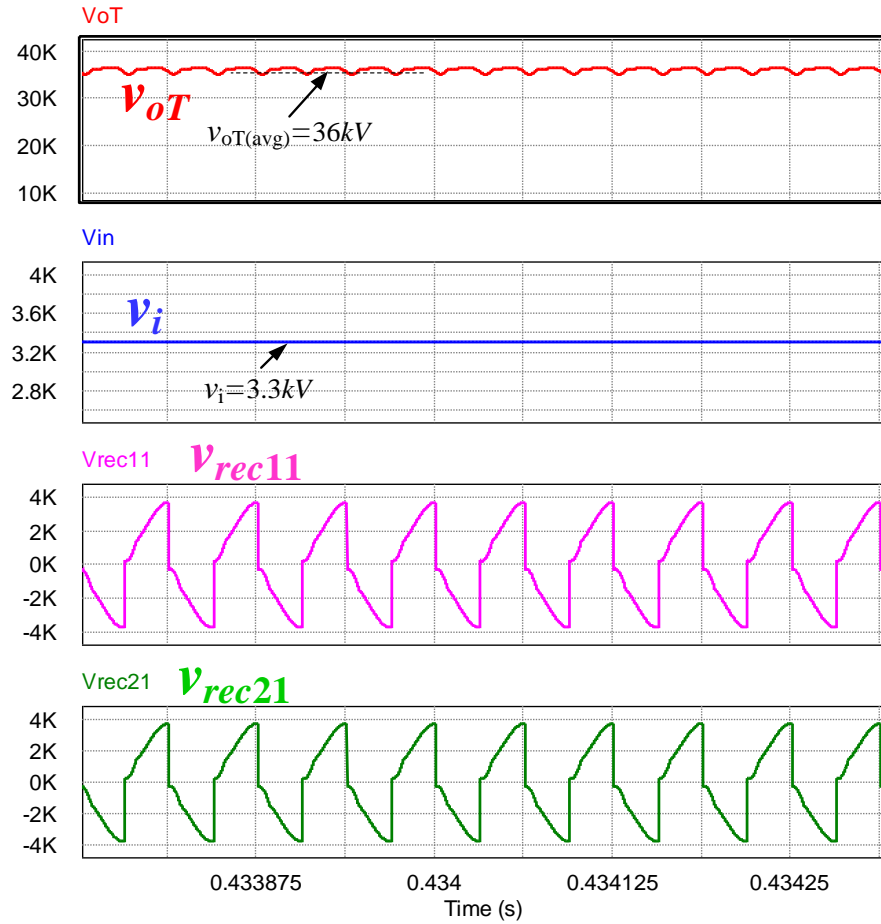


Figure 3.16– Total dc output voltage, input voltage and the balanced input voltages to the voltage-quadruplers

### 3.1.4.3 Experimental Results

To further verify the performance of the proposed topology, two modules with the rated power of 3.7 kW each and input voltage of 500V were built in the laboratory. The dc output voltage for each module is 2.7 kV, with a gain of 5.4. To provide a solid validation of the presented work, circuit component parameters of the experimental prototype is exactly similar to the simulation. Per module system specifications is illustrated in Table 3.2. Due to the identical operation of the modules, results have been shown for only one module. SiC MOSFETs from ROHM were

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utilized in the prototype implementation, and SiC Schottky diodes were employed for high frequency rectifying stages. A picture of the experimental prototype consisting two modules is shown in Figure 3.17.

In the experimental prototype, the switching frequency is 17.4 kHz and the duty ratio is  $D=0.5$ . The switching waveforms and their turn-ON and turn-OFF transitions are illustrated in Figure 3.18. This figure shows that the proposed converter can maintain ZVS turn-ON and near ZCS turn-OFF in both pairs of switches. Figure 3.19 shows the measured current and voltage waveforms across the diodes in the output high frequency voltage-quadrupler modules. As illustrated, a smooth transition due to the soft-switching operation of the SiC Schottky diodes has been obtained. It is also evident that there are no voltage spikes across the output diodes. Hence, the commutations of the diodes are almost lossless. The secondary and tertiary voltages of the high frequency isolating transformer in Figure 3.20 demonstrate a balanced performance of the circuit. The efficiency performance of the converter at full-load condition is shown in Figure 3.21, where a peak efficiency of 98.7% has been achieved.

The circuit was also tested at reduced load condition (20% of the rated power). To regulate the output voltage of each module at 2.7 kV<sub>DC</sub>, the switching frequency was increased to 18.1 kHz. The switching waveforms in Figure 3.22 demonstrate that the circuit can also achieve ZVS and ZCS at reduced load condition. The measured efficiency for the light-load condition is 95% that is shown in Figure 3.23.

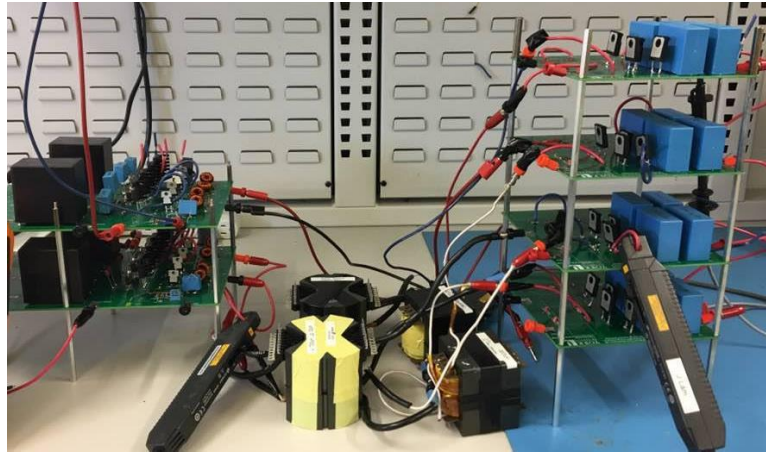
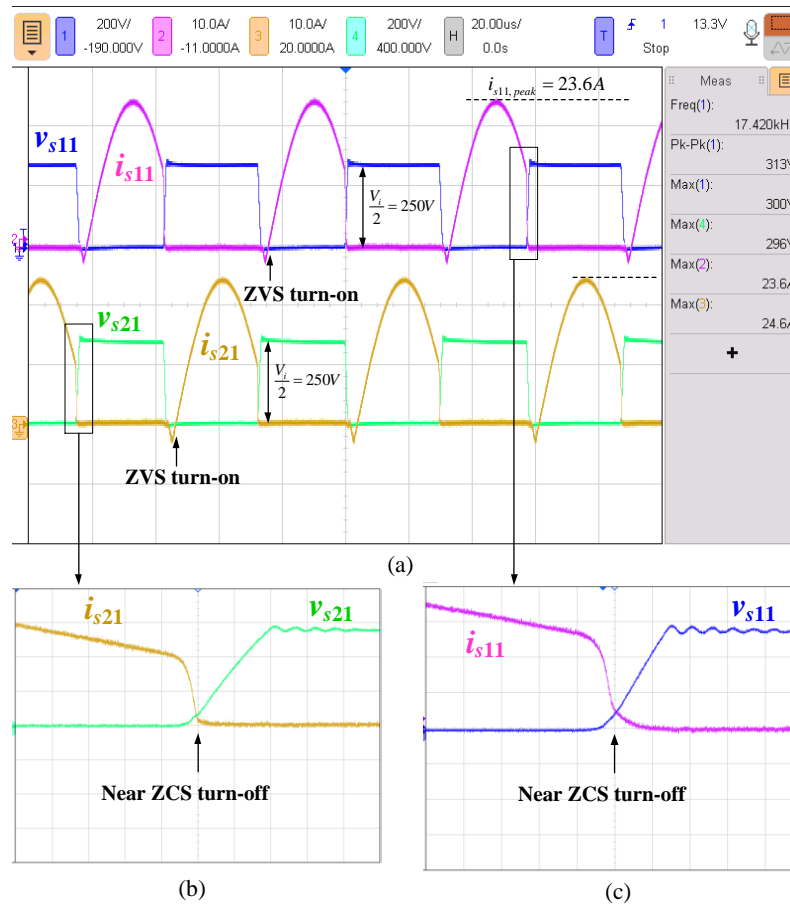


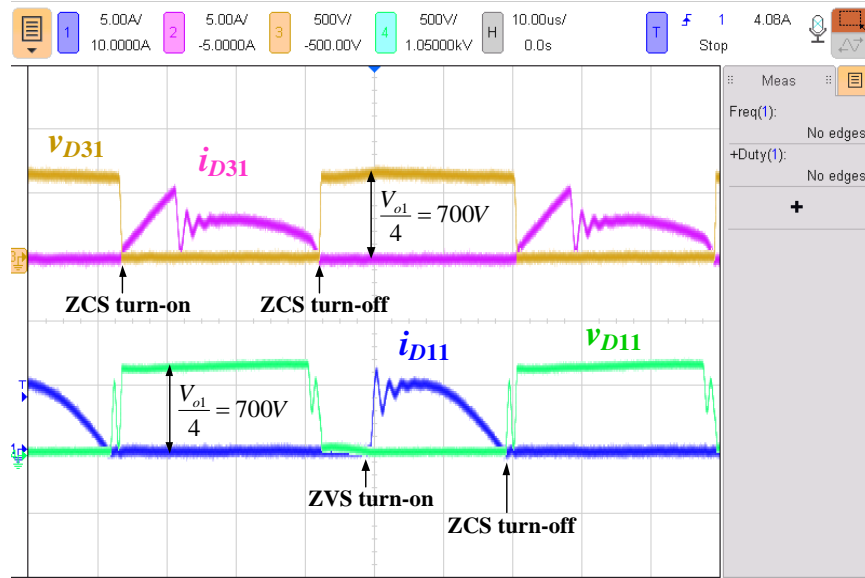
Figure 3.17– A picture of modular laboratory scale experimental prototype



(a) [ $v_{s11}$ ,  $v_{s21}$ : 200V/div;  $i_{s11}$ ,  $i_{s21}$ : 10A/div; time: 20 $\mu$ s/div]

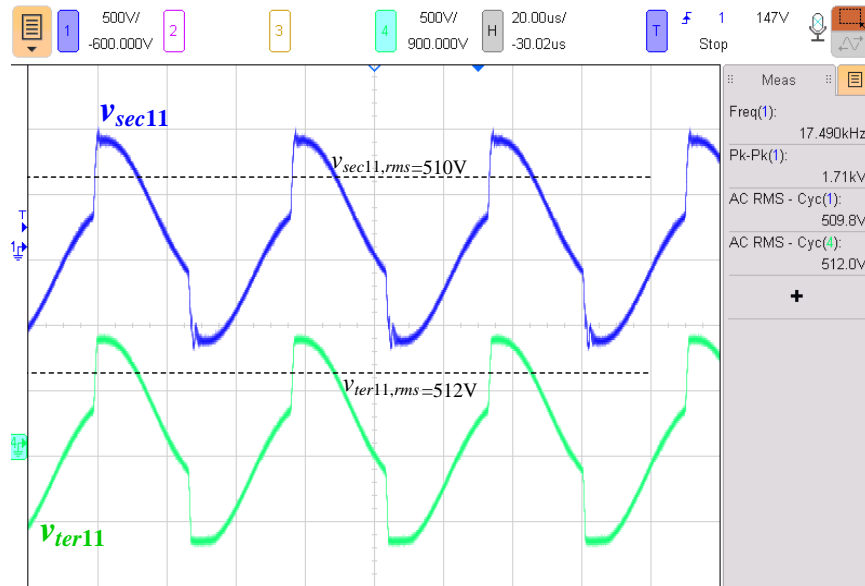
(b), (c) [ $v_{s11}$ ,  $v_{s21}$ : 200V/div;  $i_{s11}$ ,  $i_{s21}$ : 5A/div; time: 500ns/div]

Figure 3.18– Measured switching waveforms in one module at full-load



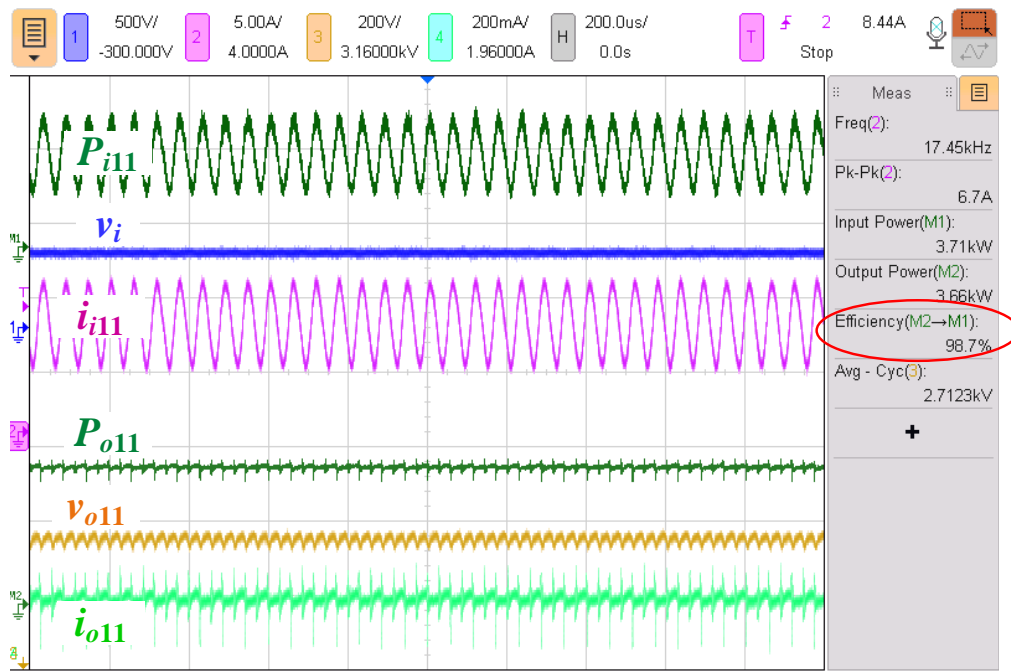
[ $i_{D11}$ ,  $i_{D31}$ : 5A/div;  $v_{D11}$ ,  $v_{D31}$ : 500V/div; time: 10 $\mu$ s/div]

Figure 3.19– Measured voltage-quadrupler diodes waveforms at full-load



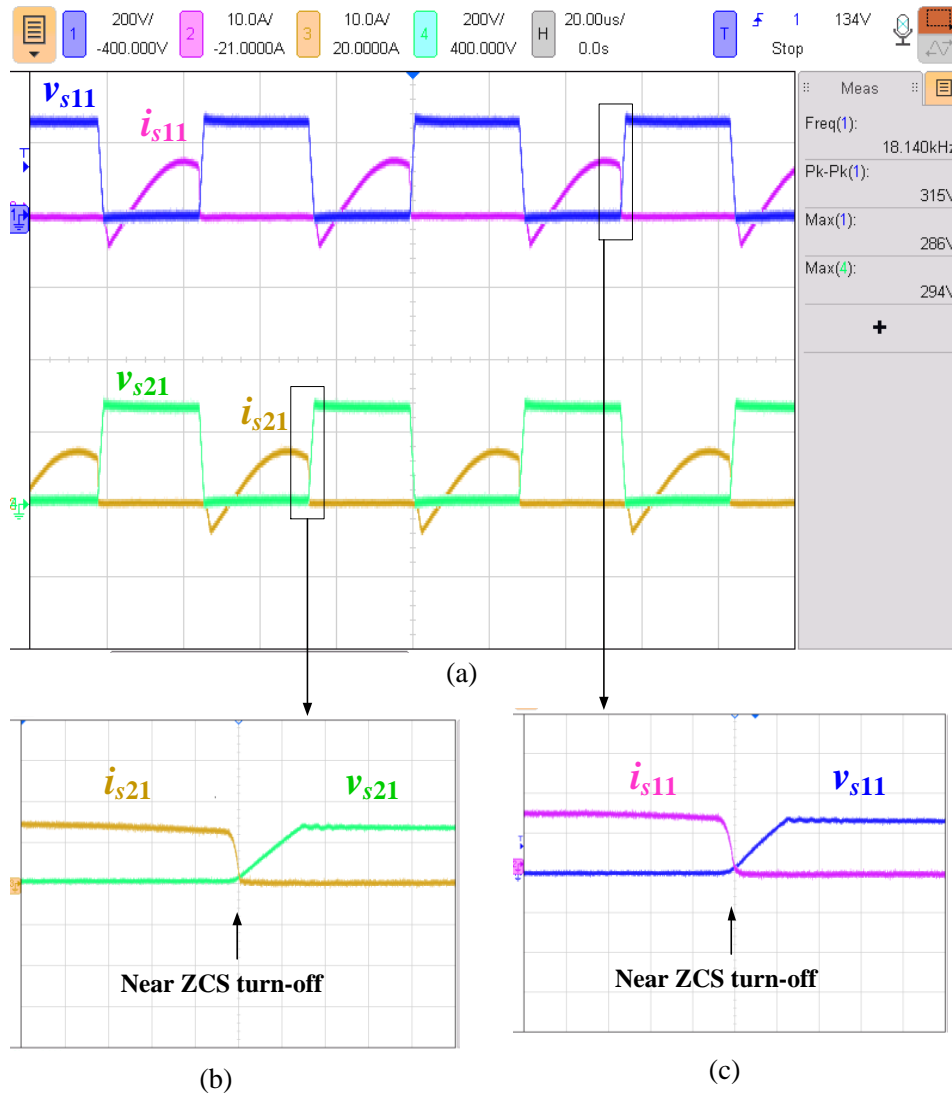
[ $v_{sec1}$ ,  $v_{ter1}$ : 500V/div; time: 20 $\mu$ s/div]

Figure 3.20– Measured output voltages of the HF isolating transformer



[ $v_i$ : 500V/div;  $i_{i11}$ : 5A/div;  $v_{o11}$ : 200V/div;  $i_{o11}$ : 200mA/div; time: 200 $\mu$ s/div]

Figure 3.21– Measured input and output power at full-load condition per module



(a) [ $v_{s11}$ ,  $v_{s21}$ : 200V/div;  $i_{s11}$ ,  $i_{s21}$ : 10A/div; time: 20 $\mu$ s/div]

(b), (c) [ $v_{s11}$ ,  $v_{s21}$ : 200V/div;  $i_{s11}$ ,  $i_{s21}$ : 5A/div; time: 1 $\mu$ s/div]

Figure 3.22– Measured switching waveforms in one module at reduced load condition (20% of rated power)

The dynamic response of the proposed converter with the step change in the input voltage is shown in Figure 3.24. As can be seen, the switching frequency is increased from 17.4 kHz at  $v_i=500$  V to 19.2 kHz at  $v_i=600$  V to maintain the output voltage at 2.7 kV with a variable

frequency control. DSP Texas Instrument TMS320F28335 was employed to implement the closed loop. The secondary and tertiary currents of the transformer with the step change in the input voltage are also shown in Figure 3.25. These waveforms once again verify the balanced performance of the converter.

Figure 3.26 shows the thermal images of the key components of the circuit including switches, output rectifier diodes, and high frequency transformer at rated power. The temperature measurements showed that the operating temperature of the switches and diodes are well below the device's maximum operating temperature.

The simulation and prototype efficiency for various power levels from 20% power level to rated power is shown in Figure 3.27. A peak efficiency of 98.7% was measured for the prototype and an efficiency of 98% was obtained for 4MW wind turbine simulation.

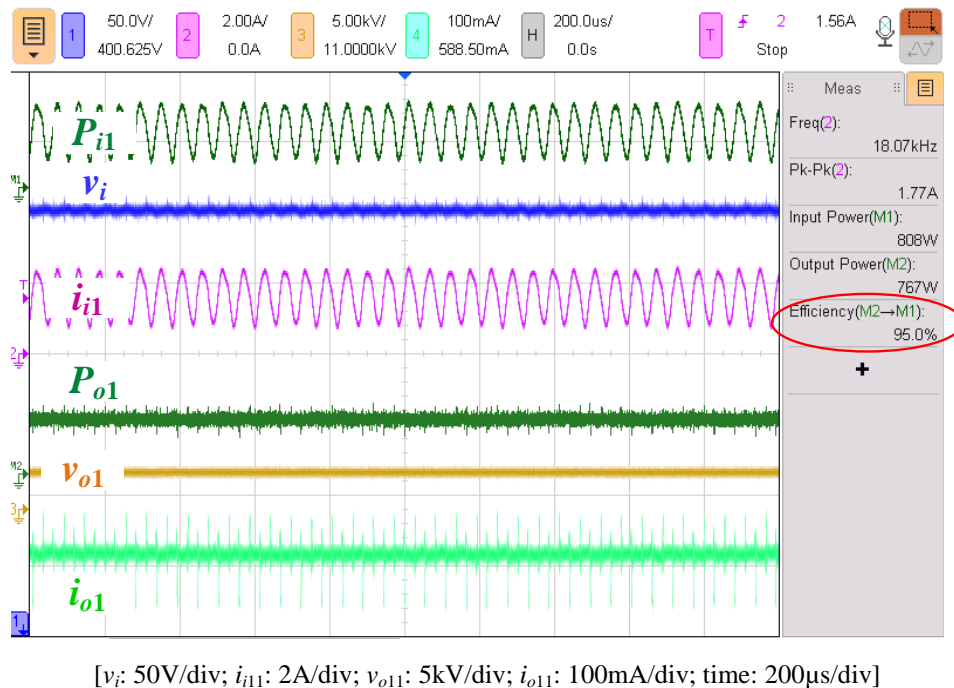
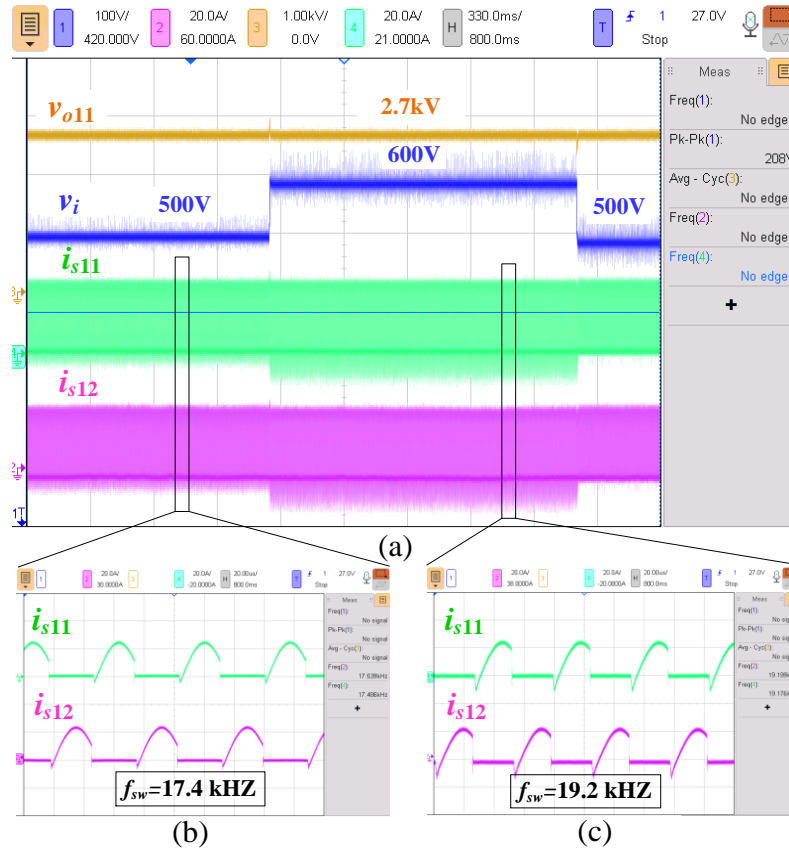
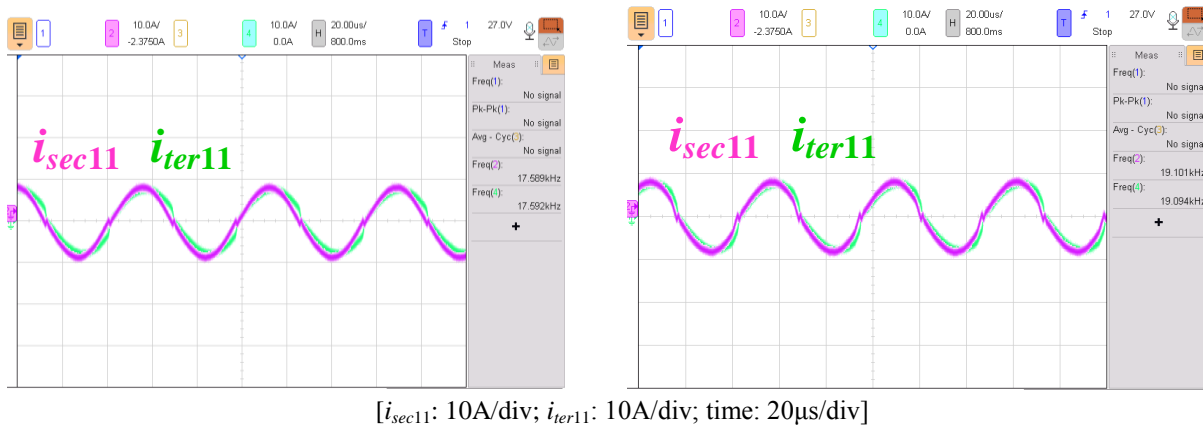


Figure 3.23– Measured input and output power in one module at reduced load condition (20% of rated power)



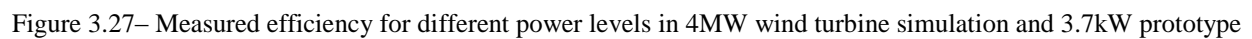
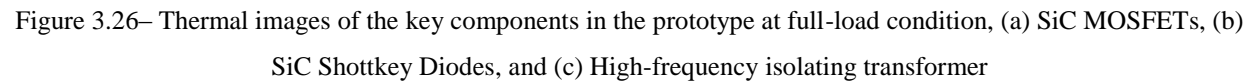
[ $v_{o11}$ : 1kV/div;  $v_i$ : 100V/div;  $i_{s11}$ : 20A/div;  $i_{s12}$ : 20A/div; time: 330ms/div]

Figure 3.24– (a) Dynamic response with the step change in the input voltage; (b) switching waveforms at  $v_i=500V$ ; (c) switching waveforms at  $v_i=600V$



[ $i_{sec11}$ : 10A/div;  $i_{ter11}$ : 10A/div; time: 20μs/div]

Figure 3.25– The secondary and tertiary currents of the transformer with the step change in the input voltage, (a) at  $v_i=500V$ , (b) at  $v_i=600V$



## 3.2 Step-Up Converter Module Configuration with a 1:1 Turns-Ratio Multi-Winding Transformer

To increase power handling (current carrying) capacity of the converter proposed in the previous section; and to fully incorporate all the switches in transferring the power to the output load and capture more power from the input inverter, a novel step-up dc-dc converter module that consists of three resonant sub-modules interconnecting with 1:1 turns-ratio multi-winding transformer and coupled current-fed voltage doubler modules is presented in this section. The presence of three resonant sub-modules circuit connecting via a three-winding two-phase transformer in the proposed circuit is able to capture more power from the input inverter. In addition, the proposed converter uses a coupled inductor at the input of the high frequency rectifying stage to form a current-fed high-gain rectifier. The current-driven structure of the high-gain rectifier guarantees smooth performance of the diodes. Hence, the diode reverse recovery losses are eliminated.

### 3.2.1 Circuit Descriptions and Operating Principles of the Proposed Converter

The proposed circuit consists of an inverter with multistring connection, three resonant circuit sub-modules connected to a multi-winding transformer, and a coupled high-frequency, voltage doubler rectifier modules. The high frequency inverter in each module consists of “multiple string” of switches so that the voltage stress across each switch is reduced to half of the dc-link voltage ( $V_i$ ). Figure 3.28 shows the proposed modular dc-dc step-up converter configuration. In each module, the resonant inverter consists of four switches. The switches ( $S_{1n}$ ,  $S_{4n}$ ) turn ON

during the interval  $D_n T_{s,n}$  and switches ( $S_{2n}, S_{3n}$ ) turn ON during the interval  $(1-D_n) T_{s,n}$ , where  $D_n$  and  $T_{s,n}$  represent the duty ratio and the period of the  $n$ th module, respectively.

The isolated *CLL* resonant circuit consists of the capacitors  $C_{r1n} \sim C_{r4n}$ , a coupled inductor ( $L_{cn}$ ) that is isolated by a unity turns-ratio transformer ( $T_n$ ) with the magnetizing inductance of  $L_{mn}$ . The converter incorporates transformer nonidealities (i.e., leakage and magnetizing inductances) into the basic operation of the *CLL* resonant circuit. The proposed circuit also benefits from implementing dc-blocking capacitors in series with the primary winding of the HF transformer to avoid core saturation. ZVS turn-ON can be achieved for all the switches by the energy stored in the magnetizing and coupled inductors which flows through the switches antiparallel diodes. Near ZCS turn-OFF can also be obtained by discharging the snubber capacitor across each switch prior to the rising edge of the gate signal.

In high power systems, using magnetic coupling is often beneficial particularly when high voltage gain is required [40]. In the proposed circuit, the coupled inductor is integrated at the input of high-frequency, high-gain rectifiers to improve the efficiency, reliability and performance by reducing the component stress and balancing the current and voltage sharings [56]. Owing to the inherent current balancing effect of the coupled inductor, the output voltages of each rectifying stage ( $v_{o1n}$  and  $v_{o2n}$ ) are also balanced. Furthermore, the combination of coupled inductor and high frequency voltage doubler builds a current-fed converter in the proposed circuit. The current-fed converter can achieve a large range of soft switching for the high-frequency rectifier diodes and consequently provides high efficiency over a wide range of operating points [80].

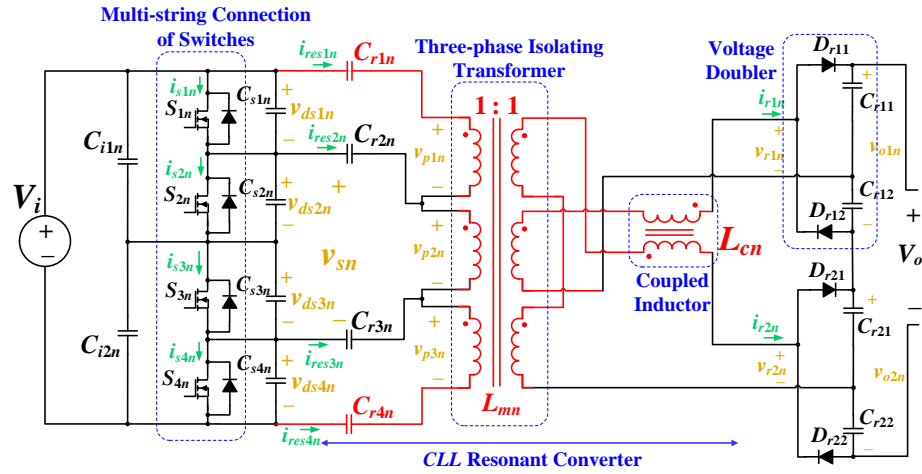


Figure 3.28– Proposed step-up converter module using magnetically-integrated step-up resonant circuits and integrated current-fed voltage doublers

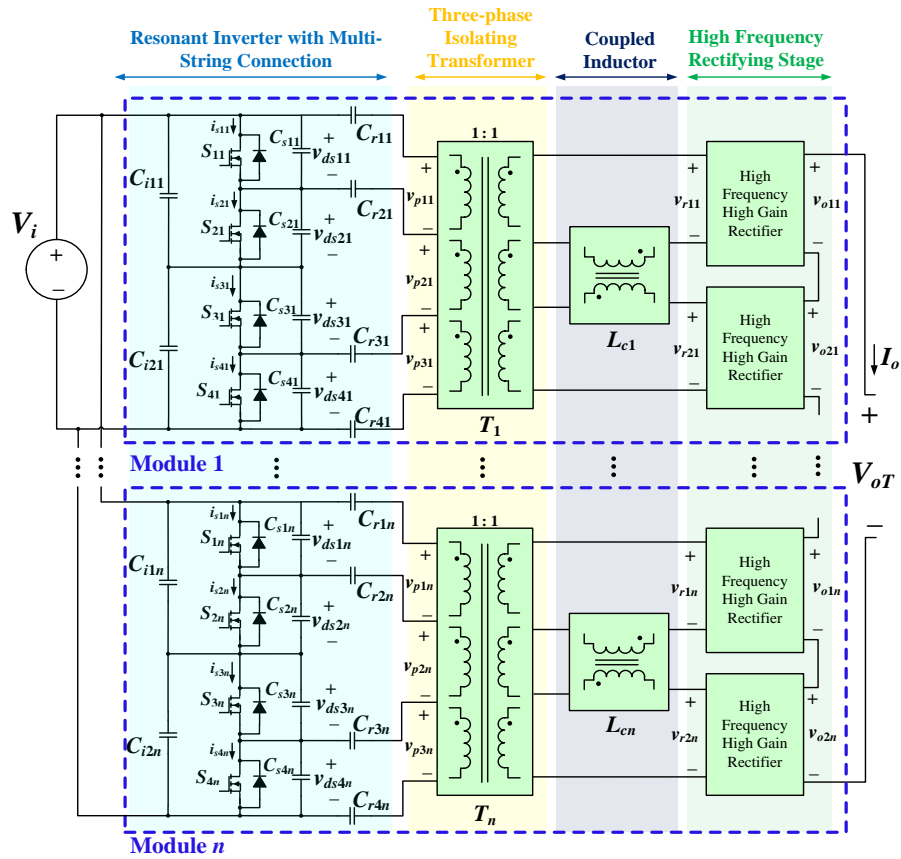


Figure 3.29– Modular MV step-up converter structure with the proposed circuit module

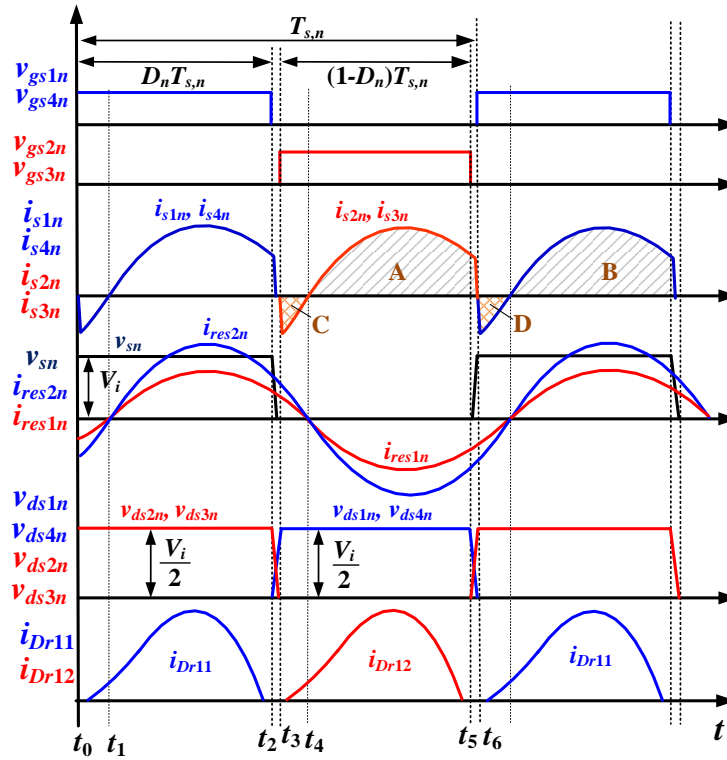


Figure 3.30– Operating waveforms of the proposed converter (only one module)

As discussed in 1.4.1.3, the main drawback of the dc-dc converters with the coupled inductors is the damaging effects of the leakage inductance, i.e., voltage ringing and high spiking on semiconductors. However, in the proposed converter the leakage inductance of the coupled inductor is used to benefit the performance as it incorporates with the series capacitors and magnetizing inductance of the transformer to form a resonant circuit. By operating all the resonant circuit modules above resonance, the *CLL* resonant circuit can produce a soft-switching condition for all the semiconductor switches and the rectifying diodes over a wide range of operating points.

In the proposed circuit, a full-bridge voltage doubler rectifier is employed at the output stage of the converter. The main advantages of this full-wave voltage multiplier rectifier (VMR) over the half-wave VMR are the reduced voltage stress on output capacitors (half of the output voltage) and the balanced voltage stress on both capacitors and diodes [81]. It should be also noted that the voltage across the input capacitors are maintained balanced using the technique discussed in section 2.4.3.7. The operating principles of the proposed converter can be analyzed according to the operating waveforms shown in Figure 3.30. The key operating stages of one module of the proposed circuit within a switching cycle are analyzed as shown in Figure 3.31 with the red arrows indicating the flow of the different currents in the converter.

**$[t_0 < t < t_1]$ :** Prior to this interval, snubber capacitor  $C_{s1n}$  and  $C_{s4n}$  have been discharged to the resonant circuit and the voltage across these capacitors have reached zero. At the beginning of this stage  $t_0$ , the gate signals are applied to  $S_{1n}$  and  $S_{4n}$ . Due to the negative portion of  $i_{res2n}$  at this interval, switch currents  $i_{s1n}$  and  $i_{s4n}$  (which are equal to  $i_{res2n}$ ) are negative. Hence, the antiparallel diodes of  $S_{1n}$  and  $S_{4n}$  are forced to turn ON. Meanwhile, the voltage across  $S_{2n}$  and  $S_{3n}$  are clamped to the dc-link capacitors ( $C_{i1n}$ ,  $C_{i2n}$ ) voltage, which is half of the input voltage ( $V_i/2$ ).

**$[t_1 < t < t_2]$ :** At  $t_1$ ,  $i_{res1n}$  and  $i_{res2n}$  become positive. The negative current flowing through antiparallel diodes of  $S_{1n}$  and  $S_{4n}$  in the previous stage, now become positive, and so  $S_{1n}$  and  $S_{4n}$  are turned ON under zero voltage condition. This implies zero turn-ON losses for  $S_{1n}$  and  $S_{4n}$ .

**$[t_2 < t < t_3]$ :** At the beginning of this interval all the switches are OFF. The snubber capacitors  $C_{s2n}$  and  $C_{s3n}$  start discharging and by the end of this interval  $C_{s2n}$  and  $C_{s3n}$  will be completely discharged into the resonant circuit. This allows the snubber capacitors to be large enough to

significantly decrease the turn-OFF losses of the switches. Meanwhile, snubber capacitors  $C_{s1n}$  and  $C_{s4n}$  that are already discharged into the resonant circuit at  $[t_5 < t < t_6]$  start to charge slowly. As a result, voltage across  $S_{1n}$  and  $S_{4n}$  begin to rise slowly and near ZCS turn-OFF is achieved for  $S_{1n}$  and  $S_{4n}$  at  $t_2$ .

**$[t_3 < t < t_4]$ :** at  $t_3$ , the gate signals are applied to  $S_{2n}$  and  $S_{3n}$ , and the positive  $i_{res2n}$  flows through the antiparallel diodes of  $S_{2n}$  and  $S_{3n}$ . The voltages across  $S_{1n}$  and  $S_{4n}$  remain at  $V_i/2$ . At the same time, the output voltages of the resonant circuits reverse their polarities and  $D_{r12}$  and  $D_{r21}$  start conducting.

**$[t_4 < t < t_5]$ :** at  $t_4$ , the positive  $i_{res2n}$  in the previous stage becomes negative, and the antiparallel diodes of  $S_{2n}$  and  $S_{3n}$  stop conducting.  $S_{2n}$ ,  $S_{3n}$  then turn ON under ZVS condition.

**$[t_5 < t < t_6]$ :** at  $t_5$ , the gating signal of  $S_{2n}$  and  $S_{3n}$  ( $v_{gs2n}$  and  $v_{gs3n}$ ) are removed. Snubber capacitors across switch  $S_{2n}$  and  $S_{3n}$  ( $C_{s2n}$  and  $C_{s3n}$ ) start to charge. This allows the voltage across  $S_{2n}$  and  $S_{3n}$  to rise slowly, allowing close to ZCS turn-OFF to be achieved for  $S_{2n}$  and  $S_{3n}$ . Due to the negative portion of  $i_{ses2n}$  at  $t_5$ , the snubber capacitors ( $C_{s1n}$  and  $C_{s4n}$ ) begin to discharge into the resonant circuit. This stage ends when the gate signals are applied to  $S_{1n}$  and  $S_{4n}$  again.

### 3.2.2 Proposed Converter Analysis

In the proposed converter, the power is transferred from the input to the output by three resonant sub-modules. Hence, the currents flowing through the resonant circuits ( $i_{res1n}$ ,  $i_{res2n}$ ) are nearly sinusoidal. This allows classical fundamental harmonic approximation (FHA) to obtain the

characteristics of the circuit; in which only the fundamental component of the square wave voltages are assumed to contribute to the power transfer. Based on FHA, the equivalent circuit of one module is derived, as shown in Figure 3.32. This circuit is used to perform the steady state analysis of the proposed topology, with the following assumptions:

- 1) All the components, including semiconductor switches and diodes are ideal.
- 2) The delay between the switches gating signals is neglected.
- 3) The effect of snubber capacitors is neglected.

The circuit consists of three resonant sub-modules connected to a multiwinding two-phase transformer. The input voltages to the resonant circuits are  $v_{ds1n}$ ,  $v_{sn}$ , and  $v_{ds4n}$ . The Fourier series representation of the input voltages to the resonant circuits are given by (3.41) and (3.42), where  $D_n$  represents the duty cycle;  $\theta_h$  is the phase angle that is given by (3.43),  $f_s$  is the operating switching frequency; and  $h$  represents the  $h$ th harmonics. The series capacitors  $C_{r1n} \sim C_{r4n}$  block the dc components of the resonant voltages (3.41) and (3.42). Hence, only the ac components are considered in Figure 3.32.

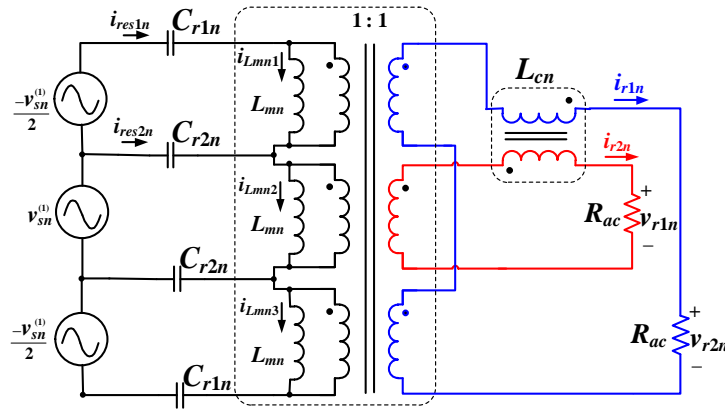


Figure 3.32– Equivalent circuit of one module in the proposed converter

$$v_{ds1n} = v_{ds4n} = \frac{V_i(1-D_n)}{2} - \sum_{h=1}^{\infty} \left( \frac{V_i}{\sqrt{2}h\pi} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_s t + \theta_h) \right) \quad (3.41)$$

$$v_{sn} = V_i D_n + \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_s t + \theta_h) \right) \quad (3.42)$$

$$\theta_h = \tan^{-1} \left( \frac{\sin(2\pi h D_n)}{1 - \cos(2\pi h D_n)} \right) = \frac{\pi}{2} - \pi D_n \quad (3.43)$$

The rms value of  $v_{ds1n}$  and  $v_{sn}$  are given by

$$V_{sn} = 2V_{ds1n} = 2V_{ds4n} = \frac{V_i}{\pi} \left[ \sum_{h=1}^{\infty} \frac{\sqrt{1 - \cos(2h\pi D_n)}}{h^2} \right]^{1/2} \quad (3.44)$$

A plot of (3.44) is shown in Figure 3.33. It can be observed that the maximum rms voltages  $V_{sn}$ ,  $V_{ds1n}$ , and  $V_{ds4n}$  occurs at  $D_n=0.5$ . Hence, with  $D_n=0.5$ , the first harmonic component of  $v_{ds1n}$ ,  $v_{sn}$  and  $v_{ds4n}$  can be given by the following:

$$v_{sn}^{(1)} = -2v_{ds1n}^{(1)} = -2v_{ds4n}^{(1)} = \frac{\sqrt{2}V_i}{\pi} \quad (3.45)$$

To simplify the analysis of the resonant circuit, the following design parameters are introduced: the ratio of coupled to magnetizing inductance is given by  $k$ , and the ratio of resonant capacitors is defined as  $m$  as in following, respectively:

$$k = \frac{L_{cn}}{L_{mn}} \quad (3.46)$$

$$m = \frac{C_{r1n}}{C_{r2n}} \quad (3.47)$$

Open- and short-circuit conditions can be used to determine the corner and critical angular resonant frequencies in the converter. The values are then given by the following, respectively:

$$\omega_{NL} = \frac{1}{\sqrt{L_{mn} C_{r2n}}} \quad (3.48)$$

$$\omega_{SC} = \frac{1}{\sqrt{L_{eq} C_{r2n}}} \quad (3.49)$$

where  $L_{eq}$  in (3.49) is the equivalent inductance value of the parallel combination of the coupled ( $L_{cn}$ ) and transformer magnetizing inductances ( $L_{mn}$ ). The normalized angular operating frequency ( $\omega_r$ ) is given by (3.51), where  $\omega_{sw}$  represents the angular operating frequency

$$L_{eq} = \frac{L_{cn} L_{mn}}{L_{cn} + L_{mn}} = \frac{k}{k+1} L_{mn} \quad (3.50)$$

$$\omega_r = \frac{\omega_{sw}}{\omega_{NL}} \quad (3.51)$$

The quality factor  $Q_n$  of the circuit is defined by (3.52), where  $R_{ac}$  represents the equivalent load resistance at the output of the resonant circuits. If KVL is applied around the outermost loop in Figure 3.32, the relationship between  $v_{r1n}$  and  $v_{r2n}$  can be obtained as shown in (3.54).

$$Q_n = \frac{L_{mn} \omega_{NL}}{R_{ac}} \quad (3.52)$$

$$R_{ac} = \frac{R_L}{\pi^2} \quad (3.53)$$

$$(v_{r1n} + v_{r2n})(jkQ_n\omega_r + 1) + \frac{2Q_n}{jm} \left[ v_{r1n} \left( \frac{k}{2} + 1 + \frac{1}{j2Q_n\omega_r} \right) \right] = 0 \quad (3.54)$$

From (3.54) it can be realized that:

- 1)  $v_{r1n} = -v_{r2n}$
- 2)  $Q_n/m \rightarrow 0$  which means  $C_{r1n} \gg C_{r2n}$  and  $Q_n \ll 1$ .

Having voltage doubler, the output voltage can be obtained by (3.55), where  $V_{r1n}$  and  $V_{r2n}$  are the rms values of  $v_{r1n}$  and  $v_{r2n}$ , respectively.

$$V_o = \frac{\pi}{\sqrt{2}} (V_{r1n} + V_{r2n}) = \sqrt{2}\pi V_{r1n} \quad (3.55)$$

Hence, the total voltage gain can be given by the following:

$$\left| \frac{V_o}{V_i} \right| = \left| \frac{V_o}{V_{r1n}} \right| \times \left| \frac{V_{r1n}}{V_i} \right| = \frac{\sqrt{2}\pi}{2} \left[ \left( 1 - \frac{3}{\omega_r^2} \right)^2 + \left( Q_n \left( k\omega_r - \frac{3k+4}{\omega_r} \right) \right)^2 \right]^{-1/2} \quad (3.56)$$

A plot of (3.56) as a function of  $k$  and  $\omega_r$  is shown in Figure 3.34. According to this figure, with increasing  $k$ , the voltage gain is becoming more sensitive to the frequency. This makes it difficult to regulate the output voltage by variable frequency control. The ratio of transformer magnetizing current,  $I_{mn}$  to  $I_{r1n}$  can be given by (3.57). According to (3.57), as the ratio of the coupled to magnetizing inductance  $k$  increases, the circulating current increases. This can be also seen by approaching  $L_{mn}$  to zero ( $L_{mn} \rightarrow 0$ ), when all the input current will flow through the parallel branch.

$$\left| \frac{I_{mn1}}{I_{r1n}} \right| = \frac{1}{2} \sqrt{k^2 + \frac{1}{(Q_n \omega_r)^2}} \quad (3.57)$$

Therefore, to reduce the circulating current and to improve the controllability of the circuit via variable frequency control, it is desirable to select the magnetic components so that  $k$  is in the neighborhood of 1 or 2. Figure 3.35 shows the voltage gain of the converter under various

quality factor  $Q_n$  with ZVS regions. According to this figure and (3.54),  $Q_n$  is selected to be between 0.1 – 0.2 in the following design example.

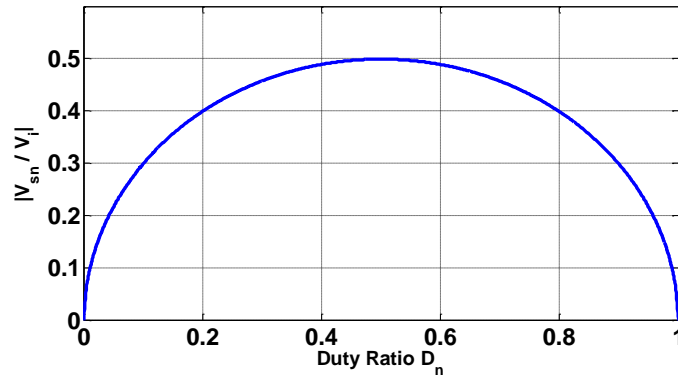


Figure 3.33– Normalized rms resonant voltage ( $V_{sn}$ ) as a function of duty ratio  $D_n$

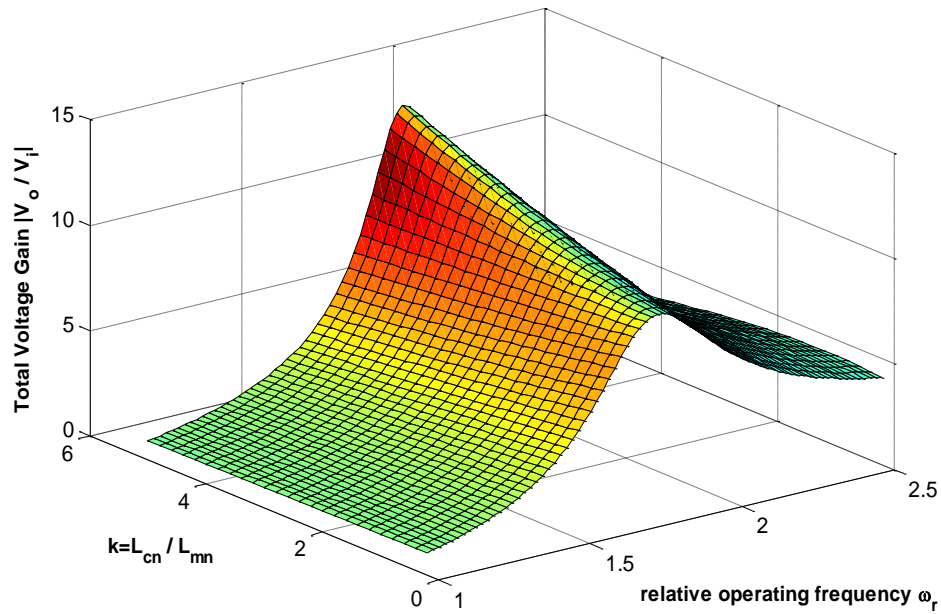


Figure 3.34– Voltage gain of the proposed converter as a function of  $k$  and  $\omega_r$

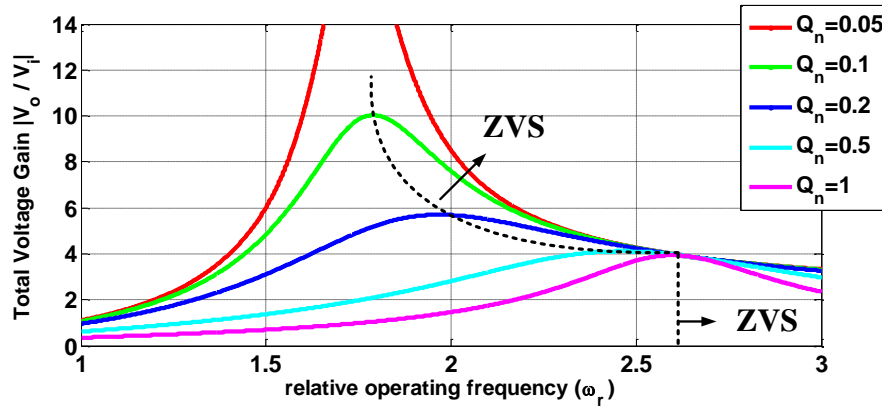


Figure 3.35– Voltage gain of the proposed circuit  $V_{sn}$  under various quality factor  $Q_n$

### 3.2.2.1 Control Principles and Voltage Balancing Technique

The control block diagram of the proposed converter is shown in Figure 3.36. The output of each module can be controlled via variable frequency control or pulse width modulation (PWM). However, in this work variable frequency control is selected to regulate the output voltage and PWM can provide a standard maximum power point tracking (MPPT) function. It should be noted that the analysis of the MPPT function is not considered in this section. The phasor model, discussed in section 2.4.4 was used to obtain the small-signal model and control-to-output transfer function. The derived model is then used to design the PI controller. The output of the discrete-time PI controller is fed to the voltage-controlled oscillator (VCO) to adjust the switching frequency of the MV converter, using a TMS320F28335 Delfino Microcontroller.

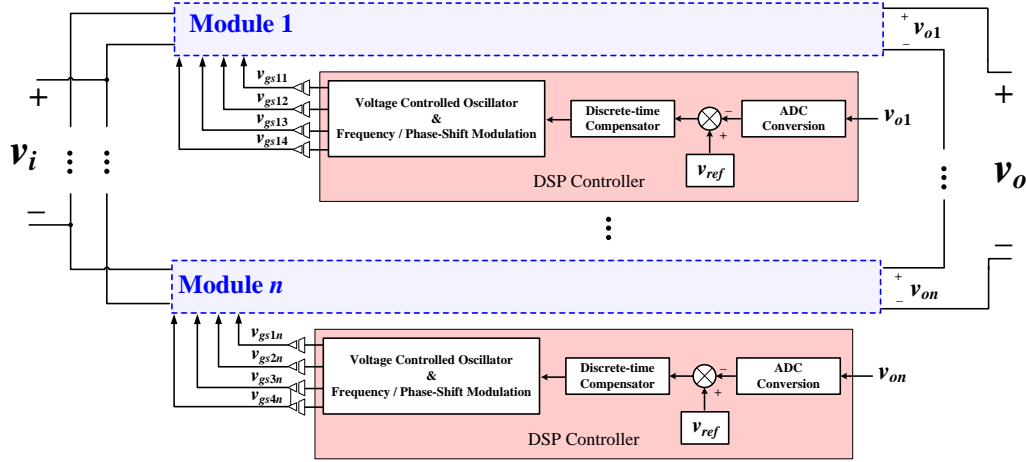


Figure 3.36– Modular control scheme with TMS320F28335 DSP controller

### 3.2.3 Power Loss Analysis

The power loss of the proposed dc-dc converter can be mainly classified to: power switch loss, diode loss, capacitors power loss, multiphase transformer and coupled inductor losses.

#### 3.2.3.1 Power Loss Analysis of the SiC MOSFETs

According to ROHM application note [82], the power losses of SiC MOSFETs mainly contain: conduction loss, switching loss, and MOSFET gate charge loss which are explained as follows:

##### 1) Conduction Loss

Conduction losses of SiC MOSFETs, caused by MOSFET on-resistance, are calculated for hatching sections *A* and *B* in the switch currents (see operating waveforms in Figure 3.30), where the switches are in the ON state

$$P_{cond\_loss} = \sum_{j=1}^4 \sum_{i=1}^n I_{Sji(rms)}^2 R_{on(sji)} \quad (3.58)$$

where  $R_{on(sji)}$  is the MOSFET on-resistance and the rms current in the switches can be obtained from the resonant current  $i_{res2n}$

$$i_{res2n} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_i}{h\pi|Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_s t + \theta_n - \varphi_{Zin}) \right) \quad (3.59)$$

where  $|Z_{in}|$  is the magnitude of the input impedance of the resonant circuit and  $\varphi_{Zin}$  is the phase angle of the input impedance. Since the harmonics components are negligible in the switching losses, only the fundamental component is considered for the calculation of the rms switch current.

$$I_{S1n} = I_{S4n} = \sqrt{\frac{1}{T_s} \int_{t_1}^{t_2} [i_{res2n}]^2 dt} = \frac{V_i}{\pi|Z_i|} \sqrt{(1 - \cos(2\pi D_n))} \times \sqrt{\left( D_n - \frac{t_1}{T_n} + \frac{\sin(2\pi D_n - 2\varphi_{Zin}) - \sin(4\pi f t_1 - 2\pi D_n - 2\varphi_{Zin})}{4\pi} \right)} \quad (3.60)$$

The maximum rms current of the switches can be calculated assuming that the switching frequency equals the resonant frequency or when  $t_1$  approaches zero ( $t_1 \rightarrow 0$ ) and consequently  $\varphi_{Zin} \rightarrow 0$

$$I_{S1n(max)} = I_{S4n(max)} = \frac{V_i}{\pi|Z_i|} \sqrt{(1 - \cos(2\pi D_n)) \left( D_n + \frac{\sin(2\pi D_n)}{2\pi} \right)} \quad (3.61)$$

Similarly, rms current of  $S_{2n}$  and  $S_{3n}$  and their maximums can be obtained by

$$I_{S2n} = I_{S3n} = \sqrt{\frac{1}{T_s} \int_{t_4}^{t_5} [i_{res2n}]^2 dt} = \frac{V_i}{\pi|Z_i|} \sqrt{(1 - \cos(2\pi D_n))} \times \sqrt{\left( 1 - \frac{t_4}{T_n} - \frac{\sin(2\pi D_n + 2\varphi_{Zin}) + \sin(4\pi f t_4 - 2\pi D_n - 2\varphi_{Zin})}{4\pi} \right)} \quad (3.62)$$

$$I_{S2n(max)} = I_{S3n(max)} = \frac{V_i}{\pi|Z_i|} \sqrt{(1 - \cos(2\pi D_n)) \left( 1 - D_n - \frac{\sin(2\pi D_n)}{2\pi} \right)} \quad (3.63)$$

## 2) *Switching loss*

The switching losses of the SiC MOSFETs can be expressed as

$$P_{sw\_loss} = \sum_{j=1}^4 \sum_{i=1}^n \left[ \frac{1}{2} v_{dsji}(t_{on}) \cdot i_{sji}(t_{on}) \cdot (t_r + t_{d(on)}) \cdot f_s + \frac{1}{2} v_{dsji}(t_{off}) \cdot i_{sji}(t_{off}) \cdot (t_r + t_{d(off)}) \cdot f_s \right] \quad (3.64)$$

where  $t_r$  is the switch rise time;  $t_f$  is the switch fall time;  $t_{d(on)}$  is the turn-ON delay time;  $t_{d(off)}$  is the turn-OFF delay time; and  $f_s$  is the switching frequency. However, due to the ZVS turn-ON and near ZCS turn-OFF of the switches, the switching loss is considered zero.

## 3) *Gate charge loss*

Gate charge loss is a power loss ascribed to MOSFET gate charging. It depends on the gate electric charge (or the gate capacity) of the MOSFET and is calculated using the following formula:

$$P_{G\_loss} = \sum_{j=1}^4 \sum_{i=1}^n Q_g \cdot V_{gji} \cdot f_{sw} = \sum_{j=1}^4 \sum_{i=1}^n C_g \cdot V_{gji}^2 \cdot f_s \quad (3.65)$$

where  $Q_g$  is the gate electric charge;  $C_g$  is the gate capacity; and  $V_{gji}$  is the gate drive voltage.

### 3.2.3.2 Power Loss Analysis of the Diodes

Conduction losses of the body diodes of SiC MOSFETs in the proposed converter are considered for hatching sections *C* and *D* in the switch currents (see operating waveforms in Figure 3.30). The power losses of diodes consist of conduction losses and switching losses. The conduction losses are produced during conduction and the switching losses of diodes are caused by reverse

recovery characteristics. However, in the high-frequency voltage doublers, the smooth transition due to the ZCS turn-ON and turn-OFF of the SiC Schottky diodes, eliminate the diode switching losses.

$$P_{cond\_diode} = \sum_{i=1}^{4 \times n} U_{D0i} \cdot I_{Fi,av} + R_{Di} \cdot I_{Fi,rms}^2 \quad (3.66)$$

where  $U_{D0i}$  is the on-state zero-current voltage and  $R_D$  is the on-state resistance of the diode.

### 3.2.3.3 Power Loss Analysis of the Capacitors

The power losses of capacitors are provided by the ESR of capacitors. The ESR is related with the operating frequency in the circuit. In the proposed converter the resonant capacitors make a significant contribution to the total power loss as they block the dc components to the resonant circuit and resonant currents go through them

$$P_C = \sum_{j=1}^4 \sum_{i=1}^n ESR \cdot I_{Csji,rms}^2 \quad (3.67)$$

Based on the dissipation factor of the capacitor and the operating frequency, the ESR of each individual capacitor can be calculated

$$ESR = \tan \delta \cdot \frac{1}{2\pi f_s C_{ji}} \quad (3.68)$$

The rms current of resonant capacitors,  $I_{Csij}$ , considering only the fundamental component, can be given by

$$I_{cs2n} = I_{cs3n} = \frac{V_i}{\pi |Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)} \quad (3.69)$$

$$I_{cs1n} = I_{cs4n} = I_{in} - \frac{V_i}{\pi |Z_{in}|} \sqrt{1 - \cos(2h\pi D_n)}$$

### 3.2.3.4 Multiphase Transformer and Coupled Inductor Losses

The conduction loss of the inductor and the multiphase transformer can be expressed as

$$P_{Ind\_cond} = 2 \sum_{i=1}^n R_{Lci\_DCR} \cdot I_{Lci,rms}^2$$

$$P_{TR\_cond} = \sum_{i=1}^n R_{TR\_pri} [I_{res2i}^2 + 2I_{res1i}^2] + R_{TR\_sec} [3I_{Lci,rms}^2]$$
(3.70)

where  $R_{Lci\_DCR}$  is the dc resistance of the coupled inductor;  $R_{TR\_pri}$  is the dc resistance for the primary side of the transformer; and  $R_{TR\_sec}$  is the dc resistance for the secondary side of the transformer.  $I_{Lci,rms}$  is the rms value of the coupled inductor and the transformer secondary windings and can be given by

$$I_{Lcn,rms} = \frac{\pi}{\sqrt{2}} I_o$$
(3.71)

Moreover, the core losses of the magnetic components can be calculated by Steinmetz equation [83]:

$$P_{core} = k \cdot \Delta B^\alpha \cdot f_{sw}^\beta$$
(3.72)

where parameters  $k$ ,  $\alpha$ , and  $\beta$  are constant, and  $\Delta B$  is the peak ac flux density, which can be expressed as

$$\Delta B = \frac{V_{in} D T_n}{4 N A_e}$$
(3.73)

where  $N$  is the number of turns and  $A_e$  is window area.

### 3.2.4 Simulation, Experimental Results and Performance

Since most of the wind turbine generators currently available in North America and Europe typically have a rated output voltage in the range from 575 to 690 V<sub>AC</sub> [5], to demonstrate the functionality of the proposed converter, a commercial 1.5 MW GE wind turbine with 690 V<sub>AC</sub> platform is simulated in PSIM. After rectifying the 690 V<sub>AC</sub>, a dc-link voltage of approximately 1 kV is applied to the input of the proposed dc-dc converter. The output dc voltage ( $V_{OT}$ ) is specified to be 20 kV. In this design, four modules were employed. As discussed earlier, the voltage stress across each switch is half of the input voltage. This feature is illustrated in Figure 3.37, where ZVS turn-ON and ZCS turn-OFF were achieved for the switches (parallel-connected SiC MOSFET modules from SEMIKRON). The switching frequency at full-load was around 25.5 kHz. A duty ratio of  $D_n=0.5$  is chosen as the maximum voltage gain occurs at this duty ratio. Figure 3.38 shows the measured current and voltage waveforms across the diodes in one of the high frequency rectifying modules. It shows that ZCS turn-ON and turn-OFF are achieved for all the diodes. Voltage variation for different duty ratio is also presented in Figure 3.39.

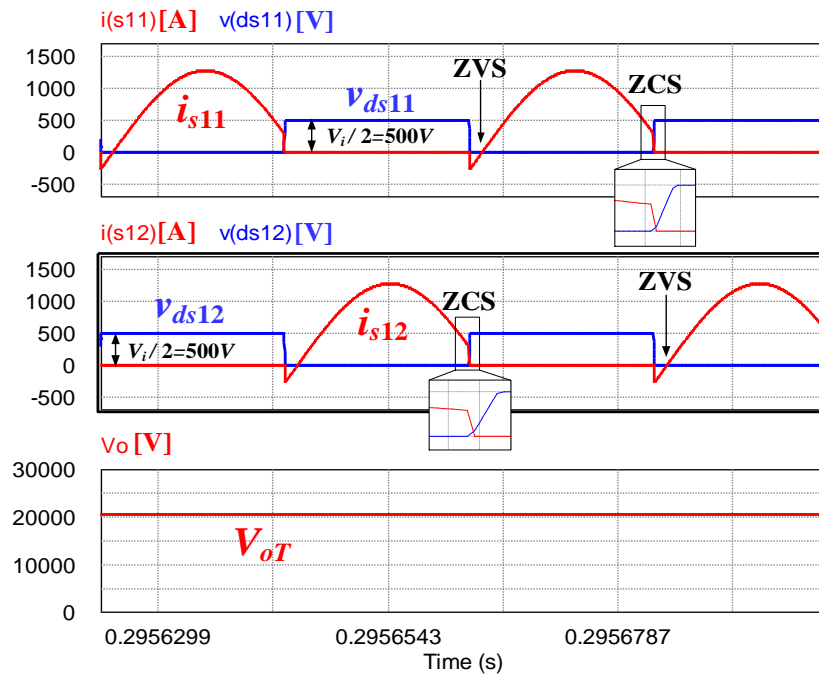


Figure 3.37– Switching waveforms and output voltage at full-load simulation

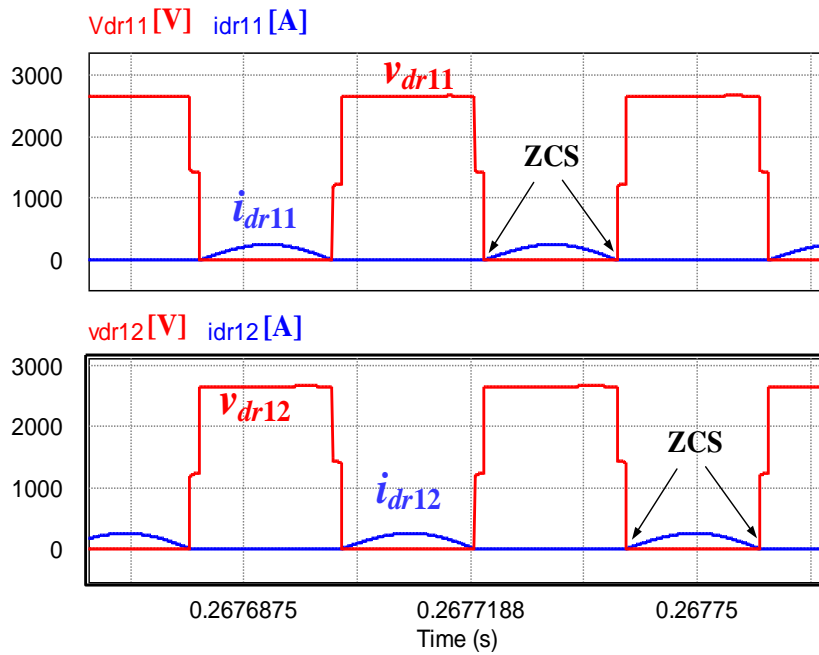


Figure 3.38– Output diode waveforms at full-load simulation

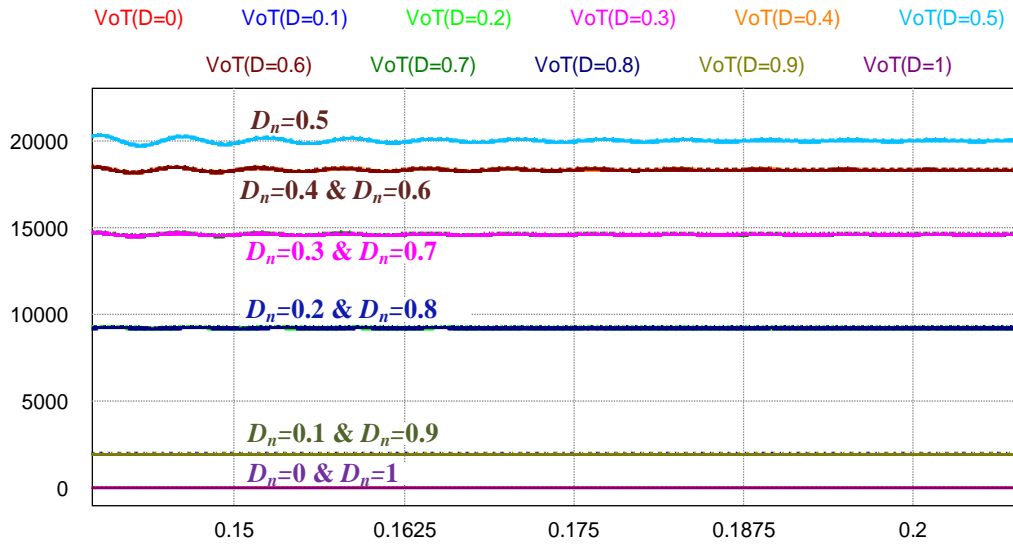


Figure 3.39– Voltage variation for different duty ratio ( $D_n$ )

To further validate the performance of the proposed topology, a laboratory-scale 2.8kW, 6kV-output proof-of-concept prototype was built and tested. To realize a dc-link voltage of 300V at the input of the converter, the front-end ac-dc rectifier is supplied from a three-phase voltage of 175V<sub>AC</sub>. The total voltage gain is the same as the simulation specifications, which is 20. The experimental prototype consists of 4 modules, with SiC MOSFETs of model: SCT3022AL from ROHM are utilized in the prototype implementation. SiC Schottky diodes are also employed for high frequency rectifying stages. The system specifications and components parameters for both simulation and prototype are summarized in Table 3.6. The design steps of the prototype components are as follows:

- 1) The equivalent ac resistance per module  $R_{ac}$  is calculated from the following:

$$R_{ac} = \frac{1}{4\pi^2} \frac{V_o^2}{P_o} = 325 \Omega \quad (3.74)$$

2) The switching frequency at full-load is taken as 26.5 kHz. According to (3.56) and (3.57), to minimize the circulating current and to achieve the desired voltage gain,  $k$  and  $Q_n$  are chosen to be 1.1 and 0.14 respectively. With respect to the duty ratio  $D_n$ , the maximum voltage gain occurs at  $D_n=0.5$ . According to (3.56),  $\omega_r$  is then calculated:  $\omega_r=2.2$ .

$$\omega_{NL} = \frac{2\pi f_{sw}}{\omega_r} = 75.7 \times 10^3 \text{ rad/sec} \quad (3.75)$$

$$L_{mn} = \frac{R_{ac} Q_n}{\omega_{NL}} = 600 \mu H \quad \text{chosen : } 590 \mu H \quad (3.76)$$

3) Consequently,  $L_{cn}=649 \mu H$  and  $C_{r2n}$  can be given by the following:

$$C_{r2n} = \frac{1}{\omega_{NL}^2 L_{mn}} = 296 nF \quad \text{chosen : } 300 nF \quad (3.77)$$

4) And finally with  $m=10$ ,  $C_{r1n}=3.3 \mu F$ .

Regarding the implementation of the multiphase transformer and the coupled inductors, Litz wire is used. The comparison picture in Figure 3.40 indicates the significant difference between the regular LF transformers and utilized HF transformer. The detailed comparison can be found in Table 3.7. More detailed specifications of the designed high frequency transformer are also presented in Table 3.8.

Table 3.6– Specifications and Components Used in the Simulation and the Laboratory-Scale Prototype

System Specifications		
	Simulation	Prototype
Rated power ( $P_o$ )	1.5MW	2.8kW
Input 3-phase voltage	690V <sub>AC</sub>	175V <sub>AC</sub>
DC-link voltage ( $V_i$ )	1kV <sub>DC</sub>	0.3kV <sub>DC</sub>
Output MVdc ( $V_{oT}$ )	20kV <sub>DC</sub>	6kV <sub>DC</sub>
Total voltage gain	20	20
Number of modules ( $n$ )	4	4
Per module output voltage ( $V_o$ )	5kV <sub>DC</sub>	1.5kV <sub>DC</sub>
Switching freq. $f_s$ (at full-load)	~25.5kHz per module	~26.5kHz per module
Circuit Components Parameters (Per Module)		
	Simulation	Prototype
SiC MOSFETs $S_{1n} \sim S_{4n}$	SKM500MB120SC (SEMIKRON) (1.2kV, 541A, 3.75m $\Omega$ )	SCT3022AL (ROHM) (650V, 93A, 22m $\Omega$ )
Snubber capacitors $C_{s1n} \sim C_{s4n}$	ECW-F6303HL (30nF, 630V <sub>DC</sub> )	R46 series (10nF, 560V <sub>DC</sub> )
Input capacitors $C_{i1} \sim C_{i2}$	C44AJGR6100ZA0J (100uF, 700V <sub>DC</sub> )	EZP-E50107MTA (100 $\mu$ F, 500V <sub>DC</sub> )
Resonant capacitors $C_{r1n}, C_{r4n}$ $C_{r2n}, C_{r3n}$	B25838T335K4 3.3uF 300nF	JBH2, N11530 3.3uF, 304V <sub>AC</sub> 300nF, 1.6kV <sub>DC</sub>
Multi-windings transformer $L_{mn}$	400uH (1:1)	590uH (1:1), 31m $\Omega$ N87 Ferrite Core
Coupled inductor $L_{cn}$	680uH (1:1)	639uH (1:1), 58m $\Omega$ N87 Ferrite Core
SiC diodes $D_{11} \sim D_{22}$	MSC030SDA120B SiC Schottky Diode (1.2kV, 65A)	GP2D005A170B SiC Schottky Diode (1.7kV, 5A)
Output capacitors $C_{11} \sim C_{22}$	B25856K7505K3 (5uF, 3kV <sub>DC</sub> )	B32774D4106K, (1 $\mu$ F, 1.3 kV <sub>DC</sub> )

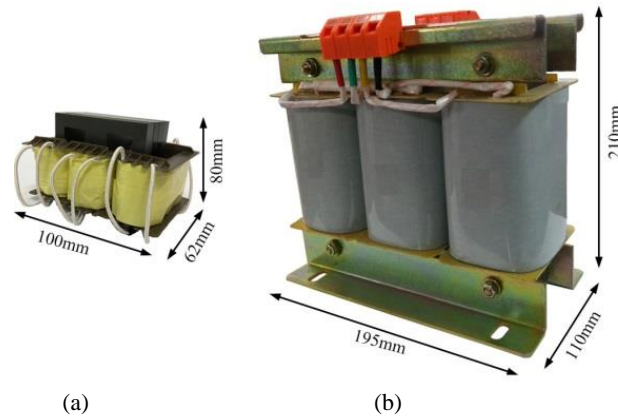


Figure 3.40– Comparative photo of (a) 25kHz HF transformer utilized in the proposed converter, and (b) 50/60Hz LF transformer [84]

Table 3.7– Line Frequency and High Frequency Transformers Size Comparison

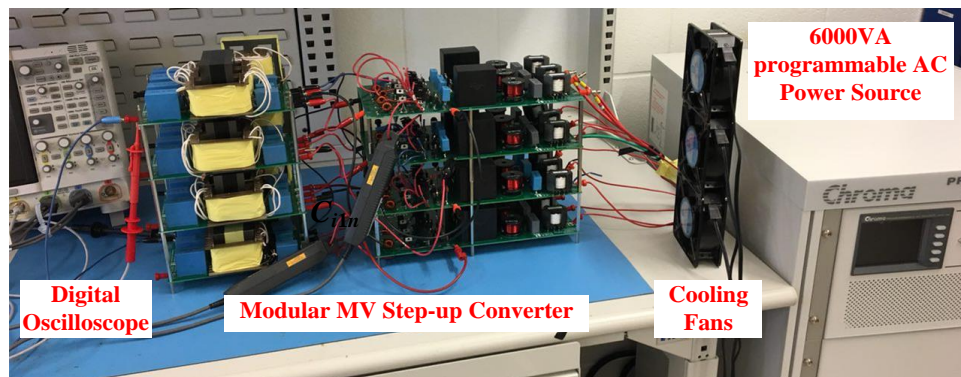
	Power	Turns-Ratio	Freq.	Dimensions	Weight
Line freq. Transformer	1kVA	1:1	50/60 Hz	195×110×210 mm <sup>3</sup>	14.5kg
Proposed Circuit Transformer	1kVA	1:1	20~30 kHz	100×62×80 mm <sup>3</sup>	1.08kg

Table 3.8– High Frequency Transformer Specifications Utilized in the Proposed Converter

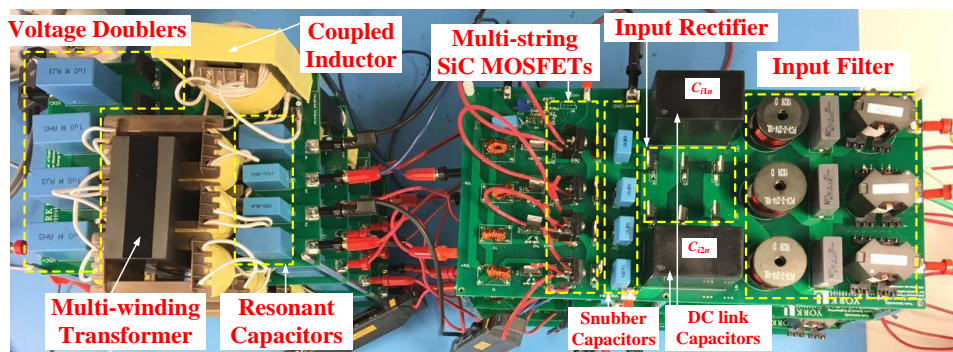
Core Material	Flux density ( $B$ )	Relative effective permeability ( $\mu_e$ )	Effective magnetic cross section $A_e$	Turns	Litz wire	Magnetizing Inductance	Parasitic Resistance
N87 Ferrite Core (TDK)	320mT	1680	390 mm <sup>2</sup>	12/12	0.050mm ×1000 strands	590μH	33mΩ

A picture of the experimental prototype is shown in Figure 3.41. The experimental waveforms per module are then illustrated in Figure 3.42– Figure 3.47. Figure 3.42 shows the input and output voltages of the high frequency voltage doublers. The output dc voltage of one module is measured to be 1.51 kV. The output voltage of each voltage doubler is observed to be almost balanced, with an error of 0.13%. Figure 3.43 shows the soft switching performance of the SiC switches in one module of the proposed converter. This figure shows that the proposed

converter can maintain ZVS turn-ON and near ZCS turn-OFF in both set of switches. Currents going through the resonant circuits are shown in Figure 3.44. Figure 3.45 illustrates the voltage doubler diodes switching waveforms, which show that the rectifier demonstrates smooth transition due to the ZCS turn-ON and turn-OFF of the SiC Schottky diodes. It is also evident that there are no voltage spikes across the output diodes. Hence, the commutations of the diodes are almost lossless.



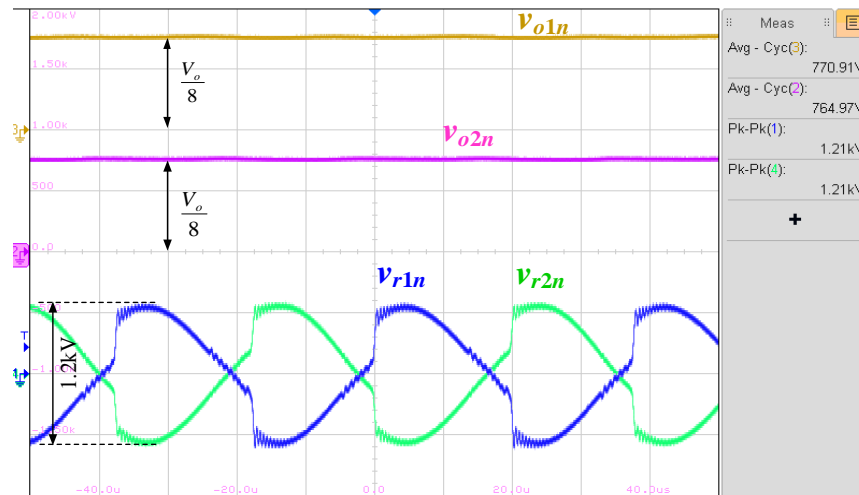
(a)



(b)

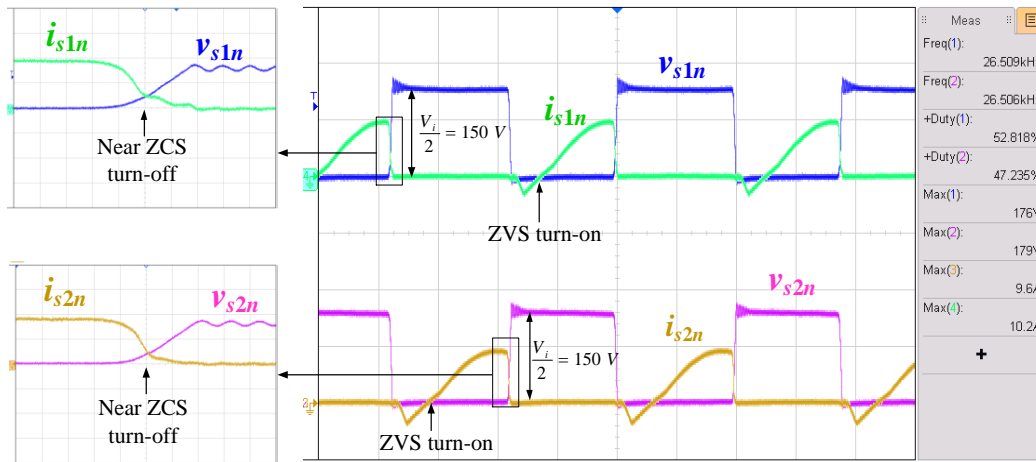
Figure 3.41– (a) Experimental set-up and (b) prototype picture

Figure 3.46 shows the input voltages of the multiphase transformer. The output voltage and input ac voltages are shown in Figure 3.47. The power loss breakdown of the key components in the prototype is illustrated in Figure 3.48. It is observed that the SiC MOSFETs exhibit 28% of the total power losses. This is mainly due to the conduction losses in the switches. The overall efficiency can be improved by choosing SiC switches with much lower  $R_{on}$ . The simulation and prototype efficiency for various power levels is shown in Figure 3.49. A peak efficiency of 97.6% was measured for the prototype and efficiency of 98.2% and 98.9% was obtained from 1.5 MW and 2.8 kW simulations, respectively.



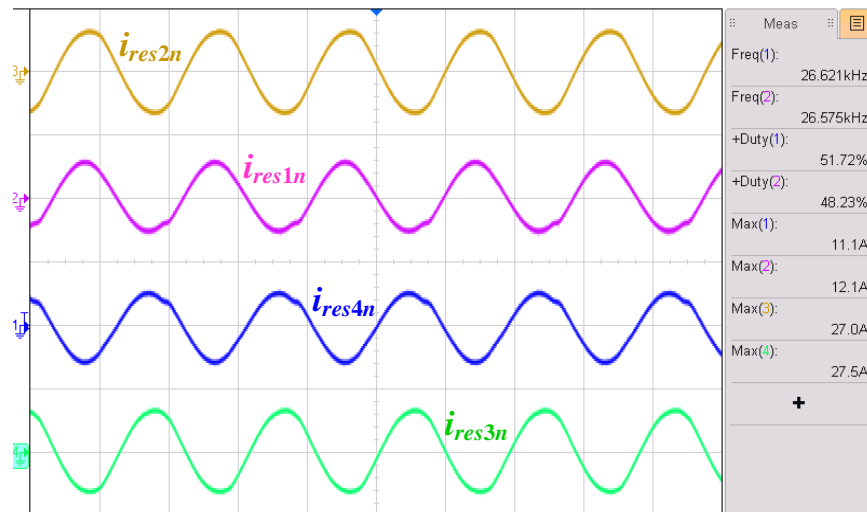
[ $v_{o1n}$ ,  $v_{o2n}$ ,  $v_{r1n}$ ,  $v_{r2n}$ : 500V/div; time: 10μs/div]

Figure 3.42– Input and output voltages of the voltage doublers in one module



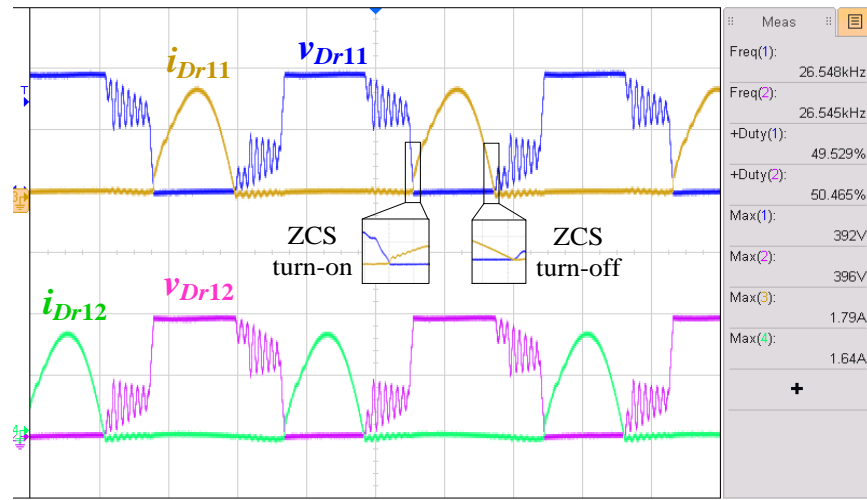
[ $v_{s1n}$ ,  $v_{s2n}$ : 100V/div;  $i_{s1n}$ ,  $i_{s2n}$ : 10A/div; time: 10 $\mu$ s/div]

Figure 3.43– Measured switching waveforms in one module



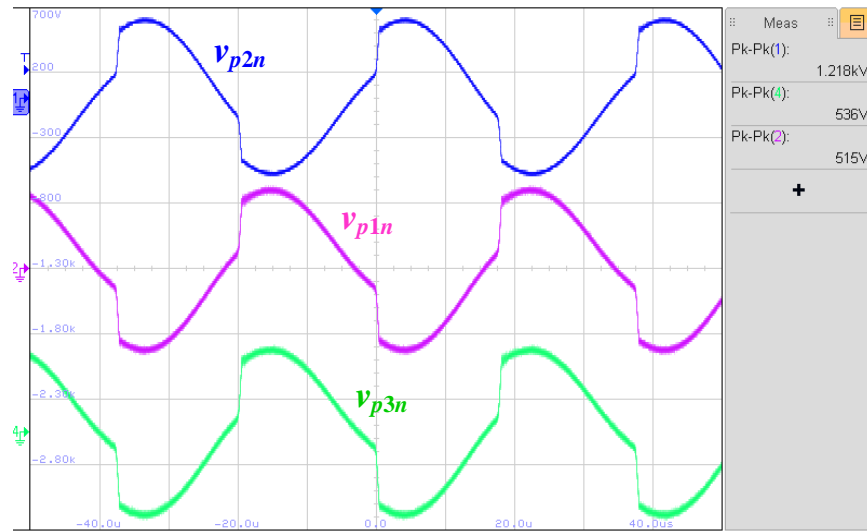
[ $i_{res1n}$ ,  $i_{res4n}$ : 20A/div;  $i_{res2n}$ ,  $i_{res3n}$ : 40A/div; time: 20 $\mu$ s/div]

Figure 3.44– Measured resonant currents of one module



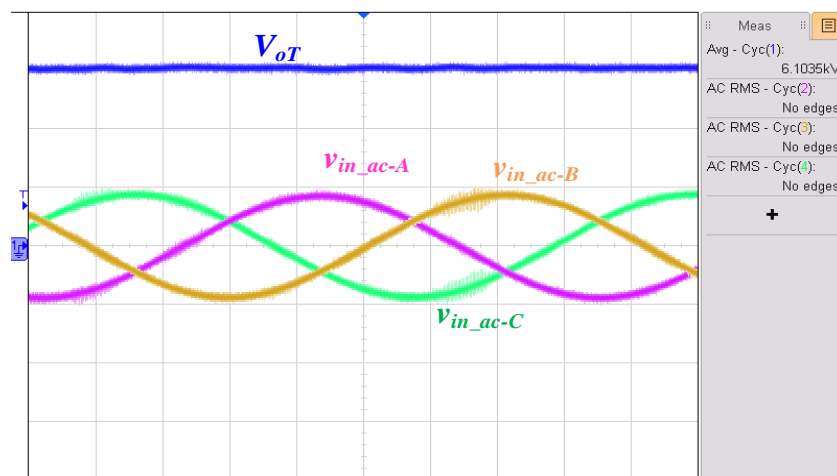
[ $v_{Dr11}$ ,  $v_{Dr12}$ : 200V/div;  $i_{Dr11}$ ,  $i_{Dr12}$ : 1A/div; time: 10 $\mu$ s/div]

Figure 3.45– Measured current and voltages of two rectifier diodes



[ $v_{p1n}$ ,  $v_{p3n}$ : 200V/div;  $v_{p2n}$ : 500V/div; time: 10 $\mu$ s/div]

Figure 3.46– Measured input voltages of HF multiphase transformer



[ $V_{oT}$ : 2kV/div;  $v_{in\_AC-A}$ ,  $v_{in\_AC-B}$ ,  $v_{in\_AC-C}$ : 200V/div; time: 2ms/div]

Figure 3.47– Measured output voltage and input ac voltages

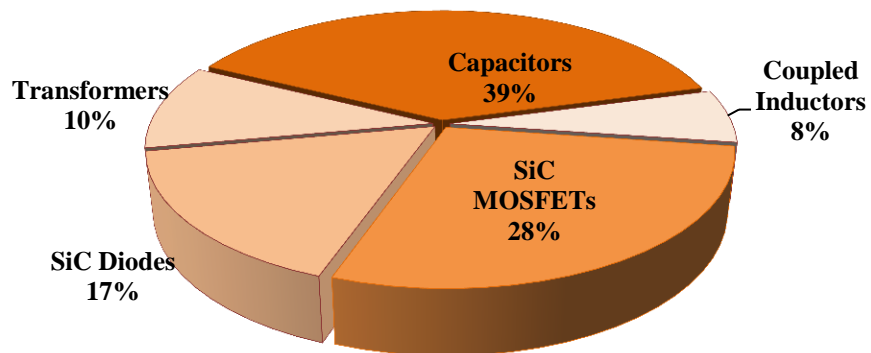


Figure 3.48– Loss breakdown of the key components in the prototype

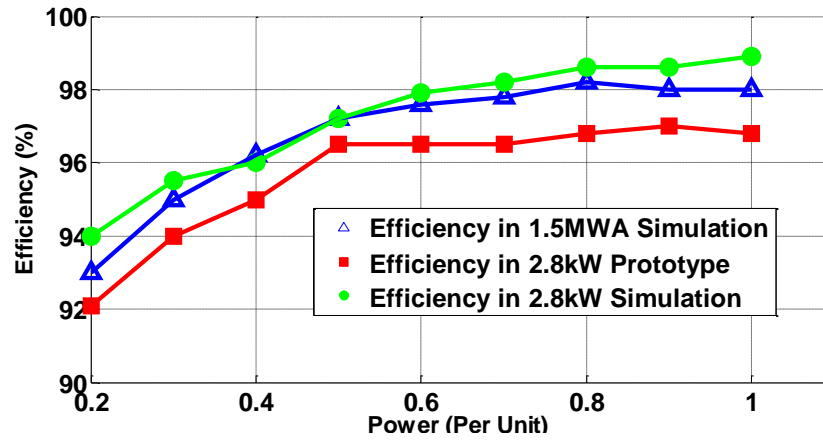


Figure 3.49– Measured efficiency for different power level

Table 3.9 illustrates the comparison between the proposed converters in this chapter with CLLC-type dual active bridge (DAB) converter, the step-up transformerless converter presented in section 2.2 and the resonant converter with two uneven transformers in [48]. The comparison is made in terms of the number of passive and active components, operating frequency, quality factor and the voltage stress of the switches. As can be seen, to achieve high voltage gain, the existing topologies either rely on step-up transformer or the resonant circuit. It was already discussed that designing a medium frequency transformer at high power level with high turns-ratio has some inherent limitations in terms of isolation and coupling effect. Achieving high voltage gain only by the resonant tank (high quality factor  $Q$ ) also suffers the drawbacks of having highly sensitive frequency control and increases the current and voltage stress of the resonant circuit components.

Table 3.9– Comparison of Existing Step-Up DC-DC Resonant Converters with the Proposed Converters

Topology		CLLC-type DAB	Resonant converter in section 2.2	Resonant converter with two uneven transformer [48]	High power resonant converter [85]	Proposed step-up converter in section 3.1	Proposed step-up converter in section 2.4	Proposed step-up converter in section 3.2
Number of	Switches	8	4	6	4	4	4	4
	Diodes	-	8	2	24	8	6	4
	Inductors	2	2	1	1	1	1	1
	Capacitors	2	6	5	5	11	11	10
	Transformer	1	2	2 (uneven transformers)	1	1 (three-winding)	3	1 (six-winding)
	Turns-ratio	(1:5)	(1:1)	(1:8)	(1:10)	(1:1:1)	(1:1)	(1:1)
Operating freq.		~10 kHz	~21 kHz	~10 kHz	~1 kHz	~18 kHz	~18 kHz	~25 kHz
Rated power		2 kW	1.1 kW	2 kW	10 kW	3.7 kW	2.8 kW	2.8 kW
Quality factor		5~10	10	~2	~200	3.5	4	7.1
Voltage stress of switches		Input: $V_i$ Output: $V_o$	$V_i/2$	$V_i$	$V_i$	$V_i/2$	$V_i/2$	$V_i/2$
Voltage gain per module		5	8	10	10	5.4	8	5
Full-load efficiency		N.A.	96.7 %	97 %	95.5 %	98.7 %	99.2 %	97.6%

### 3.3 Chapter Summary

Magnetic components are heavier and occupy more volume than any other parts in a power electronic converter. In the proposed converters in this chapter, single magnetic structures and coupled inductors were employed to further reduce the size and weight of the power conversion system. By magnetically integrating the voltage multipliers, it was shown that the output dc voltage balancing of all the converter modules could be achieved more easily without using complicated balancing control scheme. Moreover, the number of required magnetic components was also reduced, compared to the individual module's approach with separate components.

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In section 3.1, a coupled voltage-quadrupler based step-up resonant converter modules with soft-switching operation for all the semiconductor devices was presented. Since the coupled voltage-quadrupler modules were connected to the resonant circuit via a 1:1:1 high frequency transformer, high turns-ratio transformers were not required in the proposed design. Simulation results on a modular design of a SiC based 2/18 kV, 4 MW wind converter system, as well as experimental results on a laboratory-scale SiC-implemented 3.7 kW (per-module), 500 V-input proof-of-concept prototype, have been provided to validate the theoretical analysis and to highlight the merits of the proposed work. Final results have confirmed that an efficiency of at least 95% was achieved from 20% load to full-load in both simulation and experimental works.

In section 3.2, a modular SiC-based converter with a step-up module, consisting of three resonant sub-modules interconnecting with 1:1 turns-ratio multi-winding transformer and coupled current-fed voltage doubler modules, was presented for MVdc grid application in wind energy systems. By using step-up resonant circuits with a two-phase multi-winding transformer and combining it with “multistring” inverter, the proposed circuit structure completely utilizes all the switching circuits to transfer power to the output. The proposed circuit was shown to be able to achieve high voltage gain without using high turns-ratio high frequency step-up transformers. ZVS turn-ON and near ZCS turn-OFF are achieved for all switches. Simulation results have been provided on a 1.5MW wind turbine system with an output voltage of 20kV to highlight the performance of the proposed circuit. Finally, experimental results on a laboratory-scale 2.8kW prototype have been given with a peak efficiency of 97.6%.

## **Chapter 4    Proposed Three-Phase AC-DC High Voltage-Gain Converters**

In Chapter 2 and Chapter 3, several types of dc-dc step-up MV converters that do not require any high frequency step-up transformers were presented. As discussed in Chapter 1, the complete power interface for a wind turbine generator in an MVdc grid structure typically consists of two stages: an ac-dc front-end stage with PFC and a second stage step-up dc-dc converter. Based on the step-up transformerless converters presented in Chapter 2 and Chapter 3, this chapter focuses on the development of a new class of three-phase ac-dc step-up converter systems with integrated input power factor correction circuits. In particular, two different three-phase ac-dc step-up converter structures are presented in this chapter. In section 4.1, using the shared-switch concept, a three-phase boost rectifier is integrated with one of the dc-dc converters presented in Chapter 2 , which consists of step-up resonant circuits with high-gain output rectifier modules. As a result, the step-up voltage conversion function is achieved by the combination of the integrated boost rectifier and the cascaded step-up resonant circuit with high-gain output rectifier.

To reduce the number of lossy diodes required in the ac-dc front-end rectifier in the circuit presented in section 4.1, a new single-phase bridgeless ac-dc boost rectifier is first derived in section 4.2. It is then combined with the step-up dc-dc converter (from Chapter 2) to form a single-phase bridgeless ac-dc step-up converter with integrated PFC. To achieve three-phase ac-dc step-up voltage conversion, three modules of the single-phase bridgeless ac-dc step-up converter are connected in a three-phase fashion at the input, with the output of all the three converters connected in series. As a result, the number of diodes required in the overall design is less than the ac-dc converter presented in section 4.1 with the same modular approach. A high power factor is achieved at the three-phase ac input side, while at the same time, a very high voltage gain is achieved by the converter. The operating principles of each three-phase ac-dc converter topology are discussed in this chapter. The performance of each circuit is then verified through simulation results on a MW wind turbine design, as well as experimental results on a laboratory-scale kW converter design. The design procedures for each converter will also be discussed in this chapter.

## **4.1 Single-Stage PFC with HGR Approach**

The passive generator-side converters decrease the overall cost of power converters and improve the reliability of generator-side power conversion. These converters are solely used with the synchronous generators, both PMSG and WRSG in type 4 wind energy systems [86]. The diode rectifier with two-level boost converter was discussed in section 1.4.2. This configuration has been implemented in the Enercon E82, a 2MW wind turbine [5]. However, switching loss, diode

reverse-recovery loss, and voltage balancing issues of the capacitors are the main drawbacks of this converter. To address these problems, the full-bridge diode rectifier with a three-level boost converter was proposed that offers many benefits, such as reduced switching and reverse recovery losses and balancing of capacitor voltages, compared to the standard two-level boost converter [87]. This configuration is shown in Figure 4.1. The voltage rating for switches and diodes are also half of the dc-link voltage which makes it suitable for MV operation of the dc-dc stage. The three-phase diode rectifier and three-level boost converter has been utilized in both MVac [88], [89] and MVdc [26], [36] grids. Although this configuration leads to an enhanced power quality, the input current exhibits the characteristics block shape with total harmonic distortion ( $\text{THD} \approx 30\%$ ). In wind energy applications, this input current harmonics produce harmonic torque. While the input power factor suffers in this topology, the presented converter still requires a MV step-up transformer to perform step-up voltage conversion.

If the boost inductance (i.e.,  $L_b$  in Figure 4.1) is moved to the ac side, distributed over the phases, and the mode of operation is changed to DCM, the switching frequency peak values of the discontinuous phase currents follow a sinusoidal envelope [90]. This configuration is shown in Figure 4.2. It should be noted that the high quality current (more sinusoidal shape) is only achievable at high voltage ratio (when the ratio of the output dc voltage ( $V_{dc}$ ) to the generator voltage ( $v_{an}$ ) is higher than 1.76) [91]. Although this can be considered a limitation in some other applications, in wind energy systems with an MVdc grid where stepping up the voltage is a requirement, this is an advantage.

The proposed single-stage ac-dc converter in this section is formed by integrating the three-phase boost rectifier shown in Figure 4.2 with the dc-dc converters presented in Chapter 2 and Chapter 3.

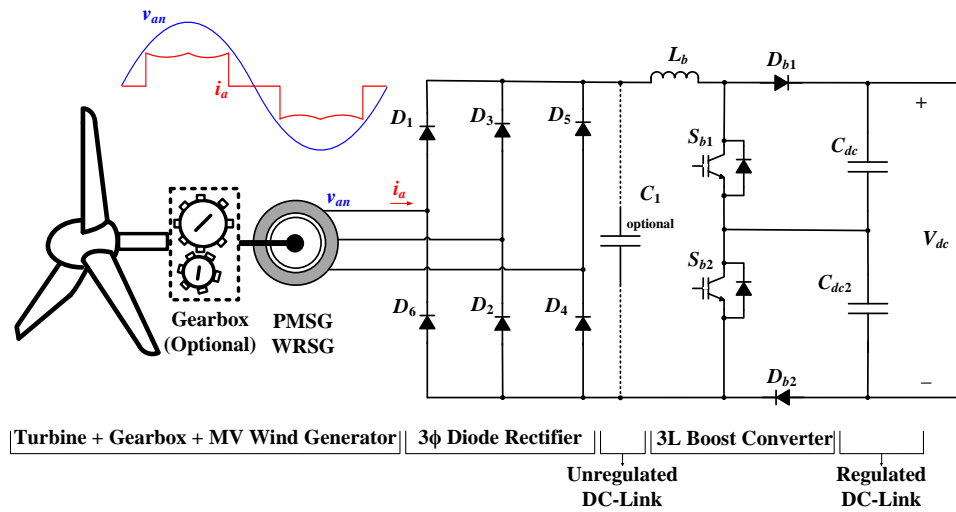


Figure 4.1– Type 4 WECS with 3 $\phi$  diode bridge rectifier and 3L boost converter operating in CCM

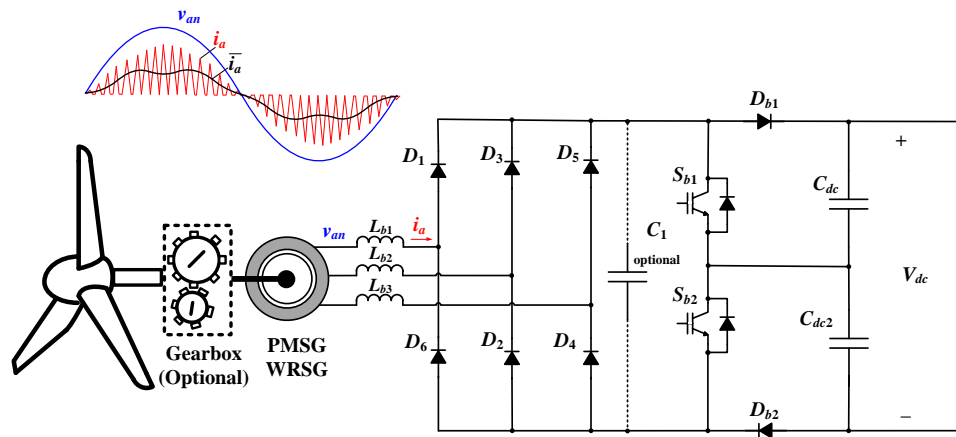
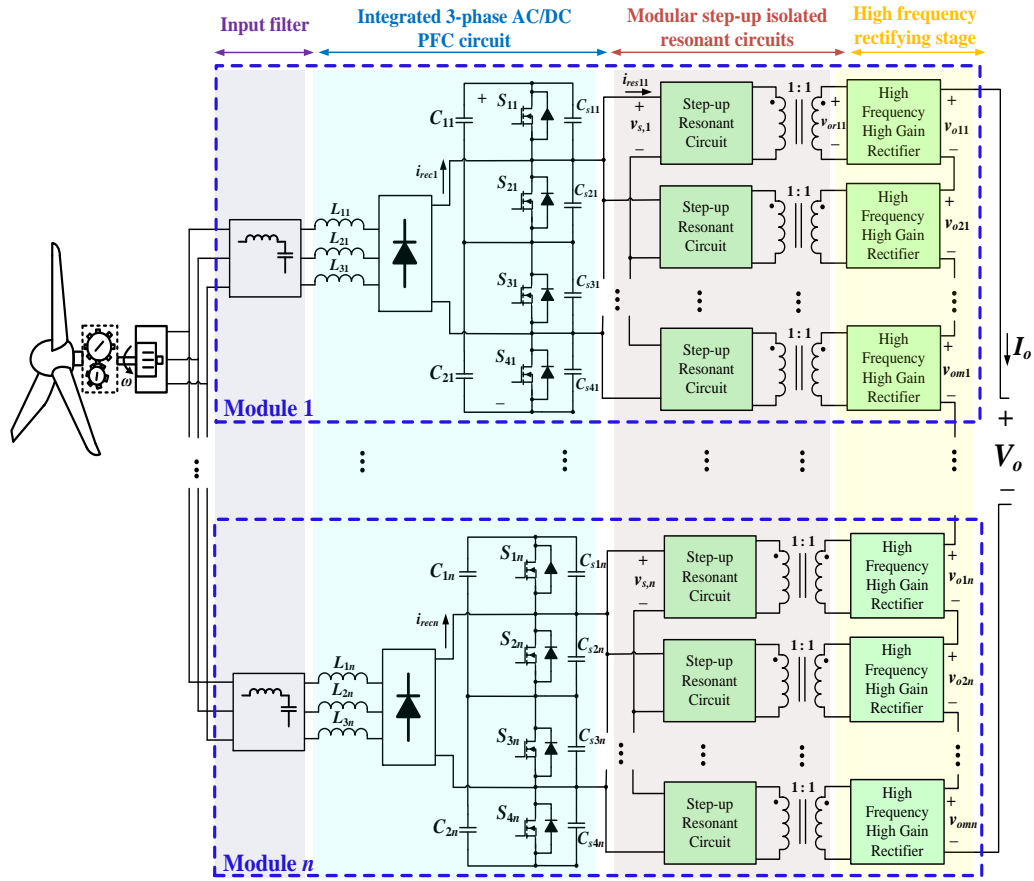


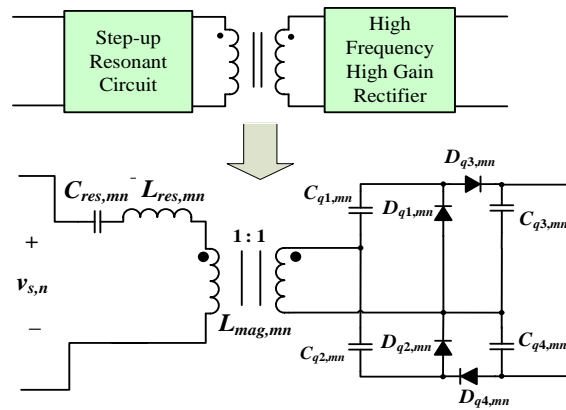
Figure 4.2– Type 4 WECS with 3 $\phi$  diode bridge rectifier and 3L boost converter operating in DCM with boost inductor is shifted to the ac side

### 4.1.1 Circuit Description of the Proposed Converter

The general block diagram of the proposed modular ac-dc step-up converter configuration is shown in Figure 4.3. Each module in the proposed converter is derived by combining the three-phase boost rectifier, modular isolated resonant circuits and high frequency high voltage-gain rectifier modules together, where  $L_{1n}$ ,  $L_{2n}$ , and  $L_{3n}$  are the three-phase boost inductors where  $n$  represents the  $n$ th module in the converter. The high frequency inverter in each module consists of “multiple string” of switches to reduce the voltage stress across each switch to half of the dc-link voltage. In each module, the inverter circuit consists of four switches,  $S_{1n}$ ,  $S_{2n}$ ,  $S_{3n}$  and  $S_{4n}$  such that switch pair  $(S_{1n}, S_{4n})$  and switch pair  $(S_{2n}, S_{3n})$  operate in complementary fashion, with switches  $(S_{1n}, S_{4n})$  turn ON during the interval  $D_n T_{s,n}$  and switches  $(S_{2n}, S_{3n})$  turn ON during the interval  $(1-D_n)T_{s,n}$ , where  $D_n$  and  $T_{s,n}$  represent the duty ratio and the period of the  $n$ th module of the converter, respectively. By operating all the resonant circuit modules above resonance and to ensure that the boost inductor currents always stay below continuous conduction mode (CCM), all switches in the proposed circuit are able to maintain zero voltage switching (ZVS) turn-ON over a wide range of operating points. By employing an *LLC* resonant circuit, the proposed topology takes on the inherent characteristics of a series resonant converter at full-load, which results in less circulating current in the resonant circuit. And as the load decreases further, the converter exploits the characteristics of parallel resonant converter to maintain ZVS and output voltage regulation for a wider range of operating points. The detailed discussion on the voltage quadrupler rectifier will be provided in section 4.1.2.4.



(a)



(b)

Figure 4.3– Proposed modular MV step-up ac-dc step-up converter structure

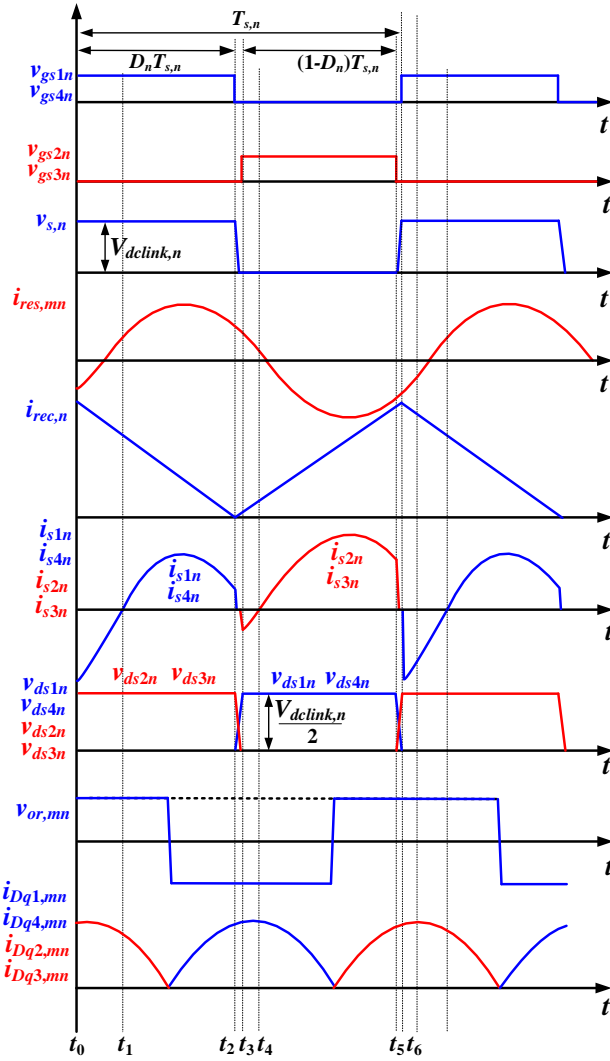


Figure 4.4– Operating waveforms of the proposed converter with only one module

For illustration purpose, the key operating waveforms of the proposed converter with one module is shown in Figure 4.4, where  $D_n$  represents the duty cycle of  $S_{1n}$  and  $S_{4n}$ , with  $S_{2n}$  and  $S_{3n}$  operating with a duty ratio of  $(1-D_n)$ . The key operating stages of one module of the proposed circuit (i.e., the  $n$ th module) within a switching cycle can be analyzed as shown in Figure 4.5, with the red arrows indicating the flow of the different currents in the converter:

**[ $t_0 < t < t_1$ ]:** Prior to this interval,  $C_{s1n}$  and  $C_{s2n}$  have been discharged to the resonant circuit and the voltage across these capacitors have reached zero. At the beginning of this stage  $t_0$ , the gate signals are applied to  $S_{1n}$ ,  $S_{4n}$ . Due to the positive current of  $i_{rec,n}$  and the negative portion of the resonant current  $i_{res,mn}$ , currents  $i_{s1n}$  and  $i_{s4n}$  are equal to the difference between  $i_{rec,n}$  and  $i_{res,mn}$ , which results in a negative current. Hence, the antiparallel diodes of  $S_{1n}$  and  $S_{4n}$  turn ON. Meanwhile, the voltage across  $S_{2n}$  and  $S_{3n}$  are equal to the capacitor ( $C_{1n}$  or  $C_{2n}$ ) voltage, which is equal to  $V_{dclink,n}/2$ , where  $V_{dclink,n}$  is dc-link voltage across capacitors  $C_{1n} + C_{2n}$ . This stage ends when  $i_{rec,n}$  equals to  $i_{res,mn}$ .

**[ $t_1 < t < t_2$ ]:** At  $t_1$ ,  $i_{res,mn}$  becomes greater than  $i_{rec,n}$ , the negative current flowing through antiparallel diodes of  $S_{1n}$  and  $S_{4n}$  in the previous stage, now become positive, and so  $S_{1n}$  and  $S_{4n}$  are turned on under ZVS. This implies zero turn-ON losses for  $S_{1n}$  and  $S_{4n}$ . During this interval, while  $S_{1n}$  and  $S_{4n}$  remain ON, the resonant circuit output voltage ( $v_{ormn}$ ) becomes negative, and hence  $i_{rmn}$  become negative and as a consequence  $D_{q1,mn}$ ,  $D_{q4,mn}$  are turned ON under ZCS.

**[ $t_2 < t < t_3$ ]:** At the beginning of this interval all the switches are OFF, the difference between  $i_{rec,n}$  and  $i_{res,mn}$  flows through the snubber capacitors. As it will be explained in the interval  $[t_5 < t < t_6]$ ,  $C_{s1n}$  and  $C_{s4n}$  are already discharged into resonant circuit. This allows using comparatively large snubber capacitors. As a result, voltage across  $S_{1n}$  and  $S_{4n}$  begin to rise slowly and ZCS turn-OFF is achieved for  $S_{1n}$  and  $S_{4n}$  at  $t_3$ .

**[ $t_3 < t < t_4$ ]:** At  $t_3$ , the gate signals are applied to  $S_{2n}$  and  $S_{3n}$ . since  $i_{res,mn}$  is greater than  $i_{rec,n}$ , the difference between  $i_{rec,n}$  and  $i_{res,mn}$  flows through the antiparallel diodes of  $S_{2n}$  and  $S_{3n}$ . The voltage across  $S_{1n}$  and  $S_{4n}$  also remain at  $V_{dclink,n}/2$ .

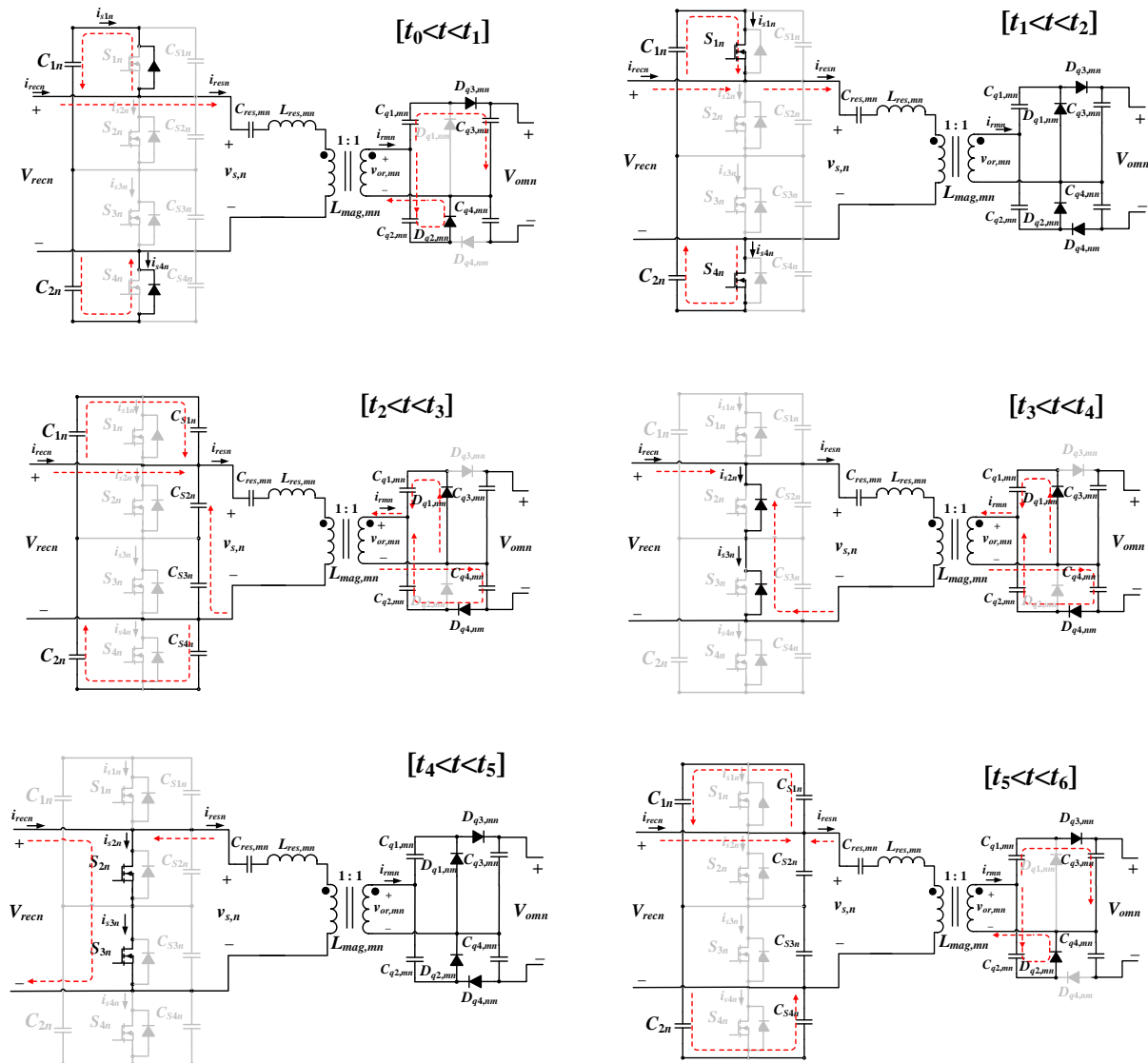


Figure 4.5– Operating stages of one module of the proposed converter (with one module of resonant circuit and voltage quadrupler)

**[ $t_5 < t < t_6$ ]:** At  $t_5$ , the gating signal of  $S_{2n}$  and  $S_{3n}$  ( $v_{gs2n}$  and  $v_{gs3n}$ ) are removed and  $C_{s2n}$  and  $C_{s3n}$  start to charge. Hence, the voltage across  $S_{2n}$  and  $S_{3n}$  rises slowly, allowing close to ZCS turn-OFF to be achieved for  $S_{2n}$  and  $S_{3n}$ . Due to the negative current of  $i_{res,mn}$ , the sum of  $i_{rec,n}$  and  $i_{res,mn}$  flows through  $C_{1n}$  and  $C_{2n}$ . At the same time, part of this negative current flows through the snubber capacitors and  $C_{s1n}$  and  $C_{s4n}$  begin to discharge into resonant circuit.

## 4.1.2 Steady-State Analysis of the Proposed Circuit

### 4.1.2.1 Input Current

Three-phase boost rectifier is well-known for its capability to achieve input PFC and to draw close-to-sinusoidal line currents when it operates in discontinuous conduction mode (DCM). The detailed discussions on its operating principles have been provided in [92]. In the proposed converter, the integrated PFC stage in each module is highlighted in Figure 4.3. Each inverter circuit in Figure 4.3 also serves as the boost converter switches and diodes for the ac-dc PFC stage. Hence, high quality input currents will be drawn at the three-phase ac input. The average input current of one phase in one module of the proposed converter is given by (4.1).

$$i_{L1n} = k \cdot \frac{\sin(\omega t)}{M - \sin(\omega t)} \quad (4.1)$$

$$k = \frac{D_n^2 T_{s,n} V_{dclink,n}}{2L_{1n}} \quad (4.2)$$

where  $M$  is the ratio of the dc-like voltage to the peak line voltage ( $M = V_{dclink,n}/V_p$ );  $k$  is defined by (4.2); the phase input voltages are given by (4.3);  $V_{dclink,n}$  represents the  $n$ th module dc-link voltage; and  $V_p$  represents the amplitude of the ac input voltage.

$$\begin{aligned}
v_a &= V_p \sin(\omega t) \\
v_b &= V_p \sin(\omega t - 120^\circ) \\
v_c &= V_p \sin(\omega t - 240^\circ)
\end{aligned} \tag{4.3}$$

(4.1) indicates that the degree of input current waveform distortion and the maximum power factor achievable are functions of the ratio of  $M$ . Practically, as  $M$  increases further from 1.25, the power factor is always better than 0.95. When  $M$  starts to decrease from 1.25, the power factor starts to deteriorate rapidly [91].

#### 4.1.2.2 Voltage Gain Analysis

The overall voltage gain equation can be obtained by first analyzing each resonant circuit module. Due to the asymmetrical square voltage generated at the output of each inverter, the input voltage to the resonant circuit ( $v_{s,n}$ ) is represented by (4.4), where  $n$  represents the  $n$ th module of the converter,  $D_n = t_{on}/T_{s,n}$  = duty cycle;  $h$  represents the  $h$ th harmonics in  $v_{s,n}$  and  $\theta_h$  is the phase angle as given by (4.5).

$$v_{s,n} = V_{dclink,n} D_n + \sum_{h=1}^{\infty} \left( \frac{\sqrt{2} V_{dclink,n}}{h\pi} \sqrt{1 - \cos(2h\pi D_n)} \sin(2\pi h f_{s,n} t + \theta_h) \right) \tag{4.4}$$

$$\theta_h = \tan^{-1} \left( \frac{\sin(2\pi h D_n)}{1 - \cos(2\pi h D_n)} \right) \tag{4.5}$$

The rms value of  $v_{s,n}$  is then given by (4.6).

$$V_{s,n} = \frac{V_{dclink,n}}{\pi} \left[ \sum \frac{1 - \cos(2h\pi D_n)}{h^2} \right]^{1/2} \tag{4.6}$$

To operate the three phase boost converter in DCM, it must satisfy (4.7).

$$\frac{V_{dlink,n}}{V_p} \leq \frac{1 + \sqrt{1 + \frac{2R_{ac} T_{s,n} D_n^2}{L_{1n}}}}{2} \quad (4.7)$$

The voltage gain of each *LLC* resonant circuit is given by (4.8), where  $r_{mn} = L_{mag,mn}/L_{res,mn}$ , where the subscript  $m$  represents the  $m$ th sub-module resonant circuit in each module,  $Q_{mn}$  is the quality factor ( $Q_{mn} = \omega_{0,mn} L_{res,mn} / R_{ac,n}$ ) in each sub-module with  $R_{ac,n}$  representing the equivalent load resistance at the output of the resonant circuit,  $\omega_{0,mn}$  represents the angular resonant frequency that is given by  $\omega_{0,mn} = 1/\sqrt{L_{res,mn} C_{res,mn}}$  and  $\omega_{r,mn}$  is the relative angular frequency defined as  $\omega_{r,mn} = \omega_{s,n} / \omega_{0,mn}$ .

$$\frac{v_{or,mn}}{v_{s,n}} = \frac{1}{\sqrt{\left(1 + \frac{1}{r_{mn}} \left(1 - \frac{1}{\omega_{r,mn}^2}\right)\right)^2 + \left(Q_{mn} \left(\omega_{r,mn} - \frac{1}{\omega_{r,mn}}\right)\right)^2}} \quad (4.8)$$

The total voltage gain of each module in the proposed converter is then given by (4.9). To illustrate the relationship between the voltage gain and the relative operating frequency, an example is given in Figure 4.6 for  $Q_{mn} = 0.5$  and  $r_{mn} = 1.6$ . It should be noted that as  $r_{mn}$  decreases to below 1, the circulating energy increases within the resonant tank circuit. Hence, to maintain high circuit efficiency,  $r_{mn}$  should be greater than 1.

$$\frac{v_{o,n}}{V_p} = \frac{2 \left[ 1 + \sqrt{1 + \frac{2R_{ac} T_{s,n} D_n^2}{L_{1n}}} \right] \left[ \sum \frac{1 - \cos(2h\pi D_n)}{h^2} \right]^{1/2}}{\pi \sqrt{\left(1 + \frac{1}{r_{mn}} \left(1 - \frac{1}{\omega_{r,mn}^2}\right)\right)^2 + \left(Q_{mn} \left(\omega_{r,mn} - \frac{1}{\omega_{r,mn}}\right)\right)^2}} \quad (4.9)$$

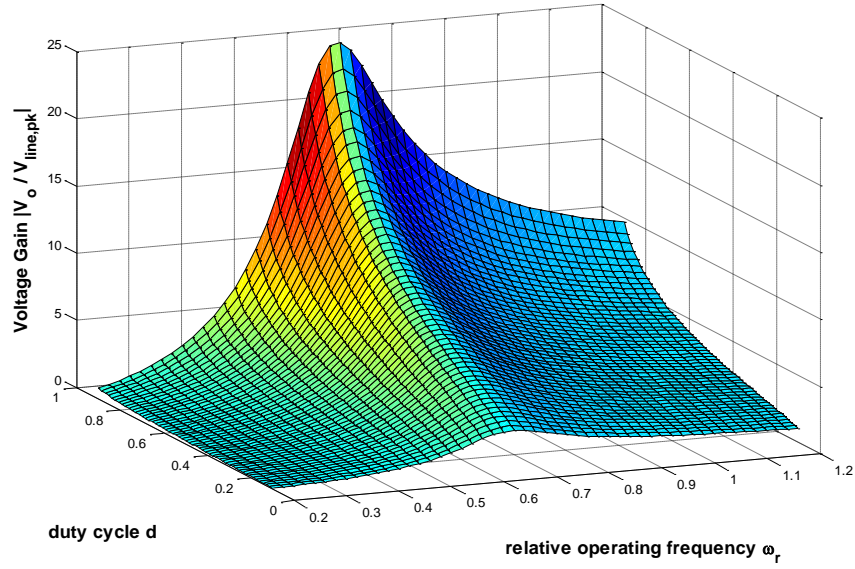


Figure 4.6– Voltage gain of the proposed converter per module

### 4.1.2.3 Resonant Current Expressions

The resonant current in each module  $i_{res,mn}$  is derived from the ac component given by (2). The final equation for  $i_{res,mn}$  is given by (4.10), where  $|Z_{i,mn}|$  represents the magnitude of the input impedance of the  $m$ th sub-module of the resonant circuit and  $\phi_{Zi,mn}$  is the phase angle of the input impedance as given by

$$i_{res,mn} = \sum_{n=1}^{\infty} \left( \frac{\sqrt{2}V_{dclink,n}}{h\pi|Z_{i,mn}|} \sqrt{1 - \cos(2nh\pi D_n)} \sin(2\pi h f_{s,n} t + \theta_h - \phi_{Zi,mn}) \right) \quad (4.10)$$

$$|Z_{i,mn}| = R_{ac,n} \sqrt{\left( \frac{1}{1 + \left( \frac{1}{r_{mn} Q_{mn} \omega_{r,mn}} \right)^2} \right)^2 + \left( \frac{r_{mn} Q_{mn} \omega_{r,mn}}{1 + (r_{mn} Q_{mn} \omega_{r,mn})^2} + Q_{mn} \left( \omega_{r,mn} - \frac{1}{\omega_{r,mn}} \right) \right)^2} \quad (4.11)$$

$$\phi_{Z_{i,mn}} = \tan^{-1} \left( \frac{r_{mn} Q_{mn} \omega_{r,mn} + Q_{mn} \left( \omega_{r,mn} - \frac{1}{\omega_{r,mn}} \right) (1 + (r_{mn} Q_{mn} \omega_{r,mn})^2)}{(r_{mn} Q_{mn} \omega_{r,mn})^2} \right) \quad (4.12)$$

Since a close-to-sinusoidal resonant current is expected to be achieved in each resonant circuit module, only the fundamental component of  $i_{res,mn}$  is considered. The rms resonant current is, then given by (4.13).

$$I_{res,mn} = \frac{V_{dclink,n}}{\pi} \left[ \sum \frac{1 - \cos(2\pi h D_n)}{(h |Z_{in,mn}(\omega_{r,mn})|)^2} \right]^{1/2} \quad (4.13)$$

#### 4.1.2.4 High-Frequency High Voltage Gain Rectifier

The output high-gain rectifier in each module in the proposed converter, also called the voltage quadrupler as shown in Figure 4.7(a), is a stacked combination of two voltage doublers. At the input of each voltage quadrupler, a voltage square waveform in theory will be generated because of the presence of the *LLC* resonant circuit. From Figure 4.7, each half-wave voltage doubler is composed of two circuits: a clamper (Figure 4.7(b)), and a peak detector or a half-wave rectifier (Figure 4.7(c)). On the negative half cycle of  $v_{or,mn}$ ,  $C_{q1,mn}$  charges to the peak of  $v_{or,mn}$ . During the positive half cycle, diode  $D_{q1,mn}$  is reversed biased and  $C_{q1,mn}$  is in series with the input voltage source with the same polarity. Thus diode  $D_{q3,mn}$  rectifies a total of  $2v_{or,mn}^{max}$  across  $C_{q3,mn}$ . Similarly, the second voltage multiplier stage doubles the peak input voltage, giving a dc output equal to four times the peak voltage value of the square-wave input voltage ( $4v_{or,mn}^{max}$ ).

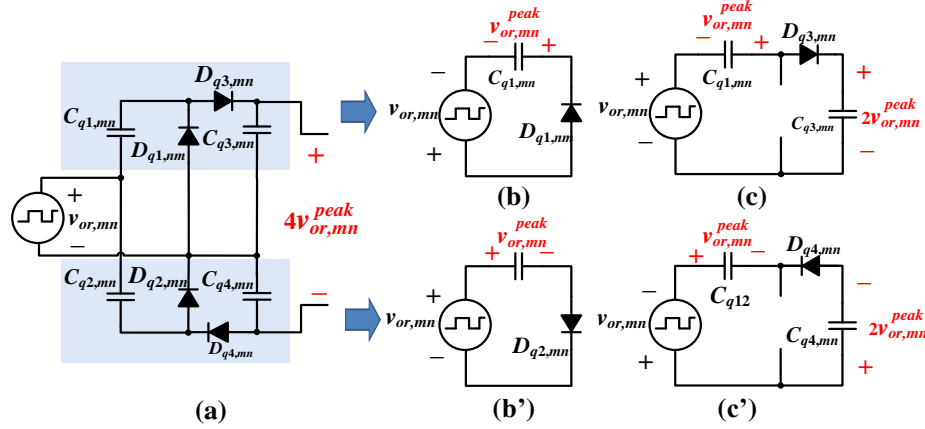


Figure 4.7– Operating principles of the voltage quadrupler rectifier

It should be noted that the number of modules used in the proposed converter strongly depends on the required output voltage. For  $n$  number modules used, the corresponding voltage gain will be equal to  $n$  times the expression given by (4.9).

#### 4.1.2.5 Voltage Balancing Technique across DC-link Capacitors

In the proposed step-up converter, the snubber capacitors across the switches in each module play an important role in reducing the turned OFF switching losses. For the  $n$ th module, with appropriate dead-time chosen between  $(S_{1n}, S_{4n})$  and  $(S_{2n}, S_{3n})$ , the energy stored in the snubber capacitors can be discharged into the resonant circuits which allows using relatively large snubber capacitors. Large capacitors force the voltage across each switch to rise linearly from zero at the turn-OFF instant, resulting in near ZCS. However, in a practical circuit, the capacitance tolerance can introduce voltage unbalance across the dc-link capacitors. Consequently, the voltage stress across each switch in each module will become unequal. To ensure that the voltage across each dc-link capacitor  $C_{1n} \sim C_{2n}$  is always balanced, a simple

passive auxiliary circuit discussed in [67] can be used. The auxiliary circuit, as highlighted in red in Figure 4.8, consists of a 1:1 auxiliary transformer, a series capacitor  $C_{se,n}$  and two fast recovery diodes. The series capacitor,  $C_{se,n}$ , blocks the dc component of the resonant voltage  $v_{s,n}$ , so that a symmetrical voltage waveform is generated across the auxiliary winding. The two diodes  $D_{aux1n}$  and  $D_{aux2n}$  are used to ensure current flowing through  $C_{1n}$  and  $C_{2n}$  will be equal in magnitude but in opposite direction. Hence, the input capacitor voltages maintain balance. Prior to turning ON the switches ( $S_{1n}, S_{4n}$ ) or ( $S_{2n}, S_{3n}$ ), the auxiliary diodes  $D_{aux1n}$  or  $D_{aux2n}$  conduct for a brief interval. If the voltage across  $C_{2n}$  ( $V_{c2n}$ ) is higher than  $V_{c1n}$ ,  $D_{aux1}$  conducts, and contrarily when  $V_{c1} > V_{c2}$ ,  $D_{aux1}$  conducts to ensure a balanced voltage across the dc-link capacitors. Since the impedance of the auxiliary circuit is higher than the input impedance of each resonant circuit module, the voltage balancing circuit does not affect the converter's operation.

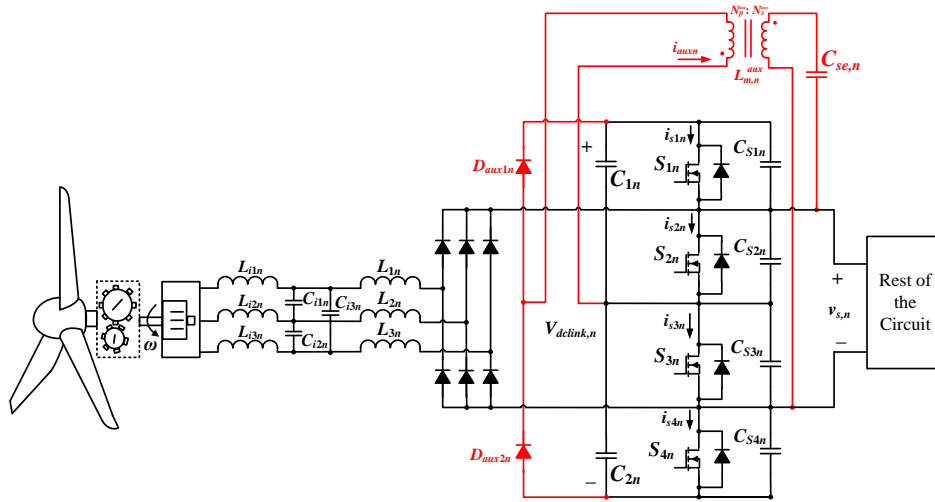


Figure 4.8– DC-link capacitor voltage balancing technique with an auxiliary circuit in the proposed converter (for one module)

### 4.1.3 Simulation, Experimental Results and Performance

To validate the functionalities of the proposed converter, a 1.5-MW, 690-V<sub>ac</sub> (line-to-line rms voltage), wind turbine system (such as the Vensys70 from Vensys AG Germany) is used as the input of the proposed converter. An output voltage of 40 kV for the MVdc grid is achieved. To accommodate this level of output voltage and power rating, two modules of the proposed circuit are used in this example with four sub-modules of the resonant circuits and high-gain rectifiers. So, each output capacitor will handle a voltage level of 5 kV. Regarding the selection of power transistors, parallel-connected SiC MOSFETs modules from Cree are used to provide the required current handling capability for each switch. High-voltage paper-film capacitors are used for all the resonant and output capacitors. The design procedures of each resonant circuit module are given below. Table 4.1 lists all the circuit parameters and the components part number used for this design example.

- 1) The output voltage of each sub-module is 10 kV with the nominal power of 375 kW.

Then, the equivalent ac resistance can be given by

$$R_{ac} = \frac{1}{2\pi^2} \frac{V_o^2}{P_o} = 54\Omega \quad (4.14)$$

- 2) To achieve 10 kV output voltage for each sub-module, the boost rectifier is designed to step up the 690-V<sub>ac</sub> input voltage to 2.5 kV across the dc-link capacitors in each module. Therefore, the largest boost inductors ( $L_{1n}$ ,  $L_{2n}$  and  $L_{3n}$ ) that allow the boost rectifier to stay in DCM are calculated by

$$L_{1n} = L_{2n} = L_{3n} = \frac{R_{ac} D_n^2}{f_{sw} \left[ \left( 2 \frac{V_{dclink}}{V_{line,peak}} - 1 \right)^2 - 1 \right]} = 40 \mu H \quad (4.15)$$

- 3) Regarding the resonant circuit component parameters, with a switching frequency  $f_{sw}$  around 21 kHz, the rms value of  $v_{sn}$  is then given by

$$v_{s,n} = \frac{V_{dclink} \sqrt{2}}{\pi} \left[ \sum_{h=odd} \frac{1}{h^2} \right]^{1/2} = \frac{V_{dclink,n}}{2} = 1250v \quad (4.16)$$

Hence, to achieve a voltage gain of 8 for each sub-module, according to (4.8), with  $r$  and  $Q$  chosen to be 1.6 and 6, respectively. The relative angular frequency for each sub module can be calculated to be  $\omega_r=0.74$ . Hence, the series resonant inductor in each module is then calculated by

$$\text{resonant inductor} = \frac{R_{ac}}{Q \omega_0} = 32 \mu H \quad (4.17)$$

Since  $r = 1.6$ , the magnetizing inductance of each transformer is calculated to be 52  $\mu H$  with a turns-ratio of 1:1. Finally, the resonant capacitor is then given by

$$\text{resonant capacitor} = \frac{1}{(2\pi f_0)^2 L_s} = 1 \mu F \quad (4.18)$$

Table 4.1– Components Part Numbers and Values in the 1.5MW design

	Components Part #/ Values
DC – link capacitors	FFLI6Q0607K, 600 $\mu$ F film Capacitor, 1.4kV
Output capacitors	T50W2NR-F (1 $\mu$ F, 5kV ) high voltage paper-film capacitor
Snubber capacitors	0.22 $\mu$ F, 1.6kV polypropylene metallized film
Resonant capacitors	T50W1NR-F (1 $\mu$ F, 5kV ) high voltage paper-film capacitor
Series resonant inductors	32 $\mu$ H, N87 ferrite core
SiC MOSFETs	CAS300M12BM2 (1.2kV, 5m $\Omega$ ) [6 in parallel]
High frequency transformers	52 $\mu$ H (1:1 turns-ratio), N87 ferrite core
High-gain rectifier diodes	DFM250XXM65 (6.5kV, 250A, fast-recovery)
Input rectifiers	APTDF400KK120G (1.2kV, 470A)

#### 4.1.3.1 High-Frequency Transformer Design

It is known that in high-power medium-to-high frequency transformers, high isolation requirements, desired leakage inductance, evaluation of the parasitic elements, skin and proximity effect and magnetic core losses have to be taken into account [93]–[95]. The additional power losses as a result of the eddy current in the magnetic core, and skin and proximity effect in the winding, together with the reduced size of the transformer, lead to higher loss densities that will increase the heat dissipation requirement. Since the high frequency transformers utilized in the proposed converter design consist of unity turns-ratio windings, and the secondary winding is not directly interfaced with the MV level, the size and weight of the transformer will be significantly less, compared to the conventional high frequency step-up transformers that require high turns-ratio and number of slots [95].

Two transformer core types that are suitable for the proposed converter design are: ferrite N87 U-shaped core [96] and nanocrystalline core material [95]. Parallel Litz wire bundles will be utilized for each winding. In order to force symmetric currents in each bundle, the

arrangement of common chokes can be placed. Figure 4.9 shows the cross-sectional view of the high frequency transformer that can be used for the proposed design. In this particular structure, both the primary and secondary windings consist of layer-to-layer winding with number of slots. This type of transformer structure can limit the voltage across each slot for both the primary and secondary windings with less insulation materials.

To minimize the leakage inductance, the primary and secondary windings are wound concentrically in a shell-type transformer core. This reduces the leakage flux and consequently the leakage inductance as both the primary and secondary windings are placed on the same center leg. Winding capacitance should also be reduced as it can increase the resonant current peak value. By distributing the windings in a number of slots as shown in Figure 4.9, the equivalent winding capacitance will be a series connection of slots' capacitances, which reduces the winding capacitance dramatically. The isolation is provided by mica tape and the system is cooled by means of aluminum water-cooled heat-sinks [95], [96].

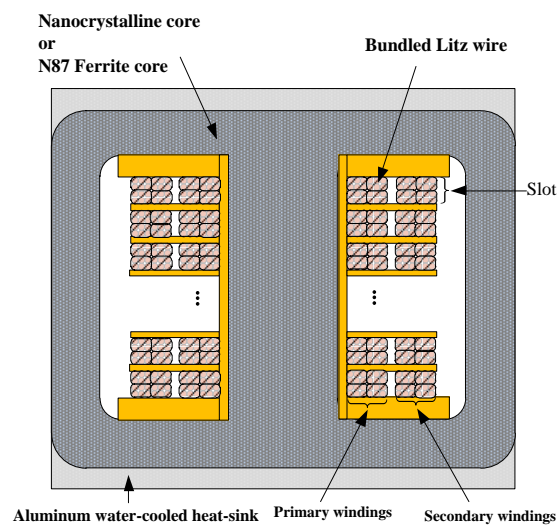


Figure 4.9– Cross-sectional view of the high frequency transformer

### 4.1.3.2 Controller in the Proposed Design

The control block diagram of this design is shown in Figure 4.10. Since two main modules were used, the output voltage of each module is controlled via variable frequency control. The voltage-controlled oscillator (VCO) discussed in section 2.2 was used in the voltage feedback loop. Each resonant circuit and high-gain rectifier module was modeled using the EDF technique. The detailed modeling of the resonant circuit has been discussed in section 2.4.4, hence, the detailed analysis will not be presented here. In general, the closed-loop small-signal transfer function of the output voltage feedback in each module is given by (4.19), where  $G_{sense,n}(s)$  is the transfer function for the output voltage sensor,  $PI_V(s)$  is given by (4.20), where  $k_c$  and  $T_c$  represent the gain and time constant of the PI compensator of the voltage feedback loop, respectively;  $\hat{f}_{s,n}(s)/\hat{v}_{con,n}(s)$  represents the transfer function of the VCO; and  $\hat{v}_{o,n}(s)/\hat{f}_{s,n}(s)$  is the control-to-output transfer function as discussed in section 2.4.4.

$$G_{loop,n}(s) = \frac{\hat{v}_{o,n}(s)}{\hat{f}_{s,n}} \frac{\hat{f}_{s,n}}{\hat{v}_{con}(s)} PI_V(s) G_{sense,n}(s) \quad (4.19)$$

$$PI_V(s) = \frac{k_c(1 + sT_c)}{sT_c} \quad (4.20)$$

Since two sub-modules of resonant circuits are used in each main module, it is essential to ensure that the resonant currents are balanced within each module. The balancing of the resonant currents in each module is achieved by the inner current control loop as shown in Figure 4.10, where duty ratio control is used in individual module. PI compensators were used in both the inner current and outer voltage loops to ensure that a high dc gain in the frequency response will

help eliminate the steady-state errors. With the control-to-output transfer function obtained in section 2.4.4, the poles and zeros placement of the PI controllers are obtained with the aid of the SISO toolbox from MATLAB. The closed-loop frequency response per module will be discussed in the next sub-section.

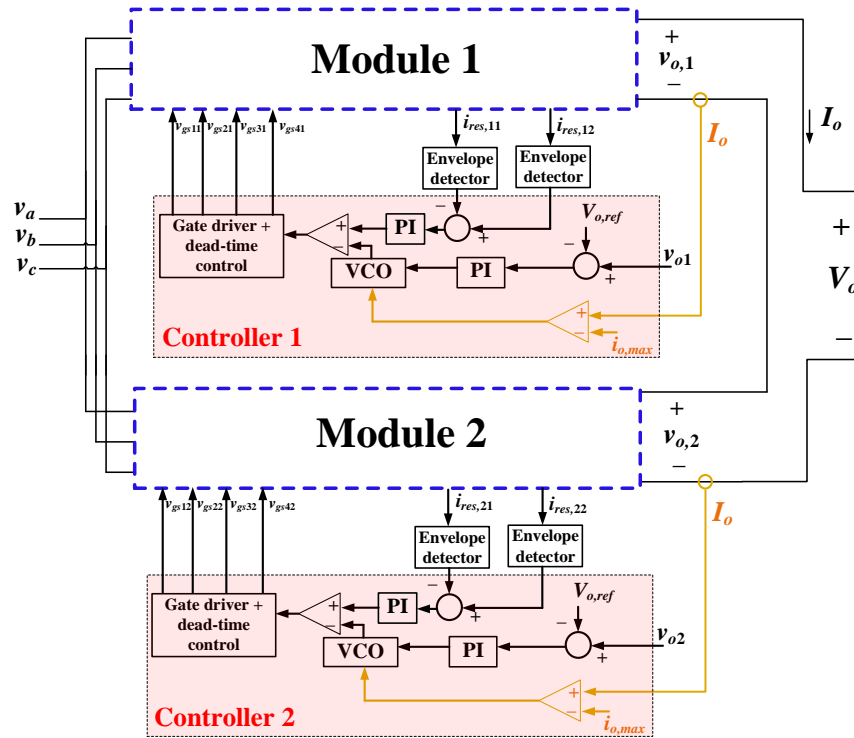


Figure 4.10– Control block diagram

### 4.1.3.3 Simulation Results

Figure 4.11 shows the switching waveforms across the SiC MOSFETs in one module of the converter at the rated power condition. Due to the relatively high output capacitance of the SiC MOSFETs (i.e.,  $2.5\text{ nF} \times 6 = 15\text{ nF}$ ), additional snubber capacitors are required to achieve ZCS turn-OFF, which is approximately  $200\text{ nF}$ . Since the duty ratio and the switching frequency of all the modules are controlled to be almost identical, only one module of the switching waveforms

will be shown here. From Figure 4.11, it can be observed that ZVS turn-ON and ZCS turn-OFF are achieved in the SiC MOSFETs. Figure 4.12 shows the switching waveforms in one module when the input voltage drops to 350 V<sub>AC</sub>, demonstrating that soft-switching condition, is also achieved in the switches.

The stability performance of the voltage regulation function in the controller was also verified through this design example. Figure 4.13 shows the closed-loop Bode plots of the system for different input voltages (i.e., when they are 690 V<sub>AC</sub> and 350 V<sub>AC</sub> respectively). The phase margins achieved are 51° and 62° respectively. Figure 4.14 shows the dynamic performance of  $V_o$  and the input currents when the input voltages continuously increases from 350 V<sub>AC</sub> to 690 V<sub>AC</sub>. It can be observed that  $V_o$  is well regulated when the input voltage changes. A plot of the converter's efficiency at different power levels is obtained as shown in Figure 4.15. The full power efficiency is 97.1%.

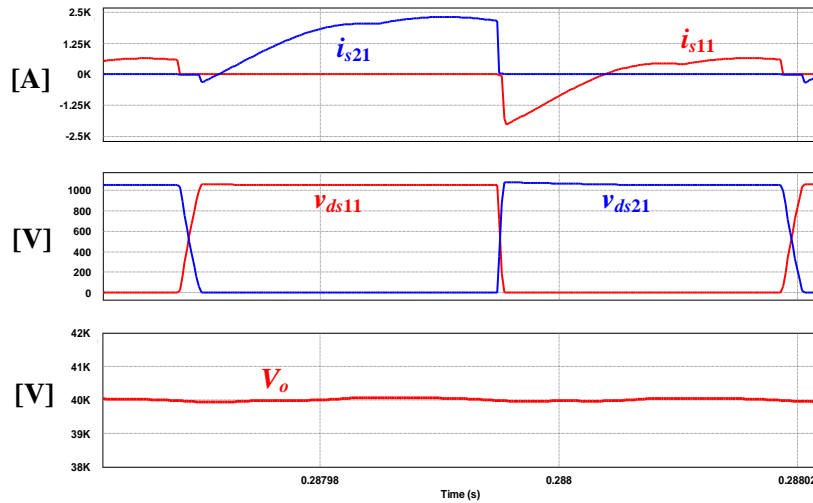


Figure 4.11– Switching waveforms at rated power condition (per module)

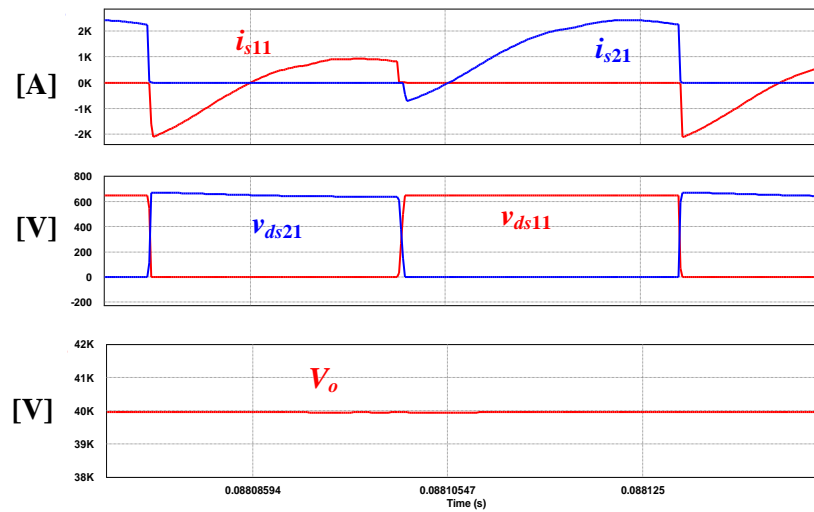


Figure 4.12– Switching waveforms at reduced load condition at an input voltage of 350V<sub>AC</sub> (per module)

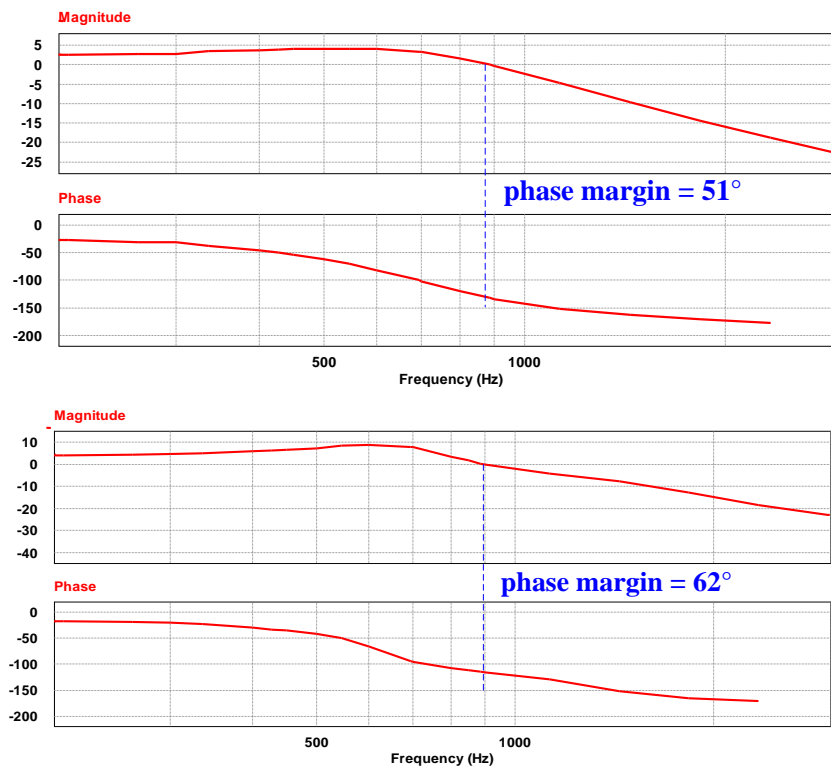


Figure 4.13– Closed loop Bode Plot (per module performance): (top) at rated power, (bottom) input voltage drops to 350V<sub>AC</sub>

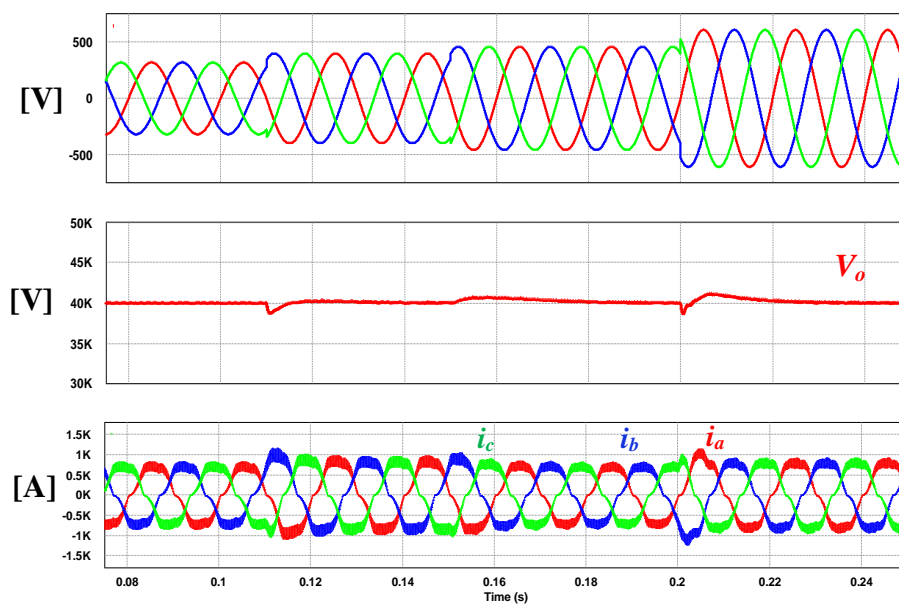
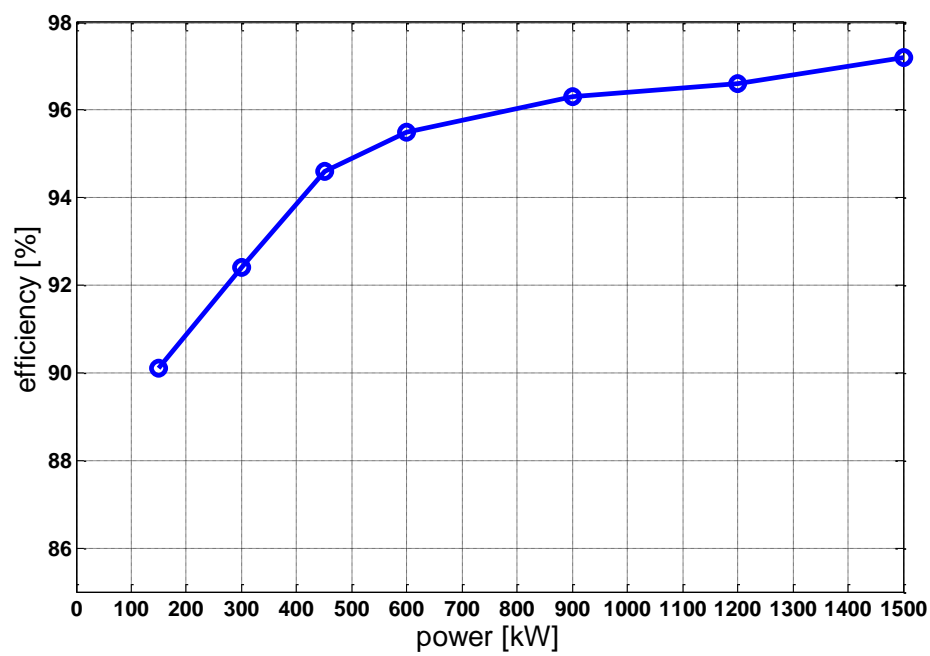
Figure 4.14– Dynamic performance of  $V_o$  when input voltage changes

Figure 4.15– Efficiency performance

#### 4.1.3.4 Experimental Results

To further verify the performance of the proposed topology, a 3.5-kW, 145-V<sub>ac</sub>/6.2-kV laboratory scale proof-of-concept prototype with three modules (one sub-module of resonant circuit and voltage quadrupler being used in each module) was built in the laboratory as shown in Figure 4.16. SiC switching devices were utilized in the prototype implementation. The circuit parameters, component model numbers of the prototype and the system specifications are given in Table 4.2. Figure 4.17 shows the input voltages and the output dc voltage at the rated power condition, with the output voltage regulated at a switching frequency of 22.6 kHz. Figure 4.18 shows the switching waveforms of one module of the prototype. It can be observed that ZVS turn-ON are achieved in the switches. The voltages across switches  $v_{ds11}$  and  $v_{ds21}$  have the same magnitude, which confirms the dc-link capacitor voltages are balanced. ZCS turn-OFF operations of the switches can be observed from Figure 4.19, which shows the turn-OFF transition of the switches. Figure 4.20 shows the current and voltage waveforms in one of the output high-gain rectifier diodes. It can be observed that ZCS turn-ON and OFF are achieved. Figure 4.21 shows the measured resonant currents in all three modules and the input voltage of the resonant circuit in one module. It can be observed that all the resonant currents are balanced. The error among these resonant currents is measured to be 3.2%, which shows that all the modules are well-balanced in the prototype.

Table 4.2– Specifications and Components for the Prototype

Prototype Specifications	
Rated power:	3.5kW
Input voltage:	145V <sub>L-L,RMS</sub>
Output medium voltage:	6.2kV
# of modules:	3
Components Part Number and Values Per Module	
Switches:	SiC MOSFET, SCT3030 (650V, 70A, 30mΩ)
Input rectifier diodes:	SiC diodes, STPSC15H12D
DC-link capacitors:	EZP-E50107MTA (100μF, 500V)
Snubber capacitors:	18nF, 300V
Resonant capacitor:	68nF, 1kV
Resonant inductor:	381 μH
High frequency transformer:	Ferrite core E N87, 638 μH, (1:1)
High-gain rectifiers:	SiC Schottky, GP2D005A170B (1.7kV, 5A)
Output capacitors:	B32774D4106K, (1μF, 1.3 kV)

Figure 4.22 shows the measured input currents, and the measured power factor is close to 0.99 in all phases. The measured efficiency for the full-load condition is 95.4%. The prototype's performance for reduced load condition was verified when the input voltage drops to 110 V<sub>ac</sub> with the output power drops to 60% load condition. Figure 4.23 shows the switching waveforms of one module when the power drops to around 2kW. It can be observed that soft-switching turn-ON and OFF are achieved in the switches. Figure 4.24 shows the measured input currents with an input power factor of 0.996. In this experimental prototype, individual controller was implemented with analog ICs for each module to regulate the module's output voltage. Figure 4.25 shows the dynamic response of  $V_o$  when the input voltages are increased from 100 to 145 V<sub>ac</sub>. It should be noted that the dynamic response of  $V_o$  can be further optimized by using a lower time-constant PI compensator in each controller.

The total power loss of the prototype at its rated power is measured to be 158.4 W. A breakdown of the losses for the key components in the prototype is shown in Figure 4.26. It can be observed that the MOSFETs conduction loss is the highest power loss. Compared to the SiC MOSFET modules used in the 1.5MW design, the  $r_{ds\_on}$  of the switches used in the prototype is much higher. Hence, the overall efficiency can be further improved by employing higher voltage rating SiC MOSFETs with much lower  $r_{ds\_on}$ . For proof-of-concept demonstration purpose, 650V SiC MOSFETs were selected in this design since the specified rated input voltage is 145V<sub>ac</sub>.

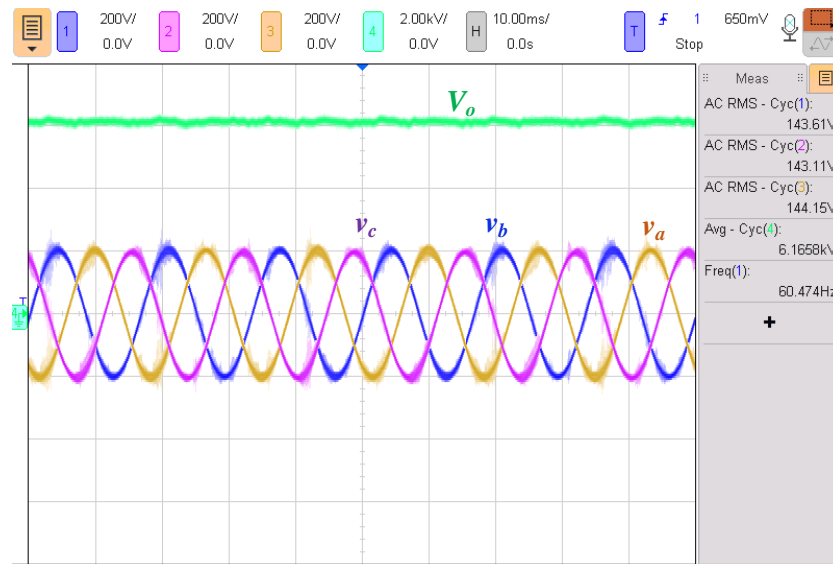
To better demonstrate the power loss analysis of the hardware prototype circuit, the thermal performance of the key components in the prototype is presented as shown in Figure 4.27 and Figure 4.28. Figure 4.27 shows the thermal images of all the switches in one module. While the temperature measurements showed that the operating temperature of the switches are well below the device's maximum operating temperature, due to the higher conduction losses in  $S_{21}$  and  $S_{31}$  (i.e., the middle switch in each inverter circuit), higher power losses are expected in this switch, and hence the operating temperature of  $S_{21}$  and  $S_{31}$  is higher than that of  $S_{11}$  and  $S_{41}$ . Figure 4.28 shows the thermal performance of one of the HF transformers, the resonant inductor, and the input rectifier diodes. The power loss breakdown of the switches in one module is also provided, where Figure 4.29 shows the detailed power loss breakdown of switches  $S_{21}$  and  $S_{31}$ . It can be observed that conduction loss contributes to the major power loss in the switch, almost 75% of the total power loss in each switch. The power loss breakdown of switches  $S_{11}$  and  $S_{41}$  is shown in Figure 4.30. It can be observed that the conduction loss of  $S_{11}$  and  $S_{41}$  is not very significant;

however, as the current flowing through the antiparallel diodes are higher than those in  $S_{21}$  and  $S_{31}$ , the category labeled as “others” is higher. It should be emphasized that in both Figure 4.29 and Figure 4.30, the switching losses can be further minimized by selecting a larger snubber capacitor across each switch with a larger dead time between the turn-ON of  $S_{11}$ ,  $S_{41}$  and  $S_{21}$ ,  $S_{31}$ .

Figure 4.31 shows the power loss breakdown in the HF magnetics designed for all three resonant circuit modules. It can be observed that power losses in these magnetic components are not very significant, and they are in good agreement with the thermal data obtained in Figure 4.28. Figure 4.32 shows the final circuit efficiency and the input power factor for different power levels. An efficiency of at least 91% is obtained from 30% to full-load condition. The input power factor is maintained to be above 0.99 for all the operations.

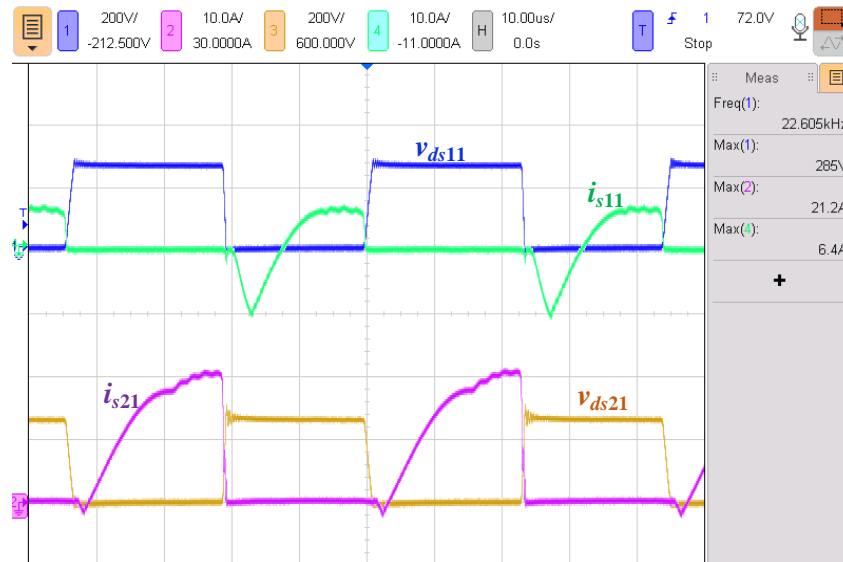


Figure 4.16– 3.5kW, 6.2kV output laboratory scale experimental prototype



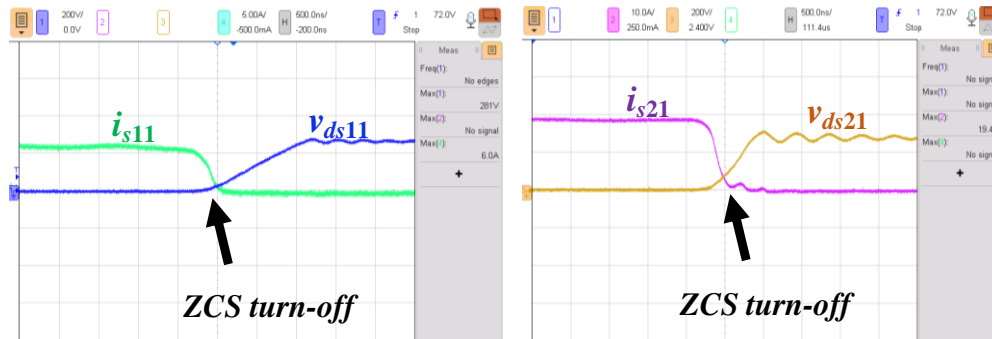
[ $V_o$ : 2kV/div;  $v_a$ ,  $v_b$ ,  $v_c$ : 200V/div; time: 10ms/div]

Figure 4.17– Measured input voltages and output load voltage ( $V_o$ )



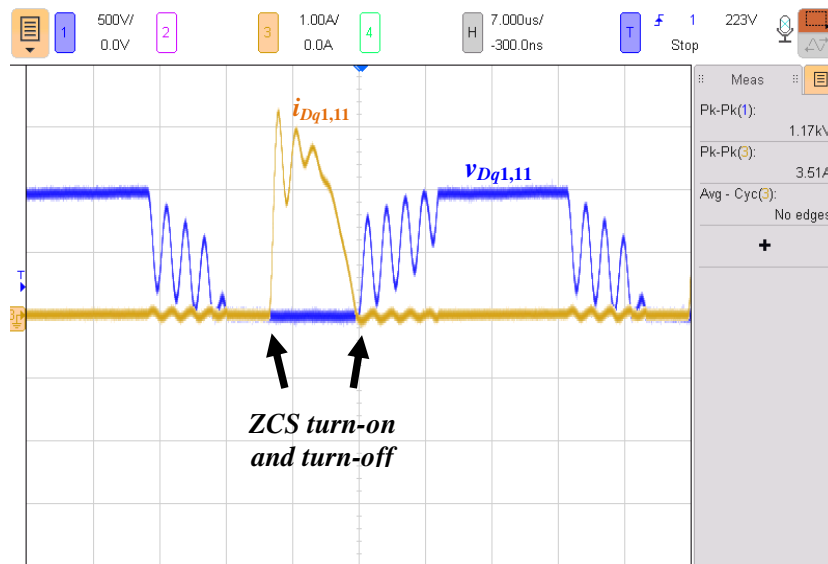
[ $i_{s11}$ ,  $i_{s21}$ : 10A/div;  $v_{ds11}$ ,  $v_{ds21}$ : 200V/div; time: 10 $\mu$ s/div]

Figure 4.18– Measured switching waveforms (one module)



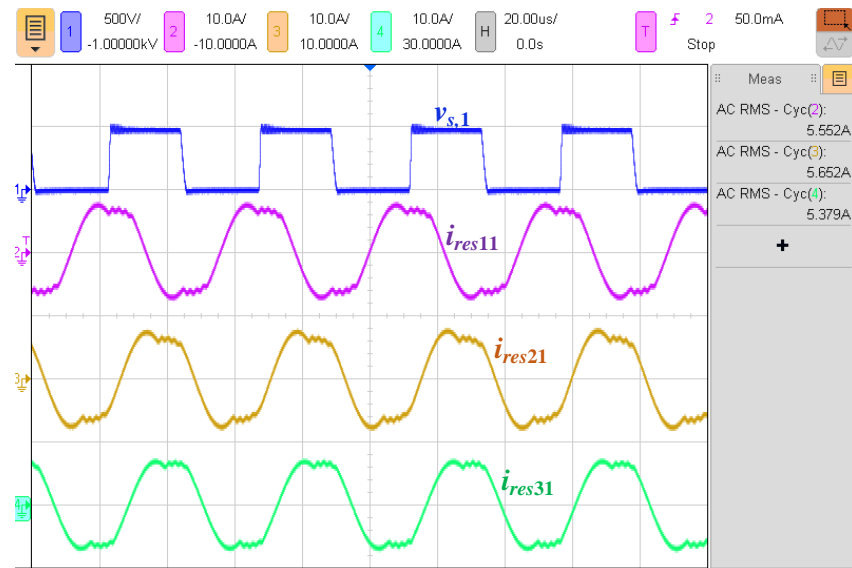
[ $i_{s11}$ : 5A/div;  $i_{s21}$ : 10A/div;  $v_{ds11}$ ,  $v_{ds21}$ : 200V/div; time: 500ns/div]

Figure 4.19– Turn-OFF transition of the switches (in one module)



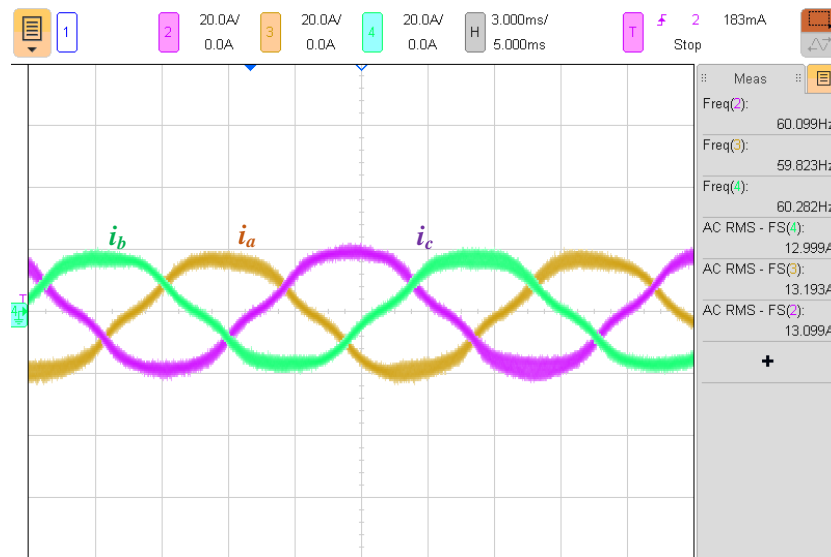
[ $i_{Dq1,11}$ : 1A/div;  $v_{Dq1,11}$ : 500V/div; time: 7 $\mu$ s/div]

Figure 4.20– Measured output diode current and voltage



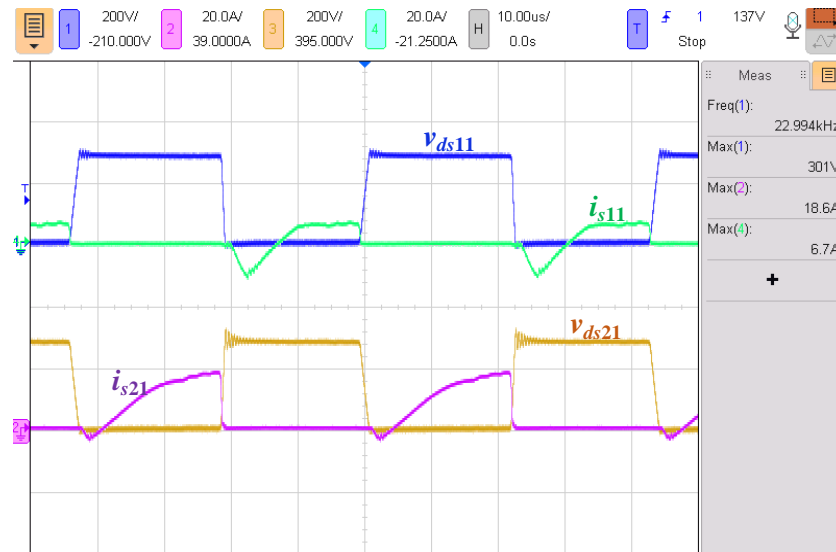
$[i_{res11}, i_{res21}, i_{res31}: 10\text{A/div}; v_{s,1}: 500\text{V/div}; \text{time: } 20\mu\text{s/div}]$

Figure 4.21– Measured resonant currents in all modules and input voltage of one resonant module



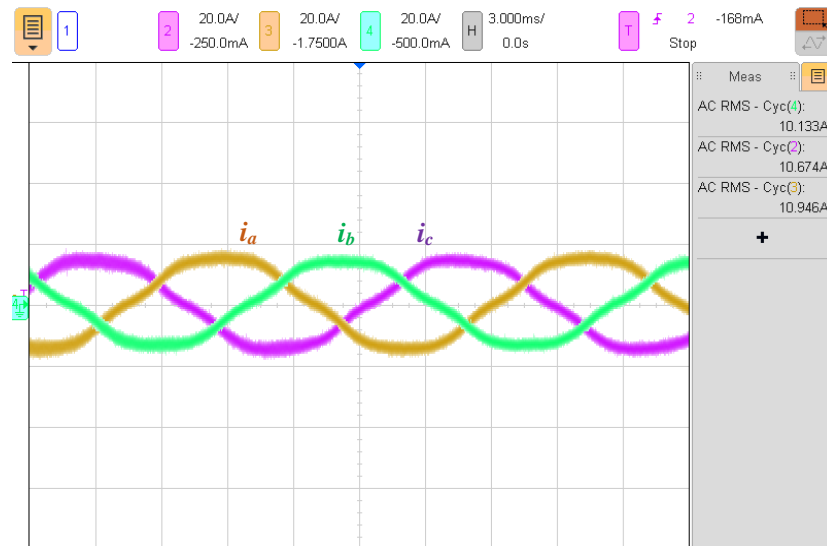
$[i_a, i_b, i_c: 20\text{A/div}; \text{time: } 3\text{ms/div}]$

Figure 4.22– Measured input currents at rated power



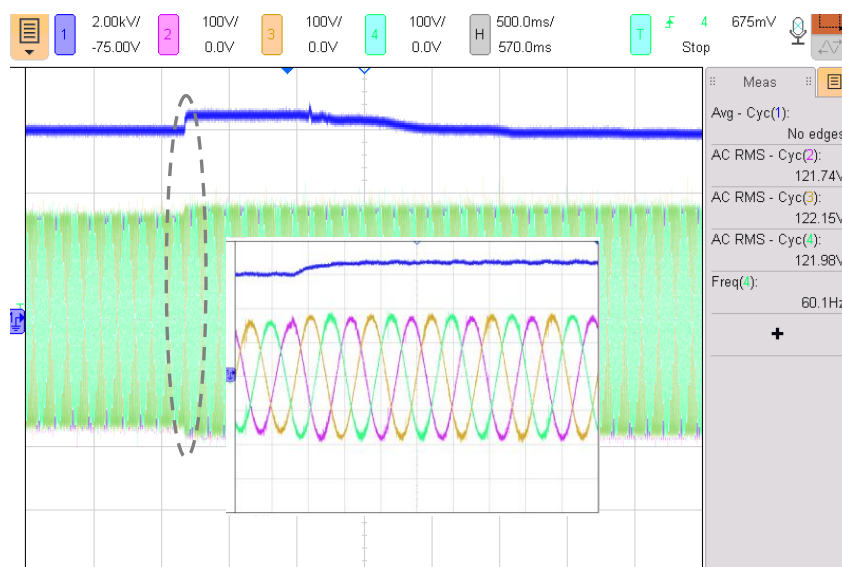
[ $i_{s11}$ ,  $i_{s21}$ : 20A/div;  $v_{ds11}$ ,  $v_{ds21}$ : 200V/div; time: 10 $\mu$ s/div]

Figure 4.23– Switching waveforms (one module) at reduced load condition



[ $i_a$ ,  $i_b$ ,  $i_c$ : 20A/div; time: 3ms/div]

Figure 4.24– Input currents at reduced load condition (at 2kW)



[ $V_o$ : 2kV/div;  $v_a$ ,  $v_b$ ,  $v_c$ : 100V/div; time: 500ms/div]

Figure 4.25– Dynamic response of  $V_o$

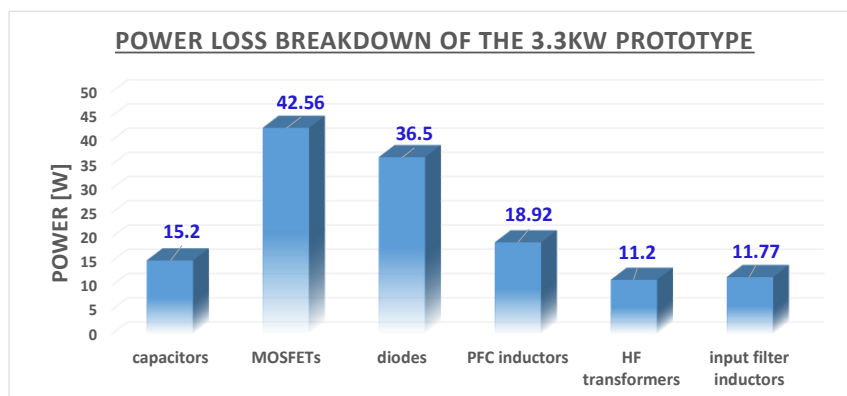


Figure 4.26– Loss breakdown of the key components in the prototype

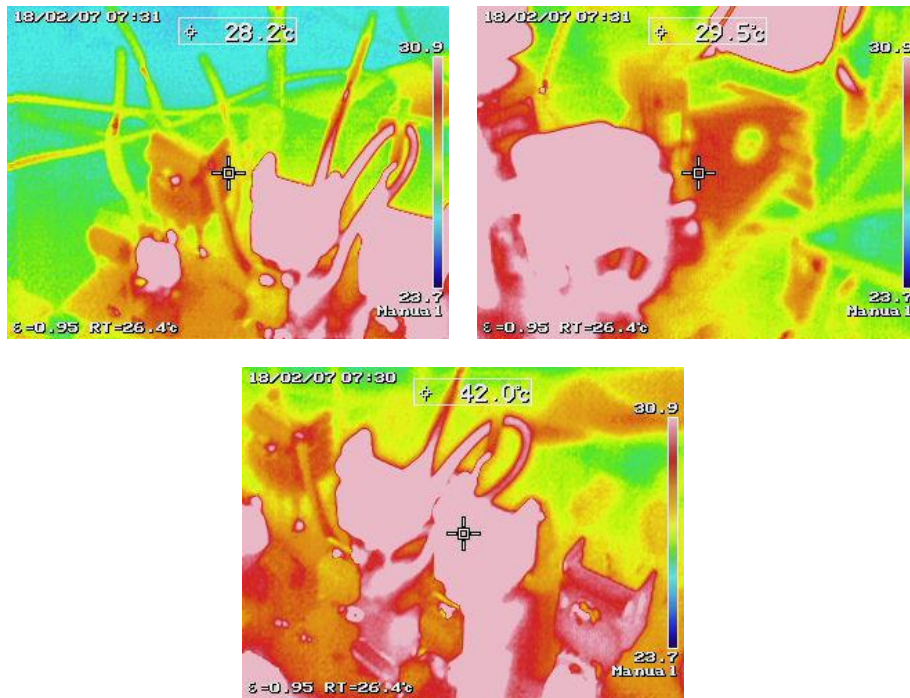


Figure 4.27– Thermal performance of the SiC switches in one module; top left:  $S_{11}$ ; top right:  $S_{41}$ ; bottom:  $S_{21}$  and  $S_{31}$

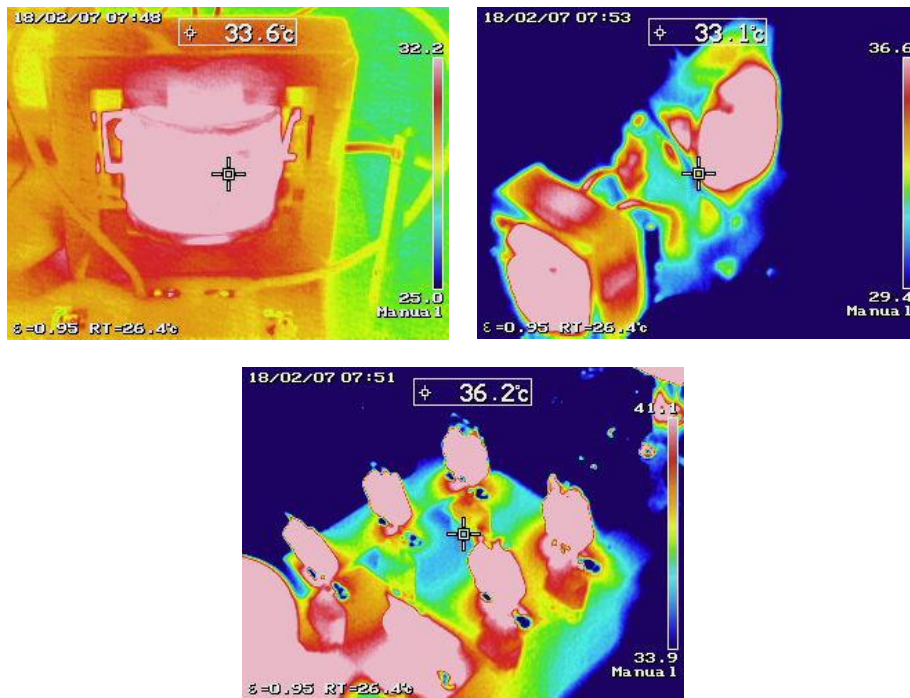
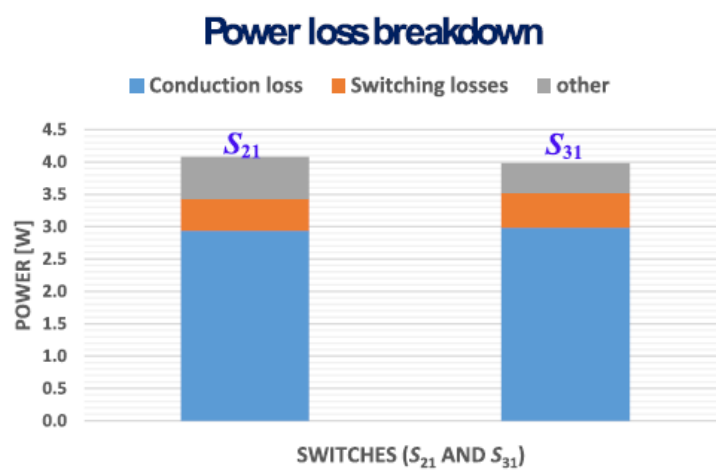
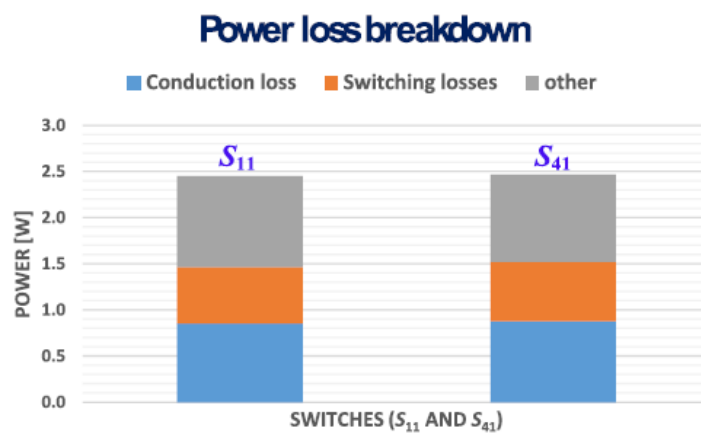


Figure 4.28– Top left: thermal performance of the HF transformer; top right: thermal performance of the series resonant inductor; bottom: thermal performance of the input rectifier diodes.

Figure 4.29– Power loss breakdown in  $S_{21}$  and  $S_{31}$ Figure 4.30– Power loss breakdown in  $S_{11}$  and  $S_{41}$

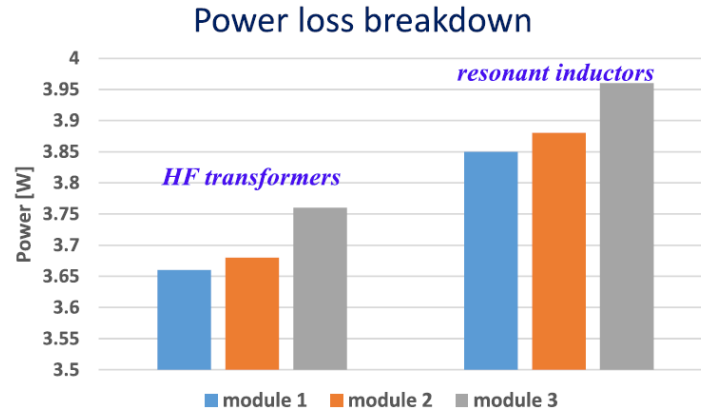


Figure 4.31– Power loss breakdown in all the HF magnetics in the resonant circuit modules

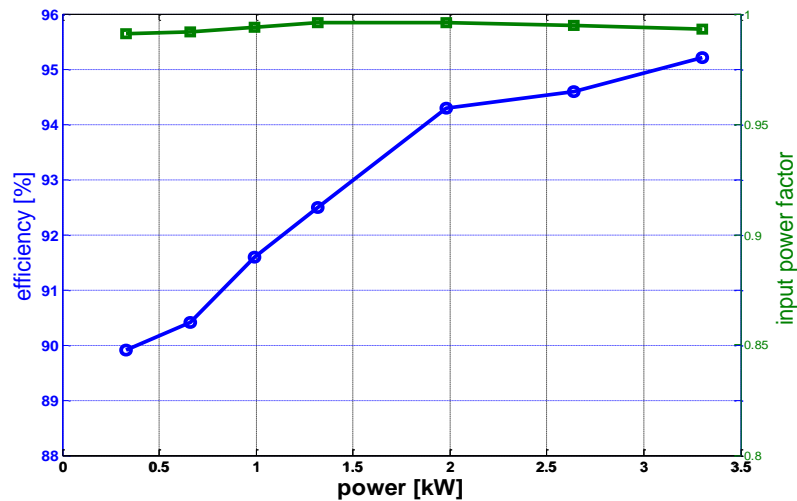


Figure 4.32– Measured efficiency and input power factor

#### 4.1.4 Maximum Power Point Tracking (MPPT)

As the penetration of wind power in the power grid becomes larger, more advanced requirements should be addressed to not only the transmission networks, but also the wind turbine itself. For

example, in the case of the faults and shutting down of transmission networks, the wind turbine systems may need be configured for black start (i.e., restart the power generation without any power supply from the grid). To achieve these more advanced features of grid interconnection, some energy storage systems may be needed for future wind turbines and wind farms. The storage system can be configured locally on the dc-link of each wind turbine unit.

A 1.5 MW, 690 V<sub>ac</sub> wind turbine with the proposed three-phase ac-dc converter and a small energy storage configuration is simulated in PSIM. The block diagram of the simulated wind turbine system is shown in Figure 4.33, in which maximum power point tracking has been achieved using power signal feedback control. In the proposed converter there are two sets of control parameters, switching frequency and duty ratio. In the simulated system, variable frequency control is selected to regulate the output voltage, and duty ratio provides maximum power point tracking. The wind energy system is simulated at three different wind speeds. Power-speed characteristics results of the simulated wind turbine at each wind speed as a function of duty ratio are shown in Figure 4.34. Each curve has a maximum power point (MPP) that occurs at a specific duty ratio. At the same time, the dc output voltage is regulated through variable frequency control of the switches. Figure 4.35 shows the regulated 25kV<sub>DC</sub> output at different duty ratios. Almost sinusoidal input currents at different duty ratios and at MPP are illustrated in Figure 4.36(a) and (b), respectively. Switch currents at different duty ratios, shown in Figure 4.37, verify the soft-switching operation of the converter over a wide range of operating points.

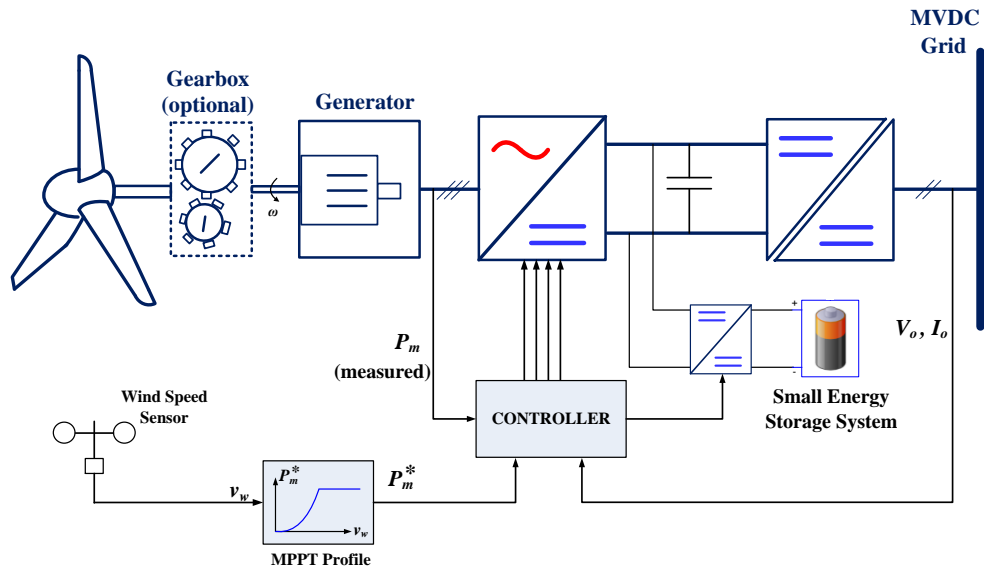


Figure 4.33– Distributed energy storage configuration for each wind turbine with MPPT

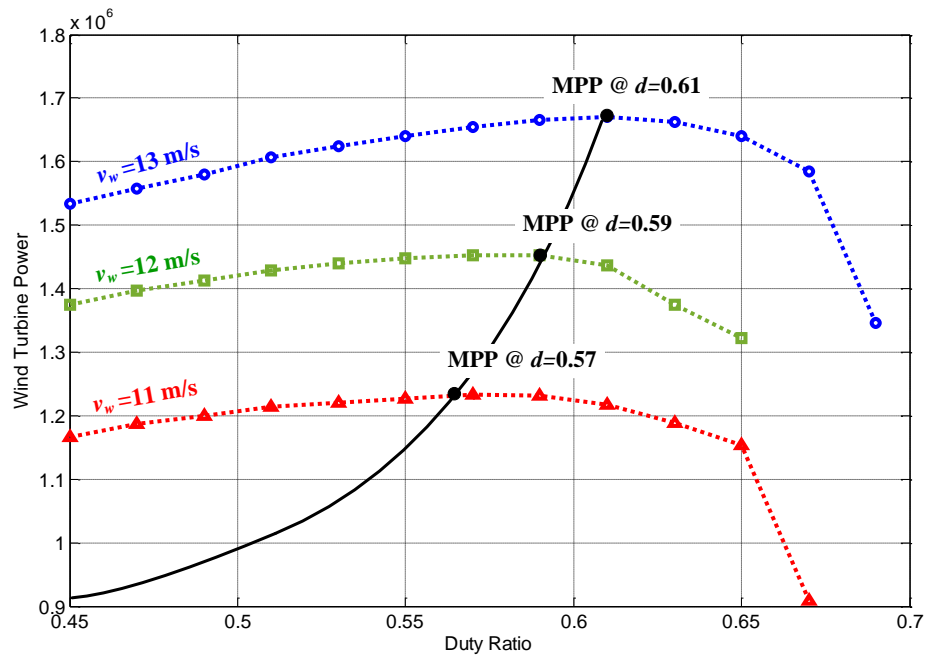


Figure 4.34–Power-speed characteristics results of the simulated wind turbine at different wind speeds as a function of duty ratio

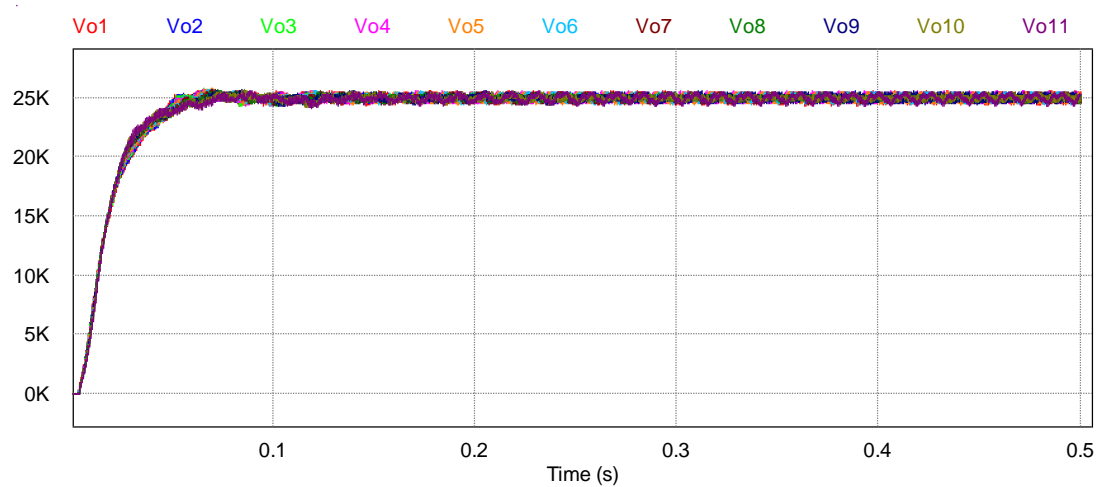
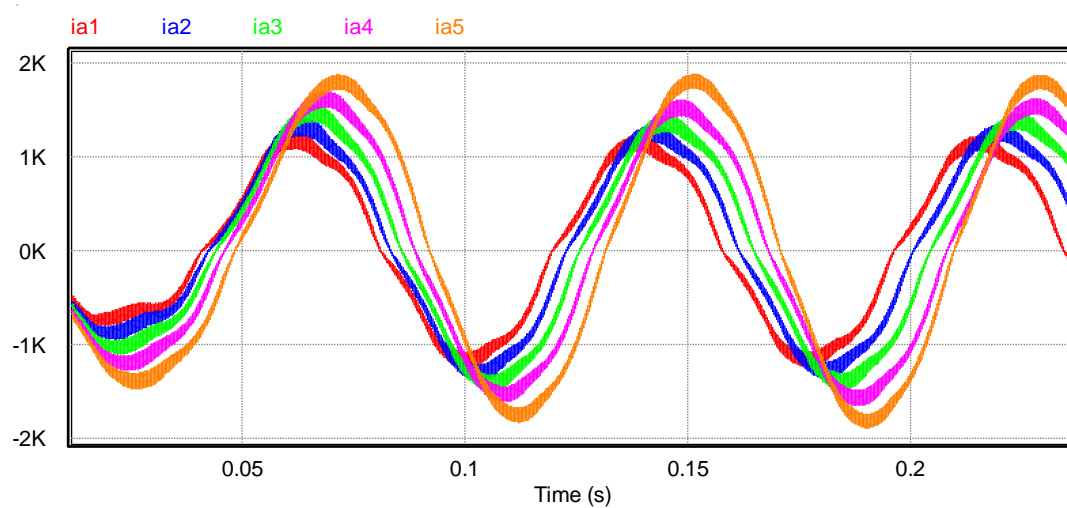
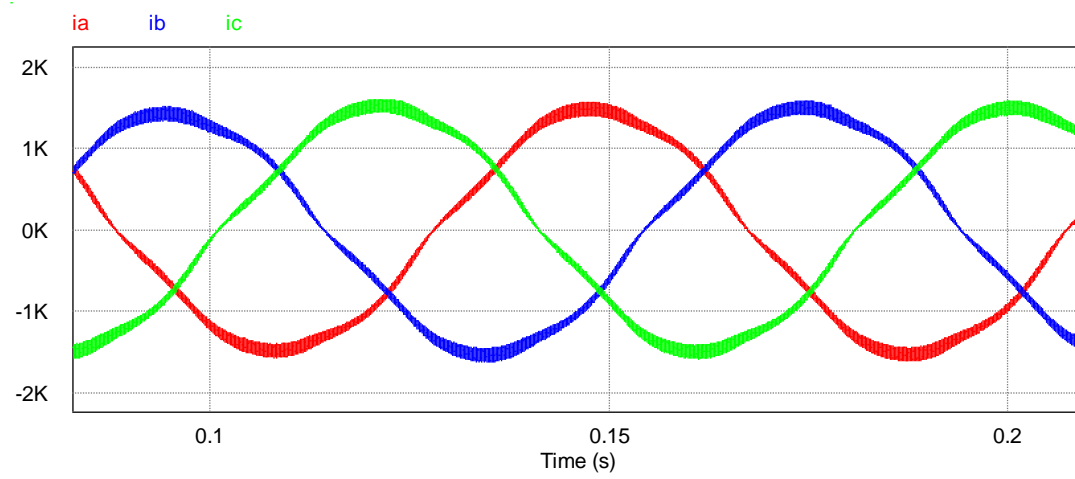


Figure 4.35– Regulated dc output voltages at different duty ratios in the simulated wind system



(a)



(b)

Figure 4.36–Input currents in 1.5MW simulation at  $v_w=12\text{m/s}$ , (a) at different duty ratios, and (b) at maximum power point

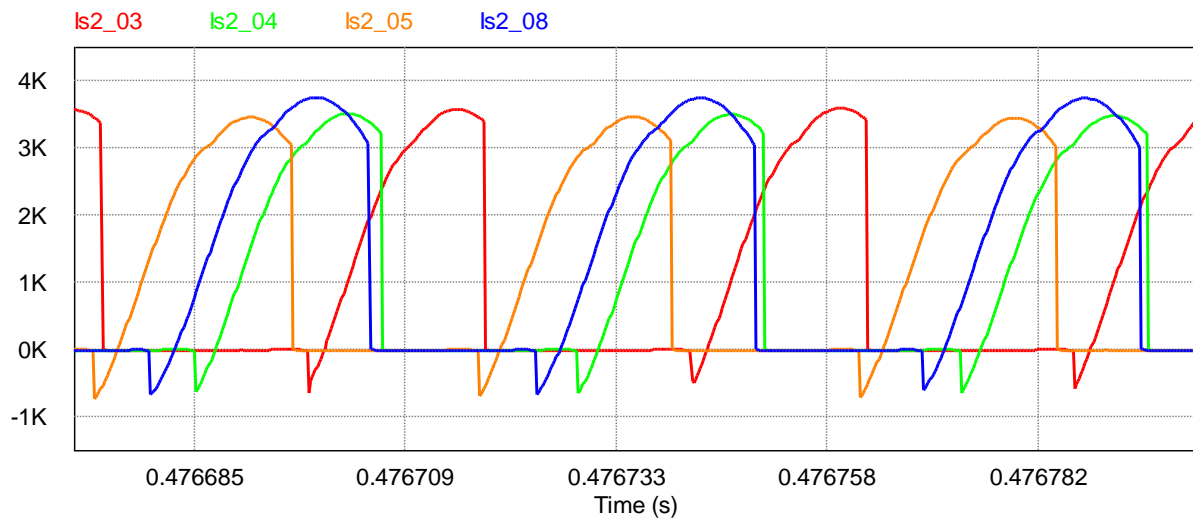


Figure 4.37– Switch  $S_2$  currents at different duty ratios in the simulated wind system

## 4.2 Bridgeless PFC with HGR Approach

The boost converter following a diode bridge rectifier is the most popular PFC converter. This converter is simple and is able to provide near unity power factor. However, it suffers from high switching loss in the switch and high conduction losses in the diode bridge. The power losses of the input diodes in a full-bridge rectifier may contribute 30–50% of the total loss at low-input conditions [97]. To address these issues in boost converters, many power supply manufacturers and companies have investigated bridgeless topologies to reduce the power loss of the input rectifier bridge, and the soft-switching techniques for bridgeless PFC converter to further improve the performance [98]–[102].

To reduce the number of semiconductors and to improve the performance of the proposed converter in section 4.1, a new three-phase bridgeless ac-dc soft-switched, step-up resonant converter with high-gain rectifier modules for MV step-up conversion is presented in this section. The proposed converter is able to reduce the number of lossy diodes required for the front-end rectifier. Unlike the conventional boost or bridgeless boost converters, ZVS turn-ON and ZCS turn-OFF can be also achieved for all switches without any auxiliary circuits.

### 4.2.1 Circuit Description of the Proposed Converter

The block diagram of the proposed modular three-phase PFC circuit is shown in Figure 4.38, which is implemented by star-connection of single-phase PFC converters. As a result, its control loops are simpler than direct three-phase PFC converter. The essential advantage of the Y-rectifier is the lower voltage stress of the power semiconductors compared to  $\Delta$ -rectifier network

[90]. The entire proposed converter is illustrated in Figure 4.39. The converter is derived by combining a bridgeless boost rectifier and a high voltage gain *LLC* resonant converter, where  $L_{B1}$ ,  $L_{B2}$  and  $L_{B3}$  are the three-phase boost inductors. To attain high voltage gain, the isolated resonant inverter modules are connected to a high-frequency voltage quadrupler. The proposed circuit structure can conveniently change the number of paralleled modules to meet required power level. The per-phase operating waveforms in one module of the proposed circuit are shown in Figure 4.40.

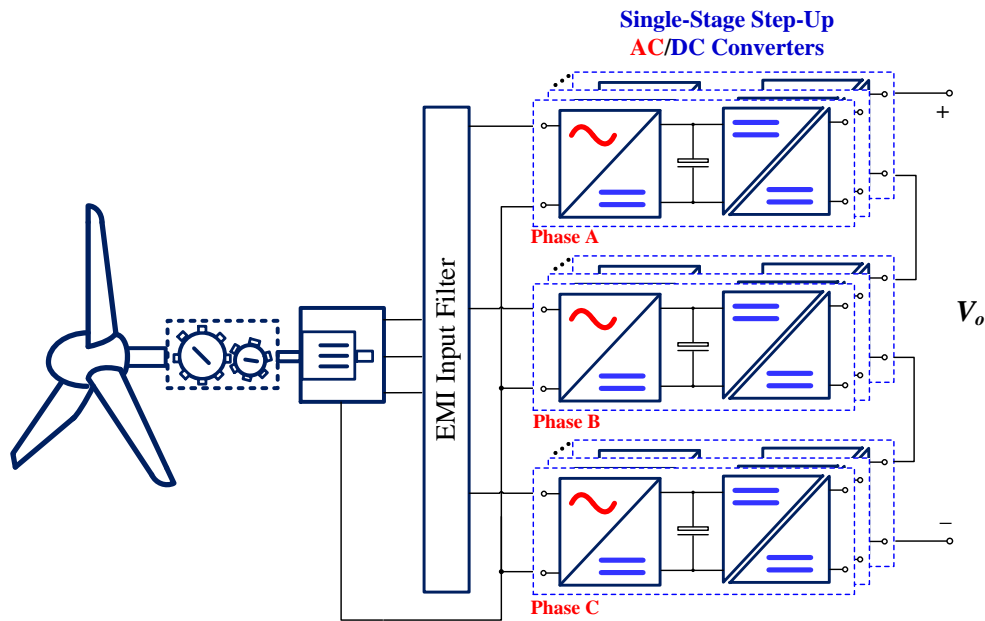


Figure 4.38– Block diagram of the proposed single-stage step-up PFC rectifier systems with star(Y)-connection

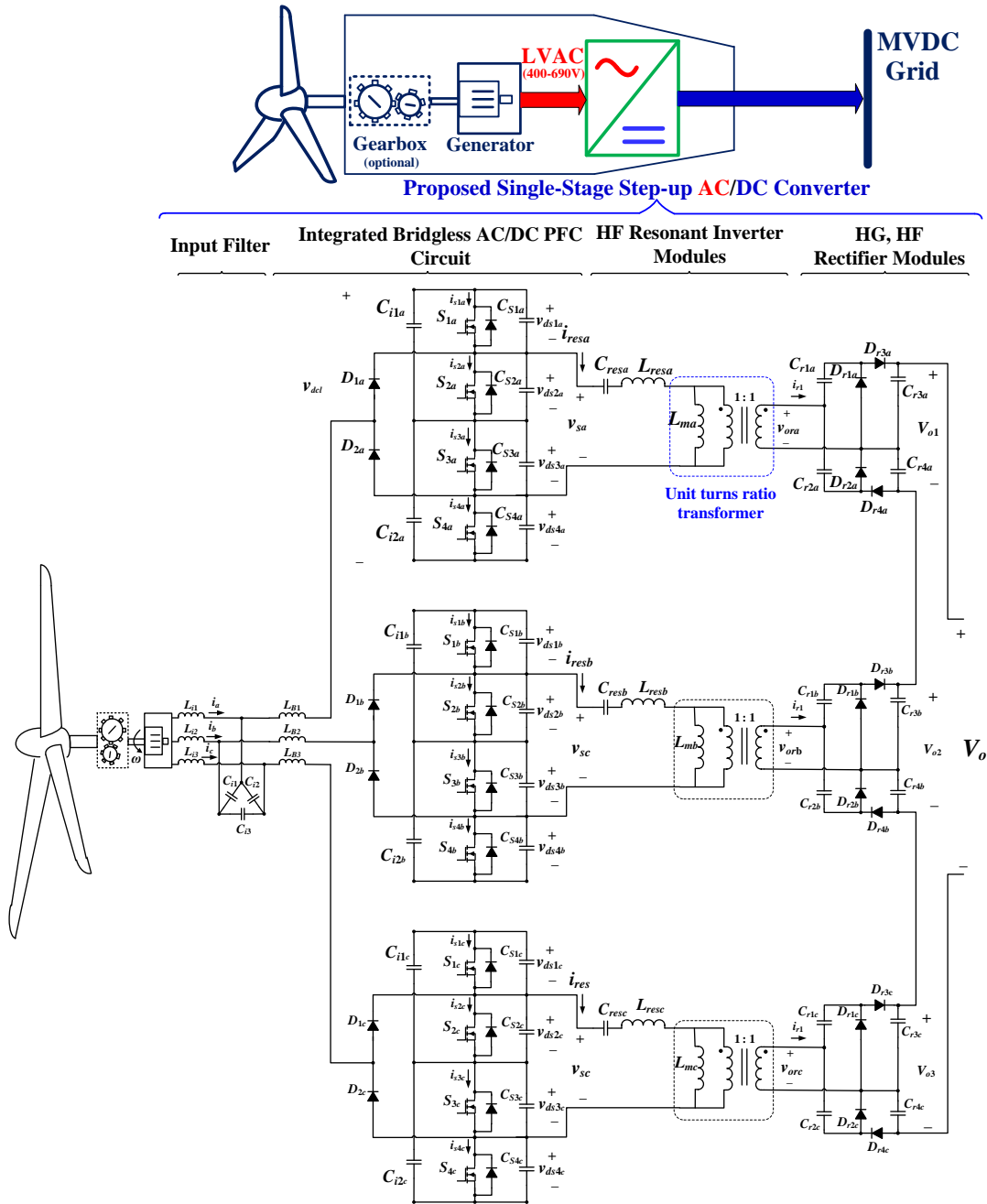


Figure 4.39– Proposed three-phase ac-dc converter with novel bridgeless boost rectifier (one module per phase)

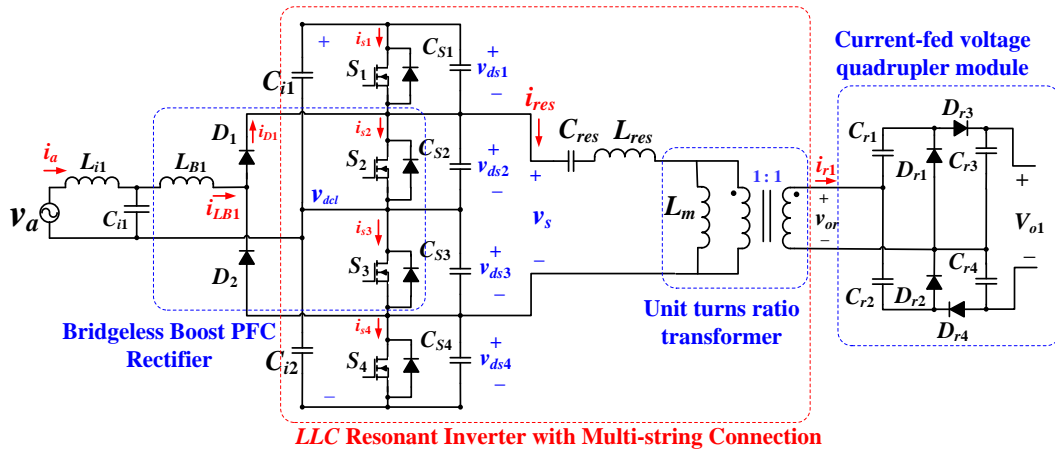


Figure 4.40— Proposed ac-dc converter with new bridgeless rectifier (single phase)

## 4.2.2 Operating Principles of the Proposed Step-up Converter

The operating principles of the proposed converter for all three phases ( $a$ ,  $b$  and  $c$ ) are identical. Hence, the operating waveforms only in phase  $a$  is presented. The key waveforms are illustrated in Figure 4.41, where  $(1-d)T_s$  indicates the duty ratio of the switches  $S_1$  and  $S_4$  and  $dT_s$  represents the interval that  $S_2$  and  $S_3$  are ON. In each phase, a square wave of voltage ( $v_s$ ) is applied to the resonant circuit. Since the resonant circuit acts as a filter, sinusoidal current waveform ( $i_{res}$ ) flows through the resonant circuit. To achieve soft switching, the resonant current is lagging the voltage applied to the resonant circuit. For steady-state operation in the positive and negative half-cycles, the switching period  $T_s$  is divided into 7 operating modes, as shown in Figure 4.42. Since the converter operates symmetrically during both positive and negative half-cycles, only the positive half-cycle is addressed in this analysis.

**[ $t_0 < t < t_1$ ]:** During this stage, the current going through the resonant circuit ( $i_{res}$ ) is negative. The boost inductor current is also discharging to the circuit through  $D_1$ . Hence, at  $t_0$  when the gate signals are applied to  $S_1$  and  $S_4$ , the sum of two currents ( $i_{res}$  and  $i_{D1}$ ) forces the antiparallel diodes of  $S_1$  to conduct. The lagging resonant current ( $i_{res}$ ) also forces the antiparallel diodes of  $S_4$  to conduct. That is why the switch current  $i_{s4}$  reaches zero sooner than  $i_{s1}$  in Figure 4.41. The voltages across the two switches ( $S_2$  and  $S_3$ ) during this interval are clamped to half of the dc-link voltage ( $v_{dcl}/2$ ). Meanwhile, in the voltage quadrupler rectifier,  $D_{r2}$  and  $D_{r3}$  are conducting and the voltage across the  $D_{r1}$  and  $D_{r4}$  are clamped to the half of the dc output voltage.

**[ $t_1 < t < t_2$ ]:** Since the boost converter operates in discontinuous conduction mode (DCM),  $i_{D1}$  becomes zero at  $t=t_1$ . Instantaneously  $i_{res}$  begins to rise from zero.  $S_1$  and  $S_4$  start to conduct, and the current flowing through the antiparallel diodes are now conducted by the switches  $S_1$  and  $S_4$ . Since antiparallel diodes were conducting before turning ON the switches, zero voltage switching can be obtained for the switches. In the voltage quadrupler rectifier,  $D_{r1}$  and  $D_{r4}$  are turned-on under zero current.

**[ $t_2 < t < t_3$ ]:** At the beginning of this stage, the gate signal  $v_{gs1}$  and  $v_{gs4}$  are removed. Switches  $S_1$ ,  $S_4$  begin to turn OFF. At the same time resonant capacitors  $C_{s1}$  and  $C_{s4}$  start to charge. Since before this interval,  $C_{s1}$  and  $C_{s4}$  are already discharged to the resonant circuit, the voltages across the switches  $S_1$ ,  $S_4$  ( $v_{ds1}$  and  $v_{ds4}$ ) begin to charge gradually. This results in near zero current turn-OFF for  $S_1$  and  $S_4$ . Meanwhile,  $C_{s2}$  and  $C_{s3}$  are discharged into resonant circuit.

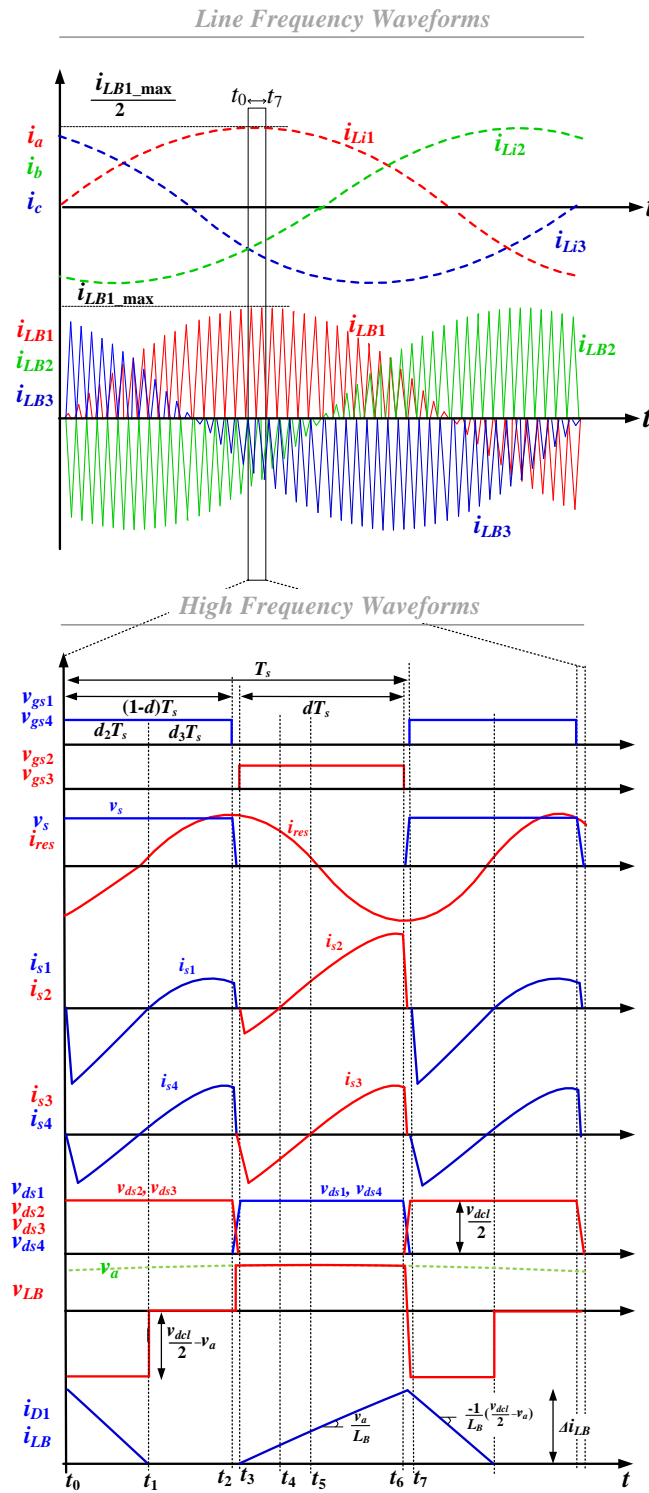
**[ $t_3 < t < t_4$ ]:** At the beginning of this interval, at  $t=t_3$ , the boost inductor  $i_{D1}$  begins to charge from zero. Hence, zero current turn-ON is obtained for diode  $D_1$ . At  $t=t_3$ , the resonant current  $i_{res}$

reaches its peak. Therefore the resonant current  $i_{res}$  is higher than  $i_{D1}$  and the difference between these two currents ( $i_{res}-i_{D1}$ ) forces the antiparallel diode of switch  $S_2$  to conduct. Simultaneously,  $i_{res}$  forces the antiparallel diode of switch  $S_3$  to conduct. Since  $i_{res} > i_{res}-i_{D1}$ , the lagging current flowing through the antiparallel diode of switch  $S_3$  is higher than  $S_2$ . The voltage across the two switches ( $S_1$  and  $S_4$ ) during this interval are clamped to half of the dc-link voltage ( $v_{dcl}/2$ )

**[ $t_4 < t < t_5$ ]:** The switch  $S_2$  now conducts the current flowing through its antiparallel diode in the previous interval. This means that  $S_2$  turns ON under ZVS. However, since  $i_{res}$  is still positive, but less than  $i_{D1}$ , the antiparallel diode of  $S_3$  remains on. During this interval, also  $D_{r1}$  and  $D_{r4}$  are turned OFF under zero current in the voltage quadrupler rectifier.

**[ $t_5 < t < t_6$ ]:** At  $t=t_5$ , the current flowing through the antiparallel diode of  $S_3$  becomes zero. Switch  $S_3$  should now carry the resonant current that has become negative. Hence,  $S_3$  turns ON under ZVS. In the voltage quadrupler rectifier,  $D_{r2}$  and  $D_{r3}$  are turned-on under zero current.

**[ $t_6 < t < t_7$ ]:** At  $t=t_6$ , the gating signal of  $S_2$  and  $S_3$  ( $v_{gs2}$  and  $v_{gs3}$ ) are removed. The snubber capacitors  $C_{s2}$  and  $C_{s3}$  start charging. This allows voltages across  $S_2$  and  $S_3$  to rise slowly, allowing near ZCS turn-OFF to for  $S_2$  and  $S_3$ . At the same time, part of the ( $i_{D1}-i_{res}$ ) flows through the snubber capacitors and  $C_{s1}$  and  $C_{s4}$  begin to discharge.

Figure 4.41– Operating waveforms of phase *a* of the proposed circuit

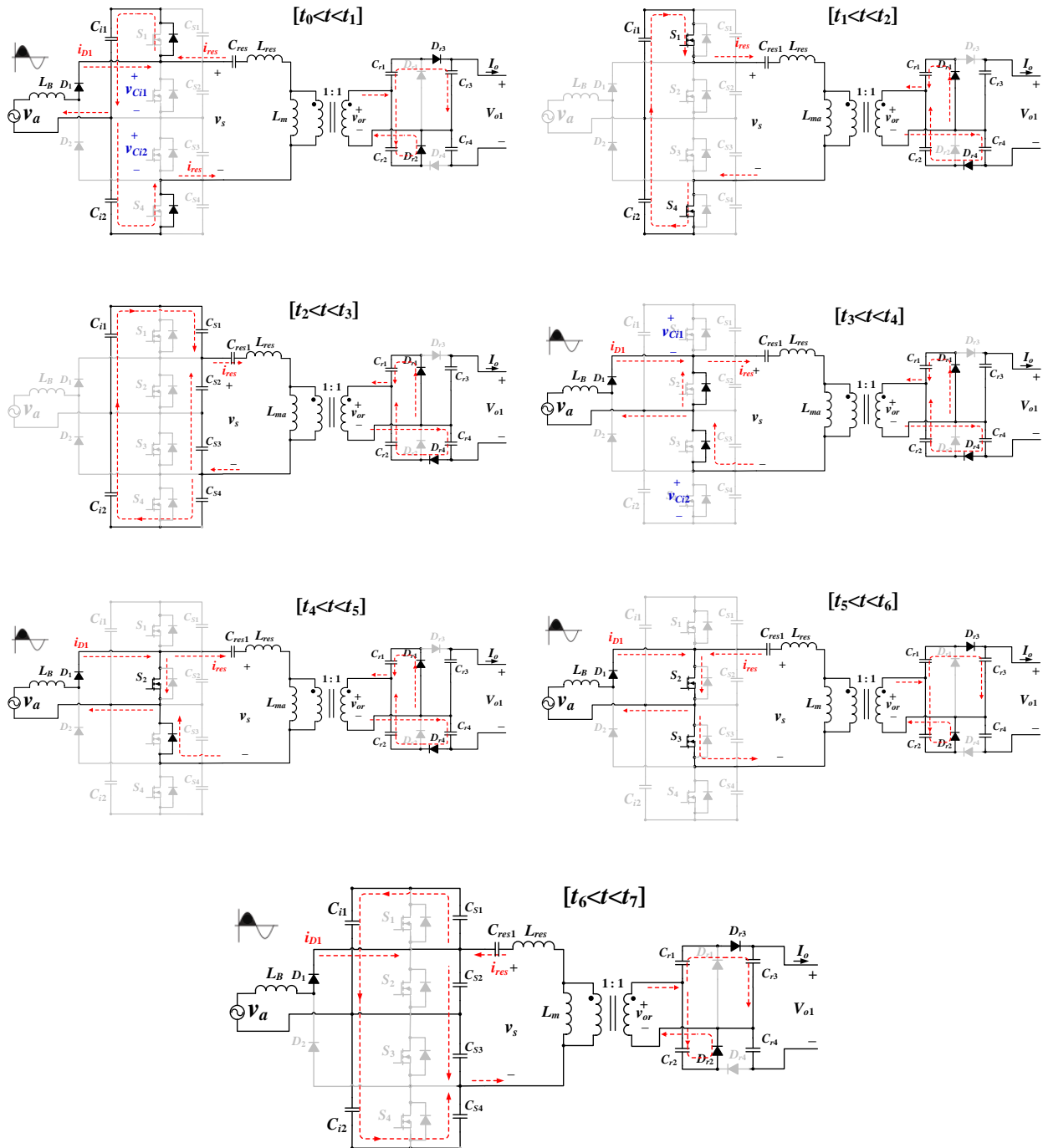


Figure 4.42– Operating stages within a switching period

## 4.2.3 Proposed Converter Analysis

### 4.2.3.1 Operation Mode of the Bridgeless Boost Converter

In the proposed converter, due to the DCM operation mode of the boost converter, the ac line current and voltage are in phase with near unity power factor. Thus, the rectifier input current should be proportional to the applied input voltage:

$$i_a(t) \cong \frac{v_a(t)}{R_e} \quad (4.21)$$

where  $v_a$  is the ac input voltage given by (4.22), and  $R_e$  is the emulated resistance and is represented by (4.23).

$$v_a = V_M \sin(\omega t) \quad (4.22)$$

$$R_e = \frac{v_{a,rms}^2}{P_{av}} = \frac{V_M^2}{2P_{av}} \quad (4.23)$$

In general, the boost converter operates in continuous conduction mode (CCM) if the average inductor current is higher than its current ripple, and operates in discontinuous conduction mode (DCM) if the average inductor current is less than its current ripple. Hence the conditions for CCM and DCM are:

$$\langle i_{LB}(t) \rangle_{T_s} > \frac{\Delta i_{LB}(t)}{2} \quad \text{for CCM} \quad (4.24)$$

$$\langle i_{LB}(t) \rangle_{T_s} < \frac{\Delta i_{LB}(t)}{2} \quad \text{for DCM} \quad (4.25)$$

where  $\langle i_{LB}(t) \rangle_{T_s}$  is the average boost inductor current given by (4.26), and  $\Delta i_{LB}(t)$  is the inductor current ripple shown in (4.27).

$$\langle i_{LB}(t) \rangle_{T_s} = \frac{|v_a(t)|}{R_e} \quad (4.26)$$

$$\Delta i_{LB}(t) = \frac{|v_a(t)|}{L_B} dT_s \quad (4.27)$$

If the boost converter operates in CCM, and if the inductor is small enough that its influence on the low-frequency components of the converter waveforms is negligible, then the duty ratio should follow the function given by (4.28).

$$d(t) = 1 - \frac{|v_a(t)|}{0.5V_{dcl}} \quad (4.28)$$

Substitution of (4.26), (4.27) and (4.28) into (4.24) leads to:

$$L_B > \frac{R_e \left( \frac{1}{2} - \frac{|v_a(t)|}{V_{dcl}} \right)}{f_s} \quad \text{for CCM} \quad (4.29)$$

Since the ac input voltage  $v_a(t)$  is varying from zero to its peak ( $V_M$ ), this equation may not be satisfied at all points on the ac line cycle, particularly when  $v_a(t)$  approaches zero. Hence, considering the worst case scenario (i.e., the time  $v_a(t)$  approaches zero), it can be concluded that the converter operates in CCM over the entire ac line cycle when

$$L_B > \frac{R_e}{2f_s} \quad \text{for CCM} \quad (4.30)$$

When a DCM boost converter operates at a constant duty cycle, the input current approximately follows the input voltage. The converter always operates in DCM when

$$L_B < \frac{\left(1 - \frac{2V_M}{V_{dcl}}\right) R_e}{2f_s} \quad \text{for DCM} \quad (4.31)$$

In the proposed bridgeless boost converter, during the positive half-cycle of the input voltage, the boost inductor discharges into the upper dc-link capacitor  $C_{i1}$ , and in the negative half-cycle discharges into the  $C_{i2}$ . This means that at each half-cycle only one dc-link capacitor incorporates in the boost converter. Noted that the voltage across each dc-link capacitor is half of the dc-link voltage ( $V_{dcl}$ ).  $m_b(t)$  is defined as the front-end converter voltage gain. In CCM the voltage gain of the boost is only a function of duty ratio, given by

$$m_b(t) = \frac{0.5V_{dcl}}{|v_a(t)|} = \frac{1}{1-d(t)} \quad \text{in CCM} \quad (4.32)$$

To derive the boost input characteristic for DCM operation, the steady-state equivalent model of the converter presented in [103] is used. In DCM, the voltage gain of the boost converter is also a function of input current  $i_a(t)$ .

$$m_b(t) = \frac{0.5V_{dcl}}{|v_a(t)|} = 1 + \frac{d^2(t)}{\frac{4L_B f_s}{V_{dcl}} i_a(t)} \quad \text{in DCM} \quad (4.33)$$

To obtain the voltage gain characteristics of the boost converter in DCM, (4.33) can be normalized with (4.34), and the normalize gain given by (4.35).

$$j_a(t) = \frac{4L_B f_s}{V_{dcl}} i_a(t) \quad (4.34)$$

$$m_b(t) = 1 + \frac{d^2(t)}{j_a(t)} \quad \text{in DCM} \quad (4.35)$$

The boundary conduction mode (BCM) characteristics can be expressed by combining (4.32) and (4.35), leading to:

$$j_a(t)m_b^2(t) - m_b(t) + 1 = 0 \quad (4.36)$$

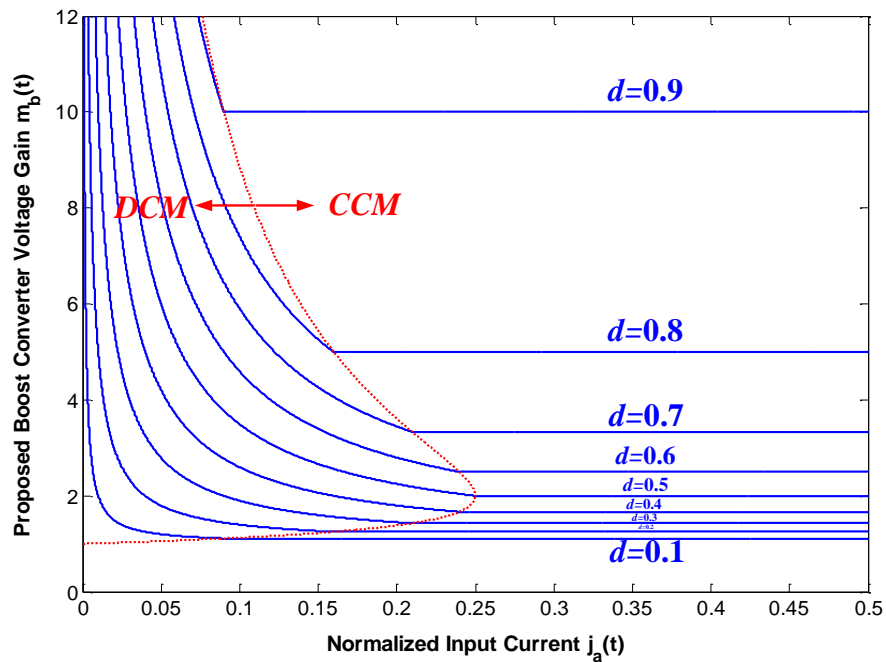


Figure 4.43– Voltage gain characteristics of the proposed boost converter as a function of normalized input current

The gain characteristics of the proposed boost converter for various duty ratios are plotted in Figure 4.43. The BCM is plotted as a red dashed line in this figure. The figure describes that the maximum  $j_a(t)$  occurs at  $d=0.5$  and  $m_b(t)=2$ . This duty ratio is desired in the proposed converter as it offers the widest range of input current while the converter maintains DCM. Figure 4.43 also illustrates that with a constant duty ratio as the sinusoidal input voltage  $v_a(t)$  approaches zero

( $m_b(t) \rightarrow \infty$ ), the converter tends to operate in DCM and as  $v_a(t)$  approaches its peak ( $V_M$ ) ( $m_b(t) \rightarrow 1$ ), the converter tends to operate in CCM. This means that the boost rectifier is more likely to operate in CCM near the peak of the input ac voltage. In the proposed converter that the bridgeless boost converter operates in DCM, the CCM operation of the boost in the peak of input voltage can result in current spikes and harmonic distortion. An example of such condition is shown in Figure 4.44. This condition may also happen when the output is overloaded, as with increasing the normalized input current in Figure 4.43, the converter goes to CCM.

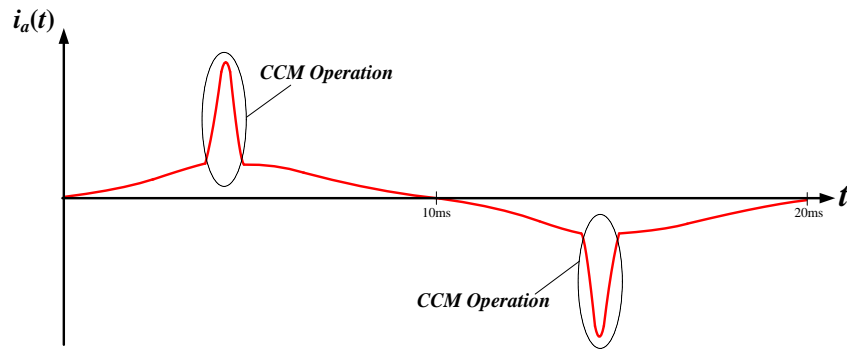


Figure 4.44– AC line current of the DCM boost rectifier example, when the converter operates in CCM at the peak of input voltage

It should be also noted that although PFC can be guaranteed with maintaining DCM in the converter, this approach has the disadvantages of the increased peak currents of DCM and the need for additional filtering of the high-frequency pulsating input currents.

#### 4.2.3.2 Maximum Switch Currents

In the positive half-cycle of the input voltage,  $S_1$  and  $S_2$  have to carry both boost inductor current and resonant current, while  $S_3$  and  $S_4$  only carry the resonant current. This can be also observed

from the operating stages in Figure 4.42. To be more precise, the antiparallel diode of  $S_1$  in the interval  $[t_0 < t < t_1]$  and the MOSFET  $S_2$  in the interval  $[t_4 < t < t_6]$  have to handle the boost inductor current as well as the resonant current. The same occurs for the antiparallel diode of  $S_4$  and the MOSFET  $S_3$  in the negative cycle of input voltage. This means that peak currents of the antiparallel diodes of  $S_1$  and  $S_4$  (minimums of  $i_{s1}$  and  $i_{s4}$ ) and the peak currents of  $S_2$  and  $S_3$  (maximums of  $i_{s2}$  and  $i_{s3}$ ) have to be taken into consideration in the design of the bridgeless boost converter. Due to the symmetrical operation of the converter  $i_{s2,\max} = i_{s3,\max}$  and  $i_{s1,\min} = i_{s4,\min}$ . As can be observed from Figure 4.42, the maximum current going through  $S_2$  is the sum of  $i_{res,\max}$  and  $i_{LB,\max}$ .

To perform the steady state analysis of the proposed topology the following assumptions are made:

- 1) All the components, including semiconductor switches and diodes are ideal.
- 2) The delay between the switches gating signals are neglected.
- 3) The effect of snubber capacitors are neglected.

The Fourier series representation of the input voltage to the resonant circuit  $v_s$  is given by (4.37). Due to the dc blocking function of  $C_{res}$ , only ac components of  $v_s$  are applied to the resonant circuit, where  $V_{dcl}$  is the dc-link voltage;  $d$  represents the duty cycle;  $\theta_h$  is the phase angle that is given by (4.38),  $f_s$  is the operating switching frequency; and  $h$  represents the  $h$ th harmonics.

$$v_s = V_{dcl}(1-D) + \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_{dcl}}{h\pi} \sqrt{1 - \cos(2h\pi(1-d))} \sin(2\pi hf_s t + \theta_h) \right) \quad (4.37)$$

$$\theta_h = \tan^{-1} \left( \frac{\sin(2\pi h(1-d))}{1 - \cos(2\pi h(1-d))} \right) = \pi d - \frac{\pi}{2} \quad (4.38)$$

The relative angular operating frequency ( $\omega_r$ ) is given by (4.39), where  $\omega$  represents the angular operating frequency  $\omega=2\pi f_s$ ;  $\omega_0$  represents the angular resonant frequency (4.40); and  $Q$  is the quality factor which is given by (4.41).

$$\omega_r = \frac{\omega}{\omega_0} \quad (4.39)$$

$$\omega_0 = \frac{1}{\sqrt{L_{res}C_{res}}} \quad (4.40)$$

$$Q = \frac{L_{res}\omega_0}{R_{ac}} \quad (4.41)$$

The resonant current  $i_{res}$  is derived from the ac components of  $v_s$  in (4.37) and given by

$$i_{res} = \sum_{h=1}^{\infty} \left( \frac{\sqrt{2}V_{dcl}}{h\pi|Z_i|} \sqrt{1 - \cos(2h\pi(1-d))} \sin(2\pi hf_s t + \theta_h - \phi_{Zi}) \right) \quad (4.42)$$

where  $|Z_i|$  represents the magnitude of the input impedance of the resonant circuit and  $\phi_{Zi}$  is the phase angle of the input impedance as given by (4.43) and (4.44), respectively.

$$|Z_i| = R_{ac} \sqrt{\left( \frac{(kQ\omega_r)^2}{1 + (kQ\omega_r)^2} \right)^2 + \left( \frac{kQ\omega_r}{1 + (kQ\omega_r)^2} + Q \left( \omega_r - \frac{1}{\omega_r} \right) \right)^2} \quad (4.43)$$

$$\phi_{Z_i} = \tan^{-1} \left( \frac{k Q \omega_r + Q \left( \omega_r - \frac{1}{\omega_r} \right) (1 + (k Q \omega_r)^2)}{(k Q \omega_r)^2} \right) \quad (4.44)$$

where  $k$  is the ratio of the high-frequency transformer magnetizing inductance ( $L_m$ ) to the resonant inductance ( $L_{res}$ ) and is given by

$$k = \frac{L_m}{L_{res}} \quad (4.45)$$

The peak currents of  $S_2$  and  $S_3$  (maximums of  $i_{s2}$  and  $i_{s3}$ ) defined as  $i_{s2,\max}$  is given by (4.46). Based on the first harmonic approximation (FHA), the maximum resonant current  $i_{res,\max}$  can be found by evaluating the resonant current (4.42) with  $h=1$ . The maximum boost inductor current can be also found from Figure 4.41.

$$i_{s2,\max} = i_{res,\max} + i_{LB,\max} \quad (4.46)$$

$$i_{s2,\max} = \frac{\sqrt{2} V_{dcl}}{\pi |Z_i|} \sqrt{1 - \cos(2\pi d)} + \frac{V_M}{L_B} d T_s \quad (4.47)$$

Since the switching frequency  $f_s$  is much higher than the grid frequency (50/60Hz), the grid voltage  $v_a$  is considered constant during each switching period  $T_s$ . Hence, from the voltage gain of the DCM boost converter, the dc-link voltage  $V_{dcl}$  can be expressed as a function of maximum input voltage  $V_M$ :

$$V_{dcl} = V_M \left[ 1 + \sqrt{1 + \frac{2d^2 R}{L_B f_s}} \right] \quad (4.48)$$

Hence,

$$i_{s2,\max} = \frac{\sqrt{2}V_M \left( 1 + \sqrt{1 + \frac{2d^2 R}{L_B f_s}} \right)}{\pi |Z_i|} \sqrt{1 - \cos(2\pi d)} + \frac{V_M}{L_B f_s} d \quad (4.49)$$

The min value for  $Z_i$  is  $R_{ac}$  that happens at resonance, and the duty ratio is desired to be 0.5, as discussed previously. Hence, the switch peak current can be approximated as (4.50).

$$i_{s2,\max} = \frac{V_M}{R_{ac}} \left( \frac{2}{\pi} (1 + \sqrt{1 + \lambda}) + \lambda \right) \quad (4.50)$$

where  $\lambda$  is given by

$$\lambda = \frac{R_{ac}}{2L_B f_s} \quad (4.51)$$

#### 4.2.3.3 RMS Switch Currents

Since the switching frequency is much higher than the ac line frequency, the rms values of the switch currents can be well-approximated as a double integral. The square of the current is integrated first to find its average over a switching period, and the result is then integrated to find the average over the ac line period. The current of switch  $S_2$  ( $i_{s2}$ ) is given as an example as it carries higher rms current compared to switch  $S_1$  ( $i_{s1}$ ). The current going through the switch  $S_2$  consists of a boost inductor current and the resonant current as given by (4.52).

$$i_{s2} = i_{LB} - i_{res1} \quad (4.52)$$

The resonant current (4.42) does not include any line frequency term. However, the boost inductor current varies with the input voltage. The rms current of switch  $S_2$  can be given by

$$I_{S2,rms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_{s2}^2(\tau) d\tau dt} \quad (4.53)$$

where  $T_{ac}$  is the period of ac line. The square of the switch current is integrated first to find its average over a switching period:

$$\frac{1}{T_s} \int_{t_3}^{t_3+T_s} \left[ i_{LB}^2(t) + i_{res}^2(t) - 2i_{LB}(t)i_{res}(t) \right] dt \quad (4.54)$$

Each term is integrated separately and are given by

$$\frac{1}{T_s} \int_{t_3}^{t_3+T_s} i_{LB}^2(t) dt = \frac{1}{T_s} \int_{t_3}^{t_3+T_s} \left[ \frac{v_a(t)}{L_B} (t - t_3) \right]^2 dt = \frac{d^3 T_s^2}{3L_B^2} v_a^2(t) = \alpha v_a^2(t) \quad (4.55)$$

$$\frac{1}{T_s} \int_{t_3}^{t_3+T_s} i_{res}^2(t) dt = \left( \frac{V_{dcl}}{\sqrt{2}\pi|Z_i|} \right)^2 (1 - \cos(2\pi d)) \left( d + \frac{\sin(2\pi d) \cos(2\phi_{zi})}{2\pi} \right) = \beta \quad (4.56)$$

$$\begin{aligned} \frac{1}{T_s} \int_{t_3}^{t_3+T_s} (-2i_{LB}(t)i_{res}(t)) dt = \\ \frac{2\sqrt{2}V_{dcl}}{\pi|Z_i|} \frac{v_a(t)}{L_B} \sqrt{1 - \cos(2\pi d)} \left[ \left( \frac{2}{\omega_s^2} \sin(\pi d) \sin(\phi_{zi}) \right) + \frac{d}{2\pi} \sin(\pi d - \phi_{zi}) \right] = \lambda v_a(t) \end{aligned} \quad (4.57)$$

where the term  $\left( \frac{2}{\omega_s^2} \sin(\pi d) \sin(\phi_{zi}) \right)$  is negligible as the switching frequency is high. Hence,

$$\frac{1}{T_s} \int_{t_3}^{t_3+T_s} (-2i_{LB}(t)i_{res}(t)) dt = \frac{\sqrt{2}dV_{dcl}}{\pi^2|Z_i|} \frac{v_a(t)}{L_B} \sqrt{1 - \cos(2\pi d)} (\sin(\pi d - \phi_{zi})) = \lambda v_a(t) \quad (4.58)$$

The summation of (4.55), (4.56) and (4.58) are then integrated over the ac line period to find the rms switch current. As discussed earlier, the term related to the resonant current (4.56) remains constant in the integral over the  $T_{ac}$ . However, (4.56) and (4.58) can be integrated over

the line frequency since they include  $v_a(t)$ . It should be noted that during the negative half-cycle of input voltage, switch  $S_2$  carries only the resonant current. Hence, rms current of switch  $S_2$  over the positive half-cycle of input voltage ( $I_{S2,rms}^+$ ) and negative half-cycle ( $I_{S2,rms}^-$ ) are given by (4.59) and (4.60), respectively.

$$I_{S2,rms}^+ = \sqrt{\frac{1}{0.5T_{ac}} \int_0^{0.5T_{ac}} \left[ \alpha (V_M \sin(\omega t))^2 + \beta + \lambda V_M \sin(\omega t) \right] dt} = \sqrt{\alpha \frac{V_M^2}{2} + \beta + \lambda \frac{2V_M}{\pi}} \quad (4.59)$$

$$I_{S2,rms}^- = \sqrt{\beta} \quad (4.60)$$

#### 4.2.3.4 Voltage Gain

The voltage gain characteristics of the front-end bridgeless rectifier were presented in the previous section. The overall voltage gain equation can be obtained by first analyzing each resonant circuit module. Due to the asymmetrical square voltage generated at the output of each inverter, the input voltage to the resonant circuit ( $v_s$ ) was represented by (4.37), the rms value of  $v_s$  is then given by (4.61).

$$V_s = \frac{V_{dcl}}{\pi} \left[ \sum_{n=1}^{\infty} \frac{1 - \cos(2n\pi d)}{n^2} \right]^{1/2} \quad (4.61)$$

The voltage gain of each *LLC* resonant circuit is given by

$$\frac{V_p}{V_s} = \frac{1}{\sqrt{\left( 1 + \frac{1}{k} \left( 1 - \frac{1}{\omega_r^2} \right) \right)^2 + \left( Q \left( \omega_r - \frac{1}{\omega_r} \right) \right)^2}} \quad (4.62)$$

where  $V_p$  is the rms voltage of the primary side 1:1 transformer. The voltage gain of the front-end bridgeless rectifier is also presented in (4.48). Considering the voltage quadrupler rectifier with a gain of 4, the total voltage gain of the converter for each phase can be given by

$$\frac{V_{o1}}{V_M} = \frac{4 \left[ 1 + \sqrt{1 + \frac{2d^2 R}{L_B f_s}} \right] \left[ \sum_{n=1}^{\infty} \frac{1 - \cos(2n\pi d)}{n^2} \right]^{1/2}}{\pi \sqrt{\left( 1 + \frac{1}{k} \left( 1 - \frac{1}{\omega_r^2} \right) \right)^2 + \left( Q \left( \omega_r - \frac{1}{\omega_r} \right) \right)^2}} \quad (4.63)$$

As discussed previously, the desired operating duty ratio in the proposed converter is  $d=0.5$ . Therefore, to simplify the overall voltage gain of the converter, the duty ratio is considered 0.5. According to Figure 4.43, the gain of PFC bridgeless boost converter with  $d=0.5$  for each half-cycle of ac input voltage can be approximated as 2, as converter operates close to BCM. The rms value of the input voltage to the resonant circuit with  $d=0.5$  is given by

$$V_s = \frac{V_{dcl}}{\pi} \left[ \sum_{n=1}^{\infty} \frac{1 - \cos(2n\pi d)}{n^2} \right]^{1/2} \bigg|_{d=0.5} = V_{dcl} \frac{\sqrt{2}}{\pi} \left[ \sum_{n=odd} \frac{1}{n^2} \right]^{0.5} = \frac{V_{dcl}}{2} \quad (4.64)$$

Hence, the total voltage-gain of each phase in the proposed converter with  $d=0.5$  can be approximated as

$$\frac{V_{o1}}{V_M} = \frac{8}{\pi \sqrt{\left( 1 + \frac{1}{k} \left( 1 - \frac{1}{\omega_r^2} \right) \right)^2 + \left( Q \left( \omega_r - \frac{1}{\omega_r} \right) \right)^2}} \quad (4.65)$$

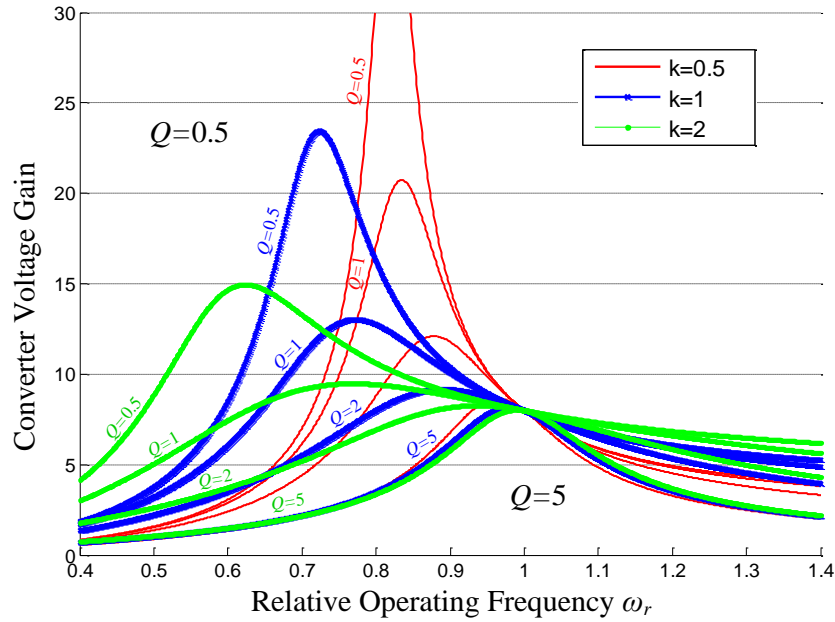


Figure 4.45– Voltage gain of the proposed converter per phase with  $d=0.5$

To illustrate the relationship between the voltage gain and the relative operating frequency, a plot of (4.65) as a function of relative operating frequency ( $\omega_r$ ) for different  $Q$  and  $k$  is shown in Figure 4.45. The gain characteristics of the proposed converter shows as the ratio of the transformer magnetizing inductance to the resonant inductance ( $k=L_m/L_{res}$ ) is increased, the converter takes the characteristics of a series resonant converter and the voltage gain reduces. However, circulating current and conduction losses will decrease as the size of  $L_m$  increases which improves the efficiency.

#### 4.2.4 Experimental and Simulation Results

To verify the performance of the proposed topology, a three-phase 2-kW, 145-V<sub>ac</sub>/4-kV laboratory scale proof-of-concept prototype was first designed using the approaches discussed in section 4.2.3. The detailed design procedure is provided in the following section. The converter was simulated in PSIM and the proof-of-concept prototype was built in the laboratory as shown in Figure 4.46. The experimental results are well matched with the simulation results as illustrated below. To further verify the performance of the proposed converter for MW scale in wind energy applications, a 1 MW wind turbine from Nordic Windpower (N1000) was simulated in PSIM.

##### 4.2.4.1 Design Procedures

The drain-source breakdown voltage ( $V_{DSS}$ ) of the employed SCT3030AL SiC MOSFETs is 650V. Since the stress of the voltage across each switch in the proposed converter is half of the dc-link voltage, the maximum voltage across each switch is designed to be 450 V, meaning the dc-link voltage  $V_{dcl}=900$  V. The output power for each phase is 667 W, and the switching frequency is selected to be around 32 kHz. From (4.31), the condition for DCM is:

$$L_B < \frac{\left(1 - \frac{2V_M}{V_{dcl}}\right) R_e}{2f_s} \quad \text{for DCM} \quad (4.66)$$

where  $R_e$  is the emulated resistance of the bridgeless rectifier and  $V_M$  is the peak of the ac line voltage ( $v_a$ ). When line current harmonics and losses are neglected, the bridgeless rectifier emulated resistance  $R_e$  at the rated power is

$$R_e = \frac{V_M^2}{2P_a} = \frac{205^2}{2 \times 667} = 31.5 \text{ ohm} \quad (4.67)$$

Given  $V_M=205$  V and  $R_e$  found from (4.67), and considering a gain of 4.4 for the bridgeless boost with  $V_{dcl}=900$  V, (4.66) gives  $L_B < 267 \mu\text{H}$  for DCM operation of the converter.

The output voltage of each phase is  $4\text{kV}/3$  with the nominal power of  $667$  W. Then, the equivalent ac resistance can be given by (4.14).

$$R_{ac} = \frac{1}{2\pi^2} \frac{V_o^2}{P_o} = 135\Omega \quad (4.68)$$

Assuming the switching frequency is in a range of  $32$  kHz,  $d=0.5$  and a gain of around  $4.4$  for front-end bridgeless rectifier ( $V_{dcl}/V_M$ ), from (4.48) the exact value of boost inductor can be calculated by

$$L_B = \frac{2R_{ac}d^2}{f_{sw} \left[ \left( \frac{V_{dcl}}{V_M} - 1 \right)^2 - 1 \right]} = \frac{2 \times 135 \times 0.5^2}{32 \times 10^3 \times \left[ \left( \frac{900}{145\sqrt{2}} - 1 \right)^2 - 1 \right]} = 200\mu\text{H} \quad (4.69)$$

From (4.70), the maximum switch current of  $S_2$  ( $i_{s2,\max}$ ) at  $d=0.5$  can be calculated

$$i_{s2,\max} = \frac{V_M}{R_{ac}} \left( \frac{2}{\pi} \left( 1 + \sqrt{1 + \frac{R_{ac}}{2L_B f_s}} \right) + \frac{R_{ac}}{2L_B f_s} \right) = 20.3\text{A} \quad (4.70)$$

Regarding the resonant circuit component parameters, with a switching frequency  $f_{sw}$  of  $32$ -kHz. The rms value of  $v_s$  is given by

$$V_s = \frac{V_{dcl}\sqrt{2}}{\pi} \left[ \sum_{n=\text{odd}} \frac{1}{n^2} \right]^{1/2} = \frac{V_{dcl}}{2} = 450\text{v} \quad (4.71)$$

To achieve a voltage gain of 6.5 for each phase, according to (4.65), with  $k$  and  $Q$  chosen to be 1.7 and 0.5, respectively, the relative angular frequency for each sub-module can be calculated to be:  $\omega_r=1.25$ . Hence, the angular resonant frequency can be found by

$$\omega_0 = \frac{\omega}{\omega_r} = \frac{2\pi f_{sw}}{1.25} = 1.6 \times 10^5 \quad (4.72)$$

The resonant inductor is then calculated by

$$\text{resonant inductor } (L_{res}) = \frac{QR_{ac}}{\omega_0} = 421\mu H \quad \text{choose: } 400\mu H \quad (4.73)$$

Since  $k = 1.7$ , the magnetizing inductance of each transformer is calculated to be 700 $\mu$ H with a turns-ratio of 1:1. Finally, the resonant capacitor is then given by

$$\text{resonant capacitor } (C_{res}) = \frac{1}{(\omega_0)^2 L_s} = 97.6nF \quad \text{choose: } 100nF \quad (4.74)$$

#### 4.2.4.2 Experimental and Simulation Results of the Laboratory-Scale Converter

ROHM SiC power MOSFETs were utilized in the prototype implementation. The circuit parameters, component model numbers of the prototype and the system specifications are given in Table 4.3, according to the design procedures presented in the previous section. A picture of 2 kW, 4 kV laboratory scale experimental prototype is shown in Figure 4.46.

Table 4.3– Specifications and Components for the Proof-of-Concept Prototype

Prototype Specifications	
Rated power:	2kW
Input voltage:	145V <sub>L-N,RMS</sub>
Output medium voltage:	4kV
# of modules:	3
Components Part Number and Values Per Module	
Switches :	SiC MOSFET, SCT3030 (650V, 70A, 30mΩ)
Input rectifier diodes :	SiC diodes, STPSC15H12D (1.2kV, 15A)
Input Inductors:	Ferrite core E N87, 1.36 mH
Filter Capacitors:	2μF, 400V <sub>ac</sub> , Film Cap
Boost Inductors:	Ferrite core E N87, 200 μH
DC-link capacitors:	EZP-E50107MTA (100μF, 500V)
Snubber capacitors:	10nF, 1kV
Resonant capacitor:	100nF, 1.6kV
Resonant inductor:	Ferrite core E N87, 403 μH
High frequency transformer:	Ferrite core E N87, 689 μH, (1:1)
High-gain rectifiers:	SiC Schottky, GP2D005A170B (1.7kV, 5A)
Output capacitors:	MKP, Film Cap (5μF, 1.3 kV)

Figure 4.47 – Figure 4.50 show the three input voltages, almost-sinusoidal input currents, and the output dc voltage at the rated power condition in 2 kW simulation and experimental results. The 4 kV output voltage ripple is less than 1%, as shown in Figure 4.49. Figure 4.50 shows the measured three-phase input currents that are completely balanced with almost sinusoidal waveforms. The input power factor of PF=0.992, measured by MSOX6004A KEYSIGHT digital oscilloscope, is shown in Figure 4.51. The per phase simulated and experimental input current along with DCM boost inductor current are shown in Figure 4.52 and Figure 4.53, respectively. Switching waveforms for SiC MOSFETs in phase *a* are also illustrated in Figure 4.54 and Figure 4.55 at both line-frequency and switching frequency. It can be observed that ZVS turn-ON

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are achieved in the switches. ZCS turn-OFF operations of the switches can be observed from Figure 4.55(c), which shows the turn-OFF transition of the switches.

The resonant current in three phases ( $a$ ,  $b$  and  $c$ ) are shown in Figure 4.56 and Figure 4.57. The balanced rms values of the resonant currents are measured in Figure 4.57. The balanced primary voltages of high frequency transformers are illustrated in Figure 4.58 and Figure 4.59. The error among the resonant currents and HF transformers' primary voltages are measured to be around 1%, which verifies that all the modules are well-balanced in the prototype.

Figure 4.60 and Figure 4.61 show the current and voltage waveforms in one of the output high-gain rectifier diodes. It can be observed that ZCS turn-ON and OFF are achieved. Finally, ZCS operation of the diodes in bridgeless front-end rectifier in Figure 4.62 and Figure 4.63 verify the soft-switching operation of the entire converter. The measured full-load efficiency of the converter is 97%.

The prototype's performance at reduced load condition was verified when the output power reduced by 50%. Figure 4.64 shows the measured three-phase input currents with an input power factor of 0.971 illustrated in Figure 4.65. Figure 4.66 shows the switching waveforms in phase  $a$  when the power is around 1 kW. It can be observed that soft-switching turn-ON and OFF are achieved in the switches.

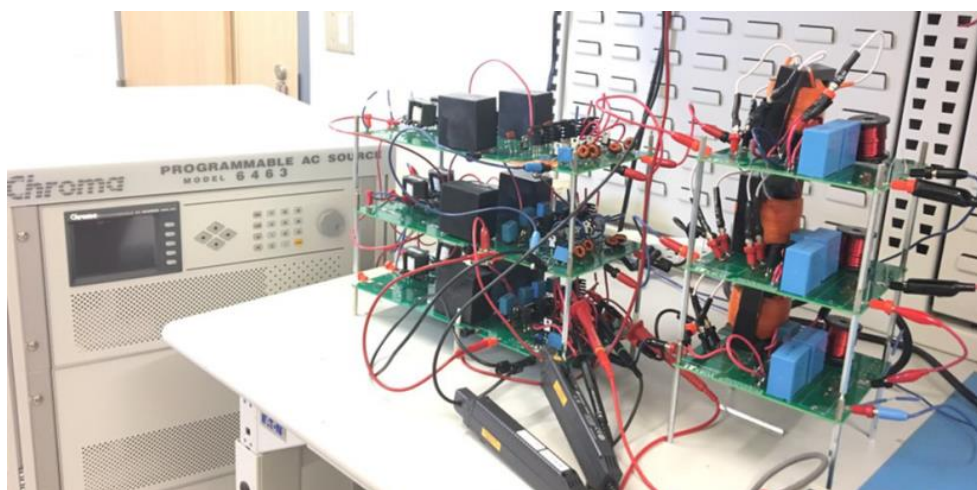


Figure 4.46– 2kW, 4kV output laboratory scale experimental prototype

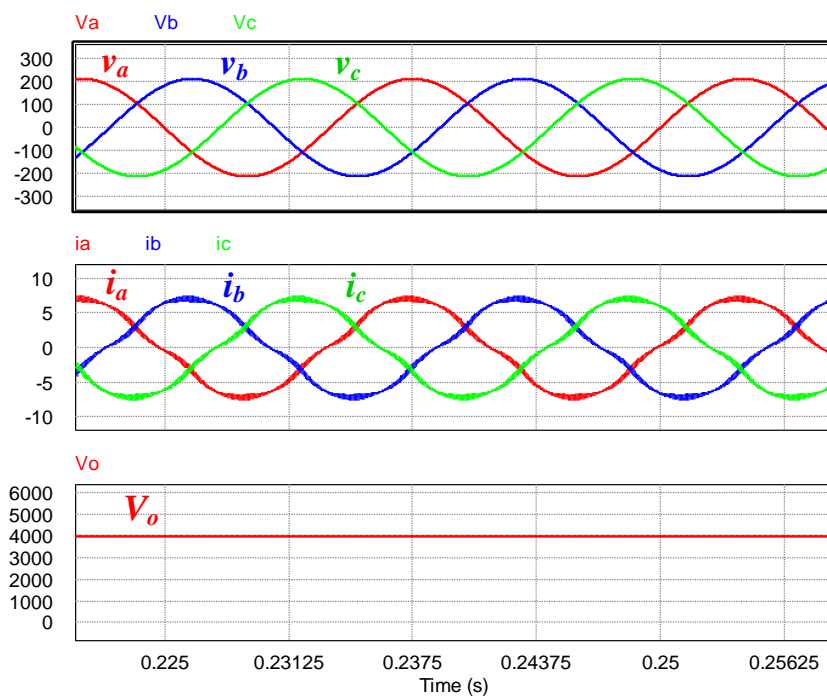
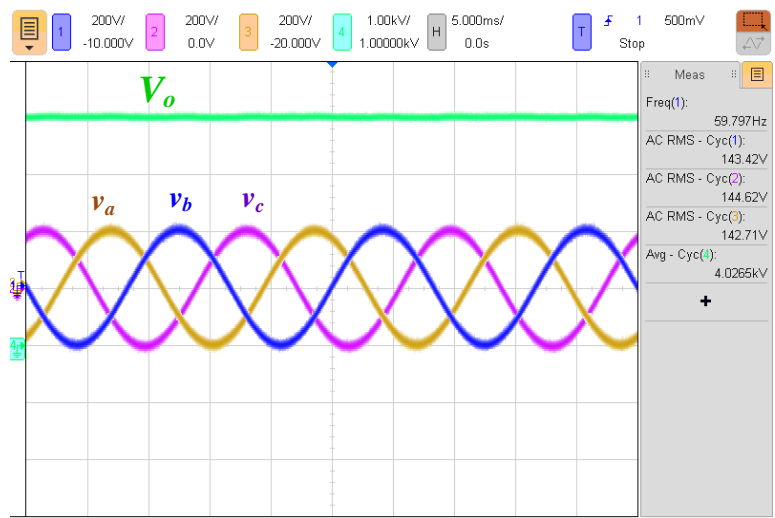
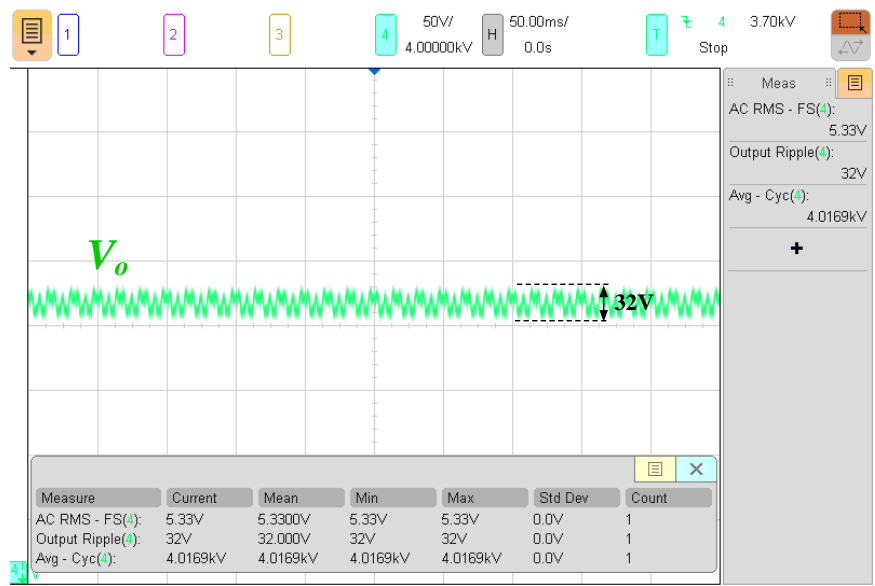


Figure 4.47– Input voltages, input current and output load voltage ( $V_o$ ) in 2kW simulation



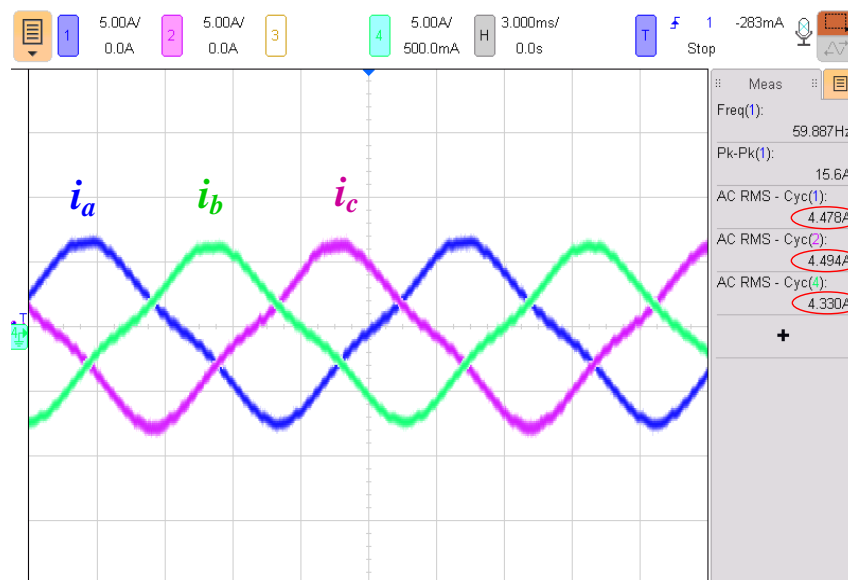
[ $V_o$ : 2kV/div;  $v_a$ ,  $v_b$ ,  $v_c$ : 200V/div; time: 5ms/div]

Figure 4.48– Measured three-phase input voltages and output load voltage ( $V_o$ )



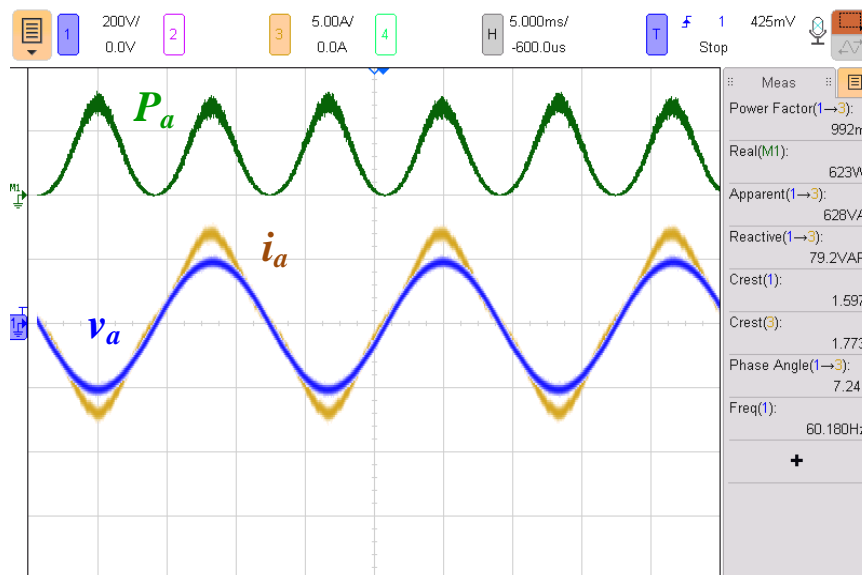
[ $V_o$ : 50V/div; time: 50ms/div]

Figure 4.49– Measured output load voltage ( $V_o$ ) ripple



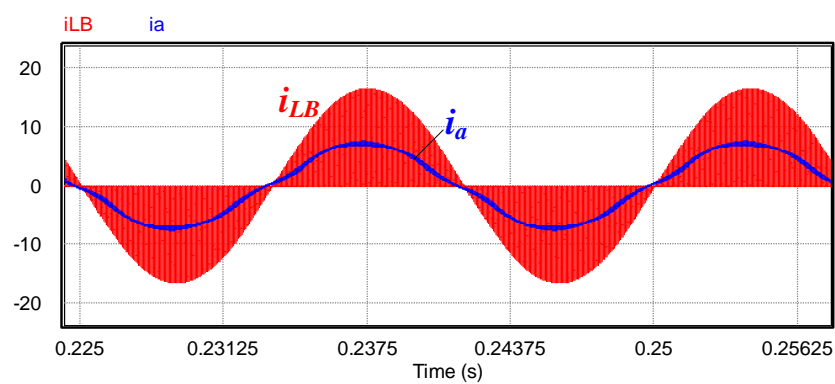
[ $i_a$ ,  $i_b$ ,  $i_c$ : 5A/div; time: 3ms/div]

Figure 4.50– Measured three-phase input currents at the rated power

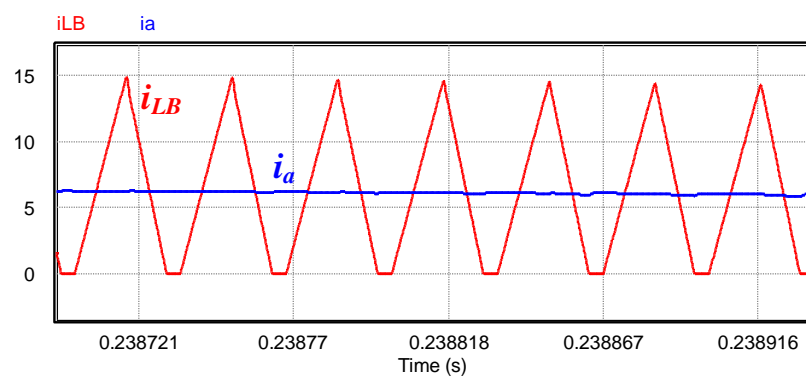


[ $v_a$ : 200V/div;  $i_a$ : 5A/div; time: 5ms/div]

Figure 4.51– Measured power factor at full-load condition

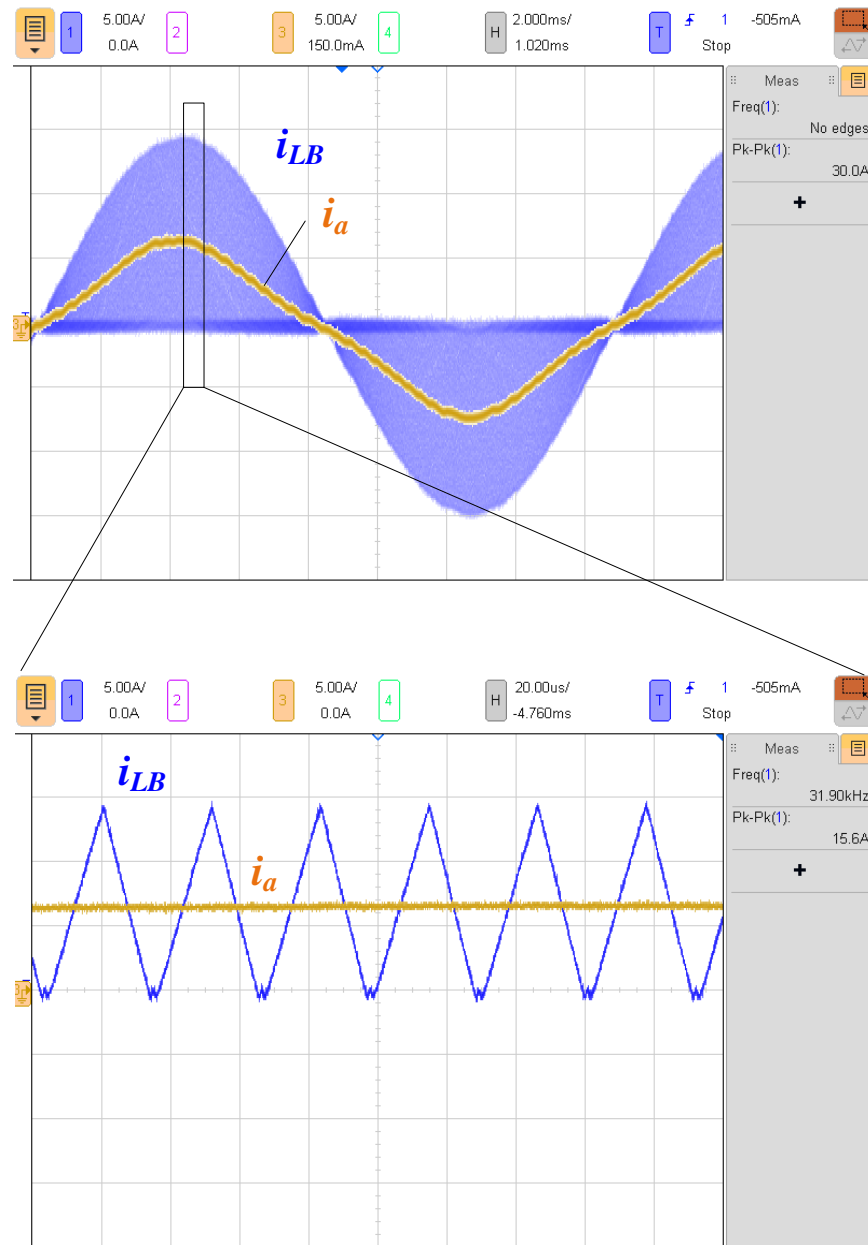


(a)



(b)

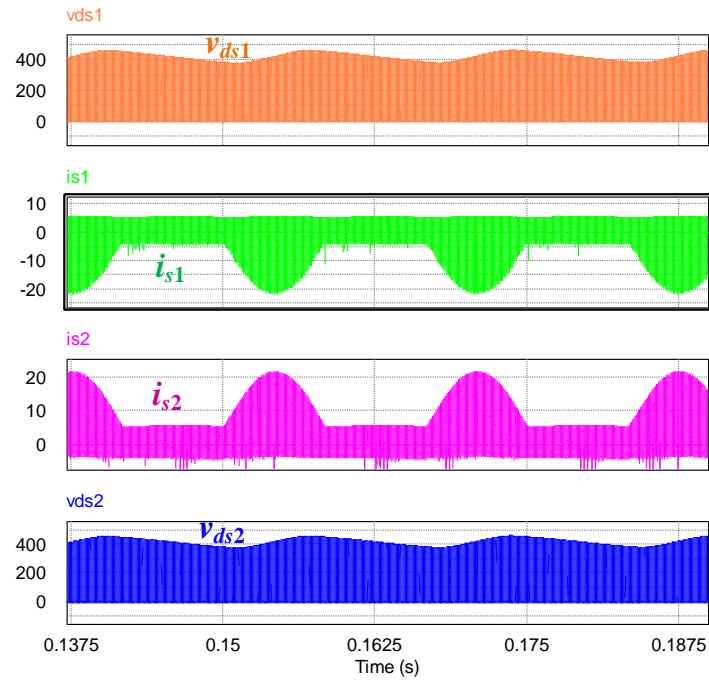
Figure 4.52– Simulated sinusoidal input current and boost inductor current; (a) line frequency waveforms, (b) high-frequency waveforms



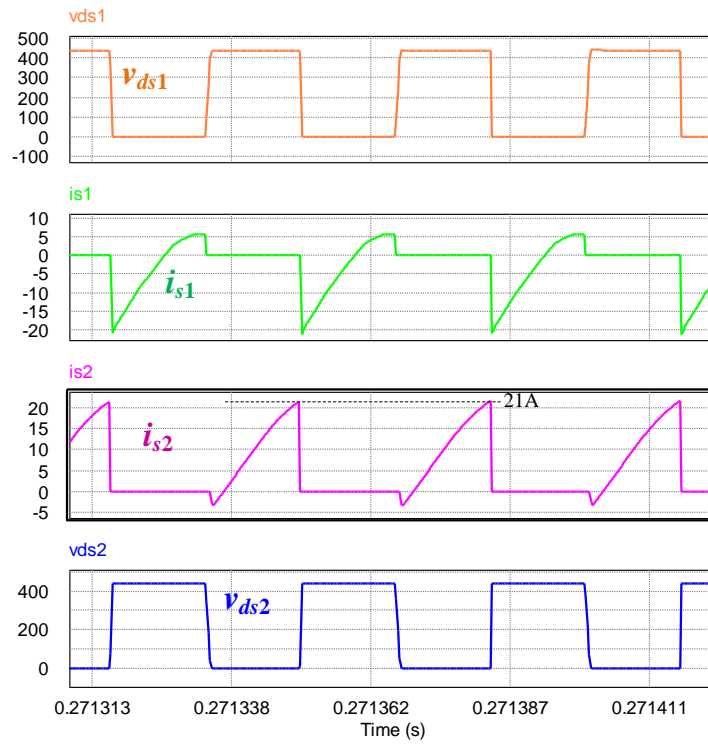
(a) [ $i_{LB}$ : 5A/div;  $i_a$ : 5A/div; time: 2ms/div]

(b) [ $i_{LB}$ : 5A/div;  $i_a$ : 5A/div; time: 20μs/div]

Figure 4.53— Measured sinusoidal input current and boost inductor current in phase  $a$ ; (a) line frequency waveforms, (b) high-frequency waveforms

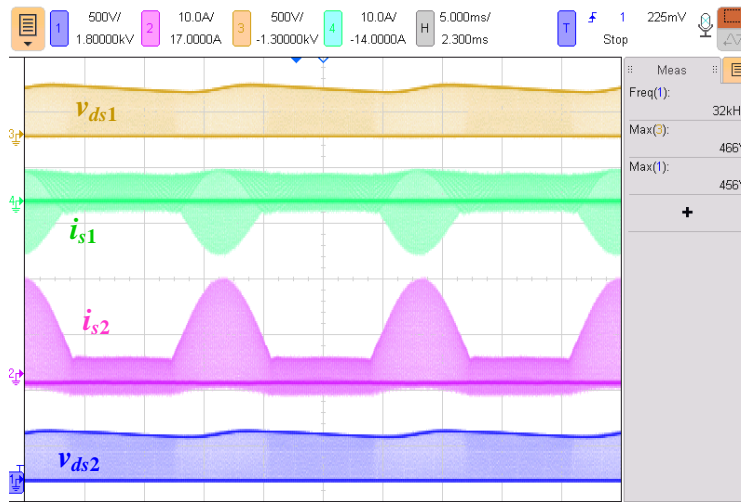


(a)

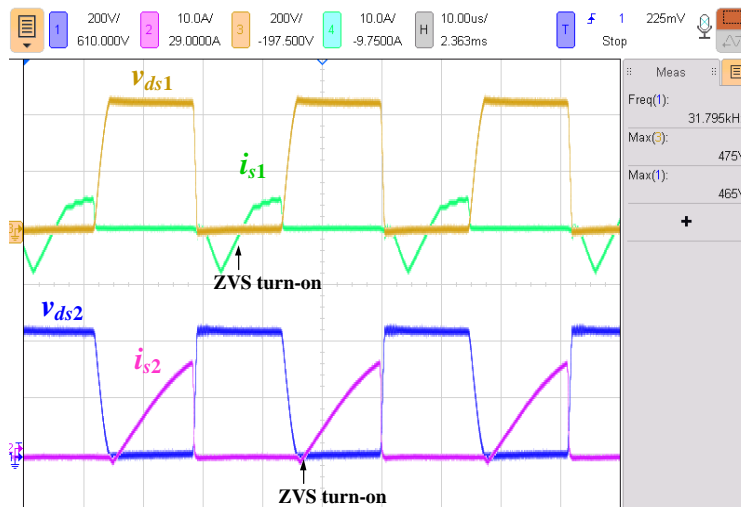


(b)

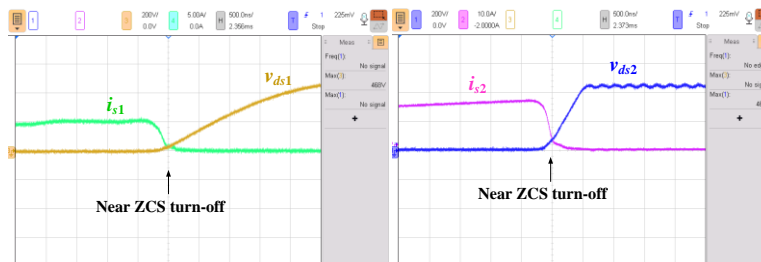
Figure 4.54– Switching waveforms in 2kW simulation; (a) line frequency waveforms, (b) high-frequency waveforms



(a) [ $i_{s1}, i_{s2}$ : 10A/div;  $v_{ds1}, v_{ds2}$ : 500V/div; time: 5ms/div]

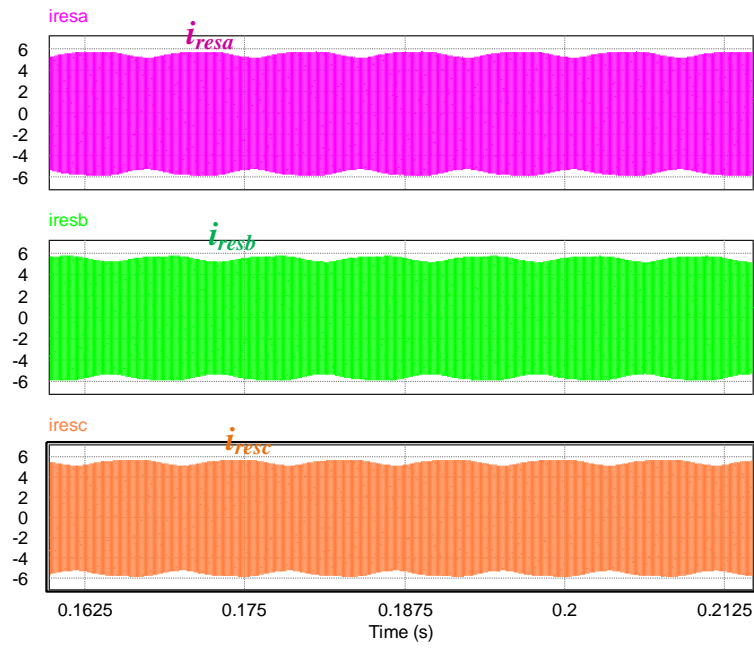


(b) [ $i_{s1}, i_{s2}$ : 10A/div;  $v_{ds1}, v_{ds2}$ : 200V/div; time: 10μs/div]

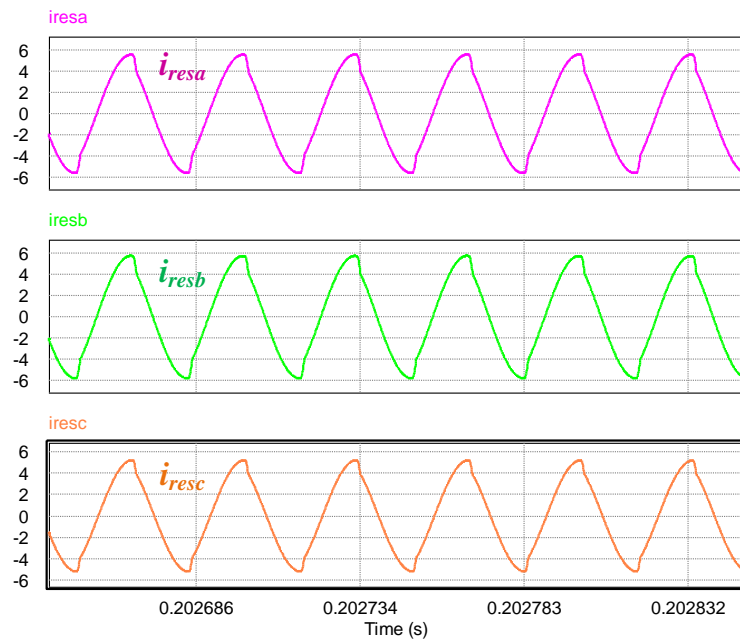


(c) [ $i_{s1}, i_{s2}$ : 5A/div;  $v_{ds1}, v_{ds2}$ : 200V/div; time: 0.5μs/div]

Figure 4.55– Measured switching waveforms (phase *a*); (a) line frequency waveforms, (b) high-frequency waveforms, (c) turn-OFF transition of the switches



(a)



(b)

Figure 4.56– Three phase resonant currents in 2kW simulation; (a) line frequency waveforms, (b) high-frequency waveforms

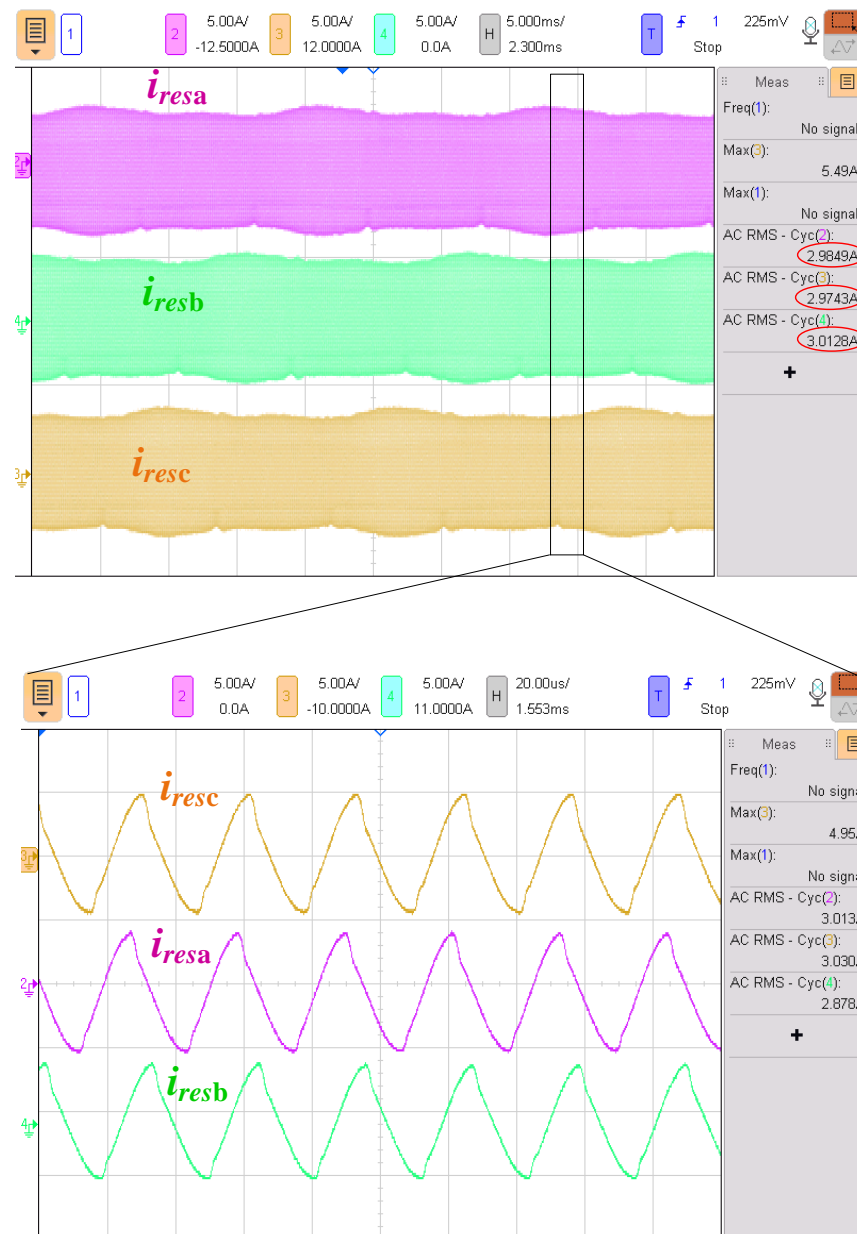


Figure 4.57– Measured three phase resonant currents in 2kW prototype; (a) line frequency waveforms, (b) high-frequency waveforms

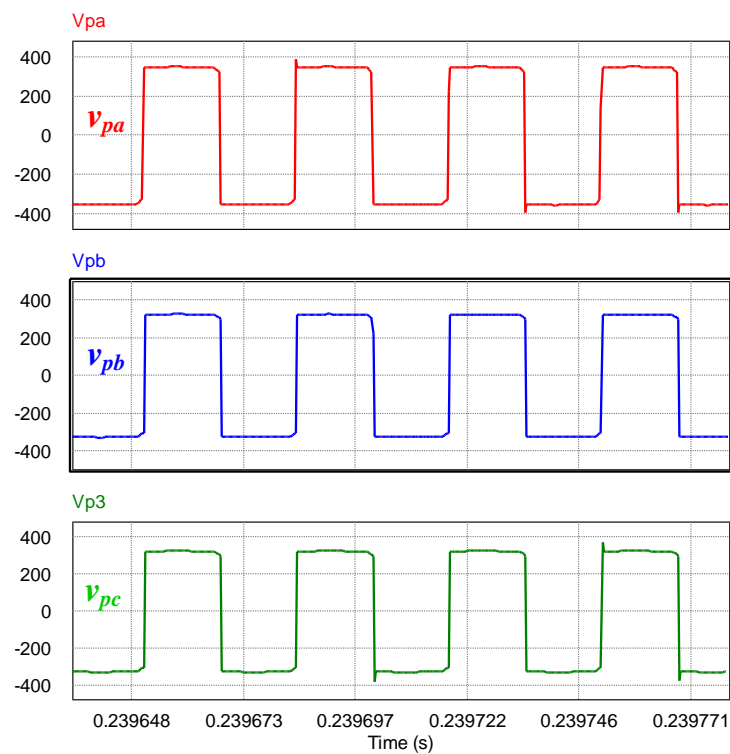
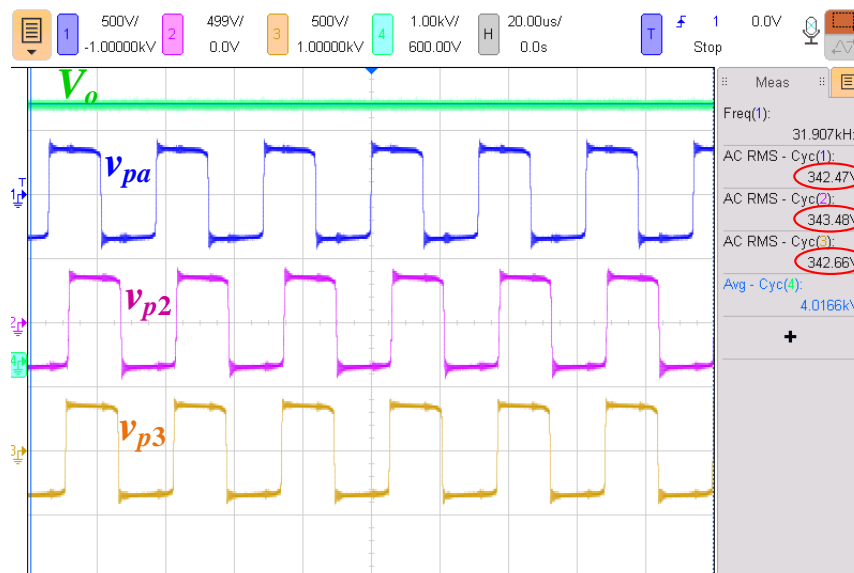


Figure 4.58– Simulated primary voltages of high-frequency transformers



[ $V_o$ : 1kV/div;  $v_{p1}$ ,  $v_{p2}$ ,  $v_{p3}$ : 500V/div; time: 20 $\mu$ s/div]

Figure 4.59– Measured primary voltages of high-frequency transformers

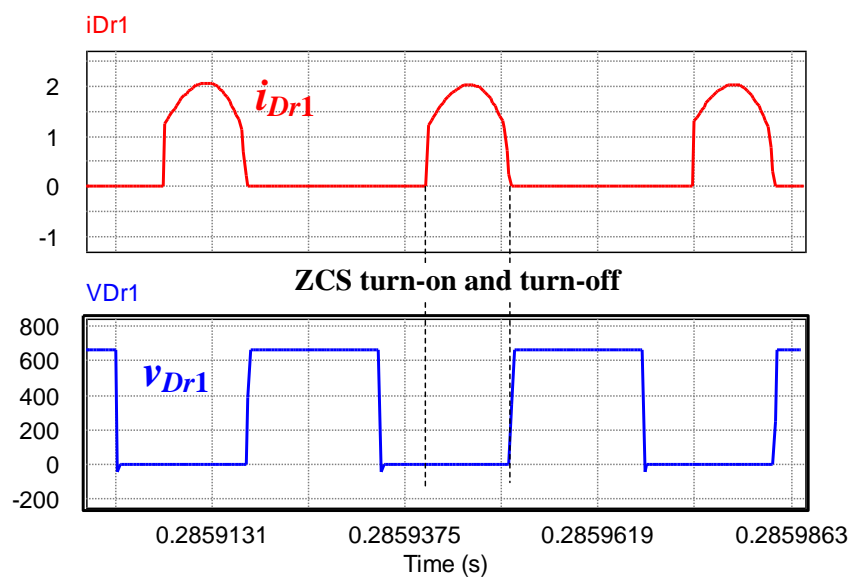
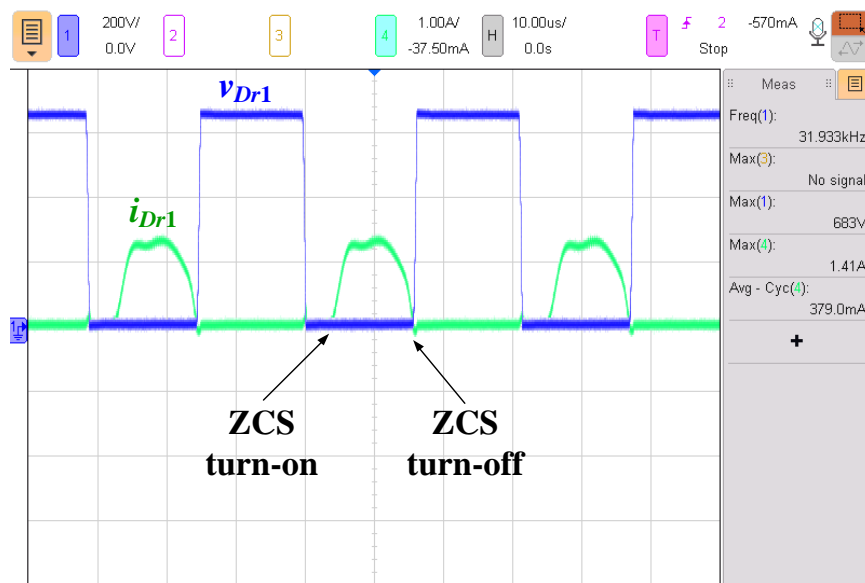


Figure 4.60– Simulated diode waveforms in high-frequency high-gain rectifier



[ $v_{Dr1}$ : 200V/div;  $i_{Dr1}$ : 1A/div; time: 10 $\mu$ s/div]

Figure 4.61– Measured diode waveforms in high-frequency high-gain rectifier

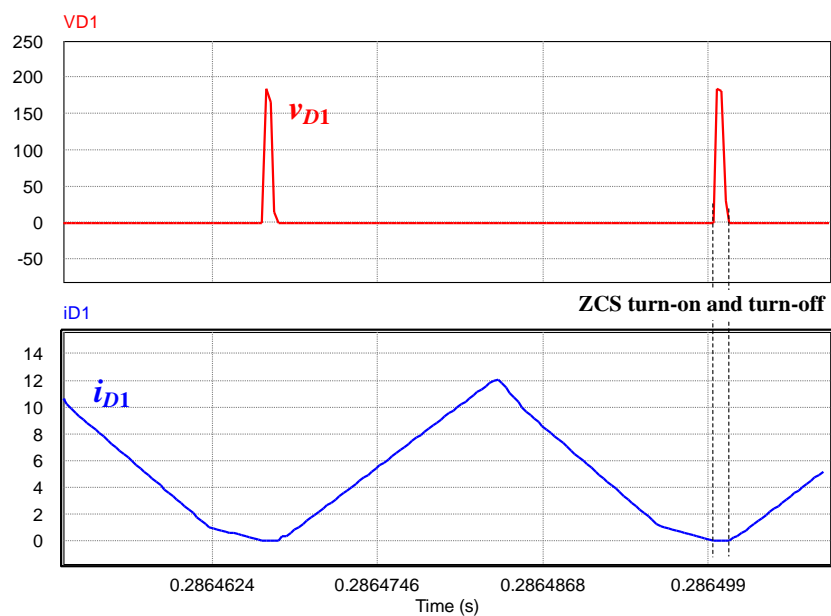
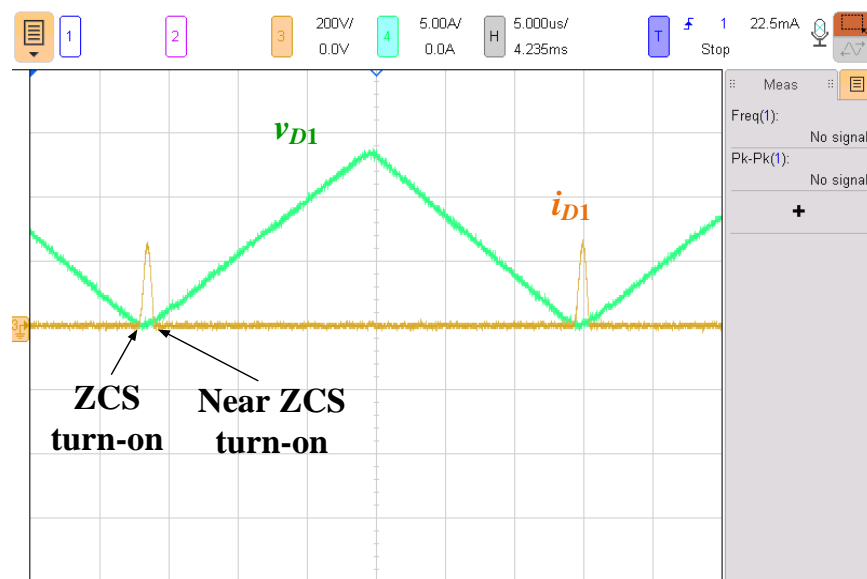
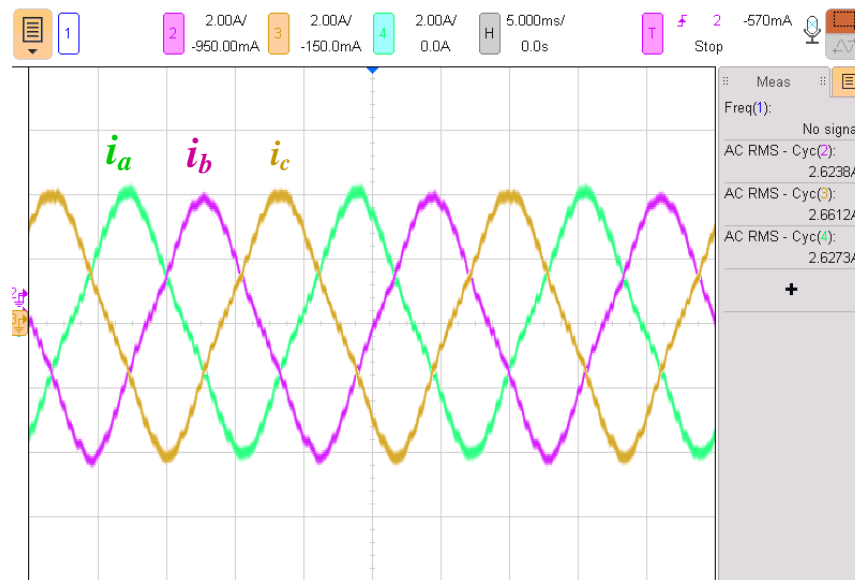


Figure 4.62– Simulated diode waveforms in bridgeless front-end rectifier



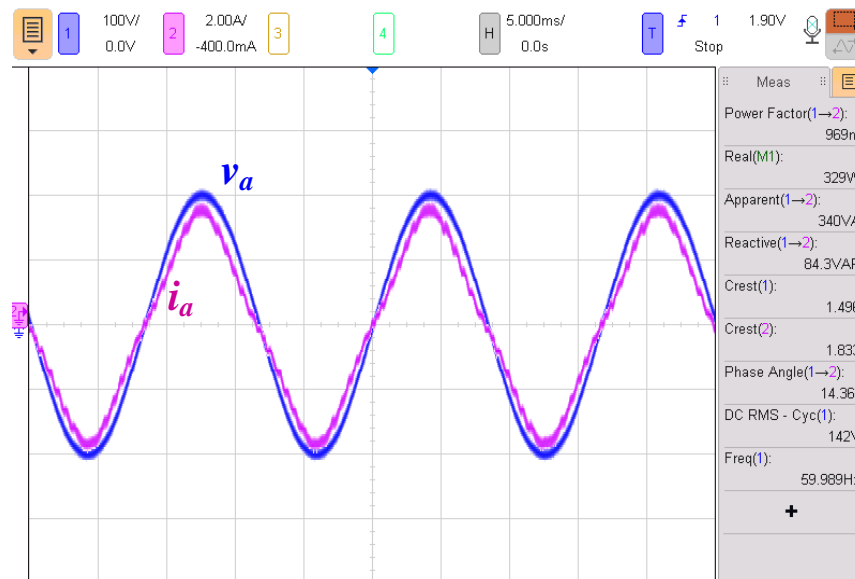
$[v_{D1}: 200\text{V/div}; i_{D1}: 1\text{A/div}; \text{time}: 10\mu\text{s/div}]$

Figure 4.63– Measured diode waveforms in bridgeless front-end rectifier



[ $i_a$ ,  $i_b$ ,  $i_c$ : 2A/div; time: 3ms/div]

Figure 4.64– Measured three-phase input currents at reduced load condition



[ $i_a$ ,  $i_b$ ,  $i_c$ : 2A/div; time: 3ms/div]

Figure 4.65– Measured per phase input voltage, input current and power factor at reduced load condition

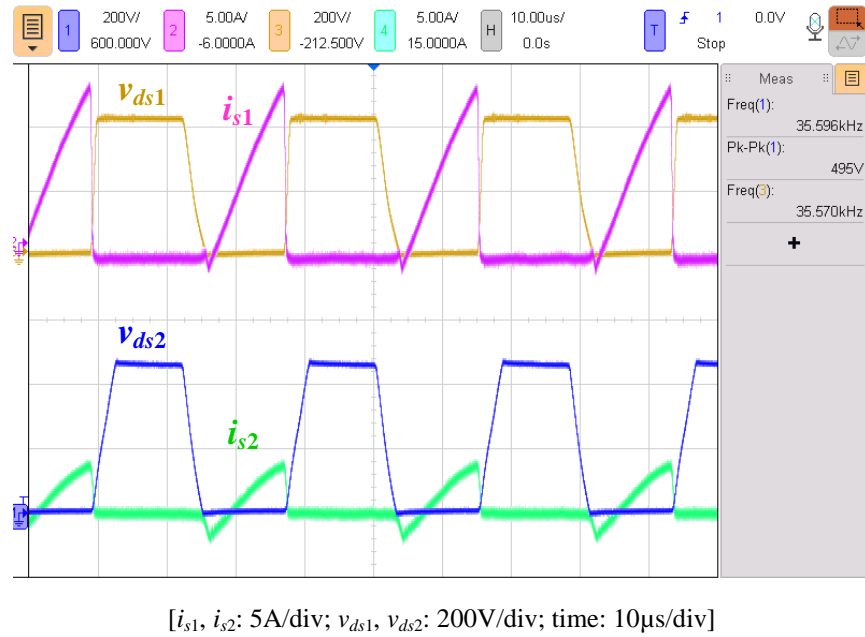


Figure 4.66– Measured switching waveforms (phase *a*) at reduced load condition

#### 4.2.4.3 Simulation Results of a High Power Wind Turbine

A 1-MW, 690-V<sub>ac</sub> wind turbine from Nordic Windpower (N1000) was used in the simulation of the proposed converter in PSIM. The achieved dc output voltage is 30 kV<sub>DC</sub>. 1200 V, 5.0 m $\Omega$ , silicon carbide, half-bridge modules (CAS300M12BM2) from CREE are used to implement the switches in the proposed converter. Simulated wind turbine specifications and the circuit parameters in the simulation are summarized in Table 4.4.

Table 4.4– Specifications and Components for the Simulated 1 MW Wind Turbine Converter

Vestas V44 Specifications	
Rated Power	1000 kW
Generator	690 V <sub>AC</sub> , 50Hz
Gear Box	three-stage planetary
Cut-in Wind Speed	4 m/s
Rated Wind Speed	16 m/s
Cut-out Wind Speed	22 m/s
Rotor Diameter	59 m
Wind Class	IEC IIA
Simulation Specifications	
Rated Power	1MW
Output Medium Voltage $V_o$	30kV <sub>DC</sub>
Number of Modules (Per Phase)	3
Switching freq. $f_s$ (at full-load)	~18kHz per module
Circuit Components in Simulation	
SiC MOSFETs	CAS300M12BM2, CREE (1.2kV, 404A, 5.0 m $\Omega$ )
Snubber Capacitors	ECW-H16153JV, Panasonic (0.015 $\mu$ F, 1.6kV <sub>DC</sub> )
DC-link Capacitors	Series 947D591K132DJRSN (590 $\mu$ F, 1.3kV <sub>DC</sub> )
Resonant Capacitors	Four in series T50W1NR-F, Cornell, (0.25 $\mu$ F, 5kV <sub>DC</sub> )
High Frequency 1:1 Transformers	500 $\mu$ H (1:1)
Resonant Inductors	403 $\mu$ H
Bridgless Diodes	SiC Schottky GB2X50MPS17-227, GeneSiC, (1.7kV, 136A)
High-Gain Rectifier Diodes	SiC Schottky GB10MPS17-247, GeneSiC, (1.7kV, 50A)
Output Capacitors	B25856K2405K3 (5uF, 4kV <sub>DC</sub> )

Figure 4.67 shows the three-phase input voltages, 30 kV MVdc grid voltage and sinusoidal input currents. Current and voltage waveforms of SiC MOSFETs are illustrated in Figure 4.68, where ZVS and ZCS have been achieved for all MOSFETs using 15 nF snubber capacitors. As discussed earlier, the voltage stress across each switch is half of the dc-link voltage. The duty ratio of  $d=0.5$  is chosen as the switching frequency is 18 kHz. The balanced resonant circuits are shown in Figure 4.69. Diode waveforms in high-frequency high-gain rectifier in 1 MW simulation are illustrated in Figure 4.70. The efficiency of the converter is more than 96%.

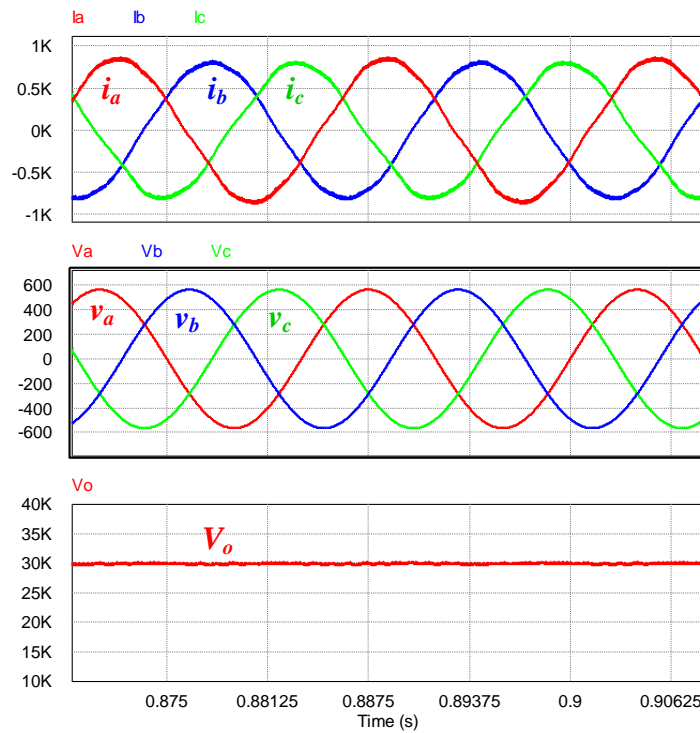


Figure 4.67– Input voltages, output load voltage ( $V_o$ ), and input currents in 1 MW simulation

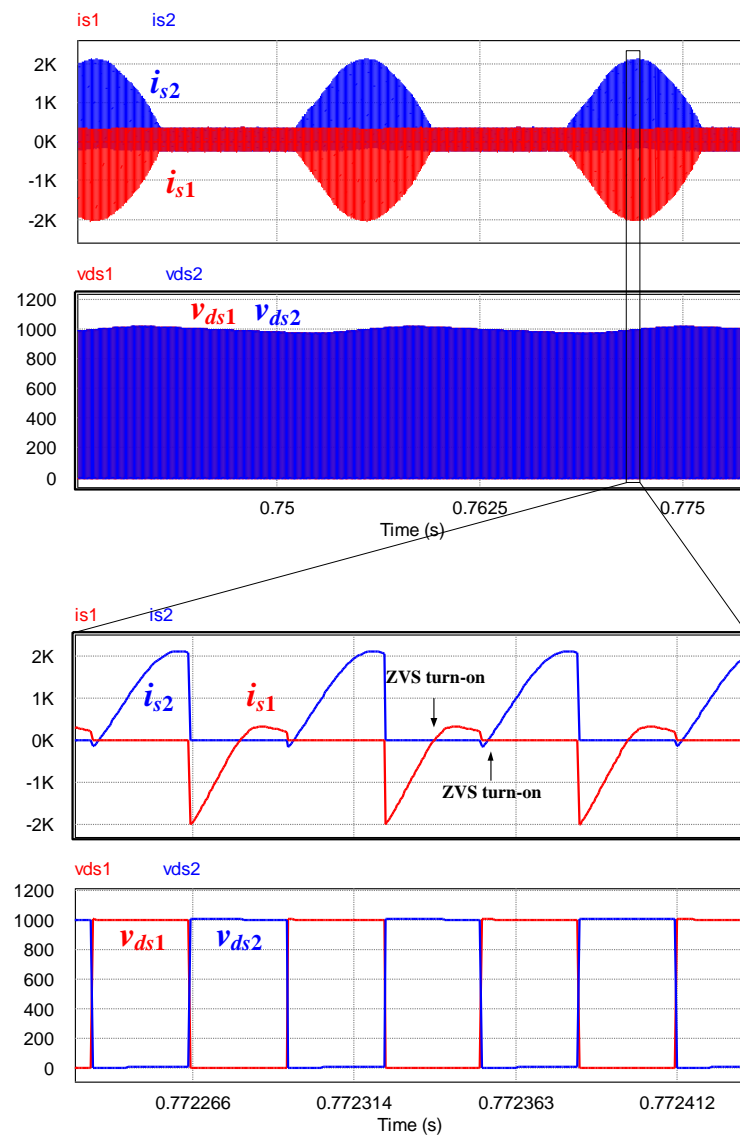


Figure 4.68– Switching waveforms in 1 MW simulation

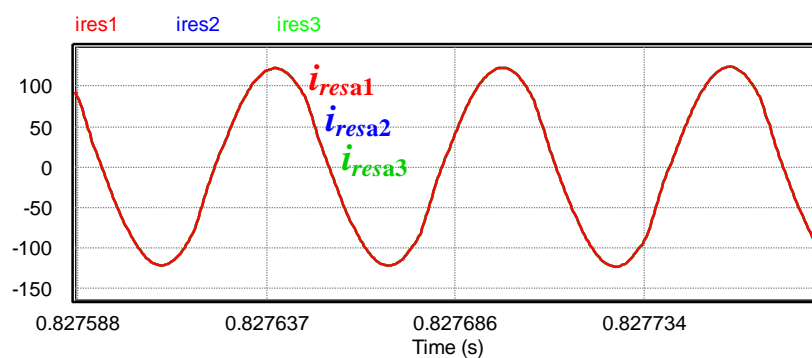


Figure 4.69– Balanced three-phase resonant currents in 1 MW simulation

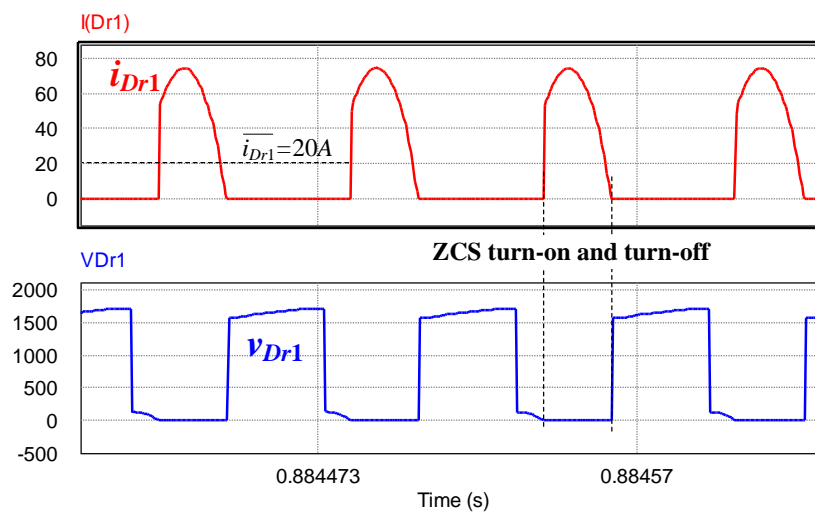


Figure 4.70–diode waveforms in high-frequency high-gain rectifier in 1 MW simulation

### 4.3 Chapter Summary

In this chapter a new class of modular ac-dc step-up soft-switched converter with unity turns-ratio high frequency transformers for medium voltage (MV) dc grid in wind energy systems was presented. To reduce the number of conversion stages in the proposed converter, the three-phase boost rectifier is integrated with high-frequency step-up resonant converter modules with high-gain rectifiers to form a single-stage ac-dc step-up converter. As a result, the proposed converter was able to achieve very high voltage gain without using any medium-to-high frequency transformers with very high turns-ratio, which greatly simplifies the insulation requirement and design of the high frequency transformer. In addition, soft-switching operations are achieved in all the semiconductor devices to maintain high efficiency.

Moreover, to reduce the number of semiconductors required for the front-end rectifier, a new, three-phase bridgeless ac-dc soft-switched, step-up resonant converter with high-gain rectifier modules for MV step-up conversion was presented in the second section of this chapter. The proposed converter was able to reduce the number of semiconductors required for the front-end rectifier.

## Chapter 5      Conclusions

Energy and environment are the two foremost areas of global crisis. The world's energy demand is ever-increasing, which is not only diminishing the reserve of fossil fuels, but also affecting the environment. It is more and more broadly recognized that developing renewable energy technologies can offer effective solutions to these enormous challenges. According to the International Energy Agency, about 14 % of the global population did not have access to electricity in 2017. Around 84% of those without access to electricity reside in rural areas where renewable energy systems can be the best possible option. Among all the renewable energy sources, wind energy is increasingly becoming mainstream and competitive with conventional sources of energy. It is expected that by 2030, about 20% of the global electric power will be supplied by wind energy [104]. Therefore, it is essential to investigate and develop the most effective grid integration structures and power converter technologies for wind power generation systems. Conventional MVac grid utilizes heavy and large-size step-up transformer for each wind turbine, which increases the installation cost and maintenance requirements, particularly in offshore and remote area applications. To address these problems, MVdc grid has been presented as an alternative and attractive option such that step-up dc-dc converters will be used to replace the low frequency step-up transformers. It can be inferred from the literature that the MVdc grid

is an emerging power structure for the wind energy systems located in distant offshore farms and remote areas. However, step-up power converters reported for MVdc systems face at least one of the following challenges: (1) the need for a medium frequency high power step-up transformer; (2) the need for high voltage switching transistors; (3) the need for two power conversion stages that reduce the overall power efficiency, and (4) the hard switching or restricted soft-switching condition. The motivation for this thesis stems from these challenges. The contributions of this thesis are summarized and are highlighted in the next section.

## 5.1 Contributions

The contributions of this thesis are summarized below:

1. A new class of modular high frequency dc-dc step-up converters has been developed that eliminates the need for high turns-ratio step-up transformers. In each of the presented dc-dc converter modules, the inverter side consists of multiple strings of switches, which has been shown to be able to reduce the voltage stress across each switch to half of the input voltage. The combination of resonant circuits and HGR modules is able to achieve high voltage gain without the use of a high turns-ratio transformer. Zero voltage switching (ZVS) turn-ON and close-to zero current switching (ZCS) turn-OFF for all semiconductor switches are achieved. In addition, the circulating energy in all the resonant circuits in each presented converter module is minimized through close-to-resonant operation for different load conditions, so that high efficiency is maintained.

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2. By magnetically integrating the HGR modules in the high frequency rectifying stage in the dc-dc converter, the number of required magnetic components is further reduced, compared to the individual module approach using separate magnetic components. The resultant current-driven structure of each HGR module guarantees smooth performance of the diodes with ZCS turn-ON and OFF. With this approach, it has been demonstrated that output dc voltage balancing of all the converter modules is achieved.
  3. To minimize the number of isolating magnetic components linking the resonant circuits and the HGR modules, a single magnetic core using multi-winding isolated transformer has been presented. Since the coupled voltage-quadrupler modules are connected to the resonant circuit via a 1:1:1 high frequency transformer, high turns-ratio transformers are not required in the proposed design. The detailed descriptions of the design of the multi-winding transformer for MV application have been provided.
  4. A new dc-dc converter module that fully utilizes all the inverter side switch networks at the input, consisting of three resonant sub-modules interconnecting with a unity turns-ratio multiphase transformer and coupled HGR modules has been presented. The operating principles and the detailed descriptions of this converter circuit have been provided. The design of the multiphase high frequency transformer used for MV application has also been discussed.
  5. A new class of modular three-phase ac-dc step-up soft-switched converter with unity turns-ratio high-frequency transformers for MVdc grid in wind energy systems has been presented. In the proposed converter, the three-phase boost rectifier was combined with step-up resonant circuits and HGR modules using the shared switch concept, resulting in

a three-phase ac-dc high voltage gain converter with integrated PFC. In this approach, a close to unity power factor is achieved in the three-phase ac-dc step-up voltage conversion without adding any extra semiconductor switches.

6. To reduce the number of the diodes required for the front-end rectifier in the devised three-phase ac-dc step-up converter, a new bridgeless single-phase ac-dc rectifier has been presented. This rectifier is then integrated with the previously presented step-up dc-dc converter modules to build various modular bridgeless ac-dc three-phase step-up converters for MV step-up conversion. The operating principles and the detailed descriptions of this ac-dc converter circuit have been provided.
7. In all the proposed dc-dc and ac-dc converter topologies, high-frequency unity turns-ratio transformers were utilized. This contribution is particularly crucial in high-power MV applications, where designing a medium-frequency transformer with a high turns-ratio has certain inherent limitations in terms of isolation and magnetic coupling effect.
8. The performance of all the dc-dc and three-phase ac-dc converter topologies presented in this thesis has been verified by simulation results based on actual MW wind turbine system parameters, as well as experimental results on laboratory-scale proof-of-concept prototypes. The design procedure of each converter topology presented in this thesis has also been described in details.

## 5.2 Future Works

With regards to the research conducted in this thesis, some future works related to this thesis are summarized below:

1. To develop a new active auxiliary circuit that allows the developed bridgeless ac-dc step-up converter to have extended soft-switching operation while at the same time, lower switch conduction loss can be achieved by utilizing larger boost PFC inductances. To achieve this, the active auxiliary circuit will have to allow the bridgeless boost rectifier to inherently change from DCM to CCM within one-half of the line cycle. By doing this, the boost inductors and EMI filter footprints can be reduced.
2. To utilize the devised multiphase high frequency transformer based dc-dc step-up converter module and combine it with the presented bridgeless rectifier to create a new three-phase ac-dc step-up converter module that will be capable of capturing more power from inverter side switches. With this approach, each bridgeless ac-dc converter in each phase will fully utilize all the switch networks at the dc-link for transferring power.
3. To continue experimentally validating the presented MPPT control scheme with output voltage regulation in the presented ac-dc step-up converters.

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## Appendix A Printed Circuit Board (PCB) Layouts

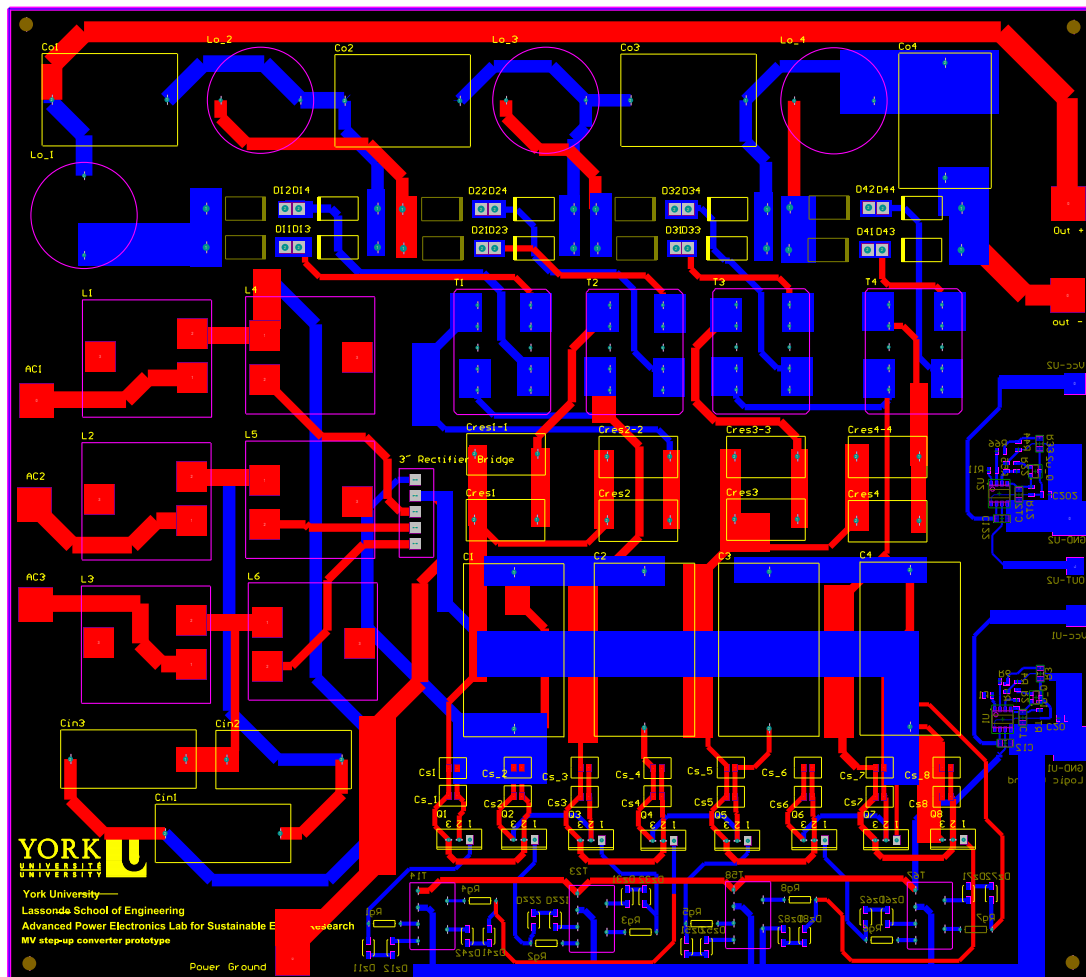


Fig. A.1 PCB layout of the proposed dc-dc converter with modular resonant circuits

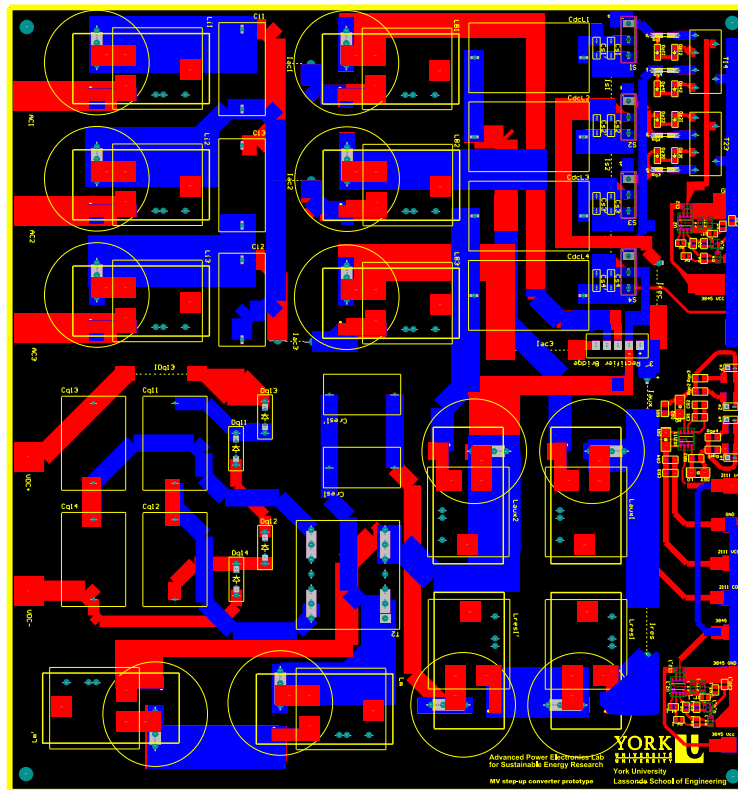


Fig. A.2 PCB layout of proposed ac-dc converter with high-gain rectifiers

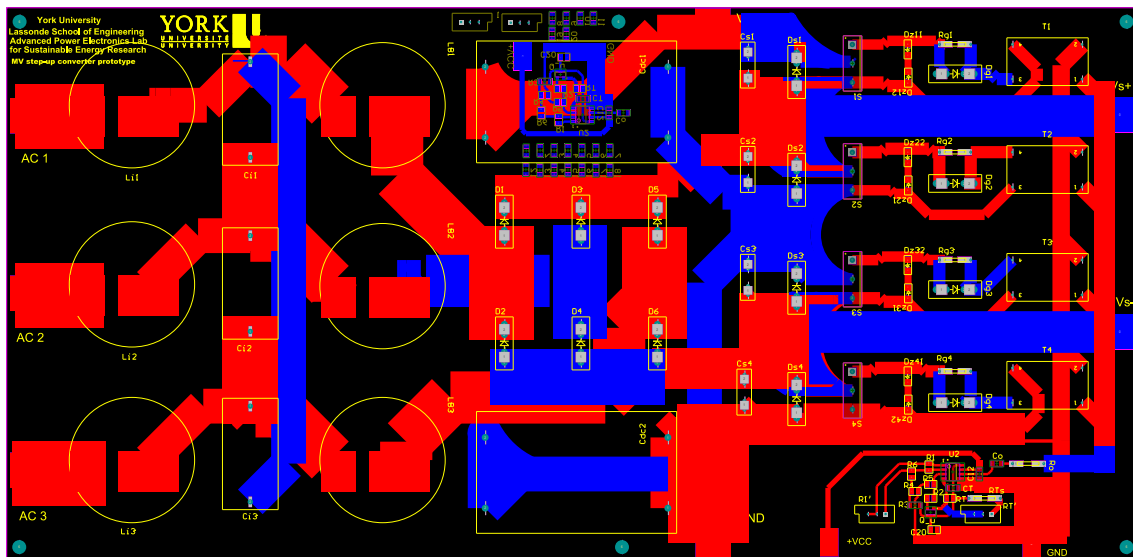


Fig. A.3 PCB layout of proposed power factor correction ac-dc converter

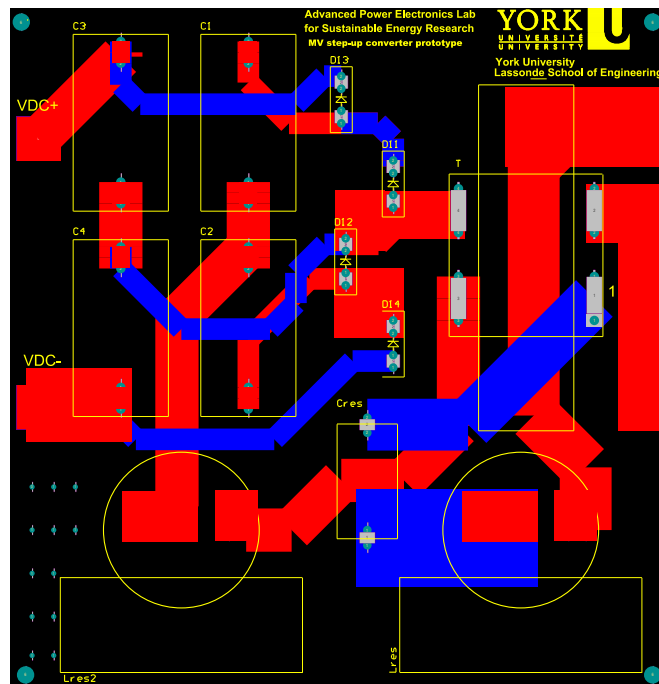


Fig. A.4 PCB layout of the high voltage rectifier (HGR)

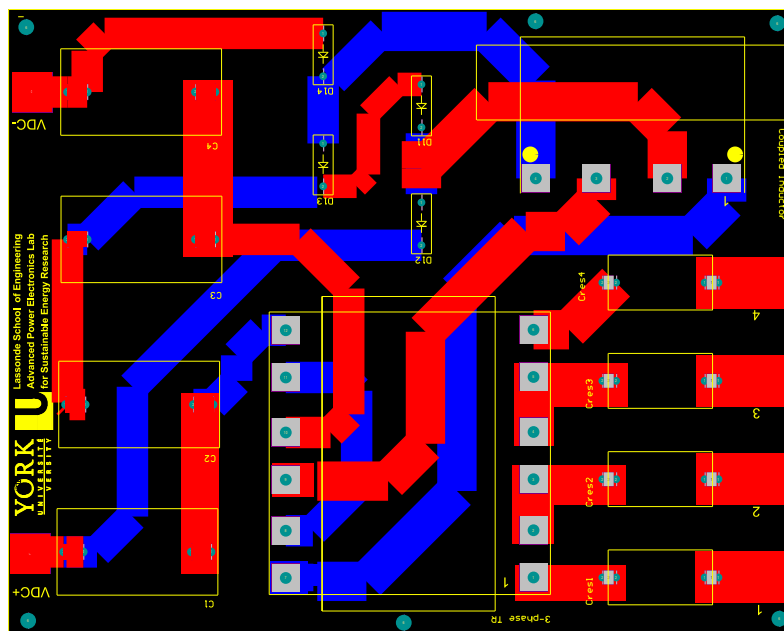


Fig. A.5 PCB layout of proposed dc-dc converter with a multiwinding transformer

## Appendix B MVdc Grid Protection for the Proposed Converter

Despite the numerous advantages of MVdc grid over MVac grid with respect to integration of renewable energy systems, mentioned in this thesis, designing and implementing an appropriate protection system for MVdc grid remains a challenging task. The challenges stem from the rapid rise of dc fault current (more than 100 times) that must be extinguished in the absence of current zero crossing [42].

The behaviour of the proposed converter under a dc fault in the MVdc grid was analysed through simulations in PSIM. The dc fault characteristics in the proposed converter consist of two stages: I) dc side capacitors discharge and II) freewheeling stage. This is shown in Fig. B.1 and the simulation results are also illustrated in Fig. B.2. Compared to a typical voltage source converter (VSC), the fault characteristics in the proposed converter does not include the third stage (i.e. grid-side current feeding) due to the series inductances in the transformer primary side.

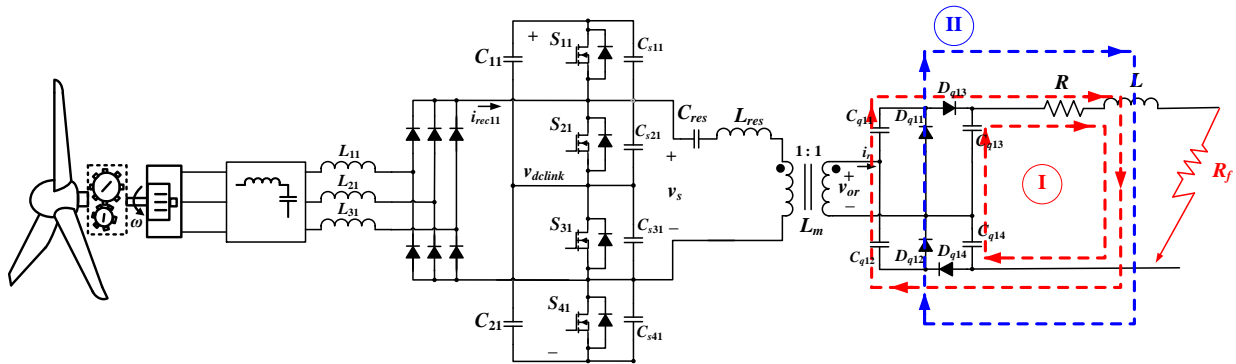


Fig. B.1 MVdc fault characteristics in the proposed converter

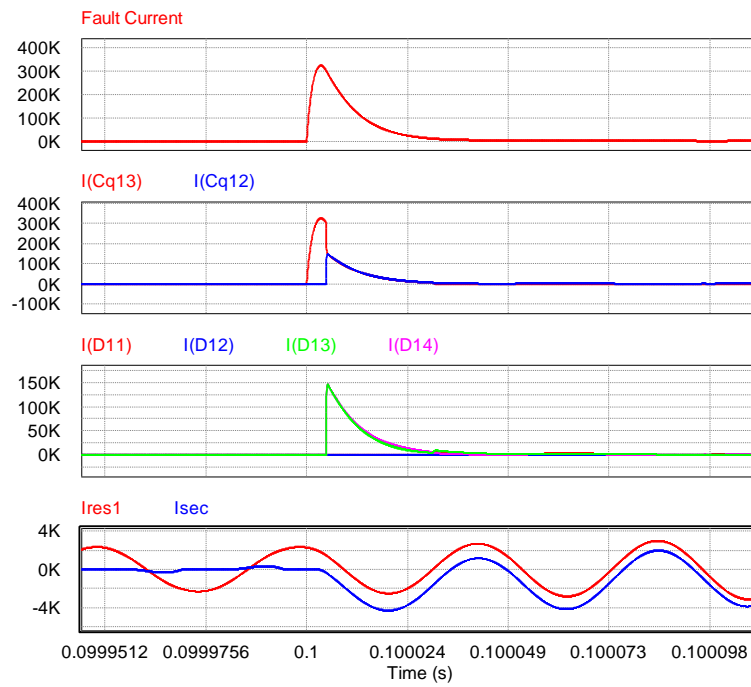


Fig. B.2 Simulation results of the proposed converter once a dc fault occurs in the MVdc grid

## Appendix C List of Publications

The following is a list of publications by the author during doctoral studies.

### C.1 Refereed Journal Papers

- [1] M. Abbasi and J. Lam, "A  $\sim 99\%$   $\eta$  Hybrid Resonant/Coupled ZCS-Voltage-Quadruplers MV SiC Converter Module for DC Grid in Wind Systems," *Submitted to IEEE Transactions on Industrial Electronics*.
- [2] M. Abbasi and J. Lam, "An SiC-Driven Modular Step-Up Converter With Soft-Switched Module Having 1:1 Turns Ratio Multiphase Transformer for Wind Systems," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7055-7066, Sept. 2019.
- [3] M. Abbasi and J. Lam, "A Modular SiC-Based Step-Up Converter With Soft-Switching-Assisted Networks and Internally Coupled High-Voltage-Gain Modules for Wind Energy System With a Medium-Voltage DC-Grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics: Special Issue on "Resonant and Soft-Switching Techniques with Wide Bandgap Devices"*, vol. 7, no. 2, pp. 798-810, June 2019.
- [4] M. Abbasi and J. Lam, "A Very High-Gain-Modular Three-Phase AC/DC Soft-Switched Converter Featuring High-Gain ZCS Output Rectifier Modules Without Using Step-Up Transformers for a DC Grid in Wind Systems," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3723-3736, July-Aug. 2018.

- [5] M. Abbasi and J. Lam, "A Step-Up Transformerless, ZV–ZCS High-Gain DC/DC Converter With Output Voltage Regulation Using Modular Step-Up Resonant Cells for DC Grid in Wind Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1102–1121, Sept. 2017.

## C.2 Refereed Conference Papers

- [1] M. Abbasi and J. Lam, "A Multimode Bridge-less SiC-Based AC/DC Step-up Converter with a Dual Active Auxiliary Circuit for Wind Energy Conversion Systems with MVDC Grid," *to appear in Proc. of the 2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019. (accepted in May 2019)
- [2] M. Abbasi and J. Lam, "A Balanced, Unity Power Factor, 3-phase Bridgeless AC/DC Step-up Transformer-less Converter with Magnetic-Coupled Soft-Switched Step-up Rectifiers for Wind Farm with a MVDC Grid," *in Proc. of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 1212–1219.
- [3] M. Abbasi and J. Lam, "A SiC-based, Fully Soft-Switched Bridge-less AC/DC Converter with High Voltage Conversion Ratio Based on Current Fed Voltage Quadrupler Modules for MVDC Conversion in Wind Energy Application," *in Proc. of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 5508–5514.
- [4] M. Abbasi and J. Lam, "A New Three-Phase Soft-Switched Bridgeless AC/DC Step-Up Converter with Current Fed Voltage Doubler Modules for DC Grid in Wind Systems," *in Proc. of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 44–51.

- [5] M. Abbasi and J. Lam, "An Improved Voltage Balancing Technique for a Soft-Switched High-Gain Converter with Low Voltage Stress Using Duty Ratio Control for Wind Energy Application," in *Proc. of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 4136–4143.
  
- [6] M. Abbasi and J. Lam, "A Modular Silicon Carbide (SiC)-Based Single-Stage Three-Phase AC/DC Step-Up Medium Voltage Converter with Extended Soft-Switching Operations for DC Grid in Wind Systems," in *Proc. of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 3005–3012.
  
- [7] M. Abbasi and J. Lam, "Dynamic Performance and Small-Signal Analysis of a DC-DC Step-Up Converter with High-Gain Output Rectifier for Offshore Wind Turbines," in *Proc. of the 2017 IEEE Electrical Power and Energy Conference (EPEC)*, 2017, pp. 1–6.
  
- [8] M. Abbasi and J. Lam, "A New Three-Phase AC/DC High Power Factor Soft-Switched Step-Up Converter with High Gain Rectifier Modules For Medium Voltage Grid in Wind Systems," in *Proc. of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.