Design Techniques of Highly Integrated Hybrid-Switched-Capacitor-Resonant Power Converters for LED Lighting Applications

Chengrui Le

Submitted in partial fulfillment of the
requirements for the degree
of Doctor of Philosophy
in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2020

ABSTRACT

Design Techniques of Highly Integrated Hybrid-Switched-Capacitor-Resonant Power Converters for LED Lighting Applications

Chengrui Le

The Light-emitting diodes (LEDs) are rapidly emerging as the dominant light source given their high luminous efficacy, long lift span, and thanks to the newly enacted efficiency standards in favor of the more environmentally-friendly LED technology. The LED lighting market is expected to reach USD 105.66 billion by 2025. As such, the lighting industry requires LED drivers, which essentially are power converters, with high efficiency, wide input/output range, low cost, small form factor, and great performance in power factor, and luminance flicker. These requirements raise new challenges beyond the traditional power converter topologies. On the other hand, the development and improvement of new device technologies such as printed thin-film capacitors and integrated high voltage/power devices opens up many new opportunities for mitigating such challenges using innovative circuit design techniques and solutions.

Almost all electric products needs certain power delivery, regulation or conversion circuits to meet the optimized operation conditions. Designing a high performance power converter is a real challenge given the market's increasing requirements on energy efficiency, size, cost, form factor, EMI performance, human health impact, and so on. The design of a LED driver system covers from high voltage AC/DC and DC/DC power converters, to high frequency low voltage digital controllers, to power factor correction (PFC) and EMI filtering techniques, and to safety solutions such as galvanic isolation. In this thesis, we study design challenges and present corresponding solutions to realize highly integrated and high performance LED drivers combining switched-capacitor and resonant converters, applying re-configurable multi-level circuit topology, utilizing sigma delta modulation, and exploring

capacitive galvanic isolation.

A hybrid switched-capacitor-resonant (HSCR) LED driver based on a stackable switched-capacitor (SC) converter IC rated for 15 to 20 W applications. Bulky transformers have been replaced with a SC ladder to perform high-efficiency voltage step-down conversion; an L-C resonant output network provides almost lossless current regulation and demonstrates the potential of capacitive galvanic isolation. The integrated SC modules can be stacked in the voltage domain to handle a large range of input voltage ranges that largely exceed the voltage limitation of the medium-voltage-rated 120 V silicon technology. The LED driver demonstrates $>$ 91% efficiency over a rectified input DC voltage range from 160 V_{DC} to 180 V_{DC} with two stacked ICs; using a stack of four ICs $>$ 89.6% efficiency is demonstrated over an input range from 320 V_{DC} to 360 V_{DC}. The LED driver can dim its output power to around 10% of the rated power while maintaining >70% efficiency with a PWM controlled clock gating circuit.

Next, the design of AC main rectifier and inverter front end with sigma delta modulation is described. The proposed circuits features a pair of sigma delta controlled multilevel converters. The first is a multilevel rectifier responsible for PFC and dimming. The second is a bidirectional multilevel inverter used to cancel AC power ripple from the DC bus. The system also contains an output stage that powers the LEDs with DC and provides for galvanic isolation. Its functional performance indicates that integrated multilevel converters are a viable topology for lighting and other similar applications.

Table of Contents

List of Figures

List of Tables

Acknowledgments

It was a long and challenging journey and luckily, with the accompany of many wise and warmhearted guides and fellows, I was able to sail to the end with extraordinary learning and growth. Before I continue on to my new stage of life, I would love to give my deepest thanks to the people that supported me through this endeavor.

Firstly I must thank my advisor Professor Peter Kinget for his guidance, help, and understanding though out my graduate study. His encourage and trust enabled me to overcome the most difficult times in my research. He is a great model to follow not only in academic but also in life. I also want to thank Professor Seth Sanders for all the inspiration, guidance, and discussion which are the key to the success of my research. I am also thankful to Professor Ioannis Kymissis, and Professor Stephen O'Brien for always being warm and supportive in my research.

A special thanks goes to my research partner Dr. Daniel Gerber, for all the days and nights we spent together to accomplish one milestone after another. It was a great time working with you and wish you a best future.

My research will not be possible without supports from Gianpaolo Lisi, Ali Djabbari, Raj Subramoniam, Glen Wells, Jianyi Wu, Zhenyong Zhang, and many fellows from Texas Instruments-silicon valley. It is a memorable and super happy time working with all of you in the beautiful campus of TI. May our friendship last forever.

Additional thanks goes to my colleagues in Columbia Integrated System Lab (CISL). Your advice and support are invaluable to my research and life in Columbia. I will always remember the pleasant time we spent together in the campus.

Finally I would like to thank my families for your unconditional love and trust. Without them I would have never been able to reach this far in my life. Deepest thank to all of you for your effort to support me.

To my lovely wife Bining
and our little angle Claire

To my beloved parents
Weihong and Yesheng

For their selfless love, trust, and support through my life

Chapter 1

Introduction

Power conversion is the process of converting electric energy from one form to another. The goal of modern electronic power converters is to provide highly efficient and reliable power processing with minimum component size and cost. Numerous power converter topologies have been developed for a wide range of applications and power levels. One emerging and important application of high efficiency power converters is in the solid-state lighting market.

Light-emitting diodes (LEDs) have been available for many years since the first LED is created by the Soviet inventor Oleg Losev in 1927 [1]. Although the light output per package and cost of the LEDs have been improved exponentially as described by Haitz's Law during the last few decades, it is not until recently that LEDs are finally on the verge of having the capability to radically alter the entire lighting landscape. The LEDs has shown great promise as an efficient, environmentally friendly, and affordable alternative to incandescent and fluorescent lights. Engineering-economic analysis suggests LED is more cost-effective due to its high luminous efficacy and long life span, which significantly saves electric energy and reduces replacement cost. As yellow/amber, green and finally blue colored LEDs became available, the applications of LEDs have exploded. Given their small form factors, LED bulb can be combined in many shapes to provide various lighting effects.

Since an LED is a current driven device whose light emission intensity is proportional to its forward conduction current, LED drivers are necessary to provide current regulation under different input and load conditions. The core of a LED driver is the power con-

verter, which is expected to have characteristics such as high conversion efficiency, wide input/output adaption range, low component cost, wide dimming range, low electromagnetic interference (EMI), and enough safety protection. Chapter 1.1 will provide a brief introduction of the fundamentals of light, human vision, flicker, and lighting history. Chapter 1.2 will cover the basics of LED devices. Chapter 1.3 will discuss the performance requirements of modern LED drivers for general lighting applications. A few widely used power converter topologies for LED driver will be introduced with their advantages and disadvantages analyzed. Chapter 1.4 will discuss the challenges in the integration of power converters. Chapter 1.5 will introduce the organization of the whole thesis.

1.1 Fundamental of Lighting

1.1.1 Light Basics

As we know, light is electromagnetic radiation within a certain portion of the spectrum, which has both wave and particle nature, which is known as the wave-particle duality. In propagation, light act as waves. However, the energy transmitted by the wave can be absorbed as a particle, which is called a photon, at a single location. The word photon is used to represent the quanta of light. The absorption of light can be viewed as an instant collapse of the light-wave energy to a single location, which is called the wave function collapse. The energy of a photon can be related to the wavelength of light as:

$$E = hf = \frac{hc}{\lambda}, \tag{1.1}$$

where E is the energy in joules, h is Planck's constant, f is the frequency of light in Hz, c is the speed of light, and λ is the wavelength of light in meters.

The main characteristics of light includes intensity, propagation direction, and frequency spectrum. The visible light is usually defined as having wavelength in the range of 400 to 700 nanometers, which corresponds with the frequency range of roughly 430 to 750 terahertz. Like other forms of waves, light exhibits properties such as polarization, superposition, reflection, refraction, diffraction, and interference. The speed of light in vacuum is constant, which approximately equals to 2.998×10^8.

1.1.2 Human Vision

The lighting technology serves human vision. The human vision characteristics determine the requirements of lighting. The human vision system is part of the central nervous system that enables people to interpret the surrounding environment using light in the visible spectrum. Specific wavelengths of light within the spectrum correspond to particular colors based on human perception of light. The long-wavelength side of the spectrum is perceived by human to be red, whereas the short-wavelength end pertains to violet light. Bounded between these two ends, lyes other colors, e.g. orange, yellow, green, and blue. The human vision is not only referring to the light reception process in which human eyes receive light and transform it into electrical neuron signals, but also a series of complex visual processing tasks such as the identification of objects and distance assessment. It all starts from the cornea, pupil, and lens of eye refracting light into a small area and project it onto the retina at the back of the eye ball. The photoreceptor cells, which are called rods and cones, on the retina then transduces the signal into electrical neural impulse. The rods, which concentrated at the outer edges of the retina, functions in lower light intensity conditions and peripheral vision, known as scotopic vision. Being more sensitive to luminance, the rods are the key of night vision, while having little contribution to color vision. The cones (photopic vision), to the contrary, function best in bright light and has different response to light of different frequency, thus is responsible for color vision. The cones contain one of the three types of pigments and are accordingly designated as L-type or long-wavelength cones, M-type or middle-wavelength cones, and S-type or short-wavelength cones. Therefore, they are able to distinguish among the different colors.

The science of the measurement of light, in terms of its perceived brightness to the human eye, is called Photometry. It is different from the measurement of absolute radiation energy, because human eye is not equally sensitive to all wavelengths of visible light. Photometry calculates the perceived light by weighing the measured energy of each wavelength with a factor representing the human-eye sensitivity at that wavelength. The factor is called the luminosity function. The relevant quantity is designated as luminous energy. There are several other measurements and units that are widely used in photometry. The luminous flux with unit lumen is luminous energy per unit time. The luminous intensity with unit

candela (cd) is the luminous flux per unit solid angle. The luminance with unit cd/m^2 or nit is luminous flux per unit solid angle per unit projected source area.

1.1.3 Luminance Flicker

Luminance flicker is a rapid and repeated change over time in the brightness of light. The cause of luminance flicker includes light source fluctuations, power supply ripples, or pulse width density modulation (PWM) of light source driver. Various studies have assessed the potential health, performance and safety-related impacts of temporal light flicker [2], [3], [4]. Studies show that flicker at certain frequencies may induce biological human response thus LED lamp driver designers needs to find mitigations. Adverse effects of flicker include annoyance, reduced task performance, visual fatigue, headache and epileptic attack by photosensitive persons. The luminance flicker that is consciously perceivable by a human viewer is called visible flicker, while invisible flicker cannot be consciously perceived by a human viewer.

Human visual sensitivity to variation of luminance over time is defined by the temporal contrast sensitivity function (TCSF). This function describes visual sensitivity as a function of temporal frequency of luminance modulation [5]. The TCSF falls rapidly at high temporal frequencies, reaching a minimum of 1 at the Critical Fusion Frequency (CFF). The CFF of flicker is defined as the frequency at which an intermittent light stimulus appears to be completely steady to the average human observer and is related to persistence of vision. The TCSF as a function of flicker frequency spectrum is affected by the following parameters:

1. The average luminance intensity;
2. The position and area on the retina where the stimulation occurs;
3. The wavelength of stimulus light;
4. The degree of light or dark adaptation;
5. Physiology conditions such as age and fatigue;
6. Person to person variation.

To estimate the flicker intensity observed by human eye, we can calculate the frequency spectrum of the received luminance at every spacial location on human retina, and multiply with the TCSF with corresponding parameters, then integrate the resulted spectrum energy.

The resulted spacial flicker intensity across the retina can then be weighted and summed together based on the retina spacial sensitivity of flicker. If the resulted overall flicker intensity is below certain threshold, the person cannot observe flicker.

It is reported visible flicker at frequencies within the range 3- 70Hz could cause risks of seizures. In addition, a few studies suggests invisible flicker at frequencies below 165Hz could have possible human biological effects including headaches and eye-strain [2]. Thus artificial light source designers needs to be aware and reduce luminance flickering in the frequency ranges of interest.

1.1.4 History of Artificial Lighting

Besides natural light source such as sunlight and moonlight, primitive human craved for artificial light source to stay away from darkness. Through out the history of human, several sources of light have been developed as the technology advances. The earliest artificial light starts from the control of fire, discovered approximately 5×10^5 years ago such as campfires and torches. The next break-through came about 3×10^4 to 7×10^4 years ago when people started burning a fiber immersed in molten fat. Later many different kinds of oil were used for this purpose including oil produced from plants, animals (e.g. whale oil), and mineral. A major reduction in the cost of lighting occurred after Abraham Gesner, a Canadian geologist, first refined kerosene in the 1840s. Then came the discovery of crude oil in 1859, and the petroleum industry arose. Around the 1880s another major drop of cost of lighting came with the introduction of electrical lighting in the form of arc lights for large space and street lighting followed by incandescent light bulb for general purpose lighting.

In particular, the first solid-state light device was invented by T. Drummond in 1826 [6]. The device was not electrical and consisted of a calcium oxide cylinder with an oxyhydrogen blowpipe producing a bright flame. This brilliant limelight was used in the theaters. The first practical electrical lighting device was demonstrated in 1876 by a Russian telegraph engineer. It is consisted of two Carbon rods separated by a thin layer of gypsum plaster and was called Jablochkoff's candle as shown in Fig. 1.1. It is the pioneer of modern electrical arc lamp aroused public interest. Later a series of inventors, including Thomas Alve Edison, an American researcher and businessman, and Joseph Wilson Swan, a British

chemist, electrical engineer, and inventor, improved and commercialized the incandescent filament lamp in 1879 [7]. Incandescent bulb works by heating a wire filament to a high temperature such that it glows visible light. The filament is protected from oxidation with a bulb that is filled with inert gas or a vacuum. It was an important milestone of lighting technology enabling humanity to produce long lasting light with extreme low cost. The subsequent lighting devices are vapor lamps. The first mercury vapor lamp to achieve widespread success was invented in 1901 by American engineer Peter Cooper Hewitt. It is a gas discharge lamp that uses an electric arc through vaporized mercury to produce light. The fluorescent lamp is a low-pressure mercury-vapor gas-discharge lamp that uses fluorescence to produce visible light. The mercury vapor lamp and fluorescent lamp converts electrical energy into useful light much more efficiently than incandescent lamps. The typical luminous efficacy of fluorescent lighting system is 50-100 lumens per watt, several times the efficacy of incandescent bulbs with comparable light output. The other advantages are their long life time in the range of 24,00 hours and a high intensity, clear white light output.

A technology revolution of lighting has taken place since the discovery of LED. It has many advantages over incandescent light sources, including lower energy consumption, longer lifetime, improved physical robustness, smaller size, and faster switching. The electro-luminescence phenomenon was discovered in 1907 by the British experimenter H. J. Round of Marconi Labs, and Russian inventor Oleg Losev reported creation of the first LED in 1927. The first visible-spectrum (red) LED was developed in 1962 by Nick Holonyak, Jr. while working at General Electric. The first high-brightness blue LED was demonstrated by Shuji Nakamura of Nichia Corporation in 1994. Table 1.1 shows a brief glance of the history of artificial lighting.

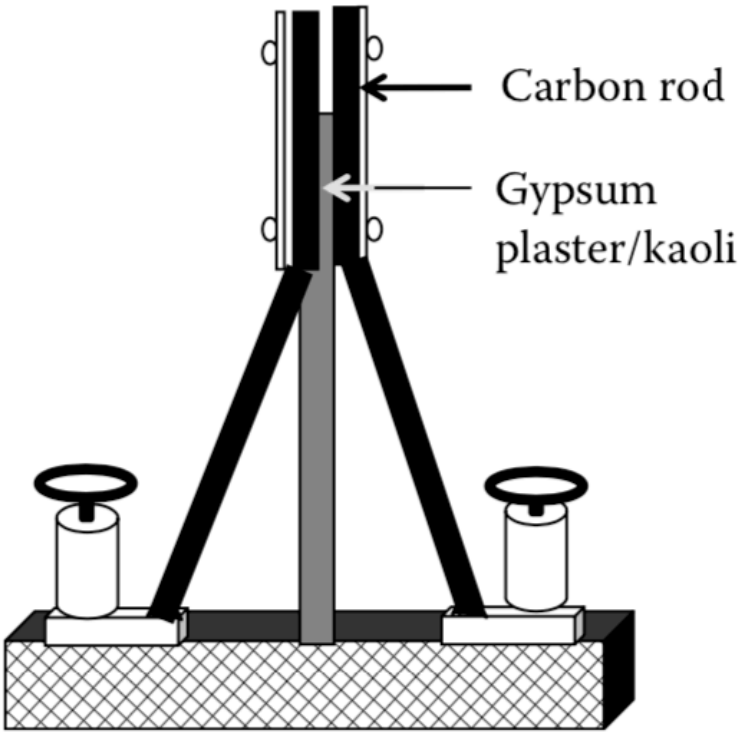


Figure 1.1: Jablochkoff candle.

No.	Event	Year
1.	Fire torch	5×10^5 years ago
2.	Wick lamp	$3 \times 10^4 - 3 \times 10^4$ years ago
3.	Oil pottery lamp	600 BC
4.	Oil reservoir lamp	500 BC
5.	Beeswax candle	400 BC
6.	Gas lighting	1772 AD
7.	Argand oil lamp	1784 AD
8.	First solid-state lighting device (limelight)	1826 AD
9.	First solid-state lighting device (Jablochkoff's candle)	1876 AD
10.	Incandescent filament lamp	1879 AD
11.	Mercury vapor lamp	1901 AD
12.	Low-pressure sodium vapor lamp	1919 AD
13.	Fluorescent tube	1927 AD
14.	First WLED	1994 AD

Table 1.1: Glance at the history of artificial lighting.

1.2 LED-Based Lighting

1.2.1 Characteristics of LEDs

As depicted in Fig. 1.2, an LED is a two-lead semiconductor light source made from a P-N junction diode. The PN junctions are created by doping impurities e.g. indium, gallium and nitrogen to silicon carbide. Once a forward voltage is applied across the LED, electrons jump to the conduction band, resulting in a forward current flow. When an electron loses energy and falls back to the valence band, energy is released in the form of a photon. The wavelength of the light emitted, and thus its color, depends on the band gap energy of the material forming the p-n junction. The materials used for the LED have a direct band gap with energies corresponding to near-infrared, visible, or near-ultraviolet light. LED development began with infrared and red devices made with gallium arsenide. Advances in materials science have enabled making devices with shorter wavelengths, emitting light in a variety of colors.

The typical I-V characteristic curves versus different colors of LED devices are depicted in Fig. 1.3. Once the forward bias voltage (V_F) of a LED passes the turn-on threshold, its forward current (I_F) increases almost exponentially, then the slope of the I-V curve gradually reduces and eventually the curve becomes linear. This linear region can be modeled by the equivalent series resistance (ESR), which dominates when the forward current is large. Since the ESR is typically designed to be as small as possible to improve power efficiency, a small change in voltage across the LED results in a large variation in the current. In other words, an LED can often be thought of as a constant voltage load. The exact forward voltage drop depends on the exact LED material, manufacturer process, color, aging condition, and environment impacts such as temperature.

LED's efficacy decreases as the driving current increases. This was initially thought to be related to temperature increase but proved to be wrong by later studies. The elevated temperature actually improves LED's efficacy. The true cause of efficiency droop of LED was identified in 2007 as Auger recombination [8]. However, higher temperature can shorten LED's lifetime, by causing light reduction and accelerated chip degradation such as defects. High-brightness LEDs often operate at 350 mA, which is a compromise between light output,

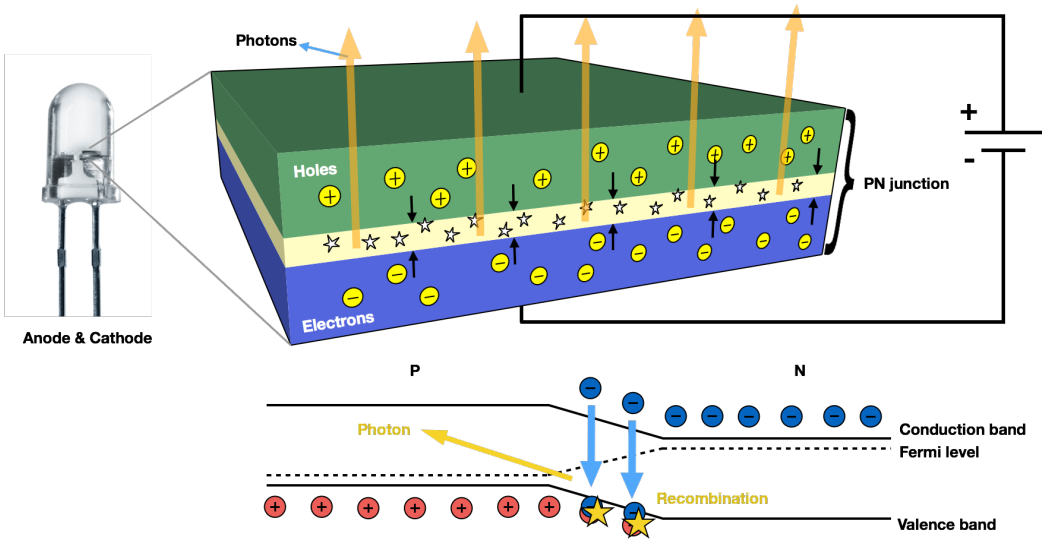


Figure 1.2: LED device structure and operation physics.

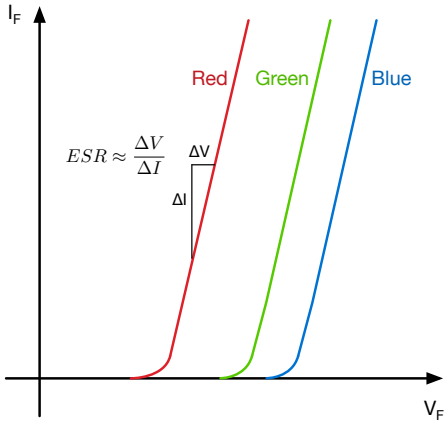


Figure 1.3: Example I-V curves of red, green, and blue LED devices.

efficiency, and longevity.

Given the thermal impact on LED's efficiency and lifespan, the heat dissipation performance of LED light bulbs are crucial for many applications. One efficient way to dissipate heat is by attaching a heat sink with large surface area. In the case of household lighting, the good news is that the LED light bulb is often designed to have the same size of the traditional incandescent bulb, ,thus making large heat sink a practical and economical solution. Advanced LED drivers should be able to compensate for the temperature impacts to LED luminance. Such function would require a temperature sensor, larger tuning capability of the LED driver and a digital compensation loop.

1.2.2 Application of LEDs in Lighting

The commercial use of LEDs started in the late 1960s. The early LEDs were first used as colored indicator lights in electronic devices. Starting with the introduction of the first transparent-substrate AlGaAs LEDs in the 1980s, hight-luminance LEDs are moving into all applications related to artificial lighting. LED lamps have a lifespan many times longer than equivalent incandescent lamps and significantly more than most fluorescent lamps. The most efficient available LED lamps have efficiencies of 200 lumens per watt [9]. The LED lamp market is projected to grow by more than 12% from $2 billion in 2014 to $25 billion in 2023.

Table 1.2 and 1.3 summarizes the pros and cons of LED lighting vs. the traditional methods.

	Advantages	
1.	Efficiency	LED has higher efficacy than incandescent/florescent lights. The efficiency of LED lighting fixtures are not affected by shape or size.
2.	Lifetime	One report estimates 35,000 to 50,000 hours of useful life, though time to complete failure may be shorter or longer [10]. Fluorescent tubes typically are rated at about 10,000 to 25,000 hours
3.	Size	LEDs can be very small, including mini and micro LEDs for display, and are easily attached to printed circuit boards.
4.	Response time	LEDs can have microseconds of response time and are ideal for high-frequency on-off cycling.
5.	Color	LEDs can emit light with intended color without color filters as traditional lighting methods need. It is more efficient.
6.	Dimming	LEDs are ideal for PWM dimming or lowering the forward current.
7.	Durability	Being solid-state device, LEDs are very durable physically compared with fragile incandescent or fluorescent bulbs.
8.	Directional light	The LED lighting is directional which are preferable for certain applications.

Table 1.2: Advantages of LED lighting.

	Disadvantages	
1.	Temperature dependence	LED performance highly depends on the temperature of the operation environment and thermal management properties.
2.	LED driver complexity	LEDs are very sensitive to driving voltage. Current and lifetime change greatly with a small voltage delta. Thus LED drivers require current regulation and temperature compensation.
3.	Color rendition	Most cool-white LED have spectra that differ significantly from a black body radiator. This can make object color look differently under LED illumination.
4.	Area light source	Single LED doesn't approximate a point source of light giving a spherical light distribution, but rather a lambertian distribution. Thus LEDs need optic lenses or fixtures to provide spherical light field.

Table 1.3: Disadvantages of LED lighting.

1.3 Introduction of LED Driver

1.3.1 The Fundamentals of LED Drivers

The concept of LED driver comes from the need to regulate the current through LEDs to achieve high efficiency operation and deliver the right amount of light. The architecture of an LED driver is determined by the characteristics of input power source, output load, available passive and active components, and application-specific requirements.

The LED driver is essentially a power converter. Today, the domestic mains electric power is delivered by an alternative AC voltage source with 50 Hz to 60 Hz frequency. Thus off-line LED drivers needs to convert electric power from a AC voltage source to a DC current through the LEDs. a typical off-line LED driver is required to have both rectification and voltage conversion function with good power efficiency.

The basic LED performance requirements are summarized and listed below.

1.3.1.1 Current Regulation

One of the basic functions of the LED drivers is current regulation. This maintains a desired LED current flow given input voltage and current fluctuation, temperature change, or component performance shift over time. As mentioned in Section 1.2.1, LED luminance is almost proportional to the current passing through and behaves similar to a constant voltage load. Thus by nature, current regulation is advantageous in LED light control over voltage regulation. Applications like LED dimming and color control of LED bulbs [11] as shown in Fig. 1.4 also requires accurate current control with LED drivers.

1.3.1.2 Power Efficiency

The U.S. Energy Information Administration (EIA) estimates that in 2018, the U.S. residential sector and the commercial sector used about 232 billion kilowatthours (kWh) of electricity for lighting, which was 6% of total U.S. electricity consumption. One percent of lighting power efficiency improvement means billions of kWh of electricity energy saving. As LED light market is growing rapidly, the power efficiency of LED drivers become more and more critical. In practice, the power efficiency often needs to be traded-off with other

Figure 1.4: Example of commercial LED light bulb with smart color control.

design considerations such as component size, cost, and input/output conditions. LED driver circuit topology, design technique, and component performance are crucial in terms of efficiency optimization.

1.3.1.3 Input and Output Range

For off-line LED drivers, the input voltage and frequency varies among different regions of the world. A voltage of (nominally) 230 V and a frequency of 50 Hz is used by most of the world population, including people in Europe, most of Africa, most of Asia, much of South America and Australia. In North America, the most common combination is 120 V and a frequency of 60 Hz. Other voltages exist, and some countries may have, for example, 230 V but 60 Hz. A wide input voltage and frequency range design can benefit LED driver providers to lower design and manufacture cost by covering more regions with the same product.

The output load specifications could also have large variation due to the various LED applications. If LEDs are connected in series the output voltage and power of LED driver is proportional to the number of LED in a string. LED dimming and color control also require output power to be controllable. It is desirable to maintain high power efficiency

and low cost across wide input and output configurations of LED driver. However, it is very challenging to meet this requirement with fixed circuit design parameters and components. Thus re-configurable LED driver could be an optimized solution.

1.3.1.4 Power Factor Correction

For the AC main power distribution system, the power factor, which is the ratio of the real power absorbed by the load to the apparent power flowing in the power rails, is required to be above certain levels e.g. 0.9 to improve energy efficiency and reduce power generation and transmittance cost. For example if the load power factor were 0.7, the apparent power would be 1.4 times the real power used by the load. Thus power-factor correction (PFC) technique, which increases the power factor of a load by adding passive or active network of capacitors or inductors, has been widely applied in power substations, distribution networks, and power-consuming devices. The PFC feature is also required for modern LED drivers in the world's main lighting markets.

1.3.1.5 Flicker

The LED luminance flicker performance is another important design specification of LED drivers. Flicker is defined as variations of luminance in time [12]. Previous reports suggest both visible and invisible flicker have potential adverse biological effects on human health [13]. Thus it is critical for LED driver designers to consider the light modulation scheme. However, it is very challenging for an electrical light source to maintain constant luminance, given the power main source is typically AC (i.e., 60Hz AC in North America). Thus special power main harmonic energy reduction technique needs to be applied for LED drivers. The human sensitivity to flicker, reported health impact, and driver voltage ripple cancellation circuits will be discussed in more details in Part 3.

1.3.1.6 Safety

Beyond normal electrical safety requirements, some LED drivers provides galvanic isolation between the high voltage AC input and the low voltage DC output to the LED string. Galvanic isolation prevents direct conduction path between functional sections of electrical

systems thus protects the users from electric shock by accidents. The isolation also prevents any disturbance on the primary side of the driver circuit from passing onto the output side. Thus the LEDs are protected against transients and surges occurring on the primary side.

Various electrical safety standards also specify the isolation requirements on the touch current and protective conductor current. Touch current is the current that flows when a human body touches the equipment. Protective conductor current is the current appearing in a protective conductor, such as leakage current or electric current resulting from an insulation fault.

1.3.2 Types of LED Drivers

There are many circuits that can provide a relative constant current through the LEDs and thus serves as a LED driver. However, in order to meet the performance requirements and standards discussed in Section 1.3.1, the LED driver circuits needs to be carefully designed and optimized. A few widely used design of LED drivers are introduced below:

1.3.2.1 Linear LED Driver

One of the simplest ways to drive LEDs is through a linear LED driver. It is preferred for a few reasons. One of them is its simplicity which leads to a lower cost for manufacturers. Another important engineer concern is the obscene of electromagnetic interference (EMI). The EMI specifications could require extra shielding or filtering which adds to the cost. However, the disadvantages are also obvious. The linear power converters usually have lower power efficiency which become worse with a wide output range. For off-line LED drivers, the efficiency would be extremely low for linear regulators since the mains voltage is high and with 50Hz to 60Hz ripple. In addition, the introduced thermal issue by low efficiency could lead to bulkier heat dissipation solution which is problematic for certain applications. Fig. 1.5 shows a linear voltage regulator and a constant current regulator using Op-Amps.

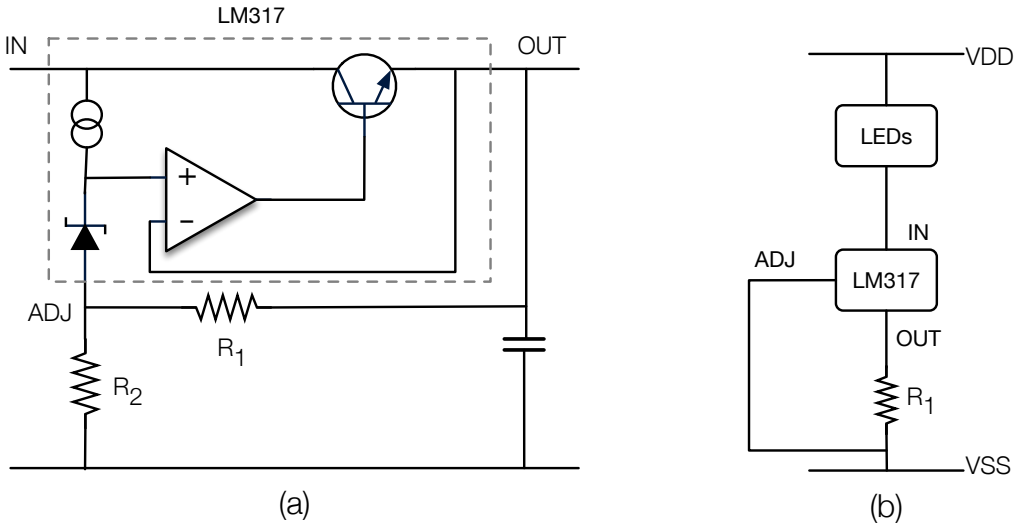


Figure 1.5: Example of (a) linear voltage regulator using an Op-Amp (LM317) and (b) linear current regulator as LED driver.

1.3.2.2 Switched-Mode LED Driver

A switched-mode LED driver incorporates a switching regulator to convert electric power efficiently and driver LEDs. The two key ideas of the switched-mode regulator are switching and filtering. The switching operation is important so that the across a wide input/output range the regulator circuit only operates at high-efficiency full-on and full-off states while reducing the time of the transitions between the two states when power efficiency is low. If the transition time is reduced to zero then ideally the switched-mode power regulator consumes no power. However, the switching operation generates electromagnetic signal at the switching frequency and thus power filters, usually low-pass filters, are required for most applications to filter out the EMI signals. Usually only passive filters are applied to power converters, since passive filters scale better to large signals and consume little power. For low-pass passive filter, the higher the switching frequency, the smaller and lighter the reactive components and thus the less cost and space is required. In addition, increasing operating frequencies improves the dynamic characteristics of converters. The bandwidth of a control loop is often determined by the characteristics of the output filter. Thus high operating frequencies can allow converters to achieve faster dynamic response, for example,

to rapid changes in the load current and/or the input voltage. In LED driver design, such benefits from higher switching frequency need to be traded-off with the increased switching power and device bandwidth limit. Another important factor that designers need to take into consideration is the device power rating limits. A lot of time the designer needs to trade-off other device performance to withstand the required power ratings.

1.3.2.3 Inductor Based LED Driver

Inductor based switched-mode LED drivers are widely applied in the lighting industry. The most common switched-mode regulators topologies include buck, boost, buck-boost, and flyback converters. Fig. 1.6 shows the basic schematics of the buck, boost and buck-boost power converters. They all utilize single inductor as energy storage elements. Take the boost converter as an example, the inductor stores energy by transforming electric potential energy into magnetic potential energy when the power switch is turned on and is then used to supply current by transforming magnetic potential energy into magnetic energy when the power switch is off. The power diode guarantees that the power flow is single direction and will not bounce between the source and load causing extra energy loss.

The buck, boost, and buck–boost topologies are all strongly related. Input, output and ground are connected through three loops. Two of the three passes through an inductor , while the other one passes through only switches. One of the two switches must be active such as a transistor, while the other one can be a diode.

The flyback converter is shown in Fig. 1.7, which is essentially a buck-boost converter with the inductor split to form a transformer, providing the advantage of galvanic isolation. The operation principle of the flyback converter is very similar to the buck-boost converter, with the difference that the magnetic energy is now stored in the transformer. Another advantage of transformer based power converter is that the converter can easily supply multiple outputs by making small circuitry modifications. The drawback of transformers is their large size.

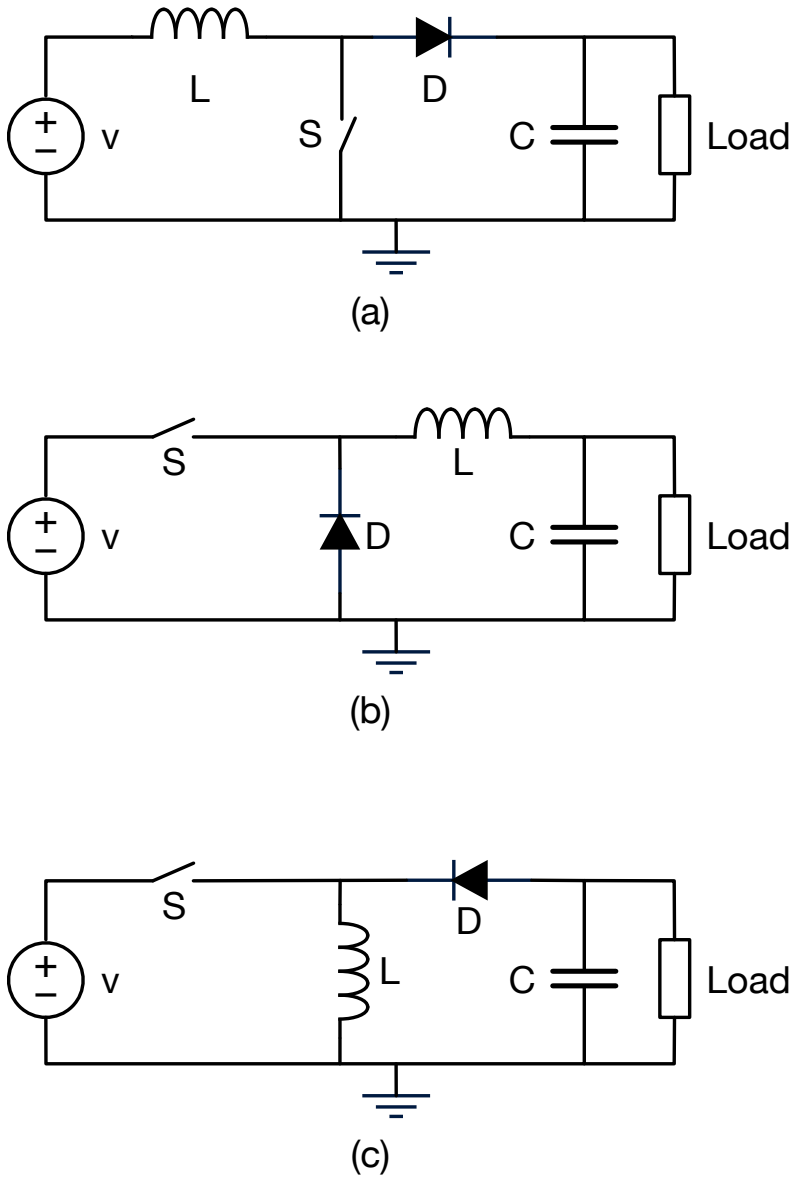


Figure 1.6: Basic schematics of (a) a boost converter, (b) a buck converter, and (c) a buck-boost converter.

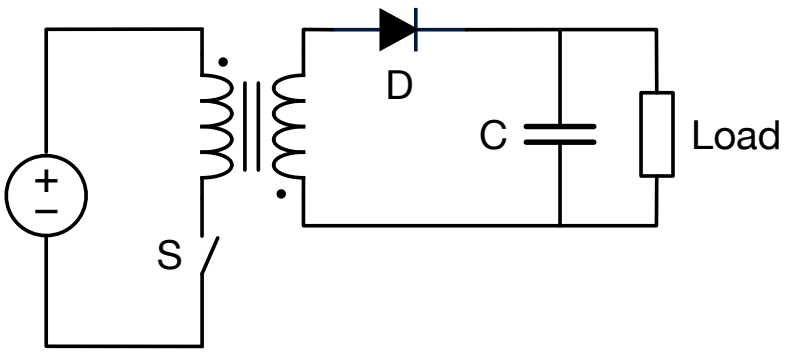


Figure 1.7: Basic schematic of a flyback converter.

1.3.2.4 Switched-Capacitor Power Converter

Switched-capacitor (SC) circuits utilizing capacitors and switches to transfer charge and regulate voltage or current. The SC converters can achieve high power efficiency (>90%) and are more friendly to integration compared with inductor or transformer based power converters.

One of the intrinsic advantage of SC converts is that existing capacitors have significantly higher energy density than inductors [14]. The energy density of surface mounted capacitors can easily achieve 1000 times of the shielded inductors. This can lead to significant Printed Circuit Board (PCB) area and cost reduction in electrical products.

The second intrinsic advantage of SC converter is that the voltage rating of the passive and active circuit components can be significantly reduced to only a small portion of the overall voltage rating of the converter. Fig. 1.8 shows a simple voltage doubler based on switched capacitor topology. There are 5 circuit elements in this schematic, and a non-overlapping clock signal controls the two switches. One can analyze and find that the voltage rating of all 5 elements are all below $\frac{V_{OUT}}{2}$,in which V_{OUT} is the overall voltage rating of the converter. By relaxing the voltage rating requirements, the other characteristics of the components can be significantly improved, such as size, cost, energy density, frequency bandwidth, and non-ideal parasitics. The end result of such improvements on overall converter performance can be dramatic. The lowered voltage ratings of electronic components also makes integration solution more viable.

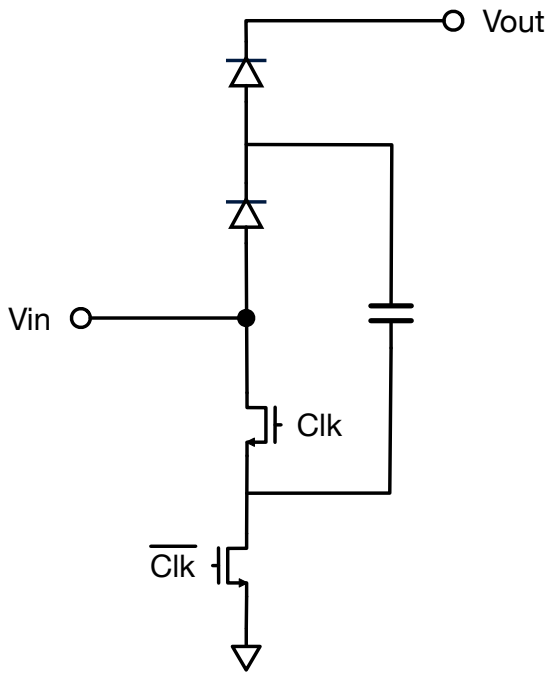


Figure 1.8: Basic schematic of a voltage doubler.

One limitation of traditional SC converters is that the voltage conversion ratio needs to be integer number, fractionally multiply or scale voltages (such as 3/2, 4/3, 2/3, etc.) when highest efficiency can be achieved. Otherwise the efficiency drops linearly like linear regulator. In certain topologies other voltage ratios can be generated by alternating between modes frequently, at the cost of topology and control complexity, which also impacts the robustness and cost of products.

1.3.2.5 Resonant Converter based LED Driver

As described above, switched mode power converters or LED drivers are widely used in various applications. However, the rectangular voltage and current waveforms cause turn-on and turn-off energy loss from circuit parasitics which limits the operating frequency and thus its benefits to the converter designs. For example, the reactive component size cannot be further reduced with limited switching frequencies. The rectangular voltage and current waveforms also generate broad-band electromagnetic energy and can pose a higher risk to the EMI issues. In order to allow converters to operate at higher frequencies, topologies that

shape either a sinusoidal current or voltage waveform have been developed by engineers to reduce switching losses. The fundamental idea of resonant converters is to utilize a resonant tank with sufficiently high quality factor to store and transfer charge. A common method to achieve loss and EMI reduction in resonant converters is the soft-switching technique, which means operating the switches or diodes under zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions. The resonant LED driver consists of a high-frequency resonant DC-AC inverter and a high-frequency rectifier. The low frequency or DC input power is first converted into high frequency AC power by the inverter, then converted back to DC output power by the rectifier. Galvanic isolation can be achieved in the AC phase by inserting isolation transformers or capacitors.

1.4 Integration of Power Converters

The global Power Management IC market is expected reach 38.4 billion US dollars by the year 2023, reflecting a coefficient of annual growth rate (CAGR) of 8.8% during the forecast period (2018-2023). Integration in power systems plays an essential role in achieving higher power efficiency, reducing product size and cost, improving reliability and EMI performance, as well as realizing various innovative features to meet the customer's need. Power ICs are widely used in applications such as switch-mode power supplies, electric motors, displays, lighting and telecommunication.

The most common power ICs are known as bipolar CMOS DMOS (BCDs), which combines the strengths of three different process technologies in a single IC: Bipolar for precise analog functions, Complementary Metal Oxide Semiconductor (CMOS) for digital design and Double Diffused Metal Oxide Semiconductor (DMOS) for high power and high-voltage devices. BCD technology can employ vertical and/or lateral power devices. The lateral BCDs have laterally-DMOS (LDMOS) devices or insulated gate bipolar transistor (LIGBT) as the power device, whereas the vertical BCDs are based on quasi-vertical DMOSs or IGBTs.

Other than BCDs, other technologies such as trench and silicon on insulator (SOI) also play increasingly more significant roles in power ICs [15]. The use of SOI technology

allows a higher device density and better vertical and lateral isolation. It can suppress the latch-up, offers considerably reduced cross-talk, decrease leakage current by two to three orders of magnitude, and allows for the integration of bipolar devices and body diode of LDMOSs. On the other hand, the trench technology can improve the current capability and cut dramatically the on-state resistance of the power device.

The performance specs for integrated high voltage and high power devices includes higher breakdown voltage, lower on-resistance, wider bandwidth and smaller size. These performance requests need to be traded-off against each other in most designs. In order to provide the optimized performance for different applications most power IC process provide a range of power device selections.

1.5 Thesis Organization

The thesis is organized as follows. In chapter 2, a hybrid switched-capacitor-resonant (HSCR) LED driver based on a stackable switched-capacitor (SC) DC-DC converter IC is introduced to demonstrate the idea of combining SC converter with resonant converter and capacitive isolation to replace the bulky transformers in traditional LED driver designs and improve the LED driver performance allowing higher efficiency, wider input and output range, and smaller component size. In chapter 3, the LED driver issues of power factor correction (PFC) and luminance flicker reduction is further addressed and the AC-DC rectifier front end for the HSCR DC-DC LED driver is discussed. To demonstrate the proposed solution, a highly integrated LED driver based on multilevel converters with sigma delta modulation is introduced and analyzed. In chapter 4, the conclusion of this thesis is made, and some possible work to extend the study of the topics in this thesis are proposed.

Chapter 2

Hybrid-Switched-Capacitor-Resonant DC-DC Converter Design

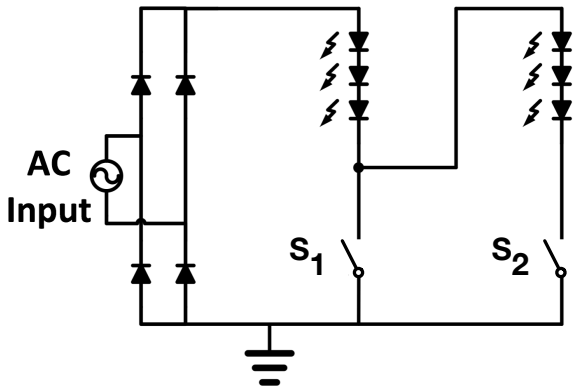
2.1 Introduction

Since an LED is a current driven device whose light emission intensity is proportional to its forward conduction current, LED drivers are necessary to provide current regulation over a range of input and load conditions. A simple way to drive LEDs is to use a linear regulator. Compared to other topologies, linear regulators are often smaller in size without bulky magnetics, easier to design, and they emit little electromagnetic interference (EMI). However, the efficiency of linear regulators is inversely proportional to the conversion ratio and thus too low for most applications requiring high energy efficiency. Fig. 2.1(a) shows a linear LED driver that efficiently performs current regulation and power factor correction (PFC) by alternating the average load impedance with switches and multi-channel LED strings [16]. Disadvantages of such a topology include difficulties in performing LED dimming and adapting to applications with various input or output specifications. Switched-mode LED drivers can achieve much higher power transfer efficiency than linear regulators by using passive energy storage devices and keeping the switch transistors in full-on and full-off states

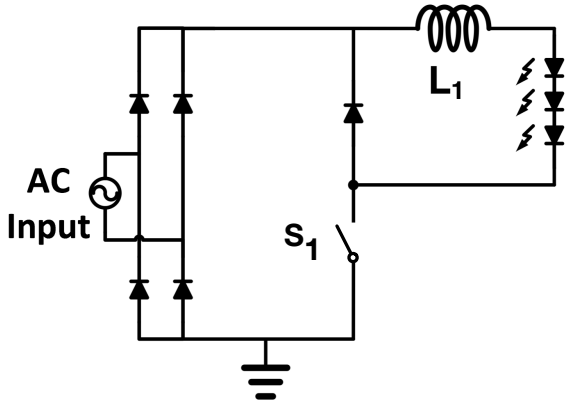
most of the time. The buck-based LED driver, as shown in Fig. 2.1(b), is a widely used topology that can achieve higher efficiency ($> 90\%$) and handle a wide range of input and loading conditions with a simple architecture. In [17], with a 5.5 mH inductor and a peak current controlled PWM method the driver achieves $> 80\%$ efficiency and > 0.9 power factor with large input and LED load variations. Despite its simple topology and good performance, the buck-based driver is not isolated from the AC mains, which can be a safety hazard in certain applications. In addition, the 5.5 mH inductor is large in size. To provide galvanic isolation, the most common solution is to use transformers. Fig. 2.1(c) shows the flyback converter based LED driver which is popular in low to moderate power applications [18]. The major drawback of the transformer-based LED driver is relatively large size and high cost due to the transformer, whose power handling capability is related to its volume. One example of commercial flyback LED driver is shown in Fig. 2.2 [19], where the magnetic transformer takes up significant space on board and cost around 2 dollars.

Switched-capacitor (SC) DC/DC converters provide another solution for high performance and highly integrated LED drivers. In comparison to magnetic-based converters, the SC topologies have a few fundamental advantages. As concluded in [20], any DC/DC converter must have at least two time-varying and/or nonlinear resistors (e.g. switches) and one reactance. The effectiveness of utilizing these two kinds of basic elements in a power converter decides its intrinsic performance-to-cost ratio. For integrated switching transistors, the cost of a device is proportional to its voltage-current (V-A) product. Larger transistors are typically required in order to stand higher voltage stress or to handle larger current while keeping resistive loss small. Likewise, in order to reduce the size of reactive components one must minimize their required energy storage or V-A stress. Thus switching converters should be designed in a way that reduces the total V-A stress over the components. Reference [20] gives two fundamental limits on the minimal V-A stress of the switches and reactive parts of a converter. Through a detailed first-order analysis in [21], it is concluded that SC converters can be superior to the inductor-based buck converter in terms of switch and reactive element utilization, approaching the given fundamental limits.

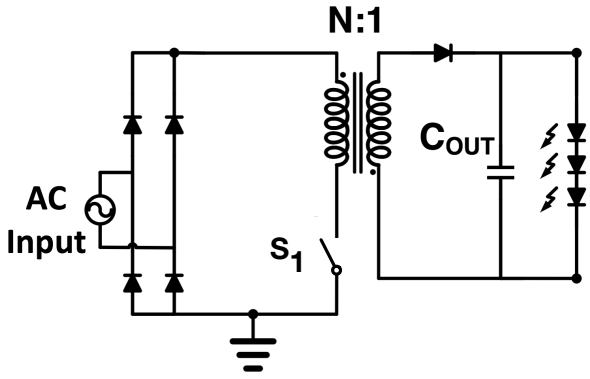
One of the noted advantages of the SC converter topologies is that their main reactive components are capacitors, which exhibit a substantially higher energy and power density



(a)



(b)



(c)

Figure 2.1: Schematics of LED drivers: (a) Simplified circuit of a AC/DC converter free LED driver; (b) Simplified circuit of a conventional Buck LED driver; (c) Simplified circuit of a conventional off-line flyback LED driver.

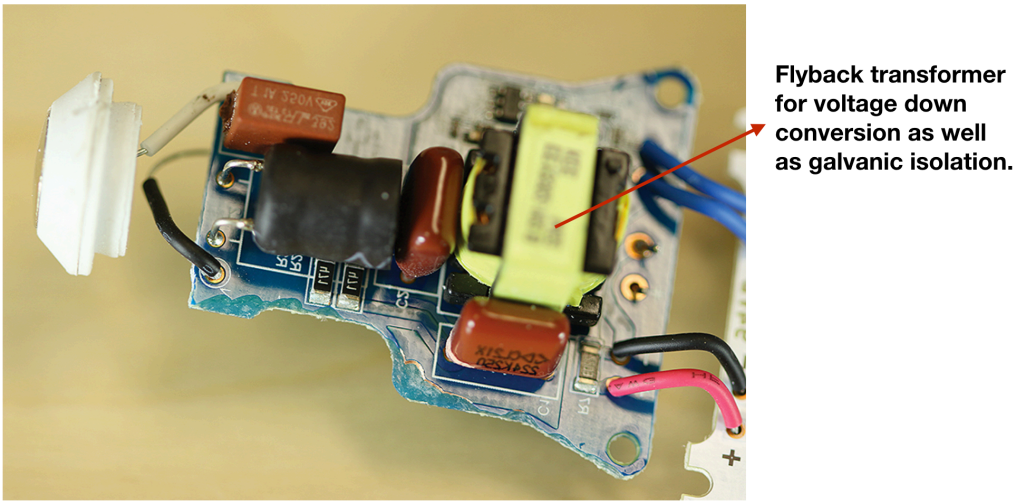


Figure 2.2: Dissembled commercial flyback LED driver circuit.

than magnetics. Such is true for both integrated and discrete components. Typical surface mount capacitors can easily have an energy density three orders of magnitude larger than that of inductors [22]. The significantly higher energy density of capacitors allows for greater potential for integration. In addition, since most of the SC converter topologies (e.g. the ladder type or series-parallel type) arrange the power elements in series to interface the high input/output voltage level, the voltage stress on each individual component is only a fraction of the total rating. This allows the SC converters to use devices with lower voltage rating for "high" voltage applications. In magnetic-based converters, the main switches and reactive elements usually need to stand the whole input voltage or even higher.

However, SC DC/DC converters typically have a fixed input to output-voltage ratio. This behavior can be a disadvantage since LED devices are more conveniently controlled by a regulated forward current. Because of the PVT variation in an LED's I-V characteristic, it is impractical to control the LED's output by voltage regulation. A highly efficient current regulation scheme is required to take advantage of the SC converter topology for use in an LED driver. To achieve this goal, a hybrid switched-capacitor resonant (HSCR) strategy has been developed to combine the SC ladder topology with the series resonant converter [23]. The proposed HSCR converter leverages the advantages of the SC topology, while offering nearly lossless regulation of the output current and a soft-switching configuration

to handle the parasitic capacitance of the switching transistors. The series resonant stage can potentially provide a capacitive galvanic isolation barrier for the LED driver application as well.

We improved the HSCR architecture and implemented a highly integrated LED driver for a wide range of mains voltage standards [24]. To assist in integration our design takes advantage of the multilevel architecture of the SC ladder topology and the lowered individual device stress. As such, we use a medium-voltage-rated Analog-Bipolar-CMOS-DMOS (ABCD) technology to integrate the power transistors, gate drivers, level shifters, and internal DC-DC converters into a standard SC module. These modules can then be stacked in the voltage domain to interface with various mains voltages. This paper analyzes the proposed HSCR DC/DC converter topology [24] and describes the modularized IC implementation in detail. The paper also provides detailed analysis of the power loss of the SC ladder, design of the resonant network, and the performance of the HSCR converter under two different output stage configurations. The measurement results of both two-chips stacking and four-chip stacking HSCR converters are reported. The paper is organized as follows: Section 2.2 introduces the proposed HSCR DC/DC converter. Section 2.3 describes the implementation details of the HSCR converter module IC and Section 2.4 discusses the measurement results. Finally, Section 2.6 concludes the paper.

2.2 Hybrid-Switched-Capacitor-Resonant DC-DC Converter

2.2.1 System Architecture

Fig. 2.3 shows the simplified system architecture of the proposed HSCR LED driver [24]. A power factor correction (PFC) rectifier interfaces the 120 V_{AC} line voltage to the input of the HSCR converter, converting the AC source voltage to about 170 V_{DC}. One example of the PFC rectifier front-end implementation that works with the proposed HSCR converter can be found in [25]. The HSCR converter consists of two main building blocks: a two-phase balanced 4:1 step-down power train, and a L-C resonant output stage. Capacitors $C_{1,2,3,4}$ in the power train are DC capacitors, which ideally distribute the input DC link voltage evenly. In order to balance the charge across each capacitor, flying capacitors C_5

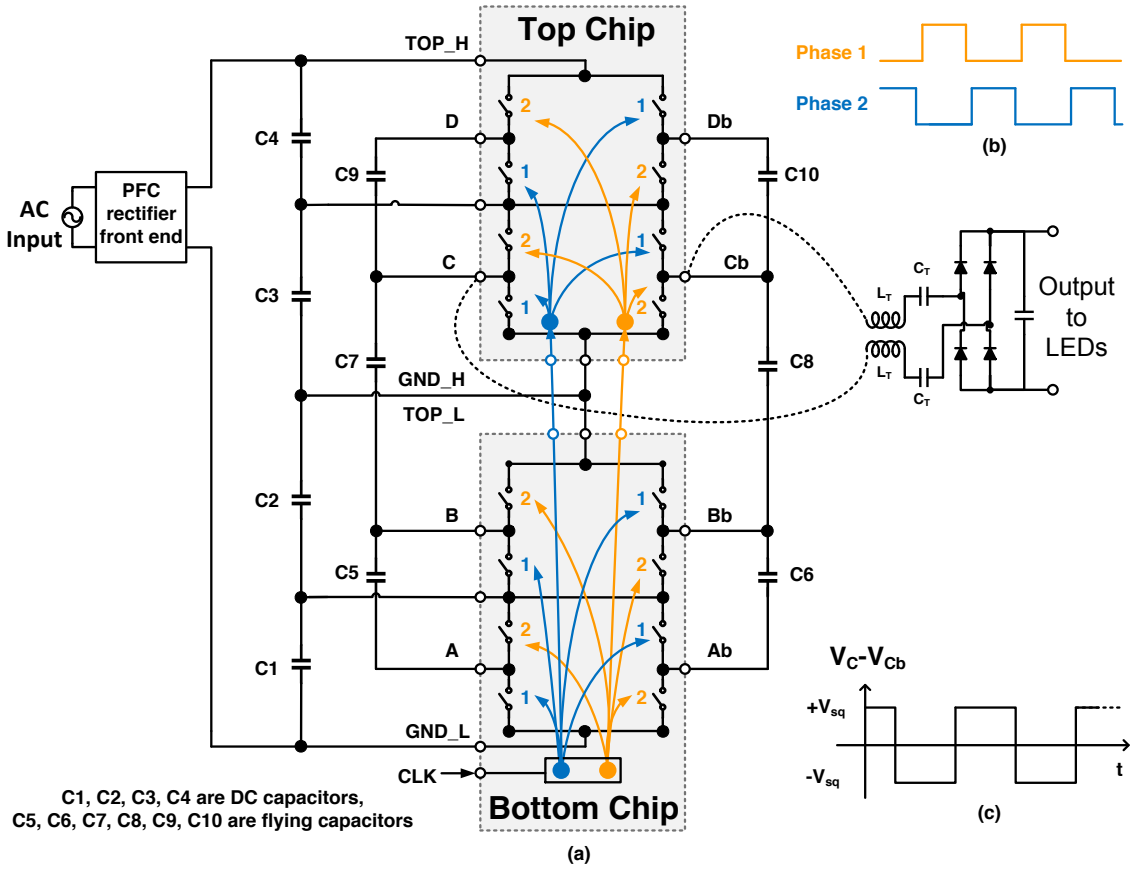


Figure 2.3: (a) System architecture of the chip-stacking hybrid-switched-capacitor-resonant LED driver. (b) Two-phase non-overlapping gate drive signals. (c) Differential output signal between nodes C and C_b of the SC ladder.

to C_{10} are switched in a pair of non-overlapping phases with 50% duty cycle, as shown in Fig. 2.3(b). All of the switches and their driving circuits are integrated on chip. As described in Section 2.1, a chip-stacking configuration is implemented in order to overcome the breakdown voltage limit of the silicon technology. The SC ladder shown in Fig. 2.3 is split into two identical parts each with two DC voltage levels and eight main switches. This eight-switch part is designed as a standard SC module which can be stacked in series in the voltage domain and configured to stand a range of input DC voltage levels. The balanced topology of the SC ladder creates a differential AC square waveform across any two of the symmetrical flying nodes (e.g. node C and Cb in Fig. 2.3(a)). This differential

AC signal is then fed through the L-C resonant tank and rectified to drive the output LEDs. The differential topology helps in minimizing the common-mode signal feed-through to the output. With high voltage (e.g. 5 kV) MLCC capacitors, the resonant bridge can provide DC galvanic isolation between the LED heat spreader assembly and the power train. Since the resonant capacitors are rated for high voltage, the input of the L-C bridge can be attached to any of the symmetrical flying nodes. By varying the switching frequency of the SC ladder, the imaginary impedance of the L-C tank can be altered, thus allowing for output current regulation. Another L-C output network that utilizes all the differential nodes in the SC ladder is shown in Fig. 2.4 and will be analyzed in Section 2.2.2. The modified topology reduces the required capacitance of the DC and flying capacitors and boosts the power efficiency.

2.2.2 Power Loss of the SC Ladder

Proper design of the HSCR DC-DC converter requires insights in analyzing and minimizing its power loss. There are three major contributions of power loss from the SC ladder in steady state: (1) charge sharing loss between the power capacitors during the two-phase operation; (2) resistive conduction loss due to the resonant output current flowing through the power switches; and (3) gate drive loss. The other switching losses, shoot-through current losses, and other parasitic losses are relatively small thus are not discussed in this paper. The efficiency of the output resonant stage and the overall converter will be discussed in Section 2.2.4. We can model the steady state behavior of the SC ladder as an ideal transformer with a series output impedance R_S [26], which represents the power losses and the requisite output voltage drop to transfer charge from input to the load.

The charge sharing loss of traditional SC converters has been well studied and given the complexity of the multi-phase and many-element R-C network, the concept of slow switching limit (SSL) and fast switching limit (FSL) have been used to approximate R_S [26], [27], [28]. The SSL and FSL operation conditions are based on the maximum time constant τ of the SC ladder with respect to the switching clock period T_{sw}. If $\tau \ll T_{sw}$, which is the SSL condition, all the charge sharing between the capacitors or voltage sources are completed within one clock phase. Thus the total loss is $\sum_i \frac{1}{2} C_i \Delta v_i^2$, where the ripple

voltage Δv_i across each capacitor C_i is irrelevant to the resistances in the SC network. The corresponding output impedance can be expressed as $R_{SSL} = \gamma \frac{1}{C_{sc} f}$, where γ is a constant factor derived from the SC ladder topology, C_{sc} is the total capacitance of the SC ladder, and f is the switching frequency. If $\tau \gg T_{sw}$, Δv_i is very small and the charging and discharging current $i_{r,i}$ through each conduction path resistance R_i can be viewed as constant. In this case, which is called the FSL condition, the total loss can be calculated as $\sum_i i_{r,i}^2 R_i$, and the output impedance is $R_{FSL} = \delta R_{on}$, where δ is another constant factor derived from the SC ladder structure. If τ is comparable with T_{sw}, the loss is a function of the two[28].

The resistive conduction loss caused by the resonant output current of the SC ladder can be written as $I_{rms}^2 \cdot \sigma R_{on}$, where I_{rms} is the rms value of the resonant output current and σ is a constant factor. Thus the equivalent output impedance is similar to the FSL condition: $R_C = \sigma R_{on}$.

The gate drive power of the primary power switches is another major source of loss. For an n:1 HSCR DC-DC converter, the number of high power switches is $2n$. Thus the total gate drive loss is given by:

$$P_G = 2nfC_{gg}V_g^2 = p_1 \cdot fnWV_g^2, \tag{2.1}$$

where C_{gg} is the parasitic gate capacitance of the switch transistors, which is proportional to the transistor width W, and V_g is the gate drive voltage. p_1 is a constant derived from transistor characteristics as follows:

$$p_1 = 2 \cdot \frac{C_{gg}}{W} = 2C_0, \tag{2.2}$$

where C_0 is the parasitic gate capacitance of the transistor per unit width. It is a common process characteristic of MOSFETs. Similarly, R_{on} of transistors in linear region can be written as:

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_g - V_{th})} = p_2 \cdot \frac{1}{W \cdot (V_g - V_{th})}, \tag{2.3}$$

where p_2 is also a constant derived as follows:

$$p_2 = \frac{L}{\mu_n C_{ox}}, \tag{2.4}$$

where μ_n and C_{ox} are also process characteristics of MOSFETs. Combining the power loss of charge sharing, resistive conduction, and gate driving, the minimum value of the total power loss from the SC ladder is limited by the following three terms: $\frac{k_1}{C_{sc}f}$, $\frac{k_2}{nW(V_g-V_{th})}$, and $k_3 \cdot fnWV_g^2$, where $k_{1,\ 2,\ 3}$ are constant parameters. Since we use off-chip ceramic DC and flying capacitors, C_{sc} is mainly limited by the component cost and PCB area. Parameters f, $(n \cdot W)$, and V_g needs to be traded-off to optimize the power efficiency.

2.2.3 Multi-level Resonant Output Network

An alternative HSCR converter topology using a multi-level resonant L-C output stage is proposed and shown in Fig. 2.4. As mentioned in Section 2.2.1, the isolation capacitors in the resonant tank are rated for high voltage (e.g. 5kV) and can be attached to any of the output differential nodes of the SC ladder. Thus in the multi-level output network we make use of every level of the SC ladder. Fig. 2.4 shows the charge flow of the modified HSCR converter in both phases of operation. Since each level of the SC ladder contributes equally to the output power in this modified topology, the converter is effectively a series-parallel circuit, but with zero charge variations of the DC and flying capacitors. As a result, the ideal circuit is free of capacitor charging and discharging loss and the current flows in the power train are purely resonant currents. From Fig. 2.4, the equivalent R_S can be written as:

$$R_S = \frac{2R_{on}}{n} = \frac{R_{on}}{2}, \tag{2.5}$$

since $n = 4$. Thus the total power loss can be expressed as:

$$P_{loss\_SC} \ = \ I_{rms}^2 \cdot R_S \ + \ P_G \ = \ \frac{k_2'}{nW(V_g - V_{th})} \ + \ k_3' \cdot fnWV_g^2. \tag{2.6}$$

Here we extract the conversion ratio n from the constants to indicate its impact on the power loss. The absence of the R_{SSL} term $\frac{k_1}{C_{fly}f}$ enables us to reduce the capacitance of the DC and flying capacitors by at least three orders of magnitude. However, the capacitors should still exist to handle the output current mismatch in the different branches of the L-C network, as well as provide enough DC supply for the gate drive channels in the SC converter IC. The absence of the R_{SSL} term also allows the switching frequency to be reduced even with scarce capacitance resources, thereby reducing gate drive loss. However,

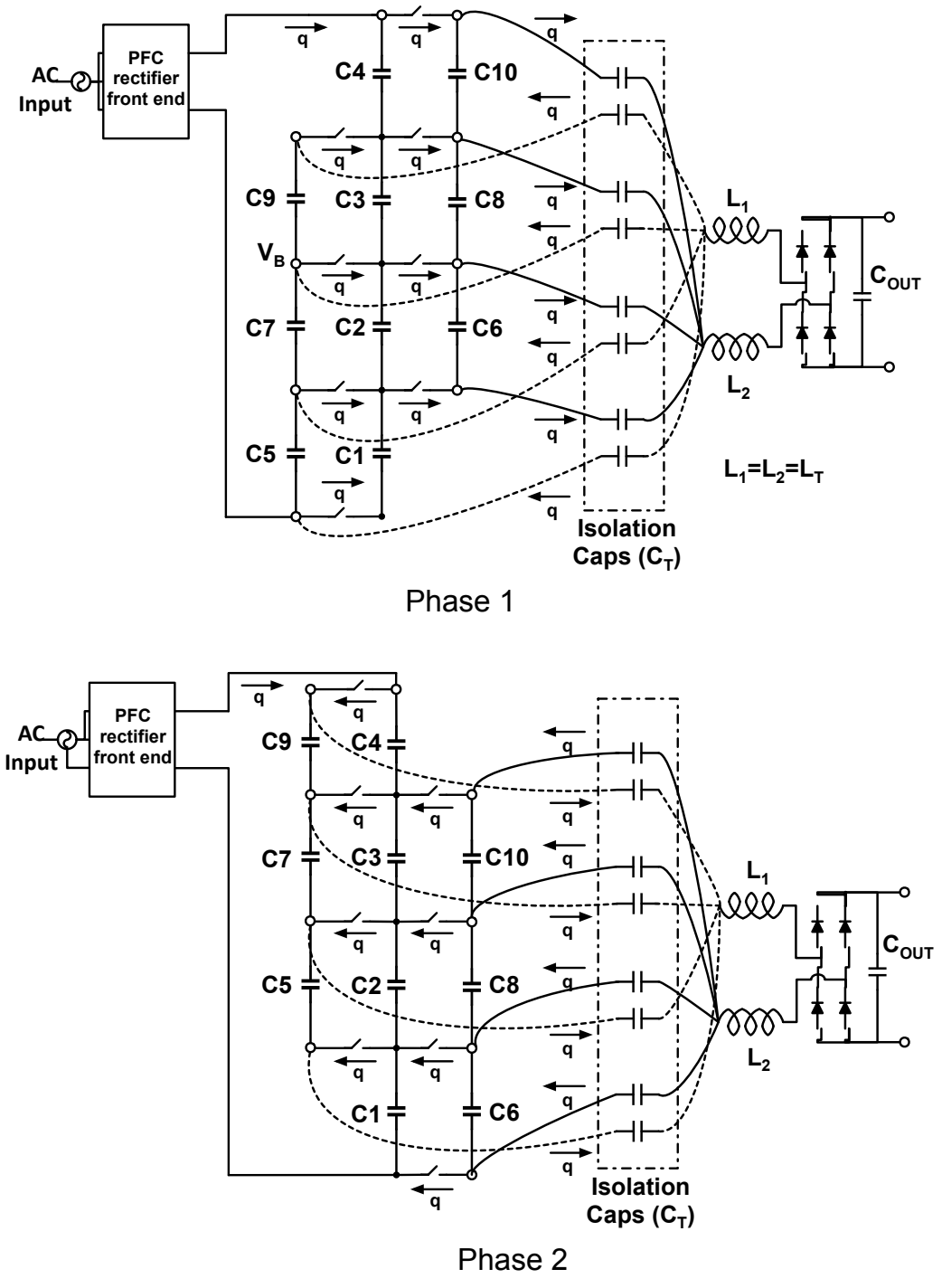


Figure 2.4: Charge flow in SC ladder when the L-C resonant bridge is attached to all four pairs of differential notes.

f is still limited by the passive components' sizes in the resonant network, which will be analyzed in the following section. The performance of this topology is reported in Section 2.4.

2.2.4 Design of the Resonant Tank

The analysis in this section is based on the improved multilevel resonant architecture as discussed in 2.2.3. As depicted in Fig. 2.4, the converter is differentially symmetric. The output stage consists of a split-wound coupled inductor, two isolation capacitors for each SC level (eight in total), and a bridge rectifier. The equivalent inductance on each side is L_T and the capacitance is C_T for each isolation capacitor. Fig. 2.5(a) shows the equivalent circuit for the AC components of the output stage. By removing the DC components, we can now look at the multilevel SC ladder stacked in the voltage domain as multiple basic switching cells aligned in parallel. Assuming the devices are perfectly matched, the parallel AC output signals from each side of the balanced SC ladder are equal and $v_{SP} = -v_{SN}$. The resonant output stage is attached to the SC ladder to provide low-loss current regulation and achieve zero voltage switching (ZVS) operation. In addition, it has the potential to serve as a galvanic isolation barrier [23]. In order to properly design the L-C tank a frequency-domain analysis is introduced below.

2.2.4.1 Circuit Analysis

The output stage is studied under the following assumptions: 1) The rectification diodes are ideal devices with fixed forward DC drop V_F and linear on resistance R_F. 2) The passive elements have no reactive parasitic elements. 3) The loaded quality factor Q_L of the resonant output stage is sufficiently high so that the current through the resonant tank is sinusoidal. Fig. 2.5(b) shows the simplified equivalent circuit of the L-C resonant stage. v_S and i_S are the fundamental components of the differential square-wave output voltage and current from the SC ladder. Voltage v_D is the fundamental component of the input square-wave signal to the diode rectifier with ideal rectification diodes. Voltage v_T is the voltage across the L-C tank, and v_R is the voltage across the resistive components in the output stage. Symbols V_S, I_S, V_D, V_T, and V_R are the amplitudes of the sinusoidal signals. P_O,

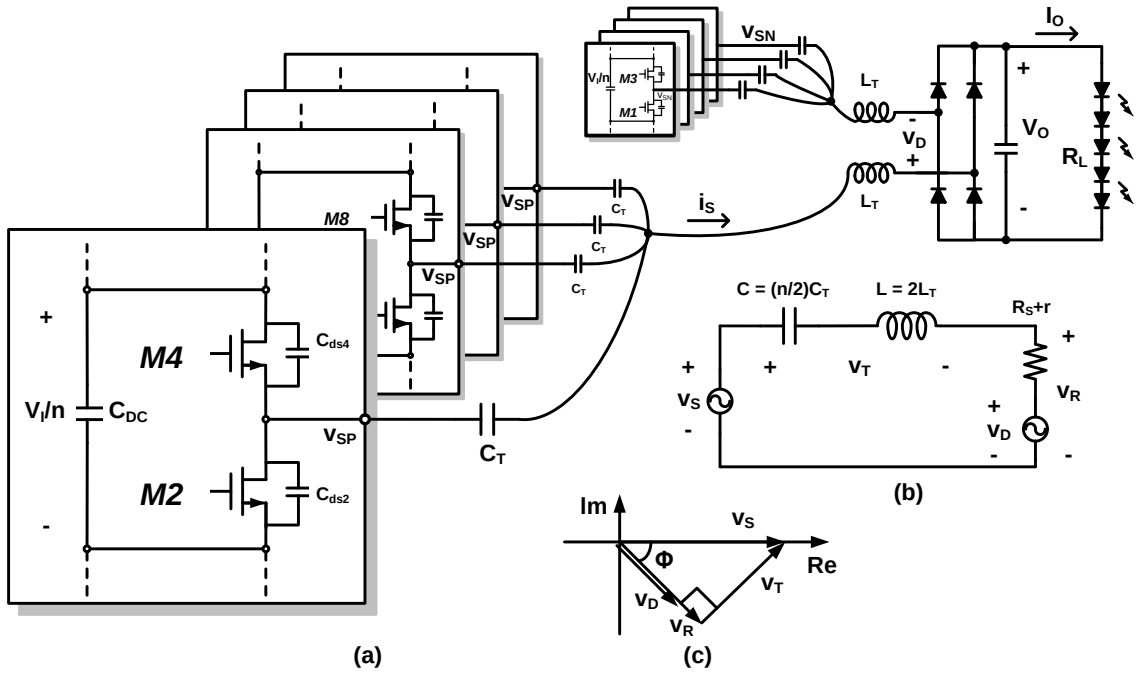


Figure 2.5: (a) Equivalent circuit of the HSCR converter for AC analysis. (b) Simplified single-end equivalent circuit of the HSCR DC-DC converter. (c) Phase diagram used to design the resonant tank.

V_O and I_O are the DC output power, voltage and current of the LED driver. $R_S = 2R_{on}/n$ is derived from the on resistance of the switch transistors. r represents the equivalent series resistances of the inductors. R_L is the LED load resistance and is equivalent of a resistance $R'_L = \frac{8R_L}{\pi^2}$ looking into the diode rectifier bridge from the resonant tank's output[1]. The total input resistance of the rectifier bridge can now be derived as $R_i = R'_L + 2R_F + \frac{2V_F R'_L}{V_O}$, where R_F and V_F are the on resistance and the forward voltage of the diodes. R_L and V_O can be derived from the output power specification P_O and the I-V characteristics of the LED load. As an example, twelve 1.2 $Watt$ LED diodes with a 3.2 V operation voltage give $R_L \approx 100\Omega$ and $R'_L \approx 81\Omega$. Together with $R_F = 0.025\ \Omega$ and $V_F = 0.5\ V$, we have $R_i \approx 85\Omega$. Thus the power path efficiency of the HSCR converter excluding the gate drive power is given by:

$$\eta_r = \frac{R'_L}{R_i + R_S + r} = \frac{R'_L}{R_i + 2R_{on}/n + \omega L/Q_i}, \tag{2.7}$$

where $L = 2L_T$ is the total inductance of the resonant tank and Q_i is the quality factor of the inductor. Using(2.1), (2.3) and (2.7), the overall conversion efficiency can be simplified as:

$$\eta = \frac{P_O}{P_G + P_O/\eta_r} = \frac{1}{\frac{P_G}{P_O} + \frac{2R_{on}}{nR'_L} + \frac{\omega L}{R'_L Q_i} + \frac{R_i}{R'_L}} = \frac{1}{c1 \cdot (nW)f + c2 \cdot (nW)^{-1} + c3 \cdot fL + c4}, \tag{2.8}$$

where $c1$, $c2$, $c3$, and $c4$ are constants derived from the output specifications and device characteristics: $c_1 = \frac{2C_0 V_g^2}{P_O}$, $c_2 = \frac{L}{\mu_n C_{ox}(V_g - V_{th})} \cdot \frac{2}{R_L}$, $c_3 = \frac{2\pi}{R'_L Q_i}$, $c_4 = \frac{R_i}{R'_L}$. The values of the design parameters f, W, and L need to be optimized for highest efficiency. Besides (2.8), we can derive another limit on the value of $f \cdot L$. Fig. 2.5(c) plots the phasor diagram of the resonant stage. As stated in assumption 3), v_S, v_T, v_R and i_s are sinusoidal signals. The phase angle between v_S and i_s is given by:

$$\tan\psi = \frac{\omega L - \frac{1}{\omega C}}{R} = \frac{\sqrt{V_S^2 - v_R^2}}{V_R} \approx \frac{\sqrt{V_S^2 - V_D^2}}{V_D}, \tag{2.9}$$

where $C = (n/2)C_T$, $R = R_i + R_S + r$, $V_S = (4/\pi)V_I/n$, and $V_D = (4/\pi)V_O$. V_I is the DC input voltage of the SC ladder. From (2.9) we derive:

$$f \cdot L = \frac{1}{2\pi}(\tan\psi \cdot R + \frac{1}{2\pi f C}) \approx \frac{\tan\psi R_i}{2\pi} + \frac{1}{4\pi^2 f C}. \tag{2.10}$$

[1] $I_S = \frac{\pi}{2} I_O, V_D = \frac{4}{\pi} V_O, R'_L = \frac{V_D}{I_S} = \frac{8V_O}{\pi^2 I_O} = \frac{8R_L}{\pi^2}$

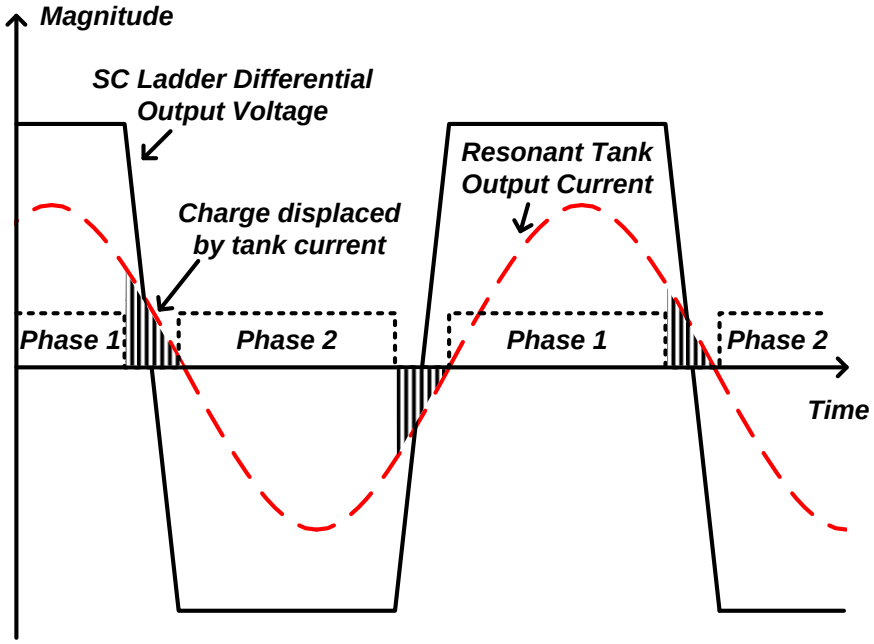


Figure 2.6: Example of ideal zero voltage switching waveforms. Solid: SC ladder differential output voltage. Dashed: resonant tank current. Dotted: two-phase gate-drive voltages.

The first term in (2.10) is constant. Combining (2.8) and (2.10), we obtain:

$$\eta \approx \frac{1}{c1 \cdot Wf + c2 \cdot W^{-1} + c3' \cdot (fC)^{-1} + c4'}, \tag{2.11}$$

where $c3'$ and $c4'$ are constant parameters. The denominator can be minimized by optimizing the transistor width W and switching frequency f once the tank capacitance C is given. From (2.11), larger capacitance within the design specifications should be used. However, the capacitance value is often safety-limited due to the common-mode impedance requirements for galvanic isolation. The usual upper bound is about 10 nF. Thus in order to meet the safety standards, each isolation capacitor C_T in the HSCR converter should be $\leq \frac{5\ nF}{n_{stage}}$, where n_{stage} is the number of stages of the converter.

2.2.4.2 Zero Voltage Switching (ZVS)

The parasitic capacitor C_{ds} of each switch transistor needs to be charged to V_I/n when the transistor is off and discharged to zero when it is on, resulting in a significant energy loss at high frequencies and voltages. In order to minimize this loss, a ZVS condition should

be enforced. This is achieved by providing a resonant switching transition during the dead time of the two-phase gate drive signals. Fig. 2.5(a) shows the parasitic C_{ds} of the switch transistors. When switch M_2 is turned on, C_{ds2} discharges from V_I/n to zero while C_{ds4} is charged from zero to V_I/n. By keeping the switching frequency of the SC ladder above resonance, the tank current can displace the charge across all the C_{ds} capacitors. Fig. 2.6 shows one example of the ideal waveforms of the differential output voltage of the SC ladder and the resonant tank current together with the two-phase gate drive signals. The total charge that needs to be displaced from C_{ds} of n stages is $Q_{ds} = C_{ds}V_I$. Q_{ds} should be smaller than the maximum charge Q_{max} the tank current can displace. As depicted by the shaded region in Fig. 2.6, Q_{max} can be found by integrating the tank current between the falling edge of the gate drive signal and the tank current's zero crossing. Thus Q_{max} and the switching frequency range for ZVS is given by:

$$Q_{max} = \frac{1}{\omega}\int_{\frac{\pi}{2}}^{\frac{\pi}{2}+\psi} |i_s|\cos\theta \; d\theta = \frac{|i_s|}{\omega}(1-\cos\psi), \tag{2.12}$$

$$f \leq \frac{|i_s|}{2\pi C_{ds}V_I}(1-\cos\psi) = \frac{I_O}{4C_{ds}V_I}(1-\cos\psi). \tag{2.13}$$

2.2.5 LED Dimming

The HSCR converter can be efficiently dimmed by gating the input clock with a low frequency pulse-width modulation (PWM) signal, as is depicted in Fig. 2.7. The PWM signal activates and deactivates the HSCR converter at around $2kHz$ with a tunable pulse width to control the average power delivered to the LED diodes. When the HSCR converter is activated, it operates with high efficiency as discussed above. When it is completely deactivated, it consumes no power. However, the converter suffers extra power loss during the start-up and shut-down transitional phases, which reduces its average efficiency in the heavily dimmed situations.

2.2.6 Safety Performance

As mentioned in Section 2.2.1, the differential topology of the HSCR LED driver minimizes the common-mode signal feed-through to the output LEDs. To understand this, a simplified

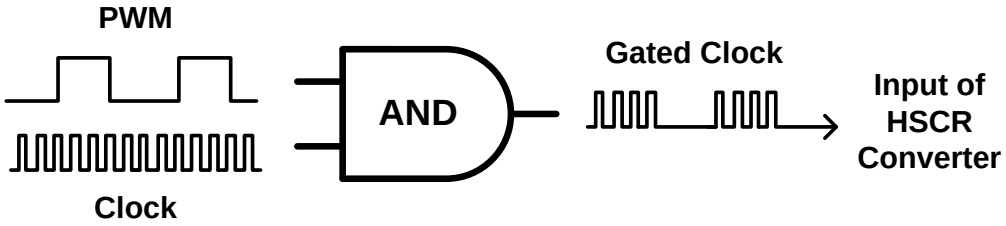


Figure 2.7: PWM dimming of the LED driver.

HSCR converter is shown in Fig. 2.8 below. In order to analyze the circuit and decompose the common-mode and differential-mode signals, we can replace the left-hand and right-hand circuits of the resonant tank with equivalent voltage sources, as depicted in Fig. 2.9. Here we neglect the parasitics of the components. V_{S_DM} represents the differential switching signal from the switched-capacitor ladder. V_L models the AC voltage (square-wave) imposed by the rectifier. V_{S_CM} is a common-mode signal source representing earth-referenced signals developed by rectifying the AC line, for example, these are the voltages present alternatively on hot and neutral input lines on the source side. Z_{large} is the high impedance between the user's ground and the neutral input line. If the components are perfectly matched and assuming perfect 50% switch duty cycle, the differential square signal from the SC ladder has zero common-mode voltage and thus has no common-mode feed through given the symmetrical circuit topology. When $V_{S_CM}$is nonzero, but at the line frequency and its low harmonics, the common-mode signal will see a large impedance due to the small capacitors in the resonant coupling network. That's why we limit our total tank capacitance to below 10 nF (133 $k\Omega$ at 120 Hz). Even with a short between the source earth and the secondary ground of the converter, the converter can still have high common-mode rejection ratio given the isolation capacitors are sized properly.

The touch current and protective conduction current analysis can be done with the circuit configuration depicted in Fig. 2.10. Only a common-mode signal is applied to the input of the resonant tank and a measuring network is connected to the center-tap of the LED string. The measuring network is a unweighted human body model shown in Fig. 2.11. The current goes through the human body can be measured as $I_B = V_B/R_B$.Assuming the rectifier diodes are ideal and the output capacitor is infinitely large, we can draw the

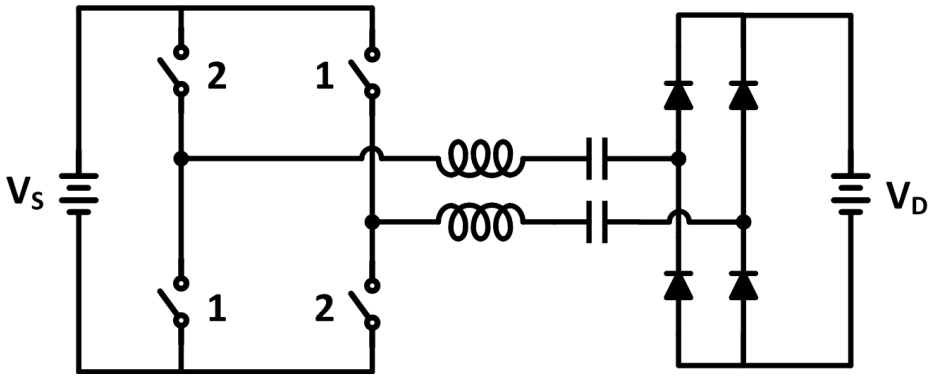


Figure 2.8: Simplified HSCR LED driver circuit diagram.

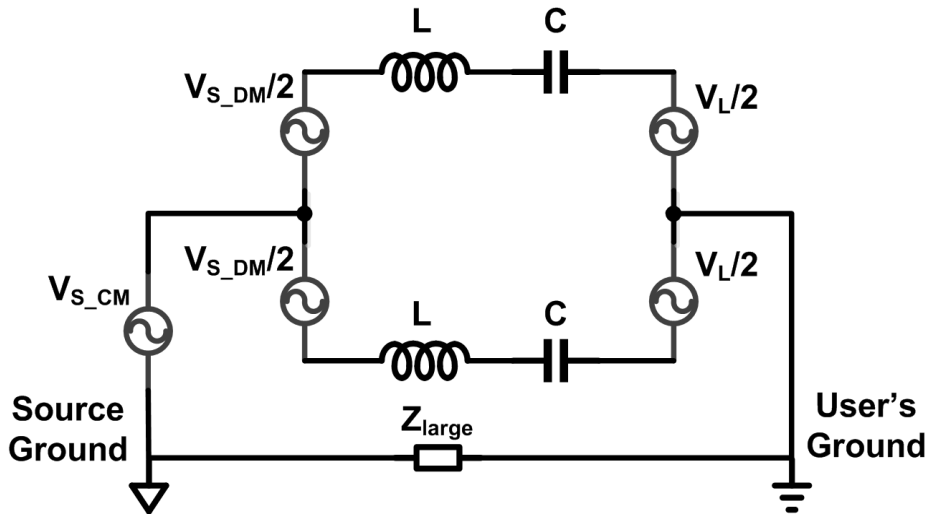


Figure 2.9: Equivalent circuit of the HSCR LED driver for common mode signal analysis.

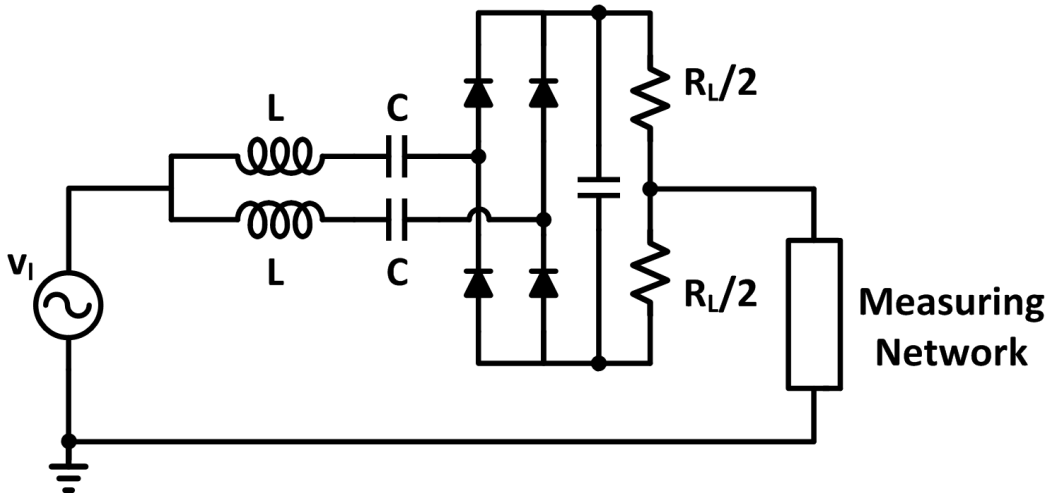


Figure 2.10: Circuit configuration to measure the 120 Hz leakage current.

common-mode half circuit in Fig. 2.12. The touch current amplitude I_B can be written as:

$$I_B = V_I|\frac{1}{R_B + \frac{R_L}{4} + \frac{j}{2}(\omega L - \frac{1}{\omega C}) + \frac{1}{1/R_S + j\omega C}}| \approx V_I \cdot 2\omega C, \tag{2.14}$$

where V_I is the amplitude of the common-mode input signal, R_L is the load resistance (around 100 Ω), R_S and R_B is from the unweighted human body model above. Since the resonant capacitance C = 2.9 nF dominates in 120 Hz frequency, the touch current and protective conductor current can both be approximated as $2\omega C \cdot V_I$. Given the 120 Hz full wave rectified sinusoidal signal can be written as:

$$f(t) = \frac{2A}{\pi} - \frac{4A}{\pi}\sum_{1}^{\inf}\frac{cos(n\omega_0 t)}{4n^2 - 1}, \tag{2.15}$$

where A = 45 V in normal operation, the fundamental component of the touch current or protective conductor current can be calculated as $I_{B1} = 8/3\pi \cdot A\omega C = 83.5\ \mu A$. The calculated current waveform is depicted in Fig. (f) below, with peak current value smaller than 120 A, which meets the IEC60950 specification.

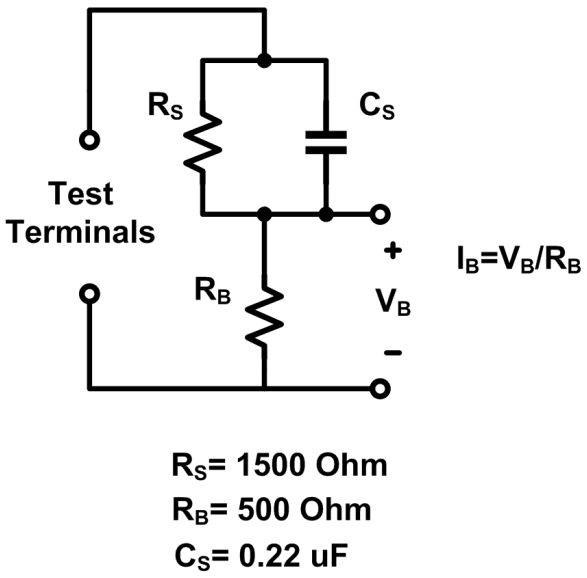


Figure 2.11: The human body model for unweighted touch current measurement.

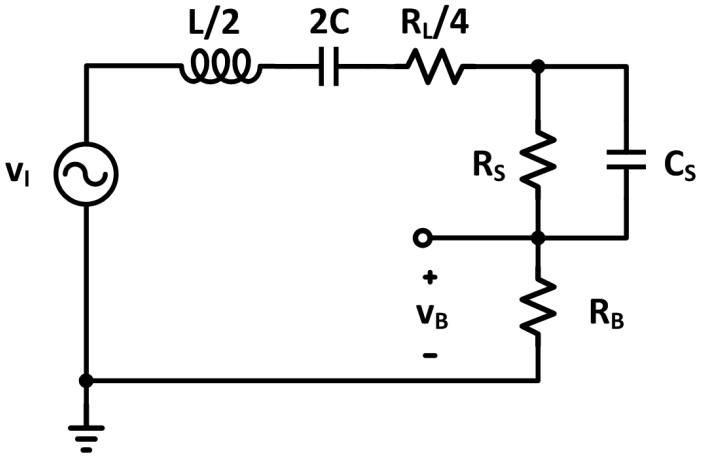


Figure 2.12: Half circuit of the 120 Hz leakage current measurement circuit.

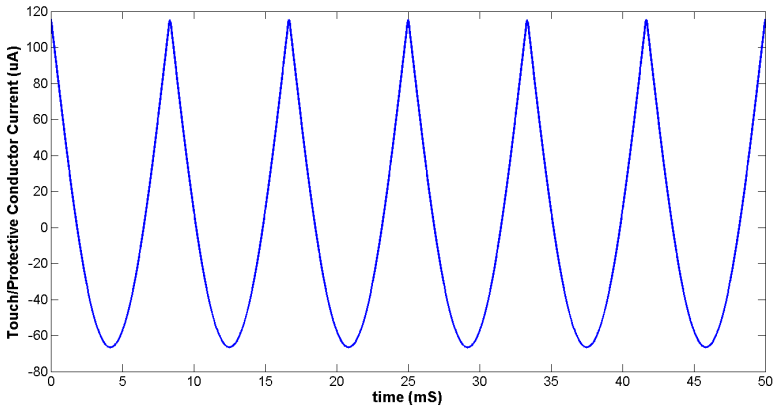


Figure 2.13: Calculated touch/protective conductor current waveform.

2.3 HSCR LED Driver IC Design and Building Blocks

2.3.1 Chip-Stacking Topology

The prototype HSCR DC-DC converter is designed to handle multiple mains voltage standards such as 120 V_{AC} and 240 V_{AC}, which respectively become 170 V_{DC} and 340 V_{DC} after rectification. The characteristics and availability of industrial high voltage silicon processes can limit the application and performance of off-line power converter ICs. Taking advantage of the multilevel structure of the proposed HSCR topology, a chip-stackable DC-DC converter is implemented in a 120 V rated technology. By stacking multiple chips in the voltage domain we can exceed the breakdown voltage limit of the silicon process and handle a range of input voltage levels.

2.3.2 Overall Architecture

The overall architecture of the stackable SC converter IC is shown in Fig. 2.14, which in this example represents the bottom chip of Fig. 2.3(a). The eight main switches, M_1 to M_8, with their gate drive circuits are integrated onto the IC. Here we represent each main switch and its driving circuits as a single channel, shown in Fig. 2.16. The main switches are implemented with N-type Laterally Diffused Metal Oxide Semiconductor (NLDMOS) transistors. Each transistor only needs to block a voltage drop of V_{IN}/n, where n is the

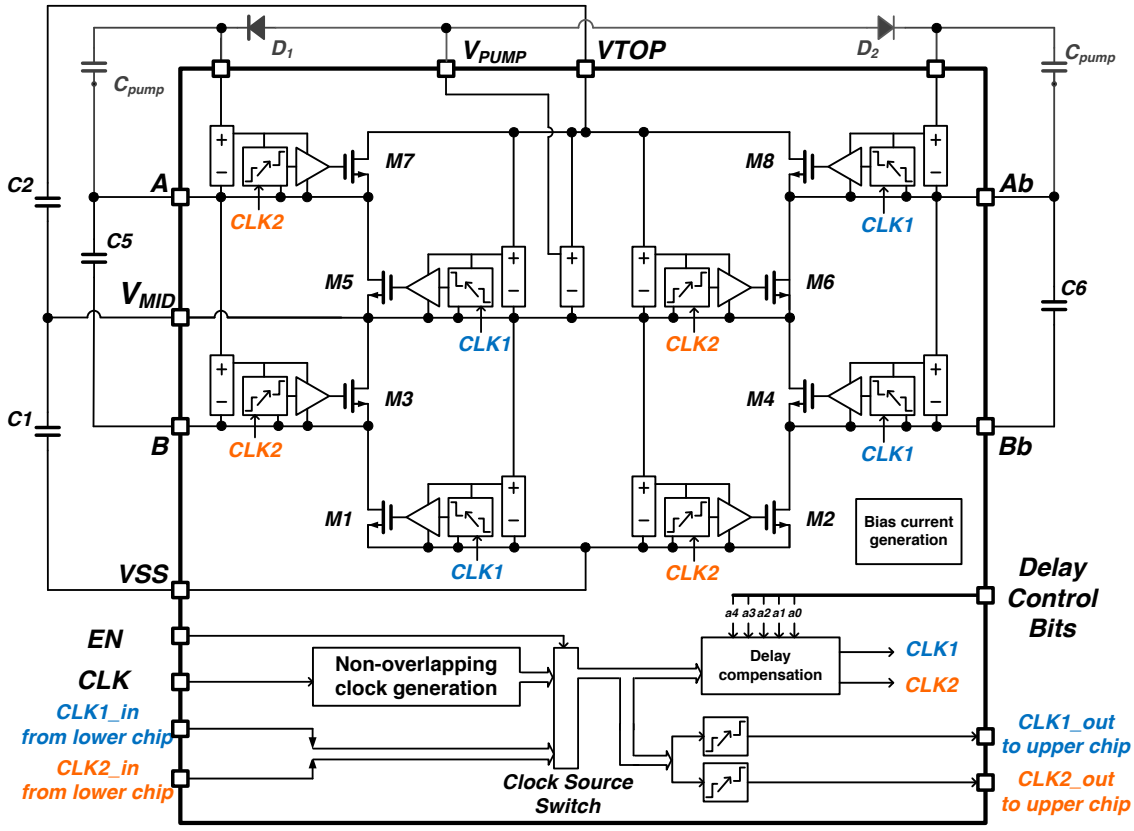


Figure 2.14: Architecture of the SC Converter IC.

conversion ratio of the converter. Since the off-chip capacitors $C_{1,2,5,6}$ are large ($> 200\ nF$), they can be used as DC voltage supplies for the gate drive channels. The static capacitors C_1 and C_2 supply the gate drive channels for $M_{1,2,5,6}$. Similarly, the flying capacitors C_5 and C_6 supply the channels for M_3 and M_4. Two small capacitors C_{pump}, a voltage supply generator for V_{pump}, along with diodes D_1 and D_2 form a charge pump that provides the supply voltage for the channels of the top switches M_7 and M_8. Note that the voltage on the positive plate of C_{pump} exceeds V_{TOP} by V_{pump} when the switches are turned on. V_{pump} should be large enough to supply the top channels while keeping $V_{TOP} + V_{pump}$ smaller than the breakdown voltage of the silicon process. C_{pump} can be as small as a few pF, and can be integrated on chip with D_1 and D_2. The operation of the main switches are controlled by a pair of non-overlapping clock signals CLK1 and CLK2. These signals are generated in the 0 V to 5 V voltage domain and are level-shifted to the voltage domain of each gate drive channel.

2.3.3 Signal Path and Delay Compensation

The stacked chips in the SC ladder can be configured to pass and synchronize the gate drive clock signals for each switch channel. By activating the control bit EN, the bottom chip selects CLK as the input, from which a pair a non-overlapping gate drive signals with the same frequency as CLK are generated. These clock signals are simultaneously sent in two directions. In one direction, the signals are fed through a delay chain and level-shifted to the gate drive channels within the chip, as shown in Fig. 2.15(a). In the other direction, the clock signals are level-shifted to above V_{TOP} and sent to the upper chip. The upper chip can then utilize the synchronized clock signals in the same way. As discussed in Section 2.2.2, in order to have optimal efficiency, the capacitor charge variation per clock phase Δq should be minimized and balanced across capacitors. However, mismatched gate drive signals lead to unbalanced charge transfer and additional loss. In the worst case, gating mismatch can cause shoot-through current, which can burn a large amount of energy and destroy the switches. For these reasons, the delay compensation block is introduced to compensate for the delay in the clock signal path between chips. In general, the delay is a product of the level shifters, buffers, and signal path parasitics. The delay compensation ultimately allows

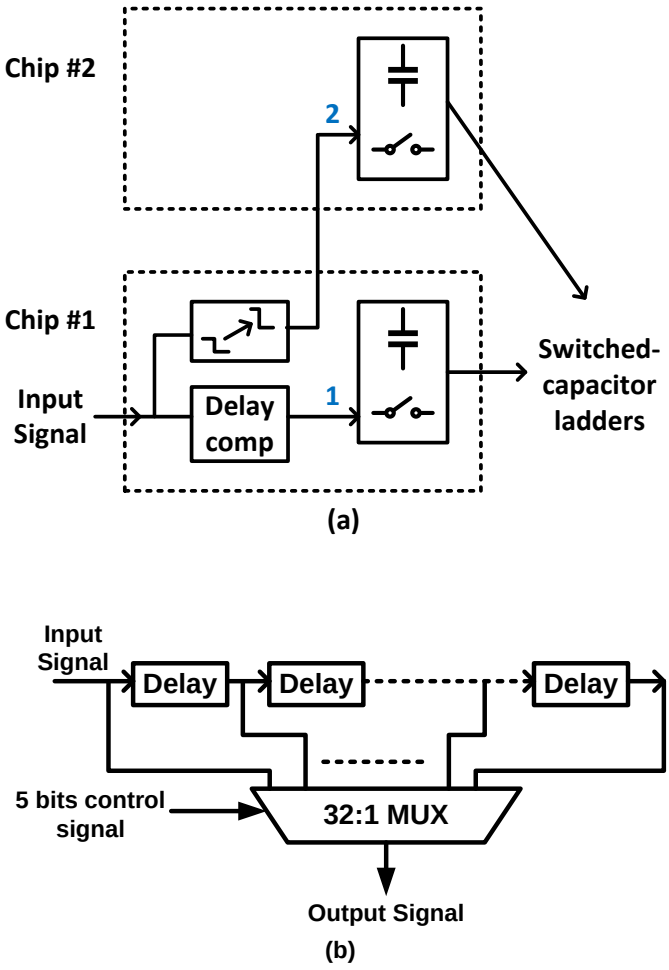


Figure 2.15: Block diagram of the (a) delay compensation system; and (b) digital controlled delay generation chain.

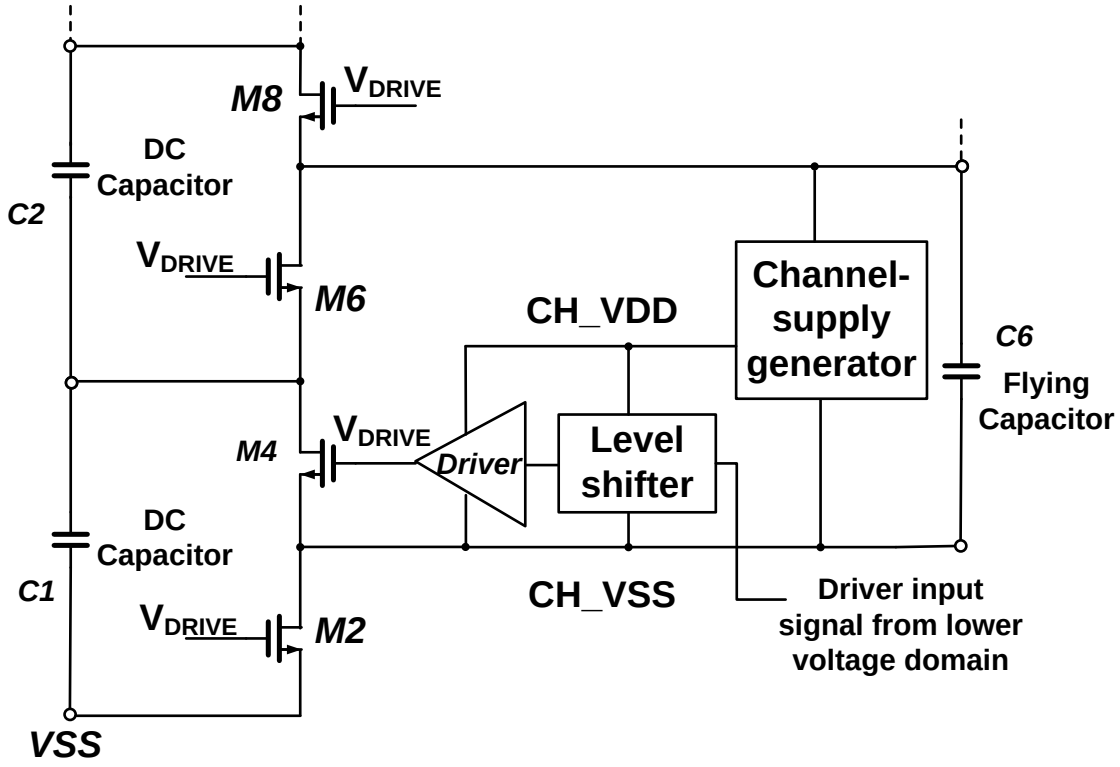


Figure 2.16: Block diagram of the gate driver.

for the gate drive signals to arrive at the main switches in all the chips with a negligible timing mismatch ($< 6\ nS$). The delay chain is implemented with 31 inverter-based delay elements and a 32:1 MUX, controlled by a 5-bit control signal. Each element can generate 580 ps of delay, allowing for a maximum delay of around 18 ns. Simulation shows that as long as the mismatch is within 6 nS between chips, its effect on efficiency is negligible.

2.3.4 Gate-Driving Circuits Implementation

The schematic of a gate drive channel is shown in Fig. 2.16. The channel consists of a channel-supply generator, a level shifter, and a gate driver.

2.3.4.1 Channel-Supply Generator

A channel-supply generator is required to generate a 5 V DC supply above the source voltage of the NLDMOS switching transistor in order to drive it. A 5 V supply voltage is selected

based on the $V_{GS,\ MAX}$ of the NLDMOS device. The supply generator is implemented as a simple linear regulator due to the restrictions on the silicon area and the self start-up requirements of the converter. Conveniently, the regulator can be built with the 5 V Zener diode provided by the technology, shown in Fig. 2.17(a). A reference voltage V_{REF} is generated from a bias current I_{bias} flowing through a Zener diode and a diode-connected PLDMOS device. This reference voltage is held constant at $V_{REF} = V_{ch\_vss} + V_{GS2} + V_Z$, where V_Z is the Zener voltage. Transistor $M1$ acts as an amplifier whose output voltage is $V_{ch\_vdd} = V_{REF} - V_{GS1} \approx V_Z + \sqrt{I_{BIAS}/K_2} - \sqrt{I_{LOAD}/K_1}$, where K_1 and K_2 are the $\frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ constants of devices M_1 and M_2. C_1 is the output decoupling capacitor. In the case where the regulator is in parallel with a flying capacitor, node ch_vss has a voltage swing of around 42.5 V. Due to the parasitics between the devices and the substrate, $V_{REF} - V_{ch\_vss}$ and V_{GS2} can change drastically during the switching period. Thus capacitor C_2 is needed to stabilize the reference node and protect devices from voltage breakdown. Ideally we would like to reduce I_{bias} to save power. On the other hand, when a large pulse current is drawn from ch_vdd, e.g. while the gate driver is turning on the main switch by charging the C_{GS} of the large NLDMOS, the pulse current can be coupled through C_{GS1} to the reference node V_{REF} and generate a significant ΔV across C_2. The rising slope of V_{REF} to its set value influences the voltage at the gate of the main switch, which ultimately affects the switch's average R_{on}. In order to reduce the voltage variation on V_{REF}, the size of M_1 needs to be limited and the value of I_{bias} should be optimized to balance power consumption and V_{REF} variation.

2.3.4.2 Level Shifter

The schematic of the level shifter circuit is shown in Fig. 2.17(b). The input clock signals Clk and Clk_b are in the low voltage domain between V_{DD} and V_{SS}, while the shifted output signal Clk_{out} is between Ch_{VDD} and Ch_{VSS}. The voltage drop from Ch_{VSS} to V_{SS} can be up to 100 V. Transistors M_1 and M_2 form a differential pair with a regenerative-connected load M_7 and M_8. M_1 and M_2 are high voltage devices that isolate the two voltage domains to protect the low voltage transistors. The swing of the up-shifted signal V_A and V_B is limited by diode connected transistors M_5 and M_6, so they stay above V_{Ch_VSS}.

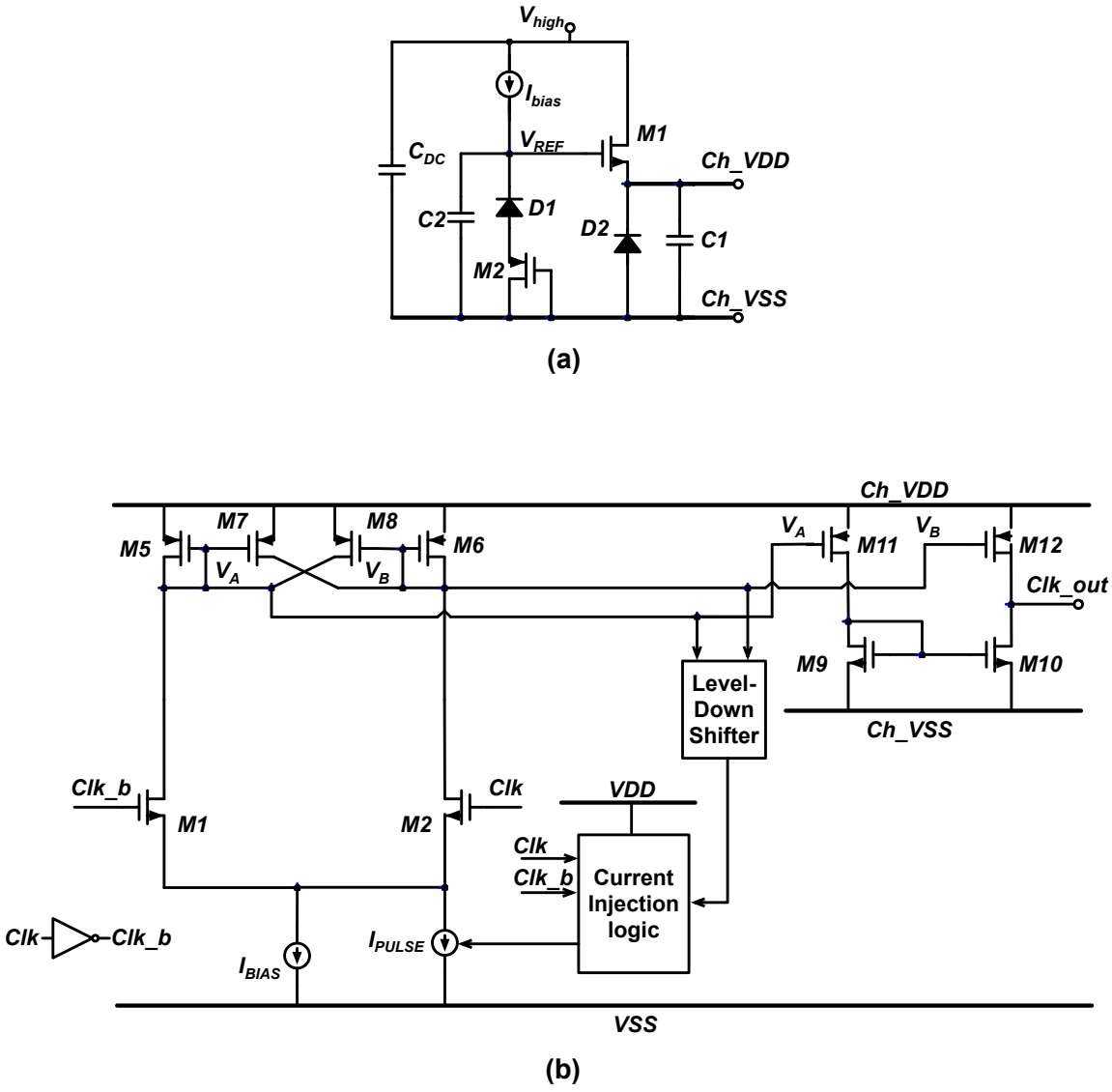


Figure 2.17: Schematic of (a) the channel-supply generator and (b) the level shifter.

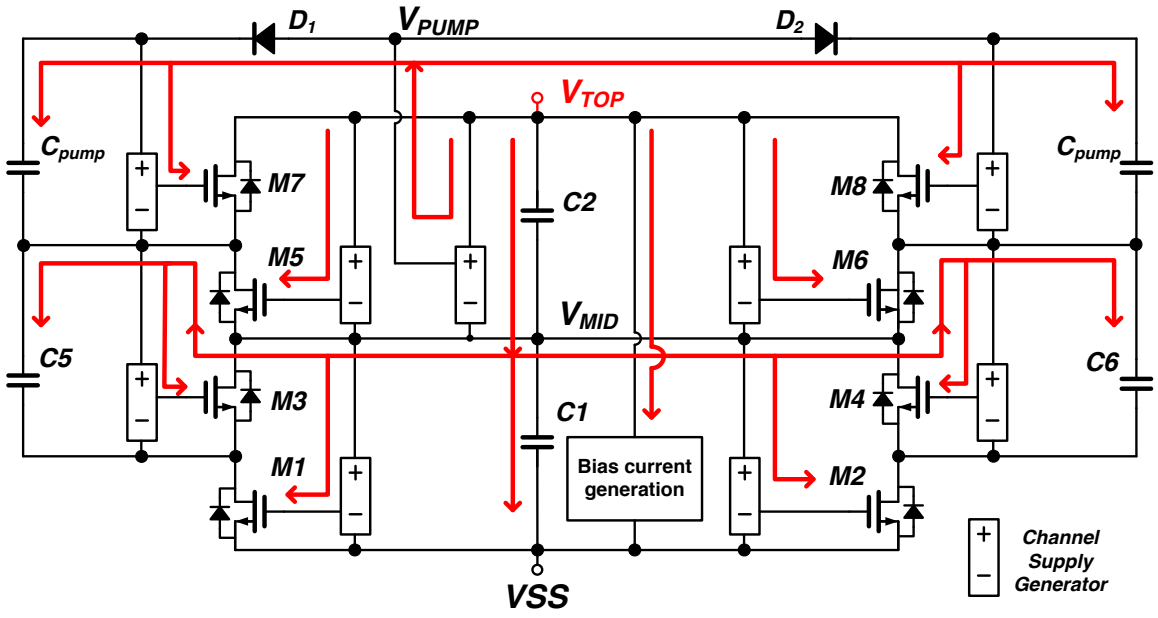


Figure 2.18: Charge flow in the start-up phase of the converter.

To speed up the transition of the differential pair, a positive feedback loop is added to the level shifter. V_A and V_B are down-shifted with another differential pair to the low voltage domain and are compared with Clk and Clk_b. In the transition interval, Clk and Clk_b will switch first and become opposite in phase to the down-shifted signals. Once the difference is detected, a large current I_{PULSE} will be injected into the differential pair to speed up the flipping of the output signals. I_{PULSE} is only injected during the transition interval and a small bias current I_{BIAS} is left in the rest of the time to keep the operation point, which is more energy efficient.

2.3.4.3 Converter Start-Up

The HSCR DC-DC converter can self start-up. As shown in Fig. 2.18, the charge flow during the start-up phase is marked with the red arrows. DC capacitors C_1 and C_2 are charged up once the input voltage V_{TOP} rises. The bias current generator is connected directly to the input node TOP and provides a 5 V supply voltage for the digital blocks. It also generates the bias current for all the channel-supply generators and level shifters. C_5 and C_6 are charged from node V_{MID} through the reverse diodes in the NLDMOS transistors

M_5 and M_6. The charge pump capacitors C_{PUMP} are charged by the charge-pump-supply generator, which converts $(V_{TOP} - V_{MID})$ to V_{PUMP}. As shown in 2.17(a), each channel-supply generator has a reference current path through a Zener diode across its DC input. In the start-up phase, the channel-supply generators stack in series and create a reference current path from V_{TOP} to V_{SS}. This guarantees that all the channel supply voltages can be generated during the start-up phase. The current path is also a resistive divider that sets the value of V_{MID}. In order to protect the transistors from the unbalanced voltage drop across the DC capacitors, V_{TOP} should be ramped up with the clock signal applied.

2.4 Experimental Results

2.4.1 Measurement Setup

The HSCR DC-DC converter IC is fabricated in an Analog-Bipolar-CMOS-DMOS (ABCD) process with maximum 120 V voltage tolerance on silicon. The die shown in Fig. 2.19 measures 14.1 mm^2, which includes the eight main switch channels, the bias generation circuitry, the delay compensation block, and all the other supporting digital circuits. The converter is packaged in a 40-pin Leadless Leadframe Package (LLP) for testing. Fig. 2.20 shows the test board of a two-chip-stacking HSCR DC-DC converter driving a string of 12 1W white LEDs. The test board is implemented with a 2-layer PCB and requires an input clock signal around 1 MHz to convert the input DC voltage to the specified output current. LED dimming is achieved by using a PWM control signal to gate the clock signal before it enters the test board. The digital configuration bits are manually set by jumper switches. Discrete 1 μF ceramic capacitors are used as the DC and flying capacitors in the SC ladder. The HSCR converter test board uses a split-wound coupled inductor with the total differential inductance 6.7 μH and two 10 nF 3 kV capacitors as the L-C resonant tank. Isolation capacitors with higher voltage ratings can be used based on the safety standards. The inductor is built from Micrometal's T50-6 iron powder toroidal core, with a height of 0.5 cm and an outer diameter of 1.3 cm. The discrete components used to implement the two-chip-stacking HSCR DC-DC converter is summaried in Table 2.1.

Fig. 2.21 shows the differential output voltage of a single stage of the switched-capacitor

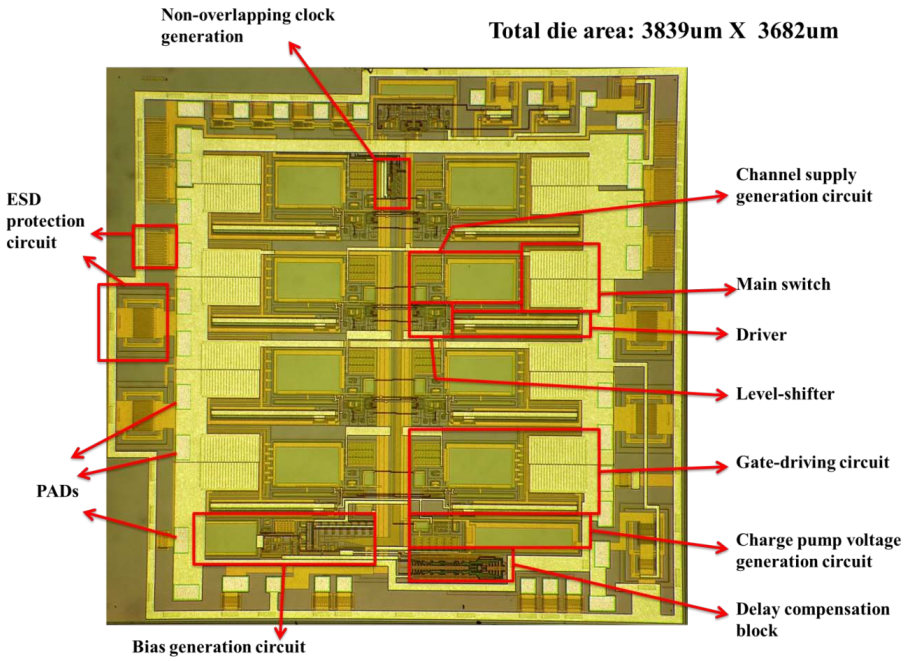


Figure 2.19: SC converter die photo.

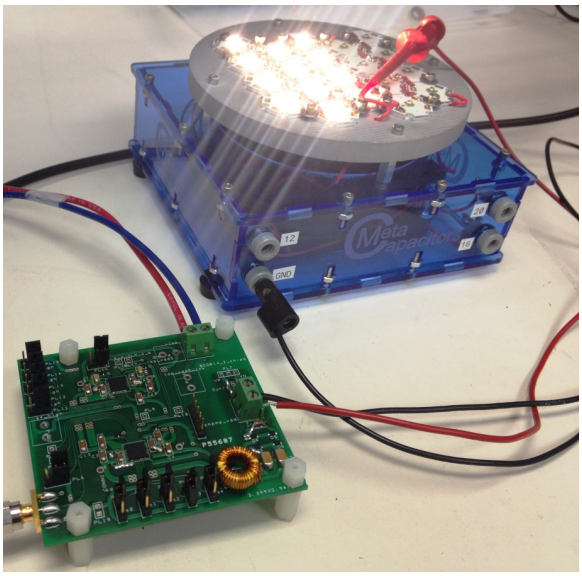


Figure 2.20: The two-chip-stacking DC/DC converter for LED driver.

Table 2.1: Components Used in Prototype DC-DC converter for LED Driver.

COMPONENT	Symbol in Fig. 3	MPN	DESC.	QTY
DC capacitor	C1 ~ C10	C3216X7R	1 µF, 50 V	10
Isolation capacitor	C_T	2220HC	10 nF, 3 kV	2
Resonant inductor	L_T	T50-6	26 AWG, 6.7 µH	1
Rectifier diode		PD3S160-7	60v, 1A	4

ladder, which is the voltage of node A and Ab in Fig. 2.3. Zero voltage switching is achieved since the voltage transition across the parasitic C_{ds} of switch transistors finishes within the 25 ns non-overlapping period of the two-phase gate-drive signals. The voltage of the flying nodes on one side of the balanced switched-capacitor ladder (node A, B, C, D in Fig. 2.3) is shown in Fig. 2.22. The peak voltage stress on the switch transistor is around 45V. The well aligned gate drive signals on chip, and between chips, enables the nearly ideally aligned waveforms of the flying nodes. Fig. 2.23 shows the output voltage across the LED string and the differential voltage of nodes A and Ab in Fig. 2.3 when the LEDs are dimmed. The start-up time of the output LEDs is 17 μs and shut-down time is about 60 μs.

2.4.2 Converter Performance with Different L-C Output Stages

Two prototypes of the two-chip-stacking HSCR converter have been realized with single-level and multi-level L-C output stages respectively. Measurements of their power efficiencies are carried out over an input voltage variation from 160 V_{DC} to 180 V_{DC}. The output currents are regulated to constant values by controlling the switching frequencies. The targeted current levels are set to show the maximum efficiencies of the converters. The measured efficiencies and switching frequencies are depicted in Fig. 2.24. With the single-level L-C stage, the converter's efficiency varies between 85.6% and 90% for a 372 mA output current. The switching frequency is tuned from 870 kHz to 1.14 MHz. The prototype with multi-level L-C stage achieves higher efficiency between 91.5% to 92.2% while delivering a larger output current of 485 mA. As is discussed in Section 2.2.3, with limited capacitance in the SC ladder, the multi-level L-C stage allows us to lower the switching frequency of the SC ladder from around 1 MHz to between 300 kHz and 400 kHz. The improved efficiency of the multi-level resonant topology is the result of the minimized capacitive charge sharing load and loss, as well as lowered gate-drive power consumption. To validate equation 2.11,

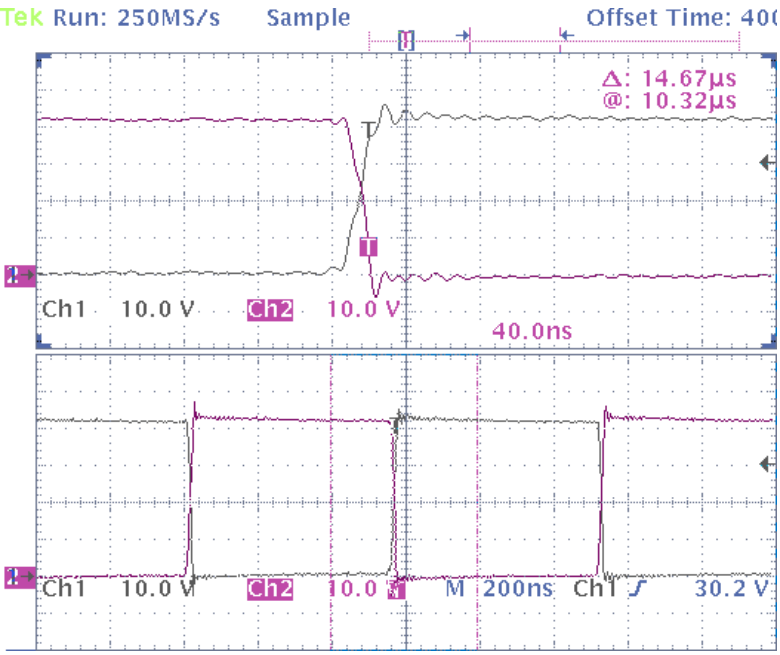


Figure 2.21: Voltage waveforms of the differential output nodes of the switched-capacitor ladder (nodes A and Ab in Fig. 2.3). The waveform on top (Ch1) is a zoomed view of the switching edge of the signals.

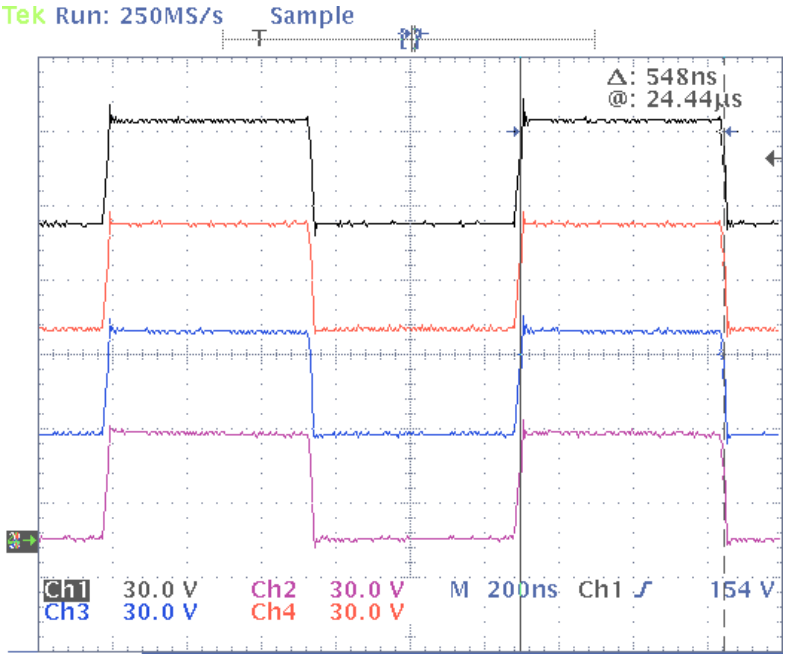


Figure 2.22: Voltage waveforms the flying nodes on one side of the switched-capacitor ladder (nodes A, B, C, D in Fig. 2.3).

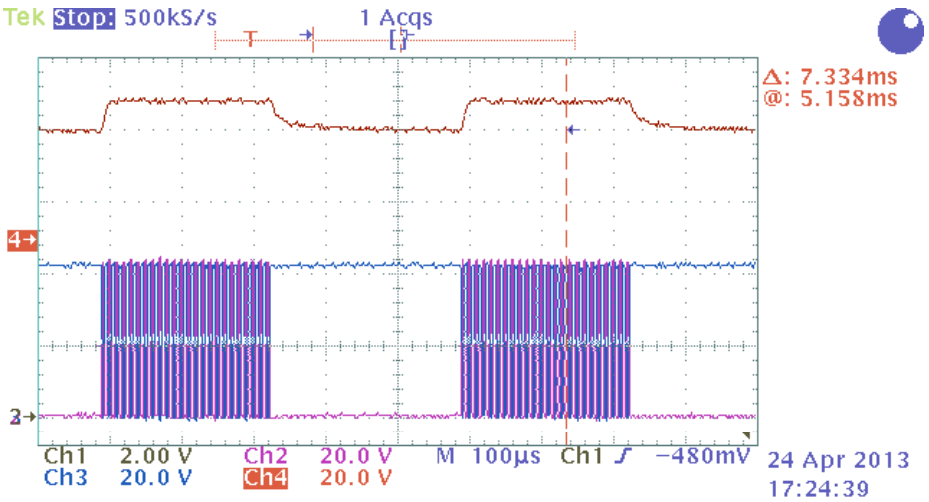


Figure 2.23: Voltage across the LED string during dimming (upper waveform) and the voltage of the differential output nodes A and Ab in Fig. 2.3 (lower waveform).

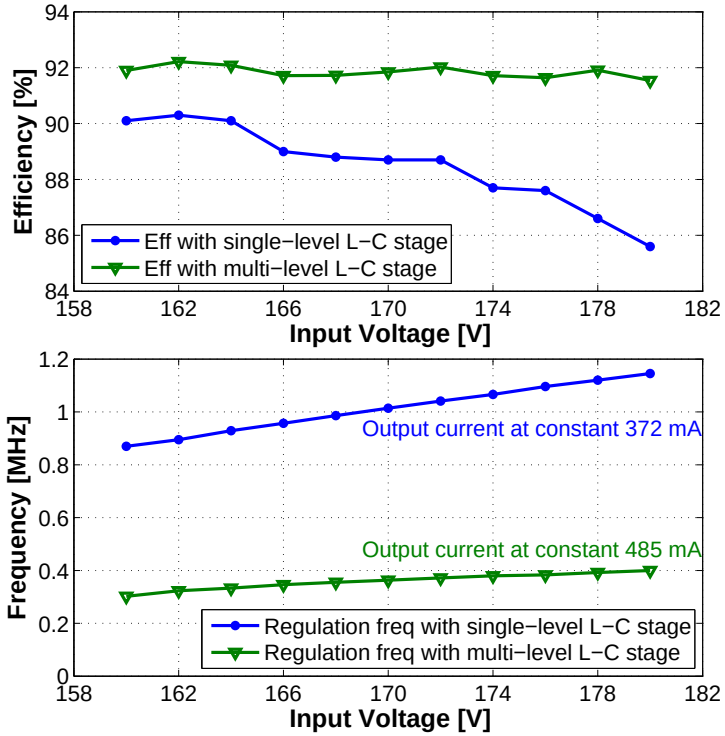


Figure 2.24: Measured switching frequencies, output currents, and efficiencies versus input voltage variation of proposed LED driver with single-level and multi-level output L-C stages connected.

we plotted the calculated versus measured efficiency of the HSCR converter with multi-level L-C stage in Fig. 2.25. The two results matches closely.

Fig. 2.26 shows the dimming performance of the converter with single-level and multi-level L-C output stages. With duty cycle control of the PWM dimming signal, the converter's output power can be dimmed from 100% to as low as 3%. When the dimming ratio is higher than 10%, the power efficiency is kept above 70% with the single-level L-C stage. 2% to 3% improvement in efficiency can be observed with the multi-level L-C stage.

2.4.3 Four-chip-stacking DC-DC Converter

As discussed in Section 2.1 the proposed DC-DC converter IC can be stacked to interface with a range of input voltage levels. A four-chip-stacking converter with the multi-level L-C output network has been implemented and measured for applications with around 240 V_{AC}

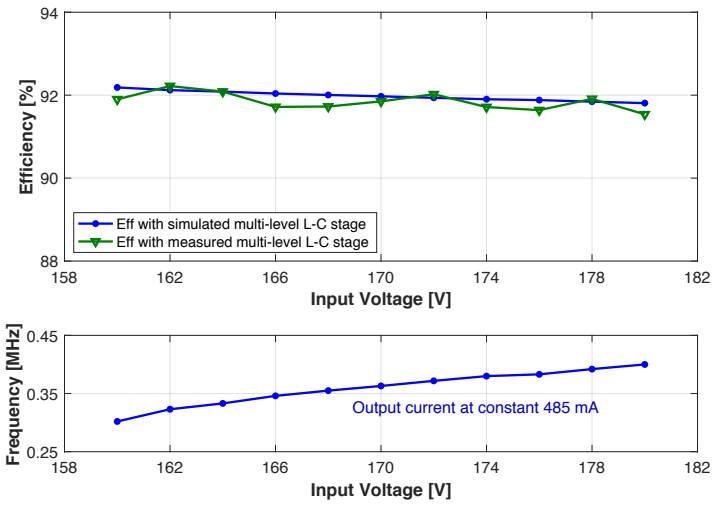


Figure 2.25: Theoretically calculated and measured efficiencies versus input voltage variation of the proposed LED driver with multi-level output L-C stages.

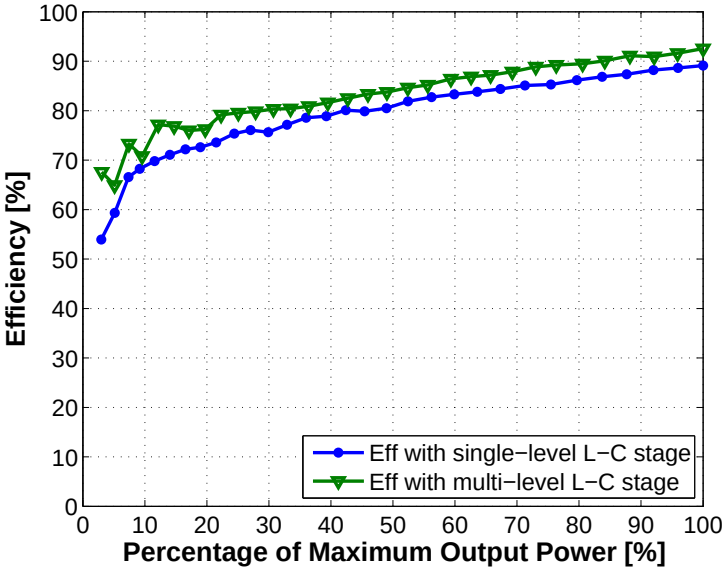


Figure 2.26: Measured efficiency versus dimmed output power of proposed LED driver with single-level and multi-level output L-C stages connected. The input voltage is 170 V_{DC}.

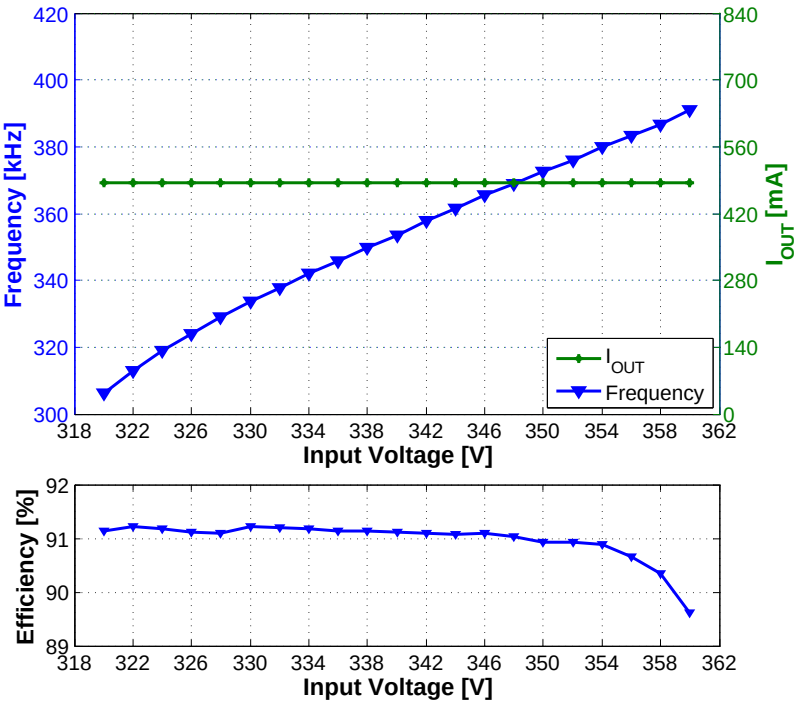


Figure 2.27: Measured switching frequency, output current, and efficiency versus input voltage variation of proposed LED driver with rectified 240V AC (340V DC) input.

(recitified $339V_{DC}$) input voltage. Fig. 2.27 shows the efficiency and current regulation performance of the converter with an input voltage range from 320 V_{DC} to 360 V_{DC}. The conversion efficiency stays above 89.6% when the current is regulated to be constant at 485 mA by tuning the switching frequency from 306 kHz to 391 kHz. The output power can be dimmed to 27.3% with $> 75\%$ efficiency, as is shown in Fig. 2.28. Based on (2.11), the transistor width, nW, has an optimized value for maximum efficiency. However, as we change the conversion ratio n of the SC ladder by stacking different number of chips, the switch transistor width W cannot be modified after fabrication. Since the circuit is optimized for the two-chip-stacking converter operation by design, the efficiency of the four-chip-stacking LED driver is slightly lower.

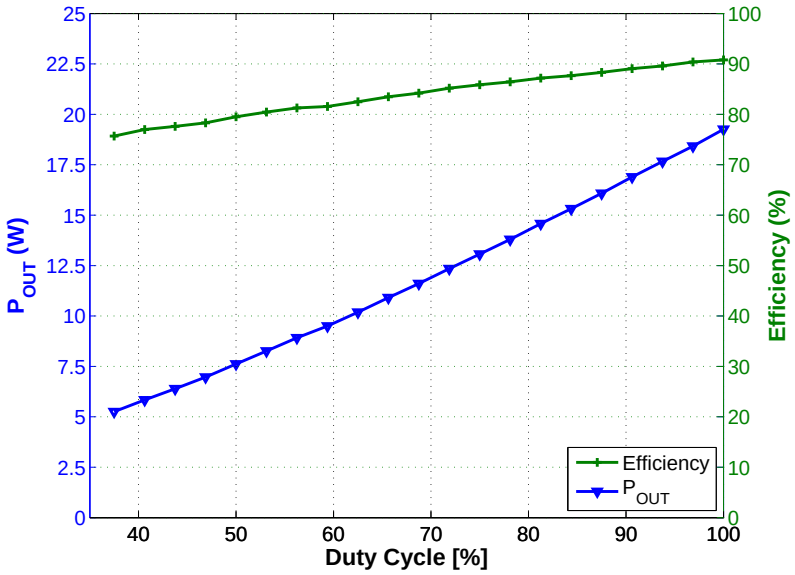


Figure 2.28: Measured output power and efficiency versus dimming duty cycle of proposed LED driver with rectified 240V AC (340V DC) input.

2.4.4 Performance Comparison

A comparison of this work with six other state-of-the-art LED drivers is given in Table 2.2. The performance of this work is based on the prototypes with multi-level L-C output networks. The table shows the proposed LED driver achieves higher efficiency compared with the designs in [17], [18], [29], [30], [31], much wider input voltage range than the designs in [29], [30], [31], and can achieve much higher input voltage level than [32]. This work provides a wide output power and dimming ranges as well. Compared with the higher voltage designs in [17], [18], and [32], the proposed design has smaller magnetic component size while providing certain degree of isolation protection. With silicon technologies that allow higher frequency operation, the size of the isolation capacitance in the resonant stage can be further reduced, resulting in larger common-mode impedance for galvanic isolation. Further more, the proposed IC can be conveniently stacked for various input voltage levels or connected in parallel for heavier output load.

Table 2.2: Comparison to State-of-the-Art LED Driver Designs

	ISSCC_12 [14]	ISSCC_11 [15]	JSSC_16 [17]	JSSC_18 [16]	ISSCC_11 [2]	JSSC_12 [3]	This Work
Converter Topology	Buck-Boost (DC-DC)	Buck-Boost (DC-DC)	Synchronous Inverted Buck (DC-DC)	Quasi-Resonant Inverted Buck (AC-DC)	Buck-Boost (AC-DC)	Flyback (AC-DC)	Hybrid_Switched-Capacitor-Resonant (DC-DC)
Technology	0.18μm CMOS	0.5μm CMOS	0.5μm 120V CMOS	Off-chip 600V GaN FETs & 0.35μm 120V CMOS	0.5μm 500V BCDMOS	0.35 um BCDMOS + 800V off-chip MOSFET	2.5μm 100V BCDMOS
Input Voltage Range (V)	**2.7 - 5.5**	**3-5.5**	**5 - 115**	**100 - 120 V_{AC}**	**50 - 320 V_{AC} or 450V_{DC}**	**180 - 260 V_{AC}**	**80 - 90, 160 - 180, 240 - 270, 320 - 360**
Output Current (A)	0.1 - 2	0.6 - 1.2	± 6.2% of 0.35	~ 0.5	~ 0.2	~ 0.36	0.485
Output Power (W)	0.5 - 10	~ 2.2 - 4.3	< 25	20 - 25	2.5 - 7	6 - 12	1.1 - 22
Efficiency vs Vin Range	80% - 91%	78% - 90.7%, 60% - 86%	77% to 94.4%	Peak 91.4% at 100V_{AC}	peak 86% at 110V_{AC}, peak 89% at 220V_{AC}	Peak 85.2% at 220V_{AC}	91% - 92.2% (160V - 180V), 89.6% - 91.2% (320V - 360V)
Switching Frequency (MHz)	2.5	1 - 2	< 2.2	1.7 - 5.7	0.086	2	0.3 - 0.4
Isolation	No	No	No	No	No	Yes	Yes
PFC Included	No	No	No	Yes	Yes	Yes	No
Magnetic Component for Peak Efficiency (uH)	**1**	**2.2**	**39**	**6.6**	**5500**	**2143**	**20**
Dimming Method	Amplitude	Amplitude	PWM	No	No	Firing angle controlled TRIAC dimming	PWM
Dimming Range (%)	5% - 100%	50% - 100%	10% - 100%	N/A	N/A	20% - 100 %	7.4% - 100%
Active Area (mm^2)	4.125	5	9.4	3.3	3.132	0.76	14.1

2.5 Metacapacitors for LED Drivers

2.5.1 Introduction of Metacapacitor

As discussed in 2.1, capacitors in general has a substantially higher energy and power density than magnetics. Typical surface mount capacitors can easily have an energy density three orders of magnitude larger than that of shielded inductors [22]. Thus developing low cost and high energy density capacitors are crucial for performance improvement of power conversion and delivery systems in applications such as LED driver. As a cross-functional effort, a multi-university consortium group was formed combining expertise in material science and electrical engineering to develop high energy density Metacapacitor and high efficiency LED drivers [33].

The proposed Metacapacitors are innovative printable thin-film capacitors with nanocomposite dielectric suitable for LED light bulb heat conditions [34]. It's designed based on high-dielectric nanocrystals, that can be prepared using high-throughput micro-fabrication/nanotechnology techniques, ink deposition and multilayering. The capacitor dielectric, a nanocomposite composed of (Ba, Sr)TiO3 nanocrystals in polyfurfuryl alcohol (BST/PFA, > 20, 100Hz–1 MHz, loss < 0.01, 20 kHz), targets a high volumetric capacitance density and ripple current capability. The dielectric is demonstrated to function in a finished capacitor > 1000 h at

125°C. A cost competitive analysis to compare the Metacapacitor concept with existing commercial off-the-shelf (COTS) capacitors and deep trench capacitors are shown in table 2.3, based on calculations and specifications from commercially available data. Note that the observation of "infinite" lifetimes is a theoretical argument, based on the potential for using thermodynamically stable inorganic structures.

Table 2.3: Table showing comparative analysis of the Metacapacitor technology and current technological alternatives.

Capacitor type	Energy density per area (μJ/mm²)	Energy density per volume (μJ/mm³)	f_{max} (MHz)	Power density per area (W/mm²)	Power density per volume (W/mm³)	Footprint area, 10 μF @ 50 V (mm²)	Cost, 10 x 1 μF @ 50 V	Operating lifetime	Package form factor	Suitable for 15 W LED driver in 1 cm³
Metacapacitors (projected)	12.5	625	10	125	6260	1000	$0.5	Infinite	PSiP/ PwrSOC	Yes
Deep trench	21.1	469	10	211	4690	154	>$7.00 (lower bound)	Infinite	PwrSOC	Yes
X7R MLCC	252	126	2	504	252	49.6	$2	Infinite	PSiP	Yes
Metallized polymer film	28.5	6.3	2	57	12.7	438	$6.6	Infinite	Non-integrated	No
Tantalum electrolytic	65	26	0.03	2	0.8	192	$5.3	50k hours	Non-integrated	No
Aluminum electrolytic	139	26	0.03	4.2	0.8	90	$0.68	10k-25k hours	Non-integrated	No

2.5.2 Integration of Metacapacitors and the HSCR LED Driver

The idea of integrating the low cost Metacapacitors with the proposed HSCR LED driver has been demonstrated in prototypes. The 2:1 HSCR modular SC IC can be integrated with the printed thin-film Metacapacitors on PCB or directly on flexible substrates. In Fig. 2.29, two printed Metacapacitors are connected to a low-voltage commercial converter IC on a flexible substrate and successfully illuminate five LEDs. In another setup as shown in Fig. 2.30, a single-chip 2:1 HSCR LED driver integrates two 100 nF Metacapacitors on a test board and can drive a string of up to 12 LEDs with 90% peak efficiency. The Metacapacitors are first mounted to two connectors using conductive paste, and then, soldered to the PCB. The above demos were built through multi-university collaboration, with nanocomposite

fabricated by Barry Van Tassel from City College of New York, thin-film capacitors printed and integrated on to flexible or PCB substrate by Shyuan Yang from Columbia University, and driver IC together with driving board developed and performance evaluated by the author, Chengrui Le from Columbia University.

2.5.3 Measurement results

Detailed performance of the single-stack LED driver is measured. Fig. 2.31 shows the measured peak efficiency of the converter with the input voltage varying from $10V_{DC} to 85V_{DC}$. In normal operation, the printed Metacapacitors need to withstand half of the input dc voltage. Thus, the maximum operation voltage of the Metacapacitors in the measurement is $42.5V_{DC}$. As predicted the peak efficiency of the LED driver goes up as the input voltage and output power rise, since the gate drive power loss of the converter is constant, and the intrinsic power loss of the SC ladder increases slower than the output power level. A comparison of the measured efficiency of the LED driver using all ceramic capacitors versus replacing two of the capacitors with printed Metacapacitors is shown in Fig. 2.32. As can be seen from the figure, the efficiency with Metacapacitor is slightly lower, where the efficiency difference is around 1%. The loss is due to the higher series parasitic resistance of Metacapacitor's printed terminals, and the extra connectors. The parasitics can be reduced by increasing the thickness of the capacitor terminals and plates, and directly integrating the LED driver on flexible substrates, as shown in Fig. 2.30.

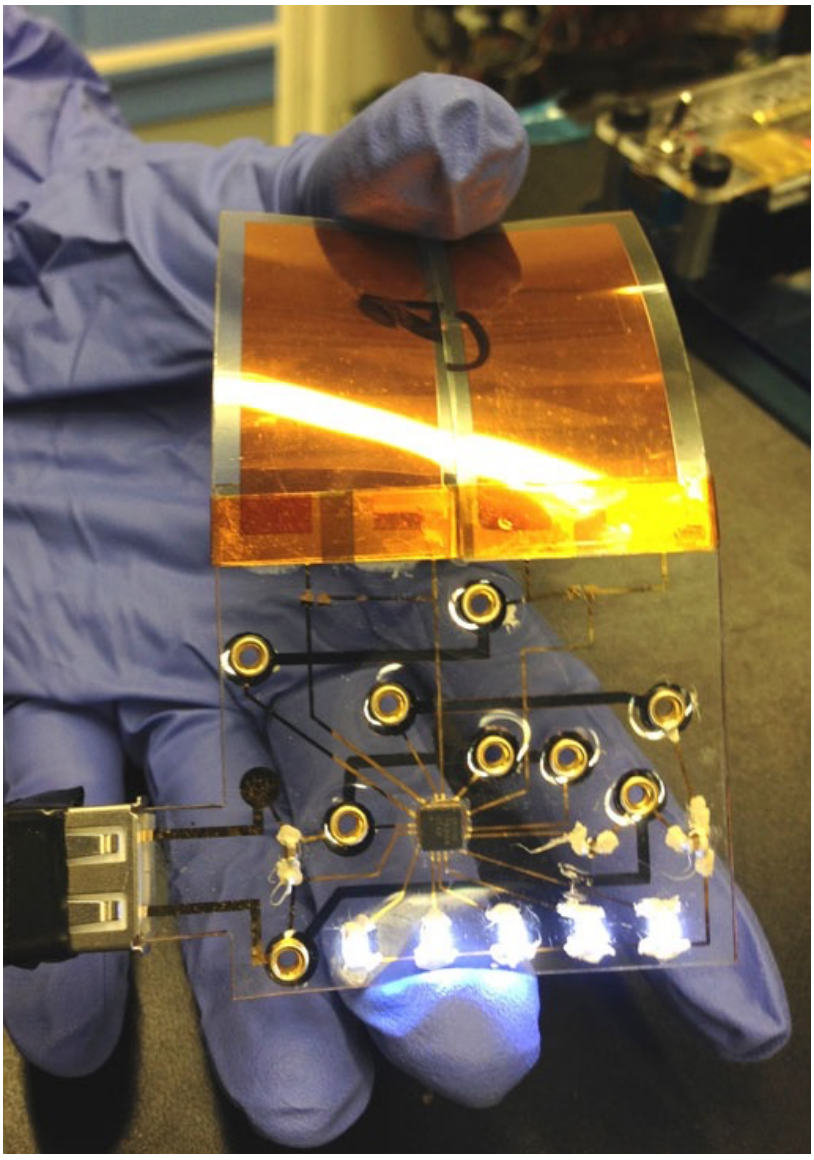


Figure 2.29: Two printed thin-film Metacapacitors integrated with a commercial converter IC on a flexible substrate.

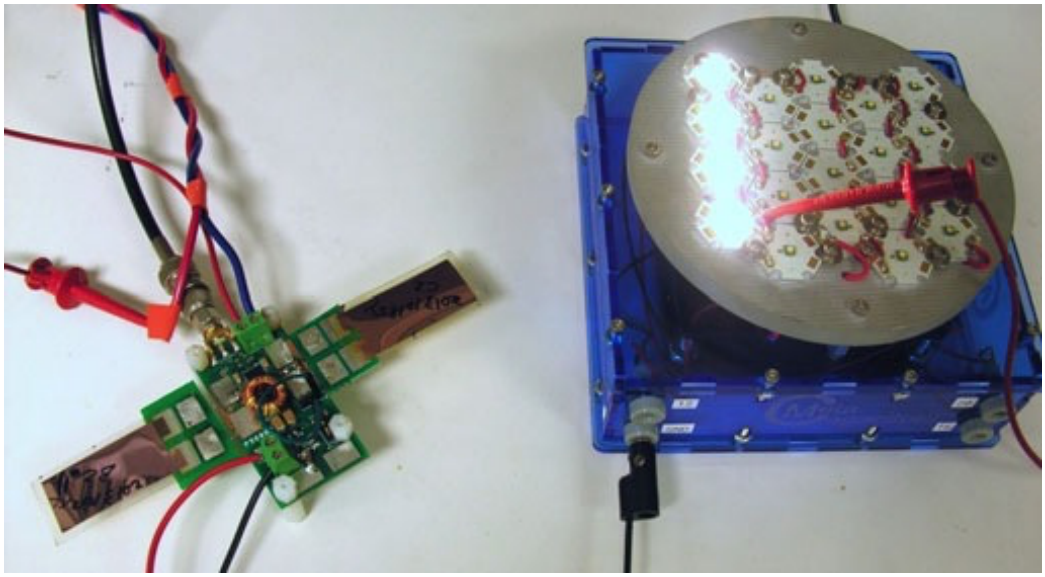


Figure 2.30: Single-stack HSCR LED driver integrated with two printed Metacapacitors driving a series of LEDs.

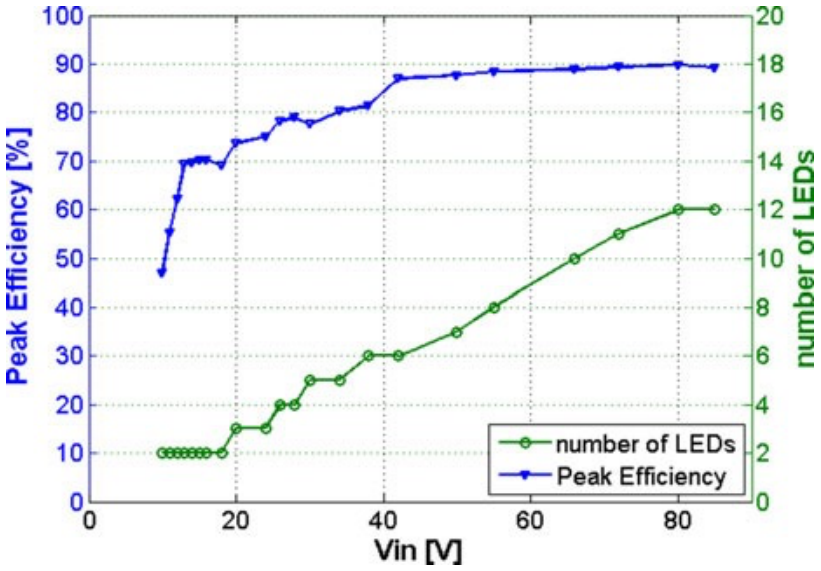


Figure 2.31: Peak efficiency of the LED driver with input voltage and load variation.

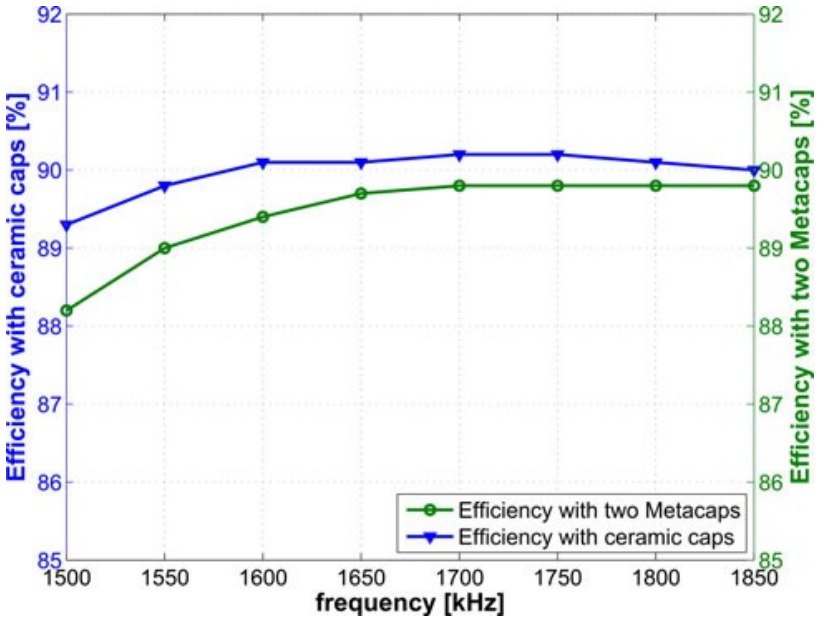


Figure 2.32: Measured efficiency of the 2:1 HSCR LED driver using two Metacapacitors versus using all ceramic capacitors.

2.6 Conclusions

This chapter presents a stackable Switched-Capacitor (SC) DC-DC converter IC for a hybrid-SC-resonant (HSCR) LED driver, and demonstrated an innovative printable low cost thin-film Metacapacitor technology, which can be board integrated to the HSCR LED driver. The HSCR topology combines the advantages of the SC converter and the series-resonant converter, achieving an optimized use of reactive elements and switches. By developing a chip-stackable integrated SC module and a multi-level L-C resonant output network, the converter can be reconfigured and extended to handle a wide range of input voltage levels with relatively constant efficiency, while requiring only a IC process that is rated for a half or a quarter of the input voltage. The HSCR converter also offers nearly lossless regulation and dimming functionality with small reactive components. The L-C stage further has the potential to serve as a galvanic isolation barrier for safety concerns. The converter prototype achieves $> 91\%$ efficiency while delivering up to 22 W to an LED string for inputs from 160 V_{DC} to 180 V_{DC} and $> 89\%$ efficiency for inputs from 320 V_{DC} to 360 V_{DC}. This

sets it apart as one of the highest power SC converters with an IC power train compared to the current state of the art.

Chapter 3

Power Factor Correction and Ripple Canceling AC-DC Rectifier Design

3.1 Introduction

As mentioned in 2.2.1, the HSCR off-line LED driver requires a rectifier front end to convert AC main voltage into stable DC voltage and interface with the HSCR DC-DC converter. In this chapter, we are going to address two additional requirements of high quality LED drivers, which are the power factor correction and LED luminance flicker compensation. The work shown in this chapter are collaborative effort between Daniel Gerber from Professor Seth Sanders' team in UC Berkeley and the author, Chengrui Le from Professor Peter Kinget's group in Columbia University. Chengrui serves as the lead in IC architecture and simulation while Daniel focus more on the PFC and flicker compensation algorithm and control loop. Daniel also designed the test board, measured the circuit performance, and debugged the IC voltage breakdown issue.

3.1.1 Power Factor Correction

As mentioned in 1.3.1.4, in an electric power system, a load with lower power factor draws more current compared with a load with a high power factor given the same amount of useful power transferred. This leads to more power lost and heat generation due to the extra current flow through the resistance of the power distribution network. Thus electrical utilities usually charge a higher cost to industrial or commercial customers where there is a low power factor.

Power-factor correction increases the load's power factor, thus improves efficiency of the power delivery system. while the linear loads with low power factor can be corrected with a passive network of capacitors or inductors, non-linear loads, such as rectifiers, requires active or passive power factor correction may be used to counteract the distortion it creates and improve the power factor. Fig. 3.1 (a) shows a non-PFC AC-DC converter, where a large filter capacitor Co is placed directly after bridge rectifier to supply a DC voltage to the load. Since most of the time the rectifier diodes are reversed biased and will not conduct, the input current waveform from the line is consisted of short pulses only when the instantaneous input voltage exceeds the voltage across the capacitor, as depicted in Fig. 3.1 (b). In order to control the input current to be sinusoidal and in phase with the AC main voltage over the entire AC cycle, an inductor can be placed in series with the capacitor as a passive PFC method. However, typically this only corrects the PF to 0.7 to 0.85 range. In most cases, active PFC methods are required to achieve the specifications of applicable standards, such as EN61000-3-2. Fig. 3.2 shows a conceptual schematic of an active PFC buck converter. By switching the power transistor at a much higher frequency than the AC main frequency, the current through the inductor can be synthesized to be in phase with the input voltage.

3.1.2 Flicker Mitigation

As mentioned in 1.3.1.5, previous reports suggest luminance flicker with certain frequency spectrum has potential adverse biological effects on human health [13]. The study on human eye temporal sensitivity shows the average human observer has peak flicker sensitivity

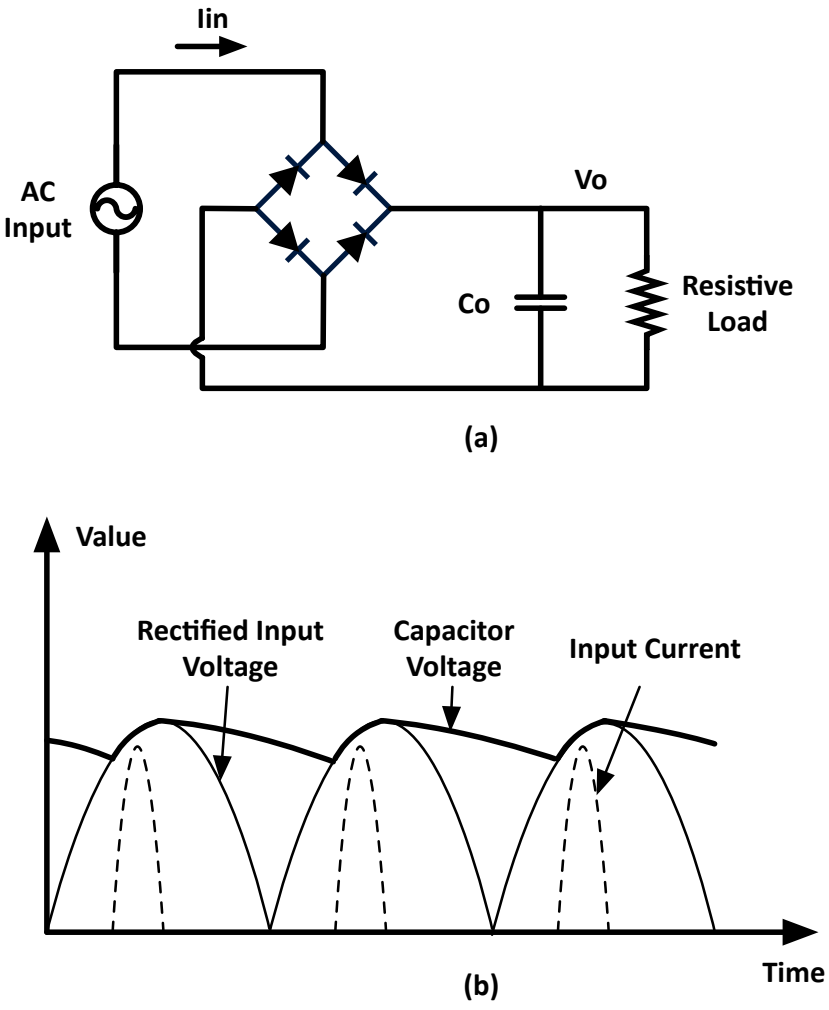


Figure 3.1: Conceptual schematic of (a) a non-PFC AC-DC converter and (b) its voltage and current waveforms.

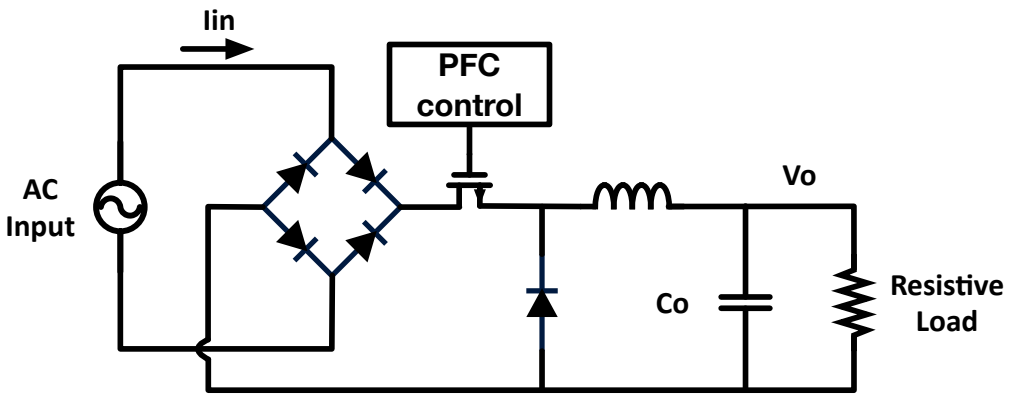


Figure 3.2: Conceptual schematic of a active PFC AC-DC buck converter.

between 10Hz to 15Hz range and can consciously detect up to 90 Hz luminance variation . About 1 in 4000 individuals is recognized as having photosensitive epilepsy. For such individuals, immediate health risk exists for as short as a few seconds' exposure to luminance flicker with frequency spectrum between 3Hz to 70Hz. Luckily, the 60 Hz AC main input voltage of LEDs is usually first rectified, doubling the frequency to between 100Hz and 120Hz, which is invisible to human eye. However, researchers suspect the long-term exposure to such invisible luminance flicker below 165 Hz could result in health risks including, but not limit to, headaches, migraines, impaired ocular motor control, and impaired visual performance.

Compared with LED lighting, incandescent lamps are naturally resistant to flicker because incandescence is a thermal process with a relatively slow time constant. After the introduction of the fluorescent lamp, flicker was discovered to be an issue [13]. Magnetically-ballasted fluorescent, metal halide, and high pressure sodium lamps can produce double line frequency flicker in light output. This was later mitigated by alternating sources on a 3-phase electrical system, or by applying the high-frequency electronic ballasts. Now the flicker concern is rising for the LED lighting devices [35]. As an example, the output voltage Vo in Fig. 3.2 has double line-frequency component and so is the output load current. Thus it's important for LED drivers to mitigate the low frequency current ripple that flows into the load LEDs.

As discussed in Section 3.1.1, a LED driver operates with close to unity power factor

with the appropriate PFC method applied. This means the input current of the LED driver is sinusoidal and in phase with the line voltage. Assume the line voltage is $V_{in}sin(\omega_0 t)$ and the input current is $I_{in}sin(\omega_0 t)$, the input power can be written as:

$$\begin{aligned} P_{in} = V_{in}sin(\omega_0 t) \cdot I_{in}sin(\omega_0 t) &= \frac{VI}{2} - \frac{VI}{2}cos(2\omega_0 t) \\ &= P_{LED} - P_{ripple} \end{aligned}, \tag{3.1}$$

where P_{LED} is the constant DC power to LEDs and P_{ripple} is the AC power that needs to be filtered out by energy storage components. Fig. 3.3 (a) shows a traditional passive ripple canceling (RC) LED driver concept diagram. In order to low-pass filter the ripple power at around 100Hz to 120Hz frequency, it requires a large DC capacitor or capacitor bank. Such a large size capacitance often is implemented with electrolytic capacitors, which is more cost effective compared with ceramic capacitors for applications that require high capacitance and voltage rating. However, the electrolytic capacitors are bulky and have a relatively short life span, which for certain higher temperature applications can be as short as five years. Other disadvantages of electrolytic capacitors include the increasing equivalent series resistance (ESR) while it's aging and safety risk of explosion due to short circuit or hydrogen build-up.

In order to remove the problematic electrolytic capacitors, multiple active ripple cancellation circuit topologies has been developed [36; 37; 38]. Fig. 3.3 (b) shows an active ripple cancellation converter is added to the LED driver to convert and store the ripple power P_{ripple} onto a energy storage capacitor C_{RC}. C_{RC} here can be much smaller than C_{DC} in a passive RC LED driver as shown in Fig. 3.3 (a). To explain this, we can define a number α as the ratio of tolerable voltage ripple magnitude across the LED load versus the DC output voltage V_{LED}. Thus the peak to peak voltage swing of C_{DC} is $2\alpha V_{LED}$. The ripple energy that can be stored in C_{DC} is given by

$$P_{ripple} = \frac{1}{2}C_{DC}V_{max}^2 - \frac{1}{2}C_{DC}V_{min}^2 = 2\alpha C_{DC}V_{LED}^2. \tag{3.2}$$

As comparison, the voltage swing of the active ripple cancellation capacitor C_{RC} can be chosen to be much larger, for example, across the whole output voltage range from $0V$ to V_{LED}. Thus the ripple energy that can stored by C_{RC} is given as

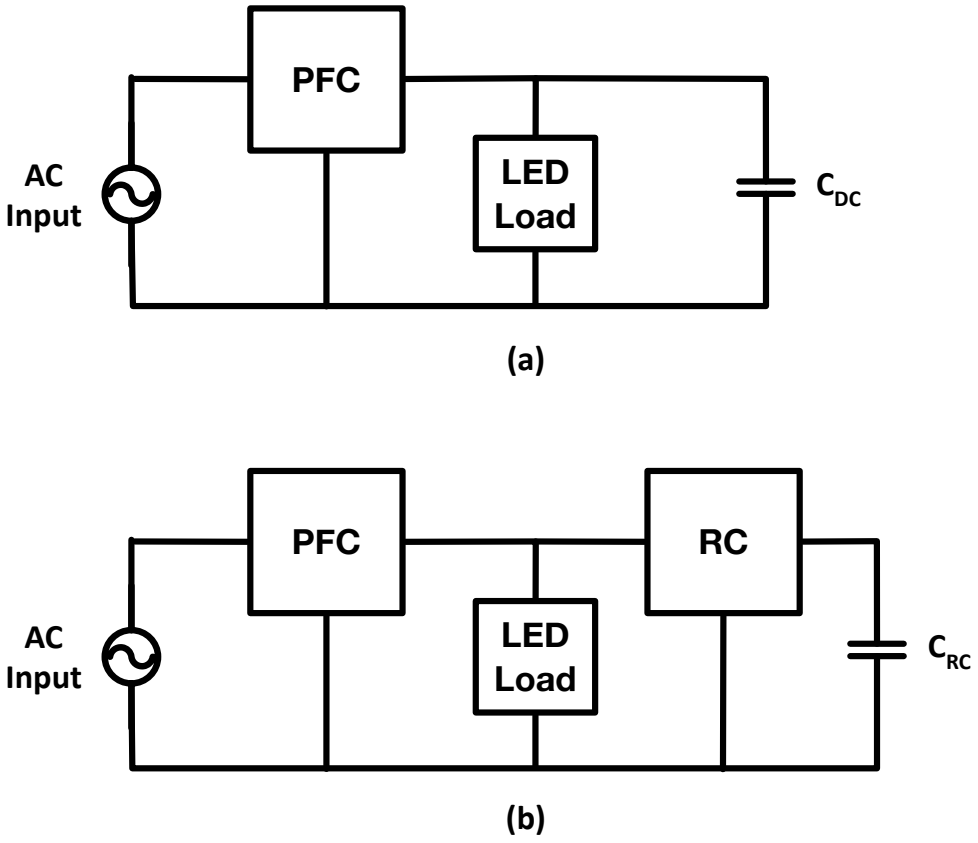


Figure 3.3: Conceptual diagram of (a) the passive ripple canceling method with large capacitor C_{DC} and (b) an active ripple canceling method involving a separate ripple canceling (RC) converter and a much smaller capacitor C_{RC}.

$$P_{ripple} = \frac{1}{2}C_{RC}V_{max}^2 - \frac{1}{2}C_{RC}V_{min}^2 = \frac{1}{2}C_{RC}V_{LED}^2. \tag{3.3}$$

Given a fixed amount of ripple power that needs to be canceled P_{ripple}, the ratio of capacitance needed for the active ripple cancellation versus the passive method can be expressed as

$$C_{RC} : C_{DC} = 4\alpha. \tag{3.4}$$

If $\alpha = 1\%$, the energy storage capacitor C_{RC} with active ripple cancellation can be 25 times smaller than C_{DC} in the discussed example.

3.2 Multi-Level Switched-Capacitor PFC and Ripple Canceling Rectifier

3.2.1 Full System Architecture

The full system in Fig. 3.4 contains an input power factor correction (PFC) rectifier, a ripple cancellation circuit, a DC capacitor bus, and an output stage. The PFC rectifier converts the AC line voltage to DC with low harmonic current injection, and provides for current regulation and dimming. The ripple cancellation circuit cancels ripple on the DC capacitor bus. Finally, the output stage down-converts the DC bus voltage and uses a small transformer to provide for galvanic isolation.

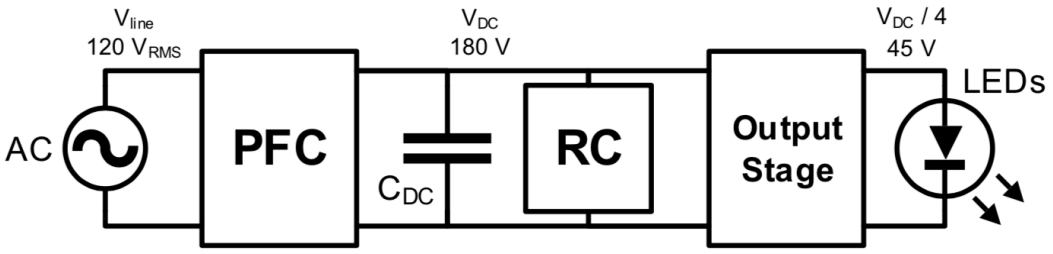


Figure 3.4: Block diagram of the multilevel converter with power factor correction (PFC), ripple cancellation (RC), and output stage.

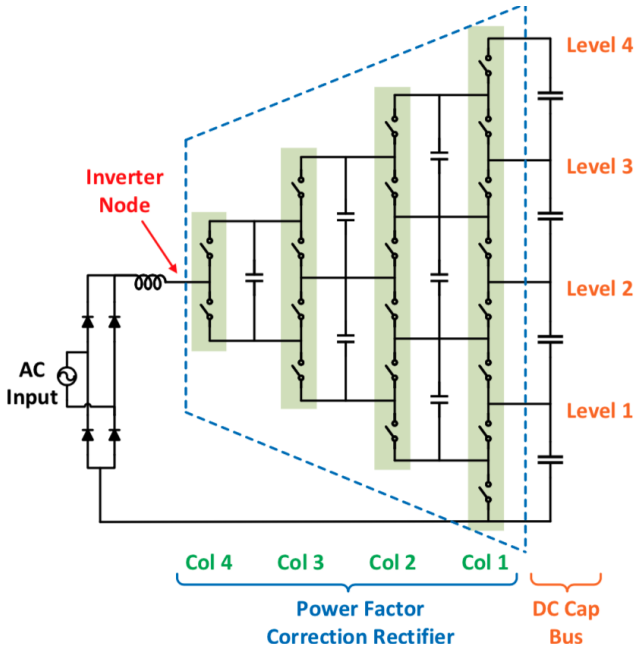
3.2.2 Multilevel Topology for PFC and Ripple Cancellation Module

The power factor correction (PFC) rectifier and ripple cancellation module use a generalized multilevel topology, as shown in Fig. 3.5. Each switching column contains transistors that switch synchronously and alternate in complementary pairs. By switching the various columns high or low, the inverter node can be connected to any of the five DC levels. Each column connects to a set of smaller integrated flying capacitors, which assist in rapidly stabilizing the column voltages and serve as a supply for the gate drivers. This topology is bidirectional, allowing the circuit to be configured as a rectifier or inverter for PFC and ripple cancellation respectively. It can also self-balance the DC capacitor bus such that the voltages across the DC capacitors are equal [39].

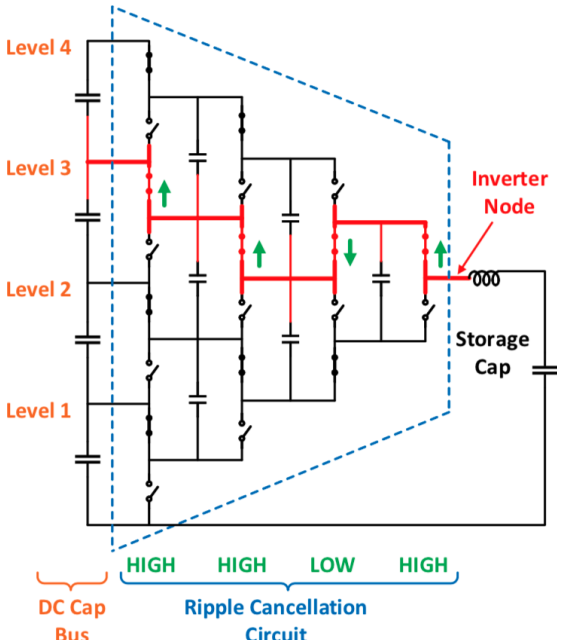
The power factor correction (PFC) rectifier functions to enforce unity power factor and control the input power. As shown in Fig. 3.5(a), the PFC rectifier can control the voltage at the inverter node. In this way, the PFC rectifier can set the voltage across the input inductor, and thus control the input current. Fine control over the input current enables harmonic reduction and allows for dimming via current control.

A 60 Hz input current in phase with a 60 Hz input voltage will generate 120 Hz input power. If this power ripple is not canceled from the DC bus, the LEDs will flicker at 120 Hz. Passive ripple cancellation is possible with large electrolytic capacitors on the DC bus. However, the use of electrolytics will increase the size and decrease the life span of the LED driver.

The ripple cancellation module functions to actively cancel ripple from the DC capacitor bus, thus greatly reducing the required DC capacitor size and obviating the need for electrolytics. As shown in Fig. 3.5(b), the ripple cancellation circuit is able to transfer energy from the DC capacitor bus to the storage capacitor by precisely swinging the storage capacitor voltage.



(a)



(b)

Figure 3.5: Generalized multilevel schematic for the PFC rectifier and ripple cancellation module. The DC capacitor bus creates the DC levels, buffers power flow, and connects to the output stage (not shown here). (a) PFC with switching columns highlighted in green. (b) Ripple cancellation module with an example switch configuration for connecting the inverter node to level 3.

3.3 Sigma Delta Control

3.3.1 Introduction of the Sigma Delta Control Loop

The multilevel converters in the power factor correction (PFC) and ripple cancellation modules are controlled via sigma delta modulation. In this context, the multilevel converter behaves like a quantizer since it can only set the inverter node to one of several quantized levels. Like any quantizer, the multilevel converter produces quantization noise. Sigma delta modulation invokes closed loop control to push the quantization noise to higher frequencies, after which it can easily be filtered out [40]. Intuitively, the output of the sigma delta modulator will attempt to best approximate the input.

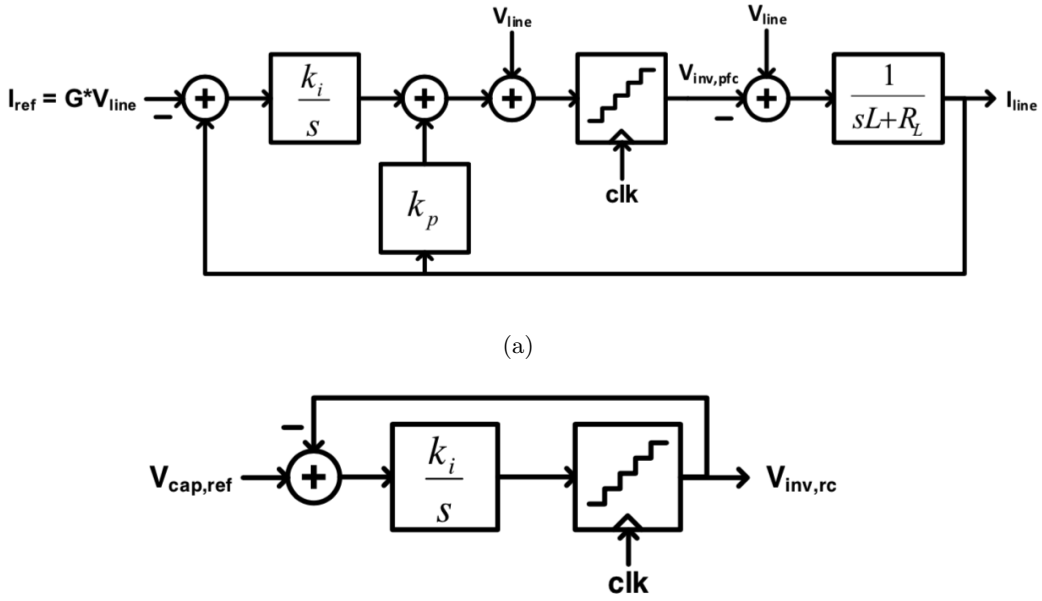
As a control scheme, sigma delta modulation has the distinct advantage of simplicity. Fig. 3.6(b) suggests that a simple first-order sigma delta control loop could be implemented with a single integrating op-amp. Sigma delta modulation also has the advantages of closed-loop robustness and stability, assuming that the loop is properly designed. Finally, the quantization behavior of the multilevel converter causes sigma delta modulation to simply be the natural and most convenient control scheme. PWM is rather difficult and complicated for multilevel converters because a triangle wave must be generated between each level. Techniques such as space vector modulation, and selective harmonic elimination all require complicated (and often digital) control.

3.3.2 Control for the PFC Rectifier

The power factor correction (PFC) rectifier uses a second order sigma delta loop to set the line current to best approximate a reference current waveform. As shown in Fig. 3.6(a), the reference waveform is nominally sinusoidal and in-phase with the line voltage. Sigma delta control is especially useful because its ability to shape quantization noise is necessary for meeting the line current harmonic specs.

The control loop design in Fig. 3.6(a) allows for the adjustment of the integral gain k_i and the proportional gain k_p. It is often reasonable to set

$$K \quad = \quad (k_i/f_s)(\Delta/\delta) = 1$$



(a)

(b)

Figure 3.6: The sigma delta control loops for the PFC rectifier and ripple cancellation module. Each loop has an integrator and a quantizer clocked at 400 kHz. (a) Second order sigma delta loop used for the PFC rectifier, where the second pole is obtained from the input inductor. The input current I_{line} relates to the voltage across the inductor $V_{inv,pfc} - V_{line}$. (b) First order sigma delta loop used for the ripple cancellation module. This module uses the sigma delta loop to set the inverter node of the ripple cancellation circuit $V_{inv,rc}$ to approximate a preprogrammed waveform $V_{cap,ref}$.

where the quantizer is clocked at frequency f_s, and its quantization levels step by Δ at the output and δ at the input [41; 42]. If $K >> 1$, the quantizer may attempt to switch by more than one level at a time. If $K << 1$, the quantizer output may experience dead zones in which it does not switch when it should. After f_s and k_i are selected, k_p can be chosen to help shape the quantization noise curve.

3.3.3 Control for the Ripple Cancellation Module

The ripple cancellation module uses sigma delta modulation to swing the storage capacitor voltage such that the 120 Hz power ripple is cancelled from the DC bus. The reference

waveform for the storage capacitor voltage is developed by a conservation of energy approach [43]. If the line current $I\sin(\omega_0 t)$ is sinusoidal and in-phase with the line voltage $V\sin(\omega_0 t)$, the power ripple P_{RC} on the DC bus is developed from:

$$\begin{aligned} P_{in} &= V_{line}I_{line} = VI(\frac{1}{2} - \frac{1}{2}\cos(2\omega_0 t)) \\ P_{RC} &= P_{in} - P_{LED} = -\frac{1}{2}VI\cos(2\omega_0 t)). \end{aligned}$$

A functional ripple cancellation module transfers all of the ripple power P_{RC} to the storage capacitor. As such, the ideal voltage waveform $v_{cap,ref}$ on the storage capacitor is derived from its energy E_{RC} as:

$$\begin{aligned} E_{RC}(t) &= \frac{1}{2}C_{RC}v_{cap,ref}^2(t) = \int_{-\infty}^{t} P_{RC}(t) \\ v_{cap,ref}(t) &= \sqrt{-\frac{VI}{2\omega_0 C_{RC}}\sin(2\omega_0 t) + \frac{V_{max}^2 + V_{min}^2}{2}} \end{aligned}$$

for storage capacitance C_{RC}. V_{max} and V_{min} are the maximum and minimum levels that the storage capacitor voltage should be constrained to.

In this work, the ripple cancellation module relies on open-loop control with a look-up table parameterized by dimming level command, eg. power level. Each $v_{cap,ref}$ waveform stored in the look-up table corresponds to one half-period of data. The data is actually the modulation waveform, generated with a system as indicated in Fig. 3.6(b). In practice, the waveform is triggered by the line voltage zero crossing.

3.4 Multi-level Transformer Based Output Stage

As shown in Fig. 3.7, power is provided to the LEDs through the output stage, which consists of an array of stacked H-bridges and an output transformer. The output stage functions as a 4:1 series-parallel step-down circuit, which serves to step the 180V DC capacitor bus voltage down to the 45V LED output. Another function of the output stage is to facilitate in balancing the voltage levels on the DC capacitor bus, which is crucial for correct operation of the power factor correction (PFC) and ripple cancellation modules.

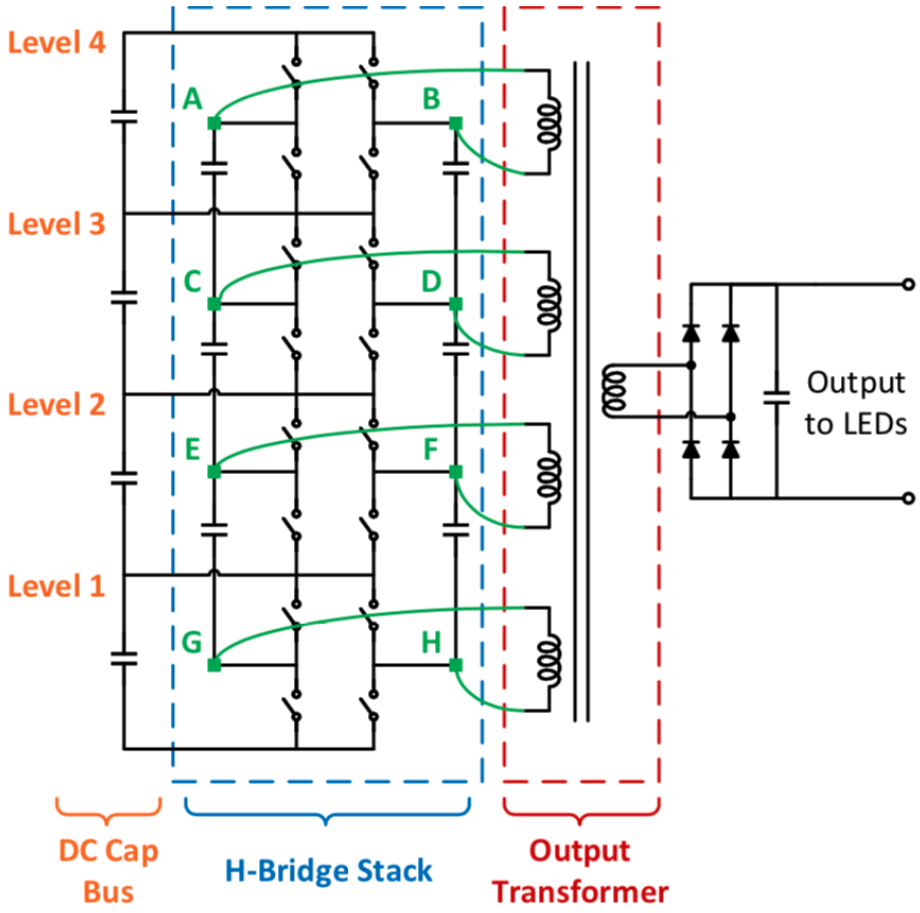


Figure 3.7: The output stage is comprised of an integrated H-bridge stack and an output transformer.

Each of the inverter nodes in the H-bridge stack are connected to a small isolation transformer. This transformer has four primary windings and one secondary, all of which have the same number of turns. The transformer is useful in galvanically isolating the LEDs from the high voltage circuits. In addition, it allows the H-bridge stack to switch at a relatively low frequency of 50 kHz. Finally, the transformer provides soft switching to the H-bridge stack via its leakage and magnetizing inductance. This transformer is not designed to store energy, and so it can be substantially smaller than that of an equivalent flyback converter.

3.5 Experimental Results

3.5.1 Integration and Testing

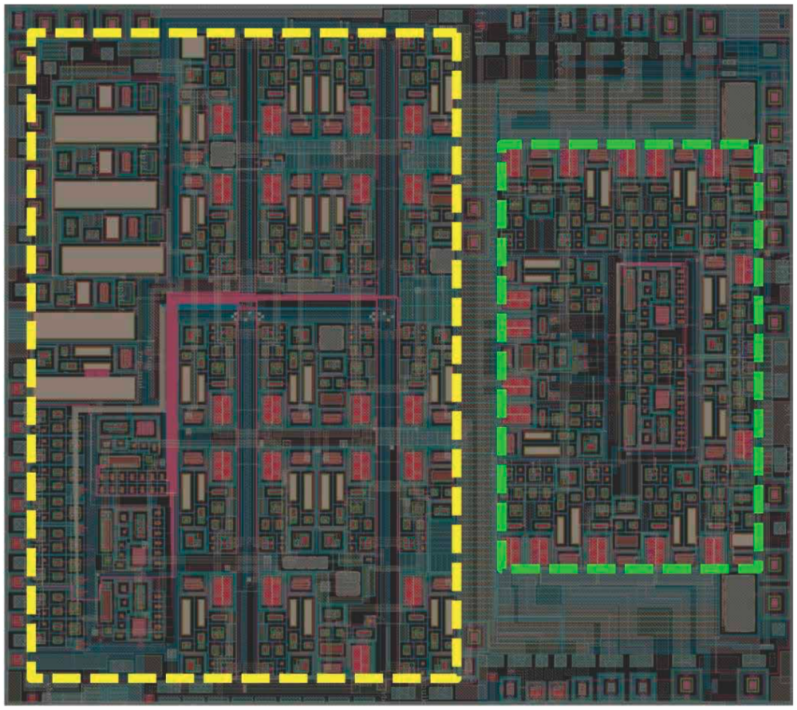


Figure 3.8: The prototype IC layout with dimensions of 7.08mm X 6.28mm. The multilevel converter is on the left (yellow). The H-bridge stack is on the right (green).

The full system from Fig. 3.4 has been simulated, experimentally tested, and verified. A prototype IC, shown in Fig. 3.8, was designed and fabricated on an Analog-Bipolar-CMOS-DMOS (ABCD) high voltage process. The IC contains the circuitry for a multilevel converter and a H-bridge stack. Both circuits use N-type LDMOS transistors as their power switches, and every power switch requires an integrated gate driver.

The design for the chip's gate driver is shown in Fig. 3.9. Each gate driver consists of a high-side channel supply generator, a level shifter, and a driver. The channel supply uses power from a DC or flying capacitor to create a floating 5V supply. Its function is to provide power to the level shifter and the driver. The level shifter is responsible for shifting a low voltage digital signal up to the floating voltage domain. Finally, the driver is an inverter

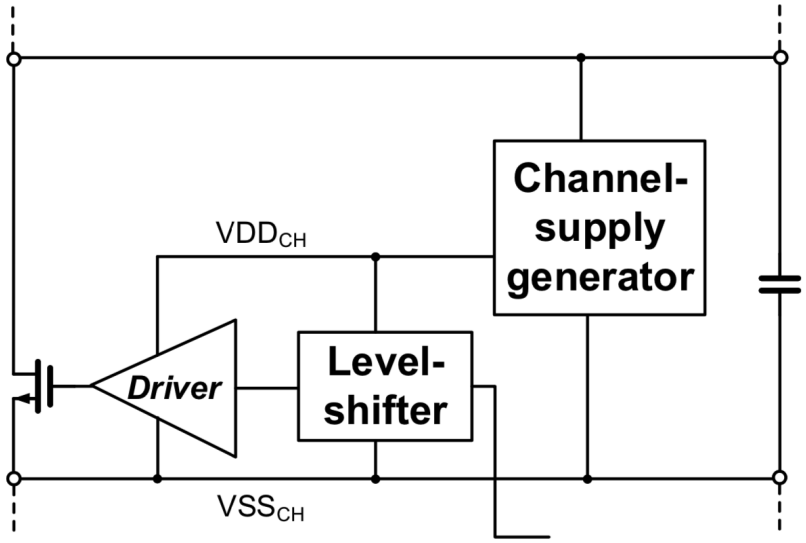


Figure 3.9: Several devices in a switching column of the multilevel converter, with the full gate driving channel shown for the high power DMOS switch M2. Each gate driving channel consists of a high-side channel supply, a level shifter, and a driver (inverter). The channel supply bootstraps off a flying capacitor and generates the CH_VDD voltage at 5V above CH_VSS.

that amplifies the floating digital signal with enough power to drive the gate capacitance of the power switch.

The test board in Fig. 3.10 is implemented on a 2-layer PCB and the system is controlled via off-chip components and a Xilinx Spartan-3 FPGA. These off-chip functions can be readily integrated on a subsequent design turn, and require very small die area. Table 3.1 shows a full list of required external components (not including the pair of multilevel converter chips).

3.5.2 Data and Results

The waveforms in Fig. 3.11 demonstrate functionality. The PLECS simulation waveforms shown in Figs. 3.11(a) and 3.11(b) can be compared to the experimental scope waveforms, shown in Figs. 3.11(c) and 3.11(d). Figs. 3.11(a) and 3.11(c) show that the power factor correction (PFC) rectifier can limit harmonics on line current (green) and ensure that it is in phase with the line voltage (yellow). The PFC inverter node (blue) of the PFC is shown

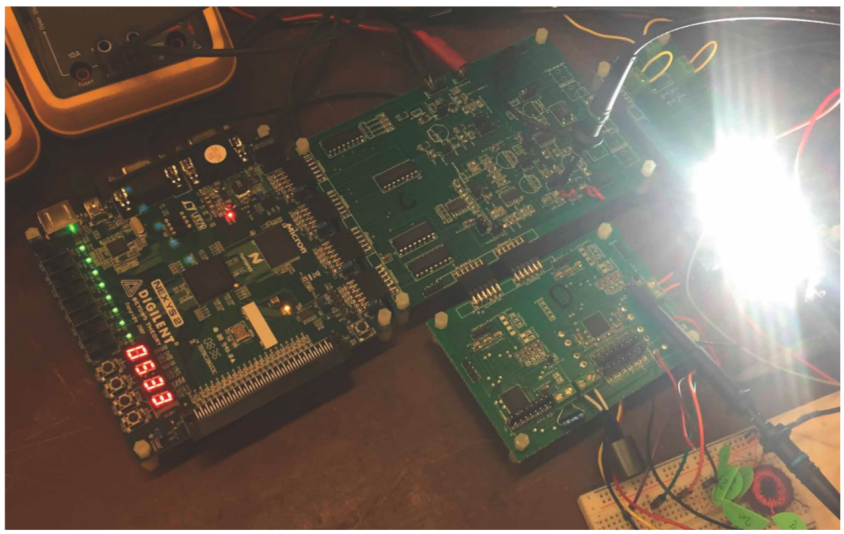


Figure 3.10: Board and lab setup. The power board (lower left of the LEDs) contains two ICs, one for the PFC rectifier and one for the ripple cancellation module. The FPGA board (left) attaches to the control board (top center). All of the control logic can be integrated in CMOS on the IC.

to utilize all four levels. Figs. 3.11(b) and 3.11(d) show that the ripple cancellation module can cancel AC ripple from the DC capacitor bus. Swinging the storage capacitor voltage (purple) allows the DC voltage at level 4 (green) to be almost entirely devoid of ripple. The ripple cancellation module inverter node (blue) only utilizes three of the DC levels, implying that the size of the storage capacitor could be reduced.

Fig. 3.12 shows an FFT of the line current input. Standards such as IEC 61000-3-2 (US) and EN 61000-3-2 (Europe) specify the acceptable limitations on specific line current harmonics [44]. For lighting applications, these standards specify that the fifth harmonic must be less than 10% of the fundamental. In this work, the fifth harmonic is 4.6% of the fundamental. Higher harmonics are required to be less than 3% of the fundamental, and these specifications are also met.

Fig. 3.13 shows how the efficiency varies over input voltage and current. Fig. 3.14 shows a loss analysis comparison between the model and measured data. For the lower input voltages, the modeled loss (multicolored bar) can be compared with the actual measured loss (dark blue bar). The test part did not function at full rated voltage, but was testable

Component	Part Number	Description	Dimensions (mm)	Quantity
PFC Inductor	RFS1317-825KL	8.2 mH 0.25 A	13.3x13.3x16	1
Rip. Canc. Inductor	RFB0810-102L	1 mH 0.35 A	9.5x9.5x11.5	1
Transformer Toroid	C055379A2		18.1x18.1x7.1	1
DC Bus Caps	C3216X7R2A105K160AA	1 uF 100 V	3.2x1.6x1.3	4
Rip. Canc. Storage Cap	SK052E475ZAR	4.7 uF 200 V	12.7x5.1x14.2	1-2
DC-DC Output Bridge	PD3S160-7	60 V	1.9x1.3x0.7	4

Table 3.1: Components used in the prototype LED driver.

to approximately half of rated voltage. The measured losses were well modeled, though slightly higher than predicted in modeling.

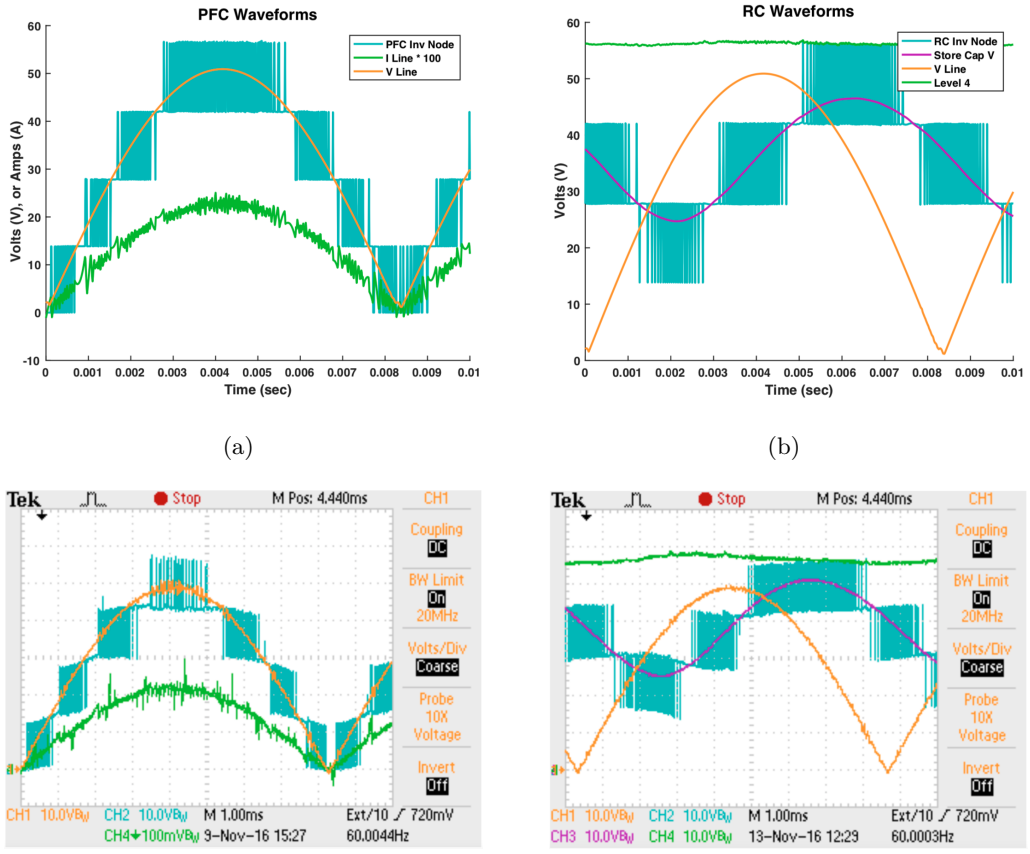


Figure 3.11: Simulated and experimental waveforms that demonstrate the functionality of the power factor correction (PFC) rectifier and ripple cancellation module. (a) Simulated PFC waveforms with the line voltage (yellow), line current (green), and the PFC rectifier inverter node of Fig. 3.5(a) (blue). The line current is scaled by 100 for visibility. (b) Simulated ripple cancellation module waveforms. Waveforms include the line voltage (yellow), the voltage at level 4 of the DC capacitor bus (green), the voltage across the storage capacitor (purple), and the ripple cancellation module inverter node from Fig. 3.5(b) (blue). (c) Experimental PFC rectifier waveforms from oscilloscope. The line current (green) is measured as the voltage across a 1 ohm current sense resistor. (d) Experimental ripple cancellation module waveforms.

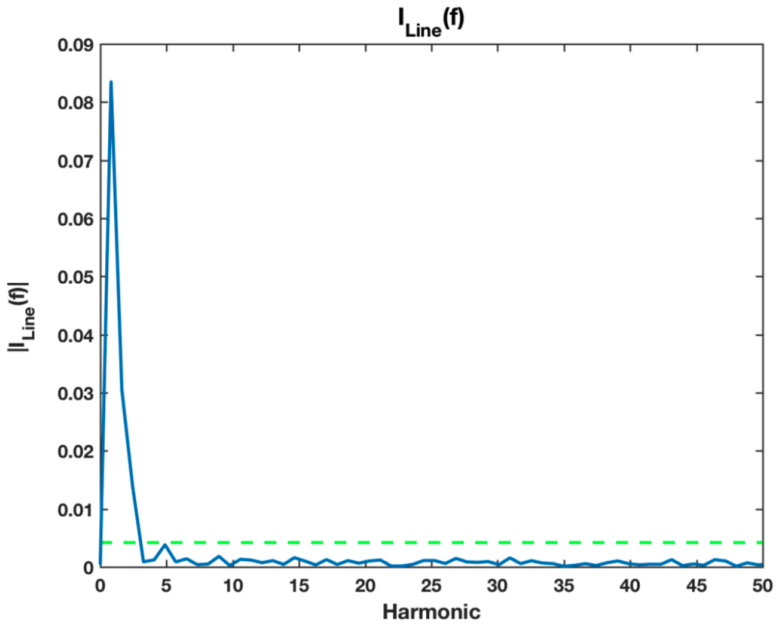


Figure 3.12: FFT of the line current input I_{Line}. Line current harmonics are all less than 5% of the fundamental. Data is obtained at $V_{in,RMS} = 36V$ and $I_{in,RMS} = 68.5mA$.

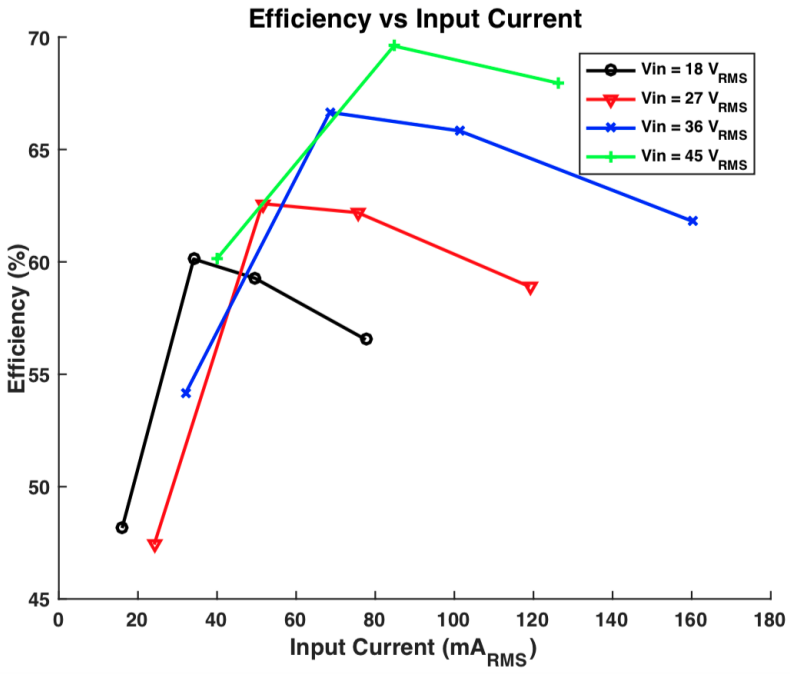


Figure 3.13: Efficiency versus input current. The output voltage was set at the optimal value using an electronic load. In general, the output voltage and current is determined by the total voltage drop of the series LED string.

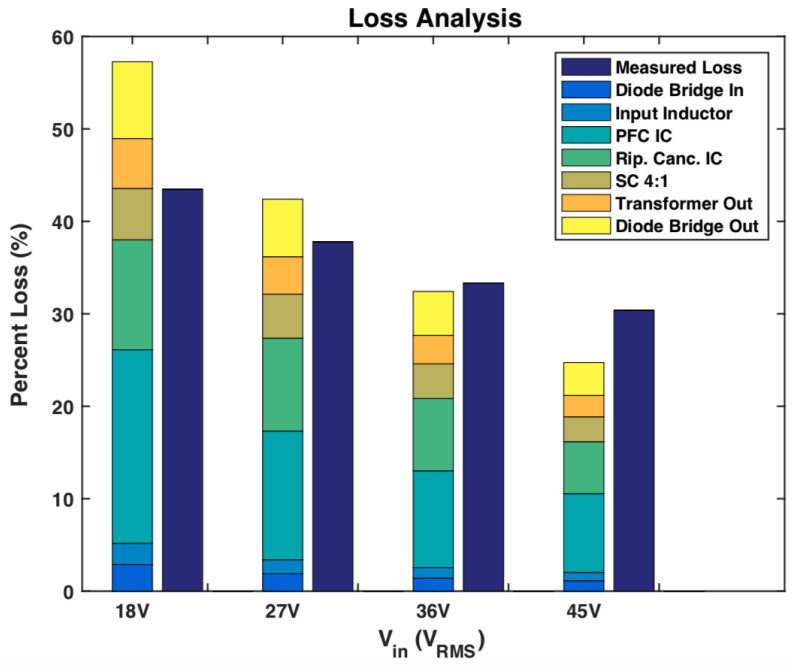


Figure 3.14: Loss versus input voltage. The lower voltages each compare a loss model (left bar) to the actual measured loss (right dark blue bar). Unfortunately, measured loss data doesn't exist for the higher voltages, but the loss model can somewhat provide a projection of how the system would perform. The model and data correspond to operation at close to 80 mA input current.

3.6 Conclusions

This chapter documents the design, fabrication, and testing of an IC LED driver based on a multilevel topology. The multilevel PFC rectifier converts AC to DC, cancels line-current harmonics, and controls the input power. The multilevel RC module swings the voltage on a storage capacitor in order to cancel ripple from the DC capacitor bus. Both modules are controlled via sigma–delta modulation.

While multilevel converters have proven to be practical for high-voltage electronics, this work demonstrates their potential to be practical in the IC space. The multilevel topology was shown to be particularly useful for expanding the capabilities of any IC process that has devices with a relatively low drain– source breakdown voltage ($V_{DS,max}$). With careful and robust design, integrated multilevel converters show great promise for lighting and household electronics.

Chapter 4

Conclusions and Future Works

The LED lighting market has been expanding rapidly for the past two decades and raised new challenges to the LED driver circuit beyond the traditional power converter design: higher energy efficacy, wider input/output range, smaller form factor, lower cost, unity power factor, and minimal luminance flicker. In order to meet the above design targets, this thesis uses a off-line LED driver as the research vehicle, proposed, analyzed and demonstrated a hybrid switched-capacitor-resonant (HSCR) LED driver and a sigma delta controlled multilevel AC main rectifier front end. The summary of each design will be made in Section 4.1 and a few possible directions for extended studies are discussed in Section 4.2.

4.1 Summary of Proposed LED Driver Solutions

In Chapter 2, we discussed the fundamental limiting factors of power converter efficiency and presented a multilevel hybrid-switched-capacitor-resonant (HSCR) DC-DC converter topology which leverages the higher energy density of capacitors and better component performance due to much lower voltage rating of, for example, capacitors, transistors, and inductors. As we know, the energy density of surface mounted capacitors can easily achieve 1000 times of the shielded inductors [14]. The presented HSCR design showed that by reducing the voltage and power rating of the inductors through SC voltage stacking, the required inductor can be greatly decreased. We also presented capacitive galvanic isolation which eliminates the need of bulky transformers. The smaller voltage rating also applies to

other components such as the capacitors and power transistors. The overall performance of transistors considering both on-resistance and gate-capacitance improve non-linearly when the voltage rating is lowered. The ratio of performance improvement is in general higher than the voltage reduction ratio of power transistors with different transistor process. Additionally, the low voltage and low power devices' performance also improves faster given their much wider market applications and thus much higher amount of investment from the industry. After all, it is demonstrated that the benefit of introducing SC topology into LED driver design is significant in terms of efficiency improvement as well as size and cost reduction.

In addition, the proposed topology combines the advantages of the SC converter and the series-resonant converter, optimizing the usage of reactive elements and switches. The zero voltage switching technique is applied to the power train switches to reduce the switching loss benefiting from the small reactive components, while nearly lossless regulation and dimming functionalities are achieved at the same time.

Another innovative technique demonstrated in the proposed LED driver is the modular design of the power train. A stackable SC module IC is developed using a process rated for 120V maximum voltage. By reconfiguration of the module IC and combining with a multi-level L-C resonant network, the converter can handle a wide range of input and output voltage levels with relatively constant efficiency.

Finally, the measurements show the proposed HSCR DC-DC converter for LED driver achieves $> 91\%$ efficiency while delivering up to 22 W to an LED string for inputs from 160 V_{DC} to 180 V_{DC} and $> 89\%$ efficiency for inputs from 320 V_{DC} to 360 V_{DC}. This sets it apart as one of the highest power SC converters with an IC power train compared to the current state of the art.

At the end of Chapter 2, a printable thin-film Metacapacitor with nanocomposite dielectric is introduced as an alternative solution for high energy density capacitor for SC power converters. The Metacapacitor can be prepared using high-throughput microfabrication/nanotechnology techniques, ink deposition and multilayering. A prototype of 2:1 HSCR DC-DC converter integrating the modular SC IC and two Metacapacitors are demonstrated and measured. The tested driver delivers about 15 W at 470 mA to a string

of 12 LEDs with 90% peak efficiency. This result shows a promising future for the Metacapacitor technology.

In Chapter 3, we target the challenges of two other performance requirements of modern LED drivers, which are power factor and luminance flicker harmonics. A multilevel HSCR topology is also applied here to lower the voltage ratings of electrical components, leverage the higher energy density of capacitors, introduce modular design flexibility, and achieve higher overall performance. Both the PFC and line-current ripple cancellation network are controlled by a sigma-delta modulation control loop. The measured input current FFT shows harmonic power meeting IEC 61000-3-2 (US) and EN 61000-3-2 (Europe) standards. The resulted luminous ripple is shown to be reduced to about 2% given an optimized conversion ratio.

4.2 Possible Directions for Future Studies

For the proposed HSCR LED driver, the switching loss of power transistors is a significant contributor of the total power loss and thus limiting the final power efficiency of the LED driver. As the voltage conversion ratio of the multilevel SC DC-DC converter increases, the number of switches also increases and thus causing more switching loss. It is important to improve the efficiency of gate driving circuits of the SC power train. In the proposed HSCR LED driver, the power of the gate driving circuitry of the switches are provided by the DC and flying capacitors, as shown in Fig. 4.1 (a). The channel-supply generator is currently implemented by a linear regulator with relative low power efficiency, as depicted in Fig. 4.1 (b). For future improvement, small size SC DC-DC converters using on chip capacitors could be designed to replace the linear regulators to minimize the switching power loss [22].

In addition, the number of channel supply generator and driver circuits in the SC module IC can be reduced by introducing PMOS power transistors as switches. As shown in Fig. 4.2, the PMOS switch transistor M4 and NMOS switch transistor M6 are driven by the same gate driving circuitry where the gate voltage swings between CH_VDD and CH_VSS. This can reduce the number of gate driving blocks by nearly a half and thus reducing the chip area and cost. The second advantages of the circuit topology shown in Fig. 4.2

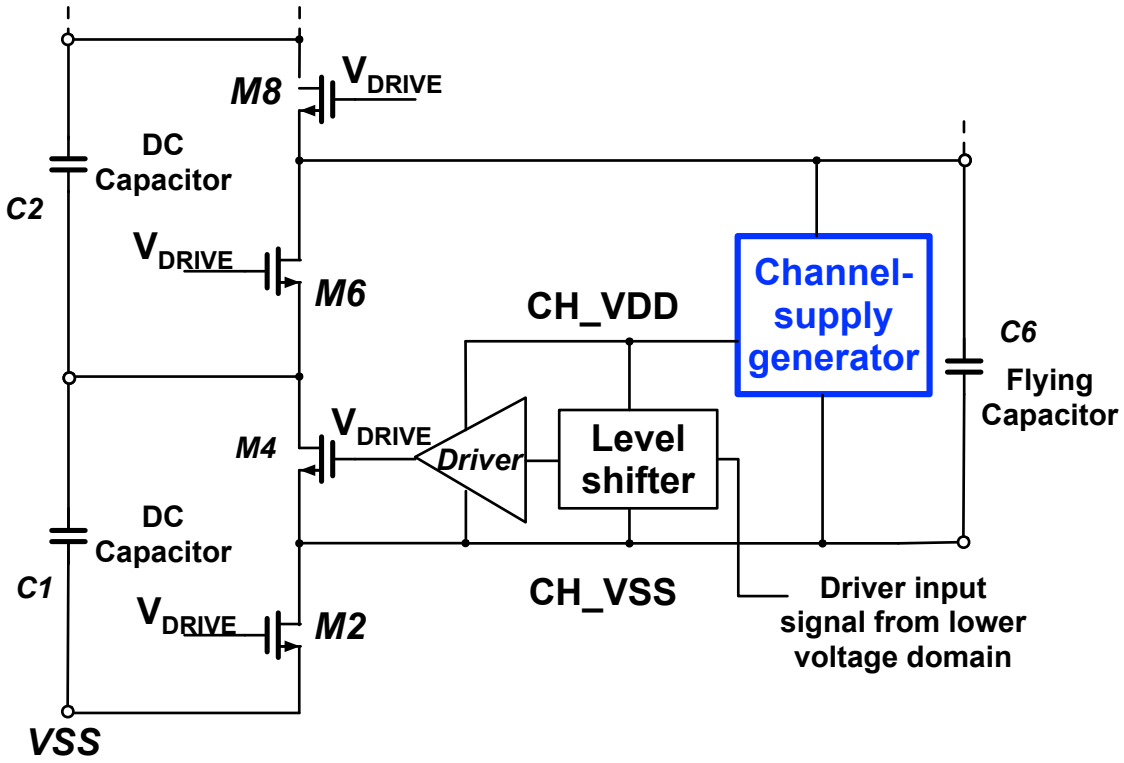


Figure 4.1: (a) Block diagram of the gate driver and (b) schematic of the channel-supply generator.

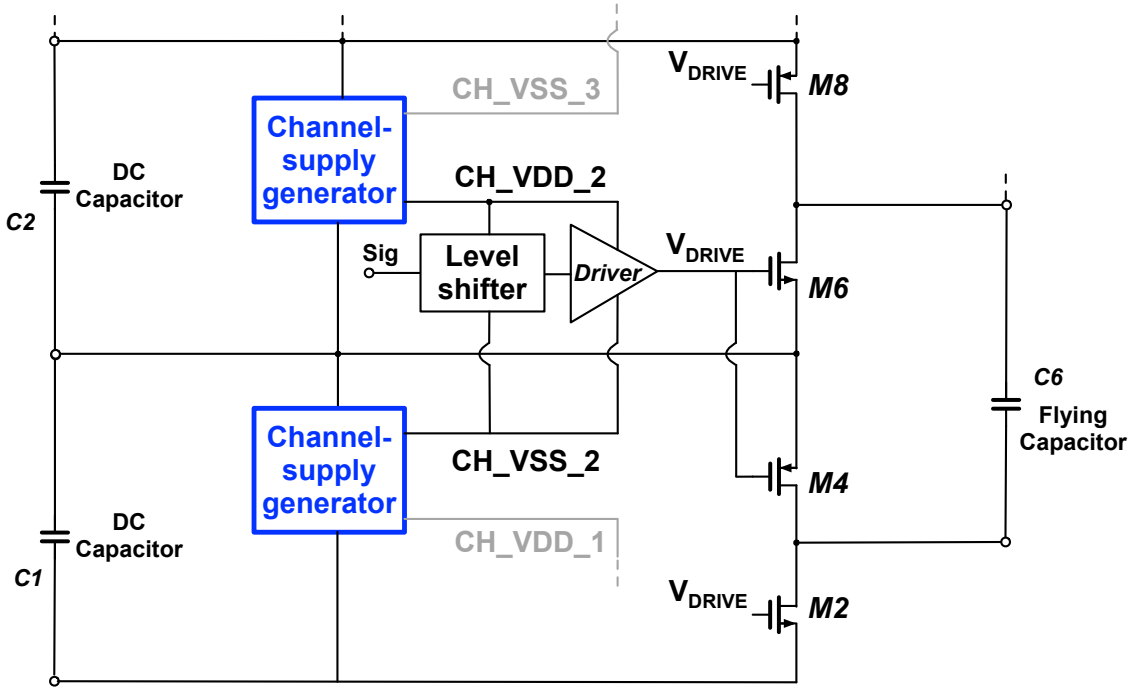


Figure 4.2: Block diagram of shared gate driving circuit for both NMOS and PMOS power transistors.

lies in the fact that each of the channel-supply generator maintains two different voltage supply levels. For example CH_VDD_1 and CH_VSS_2 are both generated by the same channel-supply generator circuit block. In this way, power transistor M1, M2, M3 and M4 shares the same channel-supply generator. Thus the number of channel-supply generators in the HSCR LED driver shown in Fig. 2.3 can be reduced to only four. Given the channel-supply generator has a significant power lost, the overall power efficiency can be improved by generating two voltage supplies from the same current branch and reducing the number of generators. Additionally, by placing the gate drive circuits only on stable DC notes and not flying nodes, the voltage variation of parasitic capacitance in the gate drive circuits are significantly lowered and thus the power lost are reduced. This also increases the overall robustness of the SC power train.

The proposed HSCR DC-DC converter IC module is implemented in an Analog-Bipolar-CMOS-DMOS (ABCD) process. The power switches are LDMOS devices with 120V drain to ground voltage tolerance. The size of the switch transistors are relatively large due to

the fact they need to tolerate a high drain to ground or body voltage even each transistor only needs to stand a fraction of that voltage from source to drain. On the other hand the silicon on insulator (SOI) technology has an advantage for application in SC circuits. The power transistors with floating body in SOI technology can tolerate large drain to body voltage without the need to significantly increase the transistor size. Such advantage of SOI technology can result in lower cost, faster switches, lower on resistance, and lower switching loss.

Another opportunity of cost and size reduction of the proposed LED driver lies in the potential integration of energy storage capacitors on chip. Deep trench capacitors can offer capacitance density of two to three orders higher than the traditional metal-insulator-metal (MIM) and metal-oxide-metal (MOM) on-chip capacitance. The development of high density deep trench capacitors with higher voltage rating and SOI technology could enable the integration of the whole SC power train on chip for LED drivers.

As discussed in Section 3.5, the multilevel PFC rectifier did not function at full rated voltage, but was testable to approximately half of rated voltage. Through failure analysis, it is believed that the chip's functionality issues are caused by the floating channels that sit on flying nodes. Specifically, the channel V_{DD} rail in the switching channel latches below the channel V_{SS} when the flying nodes undergoes drastic voltage swings. Since the SC IC was implemented with a internal testing silicon process before official released by the company, the parasitic capacitance between channel V_{DD} and ground was under estimated. For future design this issue should be mitigated with circuit improvements and carefully validated.

Bibliography

[1] O. V. Losev, "Telegrafiya i Telefoniya bez Provodov," vol. 44, pp. 485–494, 1927.

[2] "IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers," *IEEE Std 1789-2015*, pp. 1–80, June 2015.

[3] "Health effects of artificial light," SCENIHR (Scientific Committee on Emerging and Newly Identified Health Risks), Tech. Rep., March 2012.

[4] "Opinion on Potential risks to human health of Light Emitting Diodes (LEDs)," SCENIHR (Scientific Committee on Emerging and Newly Identified Health Risks), Tech. Rep., June 2018.

[5] A. B. Watson and A. J. Ahumada, "64.3: Flicker Visibility: A Perceptual Metric for Display Flicker," *SID Symposium Digest of Technical Papers*, vol. 42, no. 1, pp. 957–959, 6 2011. [Online]. Available: https://doi.org/10.1889/1.3621499

[6] T. Drummond, "Description of an apparatus for producing intense light, visible at great distances," *Edinburgh Journal of Science*, vol. 5, pp. 319–322, 1826.

[7] G. K. MacIsaac, D. and G. Anderson, "Basic physics of the incandescent lamp (light-bulb)," *Physics Teacher*, vol. 37, 1999.

[8] J. Iveland, L. Martinelli, J. Peretti, J. Speck, and C. Weisbuch, "Direct Measurement of Auger Electrons Emitted from a Semiconductor Light-Emitting Diode under Electrical Injection: Identification of the Dominant Mechanism for Efficiency Droop," *Physical review letters*, vol. 110, p. 177406, 04 2013.

[9] Philip.com, "Lighting world first: Philips breaks 200 lumens per watt barrier," August 2019.

[10] "Lifetime of White LEDs," US Department of Energy, Tech. Rep., March 2012.

[11] Gosund. Smart WiFi LED Light Bulb A19 2700K 800LmL. [Online]. Available: https://www.amazon.com/Multi-Color-Controlled-Compatible-Assistant-Equivalent/dp/B07G2CM96F

[12] K. W. H. R. G. M. DiLaura, D. L. and G. R. Steffy, "The Lighting Handbook, 10th ed." *New York: Illuminating Engineering Society*, 2011.

[13] "IEEE Recommended Practices for Modulating Current in High-Brightness LEDs for Mitigating Health Risks to Viewers," *IEEE Std 1789-2015*, pp. 1–80, June 2015.

[14] V. W.-S. Ng and S. R. Sanders, "Switched Capacitor DC-DC Converter: Superior where the Buck Converter has Dominated," Ph.D. dissertation, EECS Department, University of California, Berkeley, Aug 2011. [Online]. Available: http://www2.eecs.berkeley.edu/Pubs/TechRpts/2011/EECS-2011-94.html

[15] F. Udrea, "SOI-based devices and technologies for High Voltage ICs," in *2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Sep. 2007, pp. 74–81.

[16] S. Cha, D. Park, Y. Lee, C. Lee, J. Choi, J. Lee, and H. Lee, "AC/DC converter free LED driver for lightings," in *Consumer Electronics (ICCE), 2012 IEEE International Conference on*, Jan 2012, pp. 706–708.

[17] J. T. Hwang, K. Cho, D. Kim, M. Jung, G. Cho, and S. Yang, "A Simple LED Lamp Driver IC with Intelligent Power-Factor Correction," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, Feb 2011, pp. 236–238.

[18] J. T. Hwang, M. S. Jung, D. H. Kim, J. H. Lee, M. H. Jung, and J. H. Shin, "Off-the-Line Primary Side Regulation LED Lamp Driver With Single-Stage PFC and TRIAC Dimming Using LED Forward Voltage and Duty Variation Tracking Control," *Solid-State Circuits, IEEE Journal of*, pp. 3081–3094, Dec 2012.

[19] T. Lee. (2015) Teardown: 60-W-equivalent LED bulbs. [Online]. Available: http://www.powerelectronictips.com/teardown-60-w-equivalent-led-bulbs/

[20] D. Wolaver, "Fundamental Study of DC-DC Conversion Systems," Ph.D. dissertation, M.I.T., 1969.

[21] M. Seeman, V. Ng, H.-P. Le, M. John, E. Alon, and S. Sanders, "A Comparative Analysis of Switched-Capacitor and Inductor-Based DC-DC Conversion Technologies," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, June 2010, pp. 1–7.

[22] S. Sanders, E. Alon, H.-P. Le, M. Seeman, M. John, and V. Ng, "The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach," *Power Electronics, IEEE Transactions on*, vol. 28, no. 9, pp. 4146–4155, Sept 2013.

[23] M. Kline, I. Izyumin, B. Boser, and S. Sanders, "A Transformerless Galvanically Isolated Switched Capacitor LED Driver," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, 2012, pp. 2357–2360.

[24] C. Le, M. Kline, D. L. Gerber, S. R. Sanders, and P. R. Kinget, "A stackable switched-capacitor dc/dc converter ic for led drivers with 90% efficiency," in *Custom Integrated Circuits Conference (CICC), 2013 IEEE*, 2013, pp. 1–4.

[25] D. L. Gerber, M. Kline, S. R. Sanders, C. Le, and P. R. Kinget, "An integrated multilevel converter with sigma delta control for led lighting," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 2398–2403.

[26] M. Seeman and S. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841–851, March 2008.

[27] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun 1995, pp. 1215–1221 vol.2.

[28] B. Arntzen and D. Maksimovic, "Switched-capacitor DC/DC converter with resonant gate drive," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, vol. 1, Jun 1996, pp. 414–420 vol.1.

[29] P. Malcovati, M. Belloni, F. Gozzini, C. Bazzani, and A. Baschirotto, "A 0.18 μm CMOS 91%-efficiency 0.1-to-2A scalable buck-boost DC-DC converter for LED drivers," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, Feb 2012, pp. 280–282.

[30] S. Rao, Q. Khan, S. Bang, D. Swank, A. Rao, W. McIntyre, and P. Hanumolu, "A 1.2A buck-boost LED driver with 13% efficiency improvement using error-averaged SenseFET-based current sensing," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, Feb 2011, pp. 238–240.

[31] L. Li, Y. Gao, H. Jiang, P. K. T. Mok, and K. M. Lau, "An auto-zero-voltage-switching quasi-resonant led driver with gan fets and fully integrated led shunt protectors," *IEEE Journal of Solid-State Circuits*, pp. 913–923, March 2018.

[32] Z. Liu and H. Lee, "A wide-input-range efficiency-enhanced synchronous integrated led driver with adaptive resonant timing control," *IEEE Journal of Solid-State Circuits*, Aug 2016.

[33] Metacapacitors—Next-generation power electronics for led lighting and other applications. (2013). [Online]. Available: https://www.obrien-research.org/the-metacapacitor-project

[34] B. Van Tassell, S. Yang, C. Le, L. Huang, S. Liu, P. Chando, X. Liu, A. Byro, D. L. Gerber, E. S. Leland, S. R. Sanders, P. R. Kinget, I. Kymissis, D. Steingart, and S. O'Brien, "Metacapacitors: Printed Thin Film, Flexible Capacitors for Power Conversion Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2695–2708, April 2016.

[35] B. Lehman, A. Wilkins, S. Berman, M. Poplawski, and N. Johnson Miller, "Proposing measures of flicker in the low frequencies for lighting applications," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 2865–2872.

[36] S. Wang, X. Ruan, K. Yao, S. Tan, Y. Yang, and Z. Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4540–4548, Nov 2012.

[37] W. Chen and S. Y. R. Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1598–1607, March 2012.

[38] P. S. Almeida, M. A. Dalla Costa, J. M. Alonso, and H. A. C. Braga, "Application of series resonant converters to reduce ripple transmission to LED arrays in offline drivers," *Electronics Letters*, vol. 49, no. 6, pp. 414–415, March 2013.

[39] Fang Zheng Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, March 2001.

[40] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *Proceedings of the IEEE*, vol. 51, no. 11, pp. 1524–1535, Nov 1963.

[41] M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, vol. 2, June 1996, pp. 1013–1018 vol.2.

[42] J. Liao and M. Ferdowsi, "An improved cascaded H-bridge multilevel inverter controlled by an unbalanced voltage level sigma-delta modulator," in *2008 IEEE Vehicle Power and Propulsion Conference*, Sep. 2008, pp. 1–5.

[43] S. Wang, X. Ruan, K. Yao, S. Tan, Y. Yang, and Z. Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4540–4548, Nov 2012.

[44] M. N. Z. Abidin, "IEC 61000-3-2 Harmonics Standards Overview," Schaffner EMC Inc., Edsion, NJ, USA, Tech. Rep., 2006.