Voltage and Time-Domain Analog Circuit Techniques for Scaled CMOS Technologies

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Submitted in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy
in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2020

Abstract

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CMOS technology scaling has resulted in reduced supply voltage and intrinsic voltage gain of the transistor. This presents challenges to the analog circuit designers due to lower signal swing and achievable signal to noise ratio (SNR), leading to increased power consumption. At the same time, device speed has increased in lower design nodes, which has not been directly beneficial for analog circuit design. This thesis presents voltage-domain and time-domain circuit scaling friendly circuit architectures that minimize the power consumption and benefit from the increasing transistor speeds.

In the voltage-domain, an on-the-fly gain selection block is demonstrated as an alternative to the traditional MDAC architecture to enhance the input dynamic range of a medium-resolution medium-speed analog-to-digital converter (ADC) at reduced supply voltages. The proposed design also eliminates the need for a reference buffer, thus providing power savings. The measured prototype enhances the input dynamic range of a 12bit, 40MSPS ADC to 80.6dB at 1.2V supply voltage.

In the time-domain, a generic circuit design approach is presented, followed by an in-depth analysis of Voltage-Controlled-Oscillator based Operational Transconductance Amplifiers (VCO-

OTAs). A discrete-time-domain small-signal model based on the zero crossings of the internal VCOs is developed to predict the stability, the step response, and the frequency response of the circuit when placed in feedback. The model accurately predicts the circuit behavior for an arbitrary input frequency, even as the VCO free-running frequency approaches the unity-gain bandwidth of the closed-loop system, where other intuitive small-signal models available in the literature fail.

Next, we present an application of VCO-OTA in designing a baseband trans-impedance amplifier (TIA) for current-mode receivers as a scaling-friendly and power-efficient alternative to the inverter-based OTA. We illustrate a design methodology for the choice of the VCO-OTA parameters in the context of a receiver design with an example of a 20MHz RF-channel-bandwidth receiver operating at 2GHz. Receiver simulation results demonstrate an improvement of up to 12dB in blocker 1dB compression point (B1dB) for slightly higher power consumption or up to 2.6x power reduction of the TIA resulting in up to 2x power reduction of the receiver for similar B1dB performance.

Next, we present some examples of VCO-OTAs. We first illustrate the benefit of a VCO-OTA in a low-dropout-voltage regulator to achieve a dropout voltage of only100mV and operating down to 0.8V input supply, compared to the prototype based on traditional OTA with a minimum dropout voltage of 150mV, operating at a minimum of 1.2V supply. Both the capacitor-less prototypes can drive up to 1nF load capacitor and provide a current of 60mA. The next prototype showcases a method to reduce the power consumption of a VCO-OTA and spurs at the VCO frequency, with an application in the design of a fourth-order Butterworth filter at 4MHz. The thesis concludes with a design example of 0.2V VCO-OTA.

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Acknowledgments

If I have seen further it is by standing on the shoulders of giants

-Sir Isaac Newton

All great achievements are accomplished with the help and support of many people. Here I would like to thank those people who have helped me in the past couple of years to not only complete my doctoral program but also make it a memorable one.

I am really thankful to my thesis advisor, Professor Peter Kinget, under whose wings I learned to fly through the myriad of analog circuit design. His constant guidance, regular meetings, some chidings but not without supporting and inspiring thoughts have helped me effortlessly learn the intricacies circuit design. Besides the technical content, he has taught me how to explain and present well, which is an equally important skill for a circuit designer. While there is a long path to improvement, the fundamentals I learned from him will continue playing a significant role in shaping my future.

Next, I would like to thank Professor Yannis Tsividis, Professor Mingoo Seok, Professor John Parsons, and Dr. Shaorui Li for being on my dissertation committee and providing their valuable time, comments, and suggestions. Additionally, I would like to thank Professor John Parsons, Professor Nan Sun and Professor Tim Andeen working with whom on the Atlas project I learned how to handle the dynamics of a large team with several moving pieces.

I found great researchers and amazing colleagues as part of Columbia Integrated Systems Lab (CISL). My first interactions with Baradwaj, Jayanth, Karthik, Vaibhav, Chun-Wei, and Chengrui played a vital role in shaping my understanding of the research world. Each of them has been

great mentors for me, and I thank them for their help in shaping my career. I feel fortunate to have seniors like Tugce, Jianxun, Yang, Sharvil, Yu, and Ning with whom I always felt comfortable asking even the most basic questions for which I can not thank them enough. Sharing classes, working on projects, and having technical discussions with my colleagues Shravan, Daniel, and Manoj has always been a source of joy and great fun. I would like to thank Tanbir, Scott, and Matt, who have been my colleagues and seniors at the same time, who provided me a holistic industrial perspective, thus helping me come out of my bubble of academic understanding. Particularly, discussions with Tanbir always left me feeling even more excited about the work I am doing, and how does it fit in the broader perspective, for which I am thankful to him. His approach to life is very inspiring. I would also like to thank my other lab colleagues Yudong, Vivek, Guoxiang, Subhajit, Zhaowen, and Michael, with whom I have had interesting conversations ranging from technical topics to sports, health, family, and fun.

I feel fortunate to have been a part of Atlas project at CERN, one of the most famous physics experiment in the world. I got a chance to collaborate with a team of great people, from each of whom I got to learn many things. I thank Dr. Jaroslav for teaching me how to manage large scale engineering projects; Professor Gustaaf and Professor Georgia for valuable informal discussions on topics of Physics; and Rupal, Nancy, Amy, Bill, Chi, Kiley, and Alan for their help and support during testing at Nevis Laboratories. I also thank Ray, Chen-Kai, Chuck, Devanshu, and Mesut from UT-Austin, without whose help the collaboration project would not have been fruitful.

As part of Ph.D. projects, I also got a chance to work with several masters and exchange stu-

dents. I thank Sanket, Zhongjie, Suhas, Alessandro, and Debajit for providing me an opportunity to collaborate on their projects and learn a lot together in the process.

My thanks go to all the staff members of the EE department and GSA, especially Elsa, Yoel, Laura, Maribel, Arturo, Wendy, Susan, Cassandra, Raina, and Kington who have been very supportive of all the administrative requirements.

A special thanks to my friend Siddharth, who developed ycircuit software, using which I have drawn several figures in this thesis.

No task can be completed without the emotional support of a guide, family, and friends. I feel grateful for my spiritual master whose support was always there for me. I am also thankful to my brother, my parents, and my in-laws, who have always been there for me. Though the last couple of years have presented many trying times, their unconditional love, care, and affection have only grown throughout. I would like to thank all of my friends, particularly from Hindu Yuva, EGSC, and ISAC, all of whom made my time at Columbia not only fun but also memorable. In the end, I would like to thank the most special person in my life, without whom my life is incomplete. Rupal, my wife, has been a source of constant inspiration for me since the time we met. She has been a great colleague, a fantastic project partner, and most importantly, a wonderful friend. She has cheered for me in my achievements, inspired me during my low times, and has been patient with me in my trying times. I am looking forward to building an incredible future together with her!

Chapter 1

Analog Circuit Design Challenges in Scaled CMOS Technologies

Technology scaling has led to improved performance and increased density of integrated circuits (ICs) over the past few decades, resulting in their ubiquitous use in modern-day electronics. At the same time, it has also resulted in several challenges for analog design engineers. This thesis presents design techniques to overcome these challenges for analog and mixed-signal circuits in scaled technology. This chapter discusses how technology scaling affects the critical parameters for analog circuits.

1.1 Technology Scaling and its Benefits

Technology scaling is the trend of reducing the minimum size of the transistors used in IC design. Advances in lithographic techniques have made it possible to fabricate transistors with smaller dimensions reliably. Technology scaling has resulted in increased transistor density over the past few decades, discussed in the famous Moore's law [11] that has been serving as a guiding roadmap for the semiconductor industry since its inception.

A direct benefit of technology scaling is the reduction in the transistor area. Digital circuits,

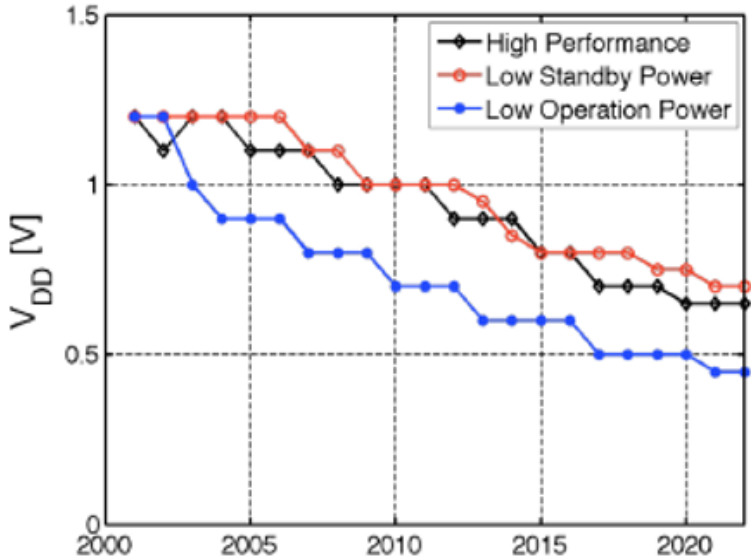


Figure 1.1: Technology scaling roadmap prediction for supply voltage V_{DD} by ITRS [1]

which are mostly composed of transistors, leverage this advantage to provide higher performance per unit area, resulting in reduced cost per IC. Another significant benefit is the reduction in parasitic capacitance, which increases the transistor speed and results in improved performance of digital circuits.

1.2 Effect of Technology Scaling on Analog Circuit Performance

While technology scaling has proven beneficial for digital circuits, it has been a mixed blessing for analog circuit designers. In this section, we discuss the major impact of scaling and their qualitative implications on analog circuit design. Readers are referred to [2, 3, 6] for detailed analysis.

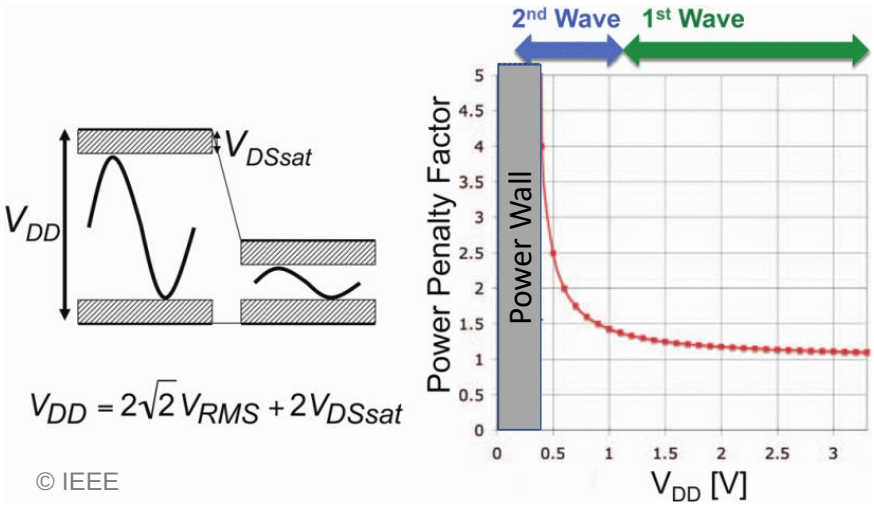


Figure 1.2: (a) Available fraction of supply voltage V_{DD} for signal swing reduces drastically with supply voltage scaling, resulting in (b) huge power consumption to achieve a given SNR at reduced V_{DD} referred to as a power wall [2].

1.2.1 Reduced SNR and High Power Penalty due to Supply Voltage Scaling

Reduction in length of a transistor is accompanied by reduction of gate thickness to maintain better control of the channel formed [12]. This results in reduced breakdown voltage, thus reducing the maximum permitted supply voltage as predicted by the International Technology Roadmap for Semiconductors (ITRS) (Fig. 1.1). For analog circuits, the maximum and the minimum signal values are limited by the supply voltage and the noise floor. With the thermal noise being constant, this leads to reduced signal swing, resulting in a lower signal to noise ratio (SNR).

This challenge is further exacerbated by the drain-source voltage headroom requirement V_{DSsat} for the transistors to operate in saturation region at sub-1V supply voltage (Fig. 1.2(a)). This requirement eats up the available voltage swing out of the supply voltage. As supply voltage V_{DD} reduces, the available signal swing reduces drastically, leading to a considerable power penalty for traditional analog circuits, represented by the power wall in Fig. 1.2(b) [2, 6].

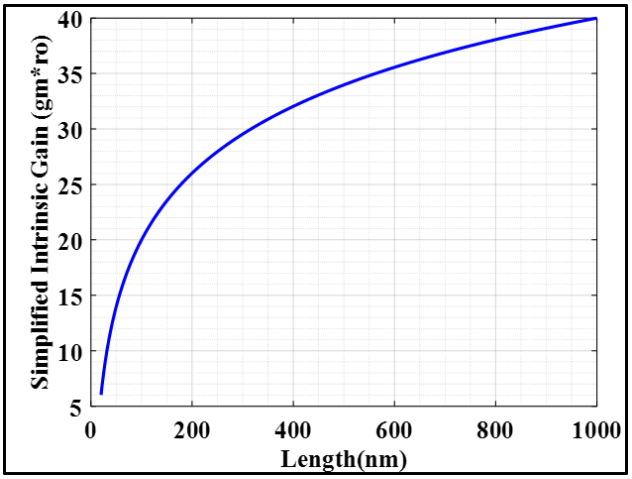


Figure 1.3: Simplified intrinsic voltage gain of a device decreases with reduction in transistor length, a side effect of technology scaling [3].

1.2.2 Need of Better Architectures to Overcome Reduced Intrinsic Voltage Gain

Reduced transistor length for lower technology nodes in planar transistors decreases its intrinsic voltage gain (IVG) because the effect of drain-source voltage in modulating the channel increases [1] (Fig. 1.3) [3]. Velocity saturation at lower technology nodes further worsens the problem. Though IVG is not a fundamental quantity required in an analog circuit, it plays a major role in the design of operational amplifiers, which are an important component of several analog-and-mixed-signal circuits. Reduced IVG along with reduced supply voltage, which prevents stacking of transistors, a methodology commonly used in traditional cascode and telescopic operational amplifiers to increase their voltage gain, necessitate analog designers to investigate scaling-friendly architectures.

[1] Finfets excluded, for which the intrinsic gain increases slightly.

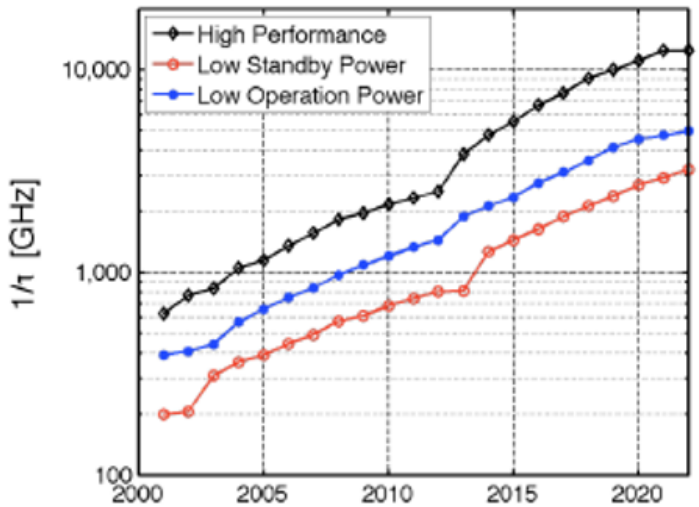


Figure 1.4: Technology scaling roadmap prediction by ITRS for the transit time from drain to source of a device, qualitatively representing the trend of device speed [1].

1.2.3 New Opportunity to Benefit from the Increased Device Speed

A significant benefit of technology scaling is the reduction in device parasitics leading to increased transistor speed (Fig. 1.4). Traditional analog circuits use voltage domain or current domain for signal representation. Increasing transistor speeds, however, provide a new opportunity to use scaling friendly circuits that represent the signal in the time domain. Such circuits can operate at extremely low supply voltages, and their performance does not rely on the intrinsic voltage gain of the transistor, thereby benefiting from technology scaling.

1.3 Thesis Goals and Organization

The goal of this thesis is to discuss circuit improvements in two signal representation domains, namely the voltage-domain and the time-domain, to address the challenges introduced by technology scaling.

Chapter 2 presents the voltage-domain approach to increase the dynamic range of a medium-to-high resolution data converter, without the additional overhead of increased power-consumption of reference buffers, by using an on-the-fly gain selection block. This approach minimizes the increased power penalty due to SNR reduction at low supply voltage by benefiting from application-specific features.

Chapters 3 through 6 focus on the time-domain signal representation for analog circuit design, which can break the power wall discussed in Section 1.2.1, provide high DC gains irrespective of reduction in intrinsic voltage gain, and benefit from increased transistor speed at lower technology nodes.

Chapter 3 discusses the state-of-the-art time-domain circuits and their benefits compared to voltage-domain circuits. It also lays the foundation for the voltage-controlled-oscillator-based operational transconductance amplifiers (VCO-OTAs), the particular time-domain circuit modeled and used in applications in this thesis.

Chapter 4 presents a zero-crossing-based discrete time-domain model (ZCTDM) for a VCO-OTA to capture entire closed-loop dynamics when the VCO-OTA placed in feedback.

Chapter 5 discusses the benefits of using VCO-OTAs in designing baseband trans-impedance

amplifiers (TIAs) for current-mode receivers. Due to the high DC gain property of the VCO-OTAs, they prove to be a power-efficient scaling-friendly solution for this application.

Chapter 6 discusses other applications of VCO-OTAs in a low-dropout regulator and a fourth-order Butterworth filter design. It also explores the option of reducing the supply voltage of VCO-OTA to 0.2V and showcases its application in first-order filter design.

Chapter 7 provides conclusions and discusses opportunities for future work.

Chapter 2

On-the-fly Gain Selection For Input-Dynamic-Range Enhancement of Data Converters[1]

2.1 Background

Data converters are used to interface the physical analog world with the digital-computer world and form an integral part of most of the electronic devices today. For Nyquist-rate converters the maximum achievable input dynamic range (IDR) is reducing with the technology scaling because reduction in supply voltage reduces the maximum achievable signal swing. For example reducing supply voltage from 5V to 1.2V reduces IDR by 12dB. To increase IDR, the thermal noise floor needs to be reduced by increasing the sampling capacitor, which leads to increased power consumption in the input driver, reference buffers, and the amplifier being loaded by the sampling capacitor.

For a medium-speed, medium-to-high resolution Nyquist-rate ADC with a multiplying digital

[1]This project was done in collaboration with Nevis Laboratories at Columbia University, and Electrical and Computer Engineering, and Physics Department at UT Austin. The funding was provided by NSF.

to analog converter structure (MDAC) as the first stage, IDR is traditionally increased by adding more bits to reduce quantization noise along with the thermal noise. This method increases both the ”instantaneous SNDR” (simply referred to as ”SNDR”) and the IDR. An example of increasing the IDR of a 12b ADC with 73.6dB SNDR and IDR to a 14b ADC with an IDR and SNDR of 85.6dB is shown in Fig. 2.1(a). The drawback of this approach is that the power consumption for the reference buffer, the input driver, and the amplifier increases proportionally.

Increased SNDR when increasing the IDR is not needed in every application. The LAR-calorimeter readout requirement for ATLAS experiment at CERN is one such example [13, 14]. In this experiment, two high-energy proton beams traveling close to the speed of light in opposite directions are made to collide inside a large calorimeter emitting a large number of particles. One of the project requirements is to measure the energy of the particles emitted during the collision. This requirement is met by passing the emitted particles through a liquid Argon (LAR) calorimeter, where a current pulse proportional to the particle energy is produced. This current is amplified, converted to voltage, and measured using an ADC to find the particle energy, which can vary from 200MeV to 3TeV. The total input dynamic range to be covered is therefore roughly 60,000 (16bit) assuming the minimum noise floor of the energy to be measured is 50MeV. The collisions happen every 25nsec, requiring the ADC conversion speed of 40MSPS. For the Phase-II upgrade, the required 16b IDR is covered by using two 14b paths as shown in the simplified system block diagram of the system in Fig. 2.2 [14]. The required IDR for each path here is greater than 80dB, but the peak SNDR requirement is less than 60dB. One critical system requirement is that the circuits need to be radiation hard. This implies that (a) thin oxide transistors with a maximum supply of 1.2V

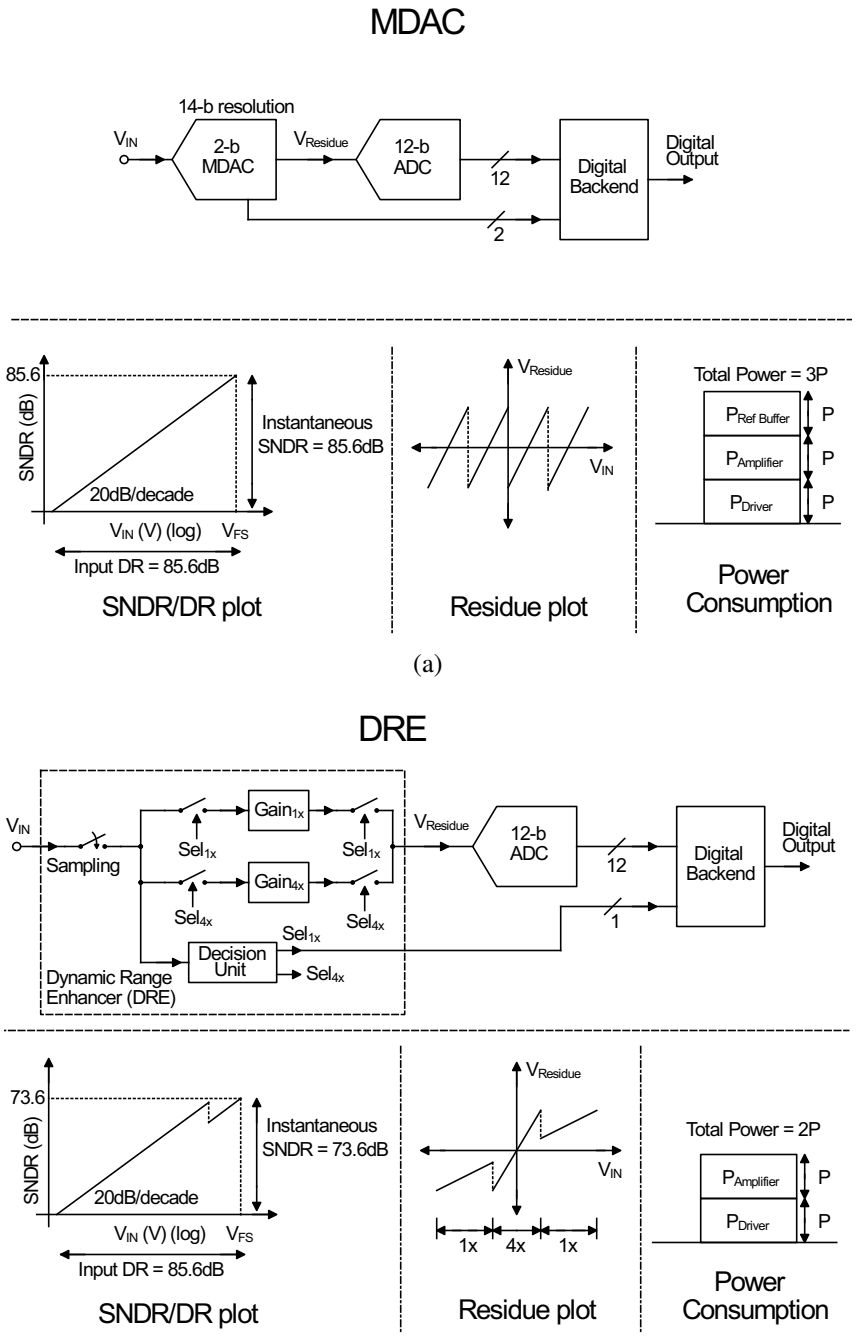


Figure 2.1: Two architectures to realize the front-end block for a 14b DR measurement (a) A traditional ideal multiplying digital-to-analog converter (MDAC) block resolving two most-significant bits and providing the residue to the 12b SAR ADC. (b) Proposed dynamic range enhancer (DRE) block providing on-the-fly gain of either 1x or 4x to the signal going to the 12b SAR ADC. The DRE does not require a reference buffer, thus saves power and area.

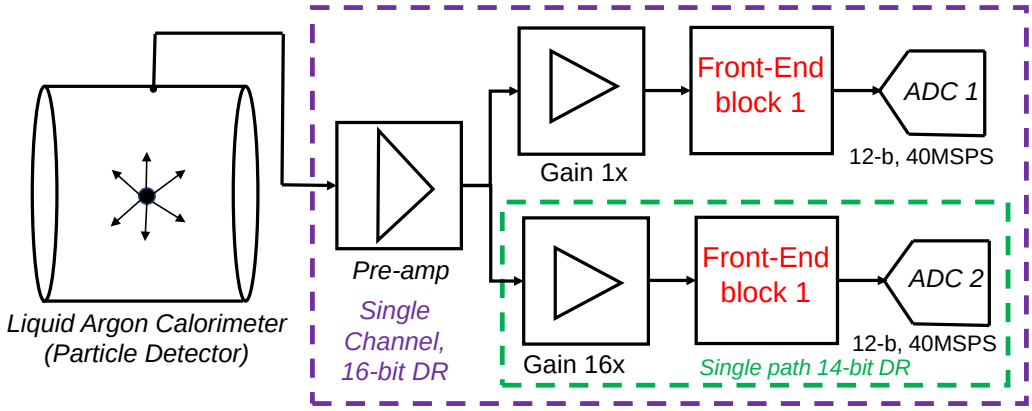


Figure 2.2: Simplified block diagram of CERN liquid-Argon-calorimeter readout system requiring 16b dynamic range (DR) per channel for particle energy measurement, fulfilled by two ADC paths each supporting 14b DR.

need to be used to reduce oxide breakdown due to radiation, (b) the minimum capacitance used for sampling capacitors needs to be greater than 10fF[2], and (c) every digital memory needs to be triple-redundant and a majority voting is to be used to read out its value. This is done to eliminate the risk of propagating the wrong digital value if the bit flips due to radiation.

To accommodate these requirements, we propose a front-end dynamic range enhancer (DRE) followed by a 12b SAR ADC, with a conceptual diagram shown in Fig. 2.1(b). The DRE samples the input and provides either the buffered (1x) version or the amplified (4x) version to the SAR. If the magnitude of the input sample is less than a particular threshold, the 4x gain is chosen, otherwise the 1x gain is used. The SNDR plot with respect to the input voltage, therefore, follows the 4x path for lower input amplitudes reaching the peak at one-fourth of the full-scale voltage V_{FS},

[2]Using 10fF as a minimum capacitance ensures the voltage level change from the background radiation energy particles charging/discharging the capacitance is within experimental accuracy levels. This result was found emperically from previous measurements

after which it drops to the 1x path (Fig. 2.1(b)). The ideal IDR achieved is therefore 85.6dB while the peak SNDR is same as the backend 12b SAR ADC, which is ideally 73.6dB.

One more application of the proposed on-the-fly gain-selection DRE in communication systems to overcome the problem of fading. When a mobile receiver is in motion, the power received at the mobile antenna can vary considerably due to presence of multipath channel interference. DRE can provide the extra front-end gain needed to provide higher amplitude signal to the back-end ADC. DRE can also be used in other experimental readout circuits with requirements similar to LAR calorimeter described above.

To increase the IDR, another obvious choice is to use a programmable gain amplifier with automatic Gain Control (AGC) before the ADC. However, most of the AGCs operate in a feedback loop and have an inherent delay before the gain is adjusted. This is a problem for the DRE because the gain needs to be chosen on a per-sample basis, so a direct use of a traditional AGC is not possible. The ”Divide and Conquer” approach for increasing the IDR of analog filters provides an alternative to AGC by having separate gain paths, each with a different gain followed by a filter and inverse gain [15]. The correct path is chosen based on the input amplitude. The design in [15] achieves a total IDR of 81dB (48dB DR achieved with 33dB SNDR) with the filters designed at 10MHz center frequency with 18MHz bandwidth. However, the peak SNDR achieved by such a system is only 45dB, which is not sufficient for the DRE block. Additionally, if this method is used in the implementation of DRE, this would mean having an ADC for each branch after the gain block, which would result in increased area and high power consumption.

Another class of amplifiers called Logarithmic Amplifiers (LogAmps) have been traditionally

used for IDR extension. Early papers such as [16] and [17] indicate the option of achieving 40dB and 80dB DR at 600MHz and 70MHz respectively. However, the instantaneous SNDR achieved by these amplifiers is less than 40dB. Similarly, a 10MSPS 80dB DR pipeline based logarithmic ADC achieves a peak SNDR of 44.3dB [18] and therefore does not satisfy ATLAS experiment requirements. Many commercial logAmps operate at higher frequencies of 3.8GHz [19] or 6GHz [20] and provide high input DR, but they are often only used to measure signal power. Their deviation from the exact logarithmic behavior in the input-output characteristic and the settling time required when the input is changed prohibits their use for the proposed application. Other classes of LogAmp such as DC LogAmp and baseband LogAmp [21] also suffer from the problem of low SNDR due to deviation from the ideal logarithmic behavior and thus are not suitable.

More recently, companding has moved from analog domain to digital domain for audio applications [22]. The input is first sampled with >16bit precision using Delta-Sigma ADC and is then compressed in the digital domain. However, this approach is also not suitable for ATLAS experiment because designing a Delta-Sigma for a 20MHz signal bandwidth is quite difficult and a point to point sampling requirement for the application disqualifies Sigma-Delta architecture. Analog companding is another similar approach in which the signal is first compressed in the analog domain, sampled uniformly and later expanded in the digital domain. The use of companding for filtering has been shown for audio signals [23]. At higher frequencies in CMOS, Progressive Compression Amplifiers (PCAs) such as [24] and [25] provide the function of companding. They can be modified from their original use as a power meter to act as a compander for point-to-point signal information compression in the analog domain, followed by sampling and digital

domain recovery using a lookup table. However, companding is a non-linear operation, resulting in expansion of the input signal bandwidth. To meet the specifications of the ATLAS Calorimeter experiment, this increase in bandwidth places prohibitively high UGB requirement of more than 10GHz for the amplifier, disqualifying this architecture as an option.

Floating-Point ADCs (FpADCs) provide another method of DR extension [26–31]. FpADCs can be considered as a modified version of AGC where amplification is changed dynamically based on the current input. All the architectures provided in the literature achieve high DR, but none of them achieves >60dB SNDR as per the requirement. For example [26] and [27] provide less than 10bit ENOB. Similarly [31] achieves a 10 to 15bit DR at a speed of 60MSPS. However, the peak SNDR achieved is less than 60dB for signals close to the Nyquist rate.

SAR ADCs have recently been shown to provide up to 78dB SNDR at Nyquist rate at 40MSPS sampling rate with 24mW input power [32]. However, achieving >80dB DR at 40MSPS has still not been demonstrated using SAR ADC architecture.

The DRE architecture proposed in this chapter is a modified version of FpADC [31] where the number of amplifiers and the required feedback capacitor to be driven have been reduced, providing 4x normalized power savings while providing similar performance. Additional switches for autozero slope distortion are used to achieve a peak low-frequency SNDR of 66.8dB, with 80.6dB DR at 40MSPS sampling rate.

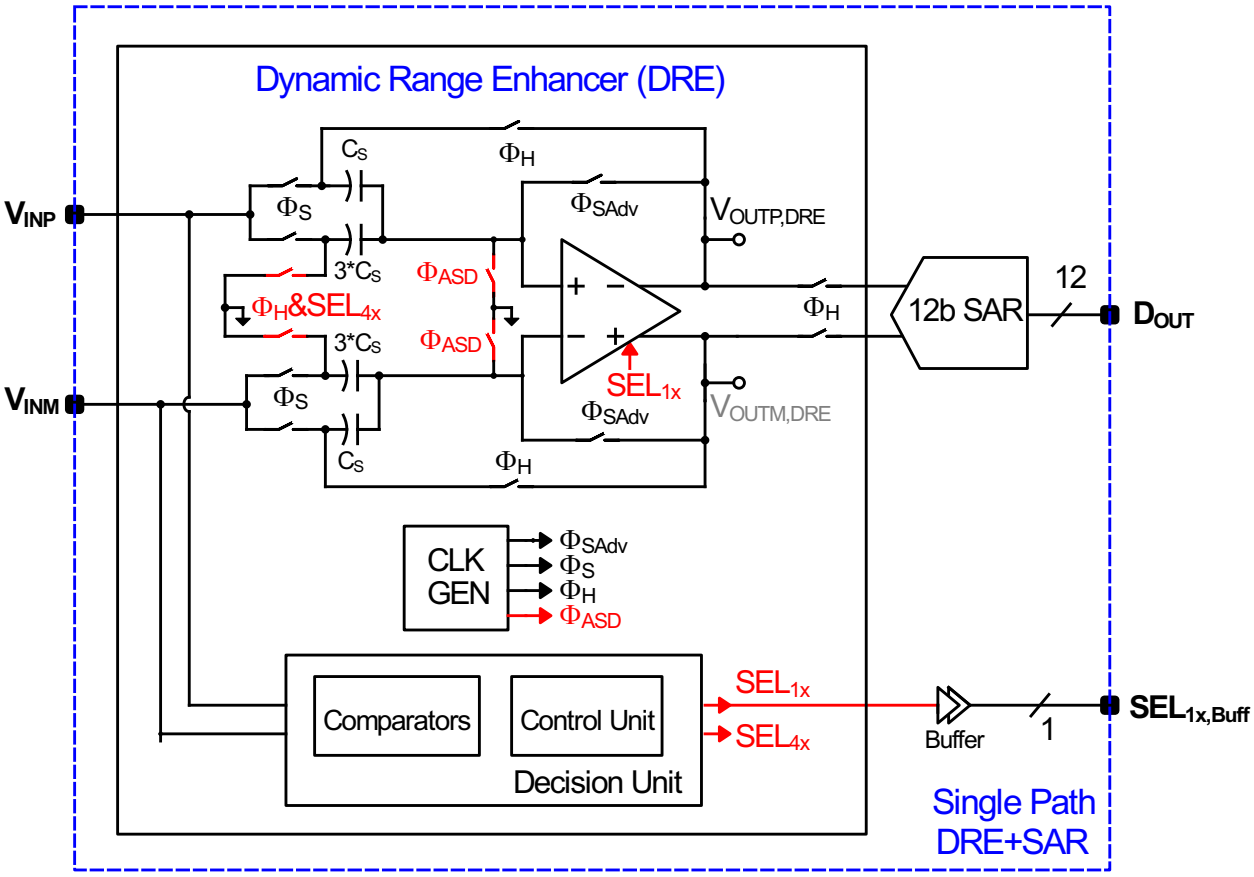


Figure 2.3: Block diagram of a dynamic range enhancer (DRE) containing a front-end sampling network, an amplifier, a decision unit (DU), and a clock generator. Based on the input sample, the DU provides select signals to the amplifier switches to configure the DRE in either 1x or 4x gain mode.

2.2 Dynamic Range Enhancer (DRE)

2.2.1 DRE Operation

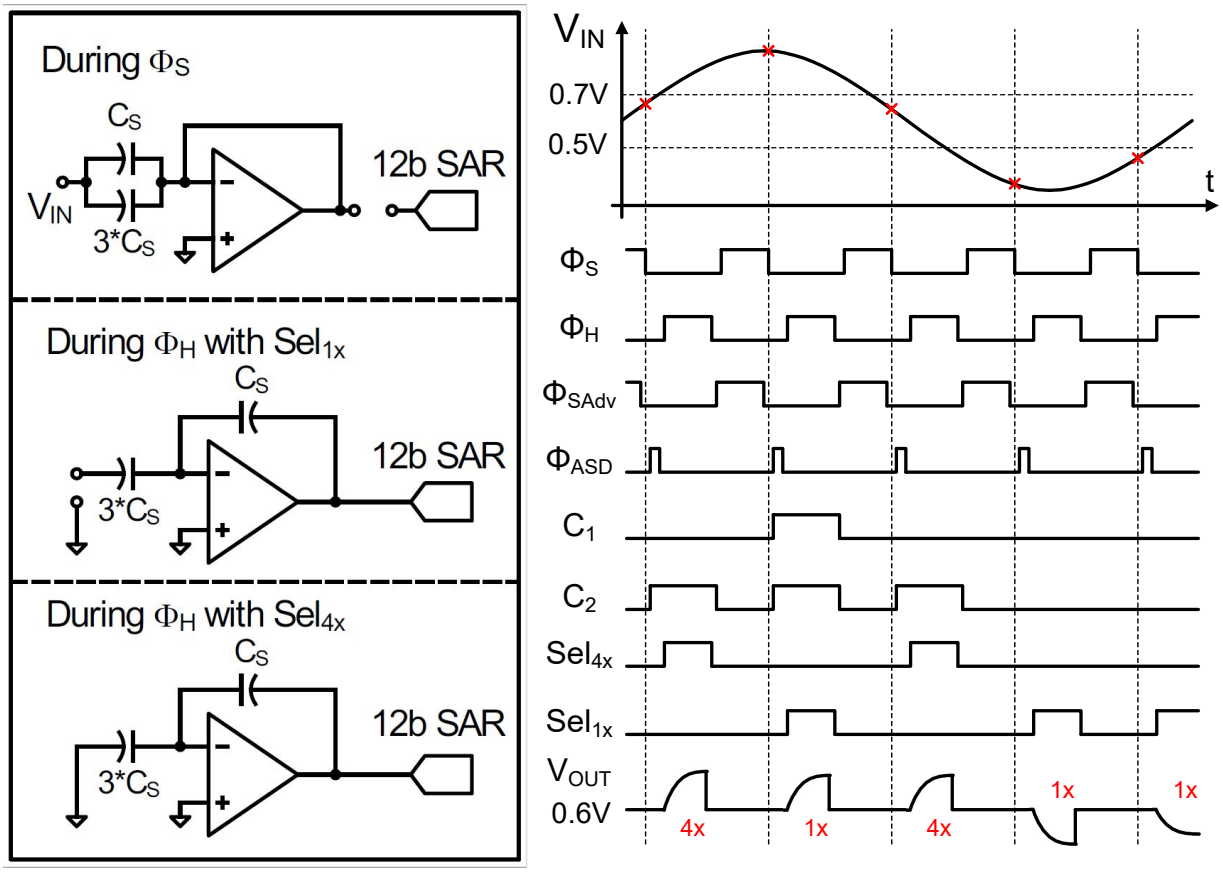
The dynamic range enhancer (DRE) consists of a sample and hold amplifier, a Decision Unit (DU), and a clock generator (Fig. 2.3). During the sampling phase ϕ_S differential input is sampled on $4 * C_S$ sampling capacitors. Just after sampling, the Decision Unit decides to either choose 1x gain if the magnitude of the sampled input voltage is larger than a particular threshold voltage or

choose 4x gain otherwise. During the non-overlapping hold phase ϕ_H, C_S capacitor is flipped over the amplifier. If 1x gain is chosen, the $3 * C_S$ capacitor is left floating. This retains the charges on both C_S and $3 * C_S$ capacitors, virtually buffering the sampled input signal to the output. If during ϕ_S 4x gain is chosen, $3 * C_S$ is connected to V_{REF}. This transfers the charge from $3 * C_S$ to C_S, thus quadrupling the total charge of the C_S capacitor and providing a gain of 4x. The circuit configuration and the timing diagram during the complete sample and hold process is shown in Fig. 2.4.

The output of the DRE is provided to a 12b SAR ADC, which further quantizes the data. The SAR output, along with the selection used for that particular sample (1x or 4x) is provided to an off-chip system. For 1x gain, the SAR data is appended with two zeros in the end, while for 4x gain, the data is renormalized by dividing by a factor of 4, implemented by adding two zeros in the front to form the final 14b result.

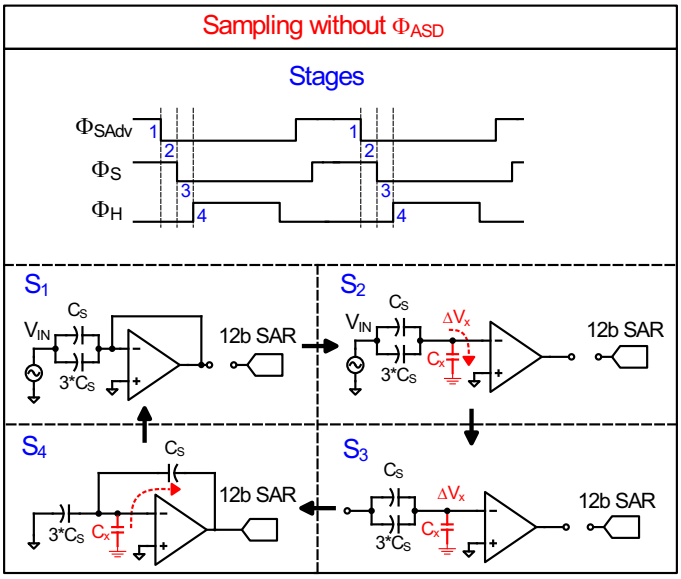
An advanced version of the sampling clock ϕ_{SAdv}, which is non-overlapping with ϕ_H as well, is used for the front-end sampling switches. Another non-overlapping clock phase ϕ_{ASD} is introduced in the proposed design to overcome second-order challenges, as discussed in Section 2.2.3.

Even though a gain of 1x and 4x is chosen here, it is possible to generalize the concept for multiple gains (similar to [31]). The backend ADC then limits the peak SNDR achieved and the peak IDR is limited by the ratio of peak signal swing limited by V_{Sup} and noise floor determined by the total sampling capacitor.

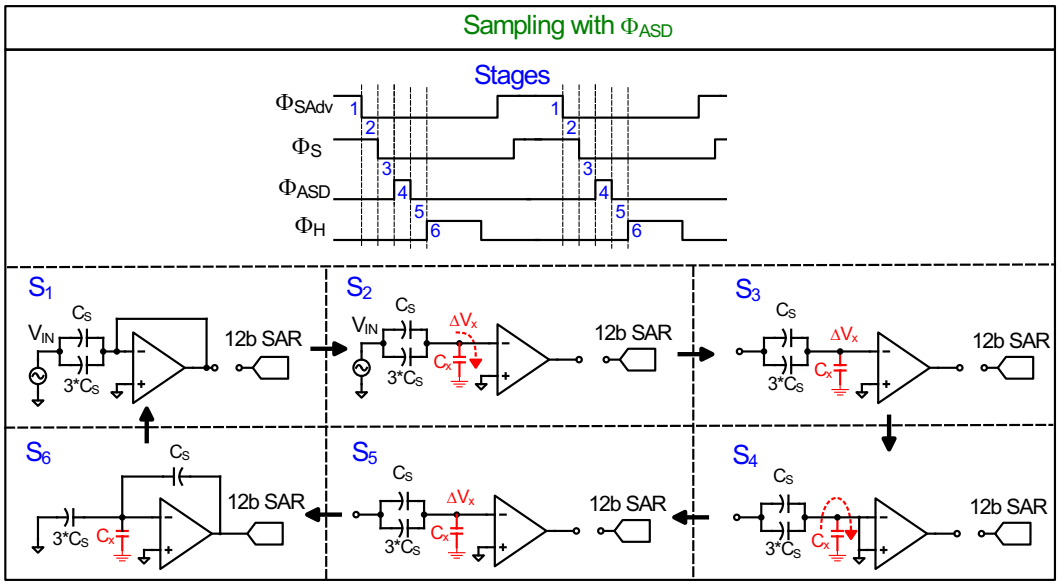


(a) (b)

Figure 2.4: (a) Single-ended configuration of DRE in sampling phase, hold phase with 1x gain, and hold phase with 4x gain. (b) Timing diagram for the DRE.



(a)



(b)

Figure 2.5: (a) Schematic diagram depicting the problem of input slope dependent based charge injection during 1x gain mode. This problem does not occur during 4x mode. (b) Solving the problem of input-slope dependent charge injection by introducing an extra Autozero slope distortion phase (ϕ_{ASD}).

2.2.2 Need of Autozero-Slope-Distortion Clock Phase (ϕ_{ASD})

Consider the single-ended equivalent of the DRE during different clock phases (shown as stages S_1 to S_4) implemented without ϕ_{ASD} clock in Fig. 2.5(a). During S_1, both ϕ_{SAdv} and ϕ_S are active, the amplifier is placed in a unity gain feedback, and the input is sampled on C_S and $3*C_S$. During S_2, ϕ_{SAdv} goes down, but ϕ_S is still on. This prevents the charge injection of the switches from affecting the differential-output linearity. In this phase, the input is still changing, thus charging up the parasitic capacitor C_X. During S_3 when all the clock phases are low, C_X retains the charge while in S_4 when the ϕ_H is on, C_X transfers its charge to C_S capacitor.

Note that this charge transfer from C_X to C_S takes place irrespective of whether 1x gain or 4x gain is chosen. This transfer creates a difference between the final normalized voltage developed at the output of DRE in the 1x and the 4x cases. To understand this, consider an example when the input voltage V_{IN} is sampled on the two capacitors during S_1. If the input changes by ΔV_{IN} during S_2 and $C_X \ll 4*C_S$, the capacitors C_S and $3*C_S$ capacitors lose approximately $1/4*C_X*\Delta V_{IN}$ and $3/4*C_S*\Delta V_{IN}$ charge respectively, while C_X gains the sum of these two charges. This charge remains on C_X during S_3 and gets transferred to C_S during S_4. For the 4x case, this was the exact charge that was lost from the sampling capacitors in S_1 and hence, the net charge is conserved. However, for the 1x case, this is more than the charge lost by C_S capacitor alone. The output voltage V_{OUT} at the end of ϕ_H can thus be derived as:

$$\begin{aligned} V_{OUT,1x} &\approx V_{IN} + 3/4*C_X*\Delta V_{IN} \\ V_{OUT,4x} &= 4*V_{IN} \end{aligned} \tag{2.1}$$

The extra term in case of $V_{OUT,1x}$ results in non-linearity during recombination of 1x and 4x samples. Since the additional charge depends on ΔV_{IN}, which depends on the input slope, degradation worsens as the input frequency increases. This non-linearity can be eliminated by using ϕ_{ASD} clock phase, as explained next.

2.2.3 Eliminating Input-Slope-based Distortion Using ϕ_{ASD}

We propose to use an extra non-overlapping clock phase ϕ_{ASD} which automatically zeroes out the input-slope dependent distortion. The single-ended circuits during different stages with ϕ_{ASD} are shown in Fig. 2.5(b). S_1 and S_2 stages are the same as earlier. After both ϕ_{SAdv} and ϕ_S are down in S_3, ϕ_{ASD} turns on in S_4 and shorts the virtual ground node to V_{REF}. This eliminates the charge at the C_X node. The charge on all the capacitors is retained in S_5. During S_6, no charge is transferred from C_X since this capacitor was already discharged in S_3.

The updated output voltage for 1x and 4x gain in the presence of ϕ_{ASD} can be given as:

$$\begin{aligned} V_{OUT,1x} &\approx V_{IN} - 1/4 * C_X * \Delta V_{IN} \\ V_{OUT,4x} &\approx 4 * V_{IN} - C_X * \Delta V_{IN} \end{aligned} \tag{2.2}$$

The normalized voltages for 1x and 4x cases are now equal as predicted by (2.2). There is a loss of charge proportional to the input frequency, which results in a slight reduction of absolute gain with the input frequency. This reduction, however, does not affect the linearity of the DRE since the relative ratio between 1x and 4x gain is maintained to be precisely 4.0. The absolute

voltage gain reduction is equivalent to placing a linear anti-aliasing filter before the ADC, which does not affect the linearity of the ADC.

2.2.4 DRE Calibration

During normal operation of the DRE, some samples undergo 1x gain while the others 4x gain. It is therefore essential to normalize the SAR digital output to obtain the final signal. In an ideal case, samples undergoing 4x gain need to be digitally divided by 4 to obtain the 1x equivalent of those samples. In practice, however, both gain error and offset play a role and need to be accounted for.

There are four primary sources of error (Fig. 2.6(a)): input offset v_{OS} of the amplifier, 1x gain error G_{1x}, 4x gain error G_{4x}, and additional output common-mode signal $v_{OUT,CM}$ representing the equivalent of SAR common-mode digital value introduced while converting a signed DRE signal into unsigned digital code at the SAR output. G_{1x} and G_{4x} account for errors due to capacitor mismatch and finite amplifier gain.

A simplified model shown in Fig. 2.6(b) can be derived from the physical model by observing two facts: a. Input offset can be moved after the amplifier and combined with common-mode voltage, and b. For linearity purpose only relative gain between 1x and 4x matters[3]. The equivalent model consists of only three variables, namely 1x mode offset $v_{OS,1x}$, 4x mode offset $v_{OS,4x}$, and 4x:1x relative gain ratio G.

Based on this model, a calibration model to reverse the effect of DRE can be derived (Fig. 2.6(c)).

[3]This is because overall channel gain is calibrated separately

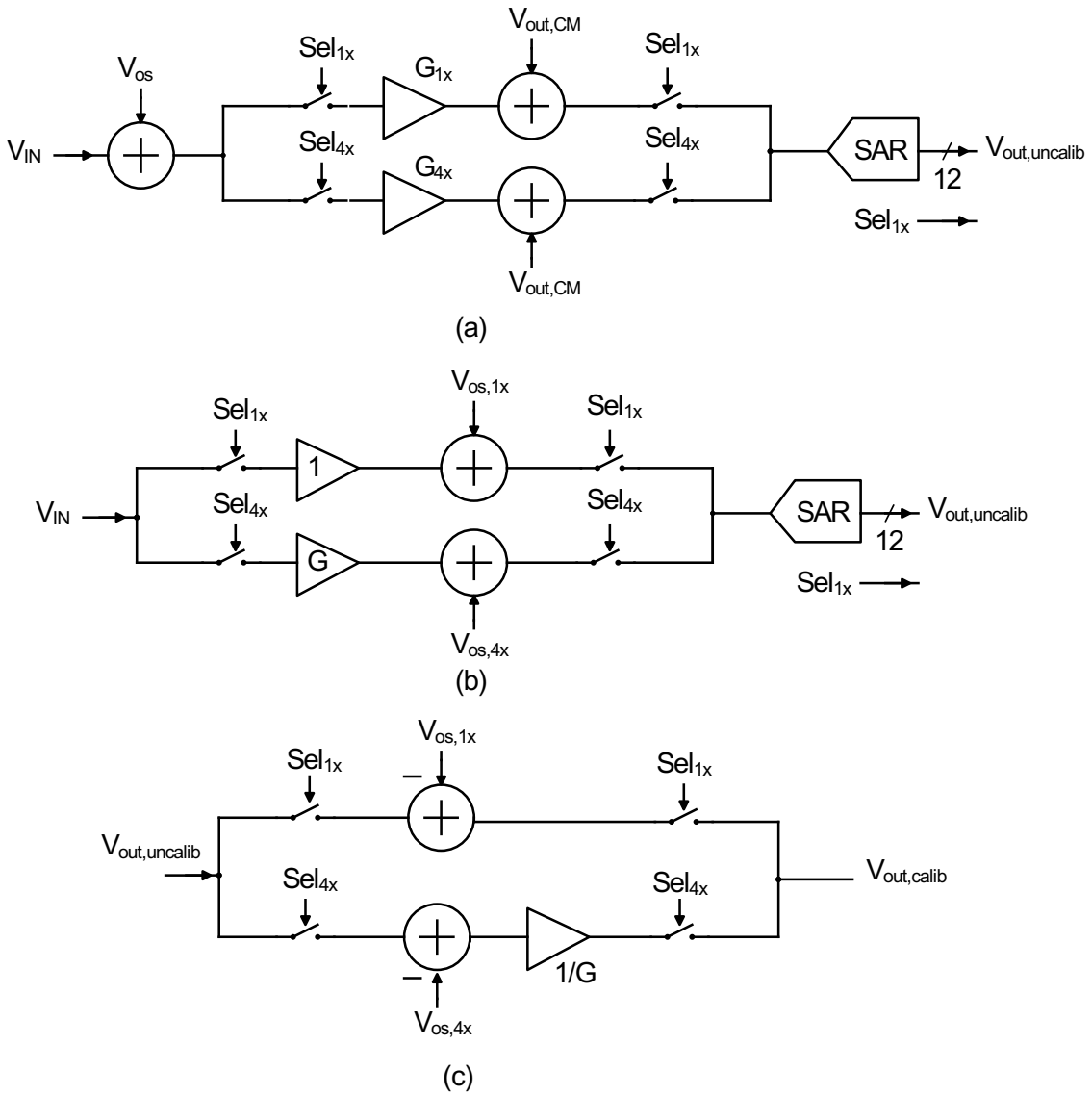


Figure 2.6: (a) DRE model depicting the expected offset and gain errors in DRE (b) Simplified DRE model for errors (c) Calibration scheme to correct for offset and gain error.

For samples with 1x gain, the final signal is obtained by subtracting $v_{OS,1x}$. For samples with 4x gain, $v_{OS,4x}$ is first subtracted followed by division with G to obtain the final result.

In the model, the number G is close to, but not precisely four. Division by G in the digital domain is therefore non-trivial. We have therefore implemented an analog gain calibration scheme using capacitors as discussed in [33]. Based on the gain estimated, it is possible to either increase or decrease the equivalent gain of the 4x path relative to 1x path. However, the gain and offset correction is applied offline using MATLAB [34] for the results used in this chapter for simplicity.

2.3 Circuit Implementation

2.3.1 Amplifier

A gain-boosted telescopic two-stage operational amplifier is used for the DRE to provide a high open-loop DC gain greater than 90dB (Fig. 2.7(a)). This is required to avoid amplifier gain errors across process, voltage, and temperature (PVT) in the 4x gain case when a feedback factor of 1/4 reduces the closed-loop gain by 12dB. Non-minimum transistor gate lengths are used to increase the DC gain. All the devices used are low threshold-voltage (LVT) to minimize the gate-source voltage drop required, except for the tail current source in the first stage which is a regular threshold voltage (RVT) device to ensure that bias transistors (not shown here) do not enter triode region with PVT corner variation. The input transistor length is kept at 2x the minimum length instead of 4x size for other transistors as a tradeoff between introducing extra parasitic capacitance at the virtual ground node that reduces the feedback factor with the DC gain achievable with the transistors.

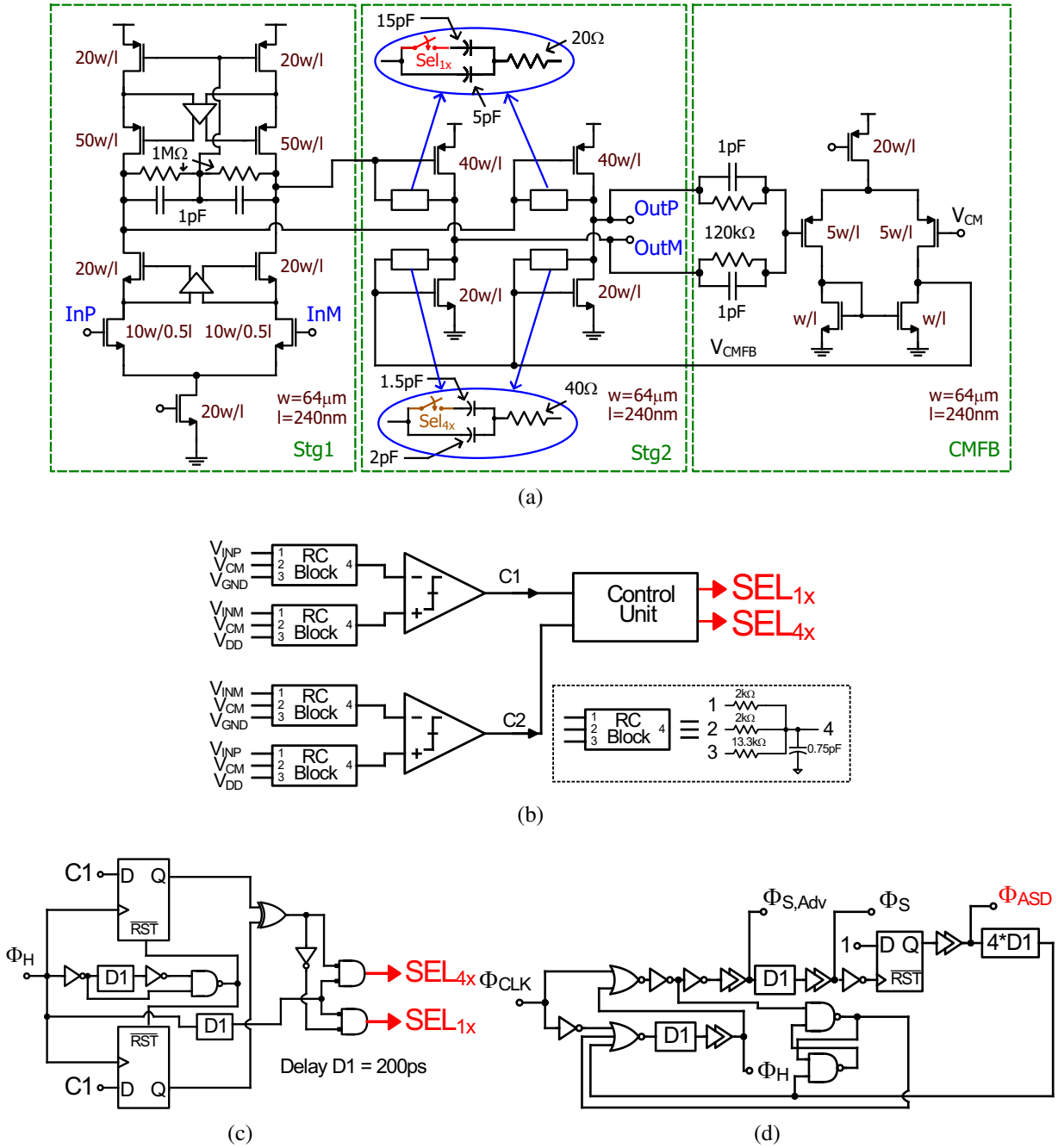


Figure 2.7: Detailed schematic diagram of (a) Amplifier, (b) Decision unit (DU), (c) Control unit, and (d) Clock generator. The transistors in the amplifier have 16 fingers each with a width of 10μm for PMOS and 2μm for NMOS, with the total width shown in the figure achieved using multiplicity.

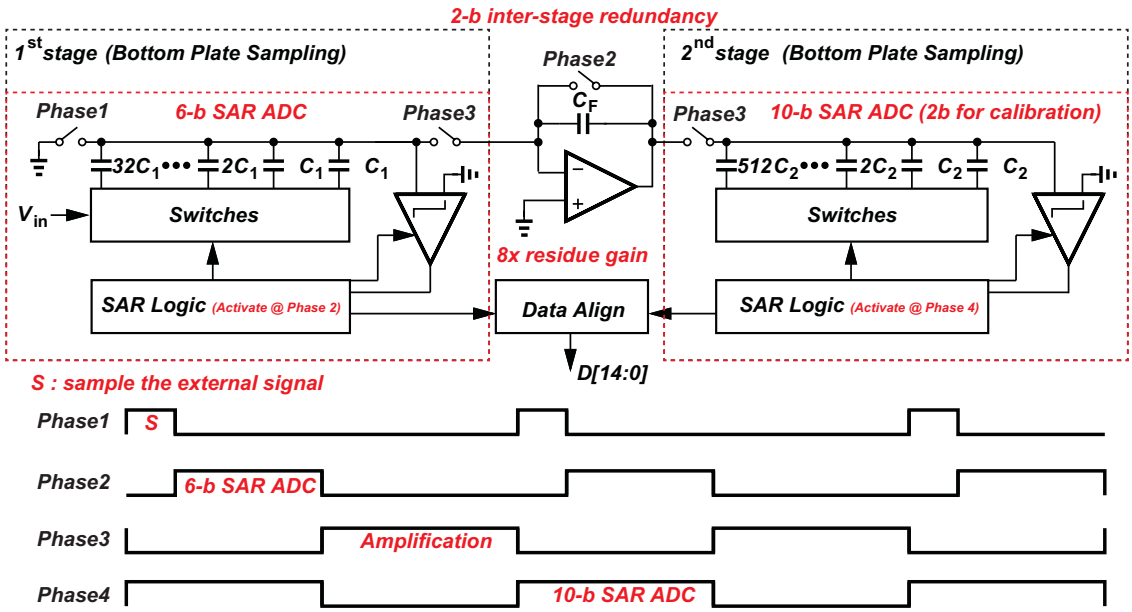


Figure 2.8: Schematic diagram of the 12b SAR consisting of two stages resolving 6b and 10b respectively, with two bits inter-stage overlap and two end bits used for calibration purposes.

Since the amplifier operates in 1x and 4x modes, a switched compensation capacitor is used. When Sel1x is on during the sample phase, and the 1x mode hold phase, the complete 20pF capacitor acts as a compensation capacitor. If 20pF capacitor is also used in the 4x gain mode, the loop gain will drop by a factor of 4x because of beta factor being 1/4, thus reducing the UGB of the closed loop. To avoid this problem, the switch in the compensation capacitor is turned off during 4x mode, thereby using a 5pF capacitor in this mode for compensation. This reduction in capacitance increases the dominant pole frequency by 4x. If used in a unity-feedback configuration, the phase margin in 4x case will be very low because of increase in the dominant pole frequency. However, since the feedback factor is 1/4 in the 4x gain mode, the loop is still stable with a similar UGB and phase margin for both the 1x and the 4x cases [31].

It is essential to maintain the common-mode voltage of the DRE output at mid-rail, to ensure

that a maximum symmetric output voltage swing is available. A differential amplifier structure providing 50dB DC gain is therefore used to provide the common-mode feedback (CMFB) for the second stage. This requires an additional compensation capacitor of 3.5pF in 4x gain mode and 2pF in 1x mode to be used for the CMFB loop, and separate first-stage feedback to maintain the high-frequency response for the second stage CMFB loop. The first stage CMFB is provided using a diode connection, which helps in PVT tracking of the threshold voltage of the second stage transistor as well. The gain-boosting amplifier for both PMOS and NMOS also use diode-connected CMFB structure.

2.3.2 Decision Unit

The decision unit (DU) is responsible for deciding the required gain to be used for the current sample with the possible option of 1x or 4x. If the magnitude of the input sample is less than a threshold voltage, 4x gain is selected, else 1x gain is selected.

Two comparators are used in the decision unit, as shown in Fig. 2.7(b), to evaluate the differential input voltage with respect to the threshold. A clocked comparator design based on [35] is used. An RC block is used to level shift the differential input to compare it with a differential reference voltage, which is derived from the supply and the ground voltage. Note that the only gain-selection criteria are to avoid saturation of the 4x path, the absolute value of the threshold voltage does not matter[4]. Compared to a traditional sub-ADC, this relaxes the total number of comparators and their offset requirements, thereby reducing their power consumption.

[4] Again, this is because the overall channel gain is calibrated separately

A metastability-detection circuit follows the comparators. If the threshold is set below the saturation limit for the 4x gain, then it does not matter whether the 1x or the 4x path is chosen during the metastability period, as long as one of them is forced. The metastability-detection circuit is configured to enforce 1x gain if such a condition arises.

The comparator outputs $C1$ and $C2$ go to a control unit consisting of flip-flops followed by a combinational circuit to generate Sel_{1x} and Sel_{4x} as shown in Fig. 2.7(c). The flip-flops are triple redundant using a majority vote counter to ensure that radiation does not cause the decision to change in case of a radiation-induced bit flip [13, 14]. These select signals are used to configure the DRE amplifier and other switches during the sample and the hold phase.

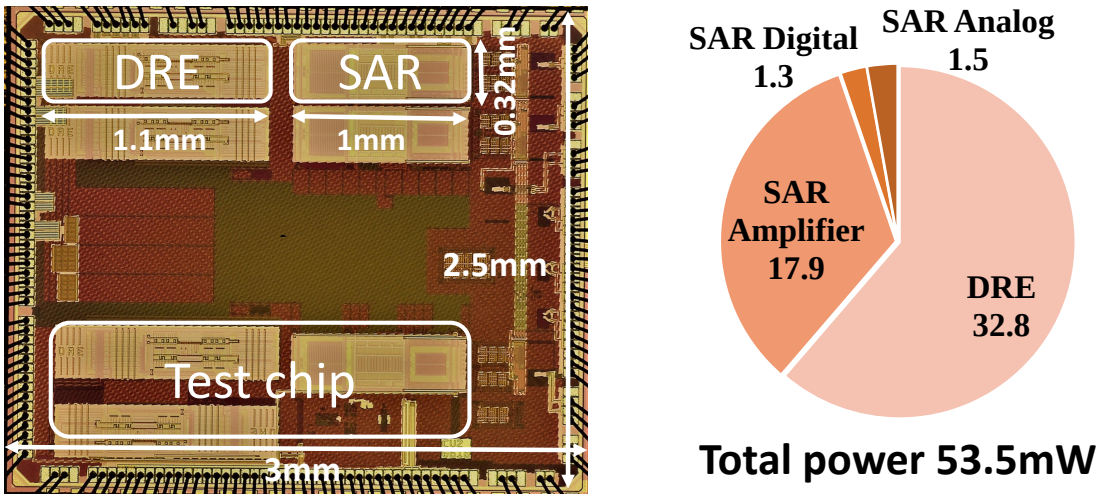
2.3.3 Clock Generation Unit

The clock generator consists of two NOR gates to generate the non-overlapping ϕ_S and ϕ_H clocks (Fig. 2.7(d)). An additional delay block is used before ϕ_S to generate ϕ_{SAdv}. The non-overlapping ϕ_{ASD} proposed for the DRE is generated using a D-flipflop. ϕ_{ASD} is enabled after ϕ_S goes down, and gets reset after a fixed amount of delay $4 * D1$. The output of ϕ_{ASD} is included in the loop with NOR gate to ensure non-overlap with ϕ_H.

2.3.4 12bit SAR[5]

A two-stage SAR amplifier resolving six bits in the first stage and ten-bits in the next stage is used as the backend ADC. Two bits are overlapping, and the last two bits are used for calibration only

[5]This block was designed at UT Austin by Chen-Kai Hsu under the guidance of Professor Nan Sun



(a) (b)

Figure 2.9: Die photo and power breakdown for the DRE-SAR system

resulting in a 12bit resolution ADC. The residue amplifier is a telescopic folded cascode with gain boosting. Since an amplification factor of 8x is used, the output swing requirements are not difficult to meet. However, the second stage capacitance needs to be large, and the amplifier needs to have a high UGB to ensure fast settling of DAC. This is required to meet the radiation-hardness criteria that the minimum capacitance is limited to 10fF, and the digital logic needs to be triple-redundant. This results in much larger power consumption for the SAR architecture used here compared to the traditional architectures. Foreground gain calibration is used to calibrate SAR offline.

2.4 Measurement Results

A prototype ADC chip was designed in 65nm LP technology (Fig. 2.9(a)) operating at 40MSPS and consuming 53.5mW power at a supply voltage of 1.2V. The power breakdown includes 32.8mW

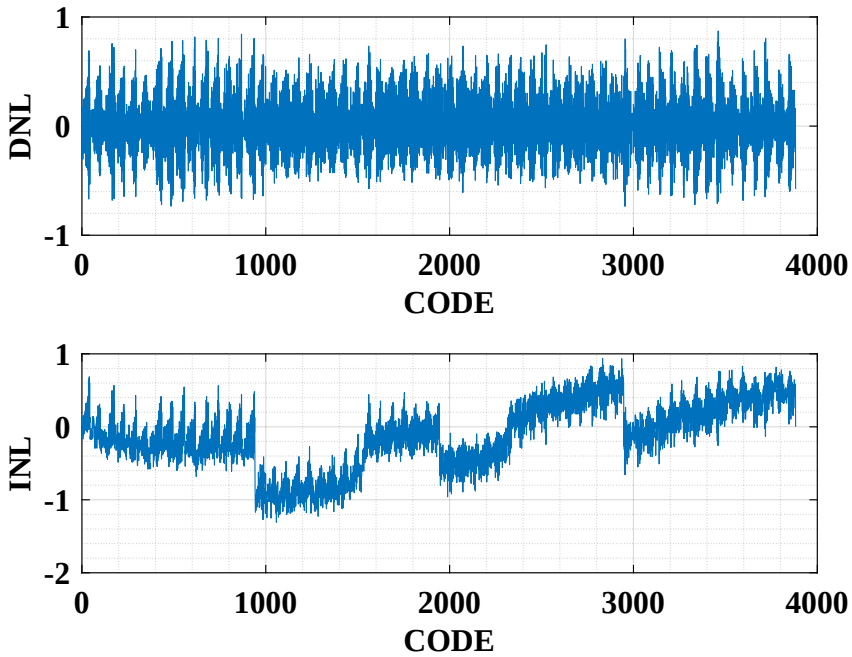


Figure 2.10: DNL and INL measurements for the DRE in 1x mode followed by SAR ADC.

in DRE amplifier, 17.9mW in SAR amplifier, and a total of 2.8mW in other SAR analog, digital and clock circuits (Fig. 2.9(b)).

Static measurement of the chip is done by providing a very low-frequency sine wave at -1dBFS amplitude to the chip. When configured in a forced 1x mode, the measured DNL and INL of DRE followed by SAR architecture are +0.87,-0.74, and +0.94,-1.31 ADC counts at a 12bit resolution (Fig. 2.10).

The dynamic performance of the chip is measured using a Keithly 3390 arbitrary waveform generator providing a single-ended input to a 6dB attenuator followed by a bandpass filter to provide a clean single tone frequency. The filter output goes to a TI THS4509 amplifier that amplifies and acts as a buffer for driving the DRE-SAR prototype. SAR data is collected using a Stratix FPGA board and processed in MATLAB in computer. An attenuator is used in the front end to

suppress the source noise by providing a larger signal from the source without saturating the DRE input. The bandpass filter is changed for every input frequency.

Auto gain (AG) mode is used in DRE to enable on-the-fly gain selection on a sample-by-sample basis. Measurement results for DRE in AG mode for three input frequencies as a function of input voltage is shown in Fig. 2.11. At low input voltage, all the samples use the 4x gain path, and the SNDR increases at 20dB/decade slope. Since a single gain path is being used, enabling or disabling ϕ_{ASD} does not matter. After a certain threshold, some of the sine wave samples start using 1x gain path as well. The SNDR plot follows results from 1x path results and continues to grow at 20dB per decade if the ϕ_{ASD} is enabled. If disabled, a significant drop in SNDR, which is frequency-dependent is observed, as predicted by (2.1).

It is not possible to use the above setup to measure input dynamic range (IDR) of the system because the amplifier noise dominates. The Keithly signal generator is directly used to drive the chip using an on-board balun for this measurement. Due to driving capabilities, it is difficult to use this setup for higher input amplitudes, so only measurements for lower input amplitudes are shown in Fig. 2.11 indicated by without amplifier case. An IDR of 80.6dB is achieved throughout different input frequencies.

The output spectrum for a low-frequency and Nyquist frequency signal at -1dBFS when measured for forced 1x and AG modes with ϕ_{ASD} enabled are shown in Fig. 2.12. Compared to forced 1x mode, AG mode results have higher harmonic content, particularly at higher frequencies resulting in SDR comparable to SNR. SNDR reduction compared to 1x case is less than a dB at low frequency to about 2.3dB near Nyquist frequency.

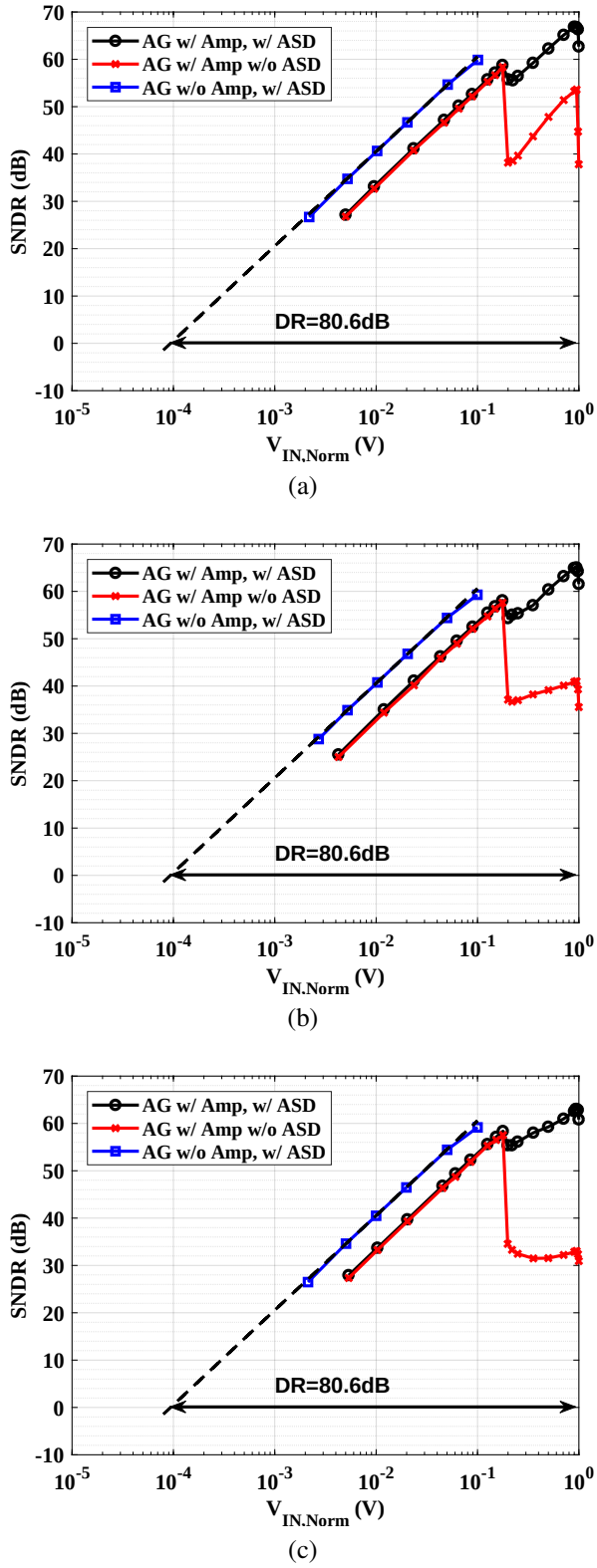


Figure 2.11: Measured SNDR and DR results with and without ϕ_{ASD} clock for DRE when measured at input frequency near (a) 1MHz, (b) 8MHz, and (c) 19.5MHz sampled at 40MSPS.

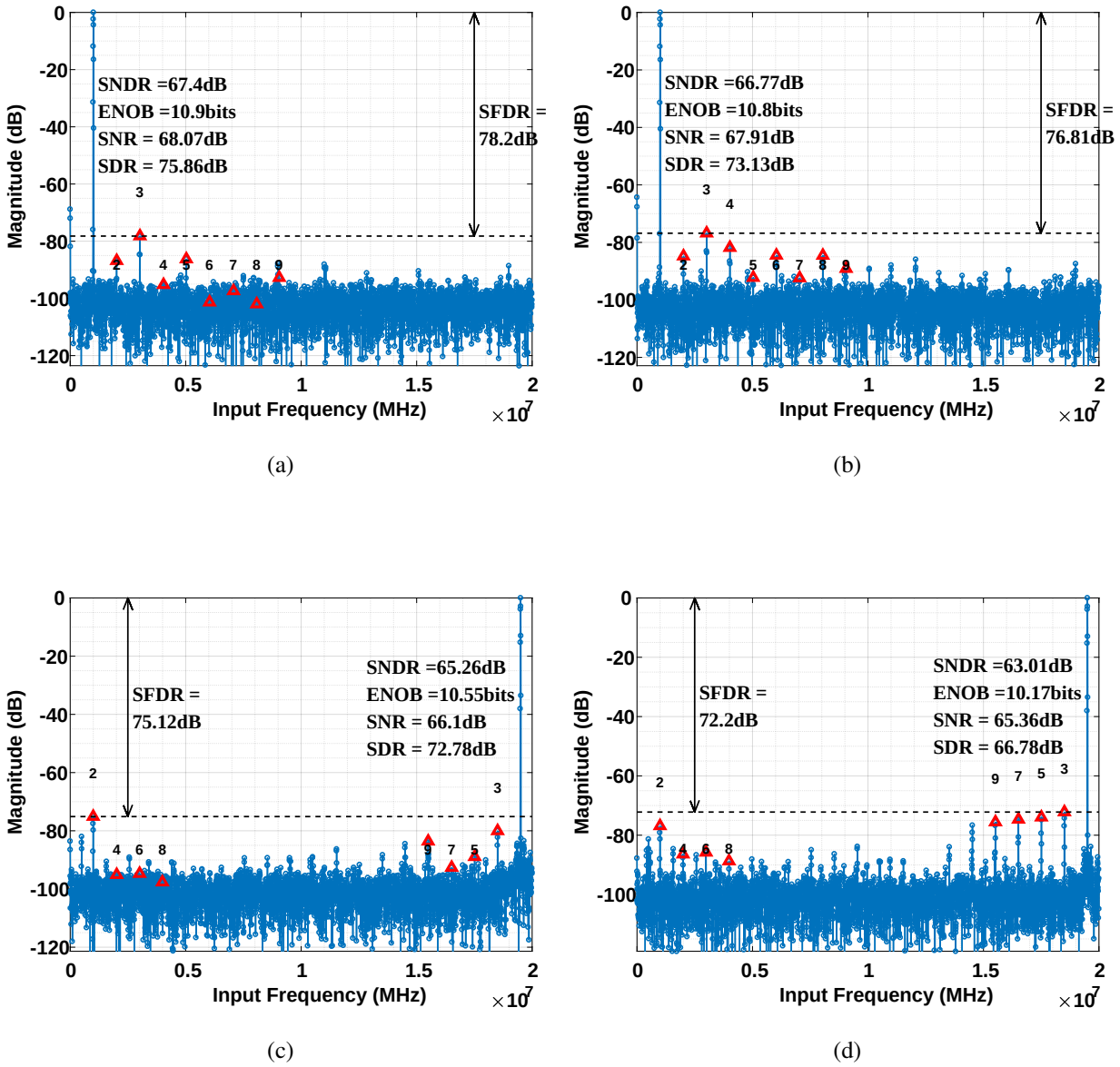


Figure 2.12: FFT plot for 1x and AG at (a), (b) low frequency, and (c), (d) Nyquist frequency.

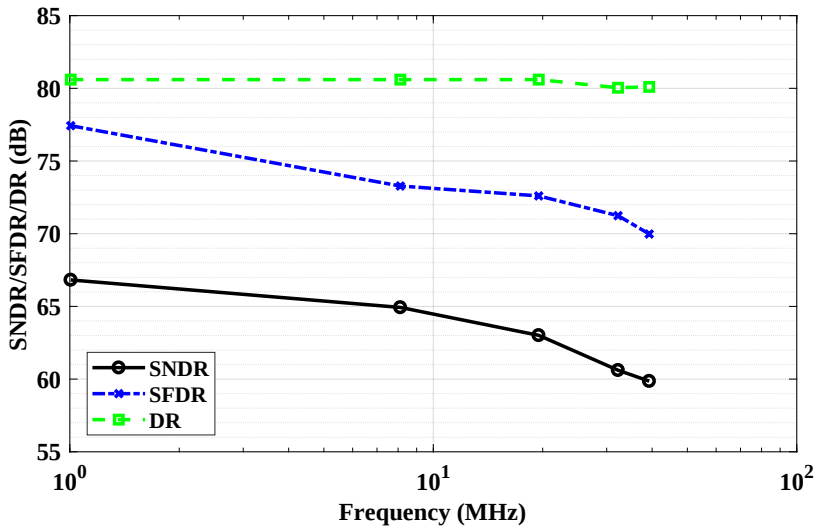
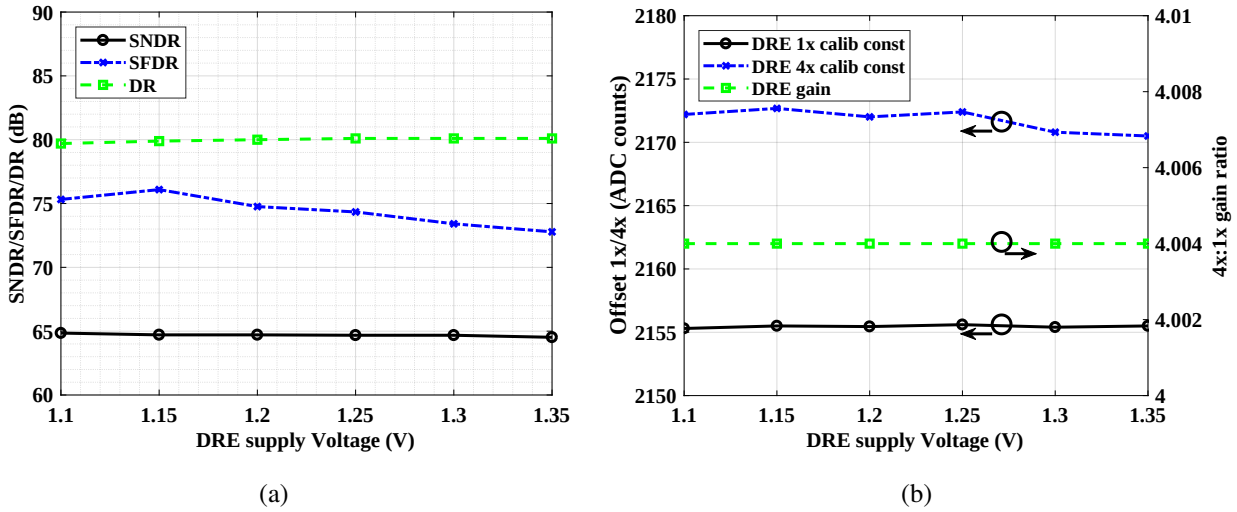


Figure 2.13: Measured SNDR, SFDR and input DR across input frequency.

Input frequency sweep results for AG mode measured at -1dBFS are shown in Fig. 2.13. A gradual reduction in peak SNDR and SFDR values is seen. Frequencies below Nyquist have same settings and calibration factor. For frequencies above Nyquist, (a) switching threshold from 4x to 1x is reduced to avoid saturation, (b) the gain calibration factor is also lowered from 4 to 3.9. With a calibration factor of 4.0 for higher than Nyquist frequencies, SNDR is reduced by 4dB-5dB. Therefore, AG mode, works best if the input frequency is limited below Nyquist frequency. Since IDR uses samples only from 4x gain, it has very low frequency dependence.

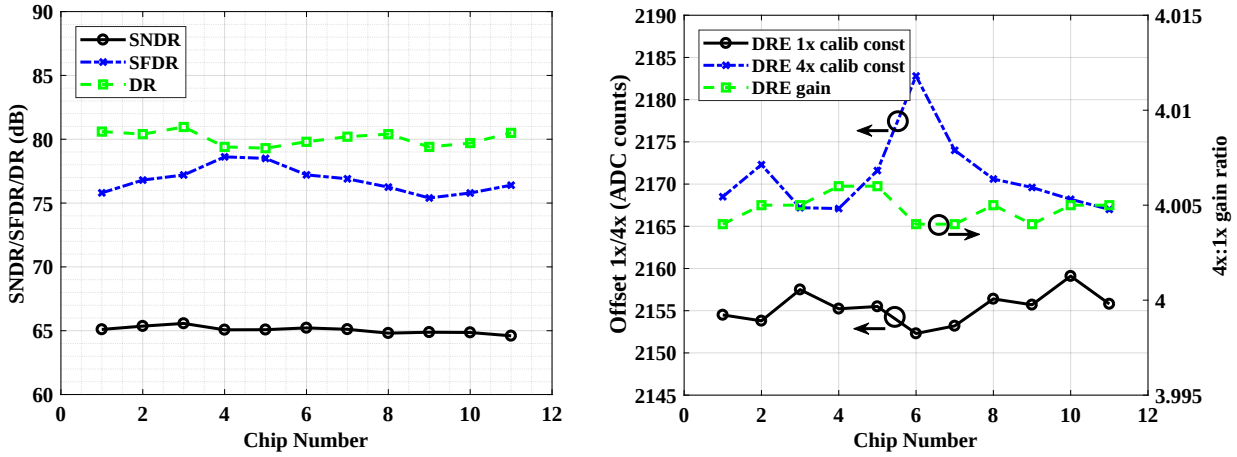
A stable SNDR, SFDR, and DR plot is obtained with the DRE supply variation as shown in Fig. 2.14(a) and reasonably constant calibration constants in Fig. 2.14(b) indicating that the DRE is robust to supply voltage variation at low frequencies. This robustness is expected thanks to the fully differential nature of the DRE amplifier used during the sample-and-hold operation.

DRE performance and calibration constant results measured for different chips are shown in



(a) (b)

Figure 2.14: (a) Variation of SNDR, SFDR, DR across DRE supply voltage $V_{DD,DRE}$ plotted for input frequency close to 8MHz for 40MSPS operation. (b) Variation of DRE coefficients across $V_{DD,DRE}$. Performance parameters and calibration coefficients are almost constant across supply voltage variation.



(a) (b)

Figure 2.15: (a) Variation of SNDR, SFDR, DR across multiple chips measured for input frequency close to 8MHz for 40MSPS operation. Less than 1dB variation observed in SNDR and DR. (b) Variation of DRE coefficients across chips. Gain is consistent across different chips.

Fig. 2.15. Less than 1dB variation in SNDR and DR indicates a robust design methodology. Offset calibration constant variation is expected due to random input-referred mismatch for the amplifier. Since 4x offset consists of additional gain compared to 1x offset, its variation is higher. Less than 0.05% variation is observed for gain calibration constant thanks to the large size of the sampling capacitor.

2.5 Comparison to the State of the Art

The proposed DRE architecture enhances the input dynamic range of a 12bit SAR to 80.6dB with 66.8dB peak SNDR at low frequency and 63.01dB peak SNDR at Nyquist frequency when operating at 40MSPS. Compared to recent works [32, 36–38], this work achieves the maximum input dynamic range. The FOM_{DR} is lower than other architectures because of higher power consumption in the backend SAR. The additional power is needed to meet the radiation hardness requirement, as explained in Section 2.1. The DRE architecture if combined with a traditional backend SAR architecture, therefore, has the potential to achieve a FOM comparable to other designs.

Compared to earlier designs [31, 39, 40], DRE achieves better efficiency (fJ/conv step) and FOM_{DR}, except for [39], despite operating at a low supply voltage of 1.2V. Thanks to technology scaling, this work also achieves the least area compared to other designs except for [32].

	This work	Xu '19	Hershberg '13	Hershberg '12	Brunsilius '11	Hurrell '10	Devarajan '09	Shu '09
Conf./Journal		JSSC	VLSI	ISSCC	ISSCC	JSSC	ISSCC	JSSC
Architecture	DRE+SAR	Split-SAR	Pipeline Ring Ampilfier	Pipeline Ring Ampilfier	Pipeline ADC	Pipeline+SAR	Pipeline	MultiGain+ Pipeline
Technology	65nm	65nm	180nm	180nm	180nm	0.5/0.25µm	180nm	180nm
Resolution	12-14bit	14bit	15bit	15bit	16bit	18bit	16bit	10-15bit
Supply (V)	1.2	1.2/1.8	1.2	1.3	1.8	2.5/5	1.8	1.8
Vpp diff (V)	2	N/A	2.4	2.5	N/A	8.2	2	2.4
fs (MSPS)	40	40	20	20	80	12.5	125	60
Peak SNDR (Nyquist) (dB)	63.01	74.4	75.9	76.8	75	80	77	59.5
Input DR (dB)	80.6	78.7	76.1	77.3	77	93	79.1	80
Power (mW)	53.5	22.2	2.96	5.1	100	105	385	300[&]
FOM_{DR}*	169.3	171.3	174.4	173.2	166.0	173.8	164.2	163.0
fJ/conv step (using DR)[#]	152.7	78.9	28.4	42.6	216.0	230.1	418.0	611.8
Area (mm^2)	0.73	0.34	1.98	1.98	9.9	6	10	6

* DR+10.log(fs/P*W/Hz); [#] P/(fs*2^$ENOB_{DR}$); $ENOB_{DR}$ = (DR-1.76)/6.02 [&] Includes driver and calibration power

Figure 2.16: Comparison to the state of the art ADCs with input DR greater than 76dB and operating at sampling rate higher than 10MSPS.

2.6 Chapter Summary

This chapter presents a voltage-domain technique to reduce power consumption of an ADC operating at a supply voltage of 1.2V, while increasing the input DR. This is achieved by leveraging application specific requirements to tradeoff instantaneous SNDR with reduced reference buffer power consumption. An on-the-fly gain selection based Dynamic-Range Enhancer is presented to achieve 80.6dB input DR with upto 66.8dB peak SNDR, when operating at 40MSPS at a supply voltage of 1.2V.

Chapter 3

Scaling-Friendly Time-Domain Circuits for Analog Circuit Design

Traditional voltage-domain analog circuits are facing challenges in the scaled technology, as discussed in Chapter 1, due to the reduced supply voltage and intrinsic voltage gain of the transistors. Several time-domain circuits (TDCs) have been explored in the past decade as a scaling-friendly alternative to the voltage-domain circuits. In this chapter, we discuss the broad classification of TDCs, their state-of-the-art examples, and some practical implementation challenges.

3.1 Classification of Time-domain Circuits

A time-domain circuit either represents or processes information in time-domain, thus benefiting from the increased transistor speed that comes with technology scaling. Pulse width modulation (PWM) is the most common time-domain representation of a signal, and forms the core of most of the time-domain circuits. A PWM signal contains information in the pulse width instead of voltage, and hence avoids the power wall penalty with supply voltage scaling [2].

PWM signal has been used in the design of Class-D amplifiers for a very long time [41]. However, supply voltage reduction resulting in reduced voltage swings, and improvement in transistor

speeds leading to shorter pulse-width duration have made the use of time-domain representation an attractive alternative to voltage-domain signal representation in the past decade.

Circuit design in time-domain has two components: first, generation of PWM, and second, use of PWM (Fig. 3.1). Two commonly used methods of generating PWM are: (i) Comparing the input signal to a triangle waveform [6, 42, 43], and (b) To use a VCO with a phase detector (PD) (Fig. 3.2).

In the first method, the input signal is sliced with a triangle wave using a comparator to produce a PWM signal. This method is traditionally used (see [42]) and is not discussed further. In the second method, the VCO converts the input voltage information to the frequency which is compared by the PD against a constant frequency signal to provide a PWM output. Either an XOR-based PD or a phase-frequency detector (PFD) can be used for phase comparison. Differential input signals can be given to two VCOs to generate differential frequencies with respect to the common-mode voltage frequency for the PD input to eliminate the constant frequency signal. The VCO-PD combination provides perfect integration of the input signal during frequency-to-phase conversion in the process of PWM generation. This ”free” integration property is exploited in several applications to either provide a high-DC gain, use it as an integrator or achieve first-order noise shaping.

The PWM thus generated can now be used in an either digital or analog way (Fig. 3.2). To generate digital code from the PWM, we can provide the PWM signal to a VCO and count the number of pulses in a given period. Alternately, we can also combine both the generation and use of a PWM by providing the input to a VCO, and directly counting the number of pulses arriving in a given period. A circuit that performs this function is called a VCO-based quantizer, and it also

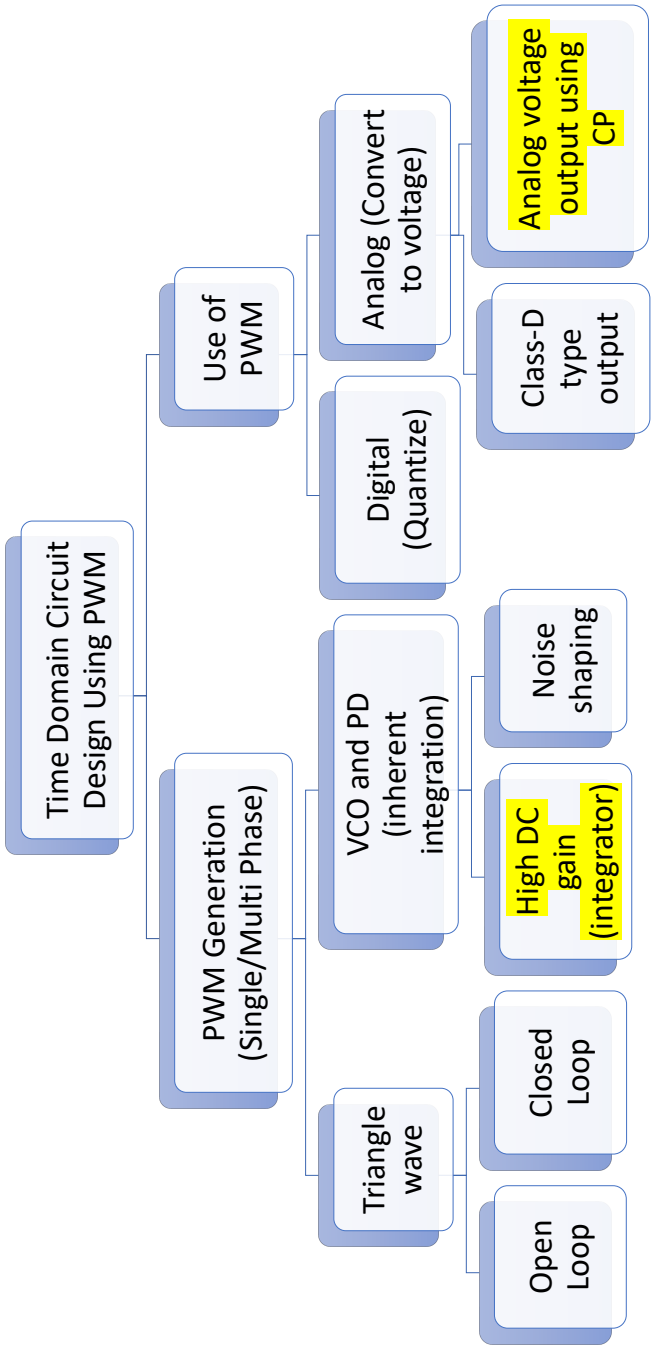


Figure 3.1: Broad classification of the state-of-the-art time-domain circuits based on generation and use of PWM signal. This thesis focuses on generating the PWM using a VCO and a PD taking advantage of high DC gain thus obtained, and converting the PWM back into voltage domaing using a charge pump (CP) followed by a load.

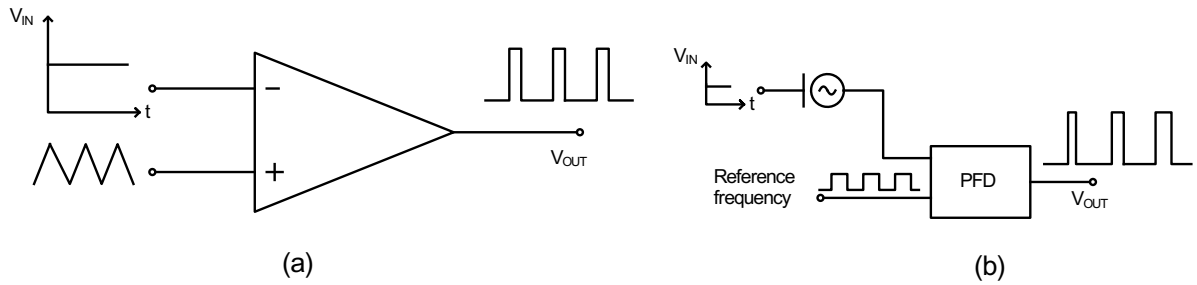


Figure 3.2: (a) Traditional method of PWM generation by comparing the input signal with a triangle wave signal (b) PWM generation using a VCO followed by a phase detetctor. Input voltage signal is converted to frequency-domain, which is then compared to a reference frequency to produce PWM signal.

provides first-order noise shaping property in addition to the digitization and is discussed further in Section 3.2.1.

To use the PWM in an analog fashion, the PWM can be used to either drive inverters and take class-D type output with rail-to-rail swings or to drive a charge pump followed by a load to convert the signal back to voltage domain. The former approach usually requires multi-level signals, which can then be averaged using resistors to provide analog value for feedback. The latter approach still requires V_{Dsat} voltage drop and needs modification before its circuits can be scaled down with supply voltage.

3.2 Examples of Time-Domain Circuits

Based on the TDC classification, we now present some examples of the state-of-the-art time-domain circuits (SOA-TDCs)[1].

[1]This list is not comprehensive, and is meant to illustrate the versatility of the proposed classification.

3.2.1 VCO-based Quantizers for Continuous-Time Delta-Sigma Modulators

Continuous-time delta-sigma modulators (CT-DSMs) have emerged as an attractive alternative to the traditional digital DSMs in the past two decades because of their inherent anti-aliasing property [44]. The block diagram of a generic CT-DSM consisting of a front-end filter followed by a clocked quantizer with a digital-to-analog converter (DAC) in feedback is shown in Fig. 3.3 [4]. Due to supply voltage scaling, voltage-domain clocked multi-bit quantizers face the challenge of reduced voltage differences between quantization levels. This results in issues of metastability and reduced voltage margin for the comparators, thus requiring low-offset high-power comparators [4, 45, 46]. Scaling-friendly VCO-based quantizers have been used in the past decade to overcome these challenges [4, 5, 47–56].

A VCO-based quantizer consists of a front-end VCO followed by a phase quantizer and a digital differentiator (Fig. 3.4). The VCO converts input voltage-domain information to frequency-domain, which is then sampled by the phase quantizer, which acts as a sampling network. The phase quantizer captures the total number of transitions of the VCO output. The digital differentiator subtracts the accumulated transitions till the current cycle from those accumulated till the previous cycle, thus providing the VCO transitions that happened in a single period T of the sampling frequency [5, 47]. Intuitively, counting operation is equivalent to digitizing the pulse width of the PWM. The VCO-based quantizer is thus equivalent to generating a PWM signal and then digitizing its pulse width. However, there is no intermediate point at which a PWM signal is produced due to the combined sampling and pulse counting operation. Note that the quantization error information is retained in the phase of the VCO, and is carried over to the next cycle. Therefore,

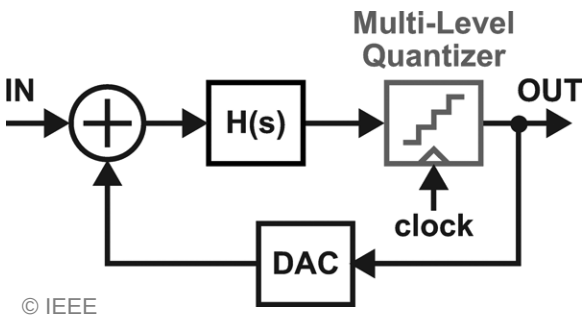


Figure 3.3: Basic CT-DSM model [4].

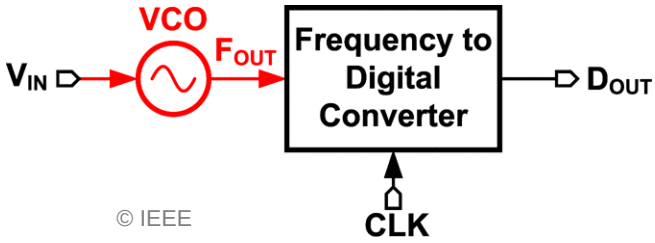


Figure 3.4: Block diagram of a VCO-based quantizer [5]

there is no loss of information due to quantization, and this property provides first-order [47]. There are several benefits of using a VCO-based quantizer. First, creating a multi-bit quantizer requires only increasing the number of VCO stages and the digital circuit used for sampling and comparison. There are no metastability and voltage swing reduction issues like those faced by the voltage-domain quantizers. Second, technology scaling reduces the gate delays, which improves the performance of the quantizers. Third, most of the components used are digital, thus easing the design effort. Fourth, the first-order front-end integration due to the VCO reduces the order of the filter preceding the quantizer by one, thereby providing power savings. Fifth, the dig-

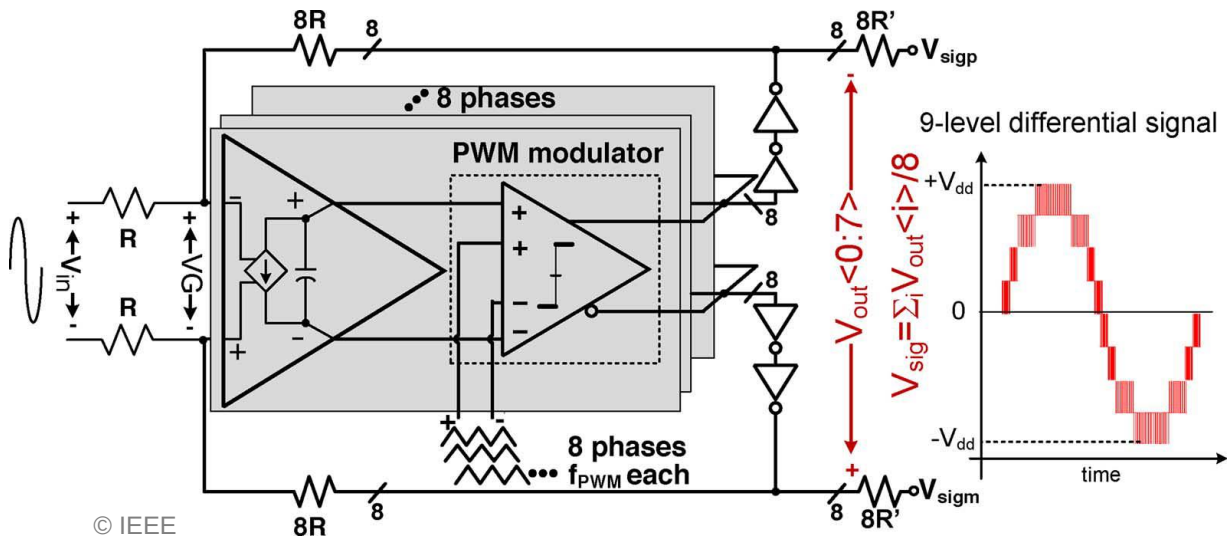


Figure 3.5: Schematic diagram of a switched-mode operational amplifier (SMOA) consisting of a traditional gm cell as the first stage followed by a fully digital second stage driven by a PWM generated using a triangle waveform [6].

ital differentiator at the end of the quantizer provides first-order noise shaping of the quantization error [4, 5, 45–56].

Despite these advantages, the non-linear voltage-to-frequency conversion curve of the VCO limits the performance of an open loop VCO-based quantizer. Several SOA CT-DSMs therefore provide calibration scheme [48, 50, 53], MASH architecture [5, 53], dynamic element matching techniques [4, 47, 52, 55] for reducing impact of DAC mismatch, and higher order filtering [4, 5, 47, 49, 56] to overcome this challenge. Overall, VCO-based quantizers type of time-domain circuits show excellent promise with technology scaling and provide exciting research opportunities.

Figure 3.6: Waveform at the output of (a) first stage, and (b) second stage of an SMOA [6].

3.2.2 Switched-Mode Operational Amplifier

Another scaling-friendly circuit is a switched-mode operational amplifier (SMOA) (Fig. 3.5) [6] consisting of two stages, with the first stage designed using a traditional voltage-domain amplifier. The first stage output does not need to swing to the full-scale voltage due to the gain in the second stage. Thus it overcomes the challenge of reduced voltage swing at lower supply voltages. The second stage of SMOA consists of inverters and is driven from a PWM signal derived by comparing the output of the first stage with a triangle wave (Fig. 3.6). The feedback is provided by averaging the multi-phase outputs using resistors, thus reducing the amount of signal swing developed at the virtual ground node. Thanks to the highly digital second stage, SMOA is scaling-friendly, has a rail-to-rail output voltage, provides low-output impedance, and has an easily replicable output signal.

In the context of the classification presented in Section 3.1, SMOA uses the traditional triangle waveform to generate the PWM signal, which is then used to drive inverters (Class-D type structures) with multi-phase implementation used with resistors to generate the average analog-output voltage.

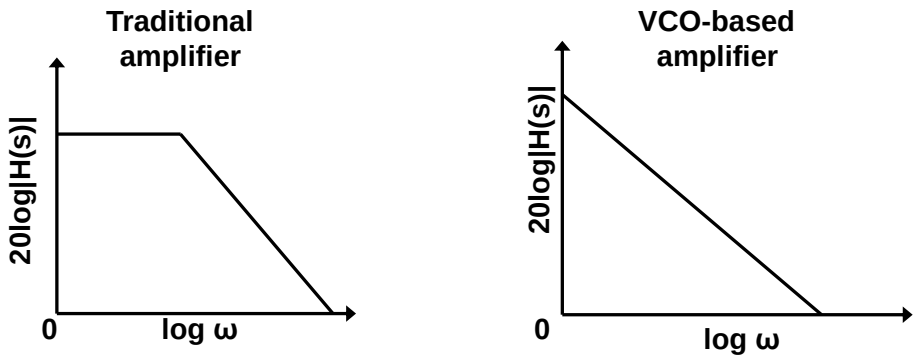


Figure 3.7: (a) Traditional amplifier has a finite DC gain dependent on the topology and the intrinsic voltage gain of the devices used. (b) The VCO-based amplifier achieves infinite DC gain from input voltage to output phase due to perfect integration during frequency to phase conversion [7].

3.2.3 VCO-based Amplifiers

The integrating nature of the VCO from input voltage to the output phase can be used to create an amplifier. Compared to a traditional voltage-domain amplifier, this integration does not rely on intrinsic voltage gain of the devices, and is, therefore, able to provide an infinite theoretical gain (Fig. 3.7) [7, 57–59]. Several architectures in literature use it to create ring-oscillator-based integrators, VCO-based opamps, and VCO-based OTAs, which can be broadly classified as VCO-based amplifiers. The basic block diagram of a VCO-OTA is similar to that of a PLL and consists of a VCO followed by a phase-frequency detector (PFD) and a charge pump (CP) (Fig. 3.8(b)). The VCO generates a signal with a frequency proportional to the input voltage. The PFD detects the phase of the VCO output relative to the phase of a constant reference frequency. The CP provides a current proportional to the PFD duty cycle output on the load to generate the output voltage. If a differential input voltage is used, it is possible to eliminate the reference frequency by generating the two signals for the PFD using two VCOs, which produces a differential signal in the frequency

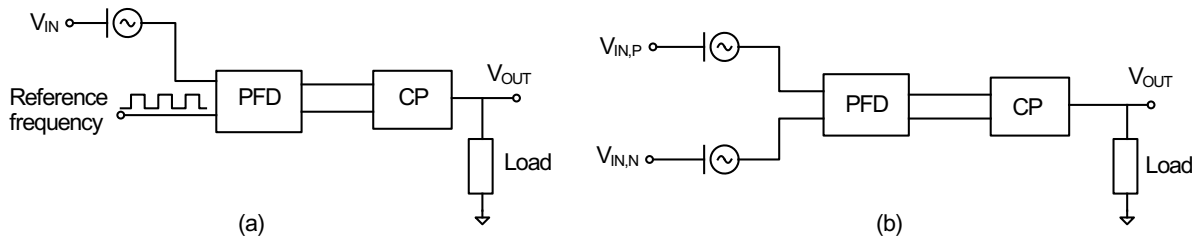


Figure 3.8: Block diagram of a (a) single ended, and (b) differential VCO-OTA.

domain (Fig. 3.8(b)). This means if the frequency of one VCO increases slightly, the frequency of the other VCO decreases by the same amount for a differential input signal and a linear voltage-to-frequency transfer curve of the VCO if the two VCOs are matched. This doubles the small-signal gain and eliminates the need to have the free-running frequency of the VCO within the locking range of the reference frequency, thus reducing the overhead of controlling VCO frequency over PVT variations and in the presence of parasitics.

The integrating action of the VCO provides the first pole of the VCO-based amplifier at DC. A second pole exists at the output of the amplifier, thus limiting the maximum allowed load capacitance [57,58]. Several passive [7,59,60] and active [61–63] zero-compensation solutions exist in literature to achieve stability when the amplifier is placed in feedback. VCO-based amplifiers have been demonstrated in a range of applications including filters, DC-DC converters, voltage regulators, phase-locked loops and current-mode receivers [7,57–67].

Revisiting the proposed time-domain circuits classification in Fig. 3.1, VCO-based amplifiers fall under the category of generating a PWM signal at the output of the PFD using a VCO and benefit from the high DC gain property of the system. They then use the PWM in an analog fashion and examples of both class-D type approach [57,58], and converting back to voltage using a CP [7,59–67] are available in literature.

3.3 Practical Challenges in Designing Time-Domain Circuits

TDCs offer numerous benefits with technology scaling. However, they come with some practical challenges.

First, many circuit parameters such as the center frequency of the VCO and the voltage-to-frequency gain of the VCO (K_{VCO}) vary with the process, supply voltage, and temperature (PVT). TDCs, therefore, need robust circuit design and calibration to be useful at a large scale.

Second, the circuits which provide analog output voltage contain spurs near multiples of VCO frequency. Therefore, they need further filtering to remove the high-frequency content before further processing. In case of multi-phase architecture where the spurs are produced at much higher frequencies, phase mismatch requires careful calibration to cancel out spurs at other multiples of oscillation frequency altogether.

Third, TDCs generally contain some components such as gates and delays, which are easier to analyze in the digital domain, and some other components such as analog filter, charge pump and load, which are better handled in the analog domain. Due to the mixed-signal nature of the circuit, it is challenging to model the entire loop dynamics of the system accurately, and one has to often rely on simplifying assumptions which prevent aggressive circuit design.

Fourth, unlike traditional amplifiers, which are always stable if the loop-bandwidth reduces, VCO-based amplifiers have a limited frequency range of stability, as is discussed in later chapters. Therefore stability of the latter is more of a concern compared to the former and needs careful analysis.

Fifth, finite locking range of the PD due to phase rollover at regular intervals of 2π requires careful design, analysis, and verification of the circuits to prevent cycle slipping.

Sixth, for the circuits containing two VCOs, the effect of frequency pulling is not understood. Also, issues such as substrate coupling are not modeled accurately in simulation software. Therefore, one has to rely on conservative estimates or go through extensive modeling to gain confidence in simulation results.

And seventh, current simulation tools are not optimized for time-domain circuits. The presence of two VCOs or a VCO not locked with a fixed input frequency often results in convergence issues in periodic steady-state simulations. One often has to rely on time-consuming transient simulations. In a fast-paced industry where time is of crucial importance, and an in-depth verification is a must, lack of quick iteration prevents the widespread use of TDCs.

3.4 Modeling, Analysis, and Applications of VCO-based OTAs

From the different categories of time-domain circuits presented in Fig. 3.1, the remaining chapters in this thesis expand on the specific category of VCO-based OTAs (VCO-OTAs) that generate PWM using VCO and PFD followed by conversion back to voltage using a CP dumping current on the load impedance.

We first discuss the small-signal discrete-time modeling of a VCO-OTA based on the difference between the zero-crossings of the two VCOs used in the system. Unlike the phase-domain model which requires input-frequency and the unity-gain bandwidth of the closed-loop system to be much less than the VCO frequency, this model captures the complete system response for an arbitrary

input frequency, even as the VCO free-running frequency approaches the closed-loop unity-gain bandwidth of the system.

Next, we present the application of VCO-OTAs as baseband trans-impedance amplifiers for current mode receivers and demonstrate their benefits over other scaling-friendly inverter-based amplifiers.

We end the thesis with other applications and design techniques for VCO-OTAs showcasing a prototype for a VCO-OTA used in a low-dropout regulator, another prototype demonstrating power-linearity tradeoff in a VCO-OTA, and a discussion on the design of VCO-OTAs at 0.2V supply.

Chapter 4

Zero-Crossings-based Time-Domain Model for VCO-OTAs

In this chapter, we present a model of Voltage-Controlled-Oscillator based Operational Transconductance Amplifiers (VCO-OTAs) based on the time difference between the zero-crossings of the two VCOs used in the system. The proposed Zero-Crossing-Time-Difference Model (ZCTDM) provides a linear, discrete-time analysis for VCO-OTA based feedback systems. The ZCTDM can predict the phase-margin degradation and the frequency response of the closed-loop system, as the system update rate f_0 approaches the unity-gain bandwidth, f_{UGB}.

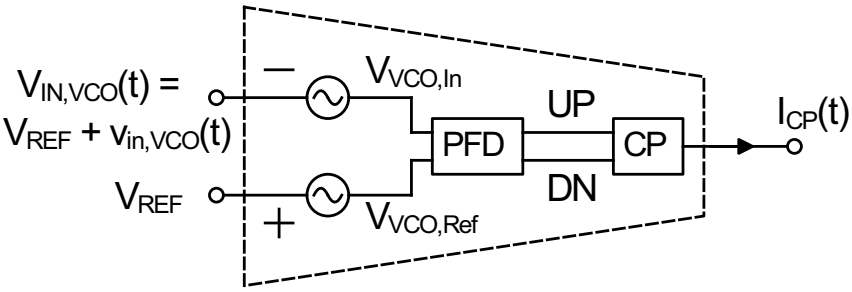
The ZCTDM is used to model two examples of a VCO-OTA architecture in an inverting-amplifier configuration. It accurately predicts the loop dynamics of the two systems where the continuous-time phase-domain model (CT-PDM) and the impulse invariant transform model (IITM) fail, particularly as the system update rate f_0 approaches f_{UGB}, as verified by the behavioral level simulations. The two examples covered in this chapter represent the systems where the output-voltage discharge rate is much less than the system update rate. Guidelines are provided for modeling systems where the reverse is true.

4.1 Background

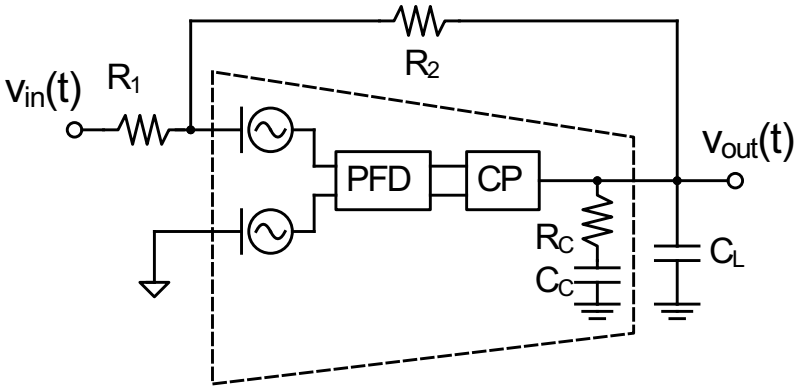
Operational Transconductance Amplifiers (OTAs) form the core of many analog and mixed-signal circuits such as filters, RF modulators, DC-DC converters, and analog-to-digital converters (ADCs) [54, 55, 57, 58, 63, 65]. With technology scaling over the past few decades, supply voltage and intrinsic gain of a transistor have reduced, while the transistor speed has increased [2]. For analog circuits, especially OTAs, a high intrinsic gain of the transistor is required to provide a high DC gain. Stacking of transistors has become increasingly difficult with scaling in supply voltage, making it necessary to use multi-stage OTAs to provide a high DC gain. However, achieving a high bandwidth while maintaining stability becomes difficult in such OTAs.

Voltage Controlled Oscillator (VCO) based OTAs (VCO-OTAs) (Fig. 4.1(a)) have emerged as an alternative to the traditional amplifiers and provide a high DC gain owing to the frequency-to-phase conversion. They benefit from the technology scaling because of the digital nature of their blocks [57–60, 63, 66]. VCO-OTAs have been demonstrated in several applications such as filters, receivers, DC-DC converters, low-dropout regulators, and ADCs [7, 54, 55, 57–60, 63–68].

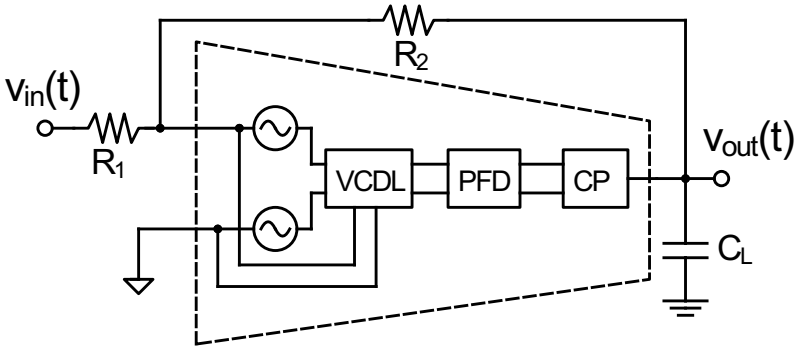
The core building blocks of a VCO-OTA (Fig. 4.1(a)) and a phase-locked loop (PLL) are the same, namely the VCO, the phase-frequency detector (PFD) and the charge pump (CP). Therefore, the continuous-time phase-domain model (CT-PDM), which is commonly used to model PLLs has been used to model VCO-OTAs as well [57–60, 63, 66]. CT-PDM provides a simple and intuitive linear-time invariant (LTI) model of a closed-loop system based on a VCO-OTA. The continuous-time assumption of an inherently discrete-time VCO-OTA, however, requires the center frequency



(a)



(b)



(c)

Figure 4.1: (a) Block diagram of a VCO-OTA and its application in an inverting amplifier configuration using (b) A passive-zero-compensated VCO-OTA, and (c) An active-zero-compensated VCO-OTA. Accurate discrete-time stability analysis for the closed-loop systems in (b) and (c) is challenging because the loaded system has both discrete-time and continuous-time elements.

of the VCOs, f_0, to be much larger than the unity-gain bandwidth f_{UGB} of the feedback loop, leading to a conservative design.

A VCO-OTA system, similar to a Type-II PLL, requires an additional zero for stability. An example of a passive-zero-compensated and an active-zero-compensated VCO-OTA in an inverting amplifier configuration is shown in Fig. 4.1(b) and (c) respectively. To completely characterize the feedback-loop dynamics, discrete-time analysis of the VCO-OTA is essential. A loaded VCO-OTA closed-loop system (Fig. 4.1(b) and (c)), contains some blocks which can be easily represented in the discrete-time domain such as the VCO, the PFD and the CP, and other blocks which are easier to represent in the continuous-time domain, such as the output load, containing passive circuit elements. This increases the closed-loop system complexity and requires careful mixed-time domain analysis for the intermediate steps, before deriving the final discrete-time representation of the system.

The discrete-time stability model for a PLL, based on the impulse-invariant transform was proposed in [69]. However, the impulse-invariant-transform model (IITM) provides incorrect results for an active-zero compensated VCO-OTA architecture, as will be discussed in Section 4.6.2. State-space based analysis [70, 71] for a PLL provides accurate stability analysis, but is quite involved and non-intuitive. It therefore requires an elaborate analysis and provides limited insight when applying to different VCO-OTA architectures. PLL analysis using harmonic balance [8] offers more insight into system stability, but its direct application in VCO-OTA analysis is non-trivial. It also does not give information about the transient response of the system. In addition, none of the PLL analysis can be used to capture the dynamics of a VCO-OTA system completely

because the signal frequency at the input of the VCO, f_{IN} for a PLL is assumed to be always less than the loop bandwidth, which is not always true for a VCO-OTA. Many analyses further rely on representing the signal in the form of phase, which is an abstract quantity and difficult to measure, especially for oscillators which do not produce a sine wave such as ring oscillators.

This chapter presents a linear zero-crossing-time-difference model (ZCTDM) which discretizes the time difference Δt_{ZC} between the zero crossings of the two VCOs for each cycle to capture the discrete-time effects of the system. ZCTDM therefore predicts phase-margin degradation caused by the reduction of f_0 for a constant f_{UGB}. It also predicts the frequency response of the system beyond f_0. Two design examples have been analyzed using the ZCTDM and compared to the simulation results using behavioral models of the individual components of the VCO-OTA to illustrate the benefits of this model over CT-PDM and IITM. The mathematical models presented in this chapter focus on the systems where the output voltage discharge rate slower than the system update rate f_0. These systems cover most of the practical applications based on VCO-OTAs. Guidelines to model systems with discharge rate faster than f_0 are also presented for interested readers.

4.2 VCO-OTA Operation

The single-ended block diagram of a typical VCO-OTA consisting of two VCOs, a Phase-Frequency Detector (PFD) and a Charge Pump (CP) is shown in Fig. 4.1(a) [59,60] with the waveforms at different nodes of the VCO-OTA shown in Fig. 4.2. The frequency of the reference-VCO is assumed to be $f_0 = 1/T_0$ when a DC voltage of V_{REF} is applied at its input. When a small signal input

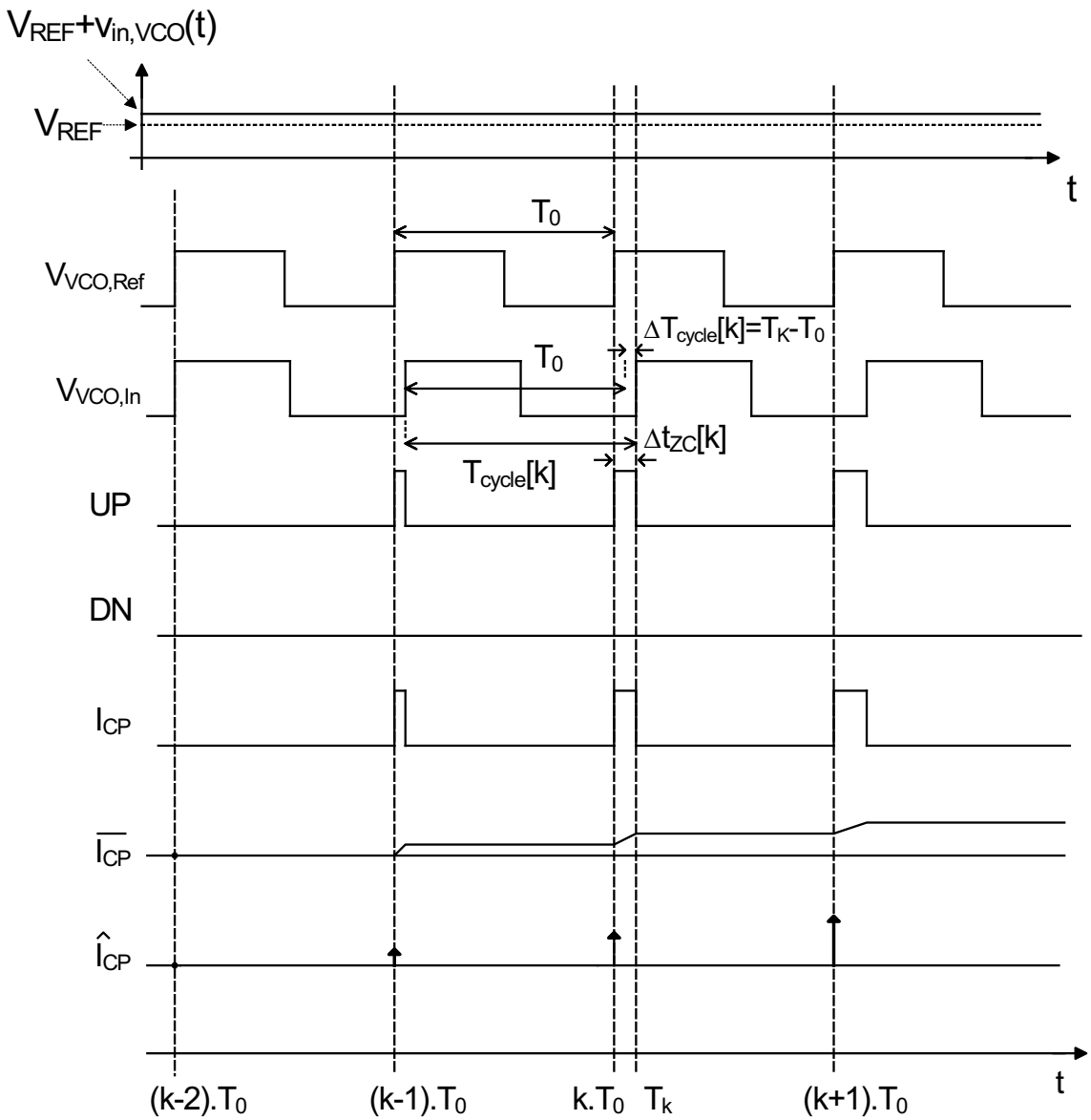


Figure 4.2: Waveforms at different points of a VCO-OTA and the definitions of T_k, $T_{cycle}[k]$, $\Delta t_{ZC}[k]$, $\Delta t_{cycle}[k]$ associated with the kth cycle of the reference-VCO, used to develop ZCTDM for the VCO-OTA.

voltage, $v_{in,VCO}(t)$, is applied to the input-VCO relative to the reference-VCO, the frequencies of the square waveforms produced at the output of the two VCOs are different. Based on the relative position of the rising edges of the two VCO outputs, the PFD produces UP or DN pulses. The CP then dumps an output current, I_{CP}, proportional to the difference between the UP and the DN pulses, into the load impedance, Z_L to generate the output voltage, V_{OUT}.

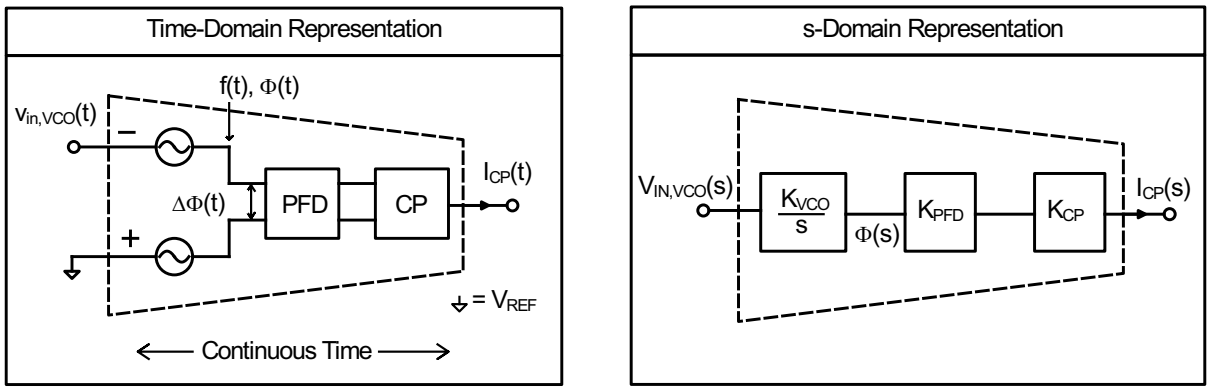
For a small DC input voltage, Fig. 4.2 indicates that the pulse width of I_{CP} increases with time. If the pulse width does not exceed the reference waveform period T_0, the average output current per cycle $\overline{I_{CP}}$ continues to increase because the error at the PFD output keeps accumulating, thus providing an infinite DC gain for the VCO-OTA in the open-loop. In a negative feedback application, such as in Fig. 4.1(b) and (c), the feedback corrects $v_{in,OTA}(t)$, thus preventing any cycle slipping, and locking the output frequencies of the two VCOs for a DC input.

4.3 Continuous-Time Phase-Domain Model (CT-PDM)

To find the frequency response of the VCO-OTA, we first develop the small signal model of the individual blocks. For the input-VCO, the instantaneous output frequency f_{VCO} can be modeled with:

$$f_{VCO}(t) = f_0 + K_{VCO} \cdot v_{in,VCO}(t) \tag{4.1}$$

where K_{VCO} is the change in the output frequency of the VCO per unit input voltage, expressed in Hz/V. The instantaneous phase of the VCO output, $\phi_{VCO}(t)$, is the integration of f_{VCO}. Assuming zero phase at time $t = 0$, $\phi_{VCO}(t)$ consists of a ramp corresponding to $2\pi f_0 t$ and an input dependent



(a) (b)

Figure 4.3: (a) Time-domain and (b) s-domain representation of the traditional continuous-time phase-domain model (CT-PDM) of a VCO-OTA.

small signal term $\Delta\phi(t)$ given by

$$\Delta\phi(t) = \int_0^t 2\pi K_{VCO} \cdot v_{in,VCO}(t)dt \tag{4.2}$$

The average output current [1] $\overline{I_{CP}}(t)$, is proportional to $\Delta\phi(t)$ and is given by:

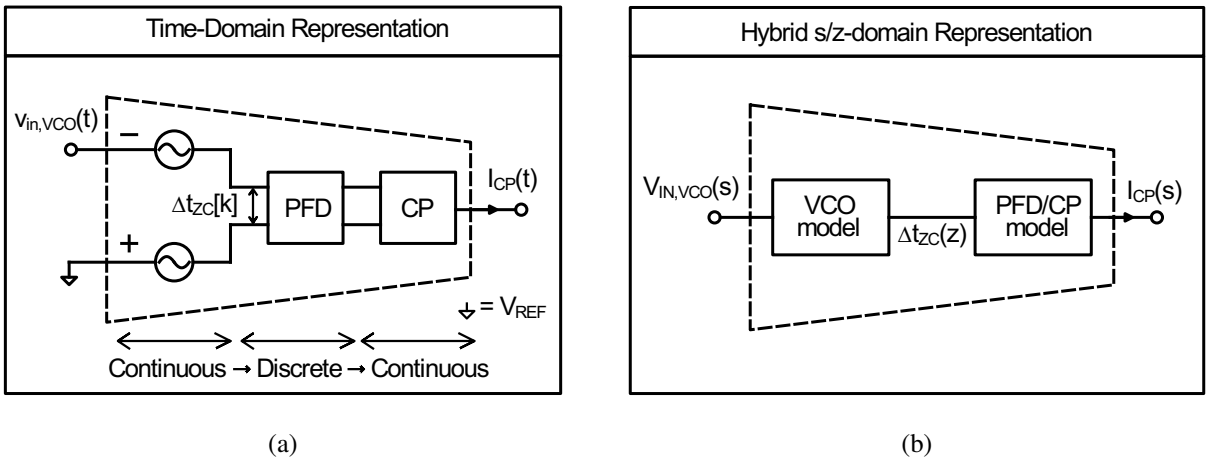
$$\overline{I_{CP}}(t) = K_{PFD} \cdot I_{CP0} \int 2\pi K_{VCO} \cdot v_{in,VCO}(t)dt \tag{4.3}$$

where $K_{PFD} = 1/(2\pi)$ is the gain constant for the PFD expressed in the units of 1/rad and I_{CP0} is the maximum possible current for the CP expressed in Amperes.

The s-domain transform or the Laplace transform of $\overline{I_{CP}}$ is given by:

$$\overline{I_{CP}}(s) = \frac{2\pi K_{VCO}.K_{PFD}.I_{CP0}}{s} \cdot v_{in,VCO}(s) \tag{4.4}$$

[1] averaged over one period of the reference-VCO, T_0.



(a) (b)

Figure 4.4: (a) Time-domain and (b) hybrid s/z-domain representation of the zero-crossing time-difference model (ZCTDM) of a VCO-OTA.

Equations (4.3) and (4.4) represent the continuous-time phase-domain model (CT-PDM) of a VCO-OTA [59, 60] (Fig. 4.3).

CT-PDM being a continuous time model, does not capture the discrete-time effects of the VCO-OTA and is valid only when (a) the update rate f_0 of the system is much higher than f_{UGB} of the closed-loop system, and (b) the input frequency f_{IN} is much less than f_0. As f_0 approaches f_{UGB} or f_{IN} approaches f_0, the closed-loop system response deviates significantly from the CT-PDM response, requiring the use of a better model for the VCO-OTA.

4.4 Proposed Zero-Crossing-Time-Difference Model (ZCTDM)

To relax the CT-PDM assumption, we propose the Zero-Crossing-Time-Difference Model (ZCTDM) for a VCO-OTA in which the intermediate variable is the time difference, $\Delta t_{ZC}[k]$, between the zero crossings of the two VCO outputs at their rising edges, as shown in Fig. 4.4(a). Here index k rep-

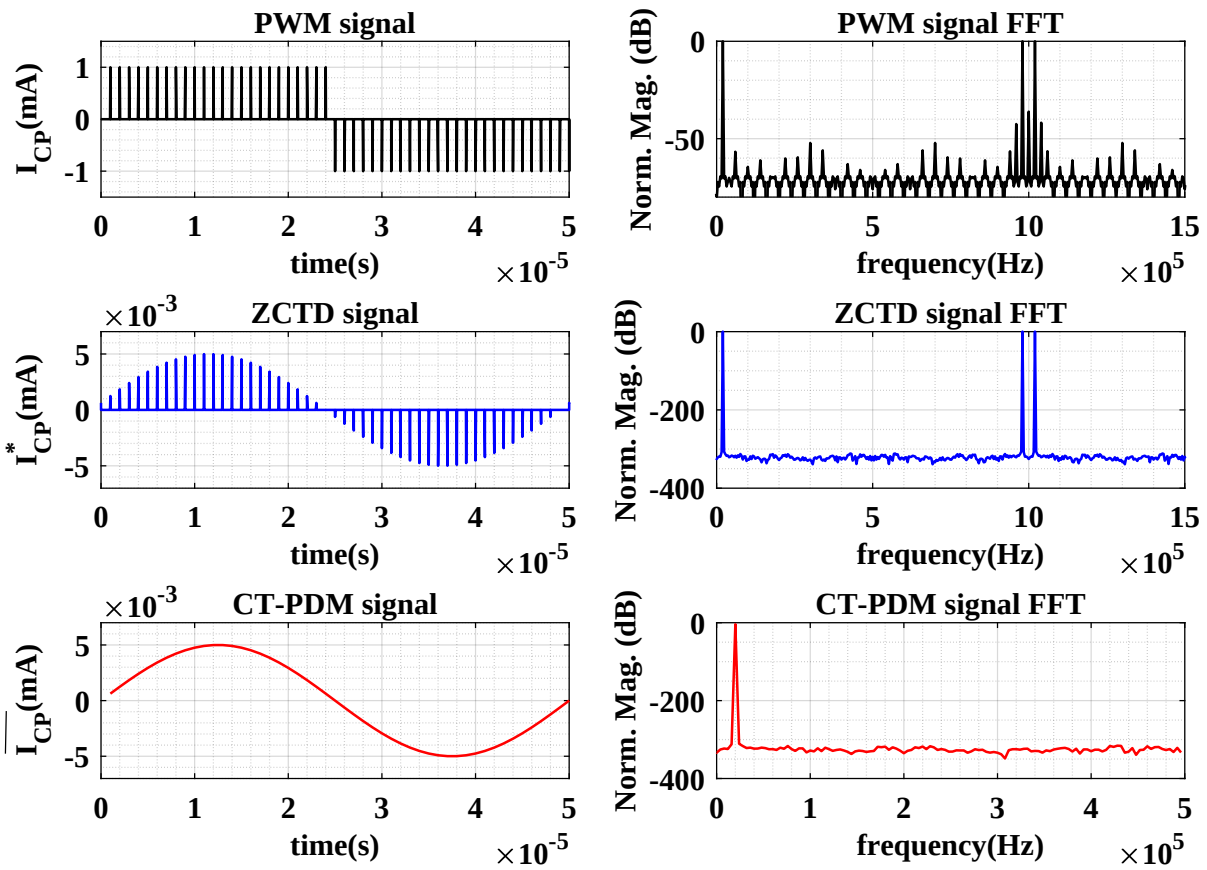


Figure 4.5: Comparing the spectra of a PWM current pulse (I_{CP}) plotted for a 20kHz input signal modulating a 1MHz VCO signal with its equivalent in ZCTDM (I^*_{CP}) and CT-PDM ($\overline{I_{CP}}$). ZCTDM simplifies the analysis while maintaining the high-frequency content to the first order, while CT-PDM neglects high-frequency content and thus provides an oversimplified model.

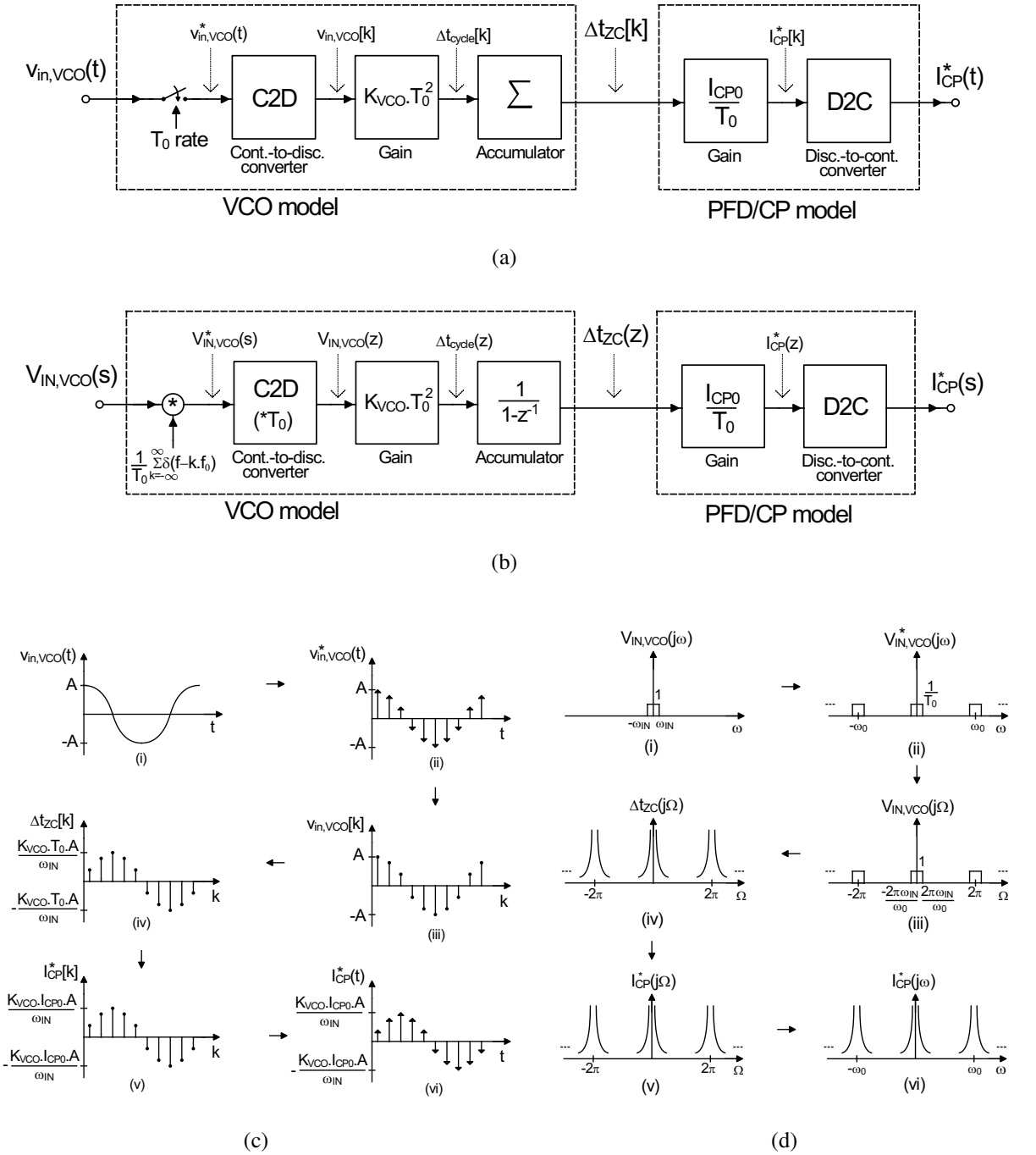


Figure 4.6: (a) and (b) Proposed time-domain and hybrid-s/z-domain model for a low-frequency input. (c) Waveforms at different points of the time-domain low-frequency model for a sine wave input. (d) Corresponding frequency domain plots at different nodes of the proposed model for a band-limited low-frequency input.

resents any general k^{th} cycle of the reference-VCO output waveform. We represent the output current as a scaled impulse train current, $I^*_{CP}(t)$ [72], with the scaling factor proportional to the width of the charge pump current, $I_{CP}(t)$, which can be shown proportional to $\Delta t_{ZC}[k]$ for the kth cycle of the reference-VCO output waveform. The different notations used for ZCTDM are shown in Fig. 4.2.

The time-domain representation of the ZCTDM in Fig. 4.4(a) is continuous in time at the input and output of the VCO-OTA, and discrete in time at the intermediate points. A mixed s/z-domain model is therefore used to represent ZCTDM model for frequency response analysis as shown in Fig. 4.4(b) similar to [71].

ZCTDM is different from CT-PDM in two aspects. First, ZCTDM uses $\Delta t_{ZC}[k]$ instead of $\Delta\phi(t)$ to capture the time difference between the two VCO outputs as shown in Fig. 4.4(a). $\Delta t_{ZC}[k]$ is much more intuitive variable than $\Delta\phi(t)$ since it has a direct physical meaning in case of oscillators, including ring oscillators, where the output is not a sine wave. Use of $\Delta t_{ZC}[k]$ also relaxes the assumption $f_{IN} \ll f_0$ as will be explained in Section 4.4.2. Second, ZCTDM assumes that I_{CP} can be represented by current impulses, $I^*_{CP}(t)$ occurring at regular time intervals of T_0, with the magnitude of the kth impulse being equal to I_{CP0} times the fractional duty cycle of the UP-DN pulse during that cycle. This captures the high-frequency content of $I_{CP}(t)$ near f_0 to the first order in addition to the low-frequency signal content, unlike CT-PDM, which ignores the high-frequency content.

To understand the second claim, we compare the output spectrum of a pulse-width modulated $I_{CP}(t)$ waveform, generated from a slowly varying sinusoidal input, with $\overline{I_{CP}}(t)$ for CT-PDM and

$I^*_{CP}(t)$ for ZCTDM, in Fig. 4.5. The spectrum of $I_{CP}(t)$ is similar to a frequency-modulated (FM) signal with tones present at $m.f_0 + n.f_{IN}$ where m and n are integers. The spectrum of $I^*_{CP}(t)$, used in ZCTDM, has tones only at $m.f_0 \pm f_{IN}$, thus simplifying the analysis as will be discussed in Section 4.4.1, while retaining the high-frequency content of I_{CP} to the first order. The spectrum of $\overline{I_{CP}}(t)$, used in CT-PDM, only represents the low-frequency input content of the PWM waveform, and leads to overly simplified model, as discussed in Section 4.3.

4.4.1 ZCTDM for a Low-Input-Frequency Signal

To derive the ZCTDM for a VCO-OTA, we first find $\Delta t_{cycle}[k]$, the change in the period of kth cycle at the input-VCO's output, with respect to T_0, as a result of applying a small input signal, $v_{in,VCO}(t)$.

If the input signal is varying slowly ($f_{IN} \ll f_0$), $v_{in,VCO}(t)$ can be considered as constant during the kth cycle of the reference-VCO output, represented by a discrete-time input sample, $v_{in,VCO}[k]$. This is a two-step process. In the first step, $v_{in,VCO}(t)$ is sampled by an impulse train, resulting in a sequence of equidistant impulses, $v^*_{in,VCO}(t)$, occurring at multiples of T_0. In the second step, $v^*_{in,VCO}(t)$ is discretized to $v_{in,VCO}[k]$, using a continuous-to-discrete (C2D) converter block as shown in Fig. 4.6(a), with the waveform for a sinusoidal input example shown in Fig. 4.6(c)(i)-(iii) [72]. Mathematically, we can write:

$$v^*_{in,VCO}(t) = \sum_{k=-\infty}^{\infty} v_{in,VCO}(t) \cdot \delta(t - kT_0) \tag{4.5}$$

$$v_{in,VCO}[k] = v_{in,VCO}(kT_0) \tag{4.6}$$

Using (4.1), $\Delta t_{cycle}[k]$ can then be written as:

$$\Delta t_{cycle}[k] = T_0 - T_k \approx K_{VCO} \cdot T_0^2 \cdot v_{in,VCO}[k] \tag{4.7}$$

where T_k is the period of the kth cycle at the output of the input-VCO.

Since the time difference between the rising edges of the two VCOs keeps accumulating, $\Delta t_{ZC}[k]$ (Fig. 4.6(c)(iv)) is given by:

$$\Delta t_{ZC}[k] = \Delta t_{ZC}[k-1] + \Delta t_{cycle}[k] = \sum_{i=-\infty}^{k} K_{VCO} \cdot T_0^2 \cdot v_{in,VCO}[i] \tag{4.8}$$

The discrete-time current impulses, $I_{CP}[k]$, are obtained by scaling Δt_{ZC} with a gain of I_{CP0}/T_0 (Fig. 4.6(c)(v)). To interface the discrete-time output-current impulses with a load, Z_L, represented in continuous-time, we use the discrete-to-continuous (D2C) converter block to obtain the continuous-time output current impulses, $I_{CP}^*(t)$ (Fig. 4.6(c)(vi)) given by:

$$I_{CP}^*(t) = K_{VCO} \cdot T_0 \cdot I_{CP0} \sum_{k=-\infty}^{\infty} \left(\sum_{i=-\infty}^{k} v_{in,VCO}[i] \right) \cdot \delta(t - k.T_0) \tag{4.9}$$

Equation (4.9) relates $I_{CP}^*(t)$ to the discrete-time input samples $v_{in,VCO}[k]$.

The mixed s/z-domain representation of the ZCTDM model is shown in Fig. 4.6(b), with the frequency response for a band-limited input signal shown in Fig. 4.6(d). Input sampling in the time domain is equivalent to multiplication by an impulse train in the mixed s/z domain, which leads to spectrum aliasing for the $V_{IN,VCO}^*(s)$ signal (Fig. 4.6(d)(ii)). Conversion from continuous-

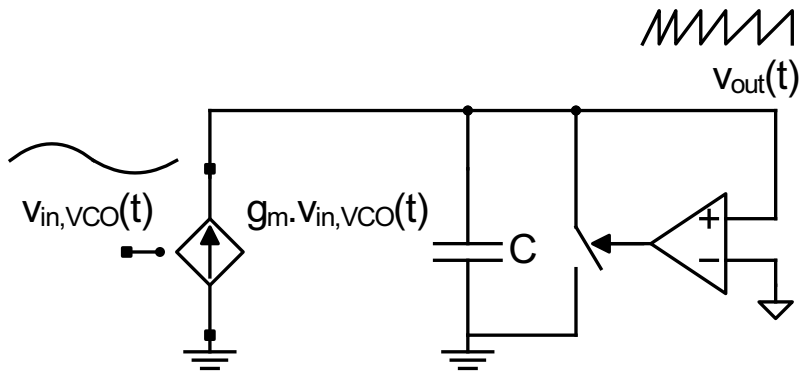


Figure 4.7: Model of a relaxation-oscillator based VCO with the period determined by the charging time of capacitor using a voltage controlled current source. The period of a given oscillation cycle at the output remains the same if a constant input voltage equal to the average of the input voltage is applied, instead of a time-varying input, for that cycle.

to-discrete time results in frequency scale conversion (Fig. 4.6(d)(iii)). The accumulator provides integrator response in the discrete-time domain resulting in a low-pass transfer function for $\Delta t_{ZC}(z)$ as shown in Fig. 4.6(d)(iv). The gain block and the conversion from discrete time to continuous time result in magnitude and frequency scaling as shown in Fig. 4.6(d)(v-vi). Thus, VCO-OTA scales, low-pass filters, and aliases the input spectra.

4.4.2 ZCTDM for Arbitrary-Input-Frequency Signal

To relax the assumption $f_{IN} \ll f_0$, we revisit the VCO model to understand its behavior for an arbitrary-input-frequency signal. Consider a relaxation-oscillator-based VCO modeled using a voltage-controlled current source (VCCS) charging a capacitor, C. The capacitor gets discharged using an ideal comparator and switch configuration after reaching a reference voltage, V_x (Fig. 4.7). The input voltage controls the charging current, and thus the charging time and oscillation frequency.

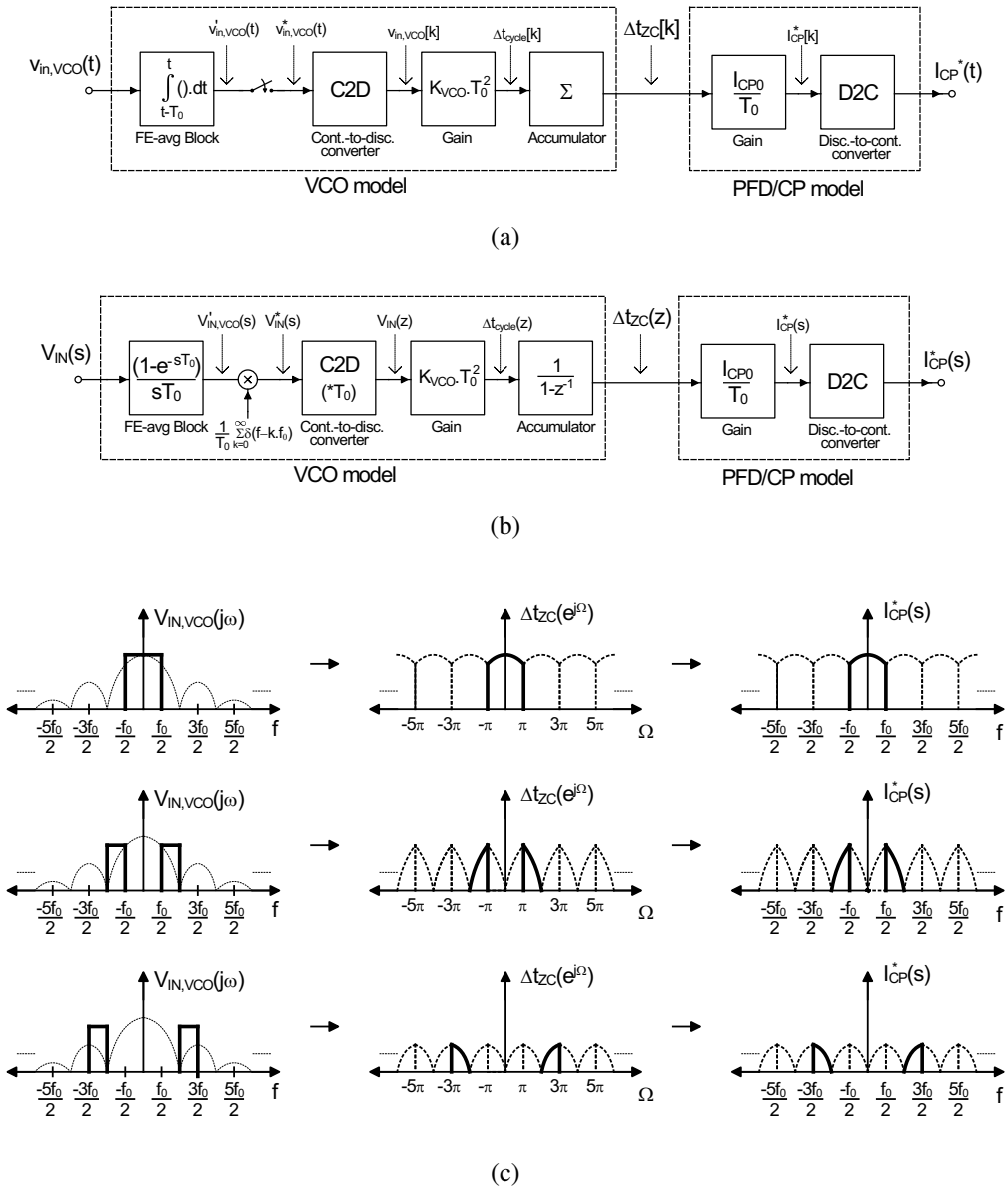


Figure 4.8: (a) Time-domain representation for the ZCTDM including the front-end average block to model a VCO-OTA for an arbitrary-input-frequency signal. (b) Corresponding z-domain model of the ZCTDM (c) Frequency-domain plots for the ZCTDM for the input, output and intermediate points, indicating that the aliased frequency response at the output is shaped with a sinc function depending on the input signal frequency f_{IN}. The top, middle, and bottom rows indicate the transfer functions for f_{IN} from 0 to $f_0/2$, $f_0/2$ to f_0, and f_0 to $3f_0/2$ respectively. The left, middle and right columns represent the frequency response for the $v_{IN,VCO}$, Δt_{ZC}, and I_{CP} respectively. The fundamental frequency is represented in solid line and the aliased frequencies, as well as the sinc function in the left column, used as reference, are shown as dotted lines.

To complete one cycle, the VCCS needs to charge the capacitor from zero to a constant voltage V_x, assuming negligible discharge time. We can consider an infinitesimally small time period $dt \ll 1/f_{IN}$ at a general time t during which the input of the VCO is almost constant, even when the input-signal frequency f_{IN} is arbitrarily large. In the duration dt the capacitor C is charged by a voltage dV given by (using (4.1)):

$$dV = V_x \cdot (f_0 + K_{VCO} \cdot v_{in,VCO}(t))dt \tag{4.10}$$

To complete a general cycle k, C is charged to V_x in one time period T_k and we can write:

$$\int_0^{V_x} dV = \int_{t'-T_k}^{t'} V_x \cdot (f_0 + K_{VCO} \cdot v_{in,VCO}(t))dt \tag{4.11}$$

where t' is the time at which k^{th} cycle ends. Using $T_k = T_0 - \Delta t_{cycle}[k]$, we can write:

$$\frac{\Delta t_{cycle}[k]}{T_0} = \int_{t'-T_k}^{t'} K_{VCO} \cdot v_{in,VCO}(t)dt \tag{4.12}$$

For a small input signal $v_{in,VCO}(t)$, $t' \approx k.T_0$ and $T_k \approx T_0$. We can then rewrite (4.12) as:

$$\Delta t_{cycle}[k] \approx K_{VCO} \cdot T_0^2 \cdot \left(\frac{1}{T_0} \int_{(k-1)T_0}^{kT_0} v_{in,VCO}(t)dt \right) \tag{4.13}$$

Comparing (4.7) and (4.13), we note that the two equations are equal if the kth sample is considered

to be the same as the average voltage in the T_0 duration from $(k-1)T_0$ to kT_0 as given by (4.14)

$$v'_{in,VCO}[k] = \left(\frac{1}{T_0}\int_{(k-1)T_0}^{kT_0} v_{in,VCO}(t)dt\right) \tag{4.14}$$

with the final equation for $I^*_{CP}(t)$ given by:

$$\begin{aligned} I^*_{CP}(t) = K_{VCO}\cdot T_0 \cdot I_{CP0}\cdot \\ \sum_{k=-\infty}^{\infty}\left(\sum_{i=-\infty}^{k}\left(\frac{1}{T_0}\int_{(i-1)T_0}^{iT_0} K_{VCO}\cdot v_{in,VCO}(t)dt\right)\right)\delta(t-kT_0) \end{aligned} \tag{4.15}$$

The generalized ZCTDM for a VCO-OTA given by (4.15) is similar to its low-input-frequency equivalent (Fig. 4.6(a)) with an additional averaging block in the front as shown in Fig. 4.8(a). Note that this averaging block is not accounted for in the CT-PDM system. The integral present in the CT-PDM is the continuous-time representation of the accumulator block in the ZCTDM, which is different from the averaging block. Therefore, CT-PDM can not be used for an arbitrary-input-frequency signal.

The front averaging block is equivalent to a zero-order hold block with its impulse response a rectangle pulse from t = 0 to t = T_0. Its s-domain transform and the frequency response can be written as:

$$H(s) = \frac{1-e^{-sT_0}}{sT_0}; \tag{4.16}$$

$$H(j\omega) = e^{-j\omega T_0/2}\cdot\frac{j\cdot sin(\omega T_0/2)}{\omega T_0/2} \tag{4.17}$$

For a sine wave input to the VCO-OTA, the averaging block scales the amplitude by sinc

transfer function. For a low-input-frequency signal, the transfer function is close to unity, and the arbitrary-input-frequency model becomes the same as the low-input-frequency model. For a high-input-frequency signal, the averaging block acts like a filter with the magnitude response corresponding to a sinc tranfer function. The waveforms at different points of the model are thus similar to the low-input-frequency model (Fig. 4.6(b)), except for the additional scaling factor.

The mixed s/z-domain representation of the generalized ZCTDM model is shown in Fig. 4.8(b). The only difference from the low-input-frequency signal representation (Fig. 4.6(b)) is the addition of averaging block to the model.

The frequency response of the model depends on the relative position of f_{IN} with respect to f_0 and is shown in Fig. 4.8(c) for three input frequencies. The input is first shaped by the sinc transfer function provided by the averaging block. For example in the top row, the transfer function for $\Delta t_{ZC}(z)$ for the fundamental input-frequency component (shown in bold lines) is shaped by the sinc function. Next, the sampling action results in spectrum aliasing of the fundamental component. $I^*_{CP}(s)$ then follows a scaled version of $\Delta t_{ZC}(z)$. The other two rows follow a similar trend where the fundamental component is first shaped by the sinc transfer function and the spectrum is then aliased due to sampling with frequency f_0.

4.5 Loading Effect in a VCO-OTA

Figure 4.9(a) shows the ZCTDM for a VCO-OTA with a load impedance, $Z_L(s)$, placed in a feedback configuration with a feedback factor $\beta_{FB} = R_1/(R_1+R_2)$ and an input node to point P transfer function of $\beta_{IN} = R_2/(R_1+R_2)$. To account for the sampling nature of the VCO-OTA, we analyze

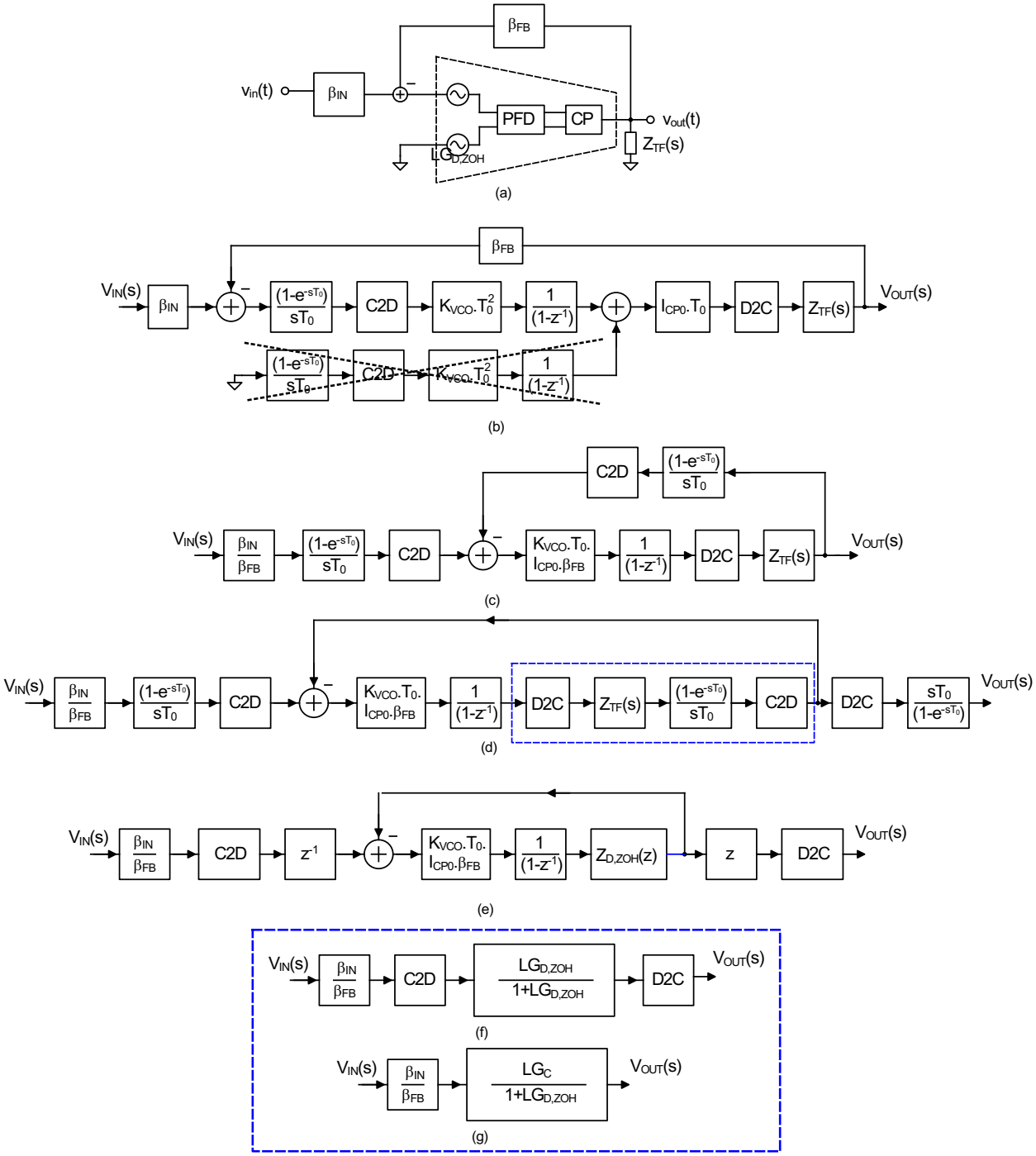


Figure 4.9: Development of a discrete-time loop-gain model for a VCO-OTA loaded with an impedance, $Z_L(s)$, using ZCTDM, in an inverting amplifier configuration.

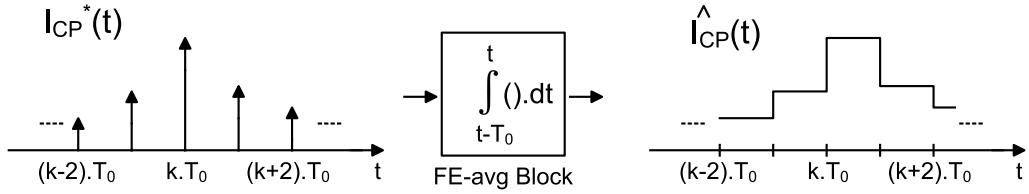


Figure 4.10: I_{CP}^{*} when passed through the front-end average block results in a zero-order hold representation $\hat{I_{CP}}$.

the closed-loop-gain stability by converting the mixed-time-domain ZCTDM-based system into a discrete-time system using the following steps:

1. Replace the VCO-OTA with its equivalent ZCTDM as derived in Section 4.4.2, load it with $Z_L(s)$ and place it in the feedback loop (Fig. 4.9(b)). The model with reference-VCO input is AC ground and can be eliminated for loop-stability analysis.

2. Move the average block and the C2D block from the forward gain path to the input and the feedback path. Also combine the gain blocks (Fig. 4.9(c)).

3. Move the average block and the C2D block from the feedback path to the forward-gain path. This requires cascading an extra D2C block and an inverse of average function block at the output. This is for mathematical analysis and does not have any physical significance (Fig. 4.9(d)).

4. Combine the D2C, $Z_L(s)$, average, and the C2D blocks to form an equivalent discrete-time block for the load impedance, $Z_{D,ZOH}(z)$, which is the zero-order-hold based z-transform of $Z_L(s)$ (Fig. 4.9(e)).

5. For the time-domain step response, the average and the inverse-average blocks evaluate to

unity in the discrete-time domain, resulting in a simplified input to output block diagram represented by a gain in front, followed by continuous-to-discrete conversion, followed by a discrete closed-loop system, followed by conversion back to continuous-time domain (Fig. 4.9(f)). The last block that converts the signal from discrete-to-continuous domain loses some information since it assumes a zero-order hold. The system stability however is captured in the closed-loop system model.

6. To analyze the frequency response, it is possible to combine all the individual blocks into a single continuous-time transfer function, LG(s), in the numerator of the closed-loop transfer function, which is similar to CT-PDM model. The distinction however is that all the discrete-time effects affecting the stability are still captured in the discrete time-domain representation in the denominator of the closed-loop system.

The fourth step can also be understood by noting that when the output current impulses pass through the averaging block, it results in a zero-order held waveform as shown in Fig. 4.10 represented by $\hat{I_{CP}}(t)$, similar to CT-PDM. However, since the overall system is now represented in the discrete-time domain, the ZCTDM captures the sampling effects unlike CT-PDM. Note that $\hat{I_{CP}}(t)$ is not the same as $\overline{I_{CP}}(t)$, the former contains high-frequency content, while the latter one does not.

The equivalent representation of the combined discrete-time impedance block, $Z_{D,ZOH}(z)$, given by the zero-order hold representation of the continuous-time block $Z_L(s)$ as:

$$Z_{D,ZOH}(z) = (1 - z^{-1}) \cdot \mathcal{Z}\left[\mathcal{L}^{-1}\left(\frac{Z(s)}{s}\right)\right] \tag{4.18}$$

The continuous-time loop-gain transfer function, $LG_C(s)$, and the zero-order-hold discrete-time loop-gain transfer function, $LG_{D,ZOH}(z)$, for the system shown in Fig. 4.9(a) can then be given as:

$$LG_C(s) = \frac{K_{VCO}}{s} \cdot I_{CP0} \cdot \beta_{FB} \cdot Z_L(s) \tag{4.19}$$

$$LG_{D,ZOH}(z) = K_{VCO} \cdot I_{CP0} \cdot \beta_{FB} \cdot T_0 \cdot (1 - z^{-1}) \cdot \mathcal{Z}\left[\mathcal{L}^{-1}\left(\frac{Z_L(s)}{s}\right)\right] \tag{4.20}$$

The discrete closed-loop-gain response for the step input, $CLG_{D,ZOH}(z)$ is then given by:

$$CLG_{D,ZOH} = \frac{\beta_{IN}}{\beta_{FB}} \cdot \frac{LG_{D,ZOH}(z)}{1 + LG_{D,ZOH}(z)} \tag{4.21}$$

and the overall transfer function from input to output in Fig. 4.9(f) is given by:

$$\frac{V_{OUT}(j\omega)}{V_{IN,VCO}(j\omega)} = \frac{\beta_{IN}}{\beta_{FB}} \cdot \frac{LG_C(j\omega)}{1 + LG_{D,ZOH}(e^{j\omega T_0})} \tag{4.22}$$

4.6 Design Examples

The generalized model for a loaded VCO-OTA in a feedback loop derived using ZCTDM in (4.21) and (4.22) can be applied to different topologies of the VCO-OTA. We now illustrate the application of this model with two design examples.

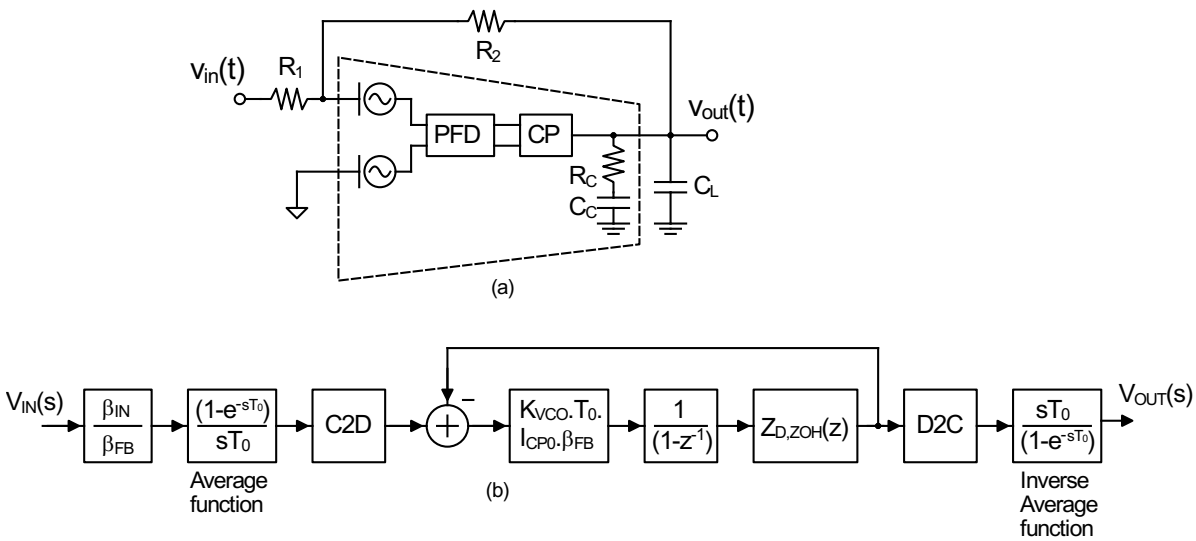


Figure 4.11: (a) Schematic of a VCO-OTA with a passive-zero compensation when placed in an inverting amplifier configuration. (b) Stability and frequency response model based on ZCTDM with loading modeled in the discrete-time domain using (4.18).

4.6.1 Passive-zero-compensated VCO-OTA

A passive-zero-compensated VCO-OTA driving a capacitive load C_L in an inverting amplifier configuration is shown in Fig. 4.11(a). This configuration is similar to the case of a Type-II PLL system and a zero created by compensation resistor R_C and capacitor C_C is used to stabilize the loop [59, 60, 67]. The loop gain in s-domain for this architecture when placed in feedback is given by (after [59]):

$$LG(s) \approx \frac{2\pi K_{VCO} \cdot K_{PFD} \cdot K_{CP} \cdot (1 + sR_C C_C)}{s^2 C_{Sum}(1 + sR_C \frac{(C_C C_L)}{C_{Sum}})} . \beta_{FB} \tag{4.23}$$

where $C_{Sum} = C_C + C_L$, β_{FB} is the feedback factor in the closed-loop system and the gain of the PFD K_{PFD} = 1/2π.

Comparing the output network to the previous section, we observe that the $Z_L(s)$ is represented

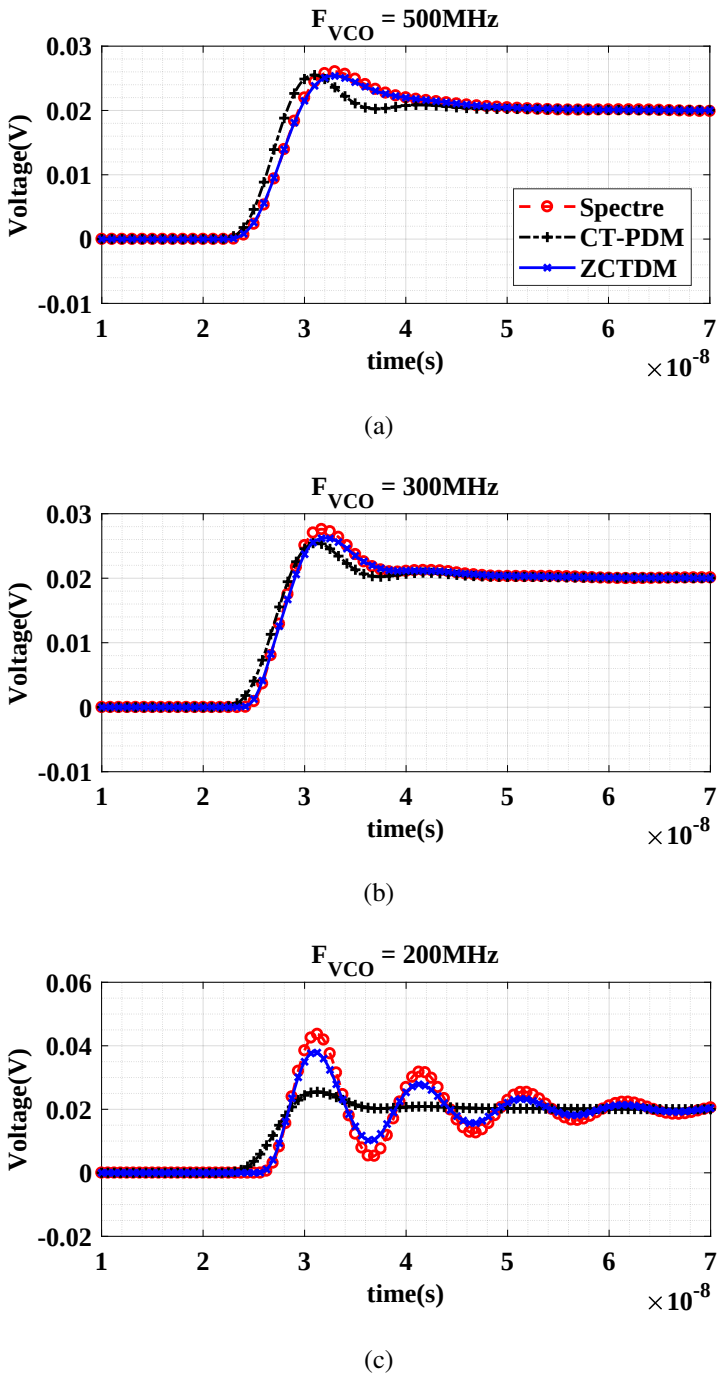


Figure 4.12: Simulated step response for a passive-zero-compensated VCO-OTA after low-pass filtering the output compared to the continuous-time phase-domain model (CT-PDM) and the zero-crossing time-difference model (ZCTDM) for f_0 = 500MHz (a), 300MHz (b), and 200MHz (c). As f_0 approaches f_{UGB} of 50MHz, the system gets more unstable, which is predicted by the proposed ZCTDM, but not by CT-PDM.

by C_L in parallel to R_C in series with C_C. The discrete transform in this case can then be written as:

$$\begin{aligned} Z_{D,ZOH}(z) &= (1-z^{-1}) \cdot \mathcal{Z}\left(\mathcal{L}^{-1}\left[\frac{(1+sR_CC_C)}{s^2C_{Sum}\left(1+sR_C\left(\frac{C_C \cdot C_L}{C_{Sum}}\right)\right)}\right]\right) \\ &= \left(\frac{T_0 \cdot z}{(z-1)^2 \cdot C_{Sum}} + \frac{C_C^2 \cdot R_C \cdot z}{(z-1) \cdot C_{Sum}^2} - \frac{C_C^2 \cdot R_C \cdot z}{(z-a) \cdot C_{Sum}^2}\right) \end{aligned} \tag{4.24}$$

where $a = exp(-T_0 \cdot C_C \cdot C_L/(R_C \cdot C_{Sum}))$. The z-domain loop-gain transfer function (LG(z)) can then be written as:

$$\begin{aligned} LG(z) &= 2\pi K_{VCO} \cdot K_{PFD} \cdot I_{CP0} \cdot T_0 \cdot \beta_{FB} \cdot \\ &= \left(\frac{T_0 \cdot z}{(z-1)^2 \cdot C_{Sum}} + \frac{C_C^2 \cdot R_C \cdot z}{(z-1) \cdot C_{Sum}^2} - \frac{C_C^2 \cdot R_C \cdot z}{(z-a) \cdot C_{Sum}^2}\right) \end{aligned} \tag{4.25}$$

The step response and the frequency response of the system can be computed using (4.21) and (4.22). It is interesting to note that $LG(z)$ in (4.25) matches the discrete-time-domain transfer function derived from for a third order Type II PLL using the impulse-invariant-transform model (IITM) [69] as presented in [71]. In IITM, the z-transform is done on the complete loop including the VCO, which provides the equivalent of integration, and in ZCTDM the integration is provided by the zero-order hold.

Detailed stability analysis of the loop for the case when f_0 approaches f_{UGB} of the system is provided in [71] using (4.25). Fig. 4.12 shows the step response of the VCO-OTA system in an inverting amplifier configuration for an f_{UGB} of 50MHz, for f_0 = 1GHz, 500MHz, and 200MHz. Behavioral models for individual blocks of VCO-OTA are used to simulate the closed-loop circuit

shown in Fig. 4.11(a) using Cadence Spectre simulator [73] and are compared to the CT-PDM and ZCTDM using MATLAB [34]. As f_0 approaches f_{UGB}, we start observing ringing effect in the Spectre simulation results. This is not observed in the case of CT-PDM but is predicted by the ZCTDM, indicating the benefit of ZCTDM in predicting the sampling nature of the system, which becomes prominent as f_0 approaches f_{UGB}.

The benefit of ZCTDM in predicting stability where IITM fails is discussed next.

4.6.2 Active-zero-compensated VCO-OTA

In recent PLL literature, active-zero compensation has emerged as a technique to reduce area overhead that results from the use of the compensation capacitor in the passive-zero-compensated scheme [61, 62]. Active-zero compensation uses a Voltage-Controlled Delay Line (VCDL) to provide a zero that stabilizes the loop gain. In this section, we derive the discrete-time loop-gain transfer function for an active-zero-compensated VCO-OTA in an inverting amplifier configuration (Fig. 4.13(a)). The s-domain continuous-time loop gain (LG(s)) using CT-PDM is given by [61, 62]:

$$LG(s) = 2\pi\left(\frac{K_{VCO}}{s} + K_{VCDL}\right) \cdot K_{PFD} \cdot \frac{I_{CP}}{s\,C_L} \cdot \beta_{FB} \tag{4.26}$$

where K_{VCDL} is the VCDL gain in cycles per Volt.

To derive the ZCTDM for active-zero compensation in the presence of loading and feedback, we note two key points. First, it is possible to model the VCDL path for the system as a parallel path to the VCO before adding the time differences resulting from the two paths together before the PFD. This model holds true even if the VCDL is placed in series with the VCO as is the case

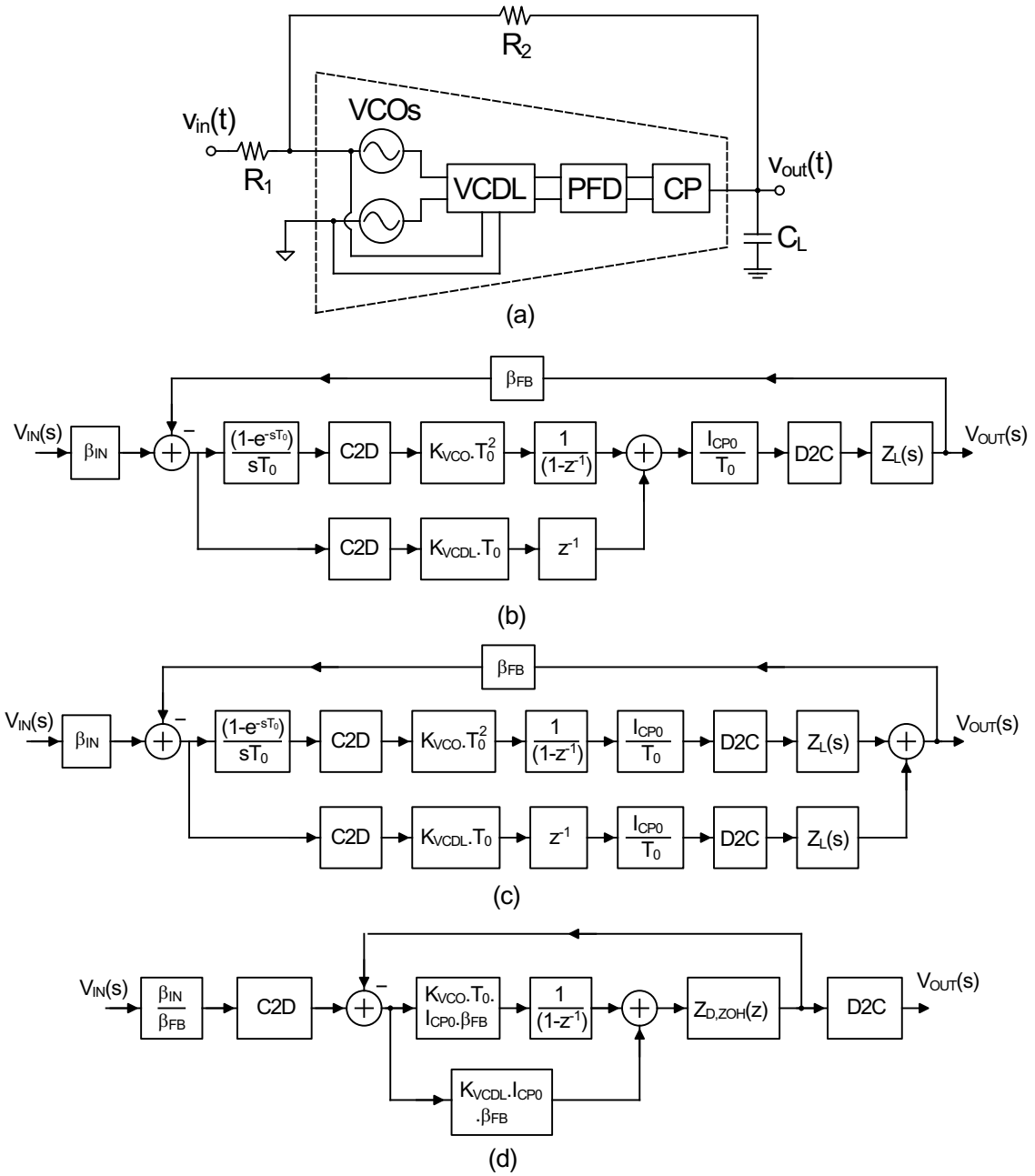


Figure 4.13: Development of a discrete time loop-gain model using ZCTDM for the active-zero-compensated VCO-OTA in an inverting amplifier configuration.

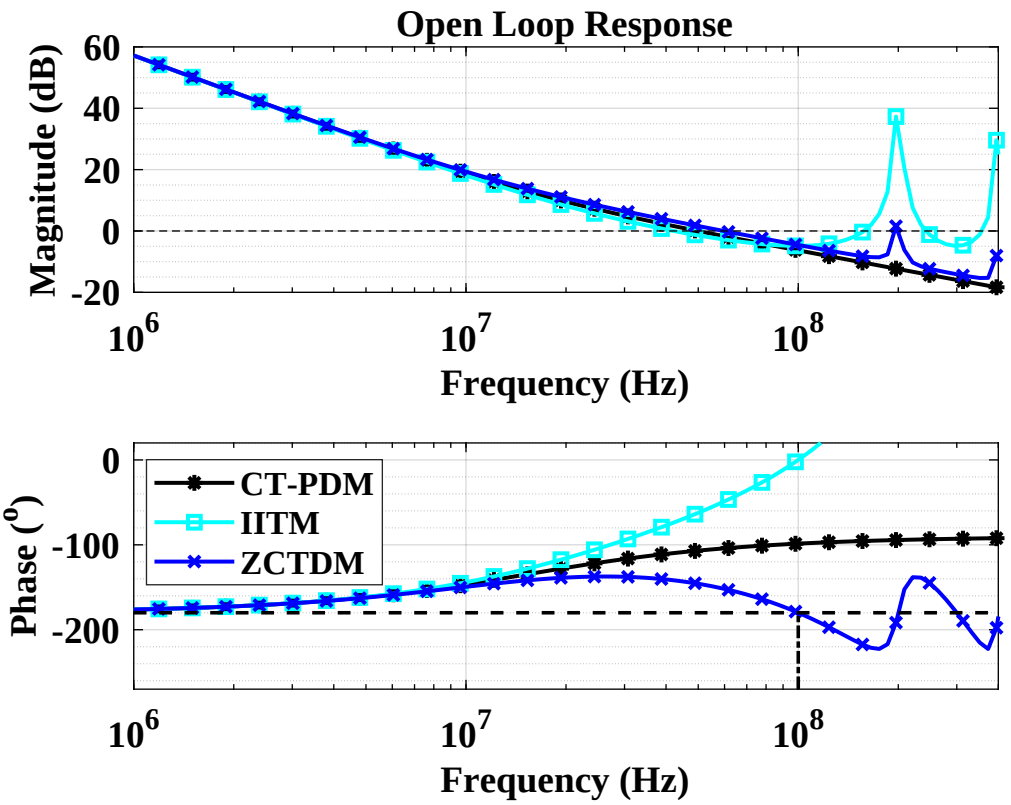


Figure 4.14: Open loop magnitude and phase response for active-zero-compensated VCO-OTA with f_0 = 200MHz and f_{UGB} = 50MHz to demonstrate phase degradation as predicted by the ZCTDM, which is not predicted by either CT-PDM or IIT model.

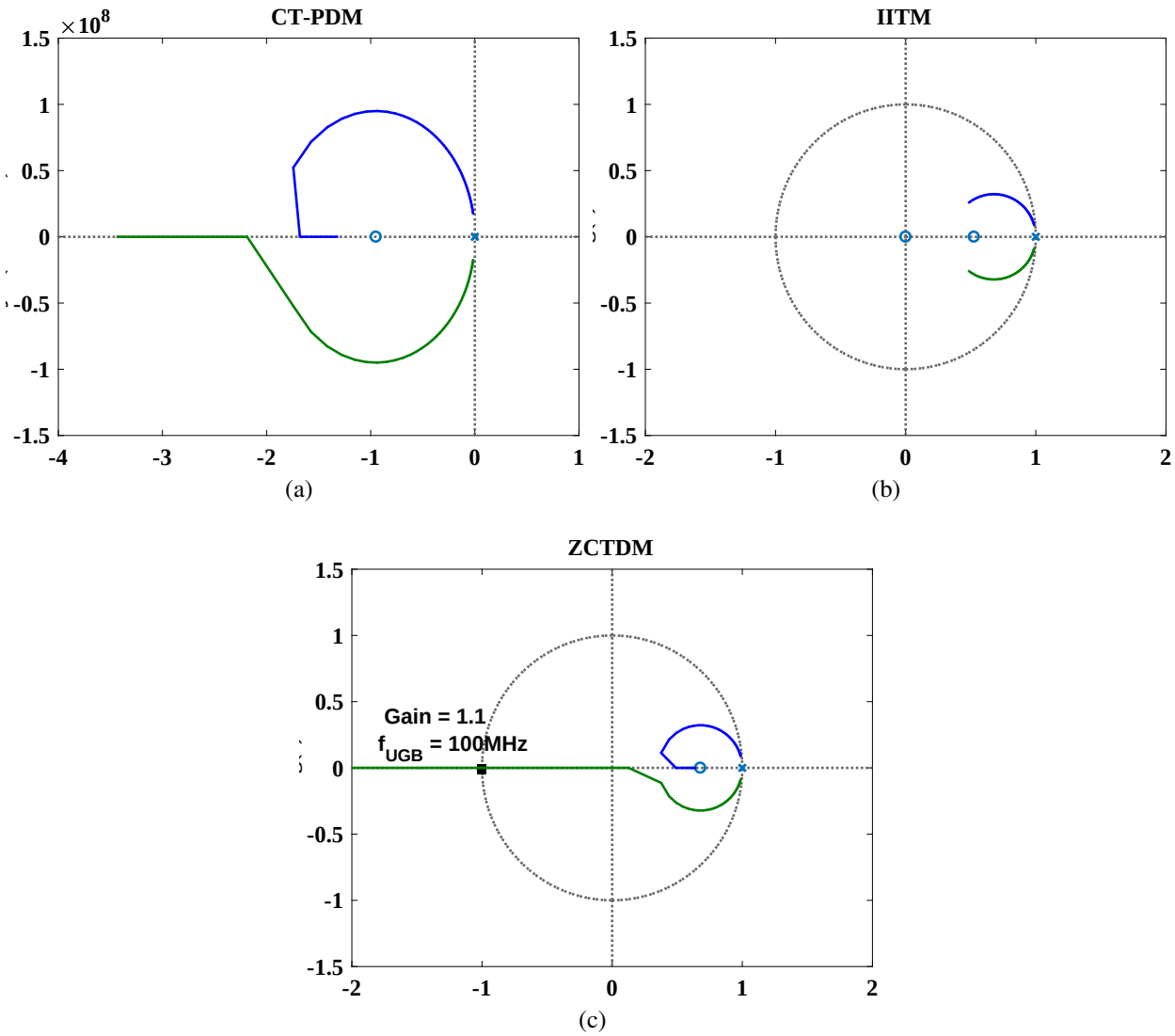


Figure 4.15: Root locus plots for active-zero-compensated VCO-OTA with 200MHz f_0 and 50MHz f_{UGB} plotted for (a) CT-PDM, (b) IIT Model, (c) ZCTDM. Only ZCTDM predicts instability when f_{UGB} exceeds 100MHz (f_0/2), which is similar to prediction in [8].

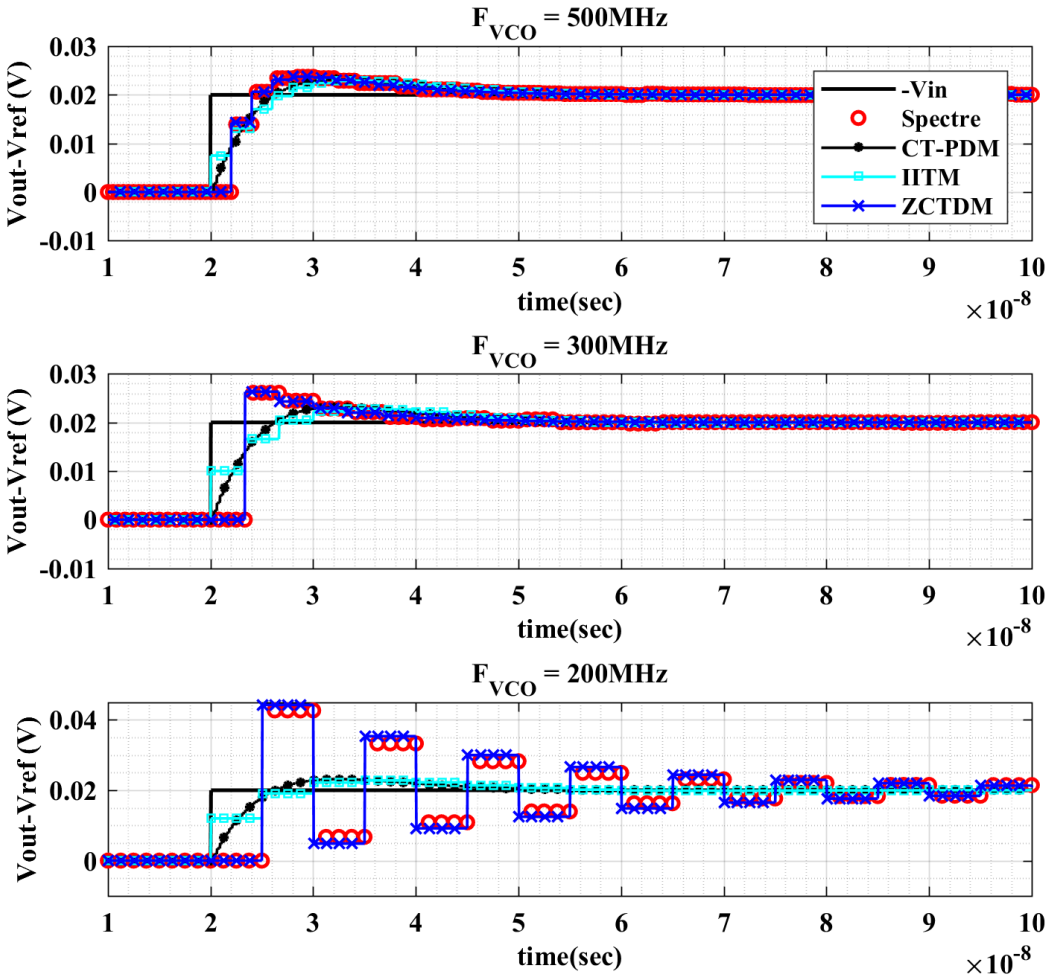
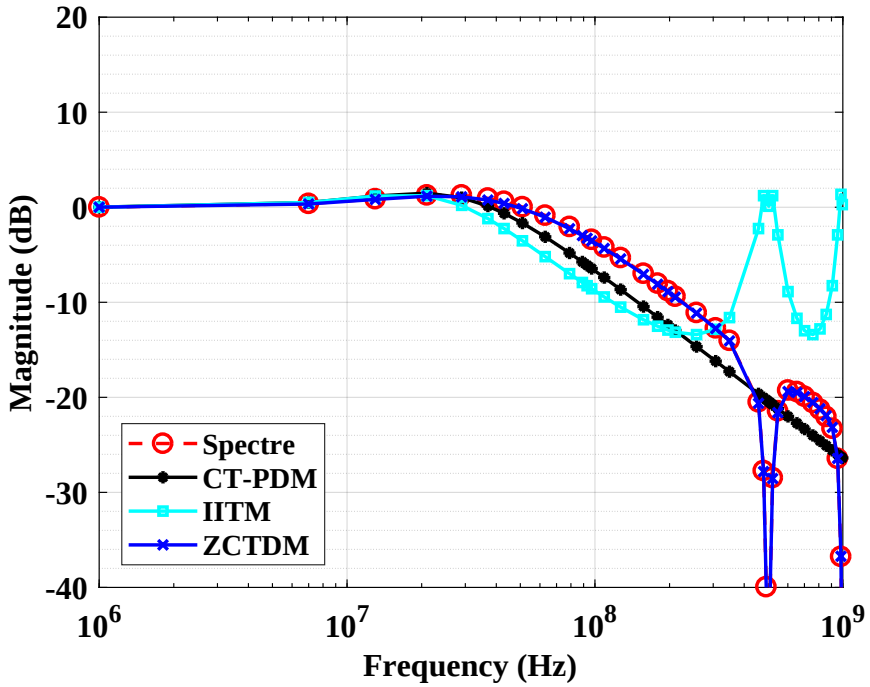
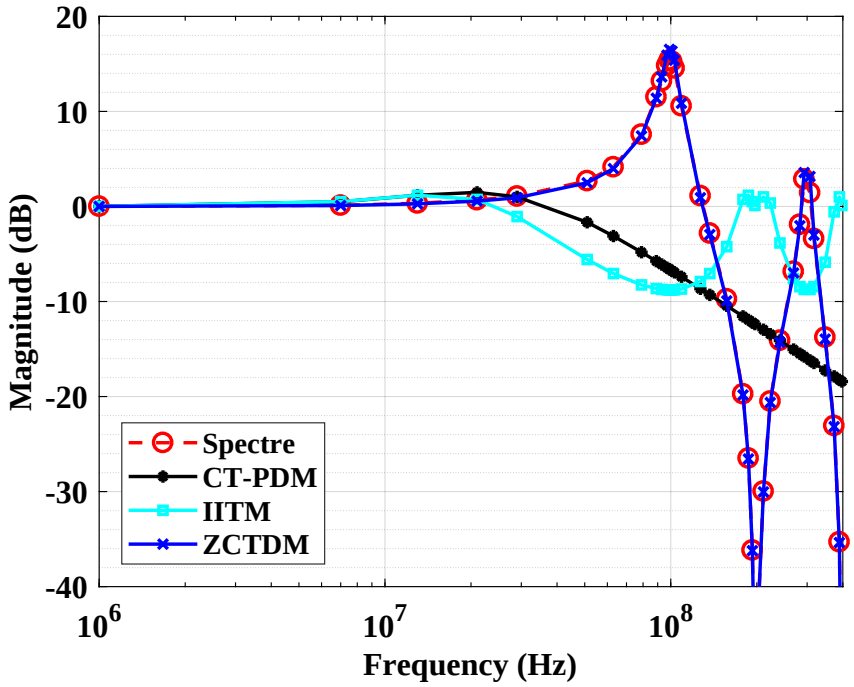


Figure 4.16: Comparison of step response for an active-zero-compensated VCO-OTA with different models for f_0 = 500MHz, 300MHz, and 200MHz with f_{UGB} = 50MHz. CT-PDM and IIT model response also plotted are different than the spectre results, particularly as f_0 approaches f_{UGB}



(a)



(b)

Figure 4.17: Comparison of closed-loop frequency response for an active-zero-compensated VCO-OTA with the predicted models for (a) f_0 = 500MHz, (b) f_0 = 200MHz. The frequency response of ZCTDM follows Spectre simulation results much better than other models.

in [61]. Second, the VCDL model will include an additional delay, z^{-1}, that models the inherent small delay of the PFD, which ensures that even if the VCO-OTA output is changing due to CP injection in the current k^{th} cycle, this affects the $(k+1)^{th}$ cycle. If this delay is not used, then the current k^{th} cycle may affect itself resulting in incorrect loop-gain estimate for small signal. Note that this is not required for the VCO since the accumulator block prevents that phenomenon.

We now replace the ZCTDM blocks for the VCO and the VCDL as shown in Fig. 4.13(b). We follow the steps illustrated in Section 4.5 to derive the final discrete-time z-domain model in Fig. 4.13(c). In this case, we have two loops, one for the VCO and one for the VCDL. For the VCO loop, we discussed in Section 4.5 that zero-order-hold is the best representation. For the VCDL loop, since the output current is in the form of impulses, impulse transform seems to be the best choice for discretizing $Z_L(s)$. However, the additional delay of the VCDL loop can be integrated with the impulse transform of $Z_L(s)$, to approximate with a zero-order-hold transform. This simplifies the overall loop since zero-order-hold can now be used for both the loops and combined in one as shown in Fig. 4.13(d). The discrete-time closed-loop gain ($LG_{D,ZOH}(z)$) in this case can be given as:

$$\begin{aligned} LG_{D,ZOH}(z) &= \left(\frac{K_{VCO}\cdot T_0}{(1-z^{-1})} + K_{VCDL}\right)\cdot I_{CP0}\cdot \beta_{FB}\cdot (1-z^{-1})\cdot \\ &\qquad \mathcal{Z}\left(\mathcal{L}^{-1}\left(\frac{Z_L(s)}{s}\right)\right) \\ &= \left(\frac{K_{VCO}\cdot T_0}{(1-z^{-1})} + K_{VCDL}\right)\cdot I_{CP0}\cdot \beta_{FB}\cdot T_0\cdot \frac{z^{-1}}{C_L\cdot (1-z^{-1})} \end{aligned} \tag{4.27}$$

The step response and the frequency response of the system can be computed using (4.21) and

(4.22). We can show that the loop gain obtained using IITM is given by:

$$\begin{aligned} LG(z) &= \mathcal{Z}\left(\mathcal{L}^{-1}\left[\left(\frac{K_{VCO}}{s}+K_{VCDL}\right)\cdot I_{CP0}\cdot \beta_{FB}\cdot T_0\cdot Z_L(s)\right]\right) \\ &= \left(\frac{K_{VCO}\cdot T_0\cdot z^{-1}}{(1-z^{-1})}+K_{VCDL}\right)\cdot I_{CP0}\cdot \beta_{FB}\cdot T_0\cdot \frac{1}{C_L\cdot(1-z^{-1})} \end{aligned} \tag{4.28}$$

The result obtained for IITM is different from the ZCTDM in this case. To understand the difference between (4.27) and (4.28), we plot the magnitude and phase response of the loop gain by replacing z with $e^{j\omega T_0}$ in Fig. 4.14. We first note that CT-PDM does not predict instability in any of the cases. It is interesting to note that IITM also predicts an unconditionally stable system. This is incorrect because as f_0 approaches f_{UGB}, sampling nature of the system results in instability, as predicted by ZCTDM only.

This fact is also supported by the root locus plots for the three models in Fig. 4.15. Only ZCTDM predicts instability where the root locus extends outside z = 1 circle. For CT-PDM, the pole-zero locations are always in the left half plane indicating a stable system at all times, while for IIT, the z-domain plots have roots always inside the unit circle. From the root-locus plot for the ZCTDM, the system will become unstable at gain = 1.1, when f_{UGB} = 100MHz [8]. We confirmed that the system is unstable with gain = 1.15 and settles with gain = 1.05.

The step response for the three f_0 values is in Fig. 4.16. The ZCTDM predicts the closest response to the behavioral model Spectre simulations of the active-zero compensated VCO-OTA in an inverting-amplifier configuration (Fig. 4.13). Finally, we plot the frequency response of the system in Fig. 4.17. While CT-PDM and IIT responses differ from the simulated Spectre results,

the predictions of ZCTDM are very close to simulated results, particularly as the input frequency approaches f_0.

4.7 Discussion

4.7.1 VCO-OTA System Design Using ZCTDM

To design a system based on a VCO-OTA, it is best to start by using CT-PDM since the expressions for UGB and PM are easier to compute. For an aggressive design, it is then possible to reduce f_0 of the VCO with respect to f_{UGB} of the system by using ZCTDM and finding out modified UGB and PM using (4.20). It is possible to obtain the required expressions in MATLAB [34] by using 'C2D' function with zero-order hold transfer function. If it is required to model the large signal behavior, we can use the state-space model [71], otherwise the final design can be directly verified using Spectre simulations [73].

4.7.2 Input Signal Aliasing for f_{IN} Close to f_0

In a VCO-OTA system, if the input signal frequency is close to VCO frequency, it is aliased back at the low-input frequency. This raises concerns regarding potential frequency-translation nature of the system which can corrupt a low-frequency signal. As discussed in Section 4.4.2, the high-frequency signal is attenuated by the sinc transfer function before translating back at low-input frequency. Knowledge of the exact suppression factor enables the designer to appropriately choose VCO frequency depending on the system requirements.

4.7.3 Differential VCO-OTA based Design

In this chapter, we have analyzed systems using single-ended VCO-OTA for simplicity. For a differential-circuit design, the frequency of the two input VCOs varies around the reference frequency, given by the average of the two frequencies set by the common mode. This is similar to a differential circuit in the voltage domain where the input signals vary around the common-mode voltage. Differential VCO-OTA design from single-ended design is therefore similar to the voltage-domain OTAs.

4.7.4 ZCTDM Accuracy Dependence on the Ratio of Output Discharge Rate Relative to the Update Rate

In this chapter, we have used the zero-order hold discretization method for the load impedance $Z_L(s)$ for both passive and active compensation schemes. However, the inherent assumption in modeling the zero-order hold system, particularly for the active-zero compensation relies on the discharge rate of the output voltage being much less than the update rate of the system f_0. Most of the real-world applications using VCO-OTAs follow this basic assumption.

If however, the discharge rate is much faster than the update rate through the use of say a resistive load R_L parallel to the capacitive load C_L, then a better discretization method to use is 'Bilinear' or 'Tustin' transform method instead of the zero-order hold method [72]. This is because the Bilinear Transform relies on the trapezoidal interpolation method and can incorporate the discharge effects. It is however not possible to generalize this approach because of the additional zero introduced in the transformation prevents accurate prediction of the former system.

Note that the distinction between the type of transform used only matters in predicting the system when f_0 approaches f_{UGB}. When f_0 is much greater than f_{UGB}, then all discrete-time transforms converge to the CT-PDM method.

4.7.5 Validity of the ZCTDM for a VCO-OTA

ZCTDM accurately predicts the small-signal behavior of the VCO-OTA system. For large-signal behavior, however, simulation results are different from ZCTDM predictions. This is because ZCTDM assumes that any change in the output voltage in the kth cycle only affects $(k+1)^{th}$ cycle and not the kth cycle itself. This assumption is not true for a large signal input if the width of the PWM current pulse is larger than the total delay from PFD and CP. In the case of active-zero compensation, the proportional path propagates the change in the current cycle to the output, resulting in deviation from the small-signal behavior.

A nominal delay of 200ps is used after the PFD to model its delay for the simulations presented in this chapter, which is much smaller than the period of the VCO. The exact value does not affect stability, it only determines the transition from small signal behavior to large signal behavior.

Fortunately, if the output affects the current cycle, the phase delay is reduced, improving system stability. ZCTDM thus provides the worst case results for stability. State-space analysis can be used for accurate prediction of the large-signal stability at the cost of increased complexity [71].

4.8 Chapter Summary

In this chapter, we presented the zero-crossing-time-difference based model (ZCTDM) for linear, discrete-time stability analysis of a VCO-OTA to predict the step and the frequency response of a passive-zero-compensated and an active-zero-compensated VCO-OTA system. Behavioral-level simulations are used to demonstrate that ZCTDM accurately matches with Spectre simulation results even when f_0 of the VCO approaches f_{UGB} of the system, whereas the continuous-time phase-domain model (CT-PDM) and the impulse-invariant-transform model (IITM) fail to predict the system behavior.

Chapter 5

Benefits of Using VCO-OTA in a Baseband TIA in Current-Mode Receivers[1]

In this chapter, a filterless blocker-tolerant current-mode receiver using a voltage-controlled oscillator (VCO)-based operational transconductance amplifiers (VCO-OTAs) for the baseband transimpedance amplifiers (BB TIAs) is presented as an alternative to inverter-based OTAs (inv-OTAs). Three key advantages of VCO-OTAs over inv-OTAs discussed are a high DC gain, a higher bandwidth for a given DC gain, and independent control of noise and the unity-gain bandwidth. These advantages are used to demonstrate power reduction in the BB TIAs, the low-noise transconductance amplifier (LNTA), and the passive mixer LO drivers in the receiver. A design methodology for the choice of the VCO-OTA parameters in the context of a receiver design is illustrated with an example of a 20MHz RF-channel bandwidth receiver operating at 2GHz. Receiver simulation results indicate an improvement of up to 12dB in blocker 1dB compression point (B1dB) for slightly higher power consumption or up to 2.6× power reduction of the TIA resulting in up to 2× power reduction of the receiver for similar B1dB performance.

[1]This project was done in collaboration with Tanbir Haque and Rupal Gupta and published in TCAS-I [67]

5.1 Background

The evolution of cellular standards from 3G to 5G and beyond require future wireless terminals to support a large number of frequency bands spanning from 600MHz to 6GHz. Narrowband CMOS receiver front-ends require external RF filtering to prevent large out-of-band (OOB) signals from blocking the desired in-band (IB) signal. This leads to exceedingly complex RF front-end solutions for cognitive and software-defined radio applications, as well as multi-mode, multi-band cellular terminal applications. In recent years, several wideband receiver architectures have been proposed that deliver both high blocker tolerance [74,75] and high sensitivity [9,10,76–83]. These architectures have the potential to meet the flexibility, performance and size targets of future mass-market applications.

In addition to the evolution of wireless standards, semiconductor technology scaling is unlocking several overall benefits like higher transistor speeds and higher capacitance densities but leads to particular challenges for the analog designer [2]. Key is the reduction of the supply voltage to sub-1V levels and reduced intrinsic gain of the transistor. Wideband current-mode receiver architectures, consisting of low-noise RF transconductors (LNTA), passive mixers, and transimpedance amplifiers (TIAs), have generally benefitted from CMOS technology scaling. However, the baseband (BB) TIA, a critical part of this type of receiver, remains a design challenge. Traditional methods of stacking multiple transistors to achieve high gain have proven difficult. Inverter-based operational transconductance amplifiers (inv-OTAs) have recently been widely used to construct BB TIAs in current-mode receivers [10,76,77,82,83]. However, the low DC gain of the inverter results in an increased noise contribution from the BB amplifiers leading to an increased BB power

consumption, which can be significant [10,76,77]. VCO-OTAs provide high DC gain even at lower supply voltages because of the perfect integration action provided by the inherent frequency-to-phase conversion, thereby taking full advantage of the CMOS scaling benefit of device speed increase while overcoming the DC gain reduction limitation [7,59,60,64,66]. This chapter compares two supply-scaling friendly architectures, namely a VCO-OTA and an inv-OTA, and demonstrates three key benefits of using a VCO-OTA over an inv-OTA: higher DC gain, higher signal bandwidth for a given DC gain, and independent selection of noise and unity-gain bandwidth (UGB). The two designs are used to construct the BB TIA for a blocker-tolerant wideband receiver, with the VCO-OTA based receiver resulting in better performance for comparable power consumption and lower power consumption for comparable performance. This chapter extends the discussion on benefits of using VCO-OTA for receiver design [66] by comparing its performance with the inv-OTA based receivers. Factors affecting receiver blocker tolerance and parameter selection guidelines to design VCO-OTA-based TIAs (VCO-TIAs) are also presented.

The chapter is organized as follows. The general requirements for a blocker-tolerant receiver are discussed in Section 5.2 and the effects of the BB-TIA parameters on blocker tolerance are discussed in Section 5.3. The advantages of VCO-OTAs over inv-OTAs are described in Section 5.4 and the system-level benefits of the former in a BB TIA are described in Section 5.5. Section 5.6 provides guidelines for VCO-TIA parameter selection with a 20MHz RF bandwidth receiver example illustrated in Section 5.7. Section 5.8 discusses the second-order effects associated with VCO-TIAs and section 5.9 concludes the chapter.

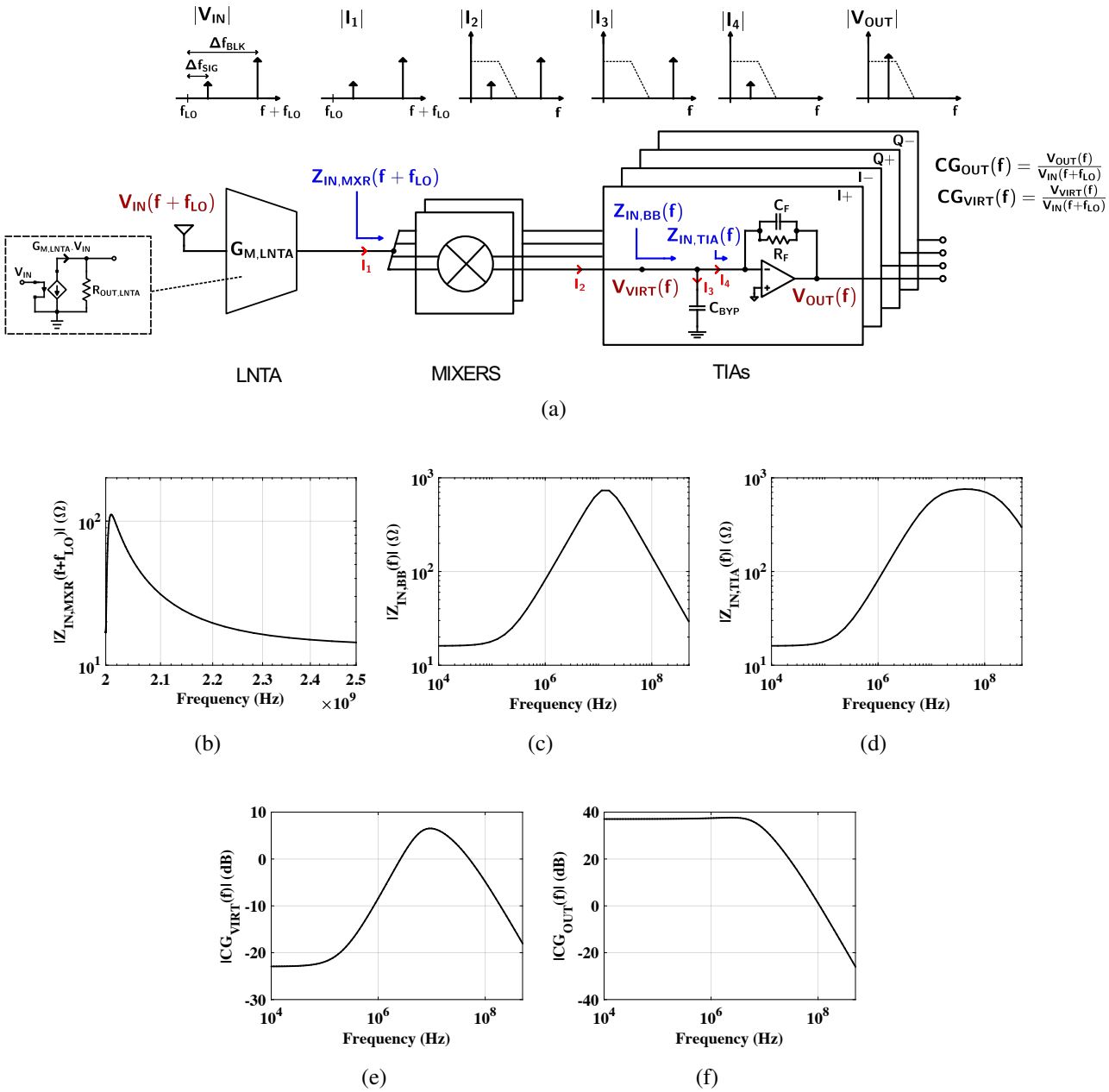


Figure 5.1: (a) Block diagram of a blocker-tolerant receiver consisting of an LNTA, passive mixers and the BB TIAs. As the signal travels through the receiver, the in-band (IB) signal gets amplified while the out-of-band (OOB) blocker gets filtered out; (b-d) Simulated frequency variation of the input impedance at the mixer, the baseband, and the TIA nodes; (e-f) Simulated conversion gain $CG_{VIRT}(f)$ and $CG_{OUT}(f)$ from the input node to the virtual ground node and the output node using parameters given for Rx1 in Fig. 5.7(b). An ideal receiver requires a high $CG_{OUT,IB}(f)$, a low $CG_{VIRT,IB}(f)$, a low $CG_{VIRT,OOB}(f)$, and $CG_{OUT,OOB}(f)$.

5.2 Requirements for Blocker-Tolerant Receivers

The architecture of a current-mode, blocker-tolerant frequency-translational receiver [82, 83] is shown in Fig. 5.1(a), consisting of a wideband LNTA, passive mixers and BB TIAs. The signal frequency around RF is downconverted to the BB due to the current being switched by the mixer. We define the following conversion gains from input node voltage V_{IN} to output node voltage V_{OUT} and virtual ground voltage at the input of the TIA V_{VIRT} as:

$$CG_{OUT}(f) = \left|\frac{V_{OUT}(f)}{V_{IN}(f+f_{LO})}\right|;\ CG_{VIRT}(f) = \left|\frac{V_{VIRT}(f)}{V_{IN}(f+f_{LO})}\right| \tag{5.1}$$

where the signal at V_{OUT}, and V_{VIRT} is at the BB frequency f and the signal at V_{IN} is at RF frequency $f+f_{LO}$. A high conversion gain from input to output for IB signals, $CG_{OUT,IB}(f)$, is needed to suppress BB noise and achieve sufficient voltage swing at the BB outputs for data converters following the BB TIAs. Due to the presence of OOB blockers, Blocker 1dB compression point (B1dB) for filterless receivers can be limited by compression at the output or at the internal nodes. A low conversion gain from input to output for OOB signals, $CG_{OUT,OOB}(f)$, is needed to avoid TIA compression due to blocker frequencies. A low IB conversion gain from the input to the virtual ground node at the TIA input, $CG_{VIRT,IB}(f)$, is also needed, since any non-linear currents, produced at the TIA output can be suppressed at the virtual ground node by the OTA-feedback loop-gain[2] [81]. Therefore, when B1dB is limited by output compression, B1dB is a function of

[2] A negative resistance is used in [81] to avoid non-linearity at the virtual ground node at the cost of increased NF. In this chapter, high DC gain suppression of the VCO-OTA is used to provide the same benefit without the noise penalty.

both the input offset frequency, Δf_{sig}, at which B1dB is measured and the blocker offset frequency, Δf_{BLK}.

To avoid compression at the internal nodes, unwanted voltage gains at the LNTA output and the mixer output need to be reduced. Since the wideband LNTA converts the input voltage into current for the complete frequency spectrum, voltages produced at the LNTA output and the mixer output are proportional to the input impedance at the mixer $Z_{IN,MXR}(f+f_{LO})$ and the input impedance at BB $Z_{IN,BB}(f)$, which is dependent on the TIA input impedance $Z_{IN,TIA}$ (Fig. 5.1(b-d)). $Z_{IN,TIA}$ is close to zero for BB signals close to DC, thanks to the high gain of the BB-OTA feedback loop. As the frequency increases, $Z_{IN,TIA}(f)$ increases and stays constant after the TIA bandwidth, f_{TIA}, until the UGB of the OTA reduces it again. $Z_{IN,BB}(f)$ follows $Z_{IN,TIA}(f)$ until f_{TIA}, after which it is determined by the bypass capacitor, C_{BYP}. Due to the impedance upconversion by the passive mixers, $Z_{IN,MXR}(f+f_{LO})$ is proportional to $Z_{IN,BB}(f)$. These impedances are used to predict the effects of BB-TIA parameters on blocker tolerance in section III.

The key receiver requirements for a blocker-tolerant receiver can therefore be summarized as (a) high $CG_{OUT,IB}(f)$ to suppress BB noise and achieve sufficient voltage swing at the BB outputs for later stages; (b) low $CG_{VIRT,IB}(f)$ and $CG_{VIRT,OOB}(f)$ to avoid compression at the TIA input node and the LNTA output node; and (c) low $CG_{OUT,OOB}(f)$ to avoid compression at the TIA output node due to blocker signals.

5.3 Effect of TIA Parameters on Blocker Tolerance

The three requirements discussed earlier can be met by the proper choice of TIA parameters such as the TIA feedback resistor and capacitor, R_F, C_F, the bypass capacitor, C_{BYP}, TIA DC gain, A_{DC}, and the open loop unity-gain bandwidth. f_{UGB}, of the TIA's OTA. In this chapter, we assume that both inv-OTA and VCO-OTA can be modeled as amplifiers with a given A_{DC} and f_{UGB}. The ideal requirements for these block-level parameters are discussed next.

5.3.1 Effect of OTA DC Gain

The passive mixer upconverts $Z_{IN,BB}(f)$ to $Z_{IN,MXR}(f)$ centered around the local oscillator frequency, f_{LO}, as shown in Fig. 5.1. For low-frequency BB signals, capacitors C_F and C_{BYP} can be ignored. The upconverted $Z_{IN,MXR}(f)$ at frequencies near f_{LO} is therefore purely resistive, and is given by [3] [**?**]:

$$Z_{IN,MXR}|_{f\approx f_{LO}} = R_{SW} + \xi\frac{R_F}{A_{DC}} \tag{5.2}$$

where R_{SW} is the switch-on impedance and ξ is the BB conversion factor based on the number of LO phases used in the receiver. For a given R_{SW} and R_F, a high A_{DC} can provide a lower $Z_{IN,MXR}$, hence increasing B1dB. Note that other methods of increasing B1dB, reducing R_{SW} and R_F result in increased LO driving power and reduced $CG_{OUT,IB}(f)$ respectively, both of which are undesirable.

To quantify the relation of A_{DC} with linearity, we define α as the LNTA topology-dependent

[3] An extra resistance R_{sh} parallel to $Z_{IN,BB}$ is also present in [**?**]. Since the value of R_{sh} is much larger than $|Z_{IN,BB}|$, it is ignored here.

constant indicating the fraction of the supply voltage V_{DD} needed to achieve the 1dB compression point given by:

$$\alpha = \frac{V_{IN,1dB}.G_{M_{LNTA}}.Z_{MXR}}{V_{DD}/2} \tag{5.3}$$

where $V_{IN,1dB}$ is the single-ended peak amplitude required to achieve the 1dB compression point. Based on (5.2), and (5.3), for low-frequency in-band signal, we can write:

$$\frac{1}{V_{IN,1dB}} = \left(\frac{G_{M,LNTA}}{\alpha.V_{DD}/2}\right).\left(R_{SW} + \frac{\xi.R_F}{A_{DC}}\right) \tag{5.4}$$

From (5.4), when R_{SW} is zero, $V_{IN,1dB}$ keeps increasing with an increase in A_{DC}, for a given R_F and $G_{M,LNTA}$. For a finite R_{SW}, $V_{IN,1dB}$ increases initially with an increase in A_{DC} and then saturates (Fig. 5.2). This trend indicates that for a given R_{SW}, a higher DC gain can result in increased linearity up to a certain A_{DC} value, dependent on the R_{SW} value. Note that increasing R_{SW} will increase the power consumption $P_{LO,MIX}$ of the LO drivers for the mixers. Alternately, for a given linearity, it is possible to reduce $P_{LO,MIX}$ by using an OTA with a higher DC gain.

5.3.2 Effect of Blocker-Filtering Bypass Capacitance, C_{BYP}

The wideband LNTA converts any incoming signal and blocker frequency into an RF current I_1 (Fig. 5.1(a)). Before this RF current is converted into the BB voltage at the TIA output, the blocker current should be filtered out. C_{BYP} acts as the first level of filtering for the OOB blocker. Current ratio I_3/I_4 in Fig. 5.1(a) is determined by the ratio of the impedance provided by C_{BYP}, to $Z_{IN,TIA}(\Delta f_{BLK})$. Increasing C_{BYP} reduces the input impedance for the OOB blocker, thus reducing

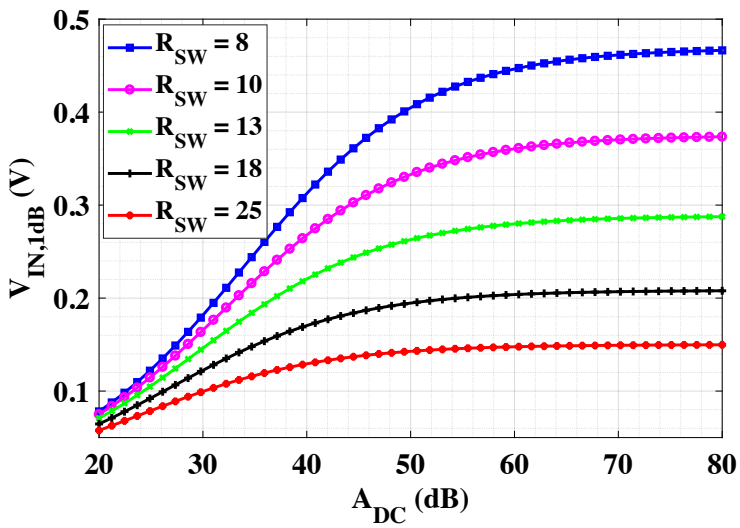


Figure 5.2: Variation of input linearity, $V_{IN,1dB}$, with the BB OTA's DC gain, A_{DC}, for various mixer switch on resistance, R_{SW}. Plotted for $\alpha = 0.5$, $\xi = 0.2$ for a receiver with 4-phase LO, $G_{M,LNTA}$=80mS, R_F = 2kΩ. For a given R_{SW}, linearity increases with an increase in A_{DC}.

$CG_{VIRT}(\Delta f_{BLK})$ and $CG_{OUT}(\Delta f_{BLK})$ and increasing B1dB as seen in Fig. 5.3(a). Size of C_{BYP} and TIA feedback-loop stability (Section 5.6) determine the upper limit of C_{BYP}.

5.3.3 Effect of OTA UGB

Blocker suppression at the output is required to avoid saturation of the BB-OTA. After first-order filtering by C_{BYP}, second-order filtering of the blocker at the output is provided by the OTA-RC filter created by the R_F, the C_F and the BB-OTA. It is possible to achieve third-order filtering at the output by using an OTA with a UGB comparable to f_{TIA}, instead of using a high-UGB OTA [**?**]. However, such third-order filtering comes at the cost of an increased $CG_{VIRT}(f)$ for frequencies around f_{TIA}. This is because reducing the UGB reduces the effective OTA loop gain near f_{TIA},

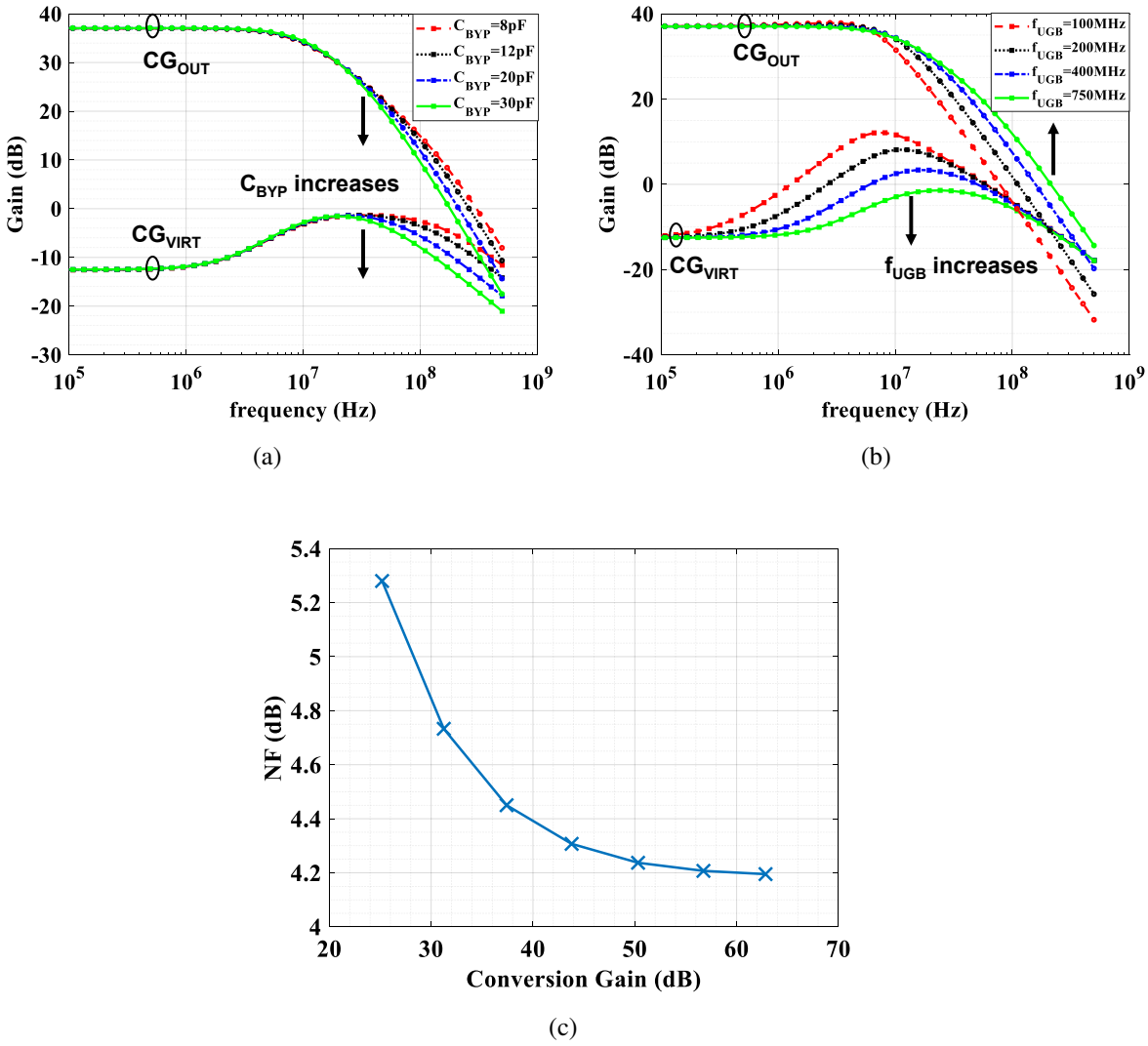


Figure 5.3: Simulation plots for (a) Conversion gain from the LNTA input to the TIA input, ($CG_{VIRT}(f)$), and to the TIA output, ($CG_{OUT}(f)$), with frequency for different values of bypass capacitor, C_{BYP}, indicating a reduction in both, with an increase in C_{BYP}, resulting in increased B1dB; (b) $CG_{VIRT}(f)$ and $CG_{OUT}(f)$ with frequency for different values of f_{UGB} indicating a trade-off between $CG_{VIRT}(f)$ and $CG_{OUT}(f)$ reduction based on UGB; and (c) noise factor (NF) with $CG_{OUT,IB}(f)$ indicating suppression of baseband noise with an increase in $CG_{OUT,IB}(f)$.

which is required to be high to keep the looking-in TIA-input-impedance low, thus increasing $CG_{VIRT}(f)$. This tradeoff is shown in Fig. 5.3(b).

In a VCO-OTA, the bandwidth can be chosen independently of other parameters (section 5.4.3), so it is possible to optimize the f_{UGB}/f_{TIA} ratio to achieve balanced contributions of $CG_{VIRT,IB}(f)$ and $CG_{OUT,OOB}(f)$ towards overall system linearity.

5.3.4 Effect of Feedback Resistance

For a current-mode receiver (Fig. 1(a)), IB conversion gain from input to output, $CG_{OUT,IB}(f)$, is proportional to the LNTA transconductance, $G_{M,LNTA}$, and the feedback resistance of the TIA, R_F, that converts the current back into voltage. Mathematically, we can write:

$$CG_{OUT,IB}(f) = \zeta \cdot G_{M,LNTA} \cdot R_F \tag{5.5}$$

where ζ is the ratio of current going into the TIA of a single LO phase branch relative to the total current generated by the LNTA and depends upon the number of LO phases. Providing a high $CG_{OUT,IB}(f)$ suppresses the BB noise. This can be understood by comparing the signal power at V_{OUT}, with the noise power from the TIA's OTA at V_{OUT}. To simplify the analysis, we consider the low-frequency component of the transfer functions, ignoring the capacitances. Assuming the LNTA to be a current source with finite impedance $R_{OUT,LNTA}$, the downconverted impedance including the effect of phases is shown in Fig. 5.4. If A_{DC} is high, then TIA input impedance is low, and most of the current flows into the TIA. Assuming $R_1 = R_{SW} + R_{OUT,LNTA}/\xi$ and the OTA

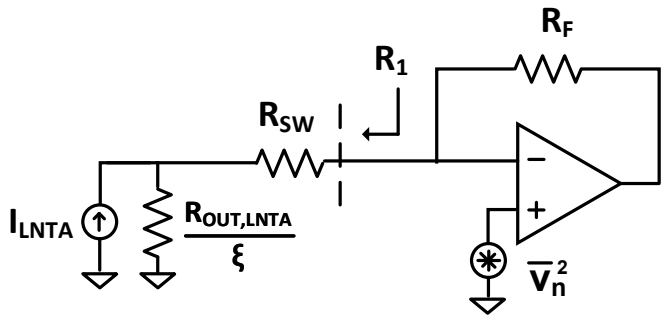


Figure 5.4: The BB TIA with the downconverted current model of the LNTA. R_F/R_1 ratio determines the amount of BB noise, $\bar{v}_n^2$, suppression.

input referred noise as $\bar{v}_n^2$, the SNR is given by:

$$SNR = \frac{(\xi G_{M,LNTA} R_F V_{IN})^2}{\bar{v}_n^2 \cdot (1 + \frac{R_F}{R_1})^2} \approx \begin{cases} \frac{(\xi G_{M,LNTA} R_F V_{IN})^2}{\bar{v}_n^2} & R_F << R_1 \\ \frac{(\xi G_{M,LNTA} R_1 V_{IN})^2}{\bar{v}_n^2} & R_F >> R_1 \end{cases} \tag{5.6}$$

In this equation, if $R_F << R_1$, then using (5.5), we can write:

$$SNR \approx \frac{(\xi . CG_{OUT,IB}(f) \cdot V_{IN})^2}{(\zeta . \bar{v}_n)^2} \tag{5.7}$$

For a given $G_{M,LNTA}$, increasing R_F can thus provide a higher $CG_{OUT,IB}(f)$ and hence a higher SNR. The benefit of increasing $CG_{OUT,IB}(f)$ to reduce NF for a given input referred noise of the OTA is shown in Fig. 5.3(c). At higher $CG_{OUT,IB}(f)$ as R_F approaches R_1, diminishing returns in NF improvement are obtained, as predicted by (5.6). Note that as R_F increases, C_F must be reduced to keep the Z_{TIA} bandwidth constant. The associated stability considerations are discussed later.

5.4 Benefits of VCO-OTAs over Inv-OTAs

A typical VCO-OTA consisting of two VCOs, a phase-frequency detector (PFD) and a charge pump (CP) with the compensation resistor and capacitor, R_C and C_C, is shown in Fig. 5.5 [66]. It transforms the input voltage from the voltage domain to the phase domain to the current domain and back to the voltage domain. The reader is referred to [59, 60, 66] for the detailed operation and stability considerations.

The voltage gain transfer function, $A_G(s)$, of a VCO-OTA from the differential input, $\Delta V(s)$, to the feedback node, $V_{FB}(s)$, in Fig. 5.5, can be written as (after [59]):

$$A_G(s) = \frac{V_{FB}(s)}{\Delta V(s)} \approx \frac{2\pi K_{VCO} K_{PD} K_{CP}(1 + sR_C C_C)}{s^2(C_C + C_L)(1 + sR_C \frac{(C_C C_L)}{(C_C + C_L)})} \tag{5.8}$$

where K_{VCO} is the VCO gain in V/Hz, $K_{PD} = 1/2\pi$ is the phase-detector gain and K_{CP} is the CP gain and is same as the CP current, I_{CP}. The compensation resistor, R_C, and capacitor, C_C, provide stability. C_L is the load seen by the opamp, which in this case is C_F.

The presence of two DC poles in (5.8) indicates that the VCO-OTA theoretically has an infinite gain at DC. The finite output impedance of the CP and the resistive loading at the output node, R_F along with C_C, shifts one DC pole to a low-frequency pole. All the benefits discussed next are however unaffected by this, so, for simplicity, we will assume two DC poles in the following discussion.

The VCO-OTA's pole-zero plot is shown in Fig. 5.6. For comparison, the open-loop gain of an inv-OTA modeled using a low finite DC gain, $A_{DC,INV}$, with a dominant pole at f_0 and the same

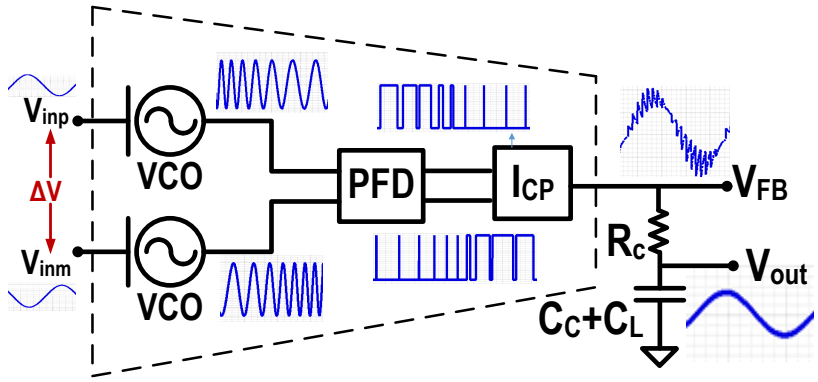


Figure 5.5: VCO-OTA architecture with typical waveforms.

UGB, satisfying (5.9) is also shown. Based on this, the three key benefits of using a VCO-TIA over the inv-OTA based TIA (inv-TIA) are explained next.

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_{DC,INV}}{\left(1+\frac{s}{2\pi f_0}\right)} \tag{5.9}$$

5.4.1 Scaling-Friendly High DC Gain

Owing to the frequency-to-phase conversion, a perfect integration is realized, and the VCO-OTA provides a theoretically infinite DC gain. Note that this gain is independent of the transistor's intrinsic gain and the supply voltage, both of which are decreasing with technology scaling. This can be contrasted with the inv-OTA and the cascoded OTA where high DC gain either relies on or is affected by the intrinsic device gain and the supply voltage.

Additionally, the VCO-OTA's power consumption decreases, and the UGB increases with scaling. The power is reduced because in a VCO-OTA, the VCO and the PFD power are mostly depen-

dent on intrinsic device self-loading. With scaling, for a given power consumption, it is possible to operate the VCO-OTA at a higher frequency, permitting a higher K_{VCO} and hence UGB (see (5.8)). Inv-OTA power requirements, however, are driven by the noise and the external capacitors and do not benefit much from scaling.

5.4.2 High Bandwidth for a Given Loop Gain

In the presence of two DC poles, the 40dB/decade gain roll-off is achieved for the VCO-OTA compared to the inv-OTA for a given UGB as shown in Fig. 5.6. This provides a lower $Z_{IN,TIA}(f)$ and $Z_{IN,BB}(f)$ for a larger IB signal bandwidth, thus providing high B1dB for a greater fraction of the signal bandwidth.

5.4.3 Independent Noise and UGB Selection

Section 5.3.3 discusses the benefit of using a finite UGB to achieve additional filtering provided by the OTA UGB thus increasing the linearity of the receiver. This becomes particularly important to achieve the necessary OOB suppression in a high $CG_{OUT,IB}(f)$ receiver. For a low-noise design, there is a minimum power requirement for the BB TIA's OTA to meet the noise specification. In a VCO-OTA, it is possible to independently reduce noise by increasing VCO power and K_{VCO} and control UGB using I_{CP}. But, an inv-OTA has a disadvantage because increasing power consumption to meet the noise requirements results in increased UGB and hence reduces the B1dB. Note that this decoupling aspect is not unique to the VCO-OTA; rather, it is a disadvantage of the inv-OTA.

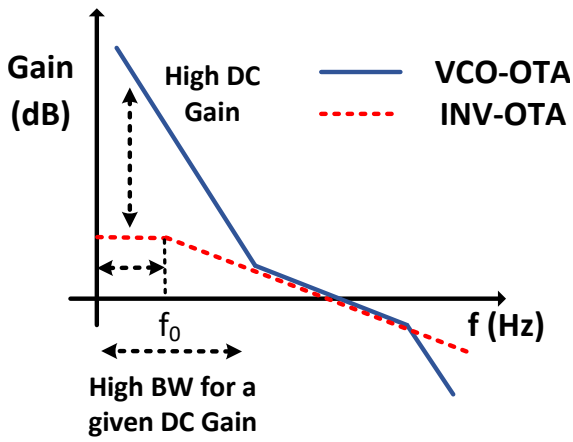


Figure 5.6: Comparison of the VCO-OTA's open-loop magnitude plot with the inv-OTA for the same UGB. The VCO-OTA achieves higher DC gain and can provide higher bandwidth for a given DC gain.

5.5 Receiver-Level Benefits of Using a VCO-TIA

Depending on the receiver requirements, it is possible to benefit from the three features by reducing power consumption of either the TIA, the mixer, or the LNTA. It is also possible to use any combination of these to realize a maximum power reduction benefit.

5.5.1 High Conversion Gain to Relax the TIA Noise Requirement

It is possible to increase $CG_{OUT,IB}(f)$ by increasing R_F and reducing C_F without increasing $|Z_{IN,TIA}|$ at low frequency due to the VCO-OTA's high DC gain. This can relax the TIA noise requirement (see Section 5.3.4) and hence reduce its power consumption. Increasing R_F increases $|Z_{IN,TIA}|$ around f_{TIA}, especially if a low-UGB OTA is used to achieve OOB rejection, however, based on the nature of the input signal spectrum, this might not be a problem if the adjacent channel require-

ments are not strict and most of the signal energy is concentrated at the lower end of the signal spectrum.

5.5.2 LNTA Power Reduction

Due to the high DC gain of the VCO-OTA, it is also possible to increase R_F and reduce $G_{M,LNTA}$ to achieve the same $CG_{OUT,IB}(f)$ and OOB linearity, while trading off LNTA power with increased receiver NF. Reducing $G_{M,LNTA}$ also increases the output impedance of the LNTA, thus increasing the maximum $CG_{OUT,IB}(f)$ limit (see Section 5.3.4). Note that this tradeoff is not available for inv-TIA because increasing R_F affects both linearity and NF.

5.5.3 LO Driver Power Reduction

For the same $CG_{OUT,IB}(f)$ as with the traditional OTA, the VCO-OTA can provide a reduced low-frequency $Z_{IN,TIA}(f)$. For a given low-frequency $Z_{IN,MXR}(f)$ value, it is therefore possible to increase the mixer on-resistance by reducing switch size (see Section 5.3.1), thus relaxing the LO driving requirement and reducing its power consumption.

5.6 Baseband VCO-TIA Design

We now discuss the steps to choose the VCO-OTA parameters such as K_{VCO}, I_{CP}, R_C, C_C and f_{UGB} for the receiver design. Since this parameter choice is a multidimensional problem, there is no single correct solution. In this section, we propose a set of guidelines to achieve a VCO-OTA

design with high B1dB linearity, balanced NF, and limited power consumption. We start with a discussion of stability for the BB TIA's OTA.

The VCO-OTA closed-loop gain, when used in the TIA configuration, is given by:

$$Loop\ Gain(s) = A_G(s) \times \left(\frac{1 + sR_F C_F}{1 + sR_F(C_F + C_{BYP})} \right) \tag{5.10}$$

where $A_G(s)$ is given by (5.8). The extra feedback pole and zero introduced in (5.10) must be considered while still obtaining sufficient phase margin. To achieve stability in the VCO-OTA, we need a zero just before the UGB. In a general VCO-OTA, R_C and C_C provide this zero. In the TIA design, we propose to use the zero provided by the feedback in (5.10) for stability, and use the compensation network zero due to R_C and C_C to cancel the feedback pole. The loop gain in (5.10) after the pole-zero cancellation becomes similar to (5.8) with two poles followed by a zero-pole pair configuration. The value of the required R_C is then given by:

$$R_C = R_F(C_F + C_{BYP})/C_C \tag{5.11}$$

To discuss the phase margin (PM), we first define a ratio κ for a VCO-OTA system:

$$\kappa = \sqrt{f_{p3}/f_z} \tag{5.12}$$

where f_z and f_{p3} are the zero and the pole used to stabilize the VCO-OTA system to the achieve PM. For a unity-gain configuration VCO-OTA, the PM is determined by the ratio of the compensation

zero to the third pole. This analysis is similar to the stability analysis of a second-order loop filter in a phase-locked loop (PLL) and has been addressed in detail in [59] and [84][4]. The maximum PM provided in such a case is

$$PM_{MAX} = tan^{-1}(\kappa) - tan^{-1}(1/\kappa). \tag{5.13}$$

This is achieved when $f_{p3} = \kappa \cdot f_{UGB} = \kappa^2 \cdot f_z$. As an example, a maximum PM of 45°/55°/60° can be achieved when κ^2 is chosen to be 6/10/14. Similarly, in (5.10), the stability is provided by the zero at the TIA frequency and the pole due to R_C and C_F. In this case, we define

$$\kappa_{CL} = f_{UGB,CL}/f_{TIA} \tag{5.14}$$

Based on this, we can derive

$$C_C = \kappa_{CL}^2 \cdot (C_{BYP} + C_F);\ R_C = R_F/\kappa_{CL}^2 \tag{5.15}$$

In this case, we can solve (5.10) to obtain the $K_{VCO} \cdot I_{CP}$ product as

$$K_{VCO} \cdot I_{CP} = \kappa^3 . \omega_{TIA}^2 \cdot (C_{BYP} + C_F) \tag{5.16}$$

For a VCO with a given output phase noise, the input-referred noise decreases with the increase in K_{VCO} [58]. A large K_{VCO} is therefore desired from the noise perspective. However, the minimum-

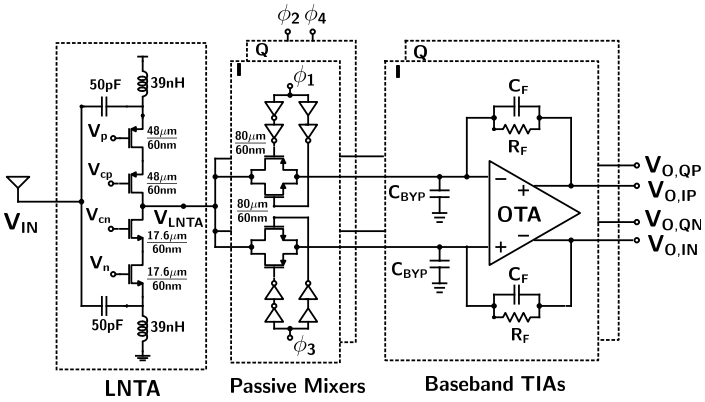
[4] In [84] the equivalent of κ is $\sqrt{b+1}$

1.	f_{UGB_CL} #	$f_{UGB\_CL} = \kappa * f_{TIA}$
2.	C_{BYP}	$\lvert Z_{C\_BYP}\rvert > \lvert Z_{MAX}\rvert \; at \; f_{TIA}$
3.	R_F	$> R_{OUT\_LNTA}/\xi + R_{SW}$
4.	C_F	$1/2\pi R_F \, f_{TIA}$
5.	C_C	$\kappa^2 * (C_{BYP} + C_C)$
6.	R_C	$R_F * (C_F + C_{BYP})/C_C = R_F/\kappa^2$
7.	f_{VCO}	$\kappa^3 * f_{UGB\_CL}$
8.	$K_{VCO} * I_{CP}$	$\kappa^3 * \omega_{TIA}^2 * (C_{BYP} + C_F)$
9.	K_{VCO}	$2 * f_{VCO}$
10.	I_{CP}	From 8,9

κ is related to maximum possible PM given by (13)

Table 5.1: Parameter selection guidelines for a VCO-TIA.

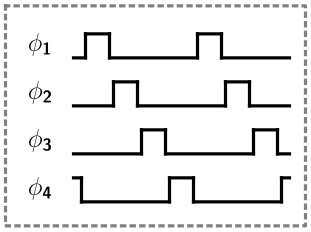
slew-rate requirement at the output of the TIA determines the minimum possible I_{CP}. Based on simulations, a balanced option is to choose K_{VCO} to be as $2 \cdot f_{VCO}$ per Volt. For example, for a VCO with 2GHz center frequency, K_{VCO} = 4GHz/V. I_{CP} can then be calculated using (5.16). To ensure that the continuous time analysis for the VCO-OTA holds true, a good choice of f_{VCO} is ten times the open-loop UGB: $\kappa^3 \times f_{TIA}$ for the proposed methodology. The above discussion is summarized in Table 5.1 and serves as guidelines. Based on the receiver requirements, further modifications can be made.



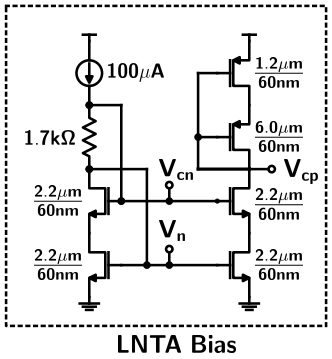
(a)

	Units	Rx1: VCO-TIA, High CG	Rx2: Inv-TIA, High CG	Rx3: Inv-TIA, Low CG
LNTA G_M	[mS]	20	20	20
TIA Feedback Resistor (R_F)	[kΩ]	16	16	4
TIA Feedback Capacitor (C_F)	[pF]	1	1	4
Next stage load (C_L)	[pF]	2	2	2
TIA Input Bypass Capacitor (C_{BYP})	[pF]	10	10	10
OTA Gain at DC (A_{DC})	[dB]	70	32	32
OTA Unity Gain BW (UGB)	[MHz]	200	200	400
OTA input referred noise	[nV/$\sqrt{Hz}$]	2.9	2.9	1.4

(b)



(c)



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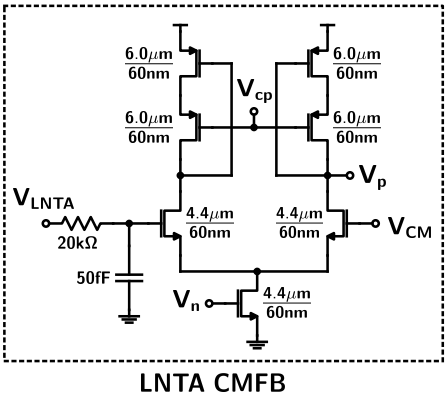
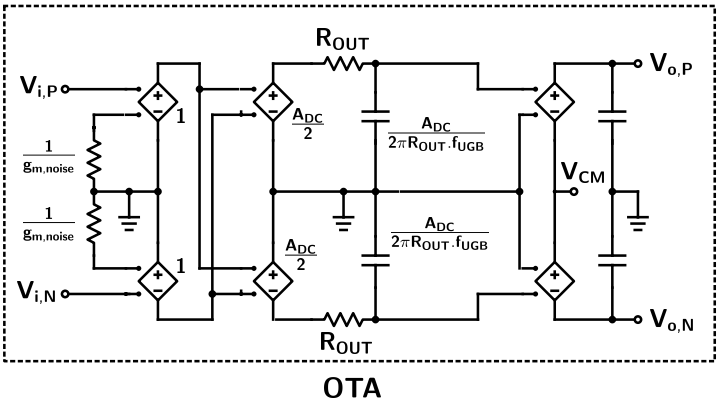


(e)



(f)

Figure 5.7: (a) Schematic diagram of the LNTA, the passive mixers, and the BB TIAs, (b) Receiver parameters used for simulating three types of receivers modeling VCO-OTAs and inv-OTAs, (c) Non-overlapping LO Clock Phases used to drive 4-phase mixers, (d) LNTA bias circuit, (e) LNTA common mode feedback circuit, and (f) OTA schematic used to model VCO-OTA and inv-OTA. (after [9])

5.7 Circuit Implementation and Simulation Results

5.7.1 Receiver simulations

To illustrate the design methodology, a current-mode receiver with a common-gate cascode LNTA, a four-phase passive mixer followed by a BB TIA as shown in Fig. 5.7 is implemented in a 65nm CMOS technology. The LNTA has a $G_{M,LNTA}$ of 20mS that provides a wideband input matching with a return loss of less than 10dB from 0.5GHz to 10GHz. The mixer on-resistance is designed to be 7.5Ω. Pseudo-differential single-pole behavioral models for a VCO-OTA and an inv-OTA are used to implement the BB TIA with a given DC gain, UGB, and an output swing of 2V differential peak to peak swing for a 1.2V supply.

Three receiver (Rx) designs with parameters given in Fig. 5.7(b) are simulated: (a) a VCO-TIA with a high $CG_{OUT,IB}(f)$ (Rx1); (b) an inv-TIA with a high $CG_{OUT,IB}(f)$ (Rx2); and (c) an inv-TIA with a low $CG_{OUT,IB}(f)$ (Rx3). Rx2 has similar power consumption as Rx1 at the cost of reduced blocker tolerance, while Rx3 has similar performance as Rx1 at the cost of increased power. PSS, PAC, and Pnoise analysis are used for CG and NF, while HB and HBAC analysis are used to find B1dB and IIP_3.

The conversion gain from the LNTA input to the TIA input, $CG_{VIRT}(f)$, and the TIA output, $CG_{OUT}(f)$, are plotted in Fig. 5.8 for the three designs. For in-band (IB) signals, a low $CG_{VIRT,IB}(f)$ and a high $CG_{OUT,IB}(f)$ is desired. $CG_{VIRT}(f)$ for the VCO-TIA design (Rx1) at low signal frequencies is much lower than the two inv-TIA designs, owing to the high DC gain, providing IB linearity benefit.

Section 5.2 shows that B1dB is a function of both Δf_{SIG} and Δf_{BLK} frequencies. For a closeby blocker placed at 5x f_{TIA} (Δf_{BLK} = 50MHz), when Δf_{SIG}=500kHz, Rx1 achieves a high B1dB of 0.5dBm compared to -11.4dBm and -4.4dBm for Rx2 and Rx3 respectively. This is expected because Rx1 has a low $CG_{VIRT}(f = 500kHz)$ indicating a high non-linearity suppression at the virtual ground node (thanks to high DC gain), even when $CG_{OUT}(f = 50MHz))$ is comparable for the three designs. For signal frequency close to the band edge (5MHz) B1dB for Rx1 is slightly worse (-5.6dBm) compared to Rx3 (-4.4dBm) due to higher $CG_{VIRT}(f = 5MHz)$ but much better than Rx2 (-12.2dBm) due to higher DC gain.

For blockers located further away at 30x f_{TIA} (Δf_{BLK} = 300MHz), B1dB is higher for all the three designs since the conversion gain at the output at the blocker frequency, $CG_{OUT}(f = 300MHz))$, is reduced. At Δf_{SIG}=500kHz, the three designs have B1dB of 6.9dBm, 5.3dBm and 6.4dBm respectively, and at Δf_{SIG}=5MHz, the B1dB numbers are 5.0dBm, 4.9dBm and 6.4dBm respectively. The B1dB trend amongst the three designs is the same as discussed earlier, but the effect is less pronounced because of the lower $CG_{OUT}(f = 300MHz)$.

IIP3 being a small signal parameter, is determined by the voltage swing at the TIA input node voltage, $V_{VIRT}(f)$. For small signal input, TIA output is linear and has a negligible contribution to IIP3. IB IIP3, therefore, follows $CG_{VIRT}(f))$ trend at the input tone frequencies (2MHz and 3.5MHz), with IIP3 for Rx2 (-0.3dBm) $<$ Rx1 (6.6dBm) $<$ Rx3 (8.0dBm). For OOB IIP3, C_{BYP} determines $Z_{BB}(f)$, and hence the voltage swing $V_{VIRT}(f)$. OOB IIP3 are therefore similar for Rx1 (7.6dBm), Rx2 (7.1dBm), and Rx3 (7.2dBm).

The simulated total power consumption of the LNTA and the LO driver for the mixer switches

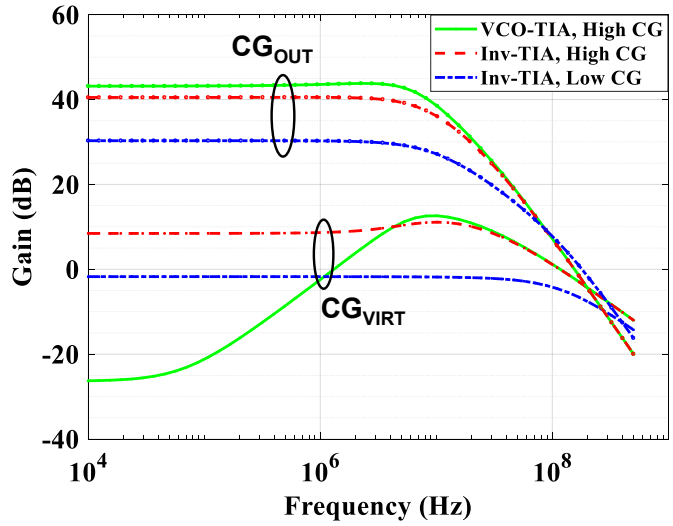


Figure 5.8: Simulated conversion gains from the input to the TIA input, $CG_{VIRT}(f)$, and the TIA output, $CG_{OUT}(f)$, for the three receivers.

at 2GHz are 1mW and 0.64mW respectively. The TIA power estimate is given in the appendix. For comparable power consumption, a VCO-OTA has more input-referred noise due to the presence of additional transistors used in the VCO to maintain a minimum current in the ring-oscillator, as shown in Fig. 5.9(a). However, the NF for the receivers is still comparable because of BB noise suppression due to high $CG_{OUT,IB}(f)$ when using a VCO-OTA. The NF, B1dB, IIP_3, and power estimates are summarized in Table 5.2. All the three receiver designs have similar NF. For slightly higher power consumption, better blocker performance is achieved in Rx1 compared to Rx2. For comparable blocker performance in Rx1 and Rx3, a power benefit of up to 2.6x in the TIAs and up to 2x in the overall receiver is achieved in Rx1 compared to Rx3.

The LNTA and the mixer LO driver powers are not adjusted in these cases for simplicity. In practice, they can provide additional power reduction advantage to the VCO-TIA design as described in Section 5.5.

	Units	Rx1: VCO-TIA, High CG	Rx2: Inv-TIA, High CG	Rx3: Inv-TIA, Low CG
Rx Noise Figure	[dB]	4.3	4.3	4.2
Rx Conversion Gain	[dB]	43.2	40.5	30.3
Rx B1dB	[dBm]	**0.5**[1]	**-11.4**[1]	**-4.4**[1]
		6.9[2]	5.3[2]	6.4[2]
		-5.6[3]	**-12.2**[3]	-4.4[3]
		5.0[4]	4.9[4]	6.4[4]
Rx IIP3	[dBm]	6.6[5]	-0.3[5]	8.0[5]
		7.6[6]	7.1[6]	7.2[6]
LNTA Power*	[mW]	1	1	1
Mixer Power*	[mW]	0.64	0.64	0.64
TIA Power#	[mW]	**2.92**	1.92	**7.68**
Total Rx Power	[mW]	**4.56**	3.56	**9.32**

[1] Δf_{SIG} = 500kHz, Δf_{BLK} = 50MHz
[2] Δf_{SIG} = 5MHz, Δf_{BLK} = 50MHz
[3] Δf_{SIG} = 500kHz, Δf_{BLK} = 300MHz
[4] Δf_{SIG} = 5MHz, Δf_{BLK} = 300MHz
[5] f_{Tone1} = 2MHz, f_{Tone2} = 3.5MHz
[6] f_{Tone1} = 50MHz, f_{Tone2} = 99.5MHz
* simulated # calculated

Table 5.2: Simulated performance for the three receivers.

5.7.2 Baseband VCO-TIA Simulations

In Section 5.7.1, we used a behavioral-OTA model for complete receiver simulation because of simplicity and ease of controlling OTA parameters. Full receiver simulations with transistor-level VCO-TIA are challenging because the periodic steady-state (PSS) and harmonic balance (HB) analysis do not converge due to the presence of two autonomous VCOs with a LO and an RF forced frequency. Hence, the CG, NF, and B1dB numbers would have to be found using very long transient simulations, which are challenging to iterate to derive trends. To demonstrate the VCO-TIA performance, BB simulations are done in a 65nm CMOS technology on a transistor-level VCO-OTA using the testbench shown in Fig. 5.9(a).

To illustrate the versatility of the VCO-TIA for use in both the CG and the CS path, a 10MHz BB VCO-TIA is designed for a 20MHz RF bandwidth CS path assuming 100mS $G_{M,LNTA}$ and thus

requiring a very low $Z_{IN_{BB}}$. The $CG_{OUT,IB}(f)$ of the receiver is chosen to be 50dB. Following the guidelines illustrated in Section 5.6, the values of R_F, C_F, C_{BYP}, f_{UGB} are chosen to be 3.183kΩ, 5pF, 10pF and 150MHz, respectively. Exact pole-zero cancellation is not used to reduce the size of the compensation capacitor. The f_{VCO}, K_{VCO}, I_{CP}, R_C, and C_C are chosen to be 2GHz, 5GHz/V, 2mA, 150Ω and 60pF. C_{LOAD} of 1pF is assumed to be part of C_C. The designed VCO-TIA block consumes 1.62mW at 1.2V supply.

Transient simulations are done to obtain the input impedance plots for the transistor-level VCO-TIA as shown in Fig. 5.9 on linear and logarithmic scales. A comparison with the input impedance of a transistor-level inv-OTA having a g_m of 2.8mS, and behavioral models for an inv-OTA and a two-stage OTA having 32dB and 52dB DC gain is also shown. For low frequencies, it is possible to achieve sub 1Ω impedance for the VCO-TIA compared to 67Ω in ideal inv-TIA, demonstrating the high DC gain property of the VCO-OTA. Low-frequency input impedance for transistor-level inv-TIA is limited to 392Ω due to resistive loading.

The impedance of the VCO-TIA is also below 70Ω for 10MHz bandwidth compared to 2MHz bandwidth in case of other OTAs for same UGB. This demonstrates that the VCO-OTAs have a higher bandwidth for a given DC gain of 32dB in this case, as discussed in Section 5.4.

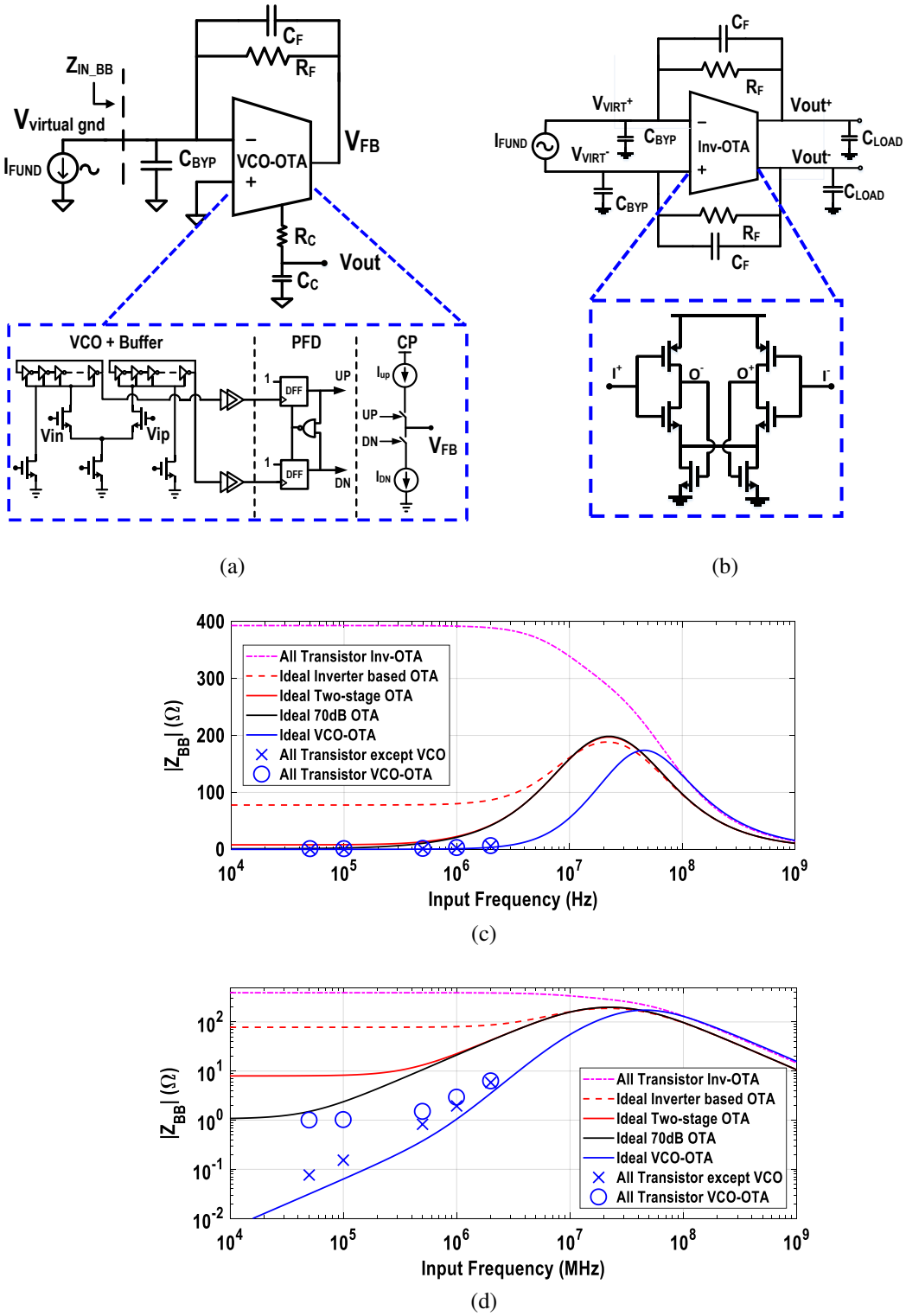


Figure 5.9: Testbench and schematics used for BB input impedance simulations for (a) VCO-OTA, (b)Inv-OTA (after [10]). (c,d) Simulated magnitude of the input impedance of BB-TIAs realized with different OTAs plotted on linear (c) and logarithmic (d) magnitude scales.

5.8 Second-Order Effects in the VCO-TIA

5.8.1 Limitation on DC Gain

A VCO-OTA can, in theory, achieve infinite DC gain due to the VCO's perfect frequency-to-phase integration. During transistor-level simulations, however, it is difficult to observe DC gain beyond a certain limit. This is because the TIA's virtual ground node voltage contains both the suppressed low-frequency input tone and a large high-frequency VCO tone, requiring long, high-accuracy simulations. Since linearity benefits provide diminishing returns with an increase in DC gain (Fig. 5.2), a compromise between simulation accuracy and time is used to showcase 70dB DC gain by demonstrating sub-1Ω TIA input impedance (see Fig. 5.9).

5.8.2 Effect of Frequency Mismatch Between the VCOs

In a VCO-OTA, due to layout-related mismatches, it is possible to have a frequency mismatch between the center frequencies of the two VCOs. During the closed-loop operation, the frequency mismatch is compensated in the form of input offset in the closed loop. This offset, however, does not limit the VCO-OTA's high-DC-gain characteristic. This is similar to the case of a traditional amplifier where the DC gain is independent of the offset voltage seen at the amplifier input, which results in a slight shift in the operating point between the two input terminals.

5.8.3 Effect of VCO-OTA Spurs

Any oscillator-based system, such as the VCO-OTA, produces spurious tones around the center frequency of oscillation. However, since the VCO frequency is much higher than the TIA frequency, it is possible to filter out the spurs with a simple first-order filter. The specific VCO-OTA topology discussed in this chapter, where the output is taken after the compensation resistor, provides first-order filtering and attenuates the spur due to the VCO [60]. Further filtering can be included in the analog or digital domain as necessary.

5.8.4 Effect of Process, Voltage, and Temperature (PVT) Variation

The center frequency of the VCOs in a VCO-OTA is determined by the current provided to the VCO and its capacitive loading. It is possible to provide a PVT-independent current using a differential pair implementation, as illustrated in this chapter. The variation of MOSFET loading capacitance is not much if the region of operation is not changed. Similarly, it is possible to control the CP current using a current mirror, making it independent of PVT variations. Hence, if appropriately designed, it is possible to achieve PVT-invariant properties for the VCO-OTA.

5.8.5 Size of the Compensation Capacitor

One of the limitations of the VCO-OTA is the use of large compensation capacitance, C_C thus requiring large silicon area. The problem is similar to a second-order PLL system where large capacitor values limit the minimum achievable area. As part of future work, capacitor reduction techniques as applied to a second-order PLL [61, 62] can be explored to provide area savings.

5.8.6 Effect of Loading at the OTA output:

The OTA transfer function has been modeled as a first-order response with a DC gain A_{DC} and unity-gain frequency f_{UGB} to calculate the closed-loop gain in (5.10). In practice, a resistive load at the output of an OTA results in complex analytical equations. However, for high conversion gain receivers like the ones used in this chapter, R_F is high compared to the output impedance of the OTA. Hence the loading effect can be ignored, so (5.10) still holds.

5.9 Chapter Summary

In this chapter, we have presented the use of VCO-OTA based TIAs as an alternative to the inv-OTA based TIAs in a wideband blocker-tolerant current-mode receiver to achieve power reduction in the receiver for given noise and linearity requirements. The three key benefits of a VCO-OTA over inv-OTA namely a high DC gain, a high signal bandwidth for a given DC gain and UGB, and possibility to adjust noise and UGB of the OTA independently have been used to achieve power reduction in the receiver.

Simulation results comparing a 20MHz RF bandwidth wideband receiver operating at 2GHz using VCO-TIA and inv-TIA are presented as a design example. When compared to the latter, the former demonstrates up to 12dB B1dB improvement for slightly higher power consumption, or up to 2.6x power reduction in the baseband TIA resulting in 2x overall receiver power reduction for a comparable noise factor and out-of-band blocker tolerance.

Chapter 6

Other Applications and Design Techniques for VCO-OTAs

In this chapter, we present two other applications of VCO-OTAs in a low-dropout regulator (LDO) and a filter design. We also discuss techniques for reducing spurs in VCO-OTAs, trading linearity for reduced power consumption, and designing a 0.2V VCO-OTA.

Section 6.1 presents a VCO-OTA used as an integrator to design a high-efficiency LDO. Due to integrator based architecture, the LDO has lower input voltage, better load regulation, and lower dropout voltage resulting in higher efficiency compared to traditional operational-amplifier based implementations. The proposed LDO is fabricated in 180nm CMOS technology along with with a traditional operational-amplifier based design for comparison. The proposed capacitor-free LDO consumes a power of 3.7W at 0.8V input and achieves a dropout voltage of 100mV with load regulation of 8.8V/mA.

Section 6.2 presents performance improvement techniques for VCO-OTAs using Butterworth filter design as an application. An on-off charge pump(CP) topology is used as an alternative to power-hungry current-steering charge pump used in earlier VCO-OTAs. This topology brings down the power consumption of the CP and also the phase frequency detector (PFD) used in VCO-

OTAs. We also present the use of inherent low pass filtering in VCO-OTAs for out-of-band spur reduction. The techniques have been demonstrated by prototyping a 4-MHz $4^{\mathbf{th}}$ order active-RC filter using VCO-OTAs. The filter prototype, fabricated in 180nm CMOS technology, shows a power reduction of 41% in the CP and 25% in the PFD, achieved by trading off in-band IIP3 from 21dBm to 19dBm and noise from $0.71\text{mV}_{\mathbf{rms}}$ to $0.75\text{mV}_{\mathbf{rms}}$.

Section 6.3 presents a 0.2V VCO-based OTA (VCO-OTA) for low-voltage, low-power applications. As discussed in chapter 3, it is possible to scale down the supply of time-domain circuits (here VCO-OTA) to really low voltages. However, the CP requires a minimum headroom, presenting a challenge in voltage scaling. The proposed architecture eliminates current sources used in the charge pump to design a 0.2V VCO-OTA. Simulations show that in unity gain configuration, the proposed architecture achieves 60kHz unity-gain bandwidth and $207\mu V_{RMS}$ input-referred noise while consuming 492nW power.

6.1 Application of VCO-OTAs in a Low-Dropout-Regulator[1]

6.1.1 Background

Voltage regulators play an important role in electronic systems. Low dropout voltage regulators (LDOs) are popular when output voltages are close to input voltages. There are various architectures of LDOs but traditional implementations use an operational-amplifier and a common-source power transistor [85–88].

[1]This project was done in collaboration with Sanket Gupta and Zhongjie Dai and published in ISCAS [7]

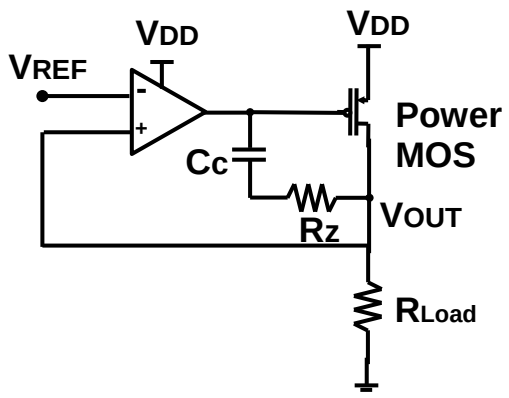


Figure 6.1: Traditional implementation of LDO with an op-amp

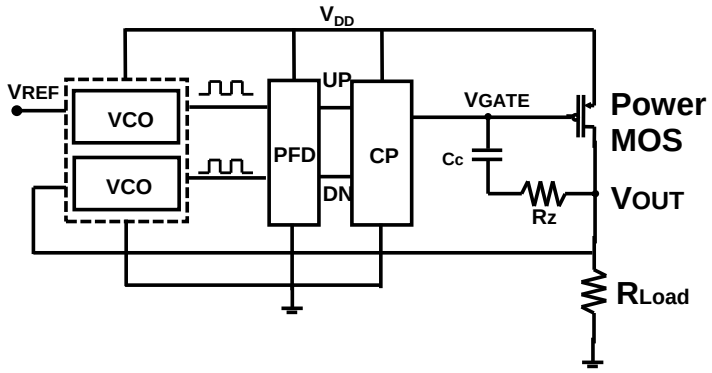


Figure 6.2: Functional block diagram of the VCO-based LDO

The DC gain for an operational amplifier is limited which leads to constant voltage difference at the output with respect to reference voltage. On the other hand, as the integrator based error-amplifier performs the integration of the voltage, it can provide an infinite DC gain which leads to zero steady-state error at the output.

Several architectural improvements have been proposed for the performance of LDOs [86, 89, 90]. However, since these designs still rely on an operational amplifier to provide the necessary loop gain; this limits the accuracy as well as minimum possible quiescent current in operation. Integrator-based approach, on the other hand, consumes lower power, provides higher accuracy, and can also support a digital-controlled loop [91]. However, this design is limited by its efficiency, line regulation, and settling time. In this section, a modified architecture of an integrator-based LDO is proposed. The LDO uses voltage-controlled oscillators (VCOs), an improved current-steering charge pump with unit buffer resulting in better line regulation, a voltage mapping network resulting in higher efficiency, and an input voltage of as low as 0.8V. A current DAC is included in the charge pump for external optimization.

6.1.2 VCO-based LDO Architecture and Building Blocks

The architecture of the proposed LDO is presented in Fig. 6.2. The LDO output voltage V_{OUT} is compared to the reference voltage V_{REF} and converted into the frequency with two differential voltage-controlled oscillators (VCOs). The phase-frequency detector compares the oscillator outputs and generates UP and DOWN pulses carrying the phase difference information, which corresponds to the integral of the difference of the voltage inputs. The charge pump (CP), then,

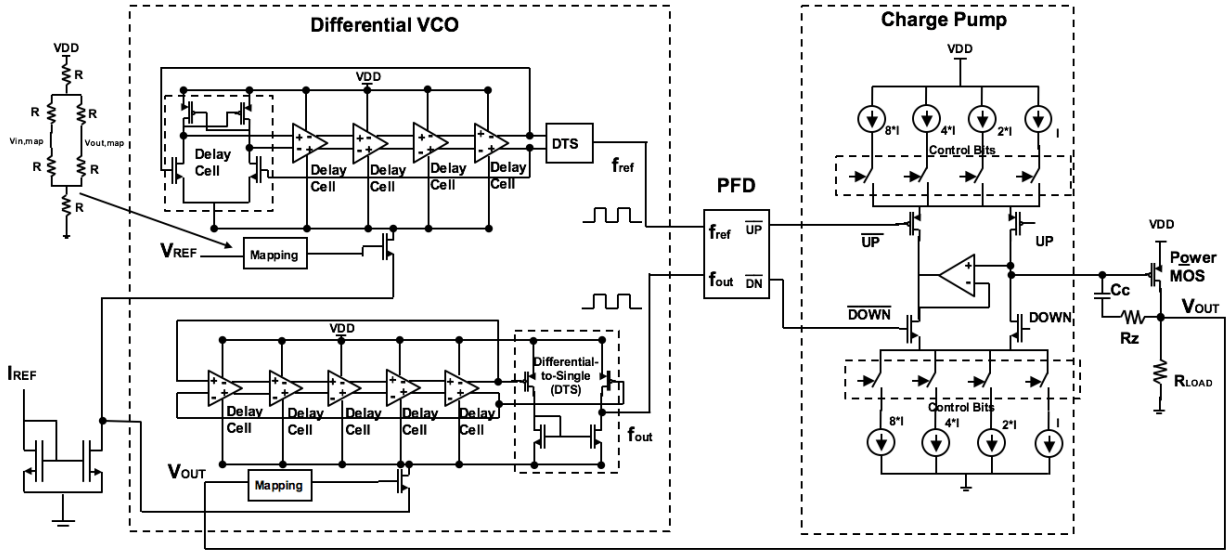


Figure 6.3: Circuit block diagram of the VCO-integrator-based LDO

converts the pulses back to current, which is then converted to a voltage V_{GATE} (Fig. 6.2) at the gate of the common-source power transistor. The transistor provides the load current, and the loop enables voltage regulation at the output.

Voltage-Controlled Oscillator (VCO)

The function of the VCO is to convert the voltage into frequency information while providing a gain K_{VCO}. This conversion is done by first converting both the reference voltage and output voltage to differential currents, which are used to bias the differential VCO. Each VCO consists of a five-stage ring oscillator followed by a differential-to-single-ended converter. The VCO oscillation frequency is proportional to the biasing current. The nominal frequency is designed to be more than ten times the loop bandwidth.

Current-Steering Charge Pump with Current DAC

The charge pump converts the output of the Phase Frequency Detector (PFD) into a current that charges or discharges the gate of the power transistor. The main design goal with the charge pump is to deliver matched currents with minimum ripple to the output. A current-steering charge pump was used to ensure that the current sources do not entirely turn off so that the voltages at the drains of the current sources are always kept around V_{GATE} (Fig. 6.3). Therefore, we can minimize charge injection and turn-on time. A unit buffer was also added between the two current steering branches to ensure that the ripple is minimized by forcing the idle branch to follow the output branch. It is worth spending the extra power for the buffer since the peak-to-peak ripple at V_{GATE} can be minimized from 5mV to 0.05mV based on simulations. A 4-bit current DAC is added to provide external digital control of power and bandwidth. As the bandwidth is directly proportional to the charge pump current, having 4-bit control allows an external tuning of bandwidth by over a decade of the frequency range.

Mapping Network and Phase Frequency Detector (PFD)

A mapping network consisting of six resistors is used after V_{REF} and V_{OUT} before feeding back into the loop. This network ensures that the VCO can operate at voltages close to V_{DD} without a significant drop in Kvco, thus supporting a low-dropout voltage at the output. The mapping network implements the following relationship: $V_{OUT,map} = 0.25*V_{DD} + 0.5*V_{IN,map}$ where with $V_{IN,map}$ and $V_{OUT,map}$ refer to the voltages at the input and output of mapping network. This does not affect the line regulation performance as it is placed after both V_{REF} and V_{OUT}.

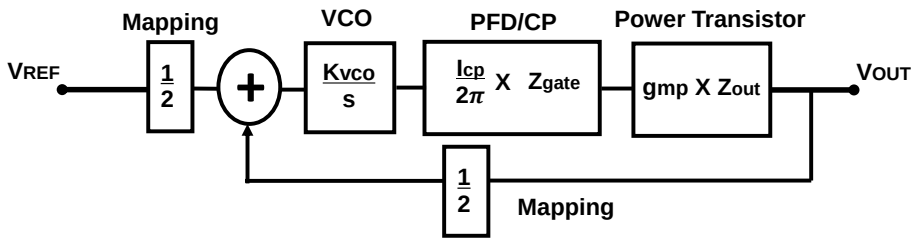


Figure 6.4: Linear model of the VCO-based LDO

Phase Frequency Detector (PFD)

The PFD was implemented with the traditional configuration of is a traditional implementation consisting of two D Flip-Flops and an AND gate.

6.1.3 Loop Analysis

The Integrator is used as an error amplifier which creates a pole at DC in the loop transfer function and this results . This contributes toin a 20-dB roll-off at low frequencies DC. This LDO is designed to be capacitor-free, hence so it is necessary to ensure that the dominant pole is placed at an appropriate location inside the loop to ensure stability across all possible load currents. The Miller capacitor (C_c) (Fig. 6.3) is used to place the dominant pole at the gate of the power transistor. This pole placement creates another pole at DC, leading to a 40-dB roll-off at low frequencies. Fig. 6.4 presents the linear model of the proposed LDO. The open-loop transfer function is presented below:

$$H(s) = \frac{K_{vco}}{s} \times \frac{I_{cp}}{2\pi} \times Z_{gate} \times g_{mp} \times Z_{out} \tag{6.1}$$

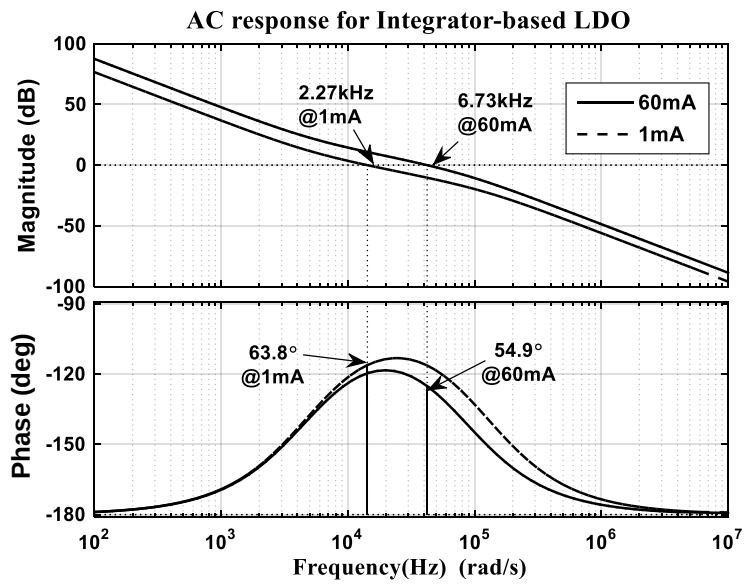


Figure 6.5: Bode plot of the loop-transfer function of the VCOBased LDO with different loads

where K_{VCO} is the gain of the VCO, Icp is the charge-pump current, gmp·Zout is the gain of the power transistor and Zgate is the impedance at the gate of the power transistor, which is shown below:

$$Z_{gate} = \frac{R_Z C_C s + 1}{s(1+A)\left(C_{gd}(R_Z C_C s + 1) + C_C\right) + sC_{gs}(R_Z C_C s + 1)} \tag{6.2}$$

In order to stabilize a loop with two poles at DC, it is necessary to bring a left-half plane zero before the unity-gain bandwidth (UGBW) point to create a phase lead. Resistor R_z is placed in series with the Miller capacitor to create the zero at $1/(R_z \cdot C_c)$ (Fig. 6.3). The parasitic capacitances of the power transistor, Cgs, and Cgd, create the third pole. Due to the possible instability arising due to this pole, it is critical to place the zero to maximizes the phase margin of the loop. Fig. 6.5 shows the use of zero in this design to compensate for the loop. The LDO is stable across all loads,

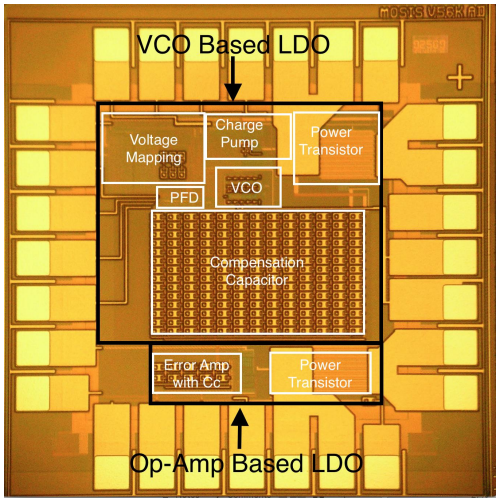


Figure 6.6: Die photograph of the VCO-based and traditional LDOs

with the best case phase margin of 65 degrees at UGBW. The digital compensation using the 4-bit current DAC in charge pump allows external tuning of UGBW.

6.1.4 Experimental Results

The proposed LDO has been implemented on a test chip in a 180nm CMOS technology (Fig. 6.6). On the same chip, a traditional LDO with an OTA as its error amplifier has been included for performance comparison. In order to make a fair comparison, the power transistor sizing and layout of both were exactly the same.

Table 6.1 shows that the VCO-based design can support output voltage of upto 0.8V compared to 1.2V and provides lower dropout voltage of 100mV compared to 150mV for traditional design. It also has better load regulation: 8.8V/mA compared to 29V/mA while consuming lower quiescent power: 3.7W compared to 30W. The traditional design has lower settling time that is possible due

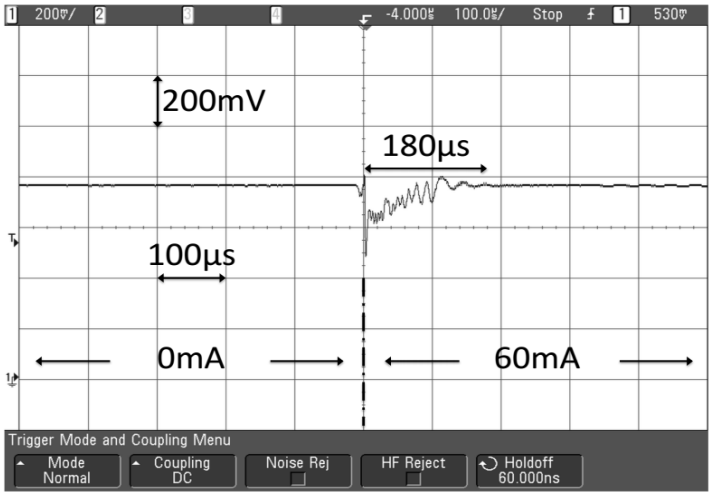


Figure 6.7: Transient response when switching from 0mA to 60mA.

to its higher bandwidth but it comes at a cost of higher power. Due to the critical nature of the zero for stability of VCO-based design, C_c and hence area is larger.

Fig. 6.7 shows the transient response of the proposed LDO. This design has a slower settling time, but this can be improved by increasing the loop bandwidth. A strategy would be to add extra circuitry to improve transient response by detecting the output spike [90]. Another strategy would be to increase the charge pump current as well as to decrease R_z to increase the bandwidth while keeping a sufficient phase margin.

6.1.5 Comparison to the State of the Art

Table 6.1 compares the presented design to other state-of-the-art sub-1V LDO designs. Compared to the previous implementation of VCO-based LDO design [91], the input voltage, line regulation, chip area, and settling time has improved in this design.

As compared to other sub-1V designs [86–88], the input voltage of the proposed LDO can go

	VCO-based LDO	Traditional Opamp-based LDO
Input Voltage	0.8V-2V	1.2V-2V
$\mathbf{V_{dropout}}$	100mV @ 60mA	150mV @ 60mA
Power Consumption	3.7µW @ 0.8V	30µW @ 1.2V
Load Regulation	8.8µV/mA	29µV/mA
Line Regulation	1.8%	0.4%
$\mathbf{t_{settling}}$**(0-60mA)**	180µsec	20µsec
Area	0.596mm^2	0.119mm^2

Table 6.1: Comparison of the measured response of the VCO-based LDO and opamp-based LDO designed on the same chip.

to 0.8V while still supporting a drop-out voltage of 100mV at 60mA load current. In designs with error amplifiers [85, 86, 89, 92], load regulation is limited by gain. In this design, high gain due to integrator results in much better load regulation of 8.8uV/mA. The proposed LDO also provides better current and power efficiency compared to [86, 88, 90], which consume a lot more power but achieve a lower efficiency. The proposed LDO can support 60mA load current with improved performance in power, load regulation and efficiency compared to [85, 88, 90, 92].

The proposed LDO has good performance in quiescent power, efficiency, and load regulation. The almost infinite DC gain due to the integrator-based design provides sufficient loop gain even when the power transistor is in the deep linear region. The current-steering charge pump with unit buffer results in better line regulation. The voltage mapping network helps sustain lower dropout

Author Last name	Chen	Lee	Wang	Guo	Or	Chen	Chong	Tan	This work VCO-LDO
Conf./Journal	APCCAS	MWSCAS	ICGCS	JSSC	JSSC	ISSCC	VLSI	JSSC	**ISCAS**
Year	2008	2010	2010	2010	2010	2014	2014	2014	**2016**
Technology (μm)	0.35	0.065	0.09	0.09	0.35	0.021	0.065	0.065	**0.18**
Chip Area (mm²)	0.8983	N/A	0.0027	0.019	0.155	0.015	0.0096	0.0133	**0.596**
V_{IN}(V)	0.9-2	0.9-1.2	1-1.2	0.75-1.2	0.95-1.4	0.65-0.9	0.75-1.2	0.75-1.2	**0.8-2**
V_{OUT} (V)	0.3-0.7	0.7-1	0.9	0.5-1	0.7-1.2	0.6	0.5	0.55	**0.7**
$V_{dropout}$ (mV)	200	200	100	200	250	50	250	200	**100**
$I_{Quiescent}$ (μA)	0.1325	N/A	9.3	8	14-43	5	16.2	15-487	**4.6**
I_{OUT} (max) (mA)	120	100	50	100	100	10	50	50	**60**
Loading Cap. (nF)	N/A	0-0.1	0-1	N/A	0-1	<0.1	0-0.1	0.47-10	**0-1**
Line Reg. (mV/V)	156.16	4.4	14	3.78	N/A	16	N/A	4	**18**
Load Reg. (μV/mA)	0.629	21	82	100	400	500	560	180	**8.8**

Table 6.2: Comparison with the State-of-the-art sub-1V LDO designs.

voltages resulting in higher efficiency. An input voltage of as low as 0.8V can be therefore achieved at much lower quiescent power.

Compared to the previous implementation of this VCO-based LDO design [91], the dropout voltage, line regulation, and settling time have improved. There exists a fundamental trade-off of dropout voltage vs. maximum output current and quiescent power vs. settling time. The proposed LDO has a significant improvement in line regulation and has a lower ripple due to unity gain buffer used in the charge pump. The voltage mapping allows the output voltage to reach as high as V_{DD} without losing more than half K_{VCO}, unlike [91] which has higher dropout voltage. The dropout voltage of the proposed LDO is limited by the power transistor size given the same loading current. Among all the state-of-art LDO designs, this work also has good performance in low quiescent power, and good load regulation. Thanks to the infinite DC gain, there is sufficient loop gain even when the power transistor is in the deep linear region. Because of low quiescent current,

the settling time of this design is poor but can be improved by expanding the bandwidth of the loop. A good strategy would be increasing the charge pump current as well as decreasing the compensation resistor R_z to simultaneously increase the DC gain and the bandwidth while keeping sufficient phase margin. Another disadvantage is the use of a large compensation capacitor. Using active-zero compensation can help mitigate this issue.

6.1.6 Section Summary

Experimental results show that the VCO-integrator-based LDO performance exceeds the performance of traditional LDO on the same chip in several key parameters such as power, efficiency, and accuracy. It also exceeds the performance in several parameters compared to other LDOs in the sub-1V range. The integrator-based approach for LDO is a promising way of implementing in low-power high-efficiency systems such as for biological and space applications.

6.2 Reducing Power Consumption and High-Frequency Spurs in VCO-OTAs[2]

6.2.1 Background

The importance of time-domain based circuits is growing in scaled CMOS technologies [6]. It is therefore essential to understand the underlying performance trade-offs involved in their design. Ring-oscillator-based VCOs are versatile time-domain circuits. A variety of blocks such as integrators, opamps and ADCs have been designed using this block [58, 59, 68]. The VCO's inherent property of voltage to phase integration provides infinite gain at DC. This high gain makes VCO-OTAs ideal candidate for error amplification in negative feedback systems. The drawback of the VCO-OTA proposed in [59] is high power consumption in the CP block. Also, an external RC filter was proposed to be used to reduce the out-of-band spurs.

This section focuses on power reduction and inherent spur reduction techniques for VCO-OTAs. This is achieved by (a) reducing the CP power by replacing current-steering CPs with on-off CPs; (b) reducing the PFD power by decreasing the number of switches driven by it, and (c) reducing out-of-band spurs by taking the output from the low-pass node inherent to VCO-OTAs. The section also discusses the power-linearity trade-offs associated with using on-off CPs instead of current steering CPs. A 4-MHz 4th order active-RC filter employing VCO-based OTAs is presented to demonstrate the design trade-offs.

[2]This project was done in collaboration with Shravan Siddharth Nagam and published in ISCAS [60]

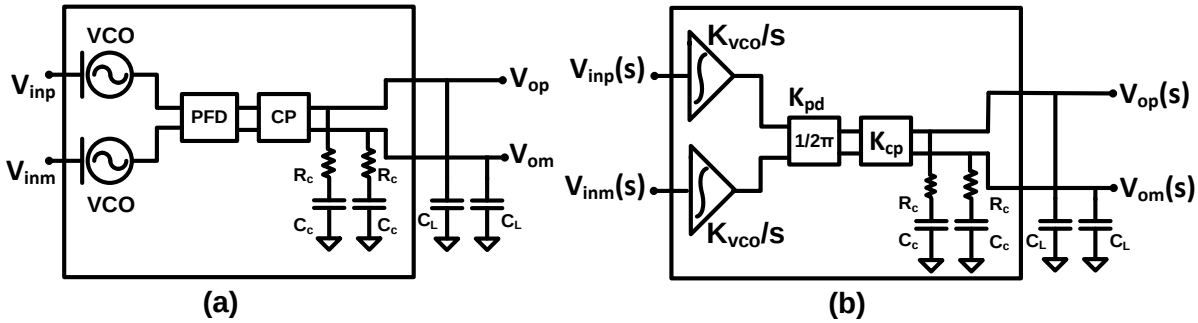


Figure 6.8: (a) Block diagram of VCO-OTA and (b) Phase-domain model of VCO-OTA

6.2.2 Important Parameters for VCO-OTAs in Negative Feedback Systems

Fig. 6.8(a) demonstrates the block diagram of the VCO-OTA topology [59]. It consists of a voltage-controlled oscillator (VCO), a phase-frequency detector (PFD), and a charge pump (CP). The equivalent phase-domain model is shown in Fig. 6.8(b). The transfer function for the VCO-OTA, can be derived as follows [59]:

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{4\pi K_{vco} K_{pd} K_{cp}(1+\frac{s}{\omega_z})}{s^2 C_c(1+\frac{s}{\omega_{p_3}})} \tag{6.3}$$

where $\omega_z = 1/R_cC_c$, $\omega_{p_3} = 1/R_cC_L$, K_{vco} is the VCO gain, $K_{pd} = 1/2\pi$ is the phase detector gain, K_{cp} is the charge pump gain and R_c, C_c and C_L are compensation resistor, compensation capacitor and load capacitor respectively.

The transfer function in (6.6) has one zero and three poles – two at the origin and the third at ω_{p_3}. The zero at ω_z created by R_c and C_c stabilizes the negative feedback system in which the VCO-OTA will be used. This methodology has been described in detail in [59] and is also a standard technique in Type-II phase-locked loop (PLL) design.

To achieve higher unity-gain bandwidth, it is imperative to have high values of K_{vco} and K_{cp}.

After exhausting the maximum achievable K_{vco} for a given technology, it is desirable to achieve higher values of K_{cp} with minimal power penalty. The following section discusses how to achieve this and the associated power-linearity trade-offs.

6.2.3 Proposed Design Improvements

On-off CP for Power Reduction

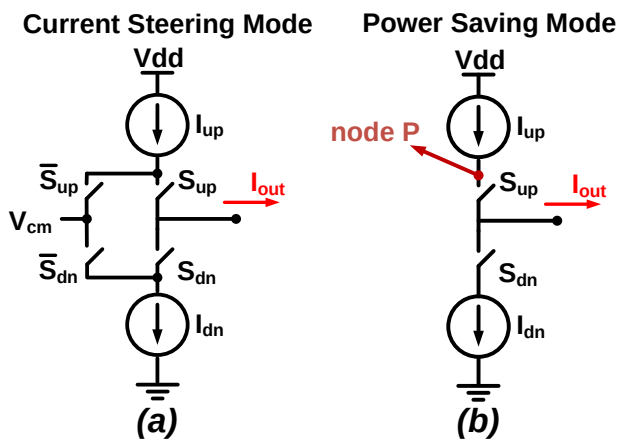


Figure 6.9: (a) Current Steering Mode (CSM) CP consuming constant DC power (b) On-off Power Saving Mode (PSM) CP consuming signal dependent power

In context of PLLs, two types of CPs: current-steering CP and on-off CP are commonly used [93]. The conceptual representation of current-steering CP topology used in [59] is shown in Fig. 6.9(a). This topology is referred to as current steering mode (CSM) for the remainder of the section. In CSM, both the current sources (I_{up} and I_{dn}) are always ON. When the CP gets an input from the PFD, switches S_{up} or S_{dn} are turned ON, and the current is either pushed into or pulled from the output node. For the remainder of the VCO cycle, current from both the sources is steered

away into a DC node (V_{cm}). This mechanism is provided to have a sharp rise and fall times for the output current, which is beneficial from a linearity standpoint, as discussed later.

It is important to note that this CP, as part of the VCO-OTA is to be used as an error amplifier in a negative feedback system. This means that the input to the VCO-OTA is not a full-swing signal, but a small error signal. The error voltage (ΔV) at the amplifier input is converted to a time difference (ΔT) between the Up and the Down pulses of the PFD. The time difference ΔT is now converted into an output current I_{out} by the charge pump. Since ΔV is small, the input to the CP (ΔT) is also relatively small compared to the VCO period. Therefore in CSM, current from the sources I_{up} and I_{dn} is utilized only during this short ΔT time and is wasted for the remainder of time (T_{vco} - ΔT).

In the on-off CP architecture, to be referred as Power Saving Mode (PSM) (Fig. 6.9(b)), the CP is simply switched off during the idle period (T_{vco} - ΔT). This results in major power reduction in the CP as $T_{vco} - \Delta T >> \Delta T$. This mechanism of on-off, however, results in a slower transition of output currents as the current sources have to be brought out of the off-state and generate current each time they are needed. This slower transition results in a linearity trade-off as discussed below.

Effect of Finite CP Transition Time on Linearity

For a given ΔT, if A is the area under the curve (Fig. 6.10(a)), then the average CP current $\bar{I}_{out}$ over a given VCO period T_{vco} and the corresponding charge pump gain K_{cp} can be derived as:

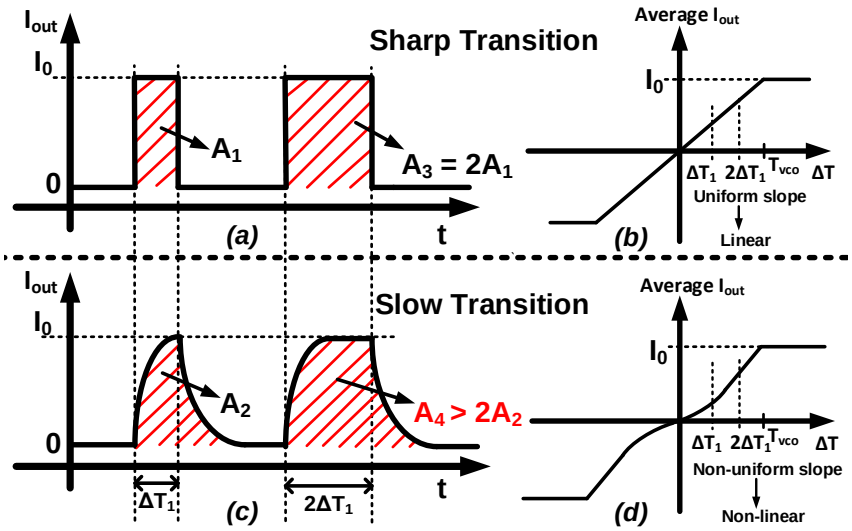


Figure 6.10: Linearity trade-off: Sharp transitions (a) result in a linear transfer curve (b) and Slower transitions (c) result in non-linear transfer curve (d).

$$\bar{I}_{out} = \frac{A}{T_{vco}} \tag{6.4}$$

$$K_{cp} = \frac{\bar{I}_{out}}{\Delta T} = \frac{A}{\Delta T \cdot T_{vco}} \tag{6.5}$$

To consider the effects on linearity due to the transition time, two scenarios are presented. The first scenario (Fig. 6.10(a)) consists of an ideal sharp transition and the second one (Fig. 6.10(c)) consists of a slow transition. In the first scenario, doubling the value of ΔT from ΔT_1 to $2\Delta T_1$, exactly doubles the area under the curve, hence giving a linear $\bar{I}_{out}$ (Fig. 6.10(b)). This gives a constant charge pump gain K_{cp} (from (6.5)). In the second scenario however, doubling ΔT does not result in exact doubling of the area under the curve, hence giving a non-linear $\bar{I}_{out}$ (Fig. 6.10(d)).

This means the charge pump gain K_{cp} varies with different values of ΔT, thus introducing non-linearity.

The effect of this slower transition is mitigated in Type-II PLLs by providing a reset time using a NAND gate in the PFD (Fig. 6.12). The reset time is set to be a fraction of the PFD operating frequency. In VCO-OTAs, however, this approach doesn't provide total shielding from finite transitions. The reason is that in VCO-OTAs the PFD is running at the VCO frequency (hundreds of MHz to GHz) as opposed to in a PLL, where the PFD runs at the reference frequency (hundreds of kHz to MHz).

In CSM, as shown in Fig. 6.9(a), the I_{up} and I_{dn} current sources are always ON, irrespective of input to the CP block. Thus, when required, the current is steered to the output. This results in comparatively faster current transition, which is desired from a linearity standpoint. However, in PSM as shown in Fig. 6.9(b) the current sources I_{up} and I_{dn} are switched off when the CP is not in use. For instance, when the switch S_{up} is turned on by the PFD, the current does not switch on instantaneously. First, the voltage at node P has to be brought down by at least one overdrive voltage for the current source to switch on completely. This results in a slower current transition in PSM compared to CSM, hence introducing more non-linearity.

Reduction in the PFD Power Consumption

In VCO-OTAs, the VCO operational frequency is much higher than the band of interest. Since the PFD operates at the VCO frequency, it accounts for a significant fraction of the total power consumption. The PFD power consumption is directly proportional to the capacitance it drives. In

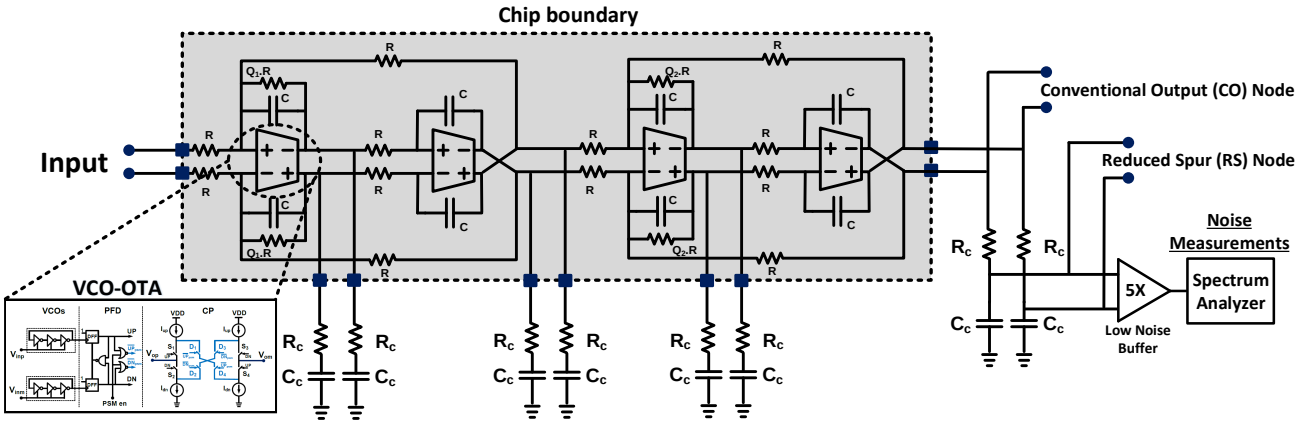


Figure 6.11: 4-MHz 4th order Butterworth low-pass filter implementation using proposed VCO-OTAs.

PSM, only switches S_{up} and S_{dn} need to be driven. In CSM (Fig. 6.9), however, the PFD needs to drive switches $\bar{S}_{up}$ and $\bar{S}_{dn}$ in addition to S_{up} and S_{dn}. This difference in the number of switches to be driven results in lower power for the PFD in PSM.

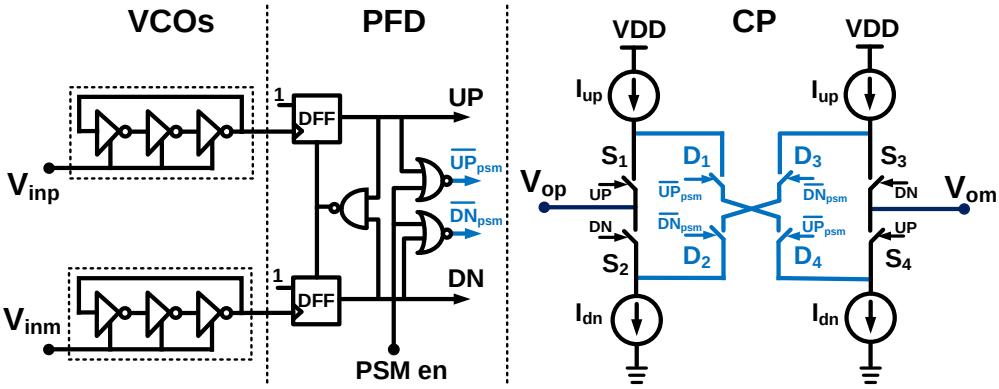


Figure 6.12: Circuit diagram of the VCO-OTA consisting of two VCOs, a PFD and a CP with PSM_en bit to switch between PSM and CSM

Spur Reduction Using Inherent Low-pass Filter Node

In VCO-OTAs, the mismatch between the Up and Down current sources results in a periodic, unwanted charge injection at the output node. This charge injection occurs in each VCO cycle, thus producing spurious tones at the VCO frequency.

A first-order filter can easily reduce out-of-band spurs for low-pass filters designed using VCO-OTAs. For a VCO-OTA, as discussed in section 6.2.2, R_c and C_c provide the compensation zero in the loop-gain transfer function. Additionally, this RC combination also acts as a low-pass filter from the conventional output (CO) node to the reduced spur (RS) node, as shown in Fig. 6.11. Therefore, if the output of the filter is taken from the RS node instead of the CO node, the spurious tones can be suppressed. The amount of suppression depends on the value of $1/(R_cC_c)$ with respect to the VCO frequency. Usually, the VCO frequency is much higher than $1/(R_cC_c)$, thus providing good suppression.

Type-II PLLs have used the R_c, C_c compensation technique for a long time. However, the filtering technique mentioned above is not used in PLLs because the required output of any PLL is the VCO output and not the CP output. Therefore using the RS node, in that case, alters the loop transfer function. In the case of VCO-OTAs, however, the desired output is the CP output. Therefore, taking output from the RS node does not affect the loop.

6.2.4 A 4-MHz 4th Order Butterworth Filter Implementation Using VCO-OTAs

To verify the proposed improvements, a 4-MHz 4th order Butterworth active-RC filter is implemented (Fig. 6.11). Each biquad section is realized using two VCO-OTAs, each consisting of two VCOs, a PFD and a CP as shown in Fig. 6.12. The differential inputs V_{inp} and V_{inm} drive two VCOs. The outputs of the VCOs are in turn given to a standard tristate PFD, which then controls the CP.

An additional gating mechanism at the output of the PFD is placed, as shown in Fig. 6.12 to compare the power reduction between CSM and PSM. Depending on the PSMen bit, the switches D1 to D4 are enabled or disabled, thus putting the CP in CSM or PSM respectively.

The circuit is designed to have a K_{vco} of 600MHz/V and charge pump current of 1mA. A compensation resistance R_c of 500Ω and C_c of 17pF is used to stabilize the system.

6.2.5 Measurement Results

The filter was fabricated in 180nm CMOS GP technology (Fig. 6.13) occupying an active area of 0.58mm^2. The total measured power consumption from 1.2V supply is 13.1mW in CSM and 9.4mW in PSM. The measured power break-down numbers for each VCO-OTA comparing CSM and PSM are shown in Fig. 6.13. The CP and the PFD power consumption are reduced by 41% and 25% respectively, from CSM to PSM, as expected.

The frequency response of the filter in CSM and PSM is shown in Fig. 6.14. The measured response closely matches the ideal filter response up to 20MHz and monotonically decreases af-

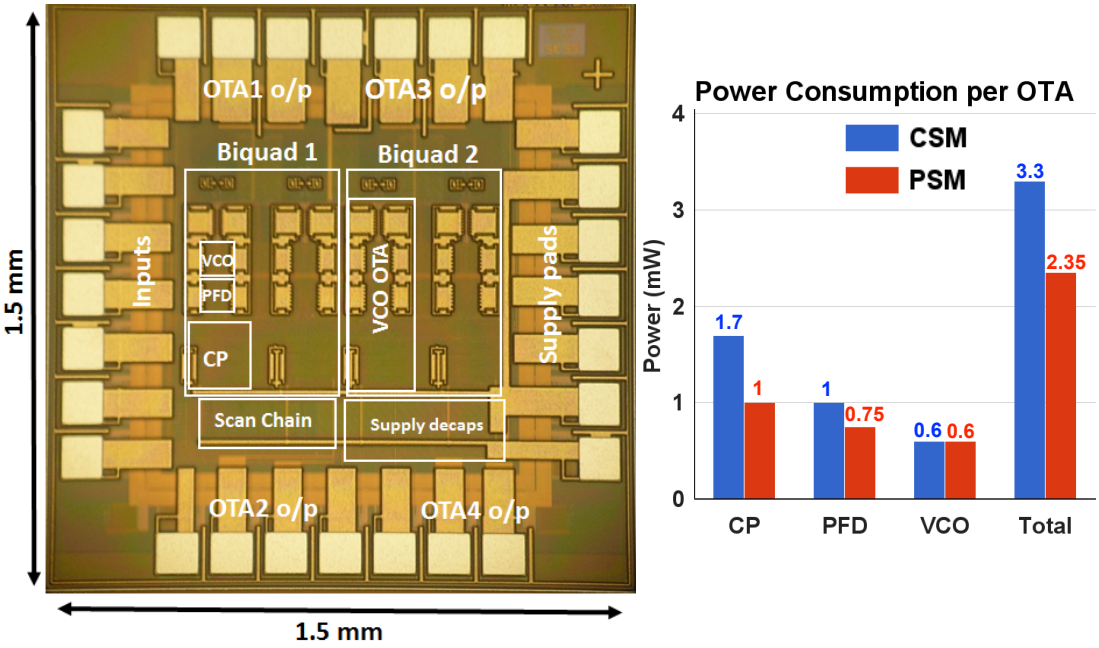


Figure 6.13: Die Photo (left) and Measured power break-down per OTA (right)

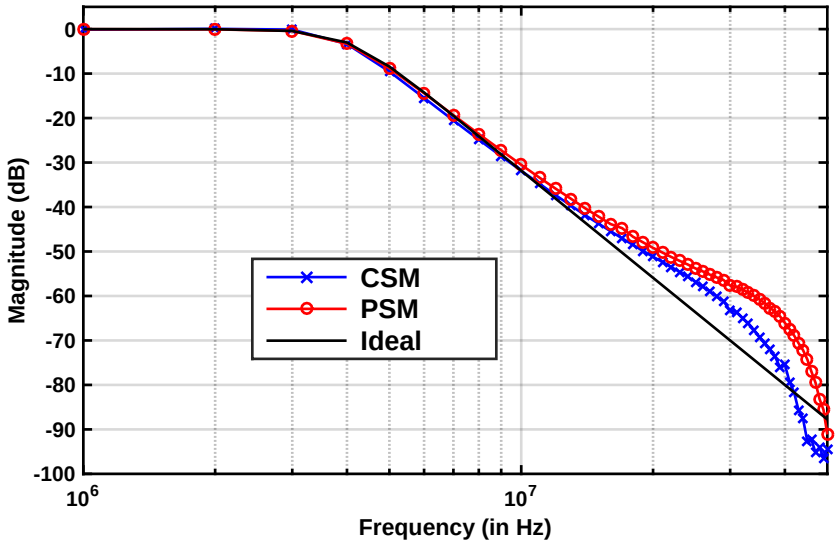


Figure 6.14: Measured filter frequency response for CSM and PSM

terward in both PSM and CSM. The in-band IIP3 measurements were performed using 0.95MHz and 1.05MHz tones. The IM3 products at 850kHz are shown in Fig. 6.15. As expected, a higher

IIP3 of 21dBm is achieved in CSM, as opposed to 19dBm in PSM. The out-of-band IIP3 measurements were done using two tones at 7MHz and 13MHz. The IM3 products at 1MHz are shown in Fig. 6.15. The achieved out-of-band IIP3 is 34dBm in CSM, whereas it is 36dBm in PSM.

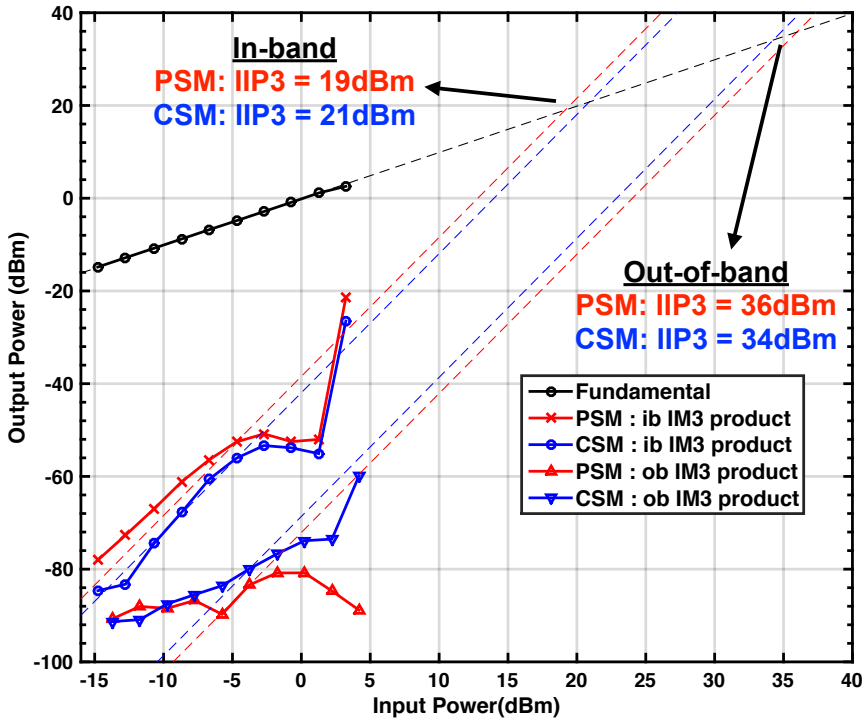


Figure 6.15: Measured IIP3 (in-band and out-of-band) results for CSM and PSM

The spectrum plot in Fig. 6.16 shows spurs at the VCO frequency for the CO node and the RS node. A reduction of 11.5dB is observed from the CO node to the RS node, as expected. The integrated output noise measured in CSM is $0.71\text{mV}_{\text{rms}}$ ($357\text{nV}/\sqrt{\text{Hz}}$ with 4MHz effective noise bandwidth) and PSM is $0.75\text{mV}_{\text{rms}}$ ($376\text{nV}/\sqrt{\text{Hz}}$ with 4MHz effective noise bandwidth).

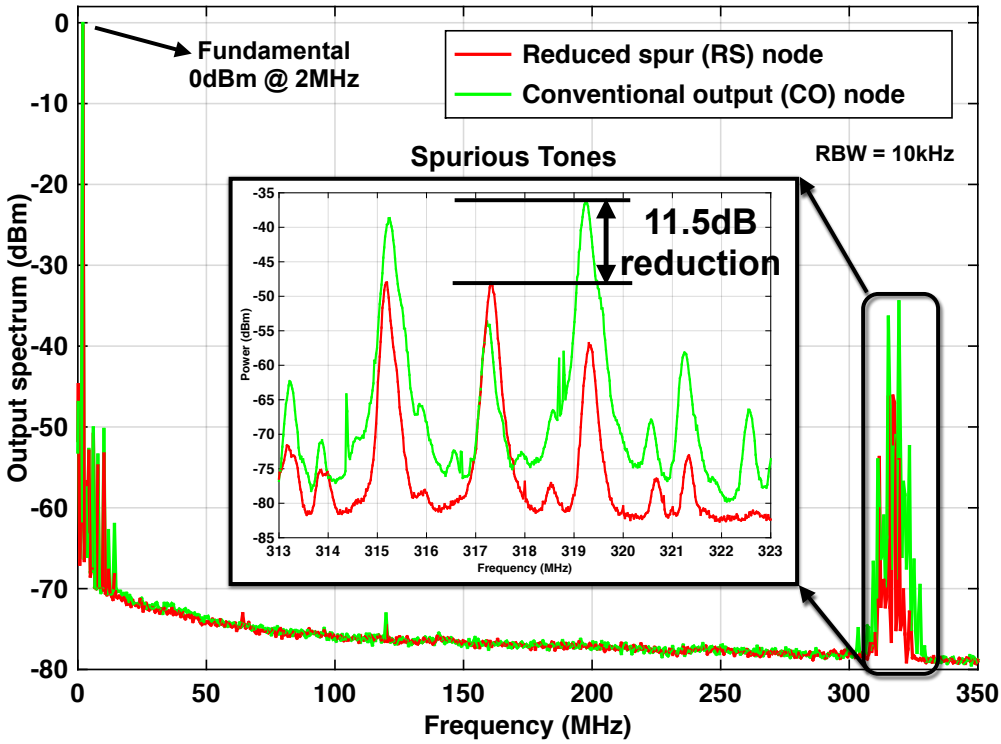


Figure 6.16: Spur reduction in VCO-OTA using RS Node in PSM

6.2.6 Section Summary

In this section, the power-linearity trade-off involved in the design of VCO based OTAs is explored. This is demonstrated by prototyping a 4-MHz 4th order active-RC Butterworth filter. A power reduction of 41% in the charge pump and 25% in the phase-frequency detector is achieved while trading off in-band IIP3 from 21dBm to 19dBm with minimal noise penalty. This trade-off methodology gives designers additional flexibility to choose CP topology, according to their power and linearity requirements. Additionally, the use of intrinsic low-pass filtering technique to reduce out-of-band spurs is demonstrated.

6.3 Design of VCO-OTAs at 0.2V[3]

6.3.1 Background

With the introduction of the Internet of Things (IoT), there has been an emphasis on scaling down supply voltage for low-power amplifier design. For example, strain gauge uses a Wheatstone bridge configuration for which power consumption is directly proportional to the supply voltage. Scaling down the supply voltage for both active and passive components reduces overall system power consumption.

In this section, we wish to scale down the supply voltage to the maximum extent for an analog voltage amplifier. In theory, a standard differential pair based two-stage amplifier requires stack-up of two or more transistors operating in the saturation region. The output voltage swing added with the minimum voltage required for keeping all the transistors in saturation determines the minimum achievable supply voltage. An additional challenge at voltages below 0.5V is to overcome the transistor threshold voltage, which does not decrease with technology scaling.

Several modifications to the standard differential amplifier have been provided in the literature to reduce supply voltage while maintaining rail to rail voltage swings. [94] uses a bulk driven differential amplifier with input dc shift to achieve operation at 0.6V. [95] uses a bulk driven differential pair amplifier, with additional feedforward network to increase the dc gain and the UGB of the amplifier at 0.5V. [96] uses dynamic threshold MOS transistor based differential pair to improve dc gain and bandwidth at 0.4V. [97] uses pseudo-differential, bulk-driven differential pair based amplifier to achieve operation at 0.35V. [98] uses a bulk-driven differential amplifier with positive

[3]This project was done in collaboration with Alessandro Bertolini and published in ISCAS [64]

feedback source-degeneration technique to achieve almost rail to rail operation at 0.25V. The minimum voltage required to maintain output transistors in the saturation region limits reducing the supply voltage further.

[6] introduces time-domain processing based switched-mode operational amplifier at 0.6V. Representing output in the form of pulse width modulation (PWM) helps in achieving rail-to-rail swing. The first stage consists of a telescopic amplifier with low output voltage swing, followed by conversion to pulse width modulation (PWM) in the 2nd stage. The information content in PWM is in the time domain, thereby allowing rail-to-rail output swing. However, similar to previous cases, the allowable reduction by the first stage telescopic amplifier limits the minimum supply voltage.

VCO-based operational transconductance amplifier (VCO-OTA) proposed in [59] is an alternate architecture to the differential pair based amplifier discussed earlier. Theoretically, it is possible to scale the supply voltage in this case because the VCO-OTA processes information in the time domain. However, in [59] the supply-voltage scaling is limited by the minimum voltage required for keeping the current sources of the current mirror transistors of the charge pump in saturation.

In this section, we propose a 0.2V VCO-OTA design where supply voltage reduction was made feasible by the elimination of the current sources. The section discusses other modifications required to scale down the supply voltage to 0.2V. Simulations show that in unity gain configuration, the proposed architecture achieves 60kHz unity-gain bandwidth (UGB) and 207μV_{RMS} input-referred noise while consuming 492nW.

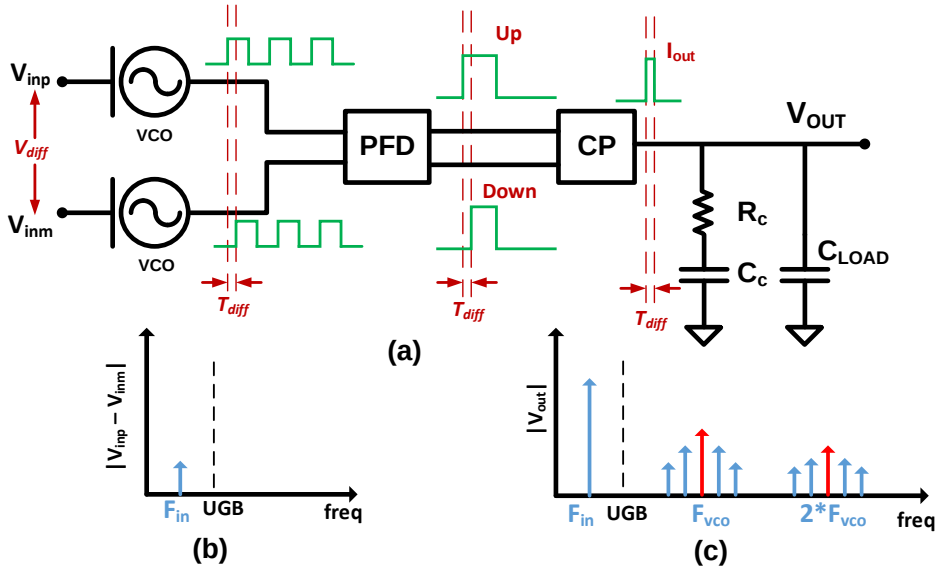


Figure 6.17: (a) The concept of the VCO-OTA in time domain (b) Typical input spectrum plot and (c) Typical output spectrum plot with spurs around multiples of VCO center frequency.

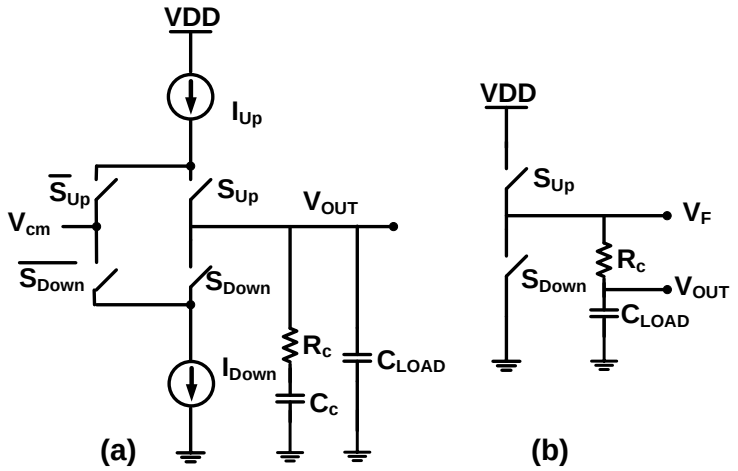


Figure 6.18: Schematic of (a) a standard CP and a second order output filter (b) the proposed CP with current sources eliminated and the modified filter for 0.2V VCO-OTA; the CP is driven from a modified PFD

6.3.2 Working of the VCO-OTA

The working of the VCO-OTA has been discussed earlier in this thesis, but we paraphrase it again in this section to provide a context for low supply voltage operation of the VCO-OTAs. Fig. 6.17(a) shows the block diagram of the VCO-OTA used in [59] with the time domain voltage waveforms at different circuit nodes. The VCO-OTA consists of two voltage-controlled oscillators (VCOs), a phase-frequency detector (PFD) and a charge pump (CP). In the time domain, the input voltages V_{inp} and V_{inm} are converted into frequencies by the VCOs with frequency difference proportional to the input voltage difference. The time difference T_{diff} between the zero crossings of the two frequencies produces Up and Down pulses at the output of the PFD. The CP then converts the difference between the Up and the Down pulses into a current pulse of the same duration T_{diff}. The output impedance, consisting of a compensation resistor and capacitor R_C and C_C and a load capacitor C_{LOAD} then converts this output pulse into V_{out}. The integration operation implemented by the PFD provides amplification in the time domain when it compares the phases of the frequencies produced by the VCO.

For a small differential input signal at a frequency F_{in}, the input spectrum of the VCO-OTA is shown in Fig. 6.17(b). In an open-loop case, the output V_{OUT} spectrum contains an amplified version of differential input and modulated signal around multiples of VCO center frequency as shown in Fig. 6.17(c). This is because of the spur injection by the CP during every VCO frequency cycle. This produces ripple at the output voltage and needs to be filtered. As discussed in [59], since the VCO center frequency is much higher than the input frequency and the UGB of the amplifier, therefore these ripples can be filtered by a first-order filter.

6.3.3 0.2V VCO-OTA Design

The block diagram of the proposed 0.2V VCO-OTA is same as shown in Fig. 6.17. However, the individual blocks are modified to enable amplifier operation at 0.2V.

Elimination of CP current sources

A standard CP is used in [59] consisting of a PMOS and an NMOS current source with on-off switches as shown in Fig. 6.18(a). These current sources need to be present in saturation region, thus limiting the minimum supply voltage possible for the CP. To scale down supply voltage to 0.2V, the current sources of the CP are eliminated, as shown in Fig. 6.18. The CP thus consists of Up and Down switches only. However this means that the current at the output is not controlled. This affects the stability of the system and its effect can be understood from the input to output transfer function. Based on the phase-domain model introduced in [59] the input to output transfer function for a single ended VCO-OTA output can be given as (refer Fig. 6.17):

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{2\pi K_{VCO} K_{PD} K_{CP}(1+\frac{s}{\omega_z})}{s^2 C_c(1+\frac{s}{\omega_{p_3}})} \tag{6.6}$$

where $\omega_z = 1/R_C C_C$, $\omega_{p_3} = 1/R_C C_{LOAD}$, K_{VCO} is the VCO gain, $K_{PD} = 1/2\pi$ is the phase detector gain and K_{CP} is the charge pump gain. It was shown that K_{CP} turns out to be the same as the CP current I_{CP}.

I_{CP} is no longer defined once the current sources are eliminated. However, it is possible to define the maximum possible current based on the supply voltage and the switch resistance. The zero is

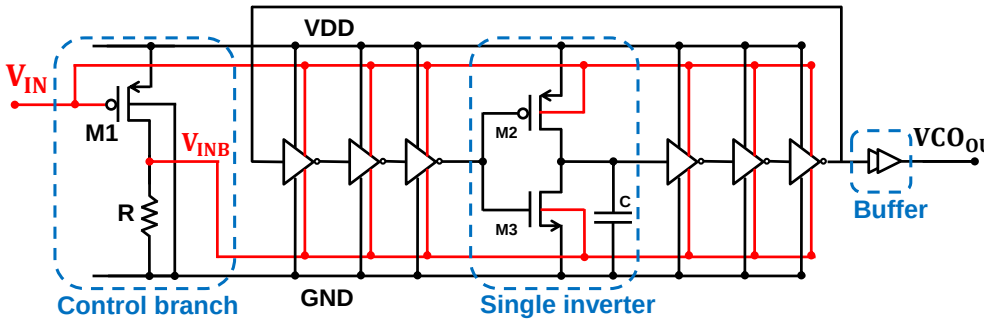


Figure 6.19: Schematic of the seven stage inverter based 0.2V VCO with control branch and output buffer

placed conservatively to ensure stability at all operating points once the maximum current I_{CP} is known.

Eliminating the current sources increases the possibility of shoot-through current in the output switches, when both Up and Down signals are on at the same time. The modified PFD ensures that Up and Down pulses do not overlap, eliminating the possibility of the shoot-through current, as explained in Section 6.3.3.

Compensation Capacitor replaced by Load Capacitor

Stability requirements for a VCO-OTA require the presence of a filter at the output of the CP. In [59], a standard second-order filter as shown in Fig. 6.18(a) is used. The compensation capacitor C_C required for the stability is much larger than the load capacitor C_{LOAD}. However, as proposed in [60] and shown in Fig. 6.18(b), it is possible to provide any feedback required from V_F node and take the final output from the first order filter output V_{OUT} node. This technique is used in the proposed 0.2V VCO-OTA to reduce the value of the compensation capacitor needed for stability and also use the load capacitor as part of the compensation capacitor.

0.2V VCO

In [59, 60], ring oscillators have been used for the VCO in the design of VCO-OTA. Fig. 6.19 shows the seven-stage ring oscillator used for the 0.2V VCO-OTA design. Since, ring oscillators are inherently scalable, reducing power supply to 0.2V is theoretically not difficult. However, to achieve maximum swing at the VCO internal nodes, the frequency tuning mechanism was chosen to be through transistor bulk terminal instead of the standard current starving approach. Inside an inverter the bulk of both the PMOS and the NMOS are driven from the control branch. To achieve maximum gain K_{VCO} from input voltage to output frequency the bulk voltages of the PMOS and the NMOS transistors need to be driven in opposite directions. The control branch provides V_{IN} and V_{INB}, such that when the control voltage V_{IN} of the PMOS increases, the corresponding control voltage V_{INB} of the NMOS decreases.

For the proposed OTA, the PFD limits the maximum oscillation frequency of the circuit, which will be explained in Section 6.3.3. Therefore, to limit the maximum frequency of the VCO, a small capacitor is used in each stage.

An inverter-based buffer is used at the output of the ring oscillator to prevent loading by the next stage. The buffer transistor sizes are adjusted so as to restore the VCO output duty cycle close to 50 percent.

0.2V Modified PFD

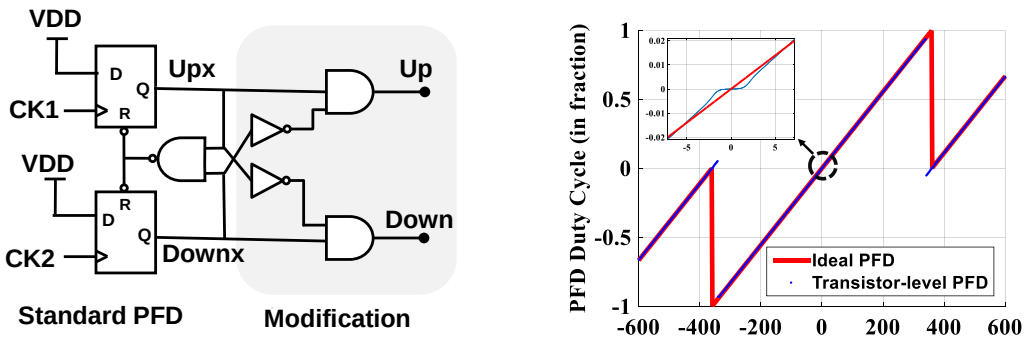
In the VCO-OTA, the PFD is a digital block, hence scaling down supply voltage is simple. However, a modified version of the standard PFD is used which does not have any overlap between Up

and Down pulses. This modification is necessary to avoid the shoot-through current of the CP (see Section 6.3.3). The block-level diagram of the modified PFD is shown in Fig. 6.20(a). It consists of two flip flops generating Upx and Downx pulses and a NAND gate to reset the flip flops when both Upx and Downx pulses are high.

The final outputs of the PFD, Up and Down are derived by the output of AND gates, with inputs Upx, DownxB and UpxB, Downx, where UpxB and DownxB are the inverse of Upx and Downx respectively. Using these gates ensures non-overlap of Up and Down outputs.

However, this non-overlap introduces a dead zone in the PFD output characteristic. Fig. 6.20 (b) shows the fraction of the duty cycle for which Up-Down pulse is on with respect to the input phase difference. The output is expected to be 1 and -1 when the phase difference is +360° and -360° respectively. The transistor-level PFD characteristic follows the ideal PFD characteristic for the rest of the plot, except around the origin. The zoomed-in version in the inset shows the presence of a dead zone around the origin. This dead zone results in the non-linearity in the proposed VCO-OTA. This is because, for small input phase differences to the PFD, the loop gain is not high enough, resulting in low suppression of any harmonics produced at the output.

Another constraint placed by the 0.2V PFD is that it limits the maximum possible frequency of the circuit. The delay of the NAND gate used for resetting the Upx and the Downx nodes is expected to be much less than the average period of the input frequency, which is set by the VCO center frequency. At 0.2V, the NAND gate delay is high, therefore limiting the maximum allowed VCO center frequency.



(a) (b)

Figure 6.20: Modified PFD (a) Schematic (b) Plot of output duty cycle fraction with input phase difference

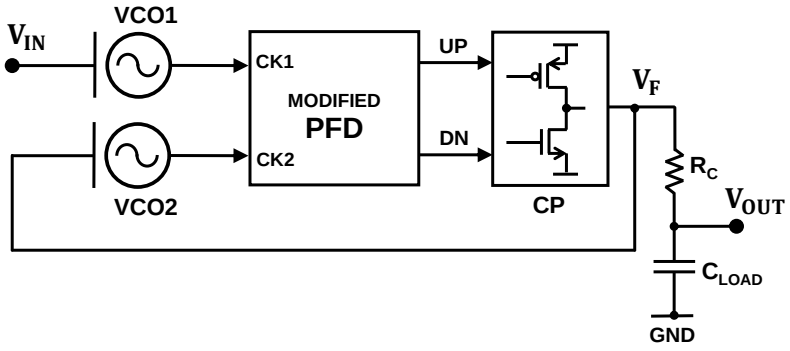


Figure 6.21: Schematic of the proposed 0.2V VCO-OTA in unity gain configuration

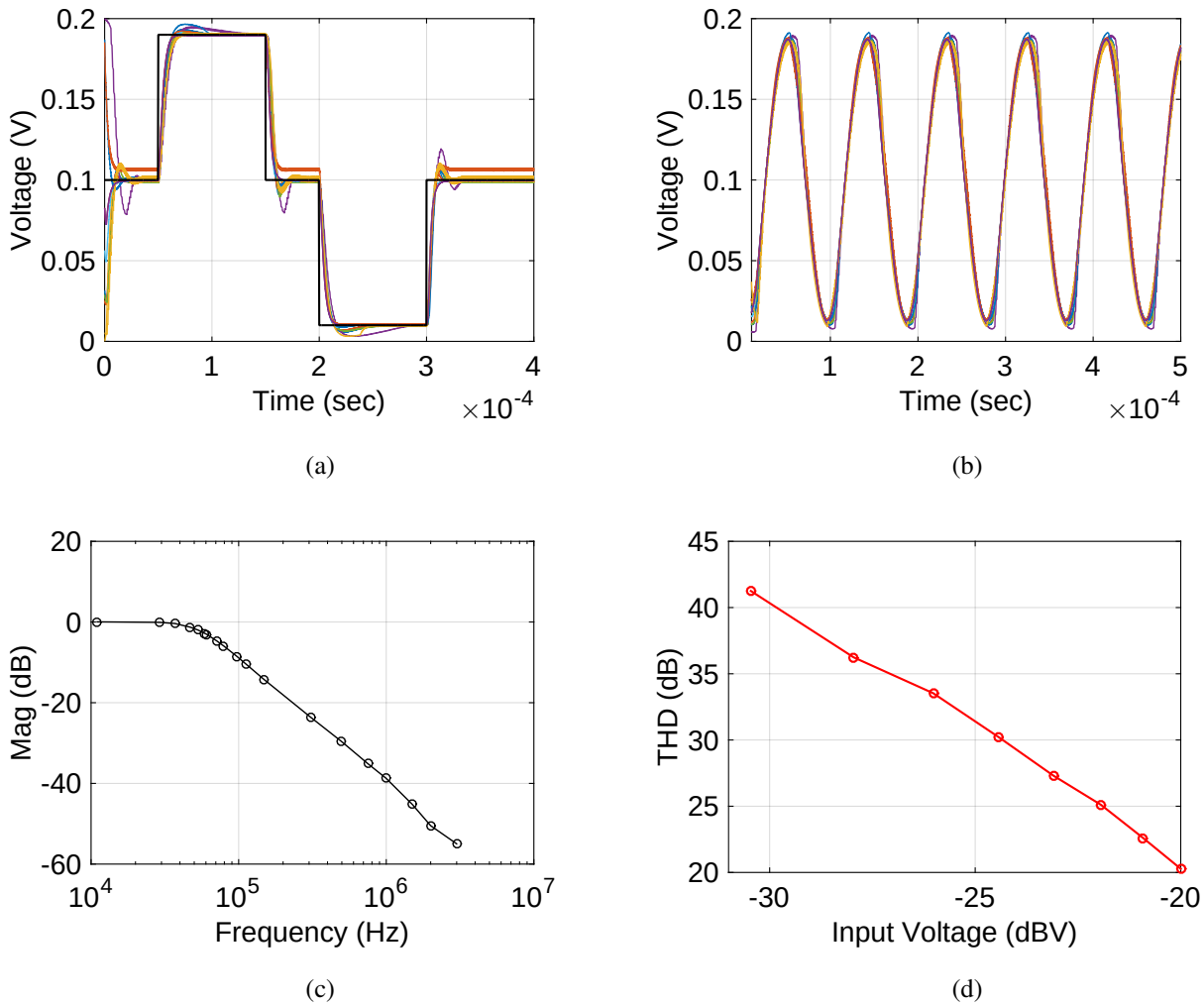


Figure 6.22: Simulation results for 0.2V VCO-OTA (a) Step Response over PT variation showing stability (b) Sine wave response for an input of 11kHz frequency with 90mV input amplitude and 100mV common mode (c) Frequency response of obtained by transient simulation for each frequency and plotting the fundamental component of input frequency (d) Total Harmonic distortion for 11kHz sine wave input with amplitude variation

6.3.4 Simulation Results

The unity gain configuration (Fig. 6.21) was used to evaluate the proposed 0.2V VCO-OTA in TSMC 65nm technology using low threshold voltage transistors. The feedback was taken from the CP output node V_F and the final output was taken at the filtered output node V_{OUT}. The sizing

of the transistors and the VCO load capacitors was done for the ss corner to ensure functionality across corners. For the ss corner at 27°C, the VCO center frequency used was 1MHz, limited by the maximum operating frequency of the PFD at 0.2V. The K_{VCO} was adjusted to 1.6MHz/V to obtain maximum voltage to frequency gain while covering rail to rail swings as well. The compensation resistance R_C and the load capacitance C_{LOAD} were chosen to be 200kΩ and 15pF.

Fig. 6.22(a) denotes the step response for an input step of 90mV above and below the common-mode voltage V_{CM} of 100mV over the process and temperature variation. Five process corners, namely tt, ff, ss, fs, and sf were simulated for 15°C and 50°C. The simulation shows that the system is stable across all process corners.

Fig. 6.22(b) shows the sine wave response over the process and temperature variation for the input of 11kHz and amplitude of 90mV over V_{CM} of 100mV. Thanks to the RC filter following the output of the CP, the ripples at VCO oscillation frequency are attenuated. Higher distortion is visible in the output for two corner cases: ss at 15°C and sf at 50°C.

Fig. 6.22(c) shows the frequency response of the circuit for tt corner at 27°C. The frequency response was obtained by taking an FFT of a sine wave input at different frequencies and measuring the magnitude of the fundamental tone. This is because a VCO-based system does not have a fixed DC operating point, hence small-signal AC simulation is not possible in Cadence. An input amplitude of 50mV was used in the simulation. The UGB of the circuit was found to be 60kHz. The intermodulation of the VCO center frequency and the input frequency produces a tone higher than the fundamental tone for input frequencies close to the VCO center frequency. Still, all the intermodulation tones were below -60dBV in simulations.

Fig. 6.22(d) shows the total harmonic distortion for the circuit with increasing input amplitude for tt corner at 27°C. An input frequency of 11kHz was used, and a total harmonic distortion of 10% was observed at rail-to-rail input. The dead zone present in the PFD is the main reason for distortion.

Fig. 6.23 shows the output spectrum and its zoomed in version for the two cases for an input frequency of 11kHz and input amplitude of 50mV.

Similar to AC analysis, noise analysis is not possible in case of VCO-OTAs. Therefore, the noise was simulated by running a transient simulation with transient noise enabled with a maximum noise frequency F_{MAX} set to 100MHz, which is much higher than oscillation frequency of the VCO. A noise scaling factor option of 10x was chosen to ensure that noise can be distinguished from numerical errors, without affecting the operating point of the VCO-OTA. The FFT of the output was then taken, and the SNR was calculated. Knowing the signal RMS voltage in advance, the RMS noise voltage was calculated from the SNR. Since the VCO-OTA is in unity gain configuration, the calculated output noise thus obtained is same as input-referred noise.

Fig. 6.24 shows the UGB, power consumption and noise values across process and temperature. The UGB of the VCO-OTA is primarily determined by the R_F and C_{LOAD}. Therefore there is not much variation in UGB, despite a large change in K_{VCO}. However, the power consumption varies noticeably with the process and temperature variation. We expect this variation because the VCO-OTA consists of inverters and switches with current consumption dependent on threshold voltage, which varies with process and temperature.

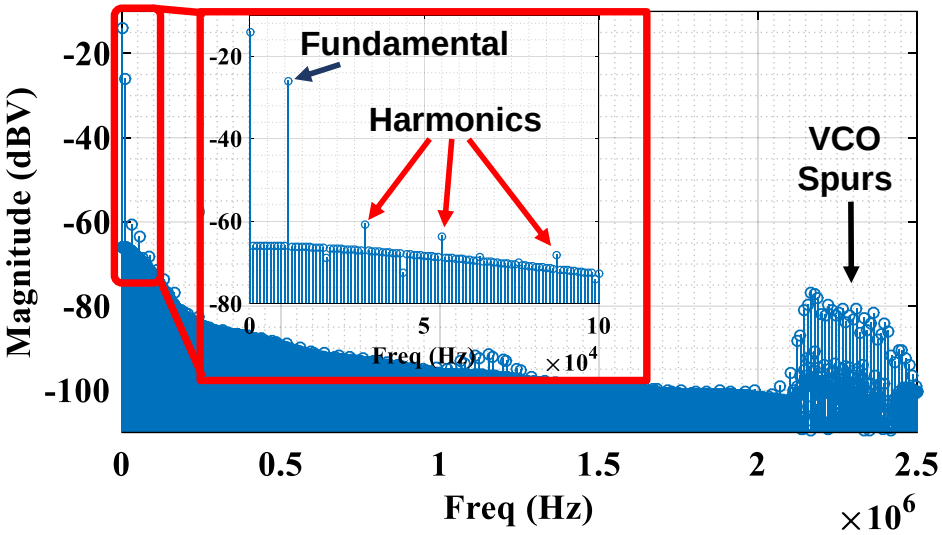


Figure 6.23: Output spectrum for VCO-OTA for a sine wave input of 100mV$_{PP}$ at 11kHz

We propose a figure of merit (FOM) to normalize for UGB, capacitive load, power consumption and input-referred noise power per unit bandwidth, and compare it to state of the art in Fig. 6.25.

6.3.5 Section Summary

In this section, we present a 0.2V VCO-based OTA processing information in the time domain. Supply voltage scaling down to 0.2V was achieved by eliminating current sources present in the CP and using a modified PFD. The proposed architecture achieves 60kHz UGB and 207μV$_{RMS}$ noise while consuming 492nW power for the typical case in simulation.

Corner	Temperature	UGB	Power Consumption	Noise (uVrms)	FOM
tt	**15**	56kHz	367nW	258	192
tt	**27**	60kHz	505nW	207	256
tt	**50**	64kHz	844nW	150	325
ss	**15**	46kHz	139nW	174	754
ss	**50**	57kHz	342nW	259	216
ff	**15**	61kHz	942nW	154	249
ff	**50**	55kHz	2010nW	121	157
sf	**15**	54kHz	438nW	158	412
sf	**50**	48kHz	915nW	112	301
fs	**15**	55kHz	387nW	205	280
fs	**50**	56kHz	946nW	167	177

Figure 6.24: UGB, noise and power numbers for proposed design over process and temperature variation and comparison to references

	This work*			[5]	[4]	[3]*	[2]*	[1]
Conference/Year	ISCAS '17			TCAS-I '14	TCAS-I '15	MWSCAS '12	ICM '08	TCAS-II '07
Corner	Typical (tt 27)	Best (ss 15)	Worst (ff 50)					
Supply Voltage (V)	**0.2**			**0.25**	**0.35**	**0.4**	**0.5**	**0.6**
Technology	65nm			130nm	65nm	180nm	180nm	350nm
Unity gain bandwidth (kHz)	60	46	55	1.88	3600	111.4	83.9	11.4
Slew rate (V/ms)	10.5	8	11.5	0.64	5600	22	52	14.6
Input referred noise (μV_{RMS})	207	174	121	143	1756	/	/	31
Capacitive Load (pF)	15			15	3	15	15	15
Power Consumption (nW)	492	139	1973	18	1700	386	1020	550
FOM (Higher is better)	**256**	**754**	**157**	**14**	**742**	/	/	**370**

* Simulation results

$$\text{Figure of Merit (FOM)} = 100 * \frac{f_{UGB} \cdot C_{LOAD}}{Power} \cdot \frac{f_{UGB}}{(\mu V_{NoiseRMS})^2}$$

Figure 6.25: Comparison to the state of the art

Chapter 7

Conclusions and Future Work

7.1 Conclusions

The goal of this thesis was to present voltage and time-domain techniques to overcome the challenges in analog circuit design presented by technology scaling.

In Chapter 1, we presented the pros and cons of technology scaling, and the need to improve the existing voltage-domain circuit architectures to overcome the challenges of reduced SNR and to break through the power wall at reduced supply voltage.

In Chapter 2, an on-the-fly gain selection technique in voltage-domain was proposed to increase the input dynamic range of a data converter. This design eliminates the need to have a highly accurate low-noise reference buffer, thus reducing the overhead of additional power consumption that comes with the design traditionally.

In Chapter 3, we introduced time-domain circuits which have emerged as an attractive scaling friendly alternative to voltage-domain circuits in recent literature. After providing an overview of classification criterion, we presented a few examples of time-domain circuits, laying the foundations for VCO-OTAs, which has been the area of focus for the rest of this thesis. Some practical design challenges for time-domain circuits were also discussed towards the end.

In Chapter 4, a discrete-time linear model of VCO-OTAs based on zero-crossings of the two

VCOs used in the system was presented. Unlike the phase-domain model that makes simplifying assumptions by placing restrictions on the input frequency and VCO frequency, the presented model captures the entire system dynamics.

In Chapter 5, we discussed the benefits of using VCO-OTAs as baseband trans-impedance amplifiers in current-mode receivers. A 20MHz RF-bandwidth 2GHz receiver was presented as a design example. Simulation results indicated up to 12dB improvement in blocker tolerance for slightly higher power consumption, or up to 2x power reduction of the receiver for a similar performance when compared to the receiver using the alternative scaling-friendly inverter-based amplifiers.

In Chapter 6, another application of VCO-OTAs in a low-dropout regulator (LDO) was showcased. Compared to the traditional voltage-domain LDO measured on the same chip, VCO-based LDO was able to go down to 100mV dropoff voltage and operate at 0.8V supply, as opposed to 150mV dropoff voltage, and 1.2V supply for the other one, thanks to the infinite DC loop gain achievable in the VCO-based design. Another prototype demonstrating the power-linearity trade-off in VCO-OTAs was discussed in a 4th order Butterworth filter application. A 0.2V VCO-OTA design placed in a unity-gain configuration was presented in the end.

7.2 Future Work

7.2.1 Dynamic Range Enhancer

In the current architecture, the dynamic range of DRE followed by SAR structure is primarily limited by the backend SAR used. It is possible to improve the input dynamic range and hence figure of merit by 3-4dB at no extra power penalty for DRE by reducing the quantization and thermal noise in the backend SAR architecture. Additionally, the backend SAR used in this topology consumes more power than state-of-the-art examples because of radiation hardness requirements. It is possible to reduce power and improve the figure of merit for the combined system by scaling down the capacitor sizes, and the triple redundancy used to drastically reduce the power consumption of the SAR for applications not having radiation hardness requirement.

7.2.2 VCO-OTA Modeling and Simulations

In Chapter 4, we have introduced a zero-crossing based model supported by behavioral level simulations. The next step is to design a controllable prototype using this methodology and demonstrate that the phase-margin degradation predicted theoretically matches the measurement value. The prototype can also provide more insight into issues such as the impact of injection locking and empirical limits of the small-signal model used in the system.

Simulating VCO-OTAs using DC/AC/PSS/PAC analysis is also a challenging problem due to the presence of two independent oscillators in the system. However, it is possible to create a steady-state periodic response for the system by using a periodic reset. This technique provides

the benefits of using PSS/PAC simulations such as noise summary and frequency response of the system. If it is possible to resolve the convergence issues and possibly utilize harmonic balance or quasi-periodic steady-state simulation tools for VCO-OTAs, then the barrier of long simulation time that prohibits the use of VCO-OTA based circuits can be drastically reduced.

7.2.3 VCO-based TIA for Receivers

In Chapter 5, we have introduced the benefits of VCO-OTAs as TIAs in current-mode receivers. The next step is to demonstrate the application using a prototype optimized to benefit from the high DC gain of the OTA. If an active-zero-compensation scheme is used, then it is possible to reduce the area of the baseband TIAs along with performance improvement of the receivers.

Another possible extension is to directly convert the PWM signal produced at the output of the PFD node to digital using VCO-based quantizers. This approach has the potential to integrate the data converter with the TIA and provide further power and area savings.

7.2.4 VCO-OTA Improvements in Other Existing Applications

In Chapter 6, we discussed the application of VCO-OTAs in an LDO. One of the drawbacks of the prototype was the large area used by the compensation capacitor. The area can be drastically reduced by implementing an active-zero-compensation. Additionally, the transient time response can be improved by implementing a PID controller approach instead of just having proportional and an integral path in the closed-loop system.

Similarly, a 0.2V application of VCO-OTA was proposed but had the challenge of significant

power variations across PVT. Using a current-controlled VCO architecture can provide better control over the power consumption at the cost of reducing K_{VCO}. It is possible however, to leverage multi-phase architecture to achieve higher bandwidth at reduced supply voltages.

7.3 Concluding Remarks

Technology scaling has led to amazing advancements in the electronics industry in the past few decades. While analog circuits have faced some challenges, it is becoming increasingly possible to benefit from this trend. This thesis is an attempt to address some of the challenges in two orthogonal dimensions: voltage-domain and time-domain.

For voltage-domain circuits, this thesis presents an example of a data converter, where application-specific requirements are used to achieve power savings compared to traditional architecture. We believe it is possible to use a similar approach for several applications to achieve performance improvement.

Additionally, time-domain circuits (TDCs) have emerged as promising scaling-friendly alternatives to voltage-domain circuits. However, they have several practical challenges in modeling, simulating, and understanding their architectures and applications. This thesis briefly explores the modeling and application of one particular type of TDCs, namely VCO-OTAs. We believe that TDCs have started challenging the traditional architectures and will continue to become their strong contenders.

The exciting thing is that these approaches have opened a whole new level of research opportunities for analog circuit designers for years to come!

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Appendix

Power Estimates for INV-TIAs and VCO-TIAs

For receiver simulations in Section 5.7.1, the total power consumption for the inv-TIAs is calculated based on the noise requirements for the OTA given in Fig. 5.7(b), assuming $\gamma = 1$ and $g_m/I_d = 10$. For Rx2, each single-ended branch of the pseudo-differential inv-OTA requires a transconductance, g_m, of 4mS, resulting in total power consumption of 1.92mW for two pseudo-differential OTAs operating at 1.2V supply in the I-Q branches. For Rx3, a higher g_m of 16mS is required to achieve the same NF, resulting in total power consumption of 7.8mW for the OTAs.

For VCO-TIA used in Rx1, power consumption is contributed by the VCO, the PFD, and the CP. Based on the design methodology described in Section 5.6, the parameters required for the VCO-OTA are f_{VCO} = 2GHz, K_{VCO} = 4GHz/V and I_{CP} = 0.35mA per single-sided branch of the VCO-OTA. The VCOs dominate the noise requirements [58] and require 0.96mW per differential VCO-OTA based on simulations. For a conservative total capacitance of 50fF in the PFD, its power consumption at f_{VCO} = 2GHz and 1.2V supply voltage is 0.15mW. Based on [60], assuming the CP to be on for 40% time, two CPs in a differential implementation of the VCO-OTA consume 0.34mW. The total TIA power estimate for the two VCO-OTAs for I-Q branches is thus 2.92mW.