

Wafer-level Packaging of Photonics and Electronics for Terabit-scale Optical Interconnects

Paraskevas Bakopoulos¹, Peter Ossieur², António José Trindade³,
Patrick Steglich^{4,5}, Igor Krestnikov⁷, Francesco Floris⁸, Gunther Roelkens²,
Mesut Inac⁴, Dimitrios Kalavrouziotis¹, David Gomez⁹, Lars Zimmermann^{4,6},
Joris Van Campenhout², and Elad Mentovich¹

¹Mellanox Technologies Ltd., Hakidma 26, Yokneam 2069200, Israel

²IMEC and Ghent University, Ghent and Leuven, Belgium

³X-Celeprint, Ltd., Israel

⁴IHP — Leibniz-Institut für innovative Mikroelektronik

In Technologiepark 25, Frankfurt(Oder) 15236, Germany

⁵Technische Hochschule Wildau, Hochschulring 1, Wildau 15745, Germany

⁶Technische Universität Berlin, Einsteinufer 25, Berlin 10587, Germany

⁷Innolume GmbH, Dortmund, Germany

⁸Tyndall National Institute, University College Cork, Dyke Parade, Cork., Ireland

⁹X-Celeprint, Inc., Israel

Abstract— Soaring data traffic requirements in datacenters are posing inordinate challenges to the optical interconnect Assemblies with an aggregate bandwidth capacity of 800 Gb/s and 1.6 Tb/s are envisioned in near-future deployments of particular use cases in intra-datacenter connectivity. On top of the vast bandwidth requirements, extensive thermal and reliability qualifications along with aggressive pricing targets are further raising the bar for future-proof technologies. In parallel to advances in chip design and manufacturing, development of viable packaging and integration approaches is of paramount importance for meeting end-user roadmaps. We highlight prominent use cases and review current and future challenges coming from the application perspective to assess how they translate into packaging requirements.

We present the approach of CALADAN European project. CALADAN aims to reduce the large number of sequential steps currently required for manufacturing an optical transceiver, eliminating manufacturing bottlenecks caused by piece-by-piece assembly of lasers and electronic chips onto the PIC. To address these shortcomings CALADAN is developing processes for wafer-level integration of lasers and electronics onto a PIC using the established micro transfer printing approach. GaAs quantum dot lasers are targeted owing to their increased efficiency at high operating temperatures. On the electronic side, 56 Gbaud capable driver and receiver chips are developed in a proven 130 nm SiGe BiCMOS process. The lasers and electronics will be transfer printed onto silicon photonic 300 mm wafers fabricated in a commercial process. For fiber attachment, a novel fast process is under development aiming to reduce the time required by an order of magnitude.

- 10:20 Non-invasive Optical Sensing Method Based on Random Lasing
Federico Tommasi (Università di Firenze); Lorenzo Fini (Università di Firenze); Emilio Ignesti (Università di Firenze); Fabrizio Martelli (Università di Firenze); Stefano Cavalieri (Università di Firenze);
- 10:40 A Universally Programmable Terahertz Chip-scale Sensor in Silicon with Direct Digital Reconfiguration of Scattering Interface
Kaushik Sengupta (Princeton University);
- 11:00 **Coffee Break**
- 11:30 Polymer Resonators for Thermodynamics Fatty Acids Phase Transition Detection
L. Garnier (Université de Rennes 1); R. Castro-Beltran (Université de Rennes 1); A. St-Jalmes (Université de Rennes 1); H. Lhermite (Université de Rennes 1); E. Gicquel (Université de Rennes 1); H. Cormerais (Université de Rennes 1); A.-L. Fameau (Biopolymères Interactions Assemblages); A. Ghoufi (Université de Rennes 1); Bruno Beche (Université de Rennes 1);
- 11:50 Multi-beam Processing Technology for High Resolution LiDAR Sensor
Jungwoo Kim (Samsung Advanced Institute of Technology); Tatsuhiko Otsuka (Samsung Advanced Institute of Technology); Yongchul Cho (Samsung Advanced Institute of Technology); Kyoung-Ho Ha (Samsung Advanced Institute of Technology);
- 12:10 Deployable Sensor for Trace Identification of Hazardous Chemicals in Dirty Environment, Based on FAST Gas-chromatography and Quartz Enhanced Photoacoustic Spectroscopy
R. Viola (Consorzio CREO); Sandro Mengali (Consorzio CREO); N. Liberatore (Consorzio CREO); S. Zampolli (CNR-IMM Bologna); I. Elmi (CNR-IMM Bologna); F. Mancarella (CNR-IMM Bologna);
- 12:30 Relationship between Human Glucose Level and Optical De/Polarization Information in 600 nm–800 nm Wavelength Region
Ercan Menguc (Akdeniz University); Selcuk Helhel (Akdeniz University);
- 12:50 Investigation of Tunnel Field Effect Transistor for Biosensing Applications
Manjula Vijn (Amity University Uttar Pradesh); R. S. Gupta (Maharaja Agrasen Institute of Technology); Sujata Pandey (Amity University);

Session 1A8
Photonics Packaging & Integration 1

Monday AM, June 17, 2019
Room 6 - Mezzanine

Organized by Francesco Floris

 Chaired by Francesco Floris

- 09:00 PIXAPP and European Open Access Pilot Lines for Integrated Photonics
Padraic E. Morrissey (Tyndall National Institute);
- 09:20 Wafer-level Packaging of Photonics and Electronics for Terabit-scale Optical Interconnects
Paraskevas Bakopoulos (MellanoX Technologies Ltd.); Peter Ossieur (IMEC and Ghent University); Antonio Jose Trindade (X-Celeprint, Ltd.); Patrick Steglich (IHP — Leibniz-Institut für Innovative Mikroelektronik); Igor Krestnikov (Innolume GmbH); Francesco Floris (University College Cork); Gunther Roelkens (Ghent University, IMEC); Mesut Inac (IHP — Leibniz-Institut für Innovative Mikroelektronik); Dimitrios Kalavrouziotis (MellanoX Technologies Ltd.); David Gomez (X-Celeprint, Inc.); Lars Zimmermann (IHP); Joris Van Campenhout (IMEC); Elad Mentovich (MellanoX Technologies Ltd.);
- 09:40 Pluggable Freespace Connectors Enabling Consumable Photonics
Kamil Gradkowski (Tyndall National Institute); Carmelo Scarcella (CERN); Luca Zagaglia (Tyndall National Institute); Francesco Floris (University College Cork); Peter O'Brien (Tyndall National Institute);
- 10:00 Packaging Challenges in Field-programmable Photonic Arrays (FPPAs)
Prometheus Dasmahapatra (Universität Politècnica de València); Daniel Perez Lopez (Universität Politècnica de València); Jose Capmany (Universität Politècnica de València);