Programmable Photonics: An Opportunity for an Accessible Large-Volume PIC Ecosystem

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(Invited Paper)

***Abstract*—We look at the opportunities presented by the new concepts of generic programmable photonic integrated circuits (PIC) to deploy photonics on a larger scale. Programmable PICs consist of waveguide meshes of tunable couplers and phase shifters that can be reconfigured in software to define diverse functions and arbitrary connectivity between the input and output ports. Off-the-shelf programmable PICs can dramatically shorten the development time and deployment costs of new photonic products, as they bypass the design-fabrication cycle of a custom PIC. These chips, which actually consist of an entire technology stack of photonics, electronics packaging and software, can potentially be manufactured cheaper and in larger volumes than application-specific PICs. We look into the technology requirements of these generic programmable PICs and discuss the economy of scale. Finally, we make a qualitative analysis of the possible application spaces where generic programmable PICs can play an enabling role, especially to companies who do not have an in-depth background in PIC technology.**

***Index Terms*—Integrated Optics, Costs, Techno-Economic Analysis, Programmable Circuits**

I. Introduction

In the past decade, photonic integrated circuits (PIC) have found their way into a wide variety of applications, going from telecom/datacom transceivers to sensors and compact spectrometers. While there is a large variation of PIC material systems with different flavours, semiconductors have proven to be the most versatile [1], [2]. Especially Silicon photonics has grown into a versatile technology, because they can be manufactured with the same technology as that of CMOS electronics. The high index contrast of silicon photonic waveguides allows scaling to densely integrated and complex circuits, while the CMOS fabrication technology opens up a route towards cost-effective large-volume manufacturing [3], [4], [5], [6].

But today, this scaling of photonics is not yet happening. While the number of building blocks in photonic circuits is steadily growing, the circuits do not grow a lot in complexity, but rather consist of a larger repetition of simple circuits [7]. This can, to a large extent, be attributed to today's limitations in photonic circuit design [8]. While the design flow for analog electronics enables first-time-right design, the tools and practices that enable this for photonic circuit design are not yet established in the overall PIC community. A full-custom photonic circuit often needs several costly fabrication iterations before it performs its function within specifications, because the design tools and foundry design kits do not yet support good models and predictive variability modelling. While this is improving, it will take several more years before photonic designers can enjoy the same first-time-right experience of electronic circuit designers. This, in turn, will allow a scaling up of photonic circuit complexity and a dramatic growth in functionality.

The key benefit of the so-called 'CMOS compatibility' of silicon photonics is the possibility to fabricate the photonics chips in a CMOS fab, because the materials and processes are very similar to those of CMOS electronics. This does not mean that the photonic circuits and the electronic circuits should be fabricated together on the same chip. Monolithic co-integration has been demonstrated, but it usually results in a significant performance trade-off between the photonics and the electronics. Except for some specific functions and applications [9], [10], it is often beneficial to fabricate photonics and electronics in separate process flows.

A second comparison with the electronics industry puts the scaling of photonic circuits in perspective: while silicon photonics is technologically compatible with the infrastructure for CMOS manufacturing, there is a significant economic mismatch. The manufacturing volumes of even very successful silicon photonics products are orders of magnitude lower than the capacity of a CMOS fab, and even though potential new markets for PICs (e.g. sensors for the internet of things or health care) could deliver the necessary volume demand, the immature and uncertain development cycle for new photonic chips is proving to be a major obstacle to rapid adoption. Today, we only see sizable silicon photonics product volumes in the datacenter transceiver markets.

Today, virtually all PICs are application specific: they are designed to perform a single or a few functions, targeted to the needs of a specific application. As already mentioned, these application specific PICs (ASPIC) are costly and risky to develop, as it can take two or three design-fabrication-test cycles, each taking up to a year, to get the circuit working to specification. This slow development cycle is really detrimental for testing the viability, both technical and economic, of a new product and its market potential.

In the development of products based on electronics, this long cycle can be cut short in many situations. Off-the-shelf programmable electronics, in the form of microcontrollers, digital signal processors (DSP) or field-programmable gate arrays (FPGA) can be configured to perform a variety of functions [11]. They come with development kits that allow rapid prototyping of new functions that can be programmed

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in software within weeks rather than months. While these off-the-shelf solutions do not always provide cutting-edge performance, they allow for rapid development cycles to validate technical and market assumptions. If these prove to work out, and improved performance is needed, a design cycle for a dedicated application-specific IC (ASIC) can be considered.

This is where programmable photonic circuits make their entrance. Programmable PICs are photonic chips that can be configured in software to perform a variety of functions for different applications. While software-based manipulation of light has been established in techniques such as adaptive optics and the use of spatial light modulators [12], [13], the definition of a generic, multifunctional photonic circuit was only proposed in 1994 [14], in the form of a universal interference circuit that could implement any linear transformation between a set of input modes and a set of output modes using a triangular arrangement of tunable beam splitters and optical phase shifters. This circuit concept remained dormant until 2013, when more mature PIC technology, control electronics and especially new configuration algorithms turned it into a practical proposition [15]. Since then, different concepts for 'photonic processors' have been proposed to implement both broadband and wavelength-filtering linear transformations [16], [17], [18], [19], [20]. All these concepts make use of an on-chip network of tunable 2×2 couplers and optical phase shifters to distribute and interfere the light to obtain the correct linear combinations of inputs at the different outputs. When combined with active photonic components, such as high-speed modulators, (balanced) photodetectors, and optical amplifiers, a generic optical chip can be constructed that can generate, modulate, distribute and filter optical signals, but also microwave signals modulated onto an optical carrier [20].

It is important for the context of this paper to stress the difference between a truly programmable PIC and an ASPIC where the functionality can be tuned electrically. Electrically tunable and switchable photonic circuits are almost as old as photonic circuits themselves. A tunable ASPIC uses the tuners to optimize its functionality or adjust it to compensate for drift or changes in the environment. A programmable PIC, as we discuss it here, can be electrically reconfigured to perform a variety of functions, even targeted at entirely different applications. As we will discuss further, there is a continuum between tunable PICs and truly generic programmable PICs, but in the framework of the discussion in this paper, the key differentiator is the reconfigurability for multiple purposes.

There is always a trade-off between genericity, cost and performance. Again, electronics serves as an example. Generic programmable electronics (FPGAs, DSPs) are usually larger than optimized ASICs, and also consume significantly more power for performing the same operations. With a larger footprint also comes an added cost. However, in many cases this larger cost can be offset by the higher production volumes of these generic chips, spreading the non-recurrent engineering cost over many customers [11]. These considerations also apply to programmable photonics, even though we can expect the production volumes for most photonic applications to remain considerably lower than for electronics in the foreseeable future.

The generic programmability makes these chips also more flexible in use, and shortens the development time of a product, compared to the development based on an ASIC. This makes most sense for applications that require optical signal processing in commonly used wavelength bands, such as those used for telecom and datacom between 1250-1600 nm. Apart from flexible fiber-optic communications (e.g. fiber-to-the-X), these applications could include sensor readout systems (e.g. fiber Bragg gratings) or optical beamforming (free-space communication, LiDAR). An application where programmable photonic circuits could really make a difference is microwave photonics, where high-frequency radio signals are processed in the optical domain [21], [18]. This can be applied in diverse applications from radar systems to 5G wireless communications.

So we can ask the question: with this generic applicability, can programmable PICs perform the same function for the photonic ecosystem as programmable electronic circuits have done? In this paper, we look into some of the conditions that need to be fulfilled in order for this to happen, and which developments are needed in programmable PIC technology. In section II we describe briefly the basics of programmable photonic circuits, and to make sure that the technical needs are well understood. We discuss the entire technology stack in section III. Based on this, we map the technology needs onto engineering cost estimates in section IV, comparing programmable PICs with ASPICs of different complexity and cost. Finally, in section V we discuss how this can affect various application fields.

II. From ASPICs to Programmable Photonic Chips

In photonic circuits, light is routed through waveguides between functional building blocks. These can can be separated into two distinct categories: on one hand we can identify subcircuits consisting of time-invariant linear elements, such as beam splitters, wavelength filters, mode filters, polarization rotators and delay lines. These can be described by a transfer matrix or scatter matrix which couples the light between the waveguide ports (and modes, if the waveguides support multiple guided modes). On the other hand we have all the other building blocks like modulators, photodetectors and amplifiers. In an ASPIC, the linear parts of the circuit are custom designed for a desired function, either with a static configuration or with electro-optic tuners to adjust the behavior. This tuning can in most cases still be considered as time-invariant, because the tuning time-scale is much slower than the optical processes on the chip. As it happens, these passive circuits (and especially wavelength-selective filters) turn out to be difficult to design in a robust way because of fabrication variability [8], [24], [25].

Programmable PICs replace the custom linear circuitry with a generic circuit that can be reconfigured to provide the desired connectivity, connecting the functional building blocks together with the correct transfer/scatter matrix, as illustrated in Fig. 1. The top-right inset shows the key element in such a circuit: a 2×2 coupler which can adjust the coupling ratio between two waveguides, as well as the respective phases in the output ports. There are several methods to practically

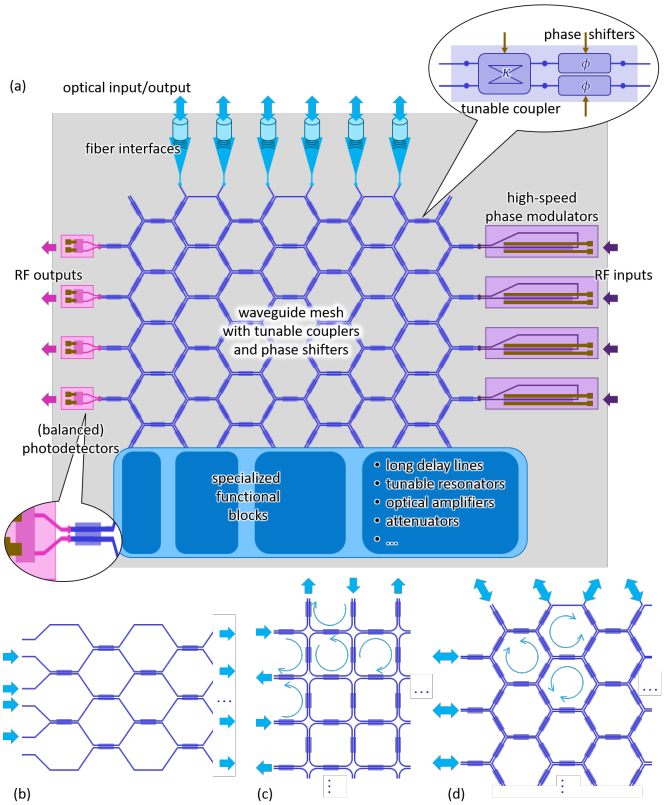

Fig. 1. Basic concept of a programmable photonic circuit, where a reconfigurable linear circuit connects the optical fiber ports, the modulators (RF inputs) and balanced photodetectors (RF outputs) together with the other functional blocks. The central mesh itself consists of electrically actuated 2×2 couplers and phase shifters. (b-d) different examples of forward-only and recirculating mesh topologies: (b) a forward-only mesh where light flows from left to right and is mixed along the various stages by the 2×2 couplers [22]; (c) a recirculating mesh with square cells, where light flows either clockwise or counterclockwise in a cell [17]; (c) recirculating mesh with hexagonal cells, where the arrangement can coupler clockwise and counterclockwise circulating light, making all ports equivalent [23].

implement such a tunable 2×2 coupler, but the most common approach is a Mach-Zehnder interferometer with a phase shifter in at least one arm. Also, at least one other phase shifter is required to provide the two degrees of freedom (coupling ratio and phase delay between the ports). This 'universal unitary gate' makes it possible to implement any 2×2 unitary transfer matrix between inputs and outputs [22], [26]. Combining these gates in meshes with different topologies makes it possible to define arbitrary linear relationships between the circuit ports. For these mesh circuits, many names such as '(nano)photonic processors', 'reconfigurable photonics' or 'field-programmable photonic gate arrays' (after the electrical FPGAs) have been coined [19], [27]. Figure 1b-d shows different topologies of such meshes. In *forward-only* meshes light is expected to propagate in one direction through the mesh, and the ports are separated into a set of inputs and outputs [22], [26], [19], [16]. In a *recirculating mesh*, the waveguides are organized in coupled loops or rings, which allows coupling from any port to any other port [17], [18], [20]. Also, in the recirculating meshes the optical path can be encoded with discretized delays, which makes it possible to construct interferometric

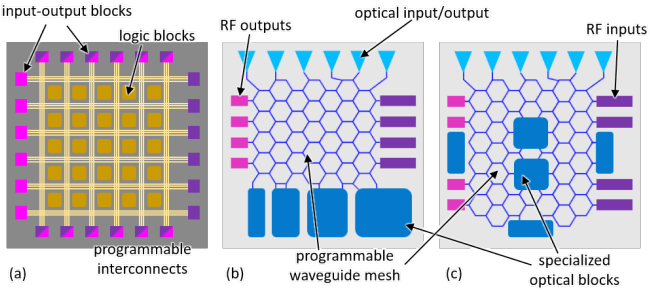

Fig. 2. Similarities between a generic programmable PIC and an electronic field-programmable gate array (FPGA). (a) an electronic FPGA consists of logical blocks and I/O blocks connected together in a programmable electrical interconnect mesh. Pictured here is an island-style architecture [28]. (b-c) A Generic programmable PIC consists of a programmable waveguide mesh that connects optical and RF input/outputs with specialized functional blocks. There are different possible architectures to position those specialized blocks.

wavelength filters and resonators. Both types of meshes are programmed by electrically setting all the tunable couplers and phase shifters to their desired state.

The other functional elements in the circuit are connected to the mesh, usually on the outside, but it is also possible to place islands inside the mesh, as shown in Fig. 2. Using high-speed electro-optic modulators, a microwave signal can be encoded onto an optical carrier wavelength, and (balanced) photodetectors can be used to demodulate the signal [21]. Balanced photodiodes have two input waveguides, and the output current is proportional to the difference of the input powers in the two input waveguide ports, making it possible to control both the magnitude and the sign of the output current. These functions turn the programmable PIC into a microwave processor, where microwave signals can be filtered or corrected in the optical domain [21], [18], [17]. Other blocks such as amplifiers can boost the optical signals or perform nonlinear operations, and long optical delay lines can be used to physically delay the signals, such as needed in microwave phased array antennas [29].

III. More than just Photons

The waveguide meshes themselves can contain hundreds or even thousands of tunable coupler and phase shifter elements, that all need to be actuated to deliver the light on the chip to its destination. To make this work, the programmable PIC becomes more than just a photonic chip: the optical circuit is merely one element in a technology stack to manipulate light. The PIC requires driver electronics, monitor circuits, control loops, a software interface and programming algorithms to bring the functionality to the user, and all the components need to be properly packaged to handle a multitude of optical and electrical (either low-frequency or RF) input and output signals. The various elements in this stack are schematically illustrated in Fig. 3.

This is similar to the use of FPGAs and microcontrollers. While these programmable electronic chips can be purchased as bare dies, they usually come packaged in a ball grid array (BGA) or similar enclosure, or already mounted on a printed circuit board with the necessary peripheral components and

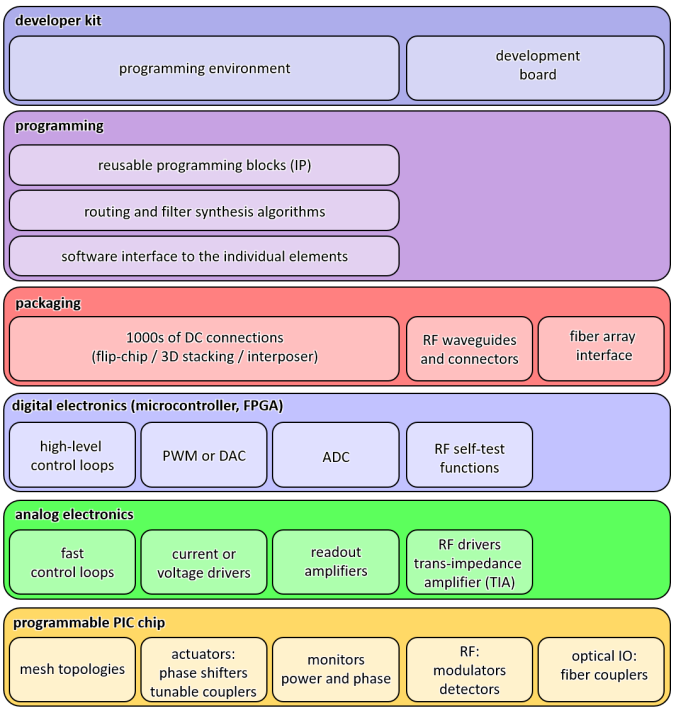

Fig. 3. Technology stack around a programmable photonic circuit. The photonic chip is just the basic hardware layer, but requires electronics (analog + digital) to control the phase shifters and 2×2 couplers and read out the monitor photodetectors. Given the large number of optical, electrical and RF signal ports, good packaging strategies are important. Specifically for programmable photonics are new layers with software routines and abstractions that enable the reconfiguration. These need to be made available to users through accessible development kits to lower the threshold of adoption.

a connectivity interface (e.g. USB or ethernet). On top of that, these chips come with a software toolkit that makes it easy for the user to program functionality, and often advanced functional programming libraries or IP (intellectual property) blocks can be sourced from third parties. As a result, the electronic 'chip' comes ready to be configured and used by the developer [11].

Therefore, when discussing programmable PICs, it is important to include the various technologies in and around the chip that are essential to provide a similar complete technology stack.

- **Optical waveguides** are the core of the photonic circuit. Because the light path through a programmable PIC is generally longer than through an optimized ASPIC, waveguides need to be of good quality, with low loss and phase errors. While silicon waveguides currently have propagation losses of less than 1dB/cm and are getting better [30], [31], [32], silicon nitride technology might offer lower losses, but the larger bend radius will result in a larger circuit [33], [34]. Steady technological improvements in losses and phase errors will be crucial to the performance and scaling of programmable PICs and it is clear that the addressable application space will depend very much on the total accumulated losses in the circuit. Apart from the waveguides, other elements in the circuit need to be optimized for low loss and compact footprint [35].
- **Electro-optic phase shifters** are one type of core actuators in a programmable waveguide mesh. Again, they need to have a low insertion loss because light has to traverse many components within the circuit. The most commonly used actuators are thermo-optic, inducing a phase shift by locally heating the waveguides [36], [37]. While this mechanism does not induce optical losses, it is power hungry and can be a cause of thermal crosstalk between the many actuators [38]. Alternative actuation mechanisms such as micro-electromechanical systems (MEMS) [39], [40], [41], piezo-electric tuners [42], liquid crystals [43], [44] or Pockels-effect based phase shifters [45], [46], [47] could address these issues, but these techniques still have to reach sufficient maturity. The choice of the actuator type also depends strongly on the speed at which the circuit needs to be configured. When the circuit configuration is mostly static, the time constants of MEMS, liquid crystals or heaters (10-100μs) is not an obstacle. For applications where very fast switching is needed, the Pockels effect with its sub-ps response time is the preferred mechanism, even if it is much weaker.
  Many applications that require a slow response could benefit from non-volatile actuation mechanisms, which do not require constant electrical control to maintain their state. Possible mechanisms for non-volatile actuation include MEMS [40] and phase-change materials [48]. In applications where reconfigurability is not a requirement and the PIC needs to be programmed only once, active phase shifters can be replaced with a one-time trimming operation where the correct phase shifts are applied by locally adding/removing material [49], inducing stress [50], or manipulate the material composition or defect density [51], [52]. This dramatically reduces the need for active control.
- **Tunable 2×2 couplers** are needed to configure the connectivity and interferences in the waveguide mesh. They can be implemented as tunable directional couplers [39], [53], or as a Mach-Zehnder interferometer with phase shifters [54]. Just as with the phase shifters, the most common actuation mechanism today is thermo-optic. But as with phase shifters, developments are underway to make tunable couplers more efficient based on electrostatic actuation with MEMS, liquid crystals or electro-optic materials. Here, too, trimming mechanisms can be considered for one-time programming.
- **Monitors** will be essential in keeping the circuit running stably in its programmed state, and need to observe the optical power (and phase) within the circuit without imposing a substantial optical loss. Techniques such as the contactless integrated photonic probe (CLIPP) [55] or in-resonator photoconductive heaters [37] can monitor the optical power in the waveguide based on the losses that are already present. Because certain functions in a programmable circuit require interference of coherent light (e.g. wavelength filters), not just power monitors are needed, but also phase monitors, which require an additional interferometer, which needs to be integrated

as compactly, and with as little perturbation as possible, into the photonic circuit [56].

- **High-speed modulators** and **(balanced) photodetectors** serve as the input and output for microwave signals in the programmable photonic circuit [21]. Whether they are needed depends very much on the application of the circuit. Given that the integration of these components in a PIC platform can dominate the overall cost of the chip, different flavors with and without these high-speed components can be considered.
- **Amplifiers** add gain to the optical circuit, which can be used to compensate optical losses, but also to implement (programmable) light sources directly in the circuit. While integration of gain is native to most III-V material platforms [2], integration in silicon (nitride) is still not pervasive but steadily becoming more mature [57], [58]. An overview of new developments for the integration of light sources in silicon photonics can be found in [59]. Because the light source depends very much on the application (wavelength, linewidth, ...), we will not take it directly into account in the calculations presented further in this paper, and instead assume that in the short term the user/developer will bring in the light from an external LED or laser through an optical fiber or co-packaging scheme [60], [61]. Other material systems than silicon, such as III-V semiconductors, which do support integrated light sources [2], could also be considered. But there are currently no established platforms that offer a similar high refractive index contrast and integration scale as silicon.
- **Circuit architectures** of the waveguide mesh define the possible functions of the programmable PIC. Waveguide meshes can be implemented with forward-only connectivity, connecting a set of input ports to a set of output ports [14], [15], or as a mesh with square or hexagonal rings which enables recirculation of the signal, forming discrete path length differences or resonators [17], [18]. Future architectures for larger meshes might require hybrid configurations, which allow for long-distance low-loss connections or different connectivity topologies, with different choices of where to incorporate the high-performance active components.
- **Driver and readout electronics** are needed to apply the voltage or current to the actuators, and read out the signals from the in-circuit monitors. These circuits usually involve a combination of analog and digital electronics, using either digital-to-analog convertors (DAC or direct digital pulse-width modulated (PWM) signals [62], [63]. The precision of these drivers should be sufficiently high to limit the imperfections in the phase and power control of the light in the circuit. Given that there can be hundreds or thousands of actuators on the photonic chip, these electronics need to provide sufficient parallel channels. For this discussion, we did not consider technology platforms where the photonics and the electronics are integrated on the same chip [9], [64], [10]. Monolithically integrated photonic-electronic ICs might well provide the most flexible platform to implement programmable PICs, but the cointegration will always require trade-offs: silicon photonic building blocks require different layer thicknesses and much larger feature sizes than deep submicron CMOS nodes. Bringing both together on the same substrate implies that the processes cannot be optimized for both the photonics and the electronics, which can translate in higher propagation losses, or slower/more power hungry electronic circuits. Therefore, in this paper, we have assumed a technology where the photonics and electronics are built on separate chips, each in the most suitable technology. Such hybrid integration introduces challenges as well, as the large number of actuators and monitors need to be electrically connected between the photonic and the electronic chip. This could require clever multiplexing techniques [65] or scalable approaches at the packaging level.
- **RF electronics** might be needed for applications where the optical chip needs to handle radio-frequency signals which are processed on the optical chip. Especially when converting the optical signals back to the RF domain using (balanced) photodiodes, a trans-impedance amplifier (TIA) is needed to boost the signal [66]. Also at the RF inputs there might be need for an RF amplifier before the signal is sent into the electro-optic modulator and some auxiliary electronic of optical circuits might be needed to compensate for nonlinearities in the modulator response curve or unwanted amplitude modulation in an electro-optic phase modulator [67].
- **Packaging** the photonic and electronics chips together, and bringing the inputs and outputs (optical, electrical

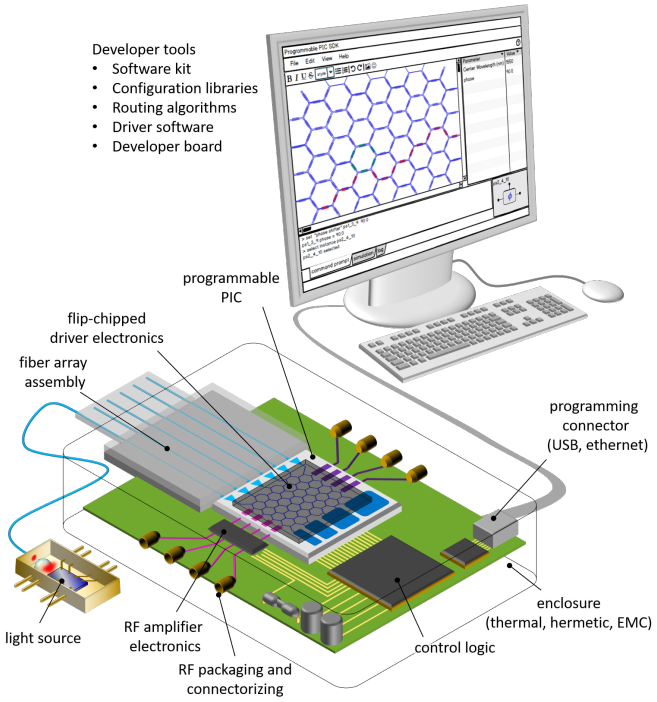

Fig. 4. Assembly of a programmable PIC (electronic, photonic, RF, thermal management, IOs). Especially the high-speed RF functionality can impose significant constraints (and therefore cost) on the interfaces and packaging.

and RF) to the outside world, is far from trivial [68], [69], [70]. The external requirements are illustrated in Fig. 4. The integration of the photonic chip with its many driver channels will eventually require a close integration with electronics, most likely involving some form of flip-chipping or 3D stacking [71], [72], [73], [30]. The scalability of these approaches depends strongly on the speed of the (re)configuration: many high-speed connections will give rise to interference and crosstalk. Given that today packaging is one of the dominant cost factors for ASPICs, it is expected that this will also hold for programmable PICs. A significant challenge (and cost) of packaging goes into the handling of high-frequency microwave signals going into and coming out of the chip [70], [74].

- **Control loops** are needed to maintain the photonic circuit in its desired configuration. These loops should function at a low level to reduce complexity, and drive the actuators in response to the monitoring signals. Labeling the optical signals with unique low-frequency tones can help to disentangle multiple signals within a waveguide [75].
- **Programming routines** control the chip at a higher level, determining how tunable couplers and phase shifters should be set to implement a function, such as signal routing, distribution networks, or wavelength filters. Graph-based routing algorithms, such as those developed for FPGA programming, can be of great help here [76], [77]. In a waveguide mesh, not only the efficient use of actively used couplers is important, but also the control of the unused couplers, as the effect of small parasitic light flows mush be minimized [78], [79]. These effects become more pronounced when the waveguide meshes become larger.
- A **programming abstraction layer** and a **programming toolkit** can help developers to reason about the optical functionality on the chip in an abstract way, even to the point that the concepts can be applied in different circuit architectures. Just like electronics can be programmed with high-level languages, programmable photonics will need such an abstraction layer.

This technology stack presents a costly bill of materials to enable the use of programmable PICs. But this stack is not unique to programmable PICs: many of these layers are also required when implementing systems based on ASPICs, but for most of these the number of actuators, monitors and input/output channels is kept to the minimum needed for the specific application. Programmable PICs, because they are conceived as a generic chip, will almost always be overdimensioned in one or more functions, and this will in most cases induce higher optical losses and higher power consumption than in an optimized ASPIC. But even an ASPIC will require driver electronics to tune its functionality, because purely passive silicon photonic chips generally suffer quite a lot from fabrication variation [80]. While the programmable PIC will not outperform a tuned ASPIC, it could well, for many functions, outperform an ASPIC without built-in tuning capabilities.

When we look at the various elements in the technology stack, we see a recurring item that greatly contributes to the cost of the system: the handling of high-frequency microwave signals [70], [74]. High-speed modulators and photodetectors, their respective electronic amplifiers, and correspondingly the packaging with RF connectors introduces a significant cost. Therefore, when considering the concept of a 'generic' programmable PIC, it might be convenient to consider a version with and without support for microwave signals, each tailored to a different application space.

Another cost in the system is the light source, without which the photonic chip would not function. While there are a multitude of promising light source integration techniques both established and under development [59], we have decided to keep the light source out of the remainder of the discussion in this paper. The motivation for this is that the choice of ligth source can be very dependent on the application, ranging from cheap fiber-coupler LEDs to narrow-linewidth tunable lasers, with a cost that can vary over several orders of magnitude. As both the ASPIC and the programmable PIC require similar light sources for each application, we can, in a first-order approximation, leave the light source out of the comparison.

IV. Large Volume Manufacturing of Programmable PICs

With the technology stack described above, programmable PICs seem to be significantly more costly than ASPICs: the chips are larger, require more complicated control electronics, and the packaging needs to accommodate a large number of input and output ports. In this light, will it make economic sense to use these programmable PICs? The same question can be raised about their electronic counterparts. Just like programmable PICs, these chips are larger and more power hungry than an optimized electronic ASIC, and yet there exist a broad variety of such programmable electronics (from low-cost to high-performance) that are used in a wide range of applications [11].

A. Shared Non-Recurring Engineering Costs

The key benefit of using programmable chips is in the savings in non-recurring engineering (NRE). Table I lists the NRE costs for a fabless company developing an ASPIC based on engineering runs in an established silicon photonics foundry [4], [81]. We make use of a standard platform offering, so additional process development costs for customizing the fabrication process are not considered here. When this is needed, it will add significantly to the overall cost, depending on the needed customizations. The numbers we quote here represent orders of magnitudes: the costs can vary significantly depending on the complexity of the chip and the eventual product [82], [83].

For a product based on an ASPIC we assume that we will need a PIC, a custom electronic driver IC, and a package. As mentioned before, we will also require an external light source, but we do not take this into account here. All these hardware elements involve a preparatory design stage, fabrication and testing. On top of that, a usable product will require a software

TABLE I
OVERALL COST ESTIMATES FOR DEVELOPING A SINGLE ITERATION OF A SILICON PHOTONICS ASPIC.

Development Stage	**NRE costs (k$)**	**Time (months)**
PIC design	50 - 200	4
Driver IC design	100 - 200	
PIC fabrication (1 run)	100-300	4
Driver IC fabrication	30-100	
DC package development	50 - 100	2 - 4
RF package development	100 - 400	
Programming / interface	50 - 200	2
Testing	100 - 300	2
Total	**580 - 1800**	**12***

* Some tasks run in parallel

TABLE II
COST ASSUMPTIONS FOR THE SCENARIOS OF *No-RF*, *Few-RF* AND *Many-RF* PHOTONIC INTEGRATED CIRCUITS.

	Low-RF	Few-RF	High-RF	
RF input ports	0	2	16	
RF output ports	0	2	16	
Fiber ports	4	4	16	
ASPIC				
PIC area	4	5	48	mm^2
Electronic IC area	5	5	15	mm^2
Package development cost	100	150	500	kUS$
PIC design effort	4	4	12	PM
EIC design effort	4	4	12	PM
Testing effort	4	4	8	PM
Programmable PIC				
PIC area	10	15	160	mm^2
Electronic IC area	20	20	50	mm^2
Package development cost	150	250	800	kUS$
PIC design effort	8	8	8	PM
EIC design effort	12	12	18	PM
Testing effort	4	4	8	PM

layer to interface with the user or the larger system. Taking all this, added up in Table I, we see that the development cost, starting from design all the way to testing, easily runs well over a million US$, and this is assuming a single, first-time right development cycle. Also, the development time is at least a year, even when some developments are done in parallel (e.g. PIC, driver and packaging design and fabrication). This is not only a significant upfront cost in product development, but it also creates a long time-to-market, presenting competitors with a window to position alternatives. Note that the numbers listed in Table I are indicative, and can easily be off with a factor of 2-4, depending on the complexity of the project. The numbers indicate the development costs and time of a product prototype, not the actual costs of the production in volume.

On the other hand, when using off-the-shelf components to build a system, a lot of the costly (in time and money) development steps of designing and fabbing custom silicon can be skipped. This is the same value proposition as FPGAs and other types of programmable electronics [11], [84]. Once an entire technology stack for programmable PICs is in place, the same benefits hold for packages, driver electronics and software libraries. The NRE costs for a programmable PIC are very similar to that of an ASPIC, with potentially a slightly higher cost because of the complexity (and footprint) of the programmable PIC. From the point of view of the user, these development costs are essentially prefinanced and distributed over all the users of a 'standard' programmable circuit. A programmable PIC that comes bundled with its driver IC, a standard package (with or without RF capabilities) and developer kit, can cut down the initial development time for a new product prototype from more than a year to a few weeks or months.

Because a programmable PIC consumes a large chip footprint, requires more driver electronics and generally has more available ports (optical and/or RF) than needed for many applications, it is likely to be more costly per chip than a custom ASPIC *fabricated in the same volumes*. But then, there are at this point only few PIC-based products that really require high production volumes, as measured by the standards of silicon foundries. Even the worldwide datacenter communication market is predicted to consume only a small fraction of the silicon photonics production capacity in the foreseeable future [85], [86], [87]. And many low-volume products require only one or a few production lots to satisfy a market of 100-10000 units. Generic programmable PICs, exactly because they can be used in a diversity of products, can be made in larger volumes (which will still be low or modest compared to volumes of many commercial CMOS chips). This will lower the cost of the chips, as production batches can be run on a more regular schedule.

A commonly used programmable PIC is not the only requirement to enjoy the benefits of scale for photonic integrated circuits. One of the most costly aspects of today's PICs lies in the packaging [68], [69], [70]. Interfacing a photonic chip with optical fibers is still cumbersome, although there is a steady progress towards low-cost passive fiber alignment techniques. Having only to support a single fiber attachment process for a multitude of applications could also present a benefit for programmable PICs. As we already mentioned, a second costly aspect, which also relates to packaging, involves the handling of radio-frequency signals that go into, or come out of the photonic chip. Packaging for RF signals with frequencies in excess of 20 GHz is complex and costly, requiring expensive ceramic carrier substrates, connectors and careful design to avoid losses and crosstalk. In that light, it makes sense not to push standardization too far, and consider at least two flavours of programmable PICs and their packages: with and without support for RF signals. These might consist of different PICs, or of the same PIC but in different packages. It will avoid that the cost of programmable PICs for non-RF applications is dominated by unused RF functionality.

The integration of the light source follows the same reasoning. Because there can be such a wide variation of light sources for different applications (LEDs, tunable lasers, modelocked

TABLE III
COST CALCULATION ASSUMPTIONS FOR BOTH ASPICS AND PROGRAMMABLE PICS. FOR PIC DEVELOPMENT A DEDICATED ENGINEERING RUN IS ASSUMED [4]. FOR THE ELECTRIC IC DEVELOPMENT, PARTICIPATION IN A MULTI-PROJECT WAFER RUN IS ASSUMED (PRICES BASED ON EUROPRACTICE IC [82] AND CMP [83]).

Photonic SOI substrates (200mm)	300	US$
Number of mask layers	25	
Reticle cost per mask layer	3'000	US$
Processing cost per lot	125'000	US$
Yield of PIC fabrication	80	%
Electronic IC cost (development) [82], [83]	1'500	US$/mm^2
Electronic IC cost (volume) [88]	1	US$/mm^2
Packaging cost RF (volume)	10	US$/port
Assembly cost (volume)	10	US$/chip
Engineering cost	10	US$/PM

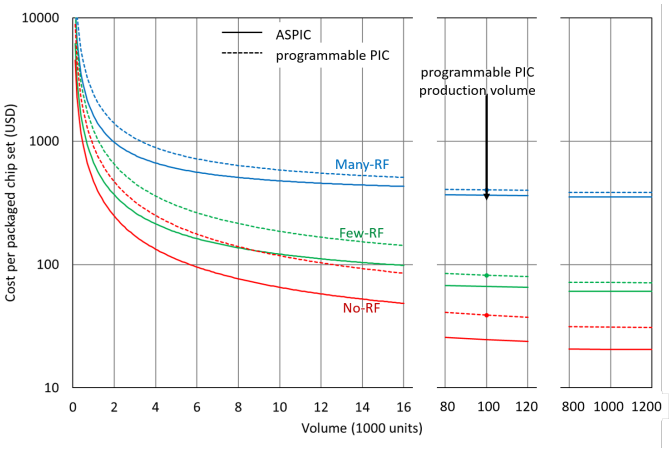

Fig. 5. Cost per packaged chip set as function of volume.

lasers, ...), we have taken the light source out of the comparison. It is then up to the user or system integrator to choose a light source with the correct wavelength range and linewidth properties.

The benefits of programmable PICs in term of NRE cost reduction and time-to-market are exactly the same as those of programmable electronics such as FPGAs. While these components will be more expensive and have lower performance than a dedicated ASIC, they can be used off-the-shelf and deployed in a product in a short development cycle. It might turn out that the performance does not satisfy the needs of the market (e.g. too high power consumption for a wearable device), but the value proposition can be tested much quicker and can justify the development of a next-generation prototype based on a more performant ASPIC. Also, in the market of programmable electronics we can discern a wide diversification, from different device types (microprocessors, DSPs, FPGAs, ...) to different performance envelopes (low power vs. high-speed) and price points. As the application space for PICs will grow, so will the need for diversification of programmable PICs [4].

B. Cost Calculations

For a more detailed cost comparison between ASPICs and programmable PICs, we we try to capture the large spread in NRE costs in Table I by building a simple cost model for three technical scenarios, dictated by the number of RF ports:

- **No-RF**: A photonic circuit that does not require high-speed input/outputs (e.g. a sensor interrogator), but still requires the integration with an electronic chip for control and readout.
- **Few-RF**: A photonic circuit that has two RF inputs and outputs, and 4 fiber ports. Such a circuit could be useful for an RF sensor readout or a driver for a microwave antenna in a radio-over-fiber scenario.
- **High-RF**: A photonic circuit that can handle up to 16 RF inputs and outputs as well as 32 fiber ports. Possible applications for such a circuit could be as a driver for a phased-array antenna in a radio-over-fiber link, or a distribution point in a hybrid optical/xDSL access network.

The cost model is based on the processing costs for wafer scale processing (similar as [89], [90]) and for packaging we assume evolutionary improvements on today's technologies, which means the costs still carry a significant per-unit cost, especially for the high-speed RF interfaces [91], [70], [68]. We detail some of the basic specifications for the different scenarios in Table II. Other assumptions in our cost calculations based on wafer cost, processing costs and number of mask layers in today's 200 mm silicon photonics processing platforms, are listed in Table III.

We separate the costs into a one-time upfront development cost (or NRE cost), and the per-chip fabrication cost during volume production. The NRE costs include the design of the photonic chip, electronic drivers, and packaging, as well as the development of the software to control the chips. For this we take both manpower and material costs into account, including an engineering run to test a chip prototype.

$$C_{\mathrm{NRE}} = C_{\mathrm{design}} + C_{\mathrm{engineering}} + C_{\mathrm{maskset}} \tag{1}$$

The cost for the volume fabrication per chip set c_{fab} is based on a cost per process step and per batch of wafers, and divided over the number of chips per wafer N_{cpw} (or per batch) , and we estimated this separately for the photonic and electronic chips. We also incorporated an overall fabrication yield γ of 80% after fabrication and testing:

$$c_{\mathrm{fab}} = \frac{1}{\gamma}\left(\frac{c_{\mathrm{fab,p}}}{N_{\mathrm{cpw,p}}} + \frac{c_{\mathrm{fab,e}}}{N_{\mathrm{cpw,e}}} + c_{\mathrm{packaging}} + c_{\mathrm{testing}}\right) \tag{2}$$

The numbers we use are focused on an early ecosystem for programmable PICs, targeting applications that do not require the high fabrication volumes or extreme performance that would automatically require the development of a dedicated ASPIC.

The NRE cost for both the ASPIC and the programmable PIC is spread over *all* fabricated chips N_{fab}: the larger the volume, the smaller the contribution of the NRE. The cost per chip set then becomes

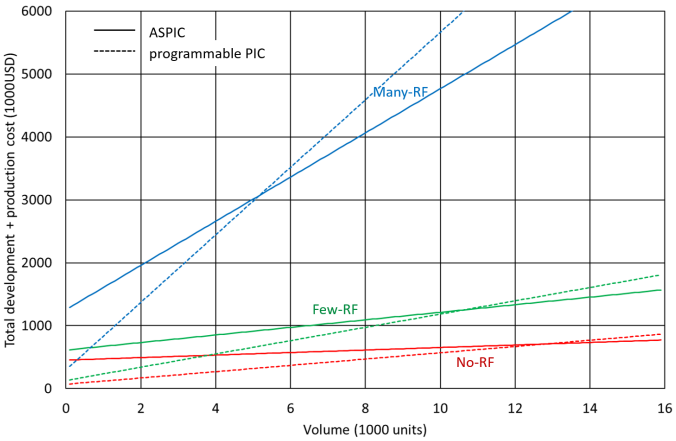

Fig. 6. Total cost (development and production) for a PIC-based product as function of volume.

$$c_{\text{chipset}} = c_{\text{fab}} + \frac{C_{\text{NRE}}}{N_{\text{fab}}}. \tag{3}$$

Figure 5 plots an estimated cost per fabricated chip set (photonic IC + electronic driver IC), as function of production volume in the low-volume regime.

The NRE costs obviously dominates for very small numbers of chips. This is true for all scenarios, for both the ASPICs and the programmable PICs. As in each scenario the programmable PIC is larger and more complex than the corresponding ASPIC, we clearly see that the dotted cost curves (programmable PIC) are systematically higher than the solid curves (ASPIC). However, we can assume that a programmable PIC supplier has its chips fabricated in higher volumes N_{fab}, and is stocking a modest volume of 100'000 units, which could then be purchased off the shelf by system developers or businesses with low-volume products (i.e. 10'000 units). On the right side of the graph we see that, when produced in larger volume, the cost of the programmable PIC does drop below the cost of ASPICs at lower volumes. This indicates that a model where programmable PICs are preproduced in larger volumes as a component for low-volume applications could be viable.

This is made even more clear in Fig. 6, which plots the total development and production cost of a product developed with an ASPIC (C_{ASPIC}) and a programmable PIC (C_{PPIC}), for the three scenarios. For low volumes the programmable PIC is significantly cheaper than the ASPIC, because the NRE costs for a custom ASPIC are spread over a small number of chips $N_{\text{fab}} = N_{\text{ASPIC}}$:

$$C_{\text{ASPIC}} = C_{\text{NRE}} + c_{\text{fab}} \cdot N_{\text{ASPIC}} \tag{4}$$

On the other hand, the NRE costs for the programmable PIC are spread over a much larger number of chips (in this case $N_{\text{PPIC}} \ll N_{\text{fab}}$ =100'000). Of course, the programmable PIC supplier, acting as a buffer between the fab and the system developer, will add a profit margin to the programmable PICs, which we here calculate as 30% of the cost:

$$C_{\text{PPIC}} = 1.30 \cdot \left[C_{\text{NRE}} \cdot \frac{N_{\text{PPIC}}}{N_{\text{fab}}} + c_{\text{fab}} \cdot N_{\text{PPIC}} \right] \tag{5}$$

As volumes increase and the NRE costs are spread over more units, the ASPICs will become cheaper than the off-the-shelf programmable PICs. We see that this crossover point is likely to happen at lower volumes for the more complex scenarios, but the actual points depends very much on the specifics of the application, and how much customization is needed in the packaging and the programming of the programmable PIC.

One benefit or programmable PICs, which is not taken into the calculation, is the lower opportunity cost, as the development time from idea to product can be dramatically shorter. We did not put a specific cost on this, as the importance of time-to-market depends very much on the application space.

C. Supply Chain

Developing a product based on a photonic integrated circuit requires a combination of photonics design and manufacturing, electronics (including RF) design and manufacturing, packaging technologies and software development [92].

Unless all these capabilities are available in house, this requires setting up a supply chain to source the expertise and materials. Both PICs and electronic circuits can be fabricated in a foundry [3], [4], and as already mentioned, each generation takes about 1 year to design, fabricate and test. And after development, the lead time for chip fabrication in volume will also take several months, depending on the fab schedule to start up photonics production lots. Custom electronics have a similar timeline. In order to buffer for these long lead times, sufficient stock of both photonic and electronic ICs is needed.

Programmable PICs, because they can serve many applications and therefore many customers, could cut this supply chain in half, as shown in Fig. 7. A chip vendor, or rather a chipset vendor (selling the combination of the photonic IC and the matching driver and control electronics), essentially becomes a buffer. Because these chips will be fabricated in higher volumes, and because there are fewer large programmable PICs on a wafer than specialized ASPICs, wafer-scale production can run on a more regular and predictable schedule.

Because the programmable PICs and their driver electronics (or at least their software and hardware interfaces) can be kept known and stable over a longer lifetime, it creates opportunities for third parties to build service offerings around these chip sets. Packages and assembly services (especially for the RF and optical interfaces) can be cheaper for standardized chips than for bespoke ASPICs. And because a lot of the functionality of a programmable PIC is defined by the programming, this can create a market for software algorithms and programming services, and even professional design environments.

While such an ecosystem relies on standardized or commonly available chips, it does create more choices for product development, and can drastically reduce the time to market, as well as the time to volume scaling.

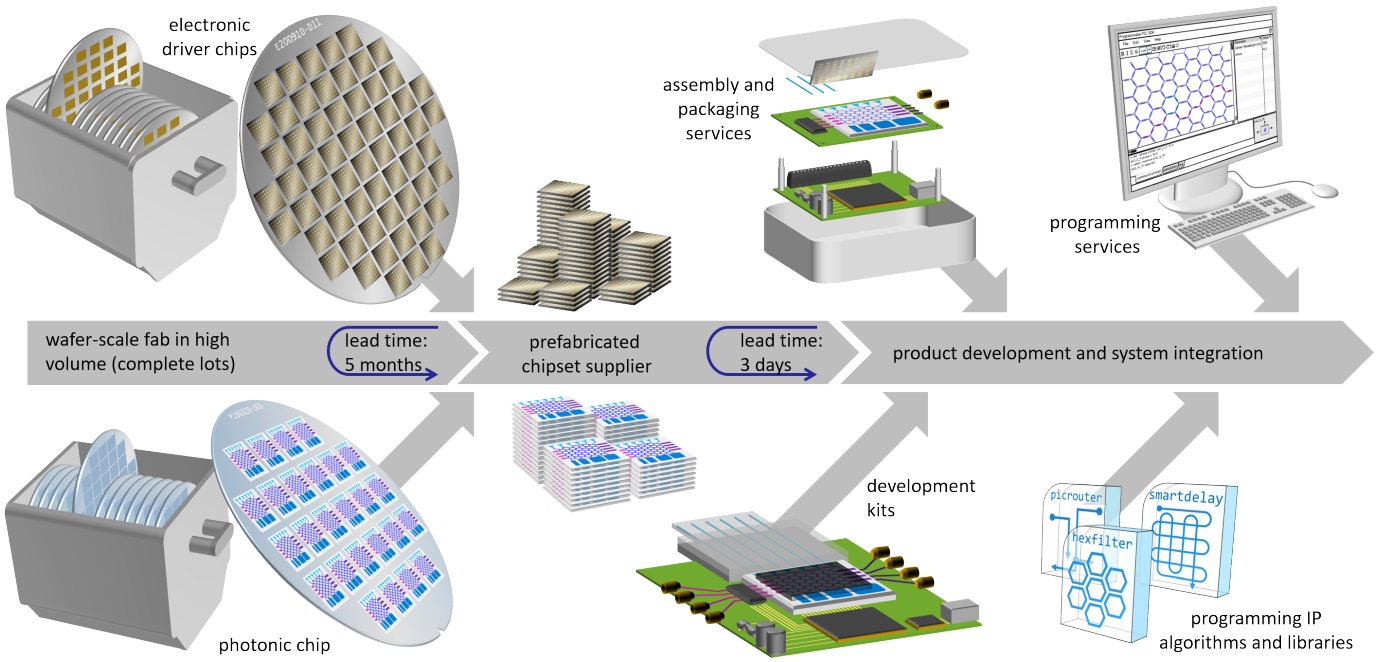

Fig. 7. Supply chain for programmable PICs. Mass manufacturing the programmable PICs upfront essentially splits the supply chain in half, dramatically shortening the time to obtain working PICs. the same holds for the electronic driver ICs. Developing a programmable PIC into a product still requires development of a package, and of course the routines need to be implemented to make the circuit perform its intended function. Here, too, arise opportunities for service and IP providers.

V. Applications for Programmable PICs

One of the key value propositions of programmable PICs (compared to ASPICs) is that they can be deployed in a variety of applications. But do these application exist, or is there at least a potential for sufficient volumes? We can separate the application spaces into three segments

- Applications that already make extensive use of ASPICs, most notably in the telecommunication and datacommunication space. These either consist of compact PICs that can be made in sufficient volumes (e.g. datacenter transceivers[86]), or complex PICs in lower volumes where the cost of the PIC represents only a small fraction of the overall system (e.g. wavelength routers in a long-haul telecom network).
- Applications where there is today a strong push to develop PICs (and mostly ASPICs) but where the technology or market has not yet matured to produce commercially viable products. This includes various sensing techniques such as (bio)chemical sensing [93], [94], spectroscopy [95], [96], LiDAR [97], [98], but also developments into microwave photonics [21], quantum information processing [26] and accelerators for artificial intelligence applications [19].
- Applications where currently no migration towards PICs is being pursued (or only on a very small scale), but which could benefit from on-chip manipulation of coherent light. Many of these applications are, by definition, still unknown, and the initial market potential (or societal benefit in the case of publicly funded research) appears to be too small to warrant the significant development investment today. Customized photonic sensors or readout circuits for internet-of-things appliances would fit under this umbrella.

The impact of programmable PICs will be different in each of these segments. To gauge this, we should keep the key benefits of programmable PICs in mind:

- Programmable PICs accelerate development of new functions because they bypass the process of designing and fabricating a custom ASPIC.
- They can be price-competitive to deploy in smaller volumes as the NRE costs are shared among all users of the PIC.
- They can be reconfigured, or functionality can be upgraded, in software.

On the other hand, it should be kept in mind that programmable PICs will most likely have lower performance (e.g. insertion loss) and higher power consumption than a dedicated ASPIC, and they can become significantly more expensive in high-volume applications. There will also be applications where the programmable PICs cannot meet the specifications. This can be for various reasons, e.g. because the required wavelength range is not supported, or because the programmable PIC cannot handle high optical powers. In the case of optical filters, the programmable mesh might not provide the required wavelength precision or a sufficiently large free spectral range. Programmable PIC technology can gradually progress to accommodate more advanced specifications, but we expect that there will always be application-specific functions that can only be addressed by an ASPIC.
Let's consider the potential for programmable PICs in a number of application domains. Some of the use cases listed below are illustrated in Fig. 8.

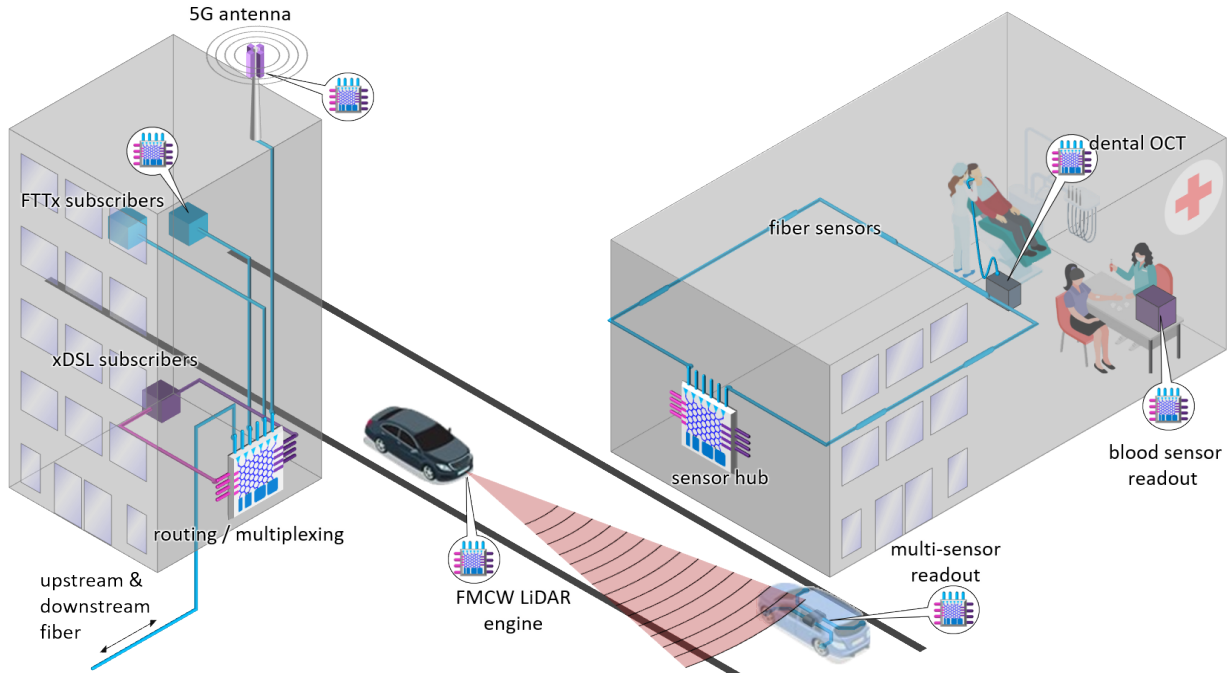

Fig. 8. Possible applications for programmable photonic chips. All the use cases illustrated here make use of coherent light and can operate in the wavelength range around 1550 nm, making them attractive for first generation programmable circuits.

A. Optical Communication

Optical communication is field where photonic integrated circuits are already well established. The penetration started in long-haul telecommunication systems, and is systematically being pushed to shorter length scales (metro, access networks, datacenters, racks). With shorter length scales comes a need for higher production volumes and lower cost per functional unit [86]. The key photonic elements in an optical communication system can be found in the transmitters/receivers, and in the switching, routing and multiplexing blocks that distribute or aggregate the optical signals. In many settings, like intra-datacenter links, the optical link requires the ultimate performance from its components: high bit rate at a minimal energy per bit, and this at a low cost. In such settings, programmable PICs do not make sense, except for accelerating system exploration while the optimized ASPICs are being developed in parallel. Other communication settings might be more amenable to programmable PICs, especially where the performance envelope is not extreme, but deployment (and upgrading) is very costly. Access networks, such as fiber-to-the-home, could well present an attractive market for programmable PICs, with opportunities to update the 'photonic firmware' remotely to enable different modulation formats or adaptively adjust datarates and bandwidth allocation [99].

Programmable PICs are also inherently capable to function as optical switches, and even wavelength routers. The waveguide mesh can be configured to perform one-to-one switching and multicasting/broadcasting. In the context of fiber-to-the-X (FTTx) access networks they could be used in gateways to premises with multiple dwellings, where traffic on an incoming fiber is distributed from different suppliers/operators to different subscribers. Again, the programmability and flexibility or a programmable PIC can extend the lifetime and upgradability of such a FTTx gateway, without the need of a technician to visit on site and manipulate fiber connections. Also, custom low-speed communication networks, such as multi-channel readout platforms for distributed sensors, could benefit from reconfigurable and upgradable programmable PICs. For switching and routing in settings where ultimate performance and power-efficiency is needed, such as datacenters, an ASPIC might be preferred.

B. Sensing

Light can be used for a variety of sensing techniques. Many materials and substances exhibit characteristics spectral features due to absorption, fluorescence or Raman scattering [95]. Also, light can be used to measure distance, movement, strain and a variety of physical phenomena [97], [100], and there has been a strong push to build powerful miniature sensing systems with photonic integrated circuits. From the point of view of the PIC, we can separate these sensors in two categories: PICs that use the actual photonic waveguide structures as the sensor transducer, and PICs that function as the sensor readout system. In the first type of sensor, the waveguide is physically modified such that its amplitude or phase transmission changes with some external event, such as the selective binding of specific (bio)molecules [93], [94], the presence of gases with specific absorption [96] or the application of strain [101]. The result is a change in transmission of the waveguide transducer (such as a long waveguide, an interferometer or a resonator) which can be measured and analysed. Because these transducers need to be physically tailored for the sensing application (e.g. exposure

to gases or integration with microfluidic channels) they are not really compatible with the concept of programmable PICs.
On the other hand, many optical sensing mechanisms also need an optical analysis or readout mechanism. For instance, a spectroscopic gas sensor needs a spectrometer to resolve the specific absorption lines of the gases [96]. Similarly, a fiber Bragg grating sensor needs to identify the shift in reflected wavelength peaks [102]. Such spectrometers can be implemented on a programmable PIC, either by using delay lines to build a reconfigurable wavelength filter [20], or by configuring the circuit as a Fourier transform IR spectrometer (FTIR) [103]. Such a spectrometer could be reprogrammed to provide either a coarse spectrum over a wide band or a high-resolution spectrum over a narrow band. This way, the programmable PIC can also serve as the readout system for the custom PICs that contain the transducer, lowering the complexity and the cost of these ASPICs.
Because a programmable PIC can essentially process any signal with coherent light, it can be configured for free-space sensing applications such as laser-doppler vibrometry (LDV) to measure vibrations or motion [100], optical coherence tomography (OCT) [104] to construct a depth profile of scattering tissue, or distance measurement using frequency modulated continuous wave (FMCW) LiDAR [97], as long as the external signal can be interfaced with the standard fiber ports of a programmable PIC. Most of these applications do not need fast reconfiguration, so can be addressed with programmable PICs with relatively slow actuators (e.g. heaters, MEMS). Optical losses might pose more of a problem: applications like LiDAR are quite constrained in terms of optical power, and the programmable PIC technology should be sufficiently mature to be useful in this setting.

C. Microwave Photonics

In microwave photonics, radio-frequency (RF) signals are modulated onto an optical wavelength, after which the signals can be processed in the optical domain, which is often easier: optical waveguides have lower losses and less dispersion than metal RF strip lines, filter circuits can be constructed from interferometers and resonators and easily tuned to create bandpass filters or equalizers, and RF signals can be converted to different frequency bands by coherently interfering the signal with a laser line at a different wavelength [105], [21].
The programmable PICs as presented are very well suited for these functions: RF signals can be modulated using the high-speed modulators, and reconverted back to RF using (balanced) photodiodes. The waveguide mesh can be configured into custom filter circuits [106], and with optical amplifiers the signal can be boosted or delayed [107]. When multiple modulators are present, the PIC can even process multiple RF signals simultaneously. Because the microwave signals are processed on an optical chip, the system can be much more compact and have higher immunity to electromagnetic interference.
These qualities are useful in areas such as aviation, such as the control of phased array radar antennas [108], and efficient microwave photonic PICs could propagate these high-end systems into more commodity applications such as automotive radar systems. However, recent developments in microwave photonics are largely driven by the need for cost-effective solutions for 5G wireless communication. Radio over fiber (RoF) technologies make it possible to transport many microwave signals over an optical fiber, connecting a single base station to many remote antennas, and keeping the logic and complexity in a single antenna station to a minimum [109]. This reduces the cost of both the equipment and the maintenance of the antennas. A readily available programmable PIC could provide an effective engine for such a remote antenna, with the possibility to update protocols and functionality in software, or upgrade the antenna capacity by adding additional channels or reconfigure it for RF beam forming [110].
For even higher frequencies, programmable PICs could process Terahertz signals in the optical domain [111], [112], even if the built-in modulators and detectors do not scale to these frequencies.

D. Optical Beamforming

Like an RF beam, a free-space optical beam can be constructed from a single large optical emitter, or from a periodic array of smaller emitters. This essentially creates an optical phased array (OPA) where the shape and the direction of the optical beam is controlled by the relative amplitudes and phases in the emitter array [98]. A programmable PIC can provide an engine for this control, as its core functionality is exactly the control of the relative amplitude and phase transmission between its different input and output ports.
Depending on the application of the free-space beam, optical phased array antennas require 10s - 1000s of emitters [113].Programmable PIC will fit best into the applications that require a smaller number of antennas, such as short-range free-space optical communication, or adaptive imaging and wavefront reconstruction. Larger antenna arrays, such as needed for long-range automotive LiDAR [114], will require a dedicated circuit that can scale better with the needs of the application.

E. Neural Networks and Artificial Intelligence

The core of a programmable PIC is a mesh of waveguides that can implement linear transformations between the input and output waveguide ports. Essentially, such a linear transformation can be mathematically expressed as a matrix-vector product. When the waveguide mesh is sufficiently flexible, it can be programmed to implement any scatter matrix, and therefore implement any linear transformation between inputs and outputs. As the optical transit time through the PIC is really short (100ps) this essentially performs a matrix-vector multiplication, also called a multiply-accumulate (MAC) operation, in real time. Combined with high-speed modulators and detectors, it can be used as a computational accelerator for complex matrix operations.
Real-time matrix algebra can support a variety of applications, but one that is gaining a lot of traction is artificial intelligence (AI), and in particular convolutional neural networks (CNN) [115], [116]. Forward-propagating configurable

waveguide meshes have already been shown to work well for matrix-vector multiplication [19]. Whether this makes generic programmable PICs suitable for these applications remains to be seen. The need to maximize capacity of such accelerators, and add additional functionality such as nonlinear activation functions for neural networks [117], might well require the development of ASPICs, even if internally they use the same type of reconfigurable waveguide mesh as in the programmable PIC.

The generic programmable PICs might prove more useful in other types of photonic neuromorphic cumputing schemes. Photonic reservoir computing does not require reconfigurable meshes in its main neural network, but the readout mechanism is based on a linear combination of the outputs where the weights can be reconfigured [118]. Such a programmable linear transformation can be handled either by a generic programmable PIC or by a dedicated ASPIC.

F. Quantum Information Processing

Another field that relies heavily on linear matrix operations is optical quantum information processing (QIP), where information is encoded in single photons [119], [120]. Forward-propagating meshes have already been used to implement a variety of linear quantum gates [26]. While in principle these operations can be carried out by a generic programmable PIC, QIP imposes stringent demands on optical losses, and truly effective implementations would require on-chip integration of single-photon sources and single-photon detectors. This means that, while architectural concepts of programmable PICs can be used for the linear processing, the actual chips will be ASPICs, fabricated in a dedicated technology that supports the special needs for single-photon components.

G. Programmable PIC Intellectual Property

While generic programmable PICs can be suitable for many applications discussed above, they cannot replace ASPICs in situations where custom technology or ultimate performance is required. This does not mean that the programmable PIC technology has no relevance in these application domains. The reconfigurable waveguide meshes, driver and monitor electronics, control loops and programming libraries can be just as useful in the context of an ASPIC where reconfigurability is required, such as the examples above for QIP and neural networks. Also, the programmable architectures can provide a level of redundancy and resilience against failures, even in an ASPIC.

This presents an opportunity for programmable PIC intellectual property (IP) blocks that can be incorporated into a custom PIC design. Such IP blocks would not just define the waveguide layouts, but also a significant part of the overall technology, with guidelines for integration of the driver electronics, all the way up to the software interface to program the tunable couplers and phase shifters in the waveguide mesh. This model can be compared to the widespread use of IP blocks in electronics, where systems-on-chip (SoC) designs combine microprocessor cores, FPGAs, digital signal processing units, digital-to-analog and analog-to-digital converters on the same

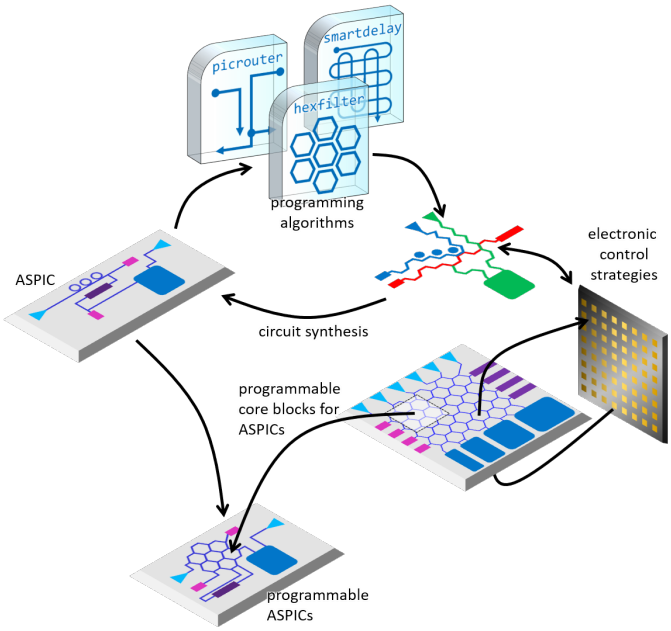

Fig. 9. Different schemes for creating intellectual property based on programmable PICs. Design tools and programming routines can help the developer to translate an ASPIC schematic into a programming strategy for the programmable PIC, such as filter synthesis, placement and routing. Advanced control routines running in the firmware of the controller IC can help the designer monitor the PIC behavior and keeping the program running. In the other direction, a programming strategy can be converted to a full-custom ASPIC layout, or an ASPIC with a programmable core where the control routines can be reused.

die [121]. This reuse of design IP shortens development times, decreases the design complexity, and improves reliability of the resulting chip. Figure 9 illustrates some of the types of IP which can coexist in an ecosystem with programmable PICs: circuit design and synthesis, control strategies and even fully reusable photonic+electronic IP blocks.

Availability of generic programmable PICs or similar IP blocks in ASPICs creates opportunities for a new type of design IP: rather than customized circuit layout, designs can now be described as a configuration or programming routine in a reconfigurable waveguide mesh. Routines for complex routing or filter synthesis could have significant economic value as they can shorten the development time for new prototypes.

Further down the development chain there will be additional opportunities. Even when, after prototyping a product using a programmable PIC, next-generation developments require an ASPIC to scale up product volume or improve performance, new software tools can help ASPIC designers to generate a circuit based on the programming and configuration of the prototype's programmable PIC. ASPICs can either be fully designed from scratch, or consists partially of a programmable photonic circuit where the control routines of the programmable PIC can be reused.

H. The Maker Space

The application space of coherent light is far from exhausted, and we can expect many new ideas to emerge in the coming decades. Low-threshold access to programmable

photonic processors can dramatically accelerate this evolution. Just like the advent of 3D printing has birthed the maker community , and flexible electronics platforms such as *Arduino* and *Raspberry Pi* have made it possible for every hobbyist to build custom electronic widgets, so can generic programmable PICs inspire a new community to build devices that make use of coherent light [122], [123]. This could result in new types of photonic sensors or smart devices home automation, health care and the internet of things.

As photonic integrated circuits become more widely used, and programmable PICs become more flexible and powerful over time, they will also become an ideal platform to provide replacement parts for legacy components: while original PIC or bulk optic components might be no longer available, a programmable PIC can be configured to perform the same function, in a similar way as FPGAs are used today to substitute discontinued electronic components. Because silicon photonics packs a lot of functionality on a small footprint, even 'large' programmable PICs are only ≈ 50 mm^2 in size and therefore likely to fit into existing form factors designed for bulk components or low-contrast PIC technologies.

VI. Conclusion

In the next decade programmable PICs could become a game-changer in the development of new applications based on coherent light. An ecosystem where prefabricated chip sets are available off the shelf, and can be enhanced through packaging and programming, dramatically lowers the threshold for implementing new functionality on photonic chips.

Not only does this model significantly shorten the development time, but for low volumes the sharing of NRE costs over many more users makes programmable PICs a more cost-effective solution than custom ASPICs. We explored this through a simple cost model, which indeed indicates that at low volumes ASPICs are more costly. Of course, like in electronics, there will always be cases where specialized chips are preferable to generic programmable chips, such as in high-volume of high-performance applications.

To make programmable PICs successful, it is essential that the technology stack for these circuits is in place. On the PIC technology side, the key push is for lower-loss waveguides, and power-efficient phase shifters and tunable couplers that do not rely on heaters. Not just the wafer-scale fabrication of the PICs needs to have sufficiently high yield, but cost-effective packaging strategies (especially for high-speed RF interfaces and optical fibers), control electronics and programming algorithms need to be available to use these generic PICs.

Today, all these layers of technologies are just barely sufficient and need to scale in performance, power consumption and price. The first programmable photonic circuits have already been demonstrated, but we expect that the first truly viable prototypes will only be deployed around 2023, with first real products appearing on the market two years later. The most likely scenario is that these will be based on commercial PIC technology platforms which are being set up today [4]. As a result, these first generic programmable PICs will operate only in a limited wavelength band around 1300 nm or 1550 nm, the two most commonly used wavelengths used today in communications, but will diversify down the line.

Within the same timeframe, we can expect the proliferation of programmable PIC technology for specific purposes, like ASPICs for optical beamforming or matrix arithmetics. The developments for these specific applications, especially in the electronics and software layers, can also contribute to ecosystem around generic programmable photonic circuits.

This creates opportunities for new IP development, and even efforts towards standardization (like programming languages). Such efforts will automatically have a stimulating effect on the Maker community, which then could well generate a wealth of creative developments around photonic chips.

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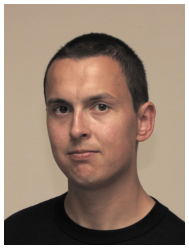

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