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Discussion on the Figures of Merit of Identified Traps Located in the Si Film: Surface versus Volume Trap Densities

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The aim of this work is a discussion on the figures of merit of identified traps located in the depletion zone (Si film) of advanced MOSFET devices. Two methodologies to estimate the volume trap densities are investigated, one using the relationship between the surface trap density and volume trap density and a second one based on the temperature evolution at fixed frequency of the generation-recombination plateau level associated to the same trap. By comparing the volume trap densities estimated using these two methods, the results are not agreeing with each other, suggesting that these methods can no longer be used with accuracy in multi-gate devices. Moreover, they may lead in certain cases to results physically not correct. Even about of the volume defects, the linear evolution between the plateau and the characteristic frequency of the generation-recombination contributions associated to the same trap give us the surface trap density without any additional assumption.

Introduction

Low frequency noise is a powerful non-destructive electrical diagnostic tools for predicting the semiconductor device quality (1,2). In particular low frequency noise spectroscopy may give information on processing-induced defects in scaled MOSFET structures, allowing the study of deep-level traps in the gate stack or in the semiconductor material, whatever are the device dimensions and architecture (3,4).
In this work, the estimation of the density of traps located in the depletion area (Si film) of devices processed using different state-of-the-art MOSFET architectures is assessed through different methodologies (5,6). The first method to estimate the volume traps density uses the relationship between the surface trap density and volume trap density. Another method for volume traps density extraction is related to the temperature evolution at fixed frequency of the generation-recombination plateau level associated with the same trap, it is shown that the obtained volume densities depend on the chosen fixed frequency of the generation-recombination level at which the estimation is made. The results obtained using these two methods are not in agreement with each other suggesting that they may be inappropriate to estimate the volume traps density in multi-gate devices. Contrary, from the linear behavior of the generation-recombination plateau versus the time constant (both associated to the same trap) the effective trap density can

be estimated, and this with no additional assumptions. Moreover, the importance of plotting this generation-recombination plateau versus the time constant is related to the fact that it may be considered as a supplementary confirmation of the trap identification that has been carried out.
In the second section, details on the investigated devices and the experimental set-up are given. In the third section, useful considerations and equations related to generation-recombination noise and the methodologies to estimate the density of traps located in the Si film are reviewed. Finally, in the fourth section, critical discussion on the different methods to estimate the volume and surface density of traps located in the Si film is given before wrapping up.

Experimental

The discussion on the figures of merit (surface and volume trap densities) is performed for identified traps located in the depletion region of different multi-gate transistors (e.g. FinFETs, UTBOX, GAA NW FETs) processed at imec (Leuven, Belgium) in fully depleted (FD) SOI (Silicon on Insulator) technologies. More technological details, e.g. the channel gate length and width ratio, the thickness of the non-intentionally doped Si film, the gate stack composition and the equivalent oxide thickness may be found in (7,8).
The low frequency noise measurements were made directly at wafer-level using a Lakeshore TTP4 prober. The home-made noise measurement set-up allows to bias the devices by choosing the polarization voltages using standard supply voltages. The current noise at the output of the devices is converted into a voltage noise using an I to V converter. A low noise voltage amplifier and a HP3562A spectral analyzer are used to obtain the noise power spectral density. The device input-referred noise power spectral density is calculated by dividing the measured output voltage noise power spectral density by the square of the measured voltage gain between the gate and the output. More details on the experimental set-up are provided in (9).
The Fermi level changes with the applied gate bias. Maximum generation recombination noise is created where the Fermi level and the traps level cross in the bandgap. Since the energy level of a point defect located in the depletion region is discrete and unique, and when the applied gate bias change, the Fermi level scans the same trap, but for increasing depth in the depletion zone (4,6). The characteristic time constant of the generation recombination noise associated with this trap will not change with gate bias variation but should only vary with temperature (3,4,6). A constant drain current polarization is necessary to keep a quasi-constant Fermi level over all the targeted temperature range. Performing low frequency noise spectroscopy measurements require to maintain a constant drain current polarization by adjusting the gate voltage at a fixed drain bias.
The methodology to estimate the noise parameters is described in (10).

Methodology - useful equations

In linear operation, the gate voltage spectral density of the generation – recombination due to traps located in the depletion region of the transistor is expressed as (3 ,6):

$$S_{Vg_Lor}(f)=\frac{q^2 N_{eff}\tau_i}{WLC_{ox}^2}\frac{1}{1+(2\pi f\tau_i)^2} \qquad [1]$$

where q is the absolute electron charge, N_{eff} is the surface trap density, W and L are the effective channel width and length, and C_{ox} is the gate capacitance per unit of area.
Each generation-recombination contribution is characterized by a plateau level A_i and a time constant τ_i (4,5,6):

$$A_i = \frac{q^2 N_{eff}}{WLC_{ox}^2}\tau_i = \frac{q^2 B W_d N_T}{WLC_{ox}^2}\tau_i \qquad [2]$$

where W_d is the silicon depletion depth (e.g. equal to the Si film thickness T_{Si} for UTBOX devices or $W_{Fin}/2$ for FinFETs, where W_{Fin} is the fin thickness) and N_T is the volume trap density.
From the slope of the linear behavior which should exist between A_i and τ_i (associated to the same trap) extracted for all temperatures where the identified trap is active, the surface trap density N_{eff} can be directly estimated.
The B coefficient which permits to estimate the volume trap density from the slope of the A_i and τ_i (associated to the same trap) parameters is defined as 1/3 [5,6]. This is the usual method to estimate the volume density of the identified traps in conventional planar MOSFET technologies (named Method 1).
A second method to estimate the volume trap density consists to use the maximum of the measured $S_{vg_Lor}(f_0,T)$ dependence with temperature (named Method 2). Indeed, the $S_{vg_Lor}(f_0,T)$ of generation-recombination noise associated to the same trap is proportional with $\tau_i(T)/\{1 + [2\pi f_0\tau_i(T)]^2\}$. For a given frequency f_0, if $2\pi f_0\tau_i(T) \gg 1$, $S_{Vg_Lor}(f_0,T) \propto \tau_i(T)]^{-1}$, and $S_{Vg_Lor}(f_0,T)$ increases with increasing temperature because τ_i decreases. If $2\pi f_0\tau_i(T) \ll 1$, then $S_{Vg_Lor}(f_0,T) \propto \tau_i(T)$ and $S_{Vg_Lor}(f_0,T)$ decreases with increasing temperature, as explained in detail in (6).

Results and discussion

A trap related to hydrogen V_2H was identified in standard <100> and rotated <110> UTBOX n-type transistors (11). From the slope of A_i and τ_i (Eq. 2) a surface trap density of $1.2\cdot10^9$ cm^{-2} was obtained for the standard device and of $8.1\cdot10^9$ cm^{-2} for the rotated one. Considering B as 1/3 (5,6), and taking into account that the Si film thickness (T_{Si}) is about 16 nm after device processing, this leads to a volume trap density N_T of $2.2\cdot10^{15}$ cm^{-3} for the standard device and of $1.5\cdot10^{16}$ cm^{-3} for the rotated one.
The evolution of the $S_{Vg_Lor}(f_0,T)$ with the temperature at fixed frequency is presented in Figure 1 for both devices. From the maximum of the bell-shaped behavior the volume trap density may be estimated. The results are summarized in Table 1.

TABLE I. Summary of estimated surface and volume V_2H traps densities for a UTBOX device.

Double gate device	N_{eff} (cm^{-2})	N_T (cm^{-3})		
		Method 1	Method 2	
standard channel UTBOX	$1.2\cdot10^9$	$2.2\cdot10^{15}$	f_0 = 4 Hz	$7\cdot10^{15}$
rotated channel UTBOX	$8.1\cdot10^9$	$1.5\cdot10^{16}$	f_0 = 5 Hz	$3\cdot10^{16}$
			f_0 = 8 Hz	$3.3\cdot10^{16}$
			f_0 = 12 Hz	$3.8\cdot10^{16}$

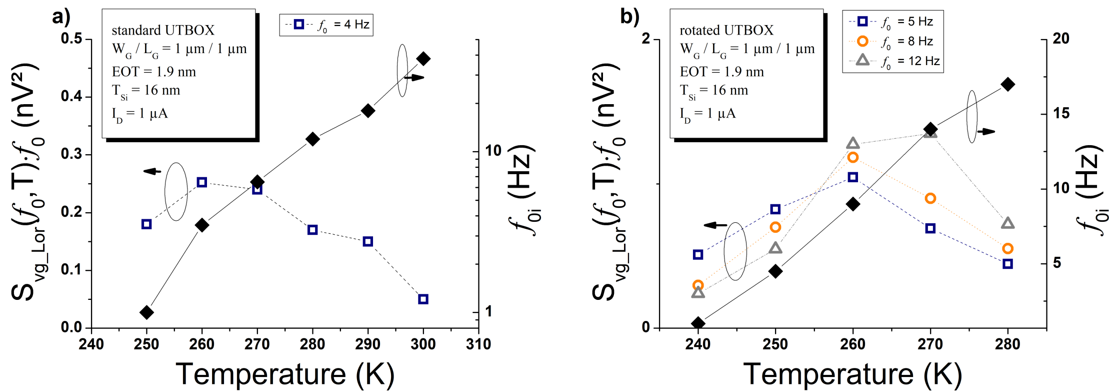

Figure 1. $S_{Vg_Lor}(f_0,T){\cdot}f_0$ versus temperature for the V_2H trap identified in (11); on the secondary Oy axis the characteristic frequency f_{0i} of the generation recombination noise is displayed in function of temperature.

As observed from Figure 1b, the maximum of the $S_{Vg_Lor}(f_0,T)$ behavior is dependent on the fixed frequency that was considered. Moreover, regarding the results of Table I, Method 2 provides higher values compared to Method 1 for both standards and rotated devices.
Concerning the triple-gate devices (FinFETs), an example of the evolution of the $S_{vg_Lor}(f_0,T){\cdot}f_0$ in a temperature range for a trap most likely related to the C_iC_s complex is given in Figure 2.

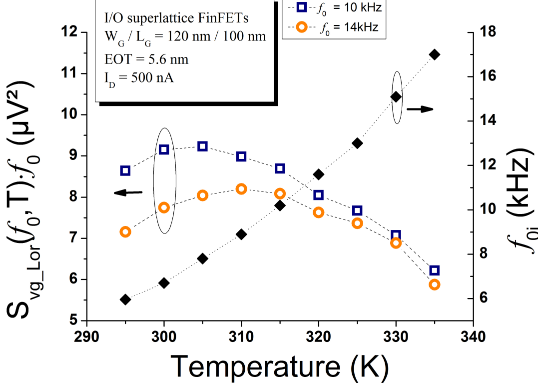

Figure 2. $S_{Vg_Lor}(f_0,T){\cdot}f_0$ versus temperature for the C_iC_s trap identified in (11); on the secondary Oy axis the characteristic frequency f_{0i} of the generation recombination noise is displayed in function of temperature

From the slope of A_i versus τ_i a surface trap density of this trap of $2.8{\cdot}10^{12}cm^{-2}$ was obtained (10).
Using Method 1 gives a volume trap density of about $1.7{\cdot}10^{19}$ cm^{-3}.
Using Method 2, volume trap densities of about $1.6{\cdot}10^{18}$ cm^{-3} at f_0 = 10 kHz and of about $1.4{\cdot}10^{18}$ cm^{-3} at f_0 = 14 kHz are obtained. It may be observed that the estimated volume trap density of this defect is about one decade lower than when using Method 1.
This trend was observed for all identified traps in the FinFET. The results are summarized in Table II.

Taking into account that the channels are non-intentionally doped (N_A of about 10^{15} - 10^{16} cm^{-3}), the obtained values of the volume trap densities in these multi-gate devices (FinFETs) may seems unphysical, whatever method (1 or 2) is employed. It should be noticed that when generation-recombination contributions of different traps have close characteristic time constants this may lead to an overestimation of the volume trap densities when using Method 2.

TABLE II. Summary of estimated surface and volume densities of identified traps for a FinFET device.

Triple gate device FinFET	N_{eff} (cm^{-2})	N_T (cm^{-3})		
		Method 1	Method 2	
V_2H	$6.2 \cdot 10^{10}$	$3.7 \cdot 10^{17}$	f_0 = 20 Hz	$9.4 \cdot 10^{16}$
$V_2(0/-)$	$2.2 \cdot 10^{11}$	$1.32 \cdot 10^{18}$	f_0 = 140 Hz	$3.5 \cdot 10^{17}$
V-P	$8.5 \cdot 10^{11}$	$5.1 \cdot 10^{18}$	f_0 = 1.2 kHz	$1.3 \cdot 10^{18}$
C_iC_s	$2.8 \cdot 10^{12}$	$1.7 \cdot 10^{19}$	f_0 = 10 kHz	$1.6 \cdot 10^{18}$
			f_0 = 14 kHz	$1.4 \cdot 10^{18}$

A last example presented is for a GAA NW FETs with an identified V_2H trap (12). The results of the estimated surface and volume traps densities are summarized in Table III. The same trend as for FinFETs is observed: Method 2 gives lower volume trap densities compared to Method 1. One should note that the considered "rectangular" gate-all-around devices having a fin height and fin width equals to 10 nm, the depletion zone is taken as 5 nm.

TABLE III. Summary of estimated surface and volume V_2H trap densities for a GAA NW FET device.

Gate all around device (GAA NW FET)	N_{eff} (cm^{-2})	N_T (cm^{-3})		
		Method 1	Method 2	
V_2H	$3 \cdot 10^{9}$	$1.8 \cdot 10^{16}$	f_0 = 80 Hz	$9 \cdot 10^{15}$

It can be observed that the estimation of volume traps densities using Method 1 and Method 2 does not match very well.

It is important to remind that Method 2 can be applied to estimate the density of the noisy centers for both "generation" and "trapping" noise, while the B = 1/3 approach is for "generation" noise (6). Furthermore, by comparing the volume trap densities obtained using Method 2 with the estimated values of the surface trap densities, one can estimate the experimental B coefficient, expressed as

$$B_{\exp} = \frac{N_{eff}}{N_T W_d} \quad [3]$$

The obtained values are summarized in Table IV. The fact that the obtained values of B_{exp} coefficient are lower (factor of 2 or 3) than the theoretical one (1/3) was already reported for UTBOX devices (11) and it was suggested that this trend may be linked to the fact that the theoretical B coefficient was theoretically evaluated for conventional planar transistor with one gate. However, for the GAA NW FET the B_{exp} is about 2 times higher than the theoretical value. In any case, the B_{exp} is lower than 1. Contrary, for FinFETs, the B_{exp} takes values higher than 1, which is unphysical.

TABLE IV. Determination of the experimental B (B_{exp}) (Note: are considered : for rotated UTBOX only the case of f_0 = 8 Hz, for the C_iC_s traps in FinFETs only the case of f_0 = 10 kHz)

device	standard UTBOX	rotated UTBOX	FinFET				GAA NW FET
trap	V_2H	V_2H	V_2H	$V_2(0/-)$	V-P	C_iC_s	V_2H
B_{exp}	0.1	0.15	1.32	1.25	1.3	3.5	0.66

This may suggests that for multi-gate devices, the methods permitting the calculation of the volume traps density developed for conventional planar transistors is no more accurate. The use of the volume trap density as figure of merit can be questioned.
As the surface trap density can be extracted directly from the slope of A_i versus τ_I (associated to the same trap) without any approximation, it is suggested here that it can be used as a figure of merit when comparing the density of traps located in the depletion region for transistors belonging to different technologies and architectures.

Conclusion

Disagreement between the obtained values of the volume traps densities when using different estimation methods is evidenced. Unphysical higher values of the estimated volume trap densities calculated using both methods is found for the FinFET case. In certain cases, unphysical values for the experimental B value are found. This suggests that the use of the volume density traps located in the depletion region as figure of merit for advanced multi-gates devices should be questioned. The effective trap densities estimation, without considering any additional hypothesis, could be used as a figure of merit even if the traps in the depletion region of the transistors are related to a volume phenomenon.

References

1. F. Scholz and J. Roach, *Solid-State Electron*., **35**, 447 (1992).
2. D.C. Murray, A. Evans, and J.C. Carter, *IEEE Trans Electron Devices*., **38**, 407 (1991).
3. V. Grassi, C.F. Colombo, and D.V. Camin, *IEEE Trans Electron Devices*., **48**, 2899 (2001).
4. E. Simoen, B. Cretu, W. Fang, M. Aoulaiche, J.-M. Routoure, R. Carin, S.D. dos Santos, J. Luo, C. Zhao, J.A. Antonio Martino, and Cor Claeys, *Phys. Status Solidi C*., **12**(3), 292 (2015).
5. L.D. Yau and C.-T. Sah, *IEEE Trans Electron Devices*., **(16)**, 170 (1969)
6. N. Lukyanchikova, edited by A. Balandin American Scientific, Riverside, CA 2002, p. 201 (2002).
7. S.D. dos Santos, B. Cretu, V. Strobel, J.-M. Routoure, R. Carin, J.A. Martino, M. Aoulaiche, M. Jurczak, E. Simoen, and C. Claeys, *Solid-State Electron*., **97**, 14 (2012).
8. G. Hellings, H. Mertens, A. Subirats, E. Simoen, T. Schram, L.-A. Ragnarsson, M. Simicic, S.-H. Chen, B. Parvais, D. Boudier, B. Cretu, J. Machillot, V. Peña, S. Sun, N. Yoshida, N. Kim, A. Mocuta, D. Linten, and N. Horiguchi. *in Tech. Dig. Symp. on VLSI Technology, The IEEE New York*, 85 (2018).
9. D. Boudier, B. Cretu, E. Simoen, R. Carin, A. Veloso, N. Collaert, and A. Thean. *Solid State Electron*., **128**, 102 (2017).

10. D. Boudier, B. Cretu, E. Simoen, G. Hellings, T. Schram, H. Mertens, and D. Linten, *Solid State Electron*., in press, (available online 2019).
11. B. Cretu, E. Simoen, J.-M. Routoure, R. Carin, M. Aoulaiche, and C. Claeys., *In Proceedings of ICNF'2015,* IEEE Xplore (2015)
12. A. Bordin, B. Cretu, R. Carin, E. Simoen, G. Hellings, D. Linten, C. Claeys. accepted to EuroSOI-ULIS'2020.