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A Deep Level Transient Spectroscopy Study of Hole Traps in Ge_xSe_{1-x}-based Layers for Ovonic Threshold Switching Selectors

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The deep levels in amorphous $Ge_{0.5}Se_{0.5}$ layers have been analyzed by Deep Level Transient Spectroscopy (DLTS). To that end, Metal-Insulator-Semiconductor (MIS) capacitors have been prepared by Physical Vapor Deposition of the films on p-type silicon substrates. A so-called quasi-constant capacitance procedure has been developed to account for the strong flat-band voltage shift of the capacitance-voltage characteristic with temperature. Applying this procedure to the as-deposited layers in the subthreshold regime reveals a dominant broad hole trap, with deep level parameters (trap concentration, hole capture cross section and activation energy) that strongly depend on the deposition conditions and the layer thickness. It is, finally, shown that the trap filling behavior does not follow the capture kinetics for simple point defects. Based on this observation, arguments are presented for an alternative analysis of the DLTS data.
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GeSe and related amorphous compounds are excellent candidates for the fabrication of Ovonic Threshold Switching (OTS) selectors in two-terminal high-density Storage Class Memories (SCM).[1–6] Important features for a two-terminal OTS selector in a crosspoint memory are a strong non-linearity in the current-voltage (I-V) characteristics, a low off current (I_{off}) and a high on current (I_{on}).[1] In the as-deposited state, the GeSe layer is amorphous and highly resistive (low I_{off}) but it can be transformed into a conductive state above a certain threshold voltage. One of the possible explanations for the low resistance is the formation of a conductive path or filament by alignment of defects across the thickness of the layer at sufficiently high forward bias, above a threshold voltage V_T. This leads to a steep turn on of the I-V characteristic when sweeping the applied voltage from zero to positive (forward sense), as in Fig. 1, followed by an ohmic regime. The selector can be turned off by a voltage sweep from high to low bias voltage. Overall, it is believed that defects play an important role in the switching of a Ge_xSe_{1-x} OTS selector.[7,8] Good thermal stability of the layers is also of crucial importance[1] and is closely linked to the defectiveness,[9] which also defines the carrier transport in both off and on state.

In such OTS materials, the current in the off-state cannot be described in terms of the classical drift-diffusion theory, assuming a well-defined band gap. Instead, it has been shown that carriers are localized in the deep potential well of attractive traps, where they move by field-assisted hopping.[10–12] Characterization of the trap states is thus key to the understanding of the transport and the stability/drift of the layers.

One of the standard methods to study deep level traps in semiconductors is Deep Level Transient Spectroscopy (DLTS),[13–15] which has also been applied in the past to amorphous silicon for example.[16–21] The aim of the present paper is to apply this method in combination with capacitance-voltage (C-V) measurements to the study of Physical Vapor Deposited Ge_xSe_{1-x} layers on p-type silicon substrates in the high-resistive state. As will be shown, the observed hole traps around activation energies in the range of 0.2 eV to 0.5 eV exhibit a broad distribution of states and non-exponential trap filling kinetics. The trap parameters are strongly affected by the deposition conditions and by the sample history. This will be discussed in view of the transport mechanisms in the layer.

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Processing and Measurement Details

For DLTS, Metal-Insulator-Semiconductor (MIS) structures have been prepared by Physical Vapor Deposition (PVD) of a 20 or 50 nm thick Ge_xSe_{1-x} layer with x ~ 0.5 on 5–10 Ωcm p-type Czochralski silicon substrates. Layers were grown in two different types of reactors (henceforth denoted as type A and B). Deposition of a circular Al gate, followed by an anneal in N_2 at 250 °C completes the fabrication of the devices, with a structure obtained as schematically represented in Fig. 2. A back-side ohmic contact is formed by an Al layer. The diameter of the gate contact is 100 μm. As the MIS capacitors may suffer degradation by storage in air, sample preparation is done as close as possible to the multi-frequency C-V and DLTS characterization.

According to the band diagram of Fig. 3, a barrier for holes is expected between p-Si and GeSe, which could result in an MIS behavior, which is suitable for DLTS.[14,21–24]

As shown in Fig. 4, a C-V behavior typical for a p-type semiconductor is obtained for as-deposited, low-leakage structures, including saturation at negative gate voltage (V_G) in accumulation and depletion for more positive V_G. Little frequency dispersion in accumulation and small hysteresis is found in the temperature (T) range used in DLTS (50 K–350 K). During the C-V sweep, care is taken to limit the maximum absolute V_G to values below V_T, so that the layer is preserved in its pristine high resistive state.

It should be noted that the value of the accumulation capacitance in Fig. 4 is smaller than expected from the layer thickness and the dielectric constant mentioned in Fig. 3. This can partly be explained by the presence of a thin native oxide layer on the silicon substrate (see below), resulting in a smaller effective ε value of around 10. In addition, the dielectric constant of the a-GeSe layer also depends on the deposition conditions (reactor type) and post-deposition thermal treatments.

A second important observation in Fig. 4 is the significant flat-band voltage (V_{FB}) shift towards negative gate voltage (V_G) upon cooling from room temperature (300 K) to 125 K (Fig. 4). This implies that at lower T more positive (or less negative) charges are present in the GeSe "dielectric" when shifting the Fermi level at the Si/GeSe interface towards the silicon valence band upon cooling. This is a natural consequence of the carrier "freeze-out" effect on the deep levels in the GeSe layer (or at the interface with silicon). In other words, at low T when E_F moves closer to the valence band and below a deep level E_T, the charge state of the latter becomes more positive (or less negative for acceptors).

In standard capacitance DLTS, the traps are filled using a periodic bias pulse from a fixed reverse bias V_r in depletion to a

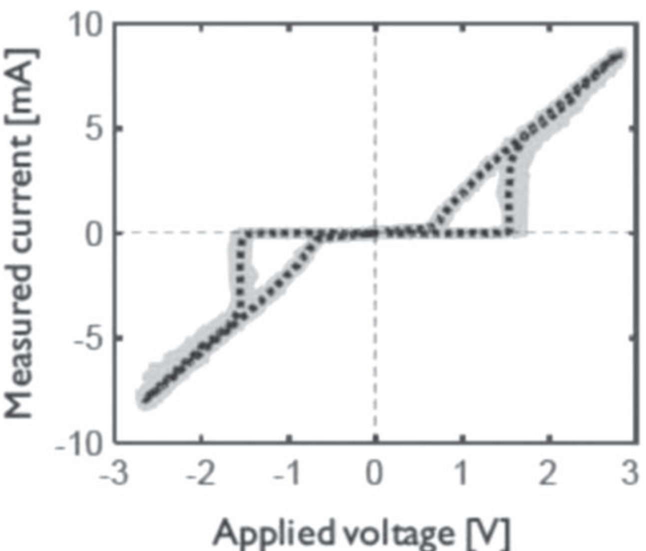

Figure 1. I-V of a GeSe Metal-Insulator-Metal (MIM) structure.

fixed pulse bias V_p in accumulation. The capacitance transient, resulting from trapped charge thermal emission is measured at V_r after the pulse by a small-amplitude 1 MHz AC signal on top of the reverse bias. However, the T-dependent shift in V_{FB} should be accounted for when performing T-scan DLTS on such capacitors if a fixed bias pulse from a constant depletion bias on the gate (V_r) to a certain value V_p in accumulation is performed. The V_r defines the depletion width W from which the traps are monitored, while V_p selects the spatial window and the type of traps (silicon bulk traps; GeSe/Si interface traps or bulk GeSe traps).[23,24] Since W(V_r) is in first instance inversely proportional to the capacitance corresponding with V_r, it is clear that the significant capacitance shift with temperature at fixed V_r results in a significant change in the traps contributing to the spectrum and their spatial origin. Especially when a continuous distribution of trap levels is present in the structure (i.e., due to interface or border traps in the gate dielectric) this procedure will lead to inference of an erroneous density-of-states (DOS) as a function of T (or as a function of energy).

In order to solve this issue, one can perform so-called Constant-Capacitance (CC) DLTS,[22] keeping the depletion capacitance constant as a function of temperature by the implementation of a feedback loop in the reverse gate bias and measuring the voltage transient resulting from carrier thermal emission following a filling pulse. However, due to the large shift of V_{FB} (up to 1 V from 125 K to 300 K), it is difficult to limit the bias window of the feedback loop always below the V_T, so that an alternative solution has been developed, which we call quasi-CC DLTS. This is achieved by first determining the evolution of V_{FB}

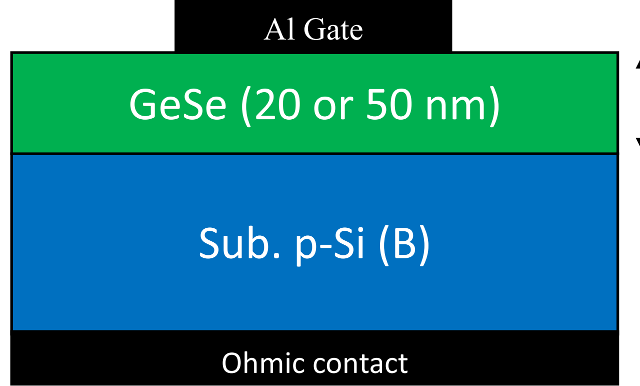

Figure 2. Schematic representation of the sample structure for DLTS measurements.

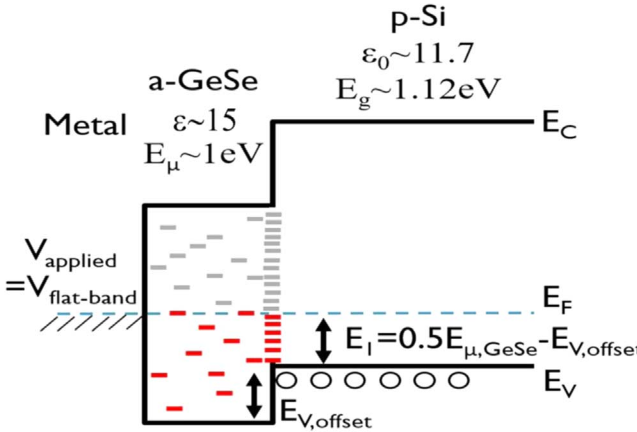

Figure 3. Band diagram of a-GeSe on a p-type silicon substrate at flat-band gate bias.

as a function of temperature from 1 MHz C-V data (operation frequency of the DLTS set-up). A routine in Python language has been written to keep the V_r-V_{FB} difference fixed with temperature, resulting in a constant depletion capacitance over the whole T-range from 50 K to 350 K. It is "quasi" CC DLTS, since the measured signal is still based on a capacitance and not on a reverse-gate-bias transient.

As mentioned above, the bias pulse V_r-V_p selects the type of traps that contribute predominantly to the DLTS signal.[23,24] For a bias pulse in deep depletion, with $V_p > V_{FB}$, one will mainly fill traps in the silicon depletion region or at the GeSe/Si interface. For a $V_p < V_{FB}$, one can also fill the traps in the GeSe layer with holes, as schematically represented by Fig. 5. At the same time, care is taken not to apply a too negative (forward) pulse bias, surpassing the threshold voltage, as this will modify the resistance state and the trap distribution and, hence, the DLT-spectrum.

The measurements have been performed for different rate windows (i.e., lock-in time constant T_w) and filling pulse times (T_p). In the latter case, one hopes to characterize the hole filling kinetics of the deep levels in the GeSe layer, which should reveal information on the hole capture cross section (σ_p).[14] The activation energy of the traps can be derived from an Arrhenius plot, representing the hole emission rate (or time constant) vs 1/kT (k Boltzmann's constant). It should also be remarked that in our system, a full trap characterization typically takes a couple of days, implying that the sample is subjected to many tens of thousands of cycling pulses, which can surpass the endurance limit of the layers. While excellent endurance has been reported extending to 10^8 cycles for 3 V/100 ns pulses,[2] it has also been shown that for thinner layers, i.e., 20 nm vs 50 nm, this parameter is reduced. In addition, the endurance has been measured at room temperature; in DLTS, on the other hand, temperature is varied from low to high during the measurement. This implies that charge trapped in deep levels cannot easily be released by thermal emission at low T, so that

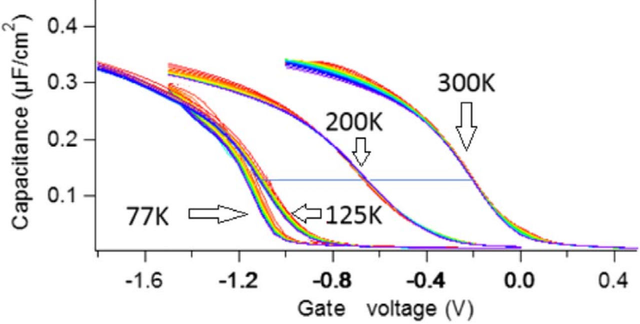

Figure 4. Capacitance-voltage (C-V) characteristic at different frequencies (10 kHz–1 MHz, from red to blue) and for different temperatures T for a capacitor with a 20 nm thick GeSe layer.

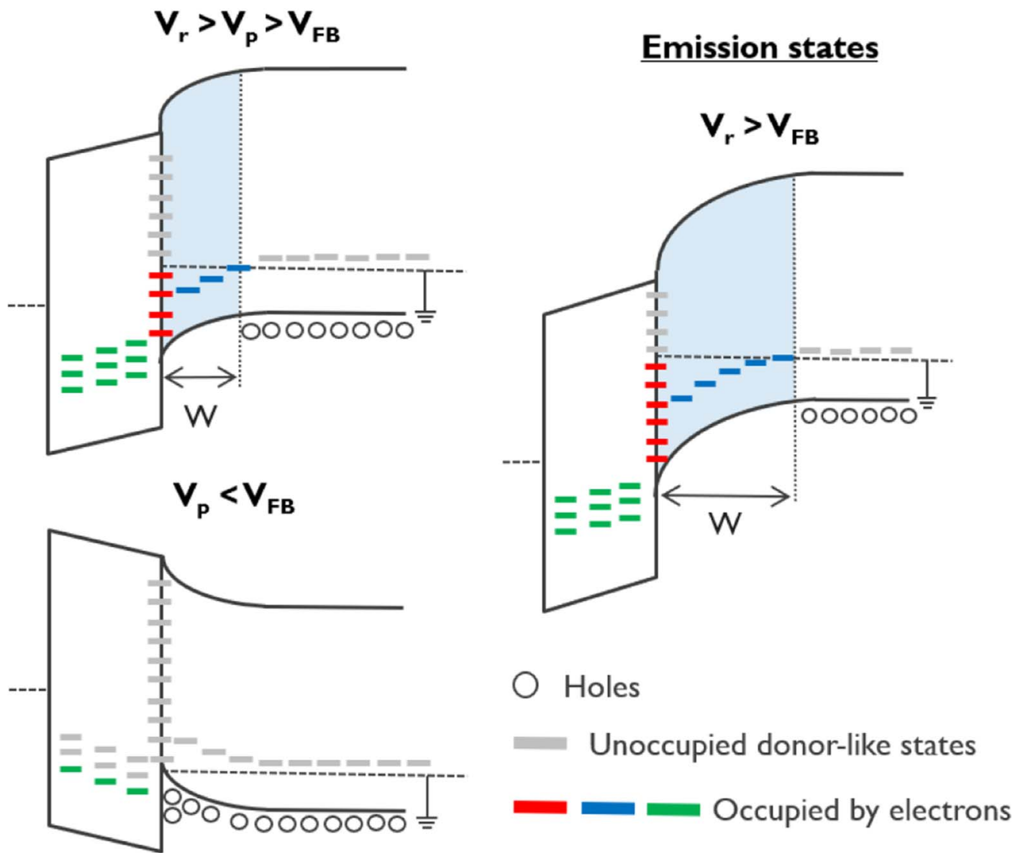

Figure 5. Schematic representation of the hole capture and hole emission in a GeSe MIS capacitor for different gate bias.

more pronounced and permanent degradation of the V_T can occur during cycling, even if small pulse heights and short pulses are being used.

The results shown here are representative for non-degraded, as-grown layers. Moreover, isothermal measurements have been performed, varying the T_w at constant T_p or at fixed T_w for different T_p. In the latter case, the hole filling kinetics of the deep levels is studied.

Results and Discussion

Figure 6 compares the standard capacitance-DLT-spectra for a reference MOS capacitor and a 20 nm thick $Ge_{0.5}Se_{0.5}$ counterpart for the same measurement conditions, i.e., a fixed V_r and V_p without compensating for the V_{FB} shift with temperature. The reference device is formed by a 10 nm HfO_2 gate dielectric on p-type Si without GeSe. A clear difference between the two spectra is observed: while for the reference device a small but broad peak starting from 200 K is observed, a clear hole trap peaking at 180 K is found for the GeSe capacitor. It should be mentioned that negative peaks correspond here with majority carrier (hole) traps.

From a standard Arrhenius plot of the sample D4, an activation energy with respect to the top of the valence band E_V in the range of 0.35 eV to 0.385 eV has been derived, while from the intercept, a σ_p in the range of 1×10^{-16} to 3×10^{-16} cm^2 was found. The minor hole trap distribution for the reference sample (D5) could result from the DOS at the HfO_2/silicon interface, while the pronounced peak in the D4 capacitor clearly corresponds with defects in the GeSe layer. Note also the discontinuity of the GeSe peak at around 120 K, which is a consequence of the strong shift in V_{FB} with temperature, reported in Fig. 4. In fact, between 77 K and 125 K, V_{FB} remains approximately constant, while a strong shift is observed from 125 K

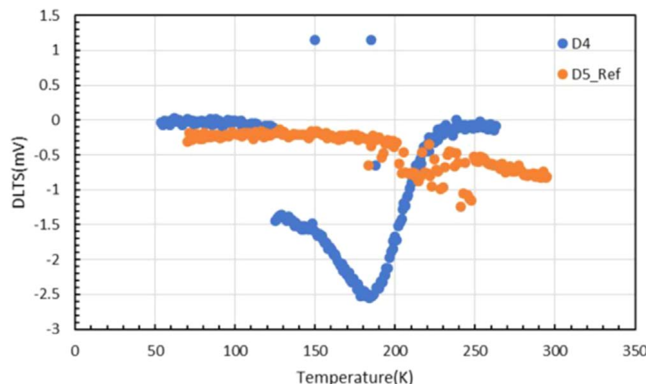

Figure 6. DLT-spectrum for a reference capacitor with 10 nm HfO_2 gate dielectric (D5) and a capacitor with 20 nm $Ge_{0.5}Se_{0.5}$ (D4). The spectra have been recorded with a $V_r = 0.4$ V and a $V_p = -1$ V.

to 200 K and 300 K. This means that for a fixed pulse from 0.4 V to −1 V, mainly traps in the silicon substrate will be filled with holes, as the pulse is mainly in the depletion part of the C-V characteristic of Fig. 4. Above 125 K, also traps in the a-GeSe layer and the interface with silicon contribute to the signal. As a result, both the steady-state capacitance and the DLTS amplitude exhibit a pronounced and rather abrupt change around 125 K.

In order to avoid such jumps in the spectra, quasi-CC DLTS has been applied in the spectra reported below. In the case of the reference device, it can be remarked that the flat-band voltage shift between 300 K and 77 K in Fig. 7 is much more modest, indicating much less traps present in the structure.

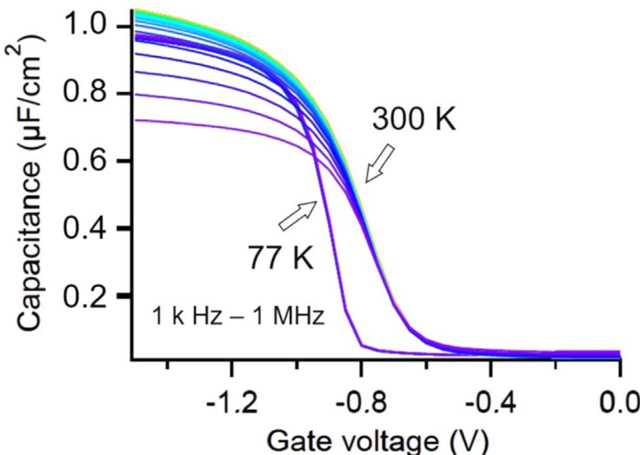

Figure 7. C-V plot at different frequencies (1 kHz–1 MHz, from red to blue) for a reference capacitor (10 nm HfO_2) on p-type Si measured at 77 K and 300 K.

Figures 8 and 9 represent the quasi-CC DLTS spectra for GeSe layers deposited in the same reactor A but with a thickness of 20 and 50 nm, respectively. Curves are shown for equal V_r at room temperature and different V_p, ranging from a value in depletion to accumulation. It is clear from Fig. 8 that for a depletion pulse from 0.5 V to 0.2 V, no hole traps are observed above the detection limit. This is in line with the expectation that no measurable deep levels are present in the depletion region of the p-type silicon substrate.

On the other hand, for a bias pulse going more into accumulation, filling both p-Si/GeSe interface and GeSe bulk (border) traps, one observes a clear peak, increasing in amplitude for increasing magnitude of V_p. However, three differences are observed between Figs. 8 and 9: one, the peak maximum position is different, implying a different trap level E_T with respect to the top of the valence band E_V. Second, the amplitude of the peak is significantly higher for the 50 nm layer compared with the thinner one. This suggests a much higher trap concentration (or DOS) in the former case, i.e., a much larger concentration of hole traps is filled after a pulse duration of 1 ms. Third, while in the 20 nm film the peak position is not strongly dependent on V_p (Fig. 8), a shift to higher T with increasing magnitude of V_p is observed in Fig. 9 for the thicker GeSe layer. This suggests an increase in the trap level energy with V_p. In all

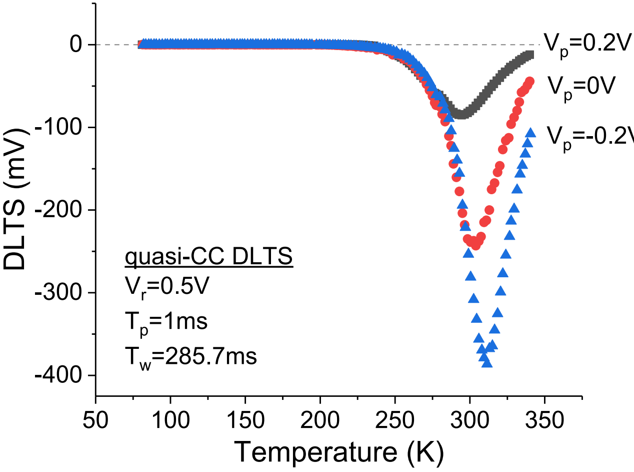

Figure 9. DLT-spectra at equal reverse bias (V_r = 0.5 V) at room temperature and different pulse bias V_p for a 50 nm GeSe capacitor deposited in reactor A. The lock-in time constant applied is T_w = 285.7 ms and the pulse time T_p = 1 ms.

cases, DLTS peaks are found that are broader than for a single-energy-level point defect, in line with an expected continuous DOS in amorphous GeSe. Evidently, the hole trap parameters, i.e., the trap concentration (peak height) and the activation energy/capture cross section (peak maximum position) depend strongly on the thickness of the layer. It should be remarked that for practical OTS applications, 20 nm is more relevant.[1–5]

Comparing the results obtained on two layers deposited under different conditions, cf Figs. 8 and 10 demonstrates that the defect parameters also strongly depend on the reactor type—note that measurements on different capacitors of the same sample growth yield quite similar results, indicating that what is reported here is typical for each type of as-deposited layer. Again, the hole trap peak in DLTS changes both in amplitude (the trap concentration) and temperature position between type A and type B 20 nm thick layers. In addition, in Fig. 10, a clear shoulder is present at the low temperature side of the main peak, becoming more pronounced for a V_p going more into accumulation (more negative values). This is a typical behavior for interface states, while the energy position corresponds with the donor states of silicon dangling bonds (P_b centers)—here at the p-Si/GeSe interface.[25–31] However, it has been shown by Transmission Electron Microscopy (TEM) that there

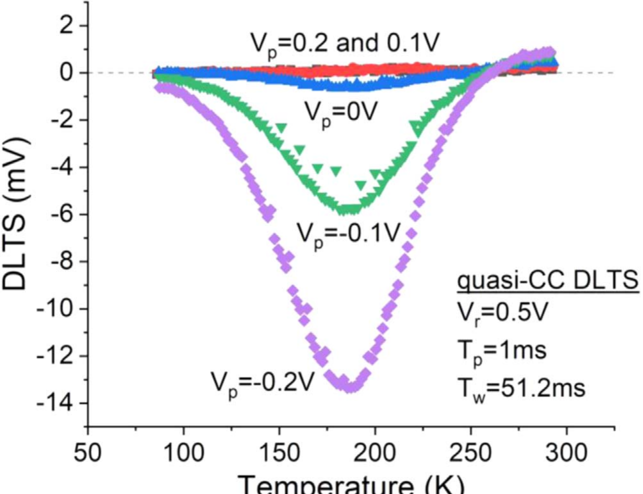

Figure 8. DLT-spectra at equal reverse bias (V_r = 0.5 V) at room temperature and different pulse bias V_p for a 20 nm GeSe capacitor deposited in reactor A. Experimental parameters used are a lock-in time constant T_w = 51.2 ms and a pulse time T_p = 1 ms.

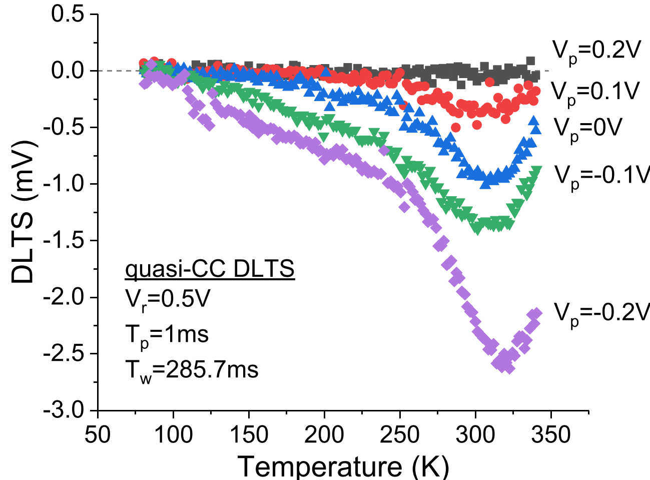

Figure 10. DLT-spectra at the same reverse bias (V_r = 0.5 V) at room temperature and different pulse bias V_p for a 20 nm GeSe capacitor deposited in reactor B. The lock-in time constant T_w = 285.7 ms and the pulse time T_p = 1 ms.

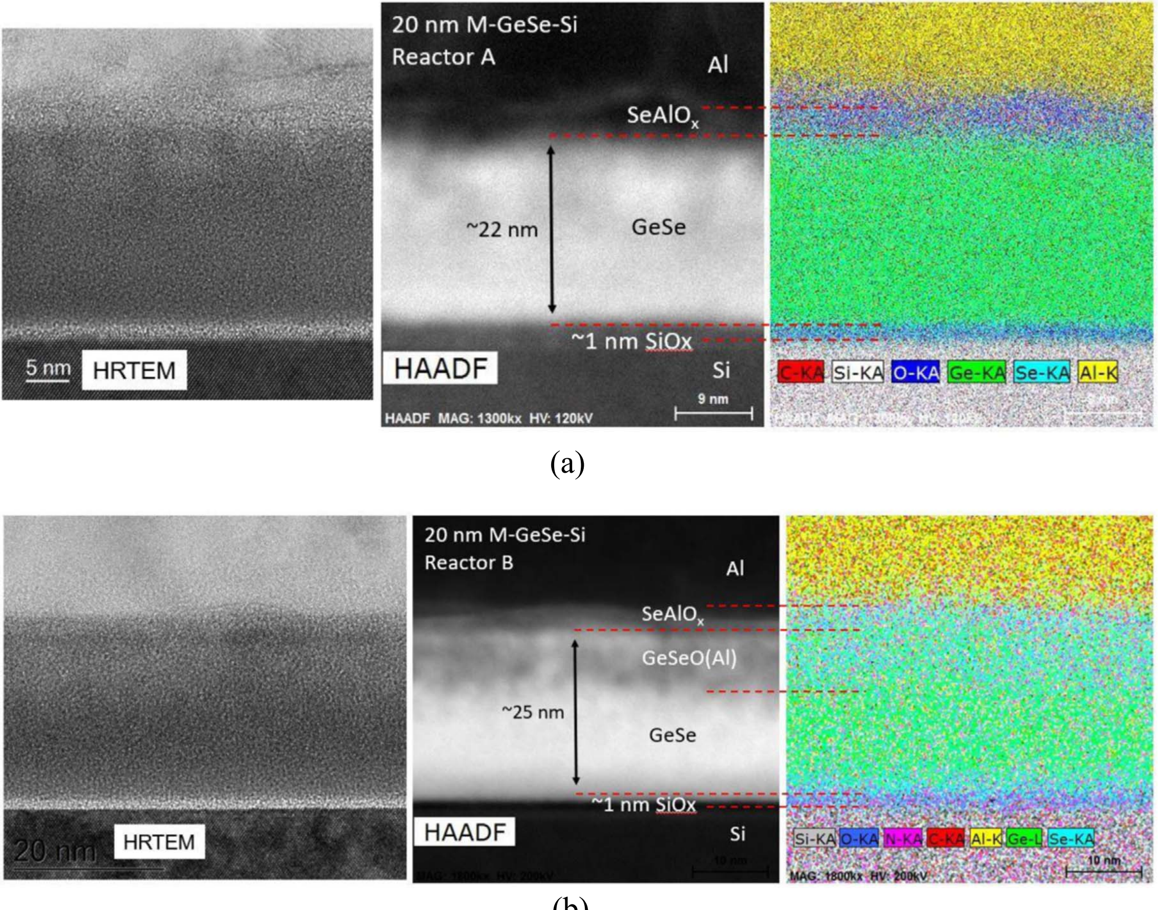

Figure 11. High-Resolution TEM cross-section (left), high-angle annular dark-field imaging (HAADF in the middle) and elemental analysis map (right) of the 20 nm GeSe-on-p-Si capacitor deposited in reactor A (a) and reactor B (b).

is a thin (native) SiO_2 layer present between the p-Si interface and the amorphous GeSe layer (Fig. 11), explaining the presence of P_b-type silicon DB centers in DLTS. The higher oxygen concentration of the type B film noticed in Fig. 11 could also explain the different behavior noted in the spectra of Figs. 8 and 10.

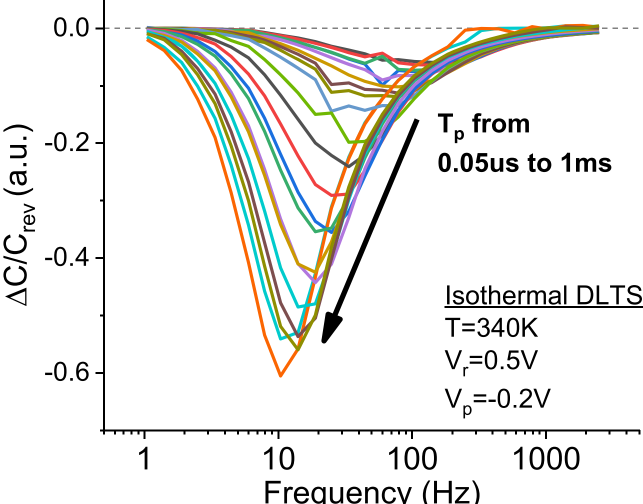

Figure 12. Frequency-scan DLTS at T = 340 K for a 50 nm GeSe layer deposited in reactor A, corresponding with different T_p between 0.05 μs and 1 ms. The bias pulse was from 0.5 V to −0.2 V.

A final experimental observation is demonstrated in Fig. 12, showing the evolution of the hole trap filling as a function of the bias pulse width T_p in the range of 0.05 μs up to the maximum of 1 ms for the 50 nm GeSe layer. In Fig. 12, frequency scans at a fixed temperature of 340 K are represented and for a pulse from 0.5 V to −0.2 V. One can see first of all that the peak amplitude increases with T_p, as expected. However, less usual is the shift of the peak position towards lower frequencies (longer time constants) for increasing T_p. Although this would suggest that in the broad DOS, hole traps with a higher activation energy are filled for longer T_p, the Arrhenius plot made later shows a consistent comparable activation

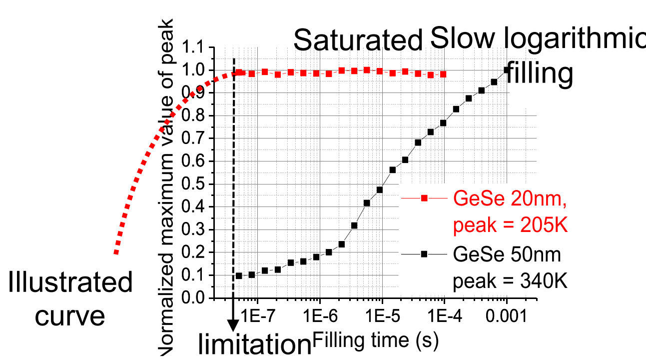

Figure 13. Hole filling kinetics for a 20 and a 50 nm thick GeSe MIS capacitor deposited in reactor A, taken with a bias pulse extending from 0.5 V to −0.2 V.

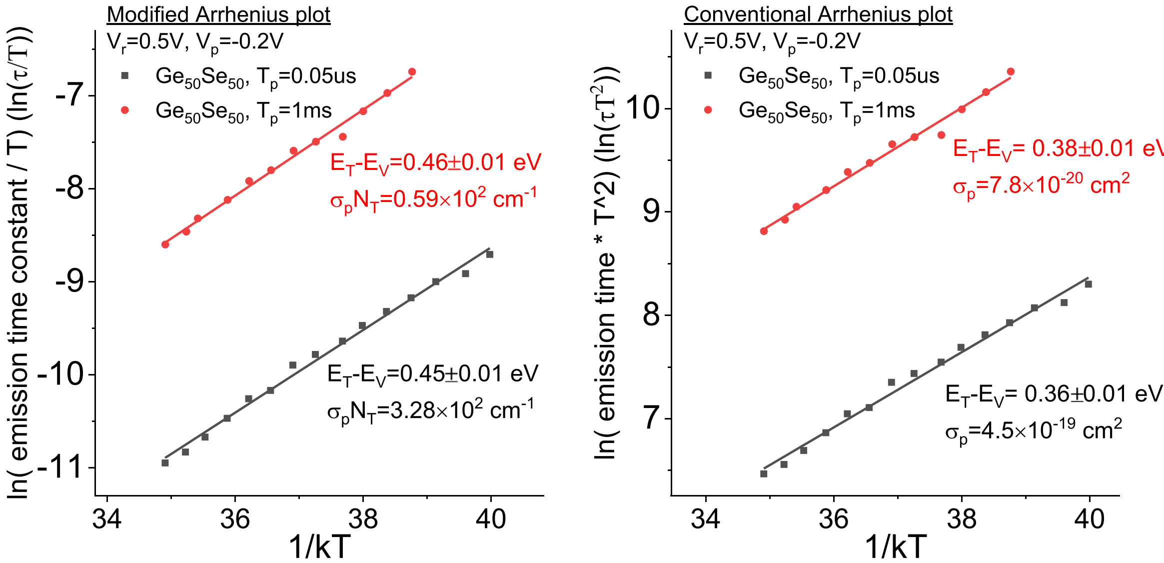

Figure 14. Arrhenius plot of a 50 nm GeSe layer deposited in reactor A, obtained for a $T_p = 0.05\ \mu s$ (black symbols) and 1 ms (red symbols).

energy and an alternative explanation would be needed. At the same time, no saturation of the peak amplitude is found in this case up to a T_p of 1 ms.

The evolution of the peak amplitude vs T_p is shown more explicitly in Fig. 13. The exposed slow filling is not typical for a point defect[13,14] but is rather similar to the logarithmic filling of so-called border traps in an MIS structure.[14,21,32–36] In that case, trap filling occurs through tunneling across the barrier at the GeSe/Si interface (see diagram in Fig. 3) leading to a logarithmic increase of the tunneling front (depth in the GeSe) and a likewise increase in the DLTS amplitude. However, there are a few arguments against this interpretation: first of all, the anticipated energy barrier at the GeSe/Si interface is rather low, on the order of 0.3 eV (Fig. 3), implying that holes can fairly easily be emitted across the barrier by thermionic emission, rather than by tunneling. This would not lead at first sight to slow capture. Second, as shown by the data in Fig. 13 for the type A 20 nm GeSe layer, trap filling by hole capture is saturated already for the shortest pulses applied. This again illustrates the contrasting behavior of the deep levels in the different layers. More importantly, it suggests that interpretation in the frame of the standard DLTS theory may not be applicable for an amorphous material like GeSe, because of the different charge transport mechanisms prevailing in this case.

As will be shown elsewhere,[37] a consistent interpretation of the DLTS data could be achieved by considering hopping transport in the subthreshold regime based on the theory by Ielmini et al.[10–12] This results in modified expressions for the capture and the emission time constant and an alternative Arrhenius analysis. In stead of the standard τT^2 analysis vs 1/kT, it is better to monitor τ/T vs 1/kT, with τ the hole emission time constant. Figure 14 represents such a modified Arrhenius plot for two filling time constants used in Fig. 12. The values are about 0.1 eV higher than in the standard analysis. More importantly, from the intercept of the linear fit, one no longer derives the hole capture cross section but rather the product of the trap density N_T and σ_p.[37] Further dedicated analysis is needed to separate these two parameters. Figure 14 illustrates the general trend that for longer T_p, the concentration of additionally filled traps reduces (assuming a constant σ_p), in agreement with the hopping transport model.[10–12]

It should, finally, be remarked that the observed E_T values in the range of 0.2 eV to 0.5 eV with respect to the valence band maximum in Ge_xSe_{1-x} are supported by the density of states extracted from ab initio Density Functional Theory (DFT) calculations for non-tetrahedrally coordinated Ge or Ge–Ge dimers.[9]

Summary

In conclusion, it can be stated that the feasibility (and reproducibility) of DLTS on Ge_xSe_{1-x} ($x \sim 0.5$) MIS capacitors on p-type silicon substrates has been established. In all layers studied, a prominent DOS of hole trap levels in the Ge_xSe_{1-x} layers has been found, whereby the deep-level parameters strongly depend on the deposition conditions and thickness of the Ge_xSe_{1-x} film. Changing the measurement conditions also indicates that the hole traps in Ge_xSe_{1-x} do not behave like simple point defects. Arguments have been provided indicating that a meaningful extraction of the trap parameters should account for the specific transport mechanisms in the amorphous Ge_xSe_{1-x} material.

Acknowledgments

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