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Graphene and its derivatives for electronic applications

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Chapter 1

Introduction

Graphene was first isolated in 2004 by a group of physicists at Manchester University [1] whose objective was to investigate the electronic properties of graphite films as thin as possible. The existance of graphene sheets stacked into 3D graphite was already known since the early days of x-ray crystallography. Graphene band structure, meant as a monolayer of graphite, was first explored around 1947 when P. Wallace was studying the electronic properties of bulk graphite [2], but the thought of a purely 2D structure was not reality yet. The first experimental research with very thin carbon sheets were practiced by Brodie in 1859 [3], who made graphite react with strong acids in order to obtain what today is known as graphite oxide. In the following century many others developed different synthetic strategies to obtain graphite and graphene oxide flakes, in most of the cases involving the reaction of graphite with strong oxidizing acids. Some of these synthetic routes to graphene will be described in more detail in section 1.2.5. However, graphene oxide structure is chemically very different from that

of graphene, because of the introduction of many oxygen-containing functionalities which affects the electrical, optical, thermal and mechanical properties of the material. Of particular interest, considering the graphene production, are also graphite intercalation compounds (GICs) [4], synthesis of which was first reported by Schäffault in 1841.

What makes graphene so attractive with respect to bulk graphite and its derivatives?

The answer is the 2D nature of a graphene monolayer. Optical and electronic properties are different because of the confinement of electrons and the absence of interlayer interactions. Other properties are a consequence of the extremely high surface area (for monolayer graphene ~ 2560 m^2/g) and the increased chemical reactivity. Finally, graphene is the first example of a 2D atomic crystal, whose existance was considered to be impossible for a long time since it was thought that both finite temperature and quantum fluctuations would preclude the existance of a perfect 2D structure [5].

1.1 Graphene structure and properties

Graphene is a one-atom-thick sheet of sp^2 hybridized carbon atoms organized in a honeycomb planar crystal lattice. This means that each graphene atom can form three σ bonds oriented towards the neighboring atoms by overlapping their sp^2 orbitals. The fourth valence electron is located in the 2p$_z$ orbital which is oriented perpendicular to the graphene sheet and leads to delocalization of electrones involved in the π bonds with adjacent atoms. The intralayer carbon-to-carbon

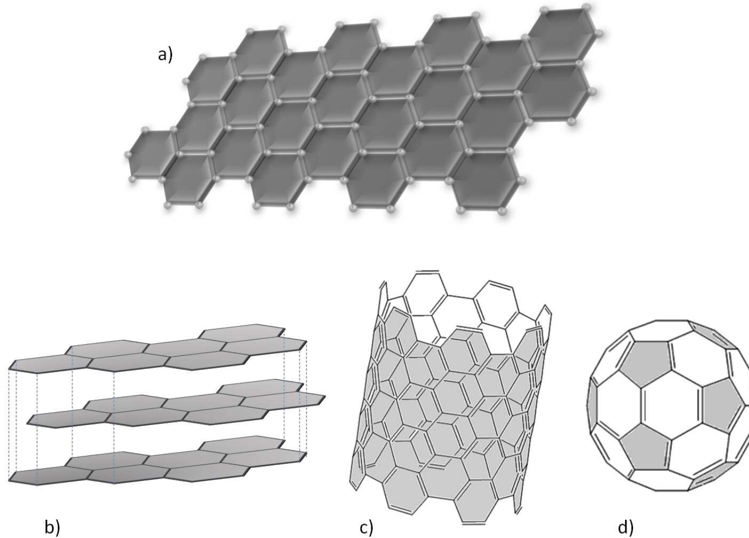


Figure 1.1: Carbon allotropes: a) graphene, b) graphite, c) carbon nanotube and d) fullerene.

distance is 1.42 Å. Among carbon-based systems, graphene plays an important role since it could be seen as a building block of other kind of carbon allotropes (see figure 1.1). In fact, graphite is a layered material formed by stacks of graphene sheets, which are held together by weak Van der Waals forces with an interlayer distance of 0.34 nm. The weak interaction between graphene layers gives graphite its writing ability and lubricating properties. More interestingly, considering the anisotropy of its chemical bonds, graphite is a good electrical and thermal conductor within the layers (due to the in-plane metallic bonding) and a poor electrical and thermal conductor perpendicular to the layers [6]. Carbon nanontubes could be considered as rolled graphene and

their remarkable electronic properties are a direct consequence of the particular band structure of graphene. Finally, fullerenes can be ideally obtained by wrapping graphene sheets and inserting some carbon pentagones to allow to the spherical shape.

The in plane conduction of electrons in graphene is dominated by π (valence) and $\pi*$(conduction) bands which are formed by the hybridization of the perpendicular p_z orbitals. Figure 1.2 (left) shows schematic of the electronic π and π^* band structure of an ideal graphene monolayer in the vicinity of the K-point, as calculated from a tight binding approach. The two cones are a direct consequence of the presence of electrones and holes (collectively called charge carriers), and corresponds to valence (lower) and conduction (upper) band. For undoped graphene these two bands intersect at a single point called the Dirac point (K-point). This configuration makes graphene a semimetal (or a zero-band gap semiconductor) and it represents one of the main issues to be considered for graphene electronic applications, as it will be explained in more detail in section 1.3.1.

A schematic of graphene lattice is shown in figure 1.2 (right). The unit cell consists of two adjacent carbon atoms as represented by the dashed lines, and is spanned by the following two lattice vectors:

$$\overline{\mathbf{a_1}} = (^{3a}/_{2}, \frac{\sqrt{3}a}{2}), \overline{\mathbf{a_2}} = (^{3a}/_{2}, -\frac{\sqrt{3}a}{2})$$

where $a = 0.142$ nm corresponds to carbon bond length.

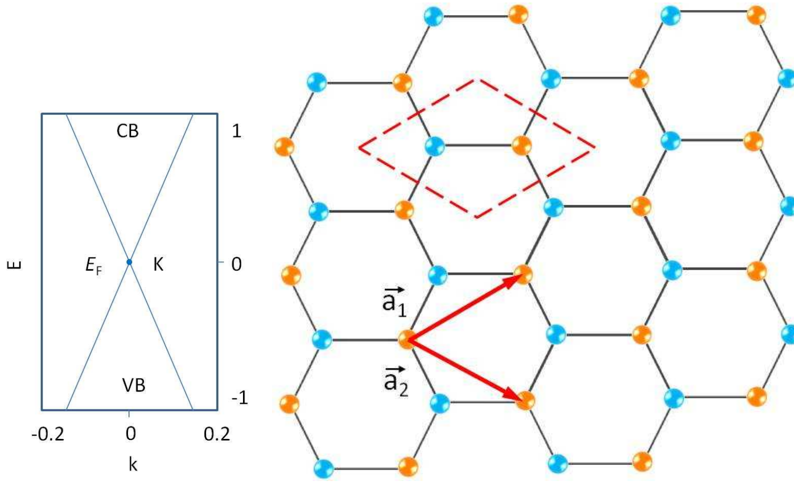


Figure 1.2: (Left) graphene band structure; (right) graphene lattice, the unit cell is represented by dotted lines and is composed by two adjacent carbon atoms. The two lattice vectors are indicated as $\bar{a}_1$ and $\bar{a}_2$.

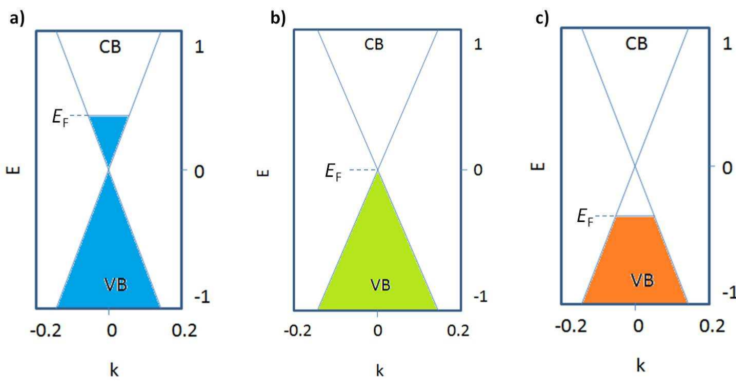


Figure 1.3: Valence and conductance bands in monolayer graphene and its respective Fermi energy levels: a) n-doped graphene; b) undoped graphene ; c) p-doped graphene.

Electrical properties

As shown in figure 1.3 b), the Fermi level $E_{\mathrm{F}}$is situated at the connection points of the two cones in undoped graphene. Since the density of states of graphene is zero at that point, the electrical conductivity reaches its minimum and is of the order of the conductance quantum $\sigma{\sim}e^2/h$ [7]. A few-layer graphene sheet (<3 nm) is reported to have sheet resistance R_s of around 400 Ω/sq [1]. By applying an external electric field or a mechanical deformation, or by doping or adsorbing molecules one can change the position of the Fermi level in order to obtain either n-doped (figure 1.3 a)) or p-doped (figure 1.3 c)) graphene. For that reason, the charge transport in graphene exhibits ambipolarity. Carriers can be tuned continuously between holes and electrons by applying the required gate bias. As shown in figure 1.4, under negative gate bias, the Fermi level shifts below the Dirac point, introducing a significant population of holes into the valence band. Under a positive gate bias, the Fermi level rises above the Dirac point, promoting a significant population of electrons into the conduction band [8].

Carrier mobility can be determined from the field effect measurements as $\mu = \sigma(V_g)/en(V_g)$ and it can vary between few hundreds to several thousands cm^2/V even at room temperature, depending mostly on the sample quality. Here, n is the charge density and e is the elementary charge. Despite the fact that a graphene crystal is theoretically free of structural defects, different phenomena such as surface charges traps and electron-hole puddles formation [9], interfacial phonons [10] or graphene rippling [11], could promote the scattering of charge carriers in practical devices. Moreover, graphene mobility is temperature-independent between 10 and 100 K. Although the ex-

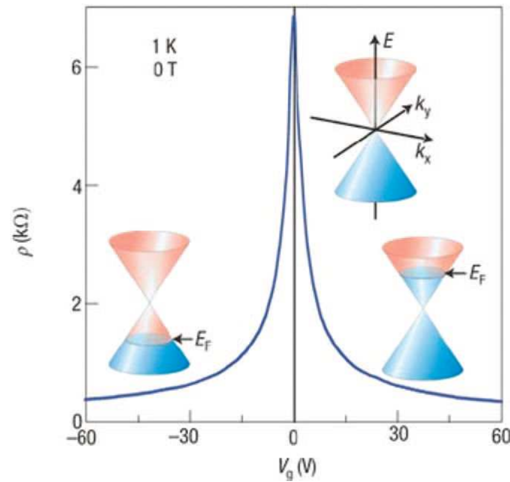


Figure 1.4: Band structure and ambipolar field effect in graphene. Under gate bias, the Fermi level moves away from the Dirac point resulting in a significant number of free carriers. At zero value of applied gate bias the conductivity reaches its minimum since the carrier density vanishes at the Dirac point. However, this minimum doesn't drop to zero because of the formation of electrons-holes puddles. Taken from reference [8].

act scattering mechanism is still not very clear, it is believed that the main contribution is given by the interaction with the underlaying substrate, especially for oxide-supported graphene devices. For this reason enhancing the mobility of graphene requires improved sample preparation and/or some post-fabrication cleaning technique such as current or thermal annealing, or even the complete removal of the substrate. Indeed, in suspended annealed graphene devices the mobility has been shown to exceed 200.000 cm^2/Vs [12], which is the largest ever reported value for any carbon-based material. Being the role of the substrate so relevant, great attention has been recently devoted to the selection of an appropriate dielectric for the fabrication of graphene-based devices. A promising candidate seems to be the hexagonal boron nitride (h-BN) [13], which possesses a large band gap, smooth surface, lattice constant similar to that of graphite and could minimize the scattering from charge traps due to the nearly absence of dangling bonds.

Thermal properties

Carbon allotropes occupy a unique place in terms of their thermal properties. Heat conduction in carbon materials is usually dominated by phonons, especially for graphene and its derivatives where, due to the strong covalent sp^2 bonding, heat is transferred by lattice vibrations [14]. The first experimental measurements of graphene thermal conductivity (K) were carried out on suspended graphene by optothermal Raman measurements and reached values from ~ 1500 to ~ 5000 W/mK near room temperature [15, 16, 17], while the limit of in-plane K for pyrolitic graphite is 2000 W/mK at room temperature. Datas deriving from measurements performed on suspended graphene are closer

to the intrinsic K because, similarly to electrical conduction, suspension reduces thermal coupling to the substrate and scattering on the substrate defects and impurities. The theoretical value of graphene K was derived from Boltzmann transport equation and estimated to be ~ 3000 W/mK [18]. Measurements of exfoliated graphene supported on SiO_2/Si substrates revealed an in-plane K of ~ 600 W/mK at room temperature [18], which is still rather high if compared to Si or Cu. It is interesting also to find out how thermal properties are correlated with the number of stacked graphene layers: thermal conductivity progressively decreases by increasing the number of atomic planes untill it reaches the value of bulk graphite. This behaviour was explained by the cross-plane coupling of the low-energy phonons and changes in the phonon Umklapp scattering [19].

Optical properties

As a consequence of its unique electronic structure it was found that graphene absorbs $\sim 2.3\%$ of the incident white light for each layer. In fact, by adopting a model based on the Fresnel law [20], light transmittance (T) of a freestanding graphene monolayer was calculated to be $T \approx 97{,}7$ %, independently of the wavelength of incident light. Thus the absorbance (A) of graphene would be $A \approx 1 - T \approx \pi\alpha \approx 2.3\%$, where α is the fine structure constant ($e^2/4\pi\varepsilon_0\hbar c$) [21]. For few-layer graphene the absorbance (or opacity) is simply the product of $\pi\alpha$ by the number of layers, as represented in figure 1.5 (right). Moreover graphene reflects only $< 0{,}1$ % of the incident light in the visible region [22]. Despite its atomic thickness, graphene can be located exploiting optical image contrast when it is deposited on top of specific substrates thanks

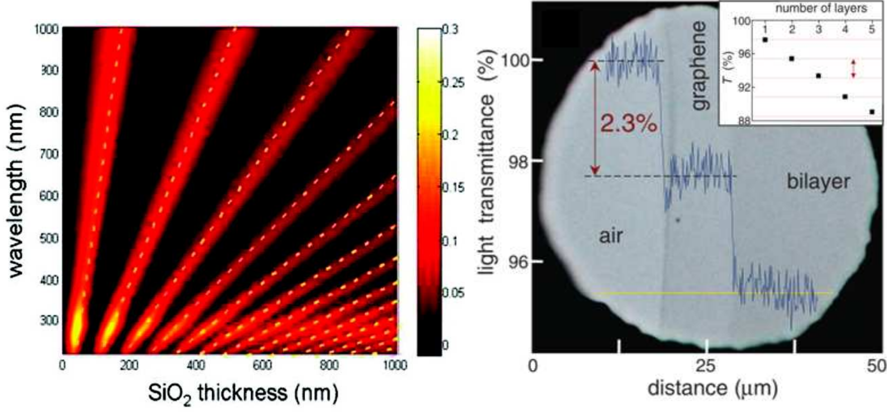


Figure 1.5: Optical properties of graphene. Left: calculated contrast of graphene as a function of silicon oxide thickness and excitation wavelength. Taken from reference [26]. Right: photograph of a 50 μm aperture partially covered with suspended mono- and bi-layer graphene. The inset shows represented the linearity dependance of transparency as a function of number of layers. Adopted from reference [22].

to the light interference effect on the substrate which is modulated by the graphene layer. Furthermore, it is demonstrated that optical spectra can be used as an efficient tool to estimate qualitatively the number of graphene layers [23]. It was found that optical contrast of deposited graphene depends on the substrate type (which determines the refractive index and absorption coefficient) and thickness [24], the number of graphene layers and the angle and wavelength of the incident light [25][26]. The highest contrast is obtained when graphene is deposited on top of SiO_2/Si substrate with the dielectric thickness of 300 nm or 90 nm [25] (see figure 1.5).

Mechanical properties

The best way to measure the intrinsic mechanical behavior of single-layer graphene is to deposit it on a prepatterned substrate in order to obtain suspended samples decoupled from the substrate [27, 28]. The first systematic experimental analysis of elastic properties and strengh of pristine graphene was performed by Lee et al [28]. In their study the graphene membrane was characterized by a tip of on atomic force microscope. They obtained Young modulus of E = 1.0 TPa, third-order elastic stiffness of D = 2.0 TPa and an intrisic strength of σ_{int}= 130 GPa, which is the highest value ever measured for any material. These results awarded graphene the title of the "strongest material ever" and are indicative of its very promising role as streigthening and toughening agent in nanocomposites [29, 30].

Chemical reactivity

From the chemistry standpoint, single-layer graphene con be considered as a giant polyaromatic molecule containing only carbon atoms with an extensive surface accessible from both sides. By chemical functionalization it is possible to control the reactivity, solubility in various solvents, electronic and absorption properties of graphene as well as the type and concentration of charge carries or to impart additional functionalities [31].

The formation of covalent bonds on the basal plane of graphene involves the change of hybridization from sp^2 to sp^3, leading to modifications of the final electronic configuration. For instance, the (massive) hydrogenation or oxidation of graphene results in a conversion from a very

good conductor to an electrically insulating material [32, 33]. The reactivity of monolayer graphene is not the same at all sites of the basal plane. Indeed when one or more carbon atoms switch to sp^3 configuration, the reactivity increases and this could trigger a chain reaction starting at the site of the primary attack. Also the sites of geometric deformation possess enhanced reactivity. At graphene edges, which can manifest as either zig-zag or arm-chair, there is different reactivity as the zig-zag type is thermodinamically unstable and more reactive [34, 35, 36].

The main challenge in graphene chemistry is to impart solution processability in order to enable the large scale production of graphene. Pure graphene is hydrophobic and has no appreciable solubility in most solvents. By derivatizing graphene with different organic moieties, the solubility of graphene can be tuned to suit different solvents needed for the processing of composite films [37, 38, 29]. One potential solution, and surely the most suited among the alternatives offered by covalent derivatization, is the synthesis of graphite oxide followed by exfoliation into individual graphene oxide (GO) sheets and their subsequent reduction. Even if this is not the best strategy for electronic applications because of the presence of residual structural defects and functional groups, the unique chemical versatility of GO allows solubility in a variety of solvents, incorporation into composites, and tailoring a wide range of its properties. The synthesis and applications of reduced graphene oxide (rGO) will be discussed in more detail in the next chapters.

The type and concentration of charge carriers in graphene can be controlled by chemical doping. If it is covalently bonded to electron-

withdrawing oxygen functionalities, p-doping can be induced. Similarly, if it is functionalized by electron-donating nitrogen functionalities, n-doping can be achieved. It is possible to selectively engineer a graphene p–n junction by chemical doping if the interface between p-doped and n-doped graphene regions is precisely controlled [39, 40]. Alternatively, graphene can be p- or n- doped by absorbing different metals on its surface such as Au [41], which has high electron affinity, or alkaline metals, which are good electron donors [42, 31].

A valid strategic route to improve graphene processability is the functionalization *via* non-covalent $\pi - \pi$ stacking with polymers or surfactants which are able to increase the compatibility of graphene sheets within different media. In this way the intrinsic properties of graphene are preserved, extending its use to electronic and other applications [43]. This type of functionalization, which allows the production of dispersed graphene, will bedescribed in sections 1.2.2 and 1.3.

1.2 Graphene synthesis

Synthesis methods of graphene which are of interest of this thesis are described in this section. These methods and their relative costs versus the quality of the so-obtained graphene-like material are illustrated in figure 1.6.

1.2.1 Micro-mechanical cleavage of graphite

This simple method was the one which allowed Geim and Novoselov to firstly isolate a graphene monolayer onto a Si/SiO_2 substrate. They

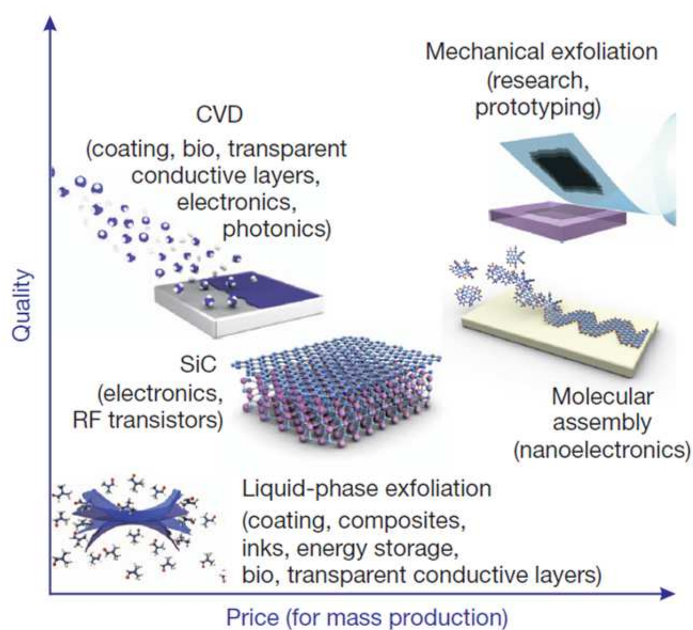


Figure 1.6: Quality of graphene versus price of production methods. Taken from reference [44].

used an adhesive tape to repeatedly split highly-oriented pyrolitic graphite (HOPG) crystals into increasingly thinner pieces. Once the material left onto the adhesive tape is thin and "transparent" enough it is pressed on top of the desired (and sometimes pretreated) substrate, which is then analyized under optical microscope. Originally the adhesive tape was dissolved in acetone, where the exfoliated flakes of mono- and few-layer graphene were left to sediment on top of silicon substrates. Different types of graphite, tapes (with a more or less pronounced tendency to leave glue residues), physical and chemical pre-treatments (to improve the adhesion of graphene flakes to the substrate), post-treatments (to remove any kind of residue left from the exfoliation, i.e. the glue), heating systems (to enhance the exfoliation of graphite into fine flakes) are used during this experimental procedure, and each of them can be fine tuned individually. This method is still largely used in the research field because the quality of the so-obtained graphene flakes is very good. However, the low throughput of this technique makes it unsuitable for large-scale use.

1.2.2 Liquid phase exfoliation

Solution processing is an indispensable prerequisite to meet demands in emerging fields such as printable electronics. Having solutions ready at hand enables chemical functionalization, purification, and transfer of graphene from the solution phase to every conceivable substrate by means of spin-, spray-, drop- or dip-casting. In order to avoid introduction of structural defects caused by chemical oxidation, several groups have attempted to exfoliate and solution process graphene from

graphite or graphite derivatives, preserving intact the basal plane of graphene.

It has been experimentally demonstrated that graphite can be exfoliated and dispersed in a wide range of solvents or surfactant solutions using ultrasound to overcome the Van der Waals forces existing between each graphite layer. Such exfoliation and stabilization of nanoparticles can only occur if the energetic cost is very small, and it can be expressed by the Gibbs free energy of mixing [45]:

$$\triangle G_{mix} = \triangle H_{mix} - T\triangle S_{mix}$$

where $\triangle H_{mix}$ is the enthalpy of mixing, T is the temperature, $\triangle S_{mix}$ is the entropy variantion in the mixing process and $\triangle G_{mix}$ must be ≤ 0 according to the solubility theory. It was shown that for large solute particles like nanotubes (and therefore graphene) $\triangle S_{mix}$ is very small [46], thus $\triangle H_{mix}$ needs to be very small too.

We can approximately calculate $\triangle H_{mix}$ for graphene-based dipersions from the equation [47]:

$$\frac{\triangle H_{mix}}{V_{mix}} \approx \frac{2}{T_{flake}} \left(\delta_G - \delta_{sol}\right)^2 \phi_G$$

where $V_{mix}$is the volume of solvent, T_{flake} is the thickness of graphene flakes, ϕ_G is the graphene volume fraction, δ_G and δ_{sol} are the surface energies of graphene ans solvent respectively. Finally, it is clear that at a given volume fraction and flake thickness $\triangle H_{mix} \propto (\delta_G - \delta_{sol})^2$, which means that for dispersion and stabilization of graphene the values of the two surface energies must be as close as possible and in this case estimated to be ~ 70 mJ/m^2 [47, 48]. However, in the most of the cases

this model fits well with the experimental data but surface energy is not the ideal predictor of solvent quality because it can only describe the overall interaction between graphene and the solvent.

More useful are the Hansen solubility parameters, which describe the solvent-solute system more accurately by distinguishing into dispersive (δ_D), polar (δ_P) and hydrogen (δ_H) intermolecular interactions. According to the solubility theory [49], $\triangle H_{mix}$ is given by :

$$\frac{\triangle H_{min}}{V} \approx \left[\left(\delta_{D,G} - \delta_{D,S}\right)^2 + \left(\delta_{P,G} - \delta_{P,S}\right)^2 /4 + \left(\delta_{H,G} - \delta_{H,S}\right)^2 /4 \right] \phi_G$$

where the subscripts S and G represent solvent and graphene, respectively. Following the previous reasoning, $\triangle H_{mix}$ is minimized when all three solubility parameters of the solvent match those of graphene, specifically $\delta_{D,G} \approx 18$ MPa$^{1/2}$, $\delta_{P,G} \approx 10$ MPa$^{1/2}$ and $\delta_{H,G} \approx 7$ MPa$^{1/2}$ [48, 50]. The sum of the squares of each solubility parameter equals the square of the Hildebrand solubility parameter, δ_T, which is usually sufficient to identify proper solvents for nonpolar solutes: $\delta_T^2 = \delta_D^2 + \delta_P^2 + \delta_H^2$. Thus also the Hildebrant solubility parameter of solvent and graphene must be very close to each other. It is observed that good graphene dispersions are achieved with solvents having $\delta_T \sim 23$ MPa$^{1/2}$ [50]. Hernandez et al. demonstrated that surface tension, Hildebrand and Hansen parameters are related to the overall solvent-graphene interaction. They tested 40 differents solvents and identified the best solvents for the production of graphene dispersions from graphite exfoliation [50].

Once the proper solvent has been chosen, a critical issue is how to in-

crease the maximum concentration obtainable while mantaining intact the quality of the graphene flakes. The parameters which define the exfoliation procedure performed by ultrasound (also called sonication) are crucial for the efficiency of the process: sonication time, sonication power, type of ultra-sonic generator (bath or probe), initial concentration of graphite and solvent temperature. Depending mainly on the sonication time and the amount of energy transferred to the graphite platelets, the flake size distribution can be quite broad both in terms of thickness and lateral dimensions [51, 52]. Coleman et al. demonstrated that the final lateral dimensions of flakes decrease with sonication time as $t^{-1/2}$, while the mean number of layers per flake is close to 3 for all sonication times [51]. They considered the influence of the sonication procedure on the maximum obtainable concentration, which was measured recording UV-vis spectra after centrifugation in order to remove the unexfoliated material. As expected, the increase in graphene concentration is correlated with the decrease in flake dimensions as sonication time and energy output of the ultrasonic bath are increased. Some other strategies to fine tune the graphene dispersions in terms of flake size and final concentration have been explored, e.g. controlled centrifugation [53] or density differentiation [54, 55] were used to separate flake by size and filtration followed by re-dispersion [56] to produce highly concentrated graphene dispersions. Finally, another important question is whether prolonged sonication causes the introduction of basal-plane defects or defects associated with new edges. The intensity of the Raman D band (indicative of defects) was monitored in a series of samples collected at different sonication times [51], and it was found that it increases with time as $t^{1/2}$. For flakes in the size range below 1 μm the edges contribute to the spectrum, appearing as defects.

Thus it is possible to state that graphene flakes produced using solvent exfoliation are relatively defect-free [48] and that the increase in the Raman D band is attributed to the formation of new edges [51].

For many applications, exfoliation of graphene in solvents is undesirable due to a number of issues such as high boiling point, toxicity or incompatibility with practical aspects of processing. For this reasons the possibility of exfoliating graphene in water in the presence of a surfactant has been explored [57, 52, 58] or polymer [59, 60] as stabilizer. Like many colloidal systems, surfactant-coated graphene flakes are stabilized electrostatically against aggregation [61, 62], thus the size of the repulsive barrier generated by the headgroup ions plays a crucial role. The nature of the hydrophobic part of the dispersant is also critical for an efficient dispersion. It has been demostrated that molecules which are able to interact with the aromatic graphene plane *via* $\pi - \pi$ interactions, i.e. possessing benzene rings, or with a planar and rigid structure, i.e. sodium cholate, tends to promote highly-concentrated and more stable graphene dispersions compared to flexible and long-chain surfactants [52].

1.2.3 Chemical vapour deposition (CVD)

One of the major advantages of substrate-based methods for graphene synthesis is their high compatibility with current complementary metal-oxide semiconductor (CMOS) technology. In the graphene context, this method is referred to decomposition of hydrocarbons into graphitic materials on a metal substrate. CVD growth of graphene has been mainly practiced on copper [63, 64] and nickel [65, 66] thin films, which

have different growth mechanisms and leads to graphene with different properties. On the other side, the carbon precursor is usually a gas, i.e. methane, but it could also be liquid or even solid. The metal substrate is put into a furnace and heated under low vacuum to around 1000 °C in order to increase its domain size by annealing. The precursor is then inserted into the furnace together with hydrogen, which act as a catalyst causing carbon atoms from the precursor to be deposited onto the surface of the metal through chemical adsorption. The furnace is then cooled to keep the deposited carbon layer from aggregating into bulk graphite, which crystallizes into a contiguous graphene layer on the surface of the metal. After growth, graphene should be transferred from the metallic support to a dielectric surface, which is performed by a wet-chemical removal of the underlying metal layer. The main difference between the Ni and Cu substrate consists in solid solubility of carbon. While Ni has a considerable solid solubility of carbon, Cu has very limited solubility and thus carbon does not diffuse to a great depth in the Cu substrate. Another advantage of Cu substrate is the fact that the graphene growth is self limiting, i.e., it stops after one layer is grown. In case of Ni the graphene film thickness depends on the time of exposure as well as the thickness of the Ni film. Despite the presence of defects (e.g., wrinkles or grain boundaries) such graphene films show transport properties equivalent to those of exfoliated graphene on both SiO_2 and hexagonal BN substrates. The transfer process of graphene from the metal substrate deteriorates the graphene quality as well as causes the formation of wrinkles and other defects. Some groups worked on the optimization of this process with the objective of minimizing the damage to graphene or recovering the sacrificial metal. One example is represented by Levendorf et al, who

developed a selective etching of the underlaying substrate by masking using photolithography, after which the remaining substrate was used as electrodes [67]. A detailed review of CVD graphene techniques and applications is reported in reference [68].

1.2.4 Epitaxial growth on Silicon Carbide (SiC)

Epitaxial graphene growth on metal carbides has been practiced since long time ago, but the use of SiC as a substrate was introduced only recently. SiC is a wide band gap (3 eV) semiconductor and it can be used as an insulating substrate in electrical measurements. This was done for the first time in 2004 on patterned epitaxial graphene grown on SiC under UHV conditions [69]. In 2009 Emtsev et al. suceeded in growing high quality, large area epitaxial graphene on SiC(0001) at close to atmospheric pressure (900 mbar) in an argon atmosphere [70]. More recently, Bao et al. prepared high quality freestanding single-layer graphene employing polycrystalline SiC granules instead of single-crystal SiC as a substrate [71]. The thermal treatment of SiC at about 1300-1600°C under vacuum results in the sublimation of the silicon atoms while the carbon-enriched surface undergoes reorganization, and eventually graphitization, due to the lower sublimation rate of carbon with respect to silicon. However, the strict operating conditions such as high-temperature, ultrahigh vacuum or inert atmosphere, single-crystal substrate (in most cases) represent a limit for large-scale applications of epitaxial graphene. Other issues that may need to be addressed are the elimination of terraces, the growth of the second or third layer at the edges of the terraces, an increase in the size of the crystallites and control of unintentional doping from the substrate.

1.2.5 Reduction of graphene oxide

In the same way as graphite is composed by stacked graphene monolayers, graphite oxide has a layered structure constituted by stacked graphene oxide (GO). The introduction of oxygen-containing groups, which occurs during graphite oxidation, expands the interlayer distance and makes each layer hydrophilic, allowing water molecules to be intercalated between each oxdized graphite sheet. Thus the separation and delamination of each layer of graphite oxide can easily be obtained by its exfoliation in water under moderate sonication or agitation, generating a stable colloidal dispersion of GO sheets [72].

The synthesis of graphite oxide was first reported by B. C. Brodie [3], who found that adding potassium chlorate to a slurry of graphite in fuming nitric acid results in a material composed of carbon, oxygen and hydrogen. The net formula, after four oxidative treatments, was determined to be $C_{2.19}H_{0.80}O_{1.00}$, and the material was dispersible in pure or basic water, but not in acidic media. Over the course of the following years many variations of the Brodie's method have been proposed, but only in 1958 it was reported by Hummers and Offeman [73] the oxidation of graphite with a mixture of concentrated sulphuric acid, sodium nitrate and potassium permanganate, which is nowdays better know as the Hummers method. The main strategy to produce GO at present is through modifications of the Hummers method [74].

The structure of graphite oxide has been widely investigated for over a century and various structural models of GO have appeared in the literature [75, 76, 77, 78]. The elemental composition of the final product depends mainly on the nature of the pristine graphite, its particle

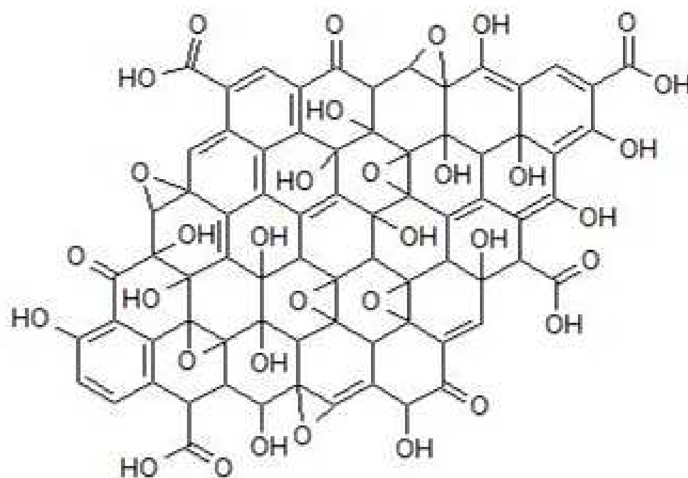


Figure 1.7: Simplified structure of GO. The carbon plane is decorated with hydroxyl and epoxy functional groups and with carboyl or carboxyl groups at the edges of the GO sheet. For simplification there is omission of minor groups (such as esters, lactones, etc.) and structural defects.

size and the conditions of preparation. Figure 1.7 shows a simplified example of the chemical structure of GO: the heavily decorated GO sheet consists partly of tethraedrally bonded sp^3 carbon atoms which give origin to different oxygen-containing groups (such as hydroxyl, epoxy, carboxyl, carbonyl, esters, lactones, etc.) displaced above or below the graphene plane. Several groups observed also the presence of highly defective regions by scanning tunnelling microscopy (STM) [79], which contribute to the roughening of the GO sheet at atomic scale. It appears evident how the conjugated structure of pristine graphene is broken by functionalization, with the subsequent localization of π-electrones. This phenomenon is expressed by the blocking of long-range (μm) conductivity of GO sheets because of the absence of percolating pathways between the intact sp^2 carbon clusters.

Therefore, the reduction of GO should both remove the oxygen-containing functional groups and repaire the structural defects, with the primary objective of recovering the conjugated network and the electrical conductivity of graphene. Chemical and Thermal reduction are the two most common techniques adopted to reduce GO, which will be subsequently examinated in more detail. The chemical route can be performed both in solution or after deposition onto a substrate, while thermal reduction requires having GO into dry powdered form or already deposited as thin-film or a single flake. Despite the presence of residual structural defects in rGO, there are several advantages of this route toward the production of graphene: 1) natural graphite is an ubiquitous and inexpensive raw material, 2) the GO production process would adopt cost-effective chemical methods with a high-yield ($>$80%) of GO monolayers, 3) stable aqueous colloidal dispersions of

hydrophilic GO allow high processability and ease of thin-film deposition techniques, thus facilitating both the assembly of macroscopic structures on various substrates or the incorporation into polymeric matrices.

Since the reduction generates great changes in the atomic structure and properties of GO, experiments for characterizing the properties of the resulting reduced material and evaluating the extent of the reduction process must be performed. The UV-vis spectrum of GO exhibits two characteristic features that can be used as a mean of identification: a sharp peak at 231 nm, corresponding to $\pi \rightarrow \pi^*$ transitions of aromatic C-C bonds, and a shoulder at ~300 nm, which can be attributed to n$\rightarrow\pi^*$ transitions of C=O bonds [38]. As shown in figure 1.8, upon reduction of GO the main absorption peak at 231 nm gradually redshifts and the absorption in the whole spectral region increases with reaction time, suggesting that the electronic conjugation within the graphene sheets is restored upon reduction [37].

The electrical conductivity is perhaps the best indicator of the extent to which GO has been reduced to graphene. It is worth to distinguish between electrical conductivity, indicated as σ(S/m), and sheet resistance, indicated as $R_s(\Omega/\mathrm{sq})$, which is a measure of the electrical resistance of a sheet, indipendent of its thickness. Sheet resistance is related to bulk conductivity as $R_s = 1/\sigma t$, where t (m) is the sample thickness.

The removal of intercalated water molecules, functional groups, structural defects as well as lattice contraction, which occurs upon GO reduction, causes a variation in the interlayer distance in GO films and powders which can be measured by X-ray diffraction (XRD) [81, 82,

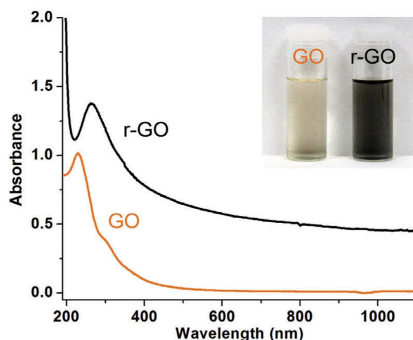


Figure 1.8: UV-vis optical absorbance of GO and rGO aqueous dispersions. The absorbance of GO is weaker than r-GO due to lower degree of π-conjugation which increases the HOMO and LUMO further away. Taken from reference [80].

83, 84]. The theoretical background of XRD applied to the analysis of GO/rGO is discussed more in detail in reference [83]. The chemical composition of both GO and rGO depends strongly on the preparation method and can be estimated through X-ray photoelectron spectrometry (XPS) analysis [85]. Typically GO has a C/O ratio of 4:1 - 2:1 [86] which can be improved upon reduction up to 12:1 in most cases, but values as large as 246:1 have been recently reported [87]. In addition to the above mentioned techniques, some other types of analysis such as Raman spectroscopy [88], Infrared spectroscopy [37], atomic force microscopy (AFM), transmission electron microscopy (TEM) [89] and solid-state FT-NMR spectroscopy [90], can be also performed to understand better the GO structure and properties changes that occurs after reduction.

Thermal treatment

The oxygen-containing functional groups of GO films or powders can be decomposed at elevated temperatures (thermal annealing). Typically, thermal reduction is achieved above 200°C in inert or reducing environments and becomes more efficient at higher temperatures [91, 92, 82, 83]. The heating temperature plays a crucial role in achieving the highest C/O ratio and restoring the electrical conductivity of rGO. The annealing atmosphere is also very important. Firstly because etching of oxygen is significantly increased at high temperatures, requiring oxygen gas to be excluded from the environment. Secondly because the removal of functional groups may be more efficient in presence of reducing gases. As a result, the annealing reduction is usually performed in vacuum or in an inert (Ar) or reducing (H_2 or Ar/H_2) atmosphere.

Kaniyoor et al. compared four different annealing conditions for the reduction of graphite oxide: in Ar at 1050°C, in vacuum at 200°C, in a mixture of Ar/H_2 at 200°C and in H_2 at 200°C [93]. It was demonstrated that the last option was the most efficient for achieving both the highest C/O ratio and electrical conductivity. Moreover, thanks to the reducing ability of hydrogen at elevated temperatures, the reduction of GO can be carried out at relative low temperatures with respect to other operating conditions. A notable effect of thermal exfoliation is the structural damage caused to the rGO platelets by the release of carbon dioxide [94]. Approximately 30% of the mass of GO is lost during the thermal treatment, leaving behind vacancies and topological defects throughout the plane of the reduced GO platelet [95]. Some other drawbacks of thermal annealing usually concerns the high

energy consumption, the long heating times (to avoid rapid evaporation of carbon dioxide in GO deposited films) and the limited choice of substrates which can undergo such critical conditions.

Chemical methods:

A variety of chemical means may be used to reduce GO. The most common and one of the first to be reported is reduction by hydrazine (N_2H_4), which can be used in aqueous solutions, as anhydrous hydrazine or as a gas under vacuum [96, 37, 72, 90]. A proposed reaction pathway for epoxide reduction by hydrazine is shown in figure 1.9. Gao et al. investigated the reaction mechanism for deoxygenation of GO with hydrazine treatments [104]. It was found that hydrazine reduction of epoxide groups attached to the interior of an aromatic domain of GO is thermodynamically spontaneous, while the reduction of an epoxide located at the edges of an aromatic domain is blocked by the formation of a hydrazin alcohol. No reaction path was found for the hydrazine-mediated reduction of hydroxyls, carbonyls and carboxyls of GO. In general, the oxygen functionalities attached to the interior of an aromatic domain in GO are removed easier than those attached at the edges, as confirmed also by Eda et al [86]. Morover, some heteroatomic impurities can be introduced. Indeed nitrogen tends to remain covalently bound to the surface of GO, likely in the form of hydrazones, amines, aziridines or other similar structures [84]. These residual C-N groups may have a profound effect on the electronic strucutre of the resulting rGO, acting as donors compensating the hole carriers. Wet-chemical reduction usually causes aggregation of the de-oxygenated rGO platelets, therefore it could be convinient to improve the sta-

Reducing treatment	Form of GO during reduction	Conductivity(σ)[$\frac{S}{m}$] ; Sheet resistance (Rs)[$\frac{k\Omega}{sq}$]	Ref.
N_2H_4	solution	10^8-fold decrease in Rs	[96]
N_2H_4/NH_3	solution	σ = 72*10^2	[37]
N_2H_4vapors	film	Rs = 4*10^6	[72]
$NaBH_4$	solution	σ =45 ; Rs = 2.6	[84]
$NaBH_4$	solution	σ = 46*10^3	[97]
$NaBH_4/H_2SO_4$/t.a.	solution	σ =2.02*10^4	[87]
$NaBH_4/N_2H_4$	solution	σ =12.5*10^2	[98]
L-ascorbic acid	solution	σ =77*10^2	[99]
PDD	solution	σ =1.5	[100]
HI acid	film	σ =4.2*10^4	[101]
N_2H_4 and t.a. Ar/H_2	film	σ =2.3*10^3	[91]
t.a. 1100°C Ar/H_2	film	σ =5.5*10^4; Rs = 1.8	[92]
Zn powder/NaOH	solution	σ =7.5*10^3; Rs = 38.5	[102]
Al foil/HCl	solution	σ =1.25*10^4; Rs = 1.4*10^2	[102]
Al foil/NaOH	solution	σ =1.12*10^3	[102]
Al powder/HCl	solution	σ =2.1*10^3	[103]

Table 1.1: Overview of some methods used to convert GO to rGO. Notes: t.a. = thermal annealing

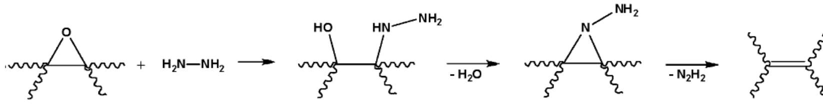


Figure 1.9: A proposed reaction pathway for epoxide reduction by hydrazine. Taken from reference [90]

bility of the rGO colloidal dispersion adopting stabilizers or choosing some proper solvents rather than water. Stankovich et al. proposed the reduction with hydrazine in the presence of poly(sodium 4-styrenesulfonate) (PSS), to yield PSS-coated graphitic nanoplatelets that can be redispersed readily in water upon mild sonication [105]. Despite its initial success in the reduciton of GO, hydrazine is a highly toxic and potentially explosive chemical and therefore it should be avoided in the large-scale implementation of this approach.

Sodium borohydride ($NaBH_4$), as well as other metal hydrides, were also demonstrated to function as very effective reductants of GO [84]. With a large excess of reducing agent, it is most effective at reducing C=O species, while having low to moderate efficiency in the reduction of epoxides and carboxylic acids [106]. Additional alcohols are the main impurities generated (as a result of the hydrolysis of the boric ester) [32]. In order to improve the deoxygenation and restoration of the sp^2 network, Gao and co-workers [87] developed a two-step reduction process: deoxygenation with $NaBH_4$ followed by dehydration with concentrated sulfuric acid. The product of this two-step reaction, compared to the use of hydrazine, has a very low number of remaining functional groups, high conductivity, larger crystallite size and good solubility. Multistep reduction based on a combination of different pro-

cesses is also an effective route for removing specific functional groups. The reduction process shown in table 1.1 from reference [98] combines the use of $NaBH_4$ and hydrazine in three steps: 1) prereduction of GO with sodium borohydride to remove the majority of the oxygen functionalities; 2) sulfonation with the aryl diazonium salt of sulfanilic acid; 3) postreduction with hydrazine to remove any remaining oxygen functionality. The slightly sulfonated r-GO can be readily dispersed in water in a pH range of 3 -10.

Another interesting alternative is represented by the use of vitamin C (L-ascorbic acid) as an environmental-friendly reducing agent, as shown in table 1.1 . It has been demonstrated [104, 99] that L-ascorbic acid has a good deoxygenation efficiency and stable suspensions of highly rGO which can be prepared not only in water, but also in some common organic solvents. This should facilitate the further manipulation and processing of this material for practical applications. Moreover, the introduction of heteroatoms is minimized since vitamin C is only composed of carbon, oxygen and hydrogen.

More recently, metallic Zn and Al have been proposed as environmentally friendly reducing agents for GO, finding their highest effectiveness in alkaline and acidic media respectively [102, 103]. Fan et al. firstly explored this green route in 2010 by adding aluminum powder to GO colloidal dispersion acidified by HCl [103]. They explained the reduction process by the highly negative standard reduction potential of Al^{3+}/Al = -1.68V ($Al^{3+} + 3e^- = Al$), which was even improved by the presence of HCl. As a countercheck, the same process was performed separately in the presence of only aluminum powder or hydrogen flux, respectively, deducing that no GO reduction was occured at all. In

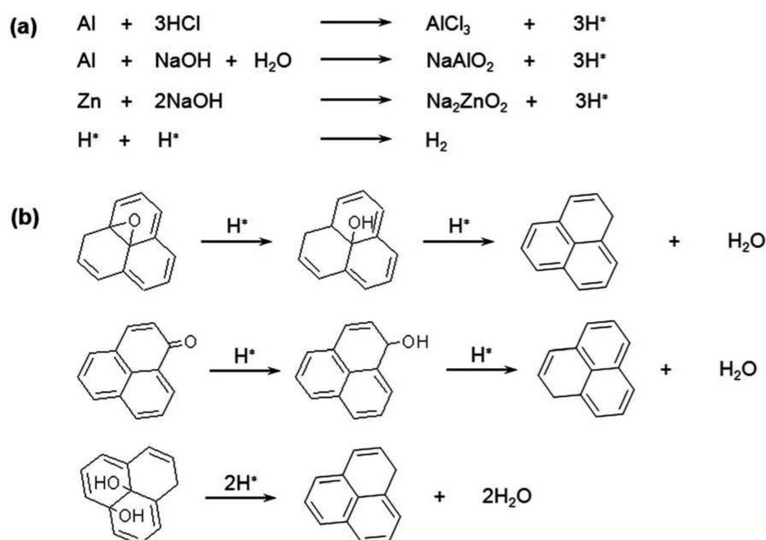


Figure 1.10: GO reduction by metallic Zn and Al through the formation of nascent hydrogen. a) Hydrogen generation in acidic or alkaline medium. b) Reaction pathway for GO deoxygenation by nascent hydrogen. Taken from reference [102].

2012, a similar study was accomplished by Pham and coworkers [102]. Three different experiments were performed with GO solution adopting as reducing environments: Zn powder in NaOH, Al foil in HCl and Al foil in NaOH. As shown in table 1.1, the most efficient combination was the GO reduction carried out in the presence of Al and HCl, which lead to rGO film conductivity as high as 1.25×10^4 S/m, almost one order of magnitude higher than that of the previous study of Fan and coworkers. In all three cases, the reaction pathway was explained by the *in situ* generation of hydrogen and subsequent removal of oxygen groups on GO by nascent hydrogen itself [102], as represented in figure 1.10.

Other reductants have been used for the production of chemically-derived graphene including hydroquinone [107], strong alkaline solutions [108], p-phenylene diamine (PPD)[100] or UV-assisted reduction of GO modified with TiO_2 particles [109]. Although the underlying mechanism remains unclear, the deoxygenation of exfoliated GO under alkaline conditions appears to be the reverse of the oxidation reaction of graphite in strong acids [108].

1.3 Graphene applications

As mentioned in the previous section, the final quality of graphene strongly depends on its production method, thus also the properties of each product will be very different. Starting from this concept, each type of produced graphene is more suitable for some specific application. For instance, electronic applications usually require the intrinsic electrical properties of graphene to be preserved, thus CVD and epitaxial growth will be ideal because of the availability of large-area and high-quality graphene crystals supported on a substrate. On the contrary, transparent conductive coatings or conductive inks request higher processability in order to allow the conductive material to be easily deposited onto the substrate from a stable solution phase. In that case rGO solutions or graphene dispersions obtained from liquid phase exfoliation possess the requirements to approach the majority of technologies for thin film deposition. In the following subsections the applications of graphene which are of interest of this thesis are briefly described.

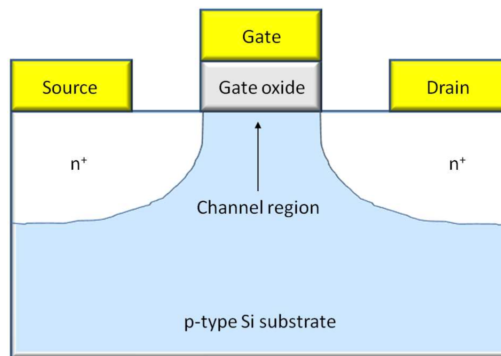


Figure 1.11: Cross section of a n-doped Si MOSFET. The length of the channel is defined by the length of the gate electrode

1.3.1 Electronic applications

The field effect transistor (FET) is the most successful device concept in electronics and most work on graphene devices has been so far related to FETs. A FET consists of a gate, a channel region connecting source and drain electrodes, and a barrier separating the gate from the channel. The operation of a conventional FET relies on the control of the channel conductivity, and thus the drain-souce current, by a voltage, V_{GS}, applied between the gate and source, due to the field effect phenomenon. Since the first uses of this type of device, the electronics industry has come a long way, and the FETs we commonly find now are the silicon metal-oxide-semiconductor FETs (MOSFETs). Any transistor based on an alternative material (other than silicon) must compete with a 50-old year history of MOSFETs.

The schematic structure of a MOSFET is represented in figure 1.11. The semiconducting channel is connected to two terminals labeled source (S) and drain (D) that are used to apply a voltage along the

channel, whereas the third terminal labeled gate (G) is electrically insulated from the semiconducting channel. It serves to control the electrostatic potential at the semiconductor/insulator interface. There are different types of FETs that can be distinguished by the way the gate is coupled to the channel. At present, the most commonly used type is the MOSFET in which the gate capacitor is formed by an insulator, i.e. SiO_2, between the metallic gate electrode and the semiconducting channel.

For high-speed applications, FETs should respond quickly to variations in $V_{\rm GS}$. This requires short gates and fast carriers in the channel. Unfortunately, FETs with short gates frequently suffer from degraded electrostatics and other problems (collectively known as short-channel effects). Scaling theory predicts that a FET with a thin barrier and a thin gate-controlled region (in the vertical direction in figure 1.11) will be robust against short-channel effects down to very short gate lengths (in the horizontal direction in figure 1.11). Thus the possibility to exploit graphene as one-atom thick channel is perhaps the most attractive feature for its use in transistors. Moreover, the series resistance between the channel and the source and drain terminals is also important, and its adverse impact on the FET becomes more pronounced as the gate length decreases.

The two principal divisions of semiconductor electronics are digital logic and analog devices. Modern digital logic is based on silicon complementary metal oxide semiconductor (CMOS) technology. CMOS logic gates consist of both n- and p-channel MOSFETs that can switch between the on-state (with a large on-current, $I_{\rm on}$, and $V_{\rm GS} = \pm V_{\rm DD}$, where $V_{\rm DD}$ is the maximum voltage supplied to the device) and the

off-state (with a small off-current, I_{off}, and $V_{\text{GS}}= 0$). The gate voltage where the FET is just on the verge of switching is labeled threshold voltage, V_{th}, or in other words this is the value of V_{GS} at which there are sufficient carriers in the inversion layer to make a low resistance conducting path between the source and drain. The ability of CMOS to switch off guarantees extremely low static power dissipation (which is the reason why silicon CMOS has bested all competing logic technologies). Thus, any successor to the silicon MOSFET that is to be used in CMOS-like logic must have excellent switching capabilities, as well as large on-off ratios ($I_{\text{on}}/I_{\text{off}}$) [110].

On the other hand in analog applications, which find place in radiofrequency (RF) devices, switch-off is not necessary. For example, in signal amplifiers the transistor is in the on-state and the RF signal to be amplified is superimposed on the dc gate bias. The cutoff frequency, f_{T}, defined as the frequency at which the short-circuit current gain becomes unity, is one of the most important figures of merit for evaluating the performance (the intrinsic speed) of RF devices. It can be maximized by making the intrinsic transductance, g_{m}, as large as possible and making the output conductance, g_{d}, and all the capacitances and resistances in the circuit as small as possible [110]. Having shorter gates, faster carriers and lower series resistances certainly increase cutoff frequency. Another figure of merit for mixed-signal circuits is the intrinsic voltage gain, $A = g_{\text{m}}/g_{\text{d}}$, which must be $>$1 in order FET to be useful in practical electronic applications. One way of improving the gain is increasing g_{m} by using a thinner gate dielectric [111], which will also reduce g_d by improving the electrostatic gate control. On the contrary, observed decrease of voltage gain with decreasing channel

Parameter	Definition
Transconductance	$g_{\mathrm{m}} = \frac{dI_{\mathrm{D}}}{dV_{\mathrm{GS}}}$
Output conductance	$g_{\mathrm{d}} = \frac{1}{r_{\mathrm{d}}} = \frac{dI_{\mathrm{D}}}{dV_{\mathrm{DS}}}$
Intrinsic voltage gain	$A = \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}}$
Cut-off frequency	$f_{\mathrm{T}} \approx \frac{g_{\mathrm{m}}}{2\pi C}$
field-effect mobility	$\mu_{\mathrm{FE}} = \frac{L_{\mathrm{ch}} g_{\mathrm{m}}}{W_{\mathrm{ch}} C_{\mathrm{G}} V_{\mathrm{DS}}}$

Index G, D and S refers to gate, drain and source respectively; V_{GS} and V_{DS}: terminal dc voltages; I_{D}: dc drain current; $L_{\mathrm{ch}}$and W_{ch}: channel length and width respectively; C: device capacitance; C_{G}: gate capacitance, here expressed per unit area.

Table 1.2: Performance measures of FETs.

length, was mainly attributed to a lack of complete current saturation in short channels [111].

The high mobility of charge carriers in graphene at room temperature makes this two-dimensional material very attractive for applications in high-speed electronics. Unlike other materials, the graphene mobility is equal between electrons and holes and much greater than that of InP, which currently dominates high-speed electronics. Unfortunately, large-area graphene is a semimetal with zero bandgap and for this reason graphene-based FETs cannot be switched off and have very low on/off ratios. Thus one of the thrust areas in the fields of graphene reasearch right from the very beginning has been the development of the techniques to open a band gap in graphene without compromising on any of its other properties. Three main techniques have been

proposed in order to open a band gap: 1) by constraining large-area graphene in one dimension to form graphene nanoribbons (GNRs); 2) by exposing bilayer graphene to strong perpendicular fields; 3) by applying strain to the graphene sheet.

The first method is based on quantum confinement of charge carriers in a single dimension similar to semiconducting single-walled nanotubes (SWNTs). It was predicted that the finite bandgap is, to a good approximation, inversely proportional to the width of the nanoribbon and experimental GNRs showed bandgaps for widths below 20 nm. One consequence of quantum confinement induced in graphene is the reduction of the on current, wich in turn reduces voltage gain [112]. Another drawback is represented by the general trend of charge carrier mobility to decrease as the bandgap increases.

The second method is based on applying a perpendicular electric field on bilayer graphene. This opens a bandgap near the K point and bands take the so-called Mexican-hat shape. It was predicted theoretically that the size of the bandgap depends on the strenght of the perpendicular field.

The third method proposed to open a bandgap is based on the effect of uniaxial strain on the band structure of graphene. It was predicted that in order to open a bandgap a global uniaxial strain exceeding 20% would be required , which is difficult to achieve in practice.

Both analog and digital would benefit from the band gap. In this thesis three type of graphene-based electronic devices are reported: audio voltage amplifier, integrated complementary invertes and gigahertz integrated ring oscillators. Their fabrication and characterization will be discussed in the next chapters.

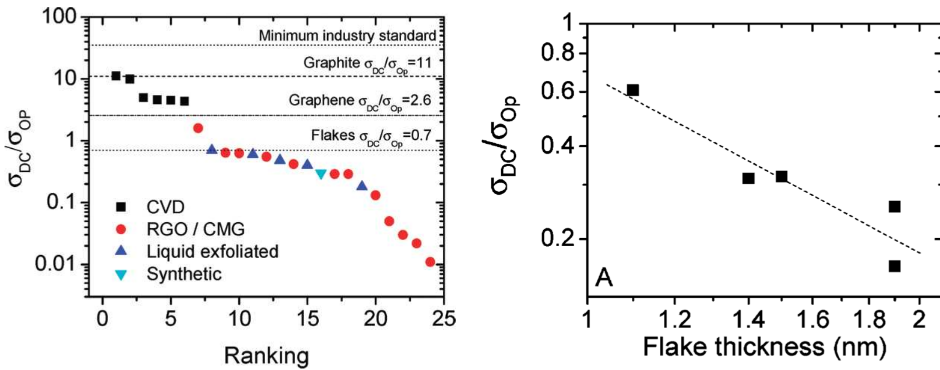


Figure 1.12: The conductivity ratio for different kind of thin graphene films. Left: conductivity ratio, $\sigma_{\mathrm{DC}}/\sigma_{\mathrm{Op}}$, as calculated from T and R_{S}, for CVD graphene, rGO films and graphene films obtained from liquid phase exfoliation and synthetically grown. The horizontal lines represents fundamentally limiting values of $\sigma_{\mathrm{DC}}/\sigma_{\mathrm{Op}}$ for each category. Right: Scaling of $\sigma_{\mathrm{DC}}/\sigma_{\mathrm{Op}}$ with flake thickness for films obtained from liquid phase exfoliated graphene. Adopted from reference [113].

1.3.2 Transparent Conductive Coatings

Among its many exciting properties, graphene is conductive and, when stacked thin enough, transparent. Thus one discipline in graphene research is the preparation of transparent and electrically conducting coatings for the substitution of commonly used transparent conductors as indium tin oxide (ITO), which is currently used for touch screen applications and transparent electrodes. As explained in section 1.2, graphene can be processed from solution to match common coating techniques, either as GO or pristine graphene in solvents. Alternatively graphene films can be grown by CVD and transferred to many different surfaces. The performance of these thin films is very different with respect to transparency and sheet resistance. Moreover, such films

tend to have various thicknesses and a comparison between them is often difficult.

The most common methods which were developed to characterize the electrical performance of graphene-based conductive films relies on the determination of the sheet resistance (Ω/sq), defined as $R_\mathrm{S} = 1/(\sigma_\mathrm{dc} t)$, where σ_dc is the dc conductivity and t is the film thickness, and transmittance (%), $T = \left(1 + \frac{Z_0}{2}\sigma_{O\mathrm{p}} t\right)^{-2}$, where $\sigma_{O\mathrm{p}}$ is the optical conductivity and $Z_0 = 377\ \Omega$ is the impedance of free space [113]. Coleman et. al identified an appropriate figure of merit which allows the comparison between different transparent and electrically conducting film, either based on graphene or other materials. The figure of merit is the dc to optical conductivity ratio, $\sigma_\mathrm{dc}/\sigma_\mathrm{Op}$, which connects T and R_S for a thin conducting film by the equation $T = \left(1 + \frac{Z_0}{2R_S}\frac{\sigma_{Op}}{\sigma_\mathrm{dc}}\right)^{-2}$ [113]. Higher values of $\sigma_\mathrm{dc}/\sigma_\mathrm{Op}$ result in the desired properties, meaning higher T and lower R_S. In figure 1.12 $\sigma_\mathrm{dc}/\sigma_\mathrm{Op}$ values are plotted versus ranking (left) and flake thickness (right), for different types of graphene. CVD films are clearly the best while solution processed films (from rGO or liquid exfoliated graphene) are worse in quality and span a wider range. Concerning rGO films, it is evident that the chemical distorsions caused by the oxidation and reduction procedure limits the performance and to further improve the quality of such films a high temperature annealing step is often required. But even when graphite is not oxidized as in liquid exfoliated graphene, the performance of the film is not much better, or even worse compared to rGO films, because of the massive presence of interflake junctions. As mentioned above, the influence of flake thickness on the $\sigma_\mathrm{dc}/\sigma_\mathrm{Op}$ values for film deposited from liquid exfoliated graphene was experimentally demon-

strated (figure 1.12 right). The σ_{dc}/σ_{Op} values tend to increase at lower flake thicknesses, reaching a maximum at ≈ 0.7 for monolayer graphene flakes, which is proposed as limiting value for network of liquid exfoliated graphene [113]. The general explanation of this limit is that the performance of such films is controlled by the topology of the network and the tunnelling probability between overlapping graphene sheets.

1.3.3 Electrically conductive inks

Electrically conductive inks are used in a wide variety of applications. The conductive tracks in printed circuit boards are a mature and well-known application. Other examples are membrane touch switches, heating elements, sensors and displays. RFID and medical applications are more recent and emerging, while photovoltaics and printed transistors present future opportunities for electrically conductive ink applications.

A conductive ink consists of a polymer (or binder), a solvent, a pigment and additives. The polymer or binder will keep the pigment particles together and determine the mechanical properties - such as adhesion, flexibility and hardness of the final ink. To make the ink processable, the binder is dissolved. The application technique determines which solvent is used. For a typical application method such as screen printing, high boiling point solvents are used. High-speed printing methods like rotogravure, require low boiling point solvents. Most important is the pigment, as it determines the conductivity of the final ink. Most of today's materials employ silver as the pigment. Usually silver par-

ticles are flake-type materials, as these tend to provide the highest conductivity. Characteristics like the surface area, particle size and the type of lubricant have great influence on the final conductivity of the dried ink. Additives can be used in the formulation in order to optimize other properties such as wetting, flow, adhesion, flexibility or the rheology of the ink.

Printing techniques, such as inkjet printing, are competitive alternatives to conventional photolithography for the production of electronic devices with advantages including low cost, ease of mass production, and flexibility. Compared with other printing techniques (e.g., screen printing and microcontact printing), inkjet printing has attracted more attention due to its significant advantages involving compatibility with various substrates, availability of non-contact and no-mask patterning, low temperature processing, and no requirement for vacuum processing. Several conductive meterials, such as metals and polymers, have been widely studied. The main shortcomings known for these materials are the extremely high costs for metal particles and the low conductivity together with poor chemical and thermal stability for conductive polymers. Graphene is a prominent contender as conductive pigment in printed electronic devices due to its high conductivity, chemical stability and intrinsic flexibility. Among different methods for its production, solution-processed graphene (rGO and liquid exfoliated graphene) is clearly the only one compatible with common printing technologies such as ink-jet printing.

There are many parameters involved in achieving a repeatable and reliable prin ting process to produce continuous and conducting patterns with high quality. Concerning the size of solid particles, these

should be smaller than the nozzle diameter, to prevent clogging. A rule of thumb states that it is sufficient to manage particles with at least 1/50 of the nozzle diameter as a maximum dimension, which in the case of graphene refers to flake lateral dimensions. Conventional pigments in inkjet inks contain particles generally in the size range of 100-400 nm, thus graphene lateral dimensions should not exceed this value. The most common technique to remove larger flakes from the graphene-based dispersions is centrifugation, as described in section 1.2.2. Ink viscosity is another important factor, which is mainly influenced by the solid content of the ink and by the choice of solvents. Highly concentrated graphene dispersions usually suffer from stability problems, while very low concentrations request the repeated passage of the same pattern in order to form a uniform conductive network of graphene flakes. The final assembly of printed nanoparticle inks depends also on the substrate surface energy and ink surface tension. The first one can be modulated by treating the substrate with proper adhesion promoters, such as hexamethyldisilazane (HMDS) or octadecyltriclorosilane (OTS). Ink surface tension depends mainly on the choice of solvent and additives, such as various surfactants which can contribute to adjust the surface tension of the ink as well as stabilizing the particles dispersion. These two parameters, together with the solvent boiling point, are responsible for the formation of the so-called “coffee ring effect”. It consists of a dense ring-like deposit of solid particles along the perimeter of the pattern, and it is one of the most important phenomena affecting the homogeneity of inkjet-printed drops.

Huang et al. studied a series of inkjet printing processes using GO

based inks [114]. In order to restore the conductivity, a reduction step after printing the GO patterns was performed by thermal treatment under Ar/H_2 environment, which allowed to reach conductivity values of $\sim$ 900 S/m in the case of few-layer GO. Inkjet printed inks obtained from liquid exfoliated graphene were produced either in organic solvents such as NMP [115] or ethanol [116] and in water with the aid of a surfactant [115]. Secor and coworkers were able to obtain conductivity values of the printed pattern as high as $2.5x10^4$ S/m after a thermal treatment at 250°C, showing at the same time the compatibility with flexible substrates [116]. Torrisi et al. demonstrated inkjet printing as a viable method for large-area fabrication of graphene devices with on/off ratios up to $\sim 4x10^5$ and conductivity of $\sim 10^2$ S/m [115].

Chapter 2

Experimental

Different types of graphene were found to be suitable for different applications described in this thesis. Graphene applications and their respective production methods are schematically represented in figure 2.1 .

2.1 Fabrication of graphene-based electronic devices

Three types of graphene-based devices have been fabricated and characterized in this thesis: an audio voltage amplifier, cascaded wafer-scale complementary inverters and gigahertz integrated ring oscillators. The first one was obtained using manually exfoliated graphene from HOPG, while in the second and third device CVD graphene was used.

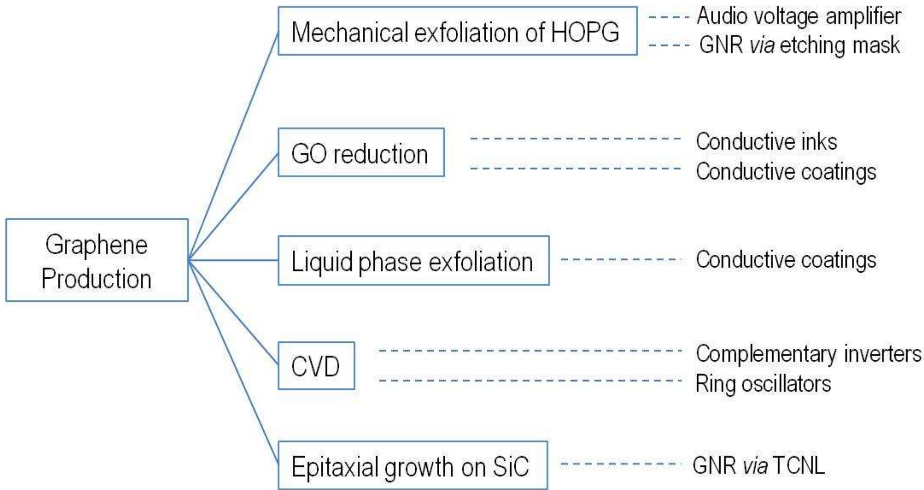


Figure 2.1: Different uses of graphene according to its production methods.

Si/SiO_2 substrates

Highly As-doped (n-type) Si chips have been used, with lateral dimensions of 3.8 mm x 3.8 mm. The bottom side of the chips is covered with metal and serves as contact electrode for the back-gate. The top side is covered with a 300 nm thick SiO_2 layer serving as back gate oxide. A gold marking grid with a spacing of 80 μm was patterned on the top side and divides each chip in 1600 square areas. This grid has a double purpose: addressing the positions of the flakes deposited on the substrate and providing alignment marks for the further lithography step. Each flake, once it has been located, can be labeled with the number of the chip plus a four digit number, indicating the column and the row of the grid to which it belongs. Before graphene deposition (either from HOPG or CVD), chips are cleaned in order to remove the

protective photoresist layer. The standard cleaning procedure consists of an ultrasound treatment of samples in N-ethyl-pyrrolidone (NEP) for 15 mins bath, acetone for 15 mins and isopropanol (IPA) for 10 mins.

Micromechanical cleavage of HOPG

The substrates are pre-heated to 160°C in oven, and then kept on the hot plate at 130°C for 5 minutes. Clean HOPG is exfoliated on 3M Scotch Magic™ tape. The tape is then pressed on another piece of tape in order to make graphite layers thinner. The master tape is pressed on a substrate when it is still hot, and removed carefully, leaving a few graphene layers among graphite residues on chip surface. The substrate is finally washed with IPA and blow-dried under nitrogen flux. Graphene monolayers are then individually localized by optical microscopy.

CVD graphene

Graphene monolayers were grown by chemical-vapor deposition (CVD) on Cu with a CH_4 precursor [117] and then transferred to Si/SiO_2 substrates.

2.1.1 Device fabrication by Electron Beam Lithography (EBL)

EBL is one of the most common top-down technique for micro and nano fabrication. In this technique an electron beam is focused on a

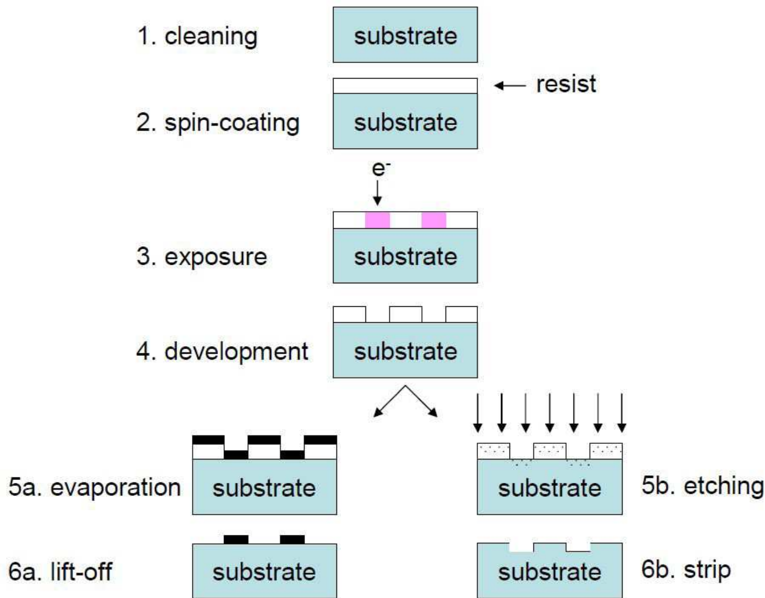


Figure 2.2: EBL process: the design is first transferred to the resist by e-beam exposure and then from the resist to the substrate by material deposition (lift-off 5a-6a) or by etching the substrate not protected by the resist (5b-6b).

polymeric material (resist) writing the desired pattern. Depending on the resist type, the electron beam locally changes the resist property making it more soluble where it has been previously exposed (in case of a positive resist) or less soluble (negative resist). After exposure, the resist is immersed in an appropriate solution that dissolves the more soluble parts (this process is called development). During development the substrate is uncovered in the developed areas. The pattern is transferred to the substrate by evaporation of material and lift-off, or by etching chemically or physically.

A schematic of the EBL process flow is shown in figure 2.2. Deposition of the e-beam resist on a clean chip is the first step. According to the different processes, different resists solutions are used. Each resist solution is characterized by its polymer density and the average lenght of its polymeric chains. Resist is deposited on the chip surface by spin-coating in order to form a uniform coverage. Every spin-coating procedure was performed at a rotational speed of 8000 revolutions per minute (r.p.m.) and was followed by a 1 hour baking at the temperature of 160°C, in order to completely remove the casting solvent.

The second step is the resist exposure by the electron beam. E-beam exposures have been performed in a Philips XL30 FEG SEM, with a Raith Elphy Quantum lithography attachment. The acceleration voltage used in all exposures is 30 kV and the resolution limit of the system is about 10 nm. The e-beam, controlled by pattern generator, scans the resist following the desired pattern previously defined in a CAD program. A standard dose of 330 $\mu C/cm^2$ is used for a positive electron beam resist poly(methyl methacrylate) (PMMA). Smaller areas are patterned with a higher dose to compensate for the smaller quantity of secondary electrons scattered from the surrounding areas. The used beam current varied depending on the structure type. A low current beam electron of 25 pA was used for the exposure of the fine structures, such as the electrodes. A larger beam current of 2.5 nA was used for the exposure of the larger features such as the bonding pads or the connections between the bonding pads and the electrodes.

To develop the PMMA resist after an e-beam exposures, methyl-isobutil-ketone (MIBK) was used. Standard procedure consists in developing the sample for 90 seconds in a MIBK : IPA (1:3) solution and stop the

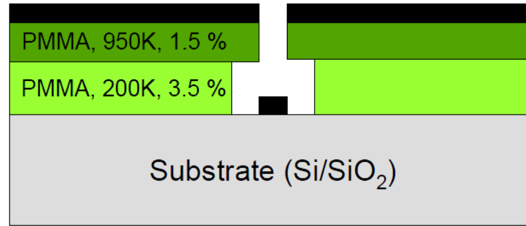


Figure 2.3: PMMA double-layer for lift-off: in order to perform lift-off the upper layer has a higher molecular weight than the bottom layer.

development by rinsing in pure IPA for 1 min.

For lift-off, a double-layer structure is prepared (figure 2.3). The bottom layer is prepared by spin-coating of a dense (3.5 % in solution), short chained (average molecular weight of the PMMA chains: 200000 a.m.u.) PMMA on a substrate. The second layer is prepared by spin-coating of a low density (1.5 % in solution), long-chained PMMA (average molecular weight of the PMMA chains: 950000 a.m.u.). The first and the second layer have an average thickness of 150 nm and 50 nm respectively. The difference in molecular weights of the resist chains gives rise to the typical undercut profile (figure 2.3) that makes easier to perform lift-off.

Metal contacts are evaporated in a Leybold L560E e-beam evaporator. Usually Ti/Au electrodes and Al top gates are evaporated with an evaporation rate of 0.1 nm/s and at an operating pressure lower than $5*10^{-6}$ mbar. The lift-off procedure is performed in a hot NMP bath, at the temperature of 55°C for two hours. The samples are sequentially rinsed first by acetone and then IPA for removing any resist residues.

In the case of CVD graphene, the whole surface of Si/SiO_2 substrates is covered by monolayer graphene. Hence, the first fabrication step

is patterning of graphene channel through a combination of EBL and reactive ion etching (RIE), as represented in step 5b and 6b of figure 2.2. RIE was used to remove unprotected graphene through an oxygen plasma treatment. The reactive gas could be selected between SF_6, CH_4 and O_2. The plasma, developed between two parallel plates, was generated through a 13.56 MHz RF signal.

In the following subsections the detailed configuration is described for each graphene-based device.

2.1.2 Graphene audio voltage amplifier

Graphene FETs were fabricated by exfoliating monolayer graphene from HOPG on conventional Si/SiO_2 substrates. Monolayer graphene flakes were localized by optical microscopy and characterized by AFM and Raman spectroscopy. Figure 2.4 a) shows the schematic configuration for this type of device and b) an SEM image of one of our integrated graphene amplifiers. All contacts were patterned by EBL. The top-gate electrode was firstly patterned and deposited simply by evaporating 100 nm of Al, after which there is a spontanoeous formation of a thin ($\sim$4 nm) AlO_x layer at the interface between graphene and Al [118] by exposing the samples to air. Source and drain contacts, consisting of 5/35 nm of Ti/Au, were patterned in the second step by overlapping the gate and obtaining a complete channel coverage.

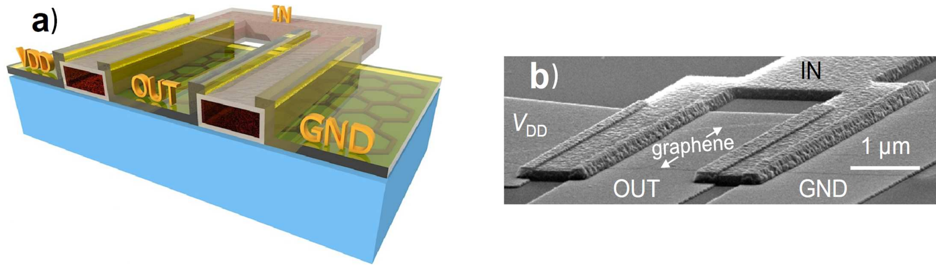


Figure 2.4: Configuration of an integrated graphene audio voltage amplifier. a) A schematic of an amplifier, where source (VDD, GND) and drain (OUT) Ti/Au contacts overlap with gate (IN) Al contacts, which is covered by an insulating AlO_x layer. b) an SEM image of a device recorded from a tilted position. The monolayer graphene flake is marked by the white arrows.

2.1.3 Cascading wafer-scale graphene complementary inverters

Integrated graphene complementary inverters were fabricated from graphene monolayers grown by CVD on Cu and then transferred to conventional Si/SiO_2 substrates. Graphene channels were patterned by EBL and etched by reactive ion etching (RIE). As in case of graphene audio voltage amplifiers, Al top gate contacts were fabricated in the first lithographic step by direct evaporation of 90 nm Al on graphene, with subsequent formation of the thin AlO_x layer. The source and drain contacts (5/35 nm or 2/35 nm of Ti/Au) fabricated in the following step were slightly overlapped with the gate contact in order to completely cover the channel, as shown in figure 2.5 a). The FET channel dimensions were gate length $L = 2$ μm and width $W = 20$ μm. Apart from these, several devices with $L = 1$ μm and 500 nm were also fab-

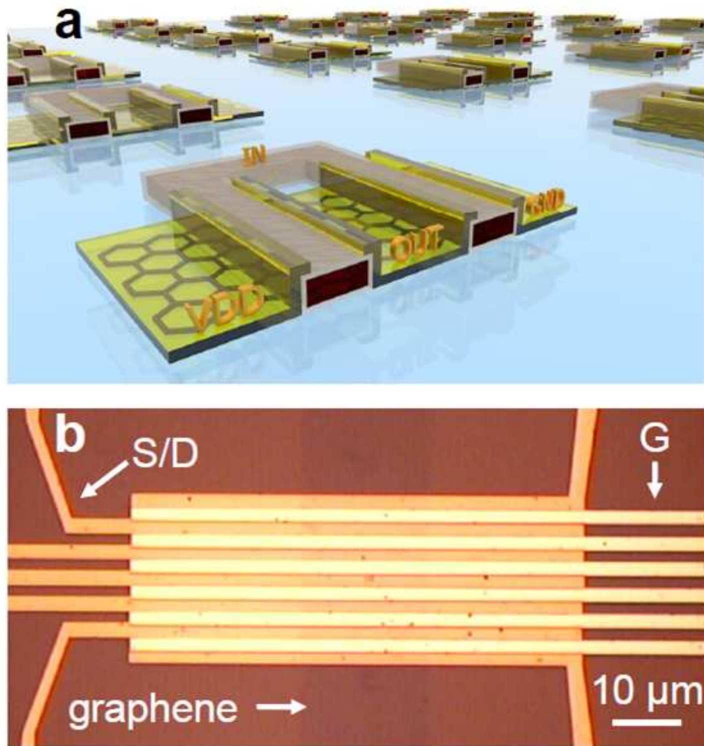


Figure 2.5: Integrated graphene complementary inverters. a) A schematic of a large array of inverters fabricated on wafer-scale graphene. Source (VDD, GND) and drain (OUT) contacts (Ti/Au; yellow) overlap with gate (IN) contacts (Al; red core) covered by an insulating layer (AlO_x; grey shell). b) An optical microscope image of three inverters integrated on the same monolayer graphene channel grown by CVD. The arrows indicate source (S), drain (D), gate (G), and graphene channel.

ricated.

2.1.4 Gigahertz integrated graphene ring oscillators

Graphene ring oscillators (ROs) were fully integrated on the monolayers, as shown in figure 2.6 b). Graphene monolayers were grown by CVD and transferred to Si/SiO_2 substrates. The lithographic steps were the same as described for complementary inverters (2.1.3). Source and drain contacts consisted of Au (75 nm), and the gate was made of Al/Ti/Au (45/2/13 nm). The back of the Si substrates was metalized and used as a global back-gate, if needed. Top gates were fabricated by direct evaporation of Al on graphene and terminated with a thin layer of Ti/Au during the same evaporation step. This approach allowed the formation of ohmic contacts between the gates of one stage and the source/drain terminals of another. All inverters in a single RO have the same access lengths (L_a), gate length (L) and width (W) (see figure 2.6 a)). ROs were fabricated with different L and W, but in all cases the access lengths were kept constant ($L_a = 0.5$ µm).

2.2 RGO conductive coatings

2.2.1 Synthesis of GO

Stable colloidal GO dispersions were produced by modified Hummers method [73]. Graphite flakes (0.5 g, 50 mesh ≈ 300 μm flake graphite

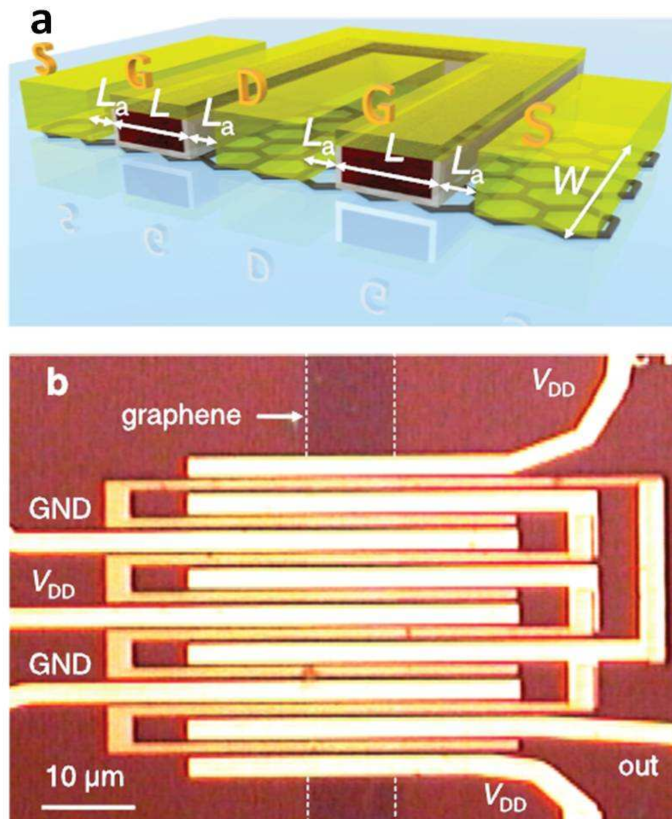


Figure 2.6: Integrated monolayer graphene ring oscillator (RO). a) Schematic of a complementary graphene inverter comprised of two FETs. Source (S) and drain (D) contacts (Au; yellow) are separated by a distance L_a from the gate (G) contact (Al; red core), which is covered by an insulating layer (AlO_x; gray shell) and terminated with a conductive layer (Ti/Au; yellow); b) Optical microscope image of a small RO (L = 1 μm and W = 10 μm) integrated on the monolayer graphene channel grown by CVD. The drain contacts of inverters (Au; bright yellow) overlap with the gate contacts (Al/Ti/Au; orange) in order to form internal connections between the inverters.

from NGS Naturgraphit GmbH) and sodium nitrate, $NaNO_3$, (0.6 g, Sigma Aldrich) were introduced in a round bottomed flask with 23 mL of concentrated sulphuric acid, H_2SO_4 (98%, Sigma Aldrich), and kept under stirring for ten minutes. Potassium permanganate, $KMnO_4$ (3 g, Sigma Aldrich), was slowly added and the mixture was kept under stirring for 6 hours at 35°C. Subsequently 10 mL of DI H_2O were added dropwise, resulting in a rapid rise of temperature (∼80°C) and stopping the oxidation reaction. After 30 minutes at this temperature, 100 mL of DI H_2O and 3 mL of hydrogen peroxide solution, H_2O_2 (30%), must be added in sequence to dissolve the insoluble manganese species. A sudden effervescence was observed and the reaction mixture turns into bright yellow colour.

Once the reaction is terminated the oxidized portion must be separated and cleaned from the unoxidized graphite and all other residual species. By centrifugation one can choose to separate the solid content (unoxidized graphite) or the solubilized metal ions simply selecting the proper centrifugation rate. The first cleaning step was performed by centrifugating (Eppendorf centrifuge 5430) the suspension at 7800 rpm for 30 minutes in order to remove both the acidic content and the ions in solution. The solid content was collected and redispersed with DI H_2O. This procedure was repeated in sequence until the pH of the supernatant rised close to neutrality. At that point the exfoliation of graphite oxide could be performed by prolongated and vigorous shaking, so that GO flakes form a brownish colloidal suspension. Alternatively, ultrasonic bath is often used as means of exfoliation but it reduces the lateral size of resulting GO flakes. The second part of the cleaning procedure was the removal of the solid unoxidized graphite

by mild centrifugation (~2000 rpm for 20 minutes). The subsequent collection of the purified supernatant resulted in stable aqueous GO suspensions.

2.2.2 Reduction of GO films

Chemical reduction by nascent hydrogen

GO acqueous solutions were drop casted onto amorphous glass substrates. After drying on the hot plate at 70 - 80 °C for 15 minutes, the coated substrates were immersed face-down in a Petri dish filled with ammonia solution (NH_3, 13%). The bottom of Petri dish was previously covered with an Al foil, so that the side coated by GO was facing the Al foil. As the reaction takes place, hydrogen bubbling and change in color of the Al foil are observed together with the darkening of GO film, which is an immediate indication of its reduction. After 30 minutes substrate is removed from the reducing solution because of the cessation of hydrogen bubbling. The resulting rGO film is homogeneously darker compared to the starting material. This operation was repeated 3 times on the same samples and after each reduction process the rGO films were characterized by XRD and by measurements of their electrical resistance. The samples were named as follows: GO (pristing GO film), rGO 30' (reduced once), rGO 60' (reduced twice) and rGO 90' (reduced three times).

Reduction by Ar plasma

GO acqueous solutions (10 mg/mL) were diluted with DI H_2O (v/v) at the following concentrations: 1:1, 1:2, 1:3 and 1:4. Each GO solution was drop casted with a micropipette onto pre-cleaned Si/SiO_2 substrates (14x14 mm). A total volume ranging from 140 to 260 µL of GO solution was deposited onto the substrates, which were placed directly on the hot plate set at 80°C. During water evaporation a uniform GO film formed and was left to further dry at 80°C for 20 minutes. The GO films were characterized by AFM and XRD before each reduction step.

GO films were reduced by the following methods: (i) under Ar plasma, (ii) under Ar plasma with H_2 fluxed at 35 sccm and (iii) under vacuum environment only at 100°C (in order to check the effect of removing water molecules intercalated within the GO film). Treatments (i) and (ii) were performed varying the direct current of the plasma between 50 A and 150 A and varying the exposure time between 10 mins and 30 mins. Treatment (iii) was carried out for 90 minutes. After each reduction step, XRD spectra were recorded and the electrical resistivity of the rGO films was measured by van der Pauw configuration.

The system used for these treatments was a low-energy plasma-enhanced chemical vapor deposition (LEPECVD) growth tool. Ar is passed into the plasma source, in which a Ta filament is heated (by an alternating current of ∼130 A) such that electrons are thermionically emitted. A negative dc bias of -20 to -30 V is applied to the filament (with respect to the walls of the chamber and the anode) such that a dc arc of 50 A - 150 A is sustained. Hydrogen could be passed directly into the plasma

chamber, leading to the generation of hydrogen ions and radicals.

2.3 GO inks for inkjet printing

GO inks were produced by a modified version of the method described in 2.2.1. Commercial expanded graphite (2 g) was used as starting raw material and mixed with 6 g $KMnO_4$ and 90 mL H_2SO_4. After 4 hours under vigorous stirring 100 mL of DI H_2O were added to the mixture. After 1 hour the reaction was terminated by adding 300 mL H_2O and 5 mL H_2O_2 (30%). The washing procedure was performed as described in section 2.2.1.

Once a clean GO solution was collected, long ($\sim$ 5 hours) sonication by tip probe was performed in order to reduce the lateral size of GO flakes. This step was needed to satisfy the dimensional requirements of the nozzles of the inkjet printer used in these experiments. The resulting GO dispersion had viscosity of 6 mPas and surface tension of 84 mN/m. Before the printing trials, a non ionic phenol ethoxylate surfactant was added to the GO dispersion (Triton X-100, Sigma Aldrich, with a CMC of $2\text{x}10^{-4}$ mol/L). The dispersion was then diluted 1:1 (v/v) with DI water and filtered with 1 μm sized filters in order to remove larger GO flakes or any possible impurity which may clog the nozzle. The final surface tension of the so-obtained dispersion was 34 mN/m.

The printing trials were carried out using a Dimatix DMP 2831 (Fuji Films) drop-on-demand piezoelectric ink-jet printer which has 16 nozzles with a diameter of 21 μm. Each nozzle was independently activated by a jetting amplitude of 15 V and the drop spacing (center-to-center

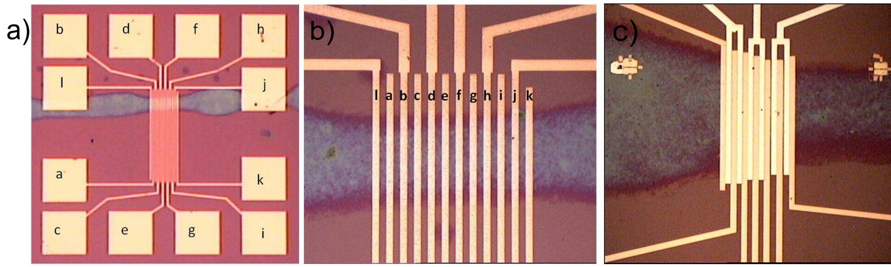


Figure 2.7: Inkjet printing of GO inks. Optical images of a) and b) Ti/Au contacts (yellow) and c) Al top gates (white) between Ti/Au electrodes. All contacts were patterned across the rGO line (light blue) by EBL.

distance) was varied from 10 to 70 μm. In order to reduce the patterns of GO inks, the Si/SiO_2 substrates were annealed after printing by thermal annealing at 400 °C under Ar/H_2 flux for 1 hour.

The electrical characterization of rGO was performed by measuring the electrical resistance and, when possible, the gate dependance. In the case of rGO printed squares the measurements were performed in van der Pauw configuration by placing the probes directly onto the square; rGO printed lines were contacted by Ti/Au (5/50 nm) electrodes and Al top gates (50 nm) patterned by EBL across the line (see figure 2.7).

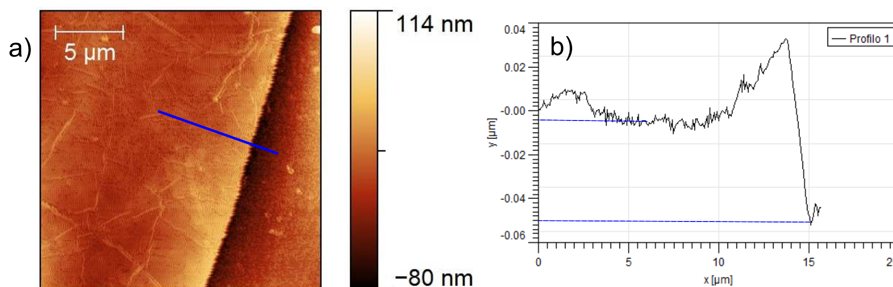


Figure 2.8: a) AFM topography of the GO film; b) step height profile measured along the blue line indicated in a), showing film thickness ∼ 50 nm.

2.4 GO for other applications

2.4.1 GO for thermochemical nanolithography (TCNL)

GO produced as described in section 2.2 was used to demonstrate the possibility to parallelize TCNL for the fabrication of graphene-based nanoribbons. GO colloidal dispersion was diluted with DI water 1:3 (v/v). GO film was prepared by drop casting 20 microliters of diluted GO dispersion on a silicon oxide chip (4x4 mm) and leaving it to dry at 70°C for 15 minutes. The thickness of the film was ∼ 50 nm, measured by AFM (figure 2.8).

TCNL on top of GO film was performed at Georgia Tech Institute as described in reference [119]. Briefly, the thermal tips array used in this project contains five cantilevers with the corresponding nano-tips, as depicted in figure 2.9. Tips are distant 110 μm from each other. Each cantilever in the array is joule-heated and it is individually addressable with a voltage bias, which is used to control the current flowing in the

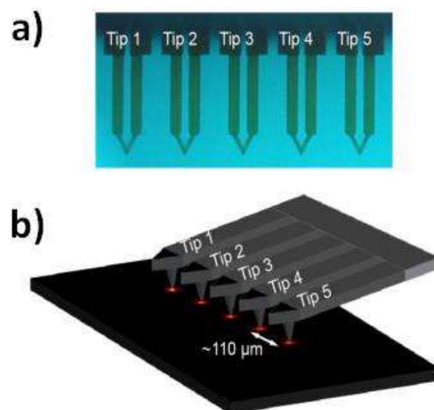


Figure 2.9: a) Optical image and b) cartoon of the five cantilevers and tips array for parallel TCNL. Adopted from reference [119].

cantilever to achieve the joule-heating at the resistive tip.

Each of the five tips was used to pattern four zig-zag conducting rGO lines at four different temperature. Current Sensing-AFM (CSAFM) was used to check the change in conductivity of the patterns, which is indicative for the successful local reduction of GO. Also, the change in surface potential between GO and thermally reduced GO was monitored by Kelvin Probe Force Microscopy (KPFM) to further verify the reduction extent.

2.4.2 Thickness determination of GO flakes

Isolated GO flakes with different thicknesses were deposited by drop casting diluted GO dispersion on top of silicon oxide and Au (13 nm, evaporated on a Si chip) substrates. GO dispersion was produced as described in section 2.2. Several GO flakes has been scanned by AFM

in order to determine their thickness. Subsequently, Auger electron spectroscopy (AES) measurements were performed on the same GO flakes in order to estimate their thickness by exploiting the attenuation of the Auger electrons through the flakes (analyses were performed at Physics department from Politecnico of Milan). The values of GO thickness obtained from the above mentioned techniques were finally compared.

AES analysis of GO samples was carried out with electron beam energy of 10 keV and beam current of 10 nA. A series of images of the flakes which have been measured with AFM before was recorded.

2.5 GNRs for memory devices

The investigated memory devices were comprised of GNR FETs, fabricated on a SiO_2 substrate with an embedded SiN layer (85 nm SiO_2 / 5 nm SiN / 5 nm SiO_2) on top of a highly-doped silicon wafer. The thin embedded SiN layer should act as a charge-trapping center influencing charge carriers in GNRs. The charge trapping is attributed to the presence of silicon and/or nitrogen dangling bonds.

Graphene flakes were mechanically exfoliated from HOPG and deposited onto the substrate. Graphene identification and preliminary characterization were performed through a combination of optical microscopy and AFM. The patterning of GNRs was performed by the use of cadmium selenide (CdSe) nanowires as etching mask deposited on top of graphene flakes.

CdSe nanowires were grown by the solution-liquid-solid method [120].

A dispersion of CdSe nanowires in chloroform was prepared by removing excess trioctylphosphine oxide (TOPO) via centrifugation and subsequent redispersion in the pure solvent, which was repeated two times. The CdSe dispersion was then drop-casted onto the whole chip surface placed on a hotplate at 50°C. Afterwards, the substrates were rinsed with chloroform for 15 s in order to remove excess of CdSe fibers and remaining TOPO. Subsequently, they were heated under argon atmosphere at 120°C for 10 minutes with the aim of improving the adhesion between the CdSe wires and graphene. The deposited nanowires could be found as single fibers - which have cylindrical section and diameter ranging between 10 - 35 nm, or as a bunch, while their length could range from 1 to 10 μm. Optical microscopy and AFM were used to assess the exact position and dimension of the CdSe nanowires with respect to the flakes and to select fibers with a diameter smaller than 40 nm, in order to achieve a substantial increase of the on/off ratio in graphene transfer curve (see figure 2.10).

In the following step, electrical contacts were patterned on top of CdSe nanowire/graphene stack. The AFM image of the stack is carefully overlapped with the optical image, which is then used to design and to align the contacts (see figure 2.11), patterned by EBL. The contacts, deposited in an e-beam evaporator, are made of Ti/Au (5/50 nm). The electrodes width ranges between 200 - 300 nm, and they are separated by 100 - 300 nm, depending on the overlapping area between graphene and the CdSe fiber. The final step is related to the morphology transfer between CdSe nanowire and the graphene flake. To this end, a 5 seconds oxygen plasma (by RIE), at 48 W and a pressure of 0.05 mbar is performed to remove the unprotected graphene,

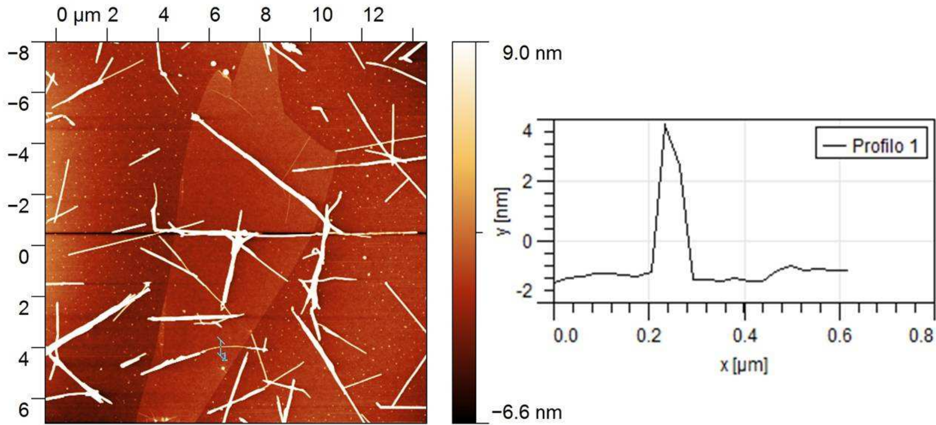


Figure 2.10: AFM topography image of CdSe nanowires partially covering monolayer graphene. Nanowires height was measured at the position of the blue bar, with the height profile along the bar shown on the right.

leaving GNRs under the CdSe nanowires. The CdSe nanowires were not removed for transport and memory measurements, as this would have required a wet chemical treatment with aqua regia, which is able to dissolve gold contacts. A different procedure to obtain GNRs from CdSe nanowires etching mask had been attempted, i.e., oxygen plasma before contact deposition, but this resulted in the complete destruction of all graphene channels.

The electrical behavior of the fabricated devices was evaluated in three different stages: firstly, graphene transfer curves (drain current I_{D} vs. gate-source voltage V_{GS}) were acquired before the oxygen plasma treatment, to evaluate the Dirac point offset and the starting on/off ratio of the channel. Secondly, the same characteristics were recorded after etching, i.e. once GNRs were realized, to verify the increase in the

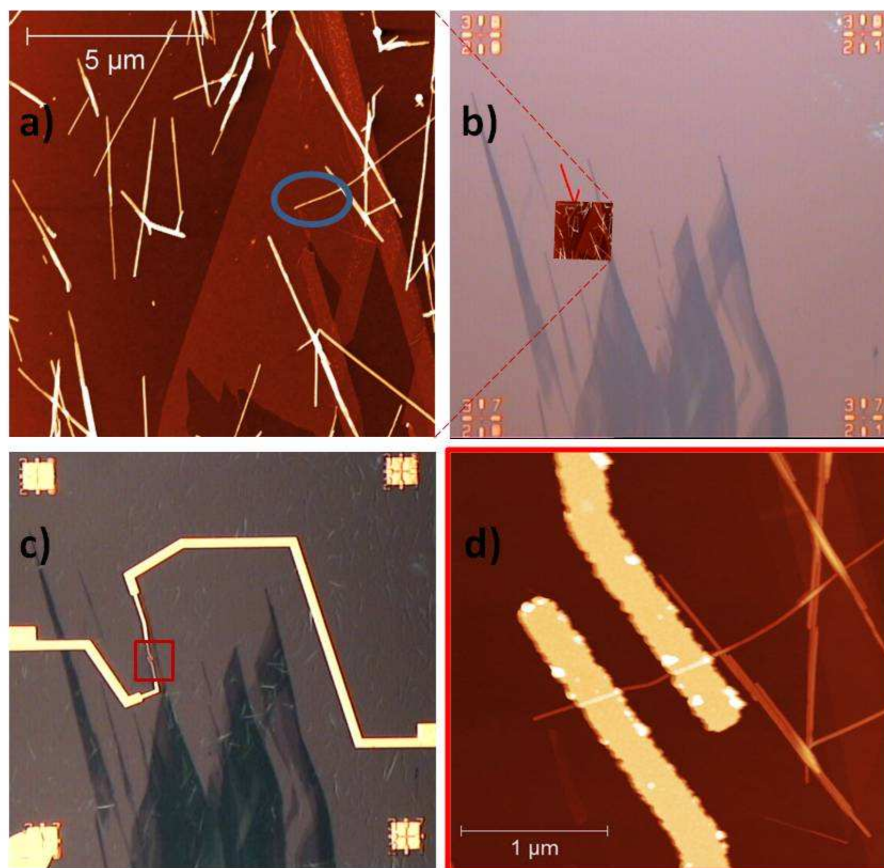


Figure 2.11: GNRs fabrication steps. a) AFM scan of deposited nanowires on top of graphene; the blue circle indicates the nanowire selected for patterning Ti/Au contacts. b) Overlapping of the AFM image on top of optical image in order to allow the correct alignment of the electrodes. c) Optical image after lift off of metal contacts (yellow) and d) AFM scan of the interested area after graphene etching.

on/off ratio. Finally, memory measurements with gate voltage pulsing were performed.

2.6 Characterization techniques

Optical Microscopy

After graphene deposition onto Si/SiO_2 substrates, the chips are manually scanned with an optical microscope. In the case of manually exfoliated graphene the primary step is localization of graphene monolayers. In case of CVD graphene the optimal region for etching graphene channels must be optically selected. Also, optical images were taken after each lithographic step. In this work, Leica DMR optical microscope with a JVC TK-C1380 color digital video camera was used. The microscope is equipped with various color filters.

Atomic Force Microscopy

After characterization by optical microscopy, samples are usually characterized by AFM. With this technique it is possible to measure the thickness of the graphene flakes or films and to have a detailed topography of their surface. Atomic force microscope Veeco 3000 has been used under ambient conditions. Since the AFM tip can damage the flakes in contact mode, all the measurements were performed in the tapping mode.

Scanning Electron Microscopy

Sometimes it has been useful to perform detailed imaging by SEM too. The instrument used in this thesis was Philips XL30 SFEG SEM with a Raith Elphy Quantum lithography attachment.

X-ray diffraction

X-ray diffraction measurements were conducted using both powder and thin-film diffraction procedures. Powders were smear-mounted onto an adhesive tape pasted on the zero-background quartz substrate, while other substrates coated with the film to be analyzed were mounted on the sample holder with the help of two magnets. A PANalytical X'Pert PRO high-resolution triple-crystal diffractometer was used, with Cu Kα1 radiation (λ= 0.1540562 nm) selected by a two-bounce hybrid Ge(220) monochromator and mirror. A three-bounce symmetrical Ge(220) monochromator was used as an analyser crystal in front of the Xe proportional detector.

2.7 Electrical characterization

2.7.1 Electrical resistance

Simple electrical resistance measurements were performed in a probe-station (single and multi probes) connected to a digital sourcemeter either in two-probe or four-probe (including van der Pauw) configurations. The four-probe configuration allows to extract the resistivity

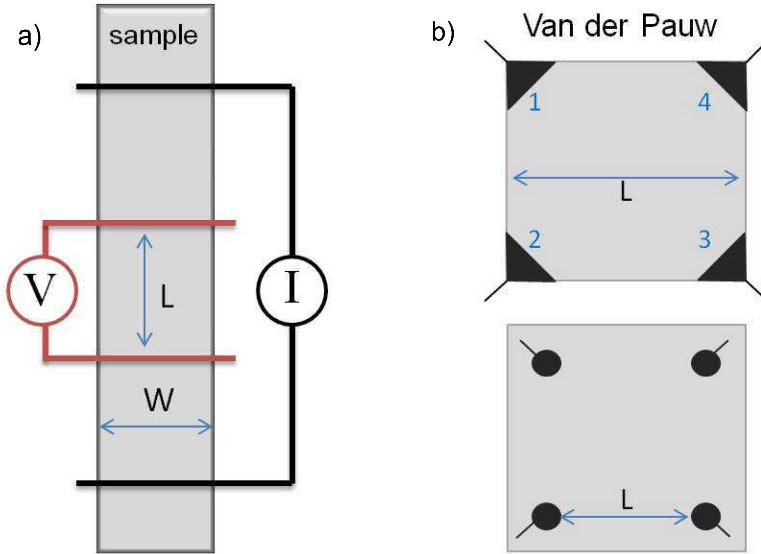


Figure 2.12: Simple resistance measurement. a) In four-probes configuration the positive dc current, I, is injected through the external electrodes (black). The voltage V is a dc voltage measured between the two internal contacts. In order to calculate sample resistivity the lenght (L), width (W) and thickness (t) of the measured area must be known. b) In van der Pauw configuration the four contacts can be placed at the corners or in the middle of the sample. The lenght (L) and thickness (t) of the squared area to be measured must be know.

of the sample without including the resistance of cables and contacts, and it requires the presence of four conductive electrodes (or probes) on the sample, as shown in figure 2.12.

When the sample has the shape of a thin line it is prefereable to measure it by placing the four electrodes directly in series, as shown in figure 2.12 a). When the sample to be measured is square-shaped or more in general it is a film where it would be difficult to fully cover

the interested area by four electrodes in series, it can be measured by van der Pauw method. The contacts are numbered from 1 to 4 in a counter-clockwise order, beginning at the top-left contact as shown in figure 2.12 b). The current I_{12} is a positive dc current injected into contact 1 and taken out of contact 2. The voltage V is a dc voltage measured between contacts 3 and 4. It is possible to measure all four configurations (where the current is injected through I_{12}, I_{23}, I_{34} and I_{41}) in order to obtain a more precise value of the sample sheet resistance, R_s.

2.7.2 Device dc-ac characteristics

Field effect measurements are performed at fixed source-drain voltage V_{D}, while the voltage applied to the gate V_{G} is slowly swept from negative to positive values, recording the flake resistance as a function of V_{G} (as shown in figure 2.13). The resistance of graphene shows the classical bell-shaped dependence from V_{G}, with the maximum value at the Dirac Point. These measurements allow to extract the on/off ratio of the device, i.e. the ratio between current in the on state and in the off state. The supply voltage V_{D} shifts the Dirac point. As V_{D} is increased, the current minimum shifts to more positive values accordingly. This phenomenon is explained by the fact that when V_{D} is increased, the potential in the channel increases, reducing the effective potential difference between the gate and channel. As a result the V_{G} should be increased by about $1/2V_{\mathrm{D}}$ to reach the Dirac point. Thus, the position of the Dirac point can be tuned by V_{D} in an individual FET.

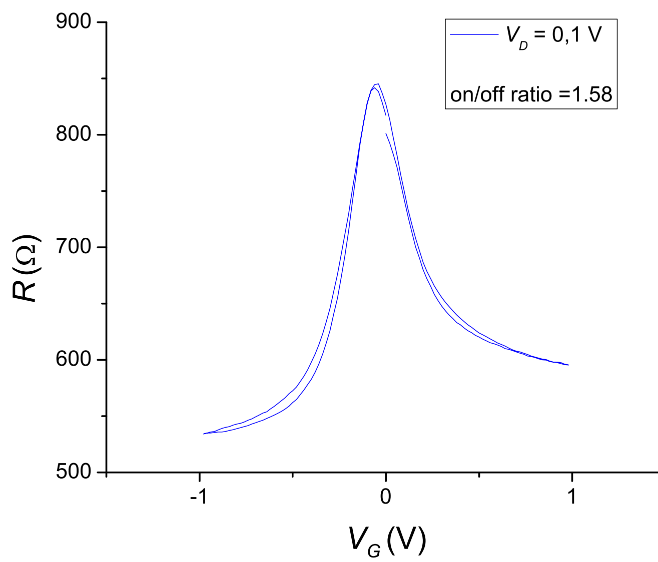


Figure 2.13: Typical transfer curve of a graphene FET.

When two adjacent working transistors are patterned on the same flake, it is possible to obtain an inverter, as shown in figure 2.14 a). The characterization of an inverter mainly consists in measuring the voltage at a common output V_{OUT}, as a function of the input voltage applied to the top gate, V_{IN}, to determine the voltage gain A_{V}. When the FETs are biased with the same voltage, their Dirac point are equal. By connecting the source of FET2 to V_{DD} and the source of FET1 to the ground, the Dirac point splitting forms along the axis of the input voltage V_{IN} and the complementary operation is then achieved between the Dirac points (figure 2.14b). In this region, the increase of V_{IN} cause the resistance R_2 of G_2 to increase (p-type behaviour), and the resistance R_1 of G_1 to decrease (n-type behaviour), resulting in a large rate of decrease of the output voltage $V_{\mathrm{OUT}} = V_{\mathrm{DD}} = (1 + R_2(V_{\mathrm{IN}})/R_1(V_{\mathrm{IN}}))$ as the input voltage V_{IN} is increased (figure 2.14c). The derivative of V_{OUT} as a function of V_{IN} corresponds to the voltage gain $A_{\mathrm{V}}= dV_{\mathrm{OUT}} \ / \ dV_{\mathrm{IN}}$.

Graphene FETs dc characteristics were measured by Keithley sourcemeters (2611) and multimeters (2000) controlled by a custom-built Labview routine. The ac measurements were performed by applying input ac/dc voltages from a Tektronix AFG 3022B function generator to the common top gate of inverters, while keeping V_{DD} fixed. Input and output voltage signals were measured by an Agilent infiniium 54832D mixed-signal oscilloscope and Agilent Infiniium DS09064A (banwidth 600 MHz) and DSO9254A (2.5 GHz) digital storage oscilloscopes. In order to minimize the parasitic capacitive load of the ROs, the outputs were connected to the oscilloscope *via* Agilent N2795A (bandwidth 1 GHz, capacitance 1 pF), N2796A (2 GHz), and 1158A (4 GHz, 0.8 pF)

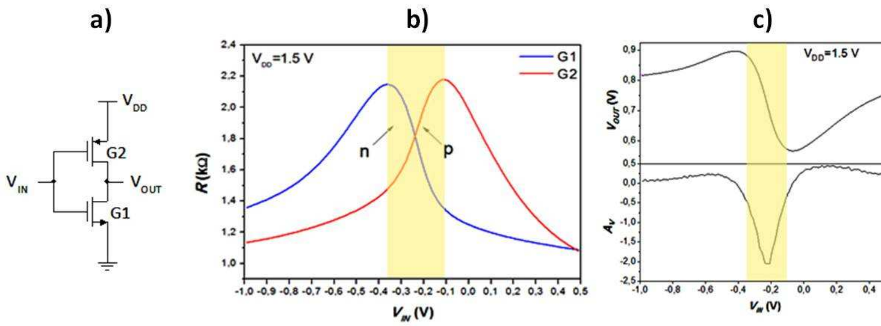


Figure 2.14: Graphene FETs characteristics. a) Circuit diagram of an inverter. b) The application of V_{DD} to G2 causes a splitting of the Diract points of the FET pair along the input voltage axis. c) Voltage inversion can be achieved in the region between the Dirac point of the two FETs (shaded in yellow), in this case corresponding to -0.37V $< V_{\mathrm{IN}} <$ -0.1V for V_{DD}= 1.5V. The measured dc voltage transfer characteristics are represented by the output voltage V_{OUT} and voltage gain $A_{\mathrm{V}} = dV_{\mathrm{OUT}} \,/\, dV_{\mathrm{IN}}$ as functions of the input voltage V_{IN} at T = 300 K.

active probes.

2.7.3 Memory measurements

This type of electrical measurements were performed only on devices fabricated from GNRs, as shown in figure 2.15 a). The triggering is performed by applying a bipolar pulse signal through the Si back-gate, whose magnitude and duty cycle are adjustable to reach well-distinguished memory states while keeping constat the drain voltage V_{D}. The drain current I_{D} values is recorded as a function of time in order to visualize the “on” (high I_{D}) and “off” (low I_{D}) states of the device, as depicted in figure 2.15 b).

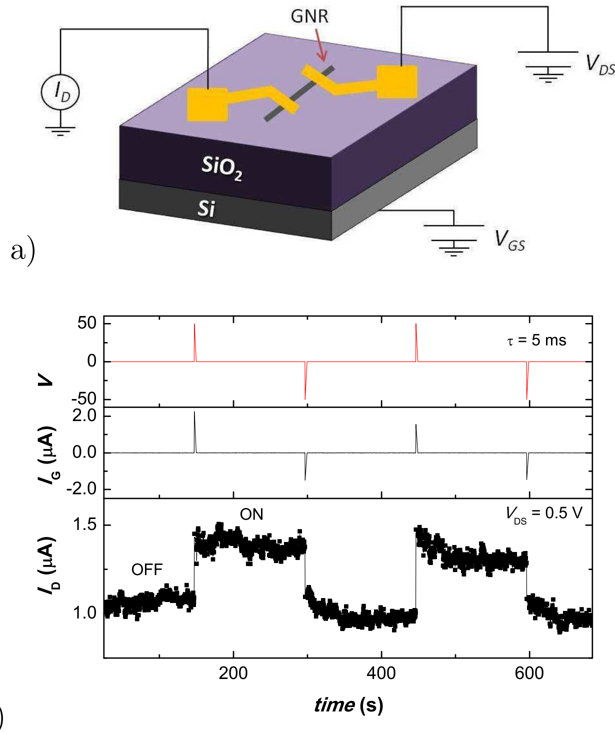


Figure 2.15: Schematic of GNR memory cell in conventional FET configuration used in memory effect measurements. a) A fixed drain-source voltage V_{DS} is applied to one of the two Ti/Au contacts (yellow), while the drain current I_{D} is measured through the other contact. Bipolar pulses are applied through the Si back-gate. b) Switching of the GNR device by a trigger signal with an amplitude of 50 V and pulse duration of $\tau = 5$ ms (top graph); I_{D} vs time is shown (bottom graph), indicating the device switching from the on (high I_{D}) to the off (low I_{D}) state. The gate current I_{G} is also reported (central graph).

Chapter 3

Results and Discussion

3.1 Graphene-based electronic devices

3.1.1 Graphene audio voltage amplifier

The main building block of analogue electronics is a voltage amplifier: an electronic device capable of amplifying small alternating current (ac) voltage signals. The low-frequency ac voltage gain can be determined in the direct current (dc) operating mode, as the derivative of the output voltage with respect to the input voltage:

$$A_{\mathrm{v}} = \frac{dV_{\mathrm{OUT}}}{dV_{\mathrm{IN}}}$$

In the transfer curve V_{OUT} vs. V_{IN} of the circuit, voltage gain is represented by the slope of the plot at each operating point Q (figure 3.2 a). An electronic circuit is an amplifier if $\mid A_{\mathrm{v}} \mid > 1$ (0 dB); it is

important to note that almost all electronic circuits, both analog and digital, need $| A_v | > 1$.

Graphene FETs were fabricated by exfoliating monolayer graphene from HOPG on conventional Si/SiO_2 substrates. The complete graphene channel coverage was obtained by overlapping the AlO_x/Al gate with source/drain contacts, as described in the experimental part (section 2.1.2). A similar full-channel coverage exists in conventional Si metal-oxide-semiconductor FETs and allows maximum drain current modulation as there are no ungated parts of the channel that contribute to fixed series resistances which reduce the voltage gain. The AlO_x layer which forms on the surface of the Al gate prevents short circuits between the contacts. The gate also serves as an additional heat sink which allows high drain currents I_D and consequently high voltage gain A_V. Additionally, as the gate fully covers the channel, desorption of adsorbates from graphene is suppressed at high drain currents, and therefore the electrical properties of FETs are stable during operation.

Two graphene FETs (G1 and G2) were integrated in a complementary configuration (figure 3.1 a), i.e. by patterning the two FETs in series on top of the same graphene flake so that FET G2 loads FET G1. The amplifier was realized by connecting the source of G1 to ground (GND), the source of G2 to a supply voltage V_{DD}, and the output (OUT) to the common drain of the FETs. As fabricated, both FETs G1 and G2 in a complementary amplifier are identical. On the application of the supply voltage $V_{DD} > 0$ the potential of the graphene channel in G2 increases with respect to that of G1, which therefore shifts the Dirac point of G2 to higher input voltages. Figure 3.1 b) shows resistances of transistors G1 and G2 measured at a very small and very large

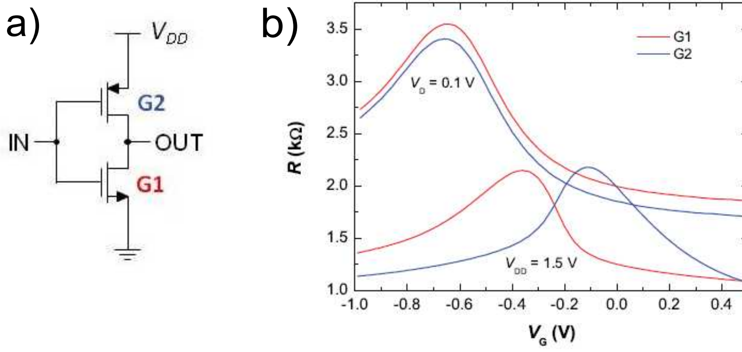


Figure 3.1: a) Simplified circuit diagram of a graphene amplifier. b) Resistances of G1 and G2 at different drain biases. At small bias (V_D = 0.1 V) the resistances were measured separately in two-probe configurations ($R = V_D/I_D$). At large bias (V_{DD} = 1.5 V) resistances were measured in a complementary configuration as $R_1 = V_{OUT}/I_D$ and $R_2 = (V_{DD} - V_{OUT})/I_D$. Resistances in a complementary configuration are lower as measurement of V_{OUT} by a voltmeter eliminates the contact resistance of the common drain od the FETs.

bias. At very small bias the transistors have identical transfer curves. At a large bias the Dirac points of both FETs move to higher input voltages, whereas the Dirac point of G2 moves more compared to G1. Complementary operation is obtained between the Dirac points of the two FETs, where the increase in input voltage ν_{IN} causes the resistance R_2 of G2 to increase and the resistance R_1 of G1 to decrease. This results in a large rate of decrease of the output voltage ν_{OUT} as the input voltage ν_{IN} is increased, and doubles the voltage gain A_v with respect to a resistive-load amplifier in which G2 is replaced by a fixed resistor.

Figure 3.2 a shows the transfer curve ν_{OUT} vs ν_{IN} of the amplifier for V_{DD} = 1.5 V. The largest value of the voltage gain $| A_v |_{max} = 2.1$ for

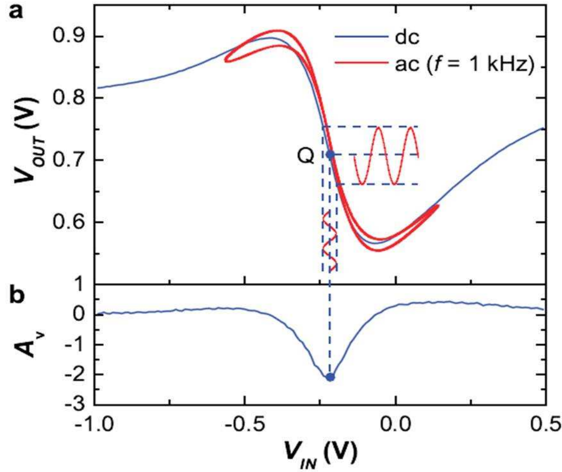


Figure 3.2: Principle of voltage amplification. **a**, Static (dc) transfer curve V_{OUT} vs. V_{IN} of the amplifier is shown in blue. Dynamic (ac) transfer curve is shown in red and was obtained by plotting output voltage ν_{OUT} vs. input voltage $\nu_{\mathrm{IN}} = V_{\mathrm{IN}} + V_{\mathrm{in}} \sin(2\pi f t)$, where V_{IN} = - 0.22 V, V_{in} = 0.35 V and f = 1 kHz. Both dc and ac curves were measured for $V_{\mathrm{DD}} = 1.5$ V. **b**, Low-frequency voltage gain $A_{\mathrm{V}} = dV_{\mathrm{OUT}}/dV_{\mathrm{IN}}$.

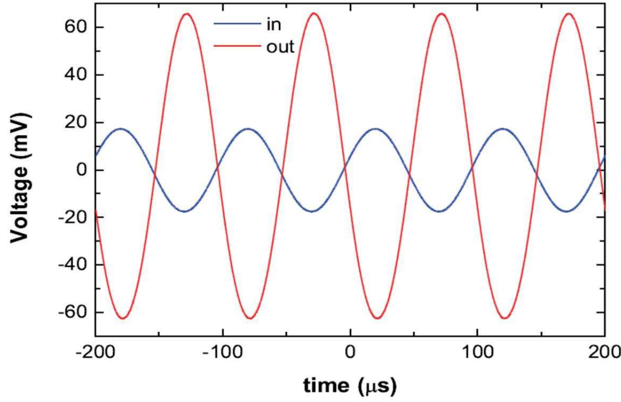


Figure 3.3: Ac components of the input and output voltage signals at a frequency f = 10 kHz for V_{DD} = 2.5 V. The voltage gain is A_{v} = -3.7. The dc components of the signals are V_{IN} = 0.15 V and V_{OUT} = 1.15 V.

this supply voltage is obtained at the dc operating point Q (figure 3.2 b).

Figure 3.3 shows measured ac components of the input and output voltage signals of the amplifier biased at V_{DD} = 2.5 V. At this supply voltage a maximum voltage gain of -3.7 was measured at an input frequency f of 10 kHz. Since the drain current density at the operating point Q is I_{D}/w ∼0.26 mA/µm, which is about 5 times smaller than the breakdown current density of exfoliated graphene, even higher gain could be obtained at higher supply voltages without risking damage to graphene channels. Signals shown in figure 3.3 confirm that high voltage gain is preserved in ac mode, which is attributed to the absence of gate hysteresis (see also 3.2 a) due to the full-channel coverage by the gate which partially screens water charge traps adsorbed on the substrate.

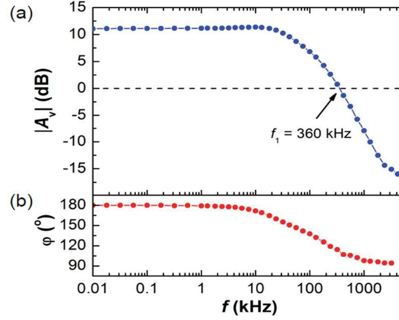


Figure 3.4: Frequency response of the amplifier biased at V_{DD} = 2.5 V. a) Magnitude $\mid A_{\mathrm{v}}(f) \mid$ of the voltage gain. b) Phase shift $\varphi(f)$ between input and output signals introduced by the amplifier.

The frequency response of the fabricated amplifier in the frequency range $f < 5$ MHz is shown in figure 3.4. The amplifier is biased at $V_{\mathrm{DD}} = 2.5$ V which gives the maximum signal amplification $\mid A_{\mathrm{v}} \mid_{\mathrm{max}}$ $= 3.7$ (11.4 dB). The gain remains constant up to about 20 kHz, and then decreases as the frequency increased. The amplifier is capable of signal amplification up to a unity-gain frequency $f_1 = 360$ kHz. At this frequency, the amplifier operates as a unity-gain amplifier (buffer), while for $f > f_1$ it attenuates the input signal.

3.1.2 Complementary integrated graphene inverter

In this experimental project, which arised as an improvement of the results obtained with exfoliated graphene for voltage amplification (section 3.1.1) and its scaling up, the inverter architecture has been implemented on wafer-scale graphene. The building block of the circuit architecture which allowed the demonstration of cascading of graphene

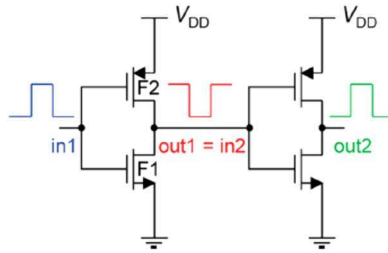


Figure 3.5: A circuit diagram of two cascaded inverters. The output (out1) of the first inverter (comprised of FETs F1 and F2) is connected to the input (in2) of the second inverter.

logic gates is a GFET, where graphene is implemented as conductive channel. An integrated graphene complementary inverter is composed of two graphene FETs (F1 and F2) connected as described in figure 3.1 a). The cascading is then performed between two different inverters, whereas the output of the first stage is connected to the input of the second stage (figure 3.5).

Importantly, here the fabrication of graphene inverters has been carried out on a wafer-scale, using chemical vapour deposited (CVD) graphene films. The use of CVD graphene, together with the development of lithography procedure to self-align the structures across the three main fabrication steps, make possible to realize up to 54 FETs on a single chip, divided in 9 structure, each of which composed of 3 inverters integrated on the same graphene channel, as showed in figure 2.5 b.

As in case of graphene audio voltage amplifiers, the FETs described here do not have ungated parts of the channel due to the overlap of Ti/Au contacts with the AlO_x/Al top gate. This maximizes the gate voltage control over the drain current. As the gate fully covers the

channel, the graphene is partially screened from water charge traps adsorbed on the substrate such that gate hysteresis is suppressed. The gate also serves as an additional heat sink allowing high drain currents and consequently higher voltage gain. This also reduces the influence of atmospheric contaminants during high-current operation such that the electrical properties of the FETs are stable. The Al oxide layer which forms on the whole aluminum electrode surface also prevents short circuits between the top-gate and the source/drain contacts (despite overalp, gate leakage was found to be negligible).

As fabricated, both FETs F1 and F2 in each inverter are identical. In the configuration shown in figure 3.5, the output voltage is given by: $V_{\mathrm{OUT}} = V_{\mathrm{DD}} \ / \ (1 + R_2/R_1)$, where R_1 and R_2 are the resistances associated with the graphene channels of F1 and F2, respectively. The two FETs change into complementary types (F2 into p- and F1 into n-type) after the supply voltage $V_{\mathrm{DD}} > 0$ is applied. Under bias, the potential of the graphene channel in F2 increases with respect to that of F1, which therefore shifts the Dirac point of F2 to higher input voltages. Complementary operation is obtained between the Dirac points of the two FETs, where the increase in the input voltage V_{IN} causes the resistance R_2 of F2 to increase and the resistance R_1 of F1 to decrease. The highest voltage gain is reached at the dc operating point that lies approximately halfway between the Dirac points of the two FETs. All the fabricated FETs were found to show a positive voltage V_0 at the Dirac point in air, if unbiased; this offset stems from a p-type doping which is commonly present in graphene devices, and it derives from ambient impurities adsorbed on graphene prior the fabrication. For this reason, the dc components of the inpunt and output voltages

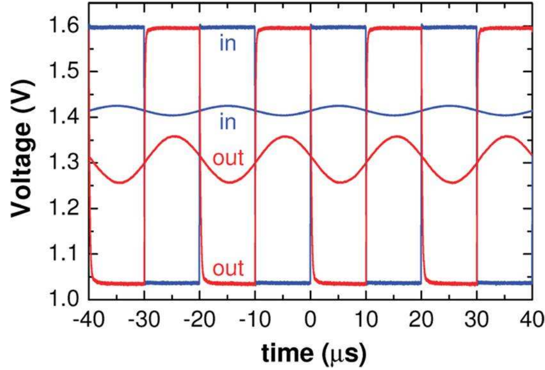


Figure 3.6: Analogue and digital waveforms measured at the input and output of a typical graphene inverter under ambient conditions at a voltage supply V_{DD} = 2.5 V and frequency f = 50 kHz. Sine waveform signals were measured at the highest-gain point at which there is a mismatch of V_0 = 0.11V between the dc components of the signals. The amplitude of the output sine wave is 4.7 times larger than the amplitude of the input sine wave; hence A_{v} = -4.7. Digital waveforms were measured at the dc operating point at which there is no in/out dc signal mismatch. The largest input voltage swing $V_{\text{IN,p-p}}$ = 0.56 V at which the signals are matched is used.

at the highest-gain point in inverter biased with negligibly small V_{DD} are $V_{\text{IN}} = V_0$ and $V_{\text{OUT}} = 0$, where V_0 is the voltage at the Dirac point of the unbiased FETs. As the supply voltage V_{DD} is increased, these two dc components shift by V_{DD} / (1 + α) to $V_{\text{IN}} \approx V_0$ + / (1 + α) and $V_{\text{OUT}} = V_{\text{DD}}$ / (1 + α) due to circuit symmetry. Here α is the ratio of transistor resistances at $V_{\text{IN}} = 0$ (typically $\alpha = 1$) [121]. Hence, V_{IN} - $V_{\text{DD}} = V_0$ represents a mismatch between the input and output dc components at the highest-gain point. This is illustrated in figure 3.6, which shows measured ac input and output signals of an inverter biased at the highest-gain point for V_{DD} = 2.5 V. The signals

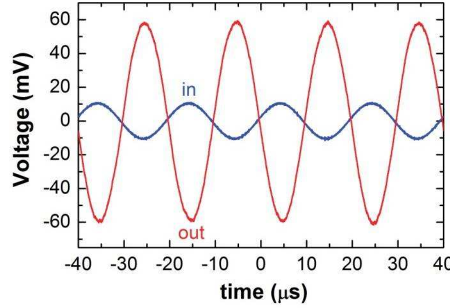


Figure 3.7: Ac components of the input and output voltage signals measured in graphene inverter at ambient conditions at a frequency f = 50 kHz for V_{DD} = 2.5 V, where A_{v} = -5.3.

are offset by $V_0 \approx 0.11$ V. In addition, it was found that V_0 is stable in air at room temperature without hysteresis present, which confirms the good quality of the devices and the protective effect of the top gate.

The largest value of the ac voltage gain in air was found to be A_{v} = -5.3 at V_{DD} = 2.5 V (see figure 3.7). Overunity voltage gain is a prerequisite for signal matching; otherwise, the voltage swing at the output is smaller than at the input. The good voltage gain is obtained here in the fabricated FETs due to a combination of factors including full-channel gating, thin gate oxide (leading to good control of the top-gate over the channel), good mobility, low output conductance, and manageable contact resistance (for the ~1 μm channel lengths explored here). Nevertheless, we note that all of the above can continue to be optimized, yielding further improvements of graphene inverters and amplifiers in future work.

Voltage gain greater than one is essential to obtain signal matching, since the output voltage swing must not be smaller than the input

swing. Digital signals are defined by two well distinguished logic state (Boolean 0 and 1), and signal matching implies that the peak-to-peak value (or swing) of the input voltage ($V_{\mathrm{IN,p-p}}$) is the same as the output swing ($V_{\mathrm{OUT,p-p}}$). Importantly, this swing should be large enough to be reliably detected. The impact of voltage gain on signal matching is exemplified in figure 3.8, where the dependence of the voltage gain of an inverter on the supply voltage V_{DD} is shown (section 3.1.1). The maximum swing $V_{\mathrm{IN,p-p}}$ at which $V_{\mathrm{IN,p-p}} = V_{\mathrm{OUT,p-p}}$ (signal matching condition) can be determined from the intersection between the transfer curve and a unity-gain line passing through the highest-gain point Q (figure 3.8 a). From these plots, it is clear that high voltage gain (large V_{DD}) are required to obtain signal matching with the proper swing. The largest value of voltage gain under ambient conditions was typically found to be A_{v} = -5 for $V_{\mathrm{DD}} = 2.5$ V (figure 3.8 b).

Figure 3.6 also shows input and output digital voltage signals of an inverter biased with$V_{\mathrm{DD}} = 2.5$ V at an input signal frequency f = 50 kHz. The output signal takes the same logic voltage levels as the input signal (signal matching), thus allowing inverters to be cascaded which is a key prerequisite in digital electronics. At this supply voltage, the maximum in/out voltage swing is $V_{\mathrm{OUT,p-p}} = V_{\mathrm{IN,p-p}} = 0.56$ V or nearly 22 times the thermal voltage V_{T}, which is large enough for logic states to be unambiguously resolved from one another by the next logic gate.

Demonstration of in/out signal matching does not necessarily imply successful cascading of graphene inverters in realistic applications. Cascading of logic gates is one of the most important tasks in realistic and

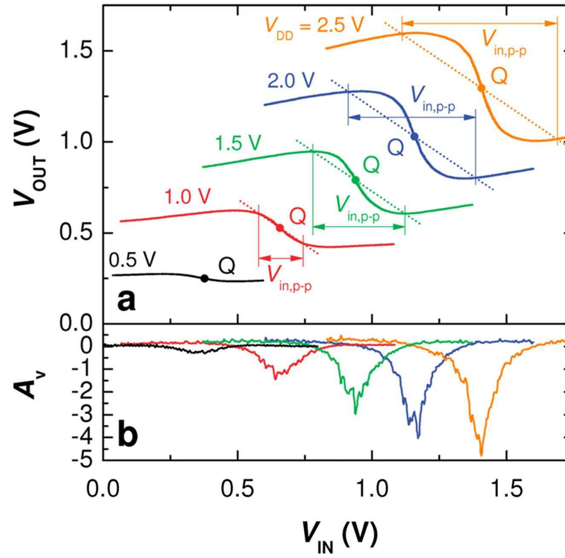


Figure 3.8: Dc characteristics of a graphene inverter under ambient conditions. a) Transfer curves of an inverter at different supply voltages. The highest-gain point at each supply voltage is denoted by Q. The maximum input voltage swing $V_{\mathrm{IN,p-p}}$ at which input and output signals are matched ($V_{\mathrm{OUT,p-p}} = V_{\mathrm{IN,p-p}}$) is determined by the intersections between the transfer curve and a unity gain line (slope of -1) passing through Q. b) Dc voltage gain A_{v} of the same inverter at different supply voltages.

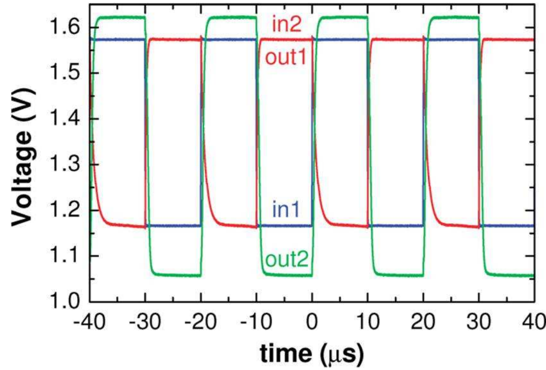


Figure 3.9: Digital waveforms measured under ambient conditions in a cascade connection of two graphene inverters (connected as in figure 3.5). The supply voltage is $V_{\rm DD} = 2.5$ V and frequency $f = 50$ kHz.

complex digital electronic circuits. This implies that the output signal of the first stage is able to drive the input of the following stage. Because of remaining fabrication challenges of graphene, two randomly selected inverters usually do not have identical transfer characteristics, i.e., their highest gain operating points Q1 and Q2 are not the same. As a consequence, it is not possible to bias two inverters such that both of them operate at their highest-gain points. However, we found that a mismatch in the positions of the highest gain points can be compensated if the gain of the inverters is large enough (typically $\mid A_{\rm V} \mid > 3$), which leads to successful cascading. Figure 3.9 shows input and output voltage signals of two inverters, where the first inverter (1) clocks the second one (2); i.e., the output of inverter 1 is connected to the input of inverter 2 as shown in figure 3.5. The signal matching in figure 3.9 was obtained at the dc operating point which lies between the highest-gain points Q1 and Q2 of the two inverters. As both inverters exhibit high gain (here $\mid A_{\rm V} \mid > 4$) at their points Q1 and Q2, they preserve

the over-unity voltage gain between these two points, and consequently the gain was maintained on making the cascade connection, resulting in the same logic states 0 and 1 of all signals shown in figure 3.9. The final low (high) logic state is correctly interpreted as 0 (1) because its voltage level is below (above) the voltage level of the same state at the input. Such small mismatches between the voltage levels in graphene inverters are expected because the saturation voltage levels in graphene inverters are not well-defined. However, this does not influence operation of the cascaded graphene logic gates, as high gain prevents the appearance of intermediate voltage levels (between the high and low levels set by the input) during the propagation of the digital signal.

3.1.3 Gigahertz integrated graphene ring oscillators

Logic gates, as almost all electronic circuits, require FETs with intrinsic voltage gain $A_{\mathrm{v}} = g_{\mathrm{m}}/g_{\mathrm{d}} > 1$, where g_{m} is transconductance and $\mathrm{g_d}$ is output conductance. Voltage gain larger than unity is needed in logic gates in order to match their input and output signals. Matching allows cascading of logic gates and realization of more complex, realistic circuits, of which the most important class are digital ring oscillators (ROs). ROs are composed of an odd number of inverters (each with two FETs) cascaded in a loop. The loop makes the RO unstable and therefore induces oscillation at higher frequencies, but only if the inverters satisfy stringent criteria. Each inverter in the loop must be identical, exhibiting overunity voltage gain and in/out signal matching. Moreover, the two FETs in each inverter must exhibit very

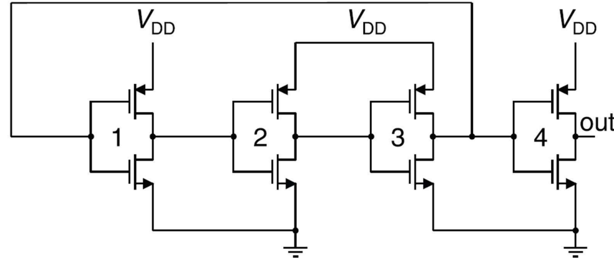


Figure 3.10: Circuit diagram of a three-stage RO. The RO is composed of three inverters (1-3) cascaded in a loop with the fourth inverter (4) decoupling the RO from the measurement equipment connected to the output (out).

low on-state resistance to be able to quickly charge/discharge the gate capacitance of the next stage. Since the oscillation frequency $f_{\mathrm{o}} < f_{\mathrm{T}}$ (where f_{T} is the cutoff frequency) is a direct measure of delays in realistic scenarios, ROs are the standard testbeds for evaluating ultimate performance limits and the highest possible clock rates of digital logic families.

Complementary operation of the graphene inverters within a RO is obtained between the Dirac points of the two FETs, after the supply voltage $V_{\mathrm{DD}} > 0$ is applied. In this configuration, the input and output voltages at the highest-gain (i.e., threshold) point of an inverter are mismatched by V_{IN} - $V_{\mathrm{OUT}} = V_0$,where V_0 is the voltage at the Dirac point of the unbiased FETs. A positive voltage at the Dirac point ($V_0 > 0.2$ V, measured in air at room temperature) was found in all fabricated FETs, stemming from p-type doping introduced by ambient impurities adsorbed on graphene. Since in/out mismatch at the threshold point rapidly reduces voltage swing in multistage graphene circuits, a positive back-gate voltage, $V_{\mathrm{BG}} = (C_{\mathrm{ox}}/C_{\mathrm{ox,BG}})V_0$,was used to shift

the Dirac point back to zero. Here C_{ox} and $C_{\mathrm{ox,BG}}$ are the top-gate and backgate capacitances per unit area, respectively ($C_{\mathrm{ox}}/C_{\mathrm{ox,BG}}$= 121.2 and $C_{\mathrm{ox}}\approx$ 1.4 µF cm^2). With the appropriate back-gate voltage, the voltage gain of such inverters at the threshold point is $|A_{\mathrm{v}}| > 4$.

Figure 3.11 shows voltage signals measured at the output of the three types of fabricated ROs with the buffering stage. The measured oscillation frequency scales approximately with $1/L$ (figure 3.11 a). The largest voltage swing in fabricated ROs was 0.57 V. All three ROs shown in figure 3.11 required relatively low back-gate voltages (as low as $V_{\mathrm{BG}} = 5$ V) and were operated in ambient air.

The oscillation frequency of conventional ROs, as well as those made from nanomaterials such as CNTs and MoS_2, strongly depends on the supply voltage V_{DD}. This represents a serious problem in complex digital circuits in which a large number of transistors and increased power consumption place increased demand on the voltage supply, causing it to fluctuate. Such fluctuations not only have a negative impact on the operation of logic gates but also deteriorate their noise performance. We found that, in contrast to other types of ROs, graphene ROs are much less sensitive to fluctuations in the supply voltage.

In order to reach a voltage gain of >1, the gate oxide thickness in graphene FETs must be more aggressively scaled than the gate length and supply voltage, breaking the conventional scaling laws. The present oxide thickness (~4 nm) is only slightly larger than that of contemporary Si FETs, and in both cases further scaling benefits can be obtained only at the expense of other advances. The only advantage of graphene ROs with respect to Si CMOS ROs is a smaller sensitivity to supply fluctuations; however, this comes as a consequence of the reduced volt-

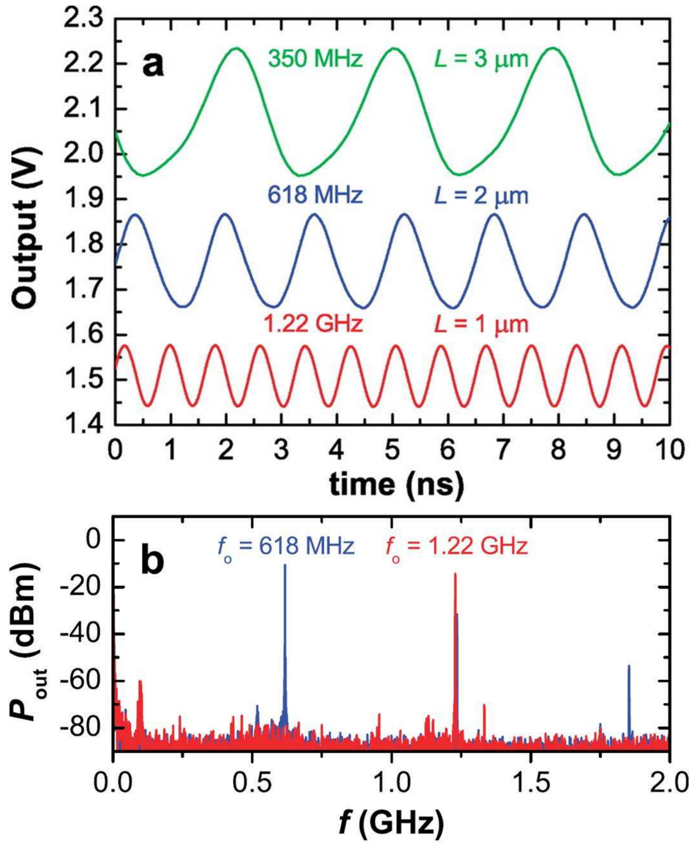


Figure 3.11: Output signals of buffered graphene ROs at $V_{\text{DD}} = 3.5$ V. (a) Large RO (green; $L = 3$ µm and $W = 20$ µm) oscillates at 350 MHz at $V_{\text{BG}} = 34$ V. The voltage swing is $V_{\text{p-p}} = 0.284$ V. Medium RO (blue; $L = 2$ µm and $W = 10$ µm) oscillates at 618 MHz at $V_{\text{BG}} = 5$ V. The voltage swing is $V_{\text{p-p}} = 0.208$ V. Small RO (red; $L = 1$ µm and $W = 10$ µm) oscillates at 1.22 GHz at $V_{\text{BG}} = 50$ V. The voltage swing is $V_{\text{p-p}} = 0.136$ V. The voltage swing is strongly suppressed by the low-pass filtering of the buffer. The green and red curves are vertically offset for clarity, from the midpoint voltage $V_{\text{DD}}/2 = 1.75$ V. (b) Respective power spectra of the medium and small ROs. The second harmonic of the medium RO is at the position of the first harmonic of the small RO.

age swing.

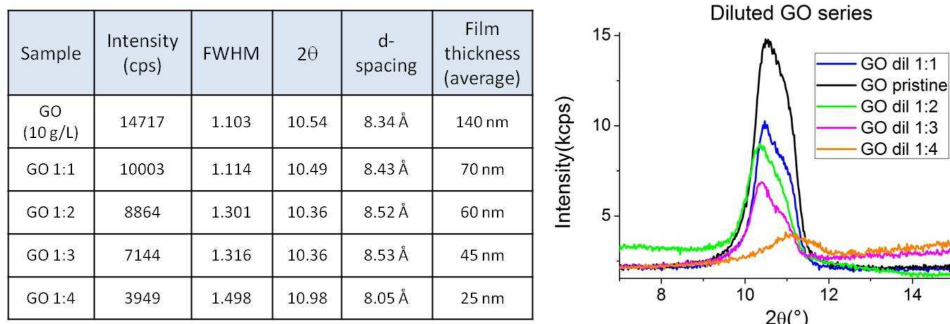
3.2 RGO conductive coatings

GO aqueous dispersions were prepared according the modified Hummers method, which allows us to obtain GO flakes with an average C:O ratio between 2.1 and 2.9 [73]. Large graphite flakes ($\sim$ 300 μm) have been used as starting material in order to extract large GO flakes (average lateral size 20 - 50 µm) after the oxidation step. For this reason, the starting material was selected in agreement with the goal of reducing the number of interflake junctions which occur through the rGO films.

The pristine GO solution (10 g/L) was diluted with DI water at different concentrations and deposited by drop casting onto Si/SiO_2 substrates. The XRD spectra recorded for films deriving from the dilution series are reported in figure 3.12, which show a good correlation between the intensity of the GO peak (at $2\theta \sim 10°$) and the film thickness measured by AFM, i.e. higher peak intensities for thicker films. The XRD pattern of GO shows a large interlayer spacing d_{002} = 8 - 8.5 Å for the (002) peak at $2\theta \approx 10°$ because of the presence of intercalated H_2O molecules, various oxide groups and other defects introduced by the oxidation step.

Reduction by plasma

GO films deriving from the GO solution diluted 1:3 were used for the reduction by Ar plasma. The samples were treated as reported in the



Sample	Intensity (cps)	FWHM	2θ	d-spacing	Film thickness (average)
GO (10 g/L)	14717	1.103	10.54	8.34 Å	140 nm
GO 1:1	10003	1.114	10.49	8.43 Å	70 nm
GO 1:2	8864	1.301	10.36	8.52 Å	60 nm
GO 1:3	7144	1.316	10.36	8.53 Å	45 nm
GO 1:4	3949	1.498	10.98	8.05 Å	25 nm

Figure 3.12: GO dilution series. XRD spectra ($2\theta = 7°$ - $15°$, right) recorded for GO films resulting from different dilution degrees, as indicated in the inset (v/v). The values of intensity, full width at half medium (FWHM), 2θ and interlayer spacing (d_{002}) corresponding to the GO (002) peak at $2\theta = 10°$ - $11°$ are reported (table, left). The thickness of each GO film was measured by AFM (table, left).

table below:

Sample	Direct current	Exposure time	H_2 flux
a	150 A	30 mins	35 sccm
b	150 A	10 mins	35 sccm
c	50 A	10 mins	35 sccm
d	150 A	30 mins	-
e	150 A	10 mins	-
f	50 A	10 mins	-

The mechanism of GO reduction is mainly attributed to the irradiation of electrons which originated inside the plasma chamber. The density of electrons inside the chamber is estimated to be $\sim 10^{17}/m^3$, having an energy $\sim$ 4 eV, thus very low compared to electrons generated in a TEM (typically $\sim$ 100 - 300 keV). Moreover, it is expected that the

electron irradiation causes the heating of the GO films, which should improve the reduction process. Unfortunately it was not possible to directly monitor the temperature of the sample inside the chamber.

The XRD patterns of all GO samples before and after plasma treatment are reported in figure 3.13. The treatment at mild conditions, in samples c and f, causes only a slight shift of the (002) peak indicating the ineffectiveness of the treatment at such conditions. The other processes by plasma, both with and without hydrogen flow, are seen to cause the disruption of the GO lattice due to the introduction of several defects during the reduction process. These phenomena are evident from the total disappearance of the (002) peak from the XRD patterns of samples a and b, as shown in figure 3.13. The origin of these defects is mainly attributed to the removal of the functional groups present in GO, which leaves behind vacancies and topological defects throughout the GO plane and causes lattice contraction. The structural disorder introduced by the plasma treatments in sample a and b prevents the detection of the typical d_{002} peak of graphene at $2\theta \approx 26.7°$ since at these low temperatures the graphene lattice is unable to rearrange into well-ordered layers. However, the XRD spectra of rGO samples d and e show a weak and broad peak at $2\theta = 20.1°$ ($d_{002} = 4.3$ Å) and at $2\theta = 18.8°$ ($d_{002} = 4.7$ Å), respectively, suggesting that the intercalated H_2O molecules and the majority of oxide groups have been removed. This supposition is reasonable because the gap of 0.9 Å between $d_{002} = 4.3$ Å(of rGO, sample d) and $d_{002} = 3.4$ Å (of graphite) is too small to contain the ∼1.25-Å epoxy group or the ∼2.75-Å H_2O molecules [122].

As an additional proof of the effectiveness of the plasma exposure, one

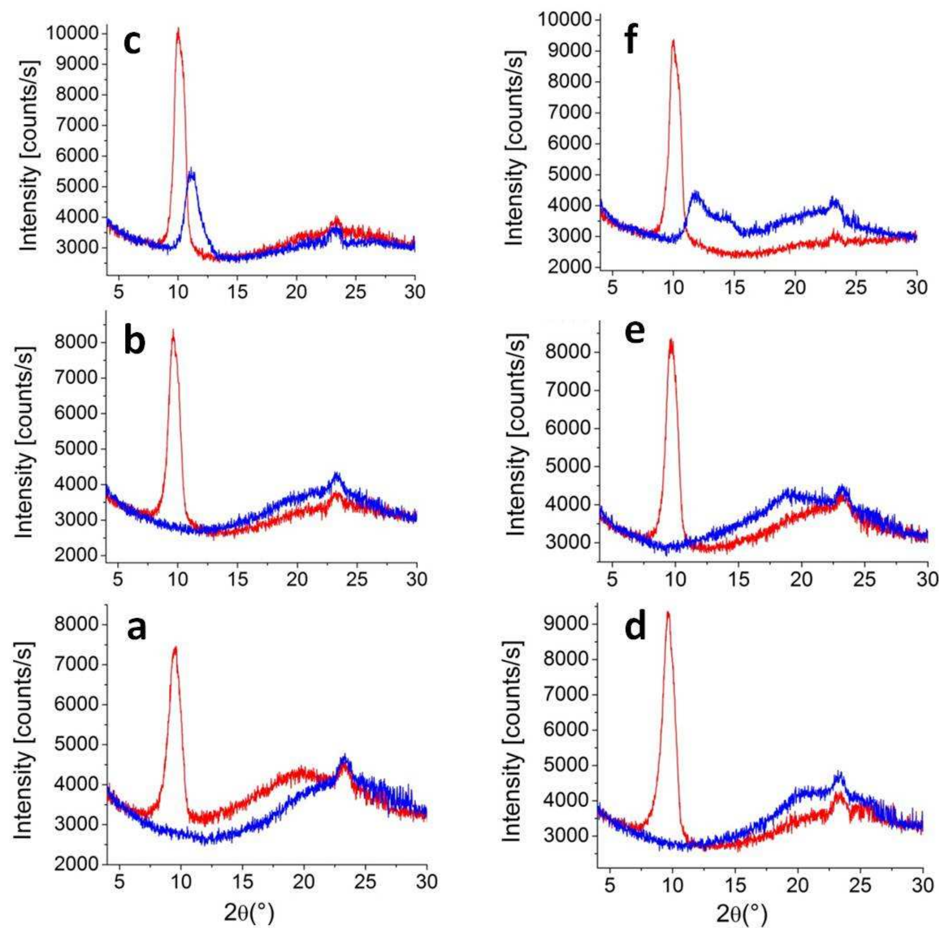


Figure 3.13: XRD spectra of GO and rGO treated by plasma ($2\theta = 4^{\circ}$ - 30°). For each sample is shown the GO spectra before (red) and after (blue) reduction by plasma.

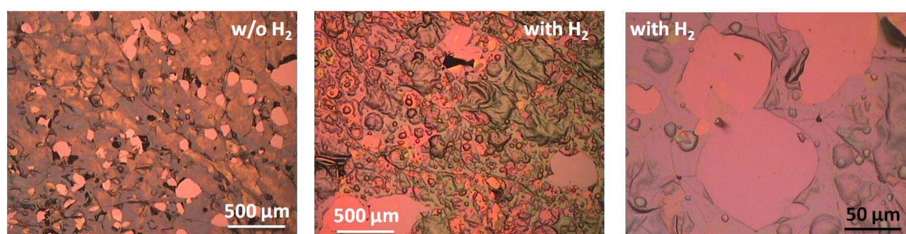


Figure 3.14: Optical images of rGO films after plasma treatment for 30 minutes at 150 A as dc current.

GO sample has been kept for 90 mins inside the chamber at a pressure $\sim 10^{-7}$ mbar and temperature ∼100°C. The XRD spectra recorded are identical before and after the treatment, indicating that these conditions are not sufficient to remove neither the intercalated H_2O molecules nor any functional groups of GO. The electrical conductivity and the optical aspect of the GO surface also remain unchanged after the treatment.

On a larger scale, charging of insulating GO flakes by the electrons in the plasma may lead to electrostatic delamination of parts of the film. Optical images of rGO films treated by plasma are reported in figure 3.14. As observed by optical microscopy, the treatments by plasma causes serious damage to the GO films introducing holes and swellings at a macro scale. Luckily, the electrostatic delamination often removes only few layers of the rGO films, thus leaving some material intact behind (figure 3.14 right image).

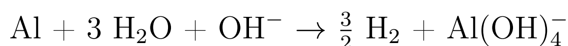
The values of electrical conductivity for all rGO films are reported in the table below.

sample	conductivity σ (S/cm)	sample	conductivity σ (S/cm)
a	12	d	14
b	4.52	e	5.55
c	0.017	f	0.13

The trend of conductivity is in agreement with the results of the XRD analysis. At longer exposure times and higher direct current, the rGO samples become more conductive indicating that the conversion of GO to rGO occurs gradually. Surprisingly, the presence of hydrogen seems to negatively interfere with the reduction process. This may be attributed to partial hydrogenation of the sp^3 (oxygen functional) groups on the GO surface, thus preventing their conversion to sp^2 domains.

Chemical reduction by nascent hydrogen

The pristine GO solution (10 g/L) was deposited by drop casting onto glass substrates and chemically reduced by nascent hydrogen generated from the reaction between the Al foil and ammonia solution. The development of hydrogen should follow the equation:



$$\mathrm{Al} + 3\,\mathrm{H_2O} + \mathrm{OH^-} \rightarrow \tfrac{3}{2}\,\mathrm{H_2} + \mathrm{Al(OH)_4^-}$$

Nascent hydrogen is a very reactive species that readily reacts with epoxy, carbonyl and hydroxyl groups following the pathway which was subsequently proposed in reference [102]. The darkening of the GO films that occurs along the reduction process should be a first indication of the conversion of GO into rGO. Figure 3.15 shows the XRD spectra of the same GO film before and after 3 subsequent reductions

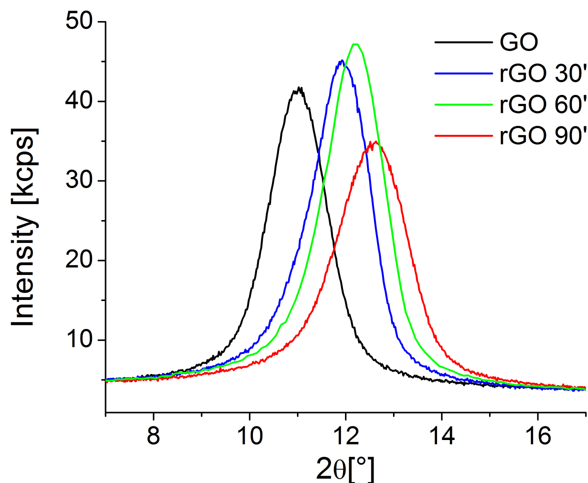


Figure 3.15: XRD patterns of chemically reduced GO

at the same conditions (GO, rGO 30', rGO 60' and rGO 90', respectively). The shift of the (002) peak from $2\theta = 11°$ to $2\theta = 12.6°$, which occurs from GO to rGO 90', corresponds to a decrease of the interlayer distance Δd_{002} ~0.1 nm. The electrical conductivity of rGO films was measured by four point probes. All rGO films showed an insulating behaviour even after all 3 reduction steps. These results indicate that the reduction of GO using nascent hydrogen developped from Al and ammonia solution was not effective at the purpose of this experimental project.

3.3 GO inks for inkjet printing

Aqueous GO dispersions were produced by oxidizing expanded graphite through modified Hummers method. An important parameter in the inkjet printing of suspensions is the size of the particles, which is limited by the diameter of the nozzle. Long sonication was required in order to fine tune the final lateral size of the GO flakes according to the nozzle diameter used in this thesis (21 μm). Some SEM images of GO flakes before and after sonication are reported in figure 3.16: the final lateral flake size is well below 1 μm, which could be achievable only by prolongated probe sonication.

As shown in figure 3.17, GO patterns were printed directly onto Si/SiO_2 substrates as lines or films varying the drop spacing. The optimal drop spacing which allows to obtain a uniform coverage of the pattern is 10 µm. The density, viscosity and surface tension of the ink are expected to be the properties that show the strongest dependence on the jetting and spreading of the droplets on the substrate. The characteristics of the GO solution were fine tuned in order to optimize the jettability by dilution 1:1 (v/v) with DI water and by adding a surfactant. However jettability was performed at not optimal conditions as it is evident form non-continuous layers, irregular line shapes and satellite drops.

The printed GO patterns were thermally reduced at 400°C under Ar/H_2 environment in order to restore the electrical conductivity of the rGO flakes. After thermal reduction electrical devices were patterned across the selected lines by EBL. Figure 3.18 shows two structures which were fabricated: Ti/Au contacts (figures a and b) and three complementary inverters comprised of six transistors (figures c and d). The roughness

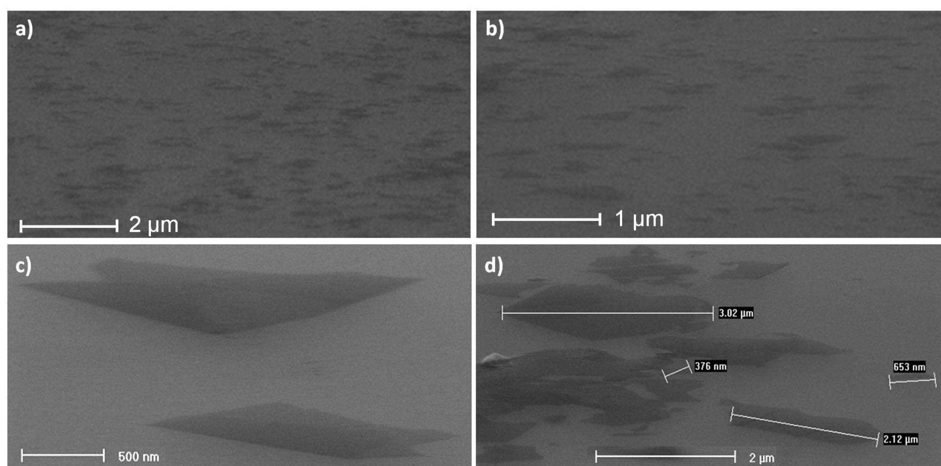


Figure 3.16: Reducing lateral size of GO flakes. a) and b) SEM images of GO flakes after long sonication by ultrasonic probe: the lateral dimensions are below 1 μm, as required by the ink-jet printer specifications; c) pristine GO flakes as deposited after Hummers method and d) after a mild sonication treatment by ultrasonic bath (3 hours), which was not suitable to reduce the lateral dimensions because of the insufficient amount of energy conferred to the flakes.

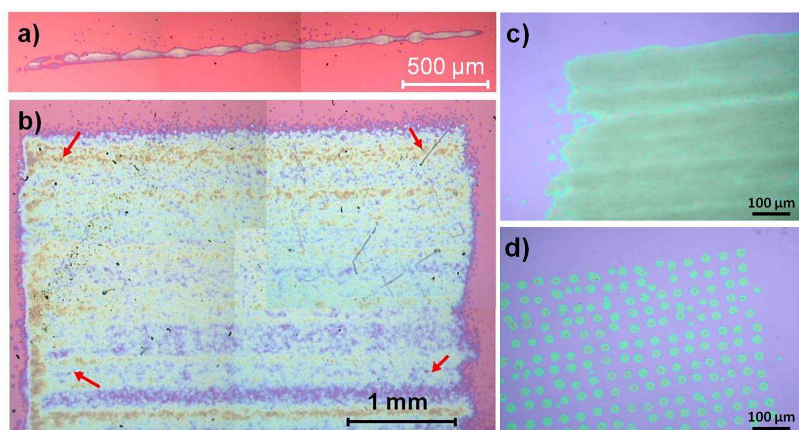


Figure 3.17: GO patterns onto Si/SiO_2 substrates printed by inkjet printers. a) GO line, one layer printed at drop spacing 10 µm; b) square-shaped pattern, one layer printed at drop spacing 10 µm. The red arrows indicate the place where the probes for electrical characterization were placed; c) and d) printing trials at 10 µm and 60 µm as drop spacing respectively.

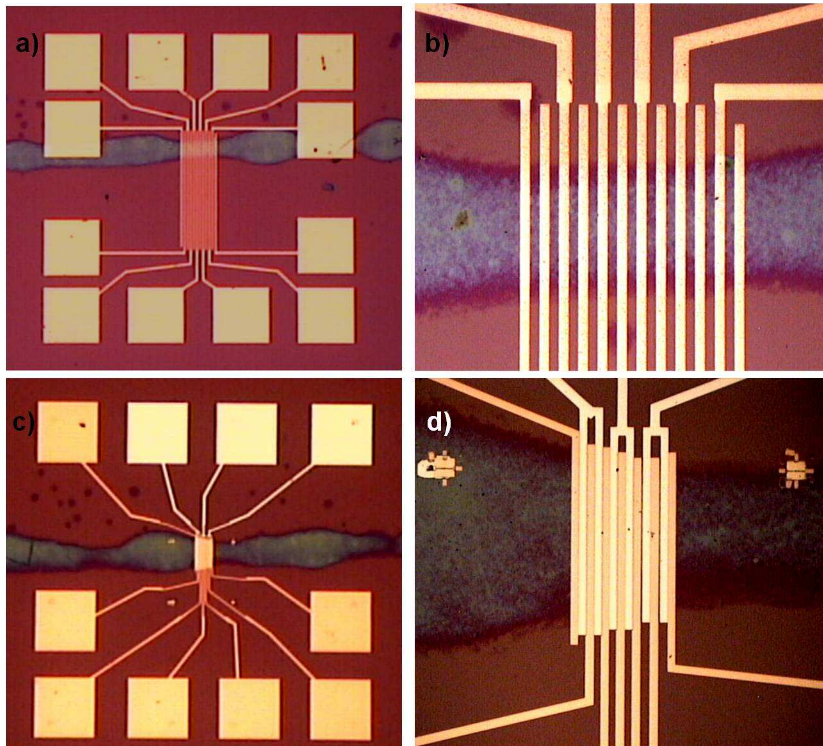


Figure 3.18: Structures patterned across the rGO line. a) and b) Ti/Au electrodes (3/12 nm) used to measure the electrical resistance of the rGO line (blue). The spacing between each electrode is 5 µm (L) while the average width (W) of the line is 64 µm and its average thickness (t) is ∼10 nm. c) and d) Ti/Au electrodes (yellow) and Al top gates (white) used to measure the gate dependance of the rGO line.

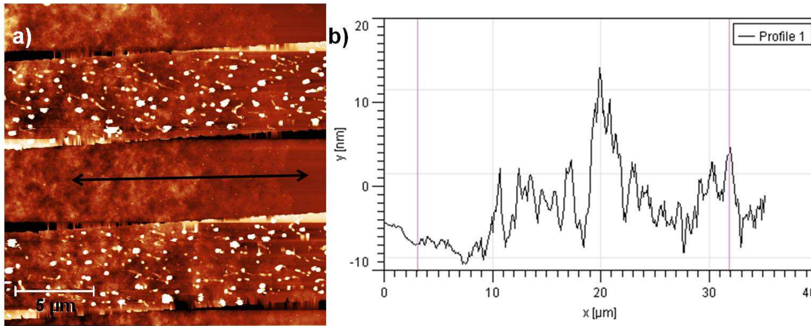


Figure 3.19: Roughness of rGO patterns printed by inkjet. a) High-resolution AFM image of rGO pattern including two metal contacts. b) Height-profile along the black arrow. The average thickness of the line is ∼10 nm.

of the rGO line and its thickness were analyzed by AFM. In figure 3.19 a high-resolution AFM image of a portion of the same device of figure 3.18 a) is reported, showing parts of two electrodes. The average thickness of the line corresponds to ∼10 nm. In the case of the square-shaped pattern, the step height was measured across a scratch made on top of the pattern and the resulting thickness is ∼50 nm.

The electrical characterization was performed only after thermal reduction of each GO pattern. Firstly the electrical resistance of an rGO film was measured in van der Pauw configuration, placing the probes directly on top of it as depicted in figure 3.17 b. The rGO film sheet resistance is $R_s = 5.05\text{x}10^3$ $(\Omega/\square)$ and its electrical resistivity is $\rho = 2.52\text{x}10^{-2}$ (Ωcm). The XRD spectra of the GO film before and after thermal annealing was recorded (figure 3.20). The results of X-ray analysis indicate a decrease of the interlayer spacing $d_{002} \sim 3$ Å due to the contraction of the rGO lattice which occurs during thermal reduction.

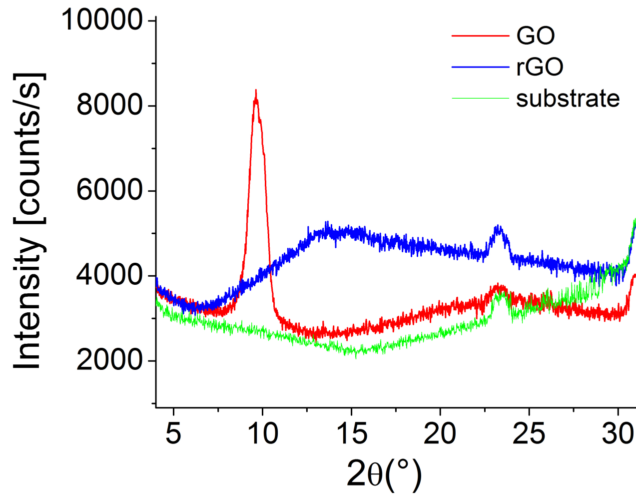


Figure 3.20: XRD spectra of GO films (2θ = 4° - 31°) before and after thermal annealing at 400°C under Ar/H_2 environment. GO spectrum (red) presents the (002) peak at $2\theta = 9.63°$, which corresponds to an interlayer spacing $d_{002} = 9.17$ Å; the rGO curve after thermal annealing (blue) shows a weak peak at $2\theta = 14.49°$, which corresponds to an interlayer spacing $d_{002} = 6.12$ Å. The XRD spectrum of the Si/SiO_2 was also recorded (green) for comparison.

Just fabricated devices			14 days after lithography		
2 probes (KΩ)	4 probes = R_s (KΩ)	resistivity (Ωcm) $\rho = R_s * W*t / L$	2 probes (KΩ)	4 probes = R_s(KΩ)	resistivity (Ωcm) $\rho = R_s * W*t / L$
a-b : 3.2	labc : 2.4	$3.1*10^{-2}$	a-b : 203	labc : 2.9	$3.7*10^{-2}$
b-c : 3.5	abcd : 2.5	$3.2*10^{-2}$	b-c : 80	abcd : 2.9	$3.7*10^{-2}$
c-d : 3.6	bcde : 3.4	$4.4*10^{-2}$	c-d : 302	bcde : 22.6	$2.9*10^{-1}$
d-e : 3.2	cdef : 2.3	$2.9*10^{-2}$	d-e : 159	cdef : 3.6	$4.6*10^{-2}$
e-f : 3.5	defg : 3.2	$4.1*10^{-2}$	e-f : 164	defg : 17.7	$2.3*10^{-1}$
f-g : 3.9	efgh : 2.9	$3.7*10^{-2}$	f-g : 214	efgh : 4.7	$6.0*10^{-2}$
g-h : 3.2	fghi : 2.7	$3.5*10^{-2}$	g-h : 222	fghi : 3.6	$4.6*10^{-2}$
h-i : 3.2	ghij : 2.6	$3.3*10^{-2}$	h-i : 120	ghij : 2.8	$3.6*10^{-2}$

Figure 3.21: Electrical resistance of rGO patterns. The resistivity of each device is calculated assuming common width ($W = 64$ µm), length ($L = 5$ µm) and thickness ($t = 10$ nm). The letters from a to j indicates the electrodes which are measured. The measurements were repeated 14 days after the device fabrication (right table) in order to check electrical stability of the rGO patterns.

Figure 3.21 reports the values of the electrical resistance measured by two and four probes on devices fabricated on the rGO line and their respectives resistivities. The same measurements were repeated 14 days after the devices fabrication, showing that rGO electrical resistance tends very slightly to increase in the course of time. This behaviour is explained by the metastable nature of rGO flakes which causes variations of their electronic properties. Figure 3.22 shows the electrical behaviour of the rGO line measured through the top gated FET. The device shows the transfer curve of the drain-source current vs gate-

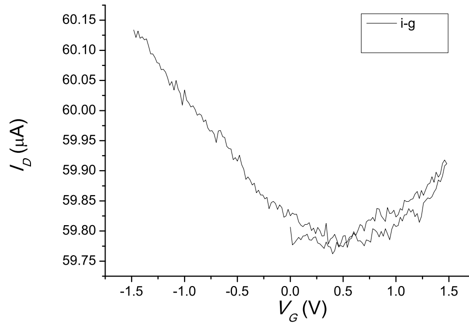


Figure 3.22: Transfer curve drain-source current (I_{D}) vs gate-source voltage (V_{G}) of a typical transistor exhibits a minimum at the Dirac point V_{G} = 0,5 V .

source voltage of a typical graphene transistor, exhibiting a current minimum at the Dirac point $V_{\mathrm{G}} = 0.5$ V . However, the current on/off ratio resulting from the transfer curve is very low (~ 1), suggesting that the rGO produced in this experiment is not suitable for for the fabrication of rGO-based transistors. On the contrary, the values of rGO conductivity ($\sigma\sim$ 3500 S/m for lines and $\sigma\sim$ 4000 S/m for films) is higher than the average values found in literature for GO-derived materials and address future research to a deeper understanding of the reduction process.

3.4 GO for other applications

3.4.1 GO for TCNL

It has been shown recently that TCNL is a versatile technique to tune the topographical and electrical properties of rGO with nanoscopic resolution by local thermal reduction of GO with a heated AFM tip [123]. The local chemical or physical transformation induced by the heated tip can be controlled in terms of spatial resolution (down to sub-50 nm) and extent of chemical conversion.

Conducting rGO zig-zag nanostructures were successfully patterned onto a highly insulating GO film deposited on SiO_2. Figure 3.23 a) shows a zoomed topography of one nanostructure having resolution down to $\sim$50 nm (inset). Friction of the four nanostructures made by one of the tips is shown in figure 3.23b), where different temperatures were used for each nanostructure by increasing the applied voltage within the range 9.0 - 10.5 V.

3.4.2 GO for scanning Auger microscopy measurements

The determination of number of GO layers still remains a challenge to fully understand and further develop potential applications of GO flakes. The aim of this project was to demonstrate the use of Auger electron spectroscopy (AES) as a fast and accurate technique to estimate the thickness of GO flakes. This was done by comparing AES

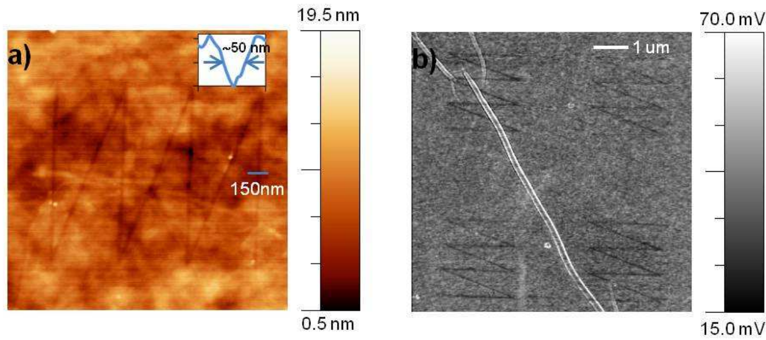


Figure 3.23: a) Zoomed in topography of one rGO nanostructure; b) Friction of the four nanostructures made by tip 1. Adopted form reference [119].

and AFM measurements performed on the same GO flakes deposited on a thin Au (13 nm) layer.

The comparison of the AES and AFM estimations of the GO thickness on Au showed a good agreement of the results (see figure 3.24).

The complete results of the estimation of GO thickness based on AES data are still confidential since they will be exploited for a future publication.

3.5 GNRs from CdSe nanowires as etching mask

GNRs were fabricated by etching manually exfoliated graphene monolayers using CdSe nanowires as etching masks. CdSe was deposited on top of graphene and contacts were defined by EBL and thermal

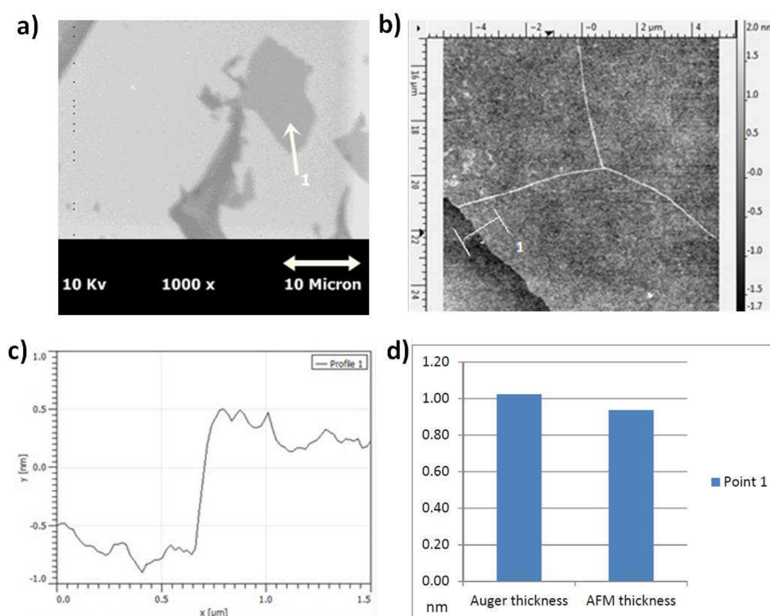


Figure 3.24: Comparison between AES and AFM analysis of the same GO flake. a) SEM image acquired in SED mode; b) AFM image acquired in tapping mode; c) step height profile measured along the line (1) depicted in b); d) thickness values recorded at the same point by AFM and AES, showing values of ∼0.9 nm and ∼1 nm, respectively.

evaporation. Subsequently, reactive-ion etching was used to etch the unprotected graphene and to achieve the morphology transfer between the nanowires and graphene. Transport measurements were performed either before and after RIE, so that it was possible to verify an increase of the on/off ratio due to quantum confinement in GNRs. It was found that the CdSe nanowires do not contribute to the transport as they are non-conductive, thus all measurements were performed by leaving them on top of the GNRs.

Graphene FETs

The first set of measurements was performed to investigate the ambipolar field effect of the graphene flake area between source and drain contacts by electrostatic back-gating, i.e., in a conventional FET configuration. The bias V_{D}, connected to the source electrode, was kept at 1 mV, while the drain was connected to the ground. The gate voltage V_{G}, applied through the doped silicon substrate used as a back gate, was varied between $\pm$ 20 V. The gate current I_{G} was constantly monitored and it was found to be always lower than 1 nA, i.e., less than 3 order of magnitude with respect to the drain current, thus demonstrating the integrity of the gate insulator and the reliability of the measurements. Figure 3.25 shows a typical transfer curve of a fabricated graphene FET (GFET), where the behavior of graphene resistance versus gate voltage is measured under ambient conditions. The average on/off ratio of the graphene FETs, in the full voltage range, was found to be around 2. All fabricated FETs tend to show a positive voltage V_{G} at the Dirac point in air, generally falling in the range $[0 \div 10]$V ; this offset stems from a p-type doping which

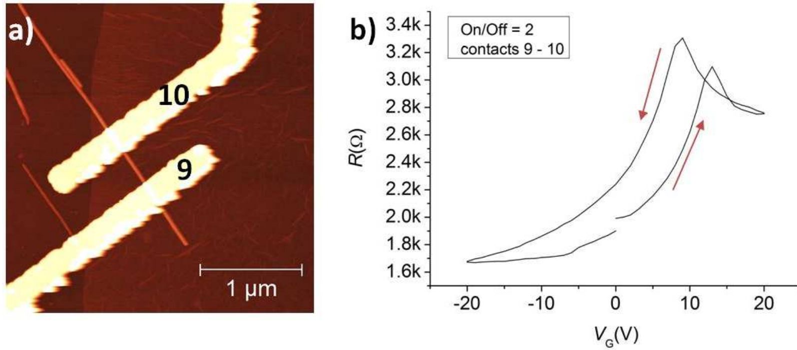


Figure 3.25: Graphene FETs. a) AFM topography of FET device (yellow) fabricated on top of graphene where the CdSe nanowire (orange) is localized. b) Transfer curve of a typical graphene FET, acquired under ambient conditions, exhibiting a maximum at the Dirac Point at $V_G \sim 10$ V.

is commonly present in graphene devices, and it derives from ambient impurities adsorbed on graphene prior to fabrication. Moreover, all transfer curves exhibit a hysteretic behavior. The hysteresis could be attributed to charge trapping by SiN, which are activated by the small gate current I_G , and a possible contribution by water molecules localized between the substrate and the graphene flake, possibly combined with hydroxyl groups on the substrate.

GNR FETs

After the oxygen plasma treatment, the resulting GNRs were electrically characterized in the same configuration previously described for GFETs. For each measurement, the bias V_D was varied between 10 mV - 500 mV while the gate voltage was swept between $\pm$ 20 V. Figure 3.26 shows four representative transfer curves of the fabricated GNRs,

related to different CdSe nanowire thicknesses (which correspond to GNR final widths). In particular, GNRs in figure 3.26 progressively show increasing widths (W) from a) to d) respectively. From their comparison, it is possible to observe the clear dependence between the ribbon width and the magnitude of the on/off ratio. In general, for nanowire thicknesses between 15 and 27 nm the on/off ratio was found to vary between 10 and 32, while for thicknesses greater than 30 nm the on/off was less than 10, progressively decreasing.

However, it was not possible to perform an experimental fit of the dependence of the bandgap on the nanoribbon width for two important reasons. Firstly, the nanoribbon widths have never been directly measured by AFM, due to the presence of the CdSe fiber on top and to the risk of physically damaging the ribbon with the AFM tip. Secondly, after the oxygen plasma step, all the GNR transfer curves showed an increase in the Dirac voltage V_0, i.e., an upshift of the Dirac point towards higher input gate voltages. In many cases the Dirac point fell above the measurement range of 20 V (figures 3.26 a, c, d). This implies that the true on/off was not detectable, since higher gate voltages were not attempted. In general, the Dirac point offset V_0 moves from ≈ 5 V in graphene FETs to $\approx$ 10-20 V in GNR FETs, revealing the introduction of adsorbates in the etching procedure which act as p-type dopants in graphene. Finally, all GNR transfer curves exhibit a hysteretic behavior, which in few cases it was found to be slightly more pronounced than before plasma etching. However, water molecules entrapped between the surface and graphene channel should not be influenced by the plasma etching treatment [112]. Although the patterning of graphene into nanoribbons allows increasing the on/off ratio

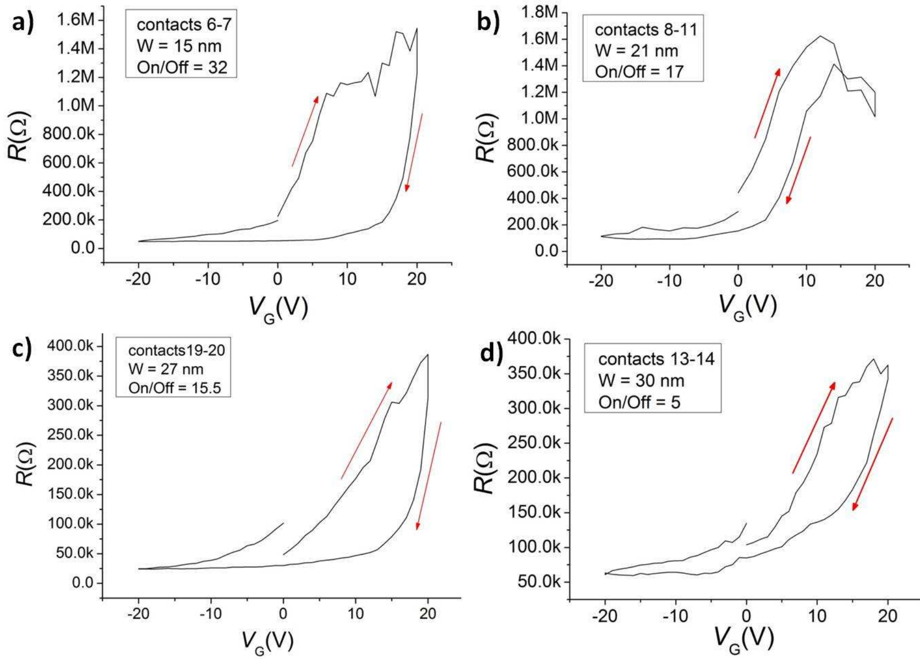


Figure 3.26: Transfer curves of GNR FETs. All devices were measured under ambient conditions at drain-source voltage $V_{\mathrm{D}} = 10$ mV. The gate sweep direction is indicated by the arrows. The GNRs respective widths and on/off ratios are indicated in the insets.

of the corresponding FETs, and therefore reducing the off current and the static dissipated power, it also has the drawback of reducing the drain current of the on state, due to a significant increase of the channel resistance. This implication has major impact on the operational clock rate of GNR FETs.

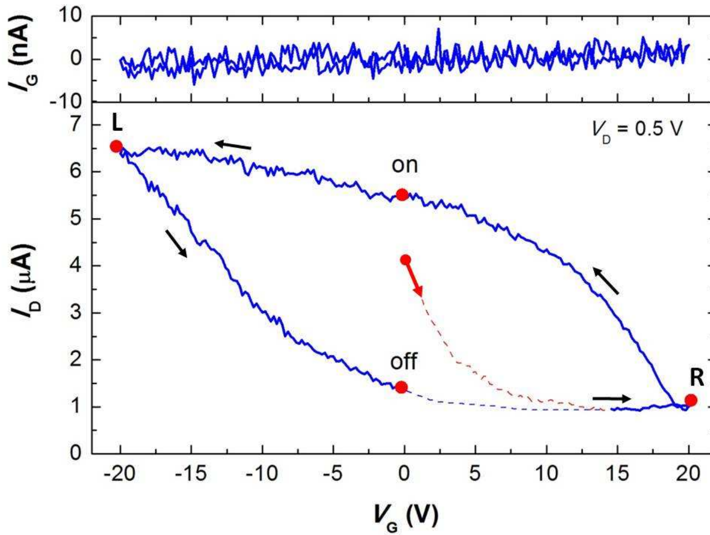


Figure 3.27: Transfer curve of an exemplary memory device recorded under ambient conditions at a $V_{\mathrm{D}} = 0.5$ V. The gate sweep direction is indicated by the arrows. The left and right turning points of the sweep are denoted by L and R, respectively, and the on and off states at $V_{\mathrm{G}} = 0$ are indicated. The sweep starts where the red arrow is located and proceeds following the black arrows until the point denoted as "off". If other sweeps are repeated in sequence they would proceed along the blue dashed line in order to repeat another cycle. The on/off ratio at $V_{\mathrm{G}} = 0$ is $\sim$4, while in the full voltage range the device shows on/off ~ 7.

GNR memory measurements

The operation of a GNR memory device can be explained through figure 3.27, which shows a GNR FET transfer curve, i.e., the drain current I_{D} versus the gate voltage V_{G}. The on and off states are associated with two different current levels I_{D} , which the GNR assumes at the same gate voltage, depending on the sweep direction. The conductance duality stems from the hysteresis of the transfer curve. In this thesis, the purpose was to effectively control the hysteresis through the SiN charge trapping layer, to be activated by the gate leakage current. The triggering is performed with a bipolar pulse signal applied through the back gate, whose duty cycle (the ratio of the pulse duration, τ, to the period of the signal) is adjustable to reach well-distinguished memory states. If the device is in the off state, by applying a positive pulse the operating point will move as off $\rightarrow$ R $\rightarrow$ on (figure 3.27), so that the memory state is changed and it will remain in the on state even after the gate voltage is reset. Similarly, a negative gate pulse moves the operating point as on $\rightarrow$ L $\rightarrow$ off , recovering the off state of the memory.

Memory measurements on GNR FETs were initially focused on the detection of a stable memory effect under ambient conditions, i.e. identification of two stable and well distinguished current states (high I_{D} = "on" and low I_{D} = "off"). At this purpose, the magnitude and the duty cycle of the bipolar pulse triggering signal were varied, while monitoring the drain and the gate current, keeping the bias V_{D} constant at 500 mV (figures 3.28 and 3.29). In general, it was possible to observe a memory effect at a pulse magnitude of 10 V. Higher voltages, up to 50 V, were used to increase both the separation between the two current

levels I_{D} (by increasing the transfer curve hysteresis) and I_{G}. In this way it was possible to achieve reliable and well-distinguished memory states and to promote the activation of the SiN trapping layer. However, a large gate leakage current represents also a discharge channel for I_{D}, which results in the loss of the stored information (figure 3.29), i.e., the two conductance levels drift to an intermediate state within one hour. The separation of the memory states could be enhanced by increasing the pulse duration. However, at this explorative stage, the pulse duration was ≤ 5 ms, while the period was gradually increased in order to investigate the retention time and the stability of the memory states (figures 3.28 a and 3.29 b).

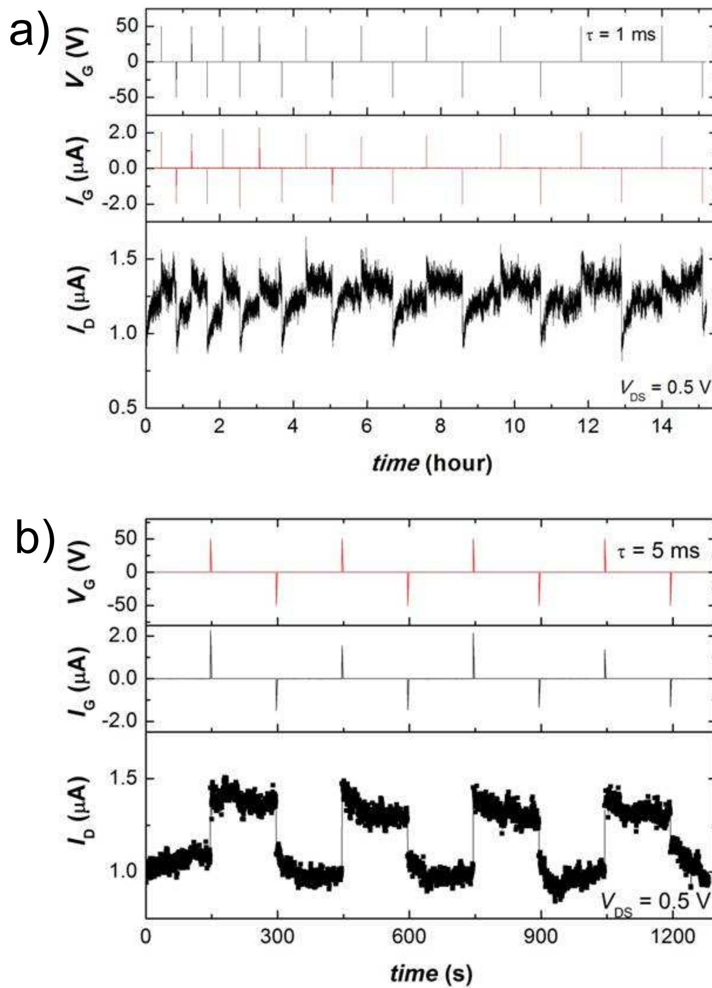


Figure 3.28: Operation of a GNR memory device. Both measurements were performed under ambient conditions at a bias $V_\mathrm{D} = 500$ mV and for each one it is shown the trigger signal V_G, the gate current I_G, the drain current I_D and the pulse duration τ. a) The retention time highlights the volatility of the two states, since the two conductance levels drift to an intermediate value. b) Memory operation of the same device working at signals with shorter periods.

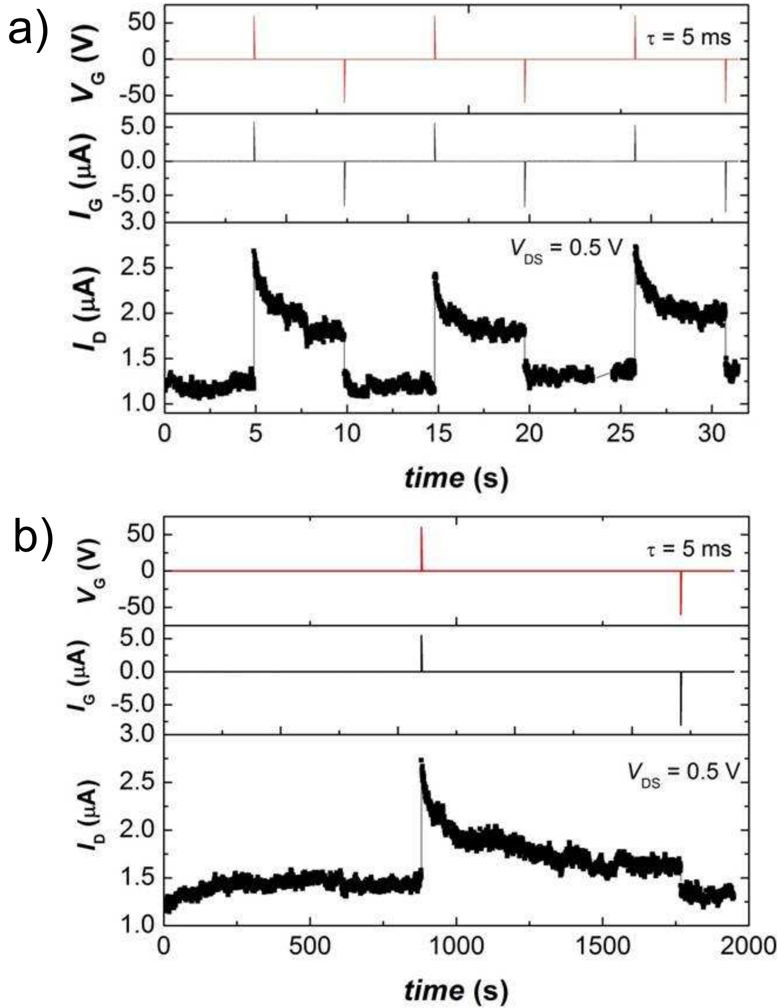


Figure 3.29: a) Memory operation and b) data retention of another GNR memory device. Both measurements were performed under ambient conditions at a bias $V_D = 500$ mV and for each one the trigger signal V_G, the gate current I_G, the drain current I_D and the pulse duration τ are shown. In this case the unstability of the two current states is even more pronounces than device in fig. 3.28.

Chapter 4

Conclusions

Graphene audio voltage amplifier

We have fabricated graphene voltage amplifiers based on graphene FETs in which the complete graphene channel is covered by an AlO_x/Al gate stack. Graphene was obtained by manual exfoliation of HOPG, which represents a limit for the scalability of device fabrication. Graphene FETs exhibited large intrinsic gain at room temperature, which was exploited to realize voltage amplifiers in complementary configuration. The complementary amplifier has a voltage gain of $\mid A_\mathrm{v} \mid_\mathrm{max} = 3.7$ V (11.4 dB) and a -3 dB frequency response up to 70 kHz, with a unity-gain frequency of 360 kHz. Even higher gains could be obtained with higher supply voltages, with the use of gate dielectrics with higher breakdown voltages. This result represents an important step toward simple, general-purpose high voltage gain graphene amplifiers which could serve as the main building block of all-graphene analog electronics.

Complementary integrated graphene inverter

The electrical performances of integrated graphene complementary inverters, fabricated on wafer scale CVD grown graphene films, were explored. Through these devices it was possible to achieve matching of input and output digital voltage signals, operating under ambient conditions and room temperature. Moreover, graphene logic gates were connected in a cascade configuration, so that more complex logic circuits were successfully realized. These results stem from the high ac voltage gain ($\mid A_{\mathrm{v}} \mid \approx 5$) obtained with top-gated wafer-scale CVD graphene FETs, the highest so far reported with this kind of devices under ambient conditions. These achievements suggest the possibility of implementing graphene as semiconductive chiannel in ultrafast logic gates, for which static power dissipation is not a concern. Importantly, our study has also served to highlight several remaining challenges of graphene FETs, most technological rather than fundamental in nature. For instance, graphene circuits remain sensitive to fabrication-induced variability, but we showed that this does not influence the operation of graphene logic gates as long as the graphene FETs exhibit high voltage gain.

Gigahertz integrated graphene ring oscillators

In summary, we have demonstrated integrated graphene ROs operating at room temperature, under ambient conditions. The ROs were fabricated from wafer-scale CVD monolayer graphene and were composed of inverters exhibiting signal matching and large voltage gain, $\mid A_{\mathrm{v}} \mid > 4$. The fabricated ROs oscillate at the highest frequency (1.28 GHz)

reported to date in a strictly low-dimensional transistor material, with the voltage swing (as a fraction of supply voltage) exceeding that of conventional InP ECL gates, the fastest logic family. Graphene ROs are more robust to variations in supply voltage compared to conventional ROs and could be used in applications where ultrafast operation is favored over static power dissipation. Oscillation frequency could be increased through further advances, e.g., by reducing the FET channel length, contact resistance, and parasitic capacitances. The fabricated ROs are an important step toward the application of graphene in electronics.

rGO conductive coatings

GO films were produced by drop casting GO dispersions onto different substrates. We studied two processes for the reduction of GO at low temperature: a) chemical reduction by nascent hydrogen and b) plasma-based treatment which exploits electron irradiation. Chemical reduction decreased the interlayer spacing (d_{002}) between the GO layers of only $\sim$0.1 nm and did not improve the electrical conductivity of the resulting rGO film, even after three subsequent treatments. According to these results, this technique was considered to be ineffective for the reduction of GO films. Plasma-based treatment was performed by exposing the GO films to an Ar plasma with and without the presence of hydrogen flux. The shift of the XRD pattern of GO (10.27°) to rGO 2θ peak (20.1°) suggested that the rGO film was reduced well. The interlayer distance of rGO was 4.3 Å, which was larger than that of graphite powder (3.4 Å) because of the presence of residual functional groups or some defects deriving from the oxidation-reduction

process. The electrical conductivity rGO films reached 1.4x10^3 (S/m), which is comparable to the highest values obtained from similar reduction techniques proposed in literature [124], but still one order of magnitude lower than the strongest reduction techniques investigated at present for the production of highly-conductive rGO [101, 125, 92].

However, GO sheets with a high concentration of lattice defects are difficult to fully deoxygenate and the defects themselves are difficult to heal by post-treatment. As a result, a controllable oxidation during the production of GO will be needed to achieve highly reducible GO, which can be converted to rGO of high quality and good properties. Moreover, GO will always benefit from the following characteristics: it can be produced using inexpensive graphite as raw material by cost-effective methods with a high yield of monolayers; stable aqueous colloidal dispersions of hydrophilic GO allows high processability and ease of thin-film deposition techniques (i.e. spincoating, dip-coating, spray-coating, dropcasting, inkjet printing), thus facilitating the assembly of macroscopic structures on various substrates.

GO inks

We have demonstrated that it was possible to print different patterns with inkjet GO inks based on aqueous GO dispersions produced by modified Hummers method. A long sonication step ($\sim$5 hours) was required in order to reduce the lateral size of the GO flakes down to 500 nm and to satisfy the nozzle dimensional requirements. With one printed layer it is enough to obtain uniform coverage of the desired patterns, which is than converted to highly electrically conductive rGO

after thermal annealing at 400°C under Ar/H_2 environment. This represents an advantage over other graphene-based inks found in literature [114, 115, 101, 116, 126], where 10 or more layers must be printed in order to obtain uniform coverage of the patterns in order to reach the conductivity threshold.

Viscosity and surface tension were fine tuned in order to improve the jettability parameters during printing. However, future studies will be devoted to optimize the ink formulation and to pretreat the substrate with the aim of improving the printing definition and to avoid defects such as satellite drops.

Metal contacts and top-gated FETs were fabricated onto rGO patterns after thermal annealing. The measured conductivity reached $\sim$ 3500 S/m, which is a significantly high value considering the fact that the highest temperature during thermal treatment was only 400°C. The electrical conductivity could be further incresed annealing the samples at higher temperatures, which imply the exclusion of substrates with a low melting-point. Fabricated rGO-FETs showed very poor gate dependance, suggesting that such material cannot be used as a channel for FETs.

GNRs memory devices

By employing CdSe nanofibers as a protective mask for graphene during oxygen plasma treatment, memory cells based on GNRs were fabricated. GNRs with widths down to 15 nm were achieved, resulting in on/off ratios of the associated GNR transfer curves up to 20, under ambient conditions. This technique is limited by the random position of

the CdSe nanowires deposited onto the substrate, which inhibits large scale integration of GNR FETs. Also, the crystallographic orientation of the GNR and its edge structure cannot be controlled, which could be detrimental to the electronics properties of the fabricated device.

The GNR memory cell was volatile in nature and exhibited low storage retention ability. This result is probably related to the inability to properly activate the SiN charge trapping layer. Possible explanations are: 1) The SiN layer is localized too far away from the GNR channels. 2) The gate current, which should activate the traps, flows from the source/drain electrodes to the back gate, so that the area below the GNRs is not really in the current path, resulting in an inefficient control of the traps. 3) The CdSe nanowires on top of GNRs prevent the proper coupling between the channel charge carriers and the gate current. Possible solutions are: 1) To use a substrate with a thicker SiN layer. 2) To implement a different electrode design, in order to surround the GNR channel with the contacts and to move the gate current flow closer to the channel. 3) To remove the CdSe nanowires in orer to investigate the behavior of bare GNR FETs. In conclusion, further experiments are required to deeply investigate the SiN trapping layer management and so to improve the performances of GNR FET memory devices.

Chapter 5

Other graphene-based materials

This part is related to commercial types of graphene-based materials. This activity was performed in collaboration with Directa Plus Spa, a technology company that developed and patented an industrial process for the production of graphene nanoplatelets (GNPs), trademarked under the commercial name G+.

5.1 Material characterization

During the first part of the collaboration with Directa Plus, an extensive work of microscopic characterization has been performed on different types of materials deriving from the G+ process. The main goal of this activity was to obtain all the information regarding the

particle morphology and dimensions in order to provide a feedback to the company during the fine tuning of the production process.

To this end, for each variation of the production parameters the material was analysed by optical, atomic force and scanning electron microscopies. G+ materials were deposited *via* liquid media on top of Si/SiO_2 substrates in order to obtain isolated particles suitable for scanning by different microscopy techniques. This task required both the preparation of well-diluted and stable dispersions and the choice of a proper deposition technique.

SEM resulted to be quite versatile for all morphologies and measurements of lateral dimensions of G+ materials, while AFM was useful to measure the flakes thicknesses. Due to the sensitivity and high resolution of both techniques, it was important to avoid the presence of residual impurities deriving from the deposition technique.

5.2 G+ applications: rubber nanocomposites

Subsequently the collaboration with Directa Plus was focused on developing potential applications for G+ materials. In particular, we worked on the applications concerning elastomeric systems.

It is well known that for most of the end use rubber applications, rubber must be reinforced with certain fillers such as carbon blacks, silica, clay and others to achieve products with improved properties. As compared to microfiller-reinforced rubber, nanofiller-reinforced rubber exhibits high hardness, modulus, anti-aging and gas barrier properties.

Therefore, the nanofillers are highly relevant for rubber compounds since their applications significantly improves the properties of rubber.

One of the most important characteristic of reinforcing fillers is their specific surface area (generally $\sim$10 - 100 m^2/g), which is directly related to their size and shape. Another important parameter that must be considered is the aspect ratio, i.e. the average length/diameter ratio. This aspect ratio may change from one (e.g., for spheres like carbon black) to values as high as several thousands, such as clays. Graphene and graphene nanoplatelets satisfy both requirements mentioned above with their high specific surface area (reaching a maximum of 2600 m^2/g for monolayer graphene) and aspect ratio (ranging from 100 to 1000). This represents a tremendous advantage for graphene-based materials since the interfacial contact area available to interact with the polymeric matrix is much larger compared to traditional fillers, thus increasing the reinforcing effect for identical or even lower levels of loading.

Another parameter that should be taken into account is the capability of the filler itself to be well dispersed and distributed within the rubber matrix. This depends on the surface chemistry of both filler and polymer, on the filler morphology and dimensions as well as on the mixing technology adopted during the compound processing. In this experimental project, the best-suited form of G+ was developed, which was perfectly capable of being incorporated in conventional industrial mixing technologies (using internal mixers for instance). The developed material was also found to be well distributed within the rubber matrix. In addition, latex-based preparation method (i.e., the co-coagulation of filler and rubber) was explored as an alternative com-

pounding method. With both compounding techniques, the dispersion degree of G+ particles within the matrix was very high and, thanks to their lamellar morphology and surface chemistry, they have an extraordinary tendency to self-orient within the rubber compound. This phenomenon has a huge impact on a series of properties were particle alignment in one favourite direction is highly desired, such as barrier permeability, electrical/thermal conductivity and anisotropic mechanical reinforcement.

G+ for tyres

The main application of G+ material in elastomers concerned its use as reinforcing nanofiller for tyre applications. The collaboration with Directa Plus in this project included the use of different types of G+ materials at various loadings (either in substitution or in addition to traditional fillers), the study of the impact of G+ morphology on the final compound properties and the fine tuning of the ideal mixing technology.

This activity was financed by Directa Plus within Project ATANOR (ID 30132114) which is a part of the programme "Bando di Invito a presentare Progetti di Ricerca Industriale e Sviluppo Sperimentale nei settori strategici di Regione Lombardia e del Ministero dell'Istruzione, dell'Università e della Ricerca." D.d.u.o. 29 luglio 2011, n.7128.

It was found that by incorporating a small quantity of G+ into tread compound for bicycle tires, the balance between the rolling resistance and the grip are greatly improved, with respect both to the same compound without G+ and to a standard commercial tread compound.

The motivation of this improvement relies on the fact that, in tread compound formulation, G+ allows the use of higher contents of polymers of a high elastic modulus with respect to other fillers (such as carbon black or silica). As a direct consequence, the rolling resistance of the final compound decreases, and the grip levels stays comparable to standard tread compounds thanks to the presence of G+ (tests made on real prototypes of bicycle tyres).

The effect of G+ on the dynamic properties of the tread compound is shown in figure 5.1. The storage modulus, E', was recorded as a function of strain amplitude (strain sweep analysis) for three different compounds: 1) "with G+", which is the compound containing a higher content of elastic polymers and G+ particles; 2) "without G+", which is the same formulation as 1) but without G+; and 3) "ref", which is a standard commercial tread compound used as a reference. The graph reported in figure 5.1 a) highlights the strain dependence of E', known as Payne effect, which is attributed to the breakdown and reformation of the filler network, accompanied by the release of the trapped rubber from the filler network. This mechanism of filler agglomeration and deagglomeration should be responsible for the energy dissipation process that occurs during dynamic strain. As a consequence, the gap between the highest (at low strain amplitude) and lowest (at large strain amplitude) plateau of E' ($\Delta E'$) is indicative of the degree of energy dissipation, and it should be as high as possible. In figure 5.1 b) the values of $\Delta E'$ for the three compounds are reported. Due to the surprisingly strong interaction between G+ particles within the polymer matrix, the degree of energy dissipation is much larger for the compound with G+ compared to the other two compounds.

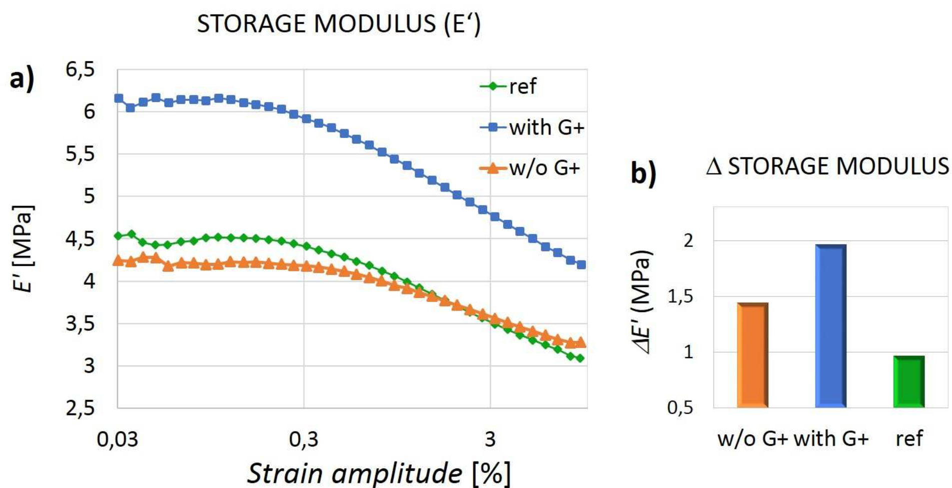


Figure 5.1: Strain sweep dynamic mechanical analysis (DMA), performed at 1 Hz, 60°C and 1-10 % of strain amplitude. a) Storage Modulus (E') recorded as a function of strain amplitude for three different tread compounds: formulation with G+ (with G+, blue), same formulation without G+ (w/o G+, orange) and commercial tread compound as a reference (ref, green); b) difference of E' values ($\Delta E'$) between its highest (at low strain amplitude) and lowest (at large strain amplitude) point for each compound measured during the strain sweep.

Moreover, the value of E' at very low strain is much higher than the values recorded for the other two compounds. E' is correlated to the overall stiffness of the polymer/filler system, thus also to the rolling resistance. This is because the cycles of deformation and recovery during tire rotation result in a hysteretic behaviour. At higher E', lower values of rolling resistance are expected.

These results represent an important breakthrough for all tyre applications since the reduction of rolling resistance is associated to smaller energy consumption; especially in the automotive field, tread compounds with lower rolling resistance would allow to consume less fuel thus lowering the CO_2 emission too.

Another important breakthrough was represented by the use of G+ nanoplatelets as physical barrier to gases. In particular, it was found that the permeability of natural rubber to oxygen decreases linearly by increasing the G+ content. At 30 parts per hundred of parts rubber (phr) of G+ the oxygen permeability is 70 % less than that of pristine natural rubber compound (figure 5.2). These values of air retention are very close to those of butyl rubber, which is a widely used elastomer in the production of inner tubes and inner liners because of its excellent air retention properties. The use of G+ as gas barrier in natural rubber compounds would allow to keep very high values of air retention and, at the same time, to exploit the well-known mechanical properties of natural rubber, thus contributing to improve the overall performances of the tyre.

Finally, the incorporation of G+ within various elastomeric systems lead to great improvements of both electrical and thermal conductivity. Recently, Araby and co-workers demonstrated the use of GNPs as

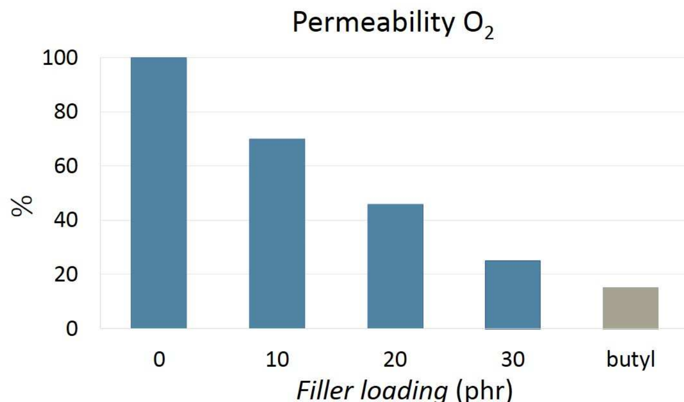


Figure 5.2: Oxygen permeability of natural rubber compounds at various G+ loadings. All values of permeability are normalized to the thickness of the sample and expressed as percentage of the unfilled compound. The permeability of butyl rubber compound (typical formulation for inner tubes, containing ∼60 phr of CB) is also indicated.

fillers to develop electrically and thermally conductive elastomers [127]. They mixed GNPs within styrene butadiene rubber (SBR) by a two-roll mill at room temperature. The resulting nanocomposite showed an improvement in thermal conductivity of 240 % (0.6 W/mK at GNPs vol. fraction = 41.6 %) with respect to the unfilled compound and values of electrical conductivity of $\sim 10^7$ Ωcm (at GNPs vol. fraction = 24 %).

In this experimental project we developed electrically and thermally conductive elastomers by incorporating G+ within silicon rubbers. The values of both electrical and thermal conductivity are higher at much smaller filler loading compared to the work reported in literature [127]. In particular, we found that the effect of G+ incorporation within the silicon matrix is significantly more pronounced than that of electrically

conductive carbon blacks available on the market.

Further and detailed technical data, which were produced within the collaboration with Directa Plus, are business confidential.

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