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Ultra-Low Power Wake Up Receiver For Medical Implant Communications Service Transceiver

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ULTRA-LOW POWER WAKE UP RECEIVER FOR MEDICAL IMPLANT COMMUNICATIONS SERVICE TRANSCEIVER

by

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DOCTOR OF PHILOSOPHY

Department: Electrical and Computer Engineering
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Major Professor: Dr. Numan S. Dogan
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ABSTRACT

Griggs, James. ULTRA-LOW POWER WAKE UP RECEIVER FOR MEDICAL IMPLANT COMMUNICATIONS SERVICE TRANSCEIVER. **(Major Professor: Numan Dogan),** North Carolina Agricultural & Technical State University.

The Medical Implant Communications Service (MICS) is an ultra-low power, unlicensed, mobile radio service for transmitting data in support of diagnostic or therapeutic functions associated with implanted medical devices. Medical devices that are implanted in the human body have limited size and battery capacity thus requires ultra-low power circuitry. Due to the power consumed by the radio transceiver when the system is active, system level power saving techniques such as "sleep mode" is very essential to achieve "low-power". A wake up receiver (WuRx) is used to detect wireless traffic directed to a node's receiver and activate it upon detection, without compromising latency and energy dissipation by maximizing data transceiver sleep time.

However, the WuRx power consumption must be small compared to the node's main transceiver because it remains active at all times. Due to the always on nature on the WuRx, it sets a power dissipation floor for the entire system, which requires the receiver design to utilize low-power mixed-signal circuits in the RF front-end and baseband circuit blocks. The WuRx employs various architectural and circuit techniques to minimize power while maintaining an acceptable sensitivity to detect the wake-up signal and preserving data throughput.

This thesis explores the specific requirements and challenges for the design of a dedicated wake-up receiver for medical implant communication services equipped with a novel “uncertain-IF” architecture combined with a high – Q filtering MEMS resonator and a free running CMOS ring oscillator as the RF LO. The receiver prototype, implements an IBM 0.18µm mixed-signal 7ML RF CMOS technology and achieves a sensitivity of -62 dBm at 404MHz while consuming <100 µW from a 1 V supply.

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DEDICATION

To My Heavenly Father. May you receive all the glory.

BIOGRAPHICAL SKETCH

James Griggs, a native of Dothan, Alabama, a doctoral candidate in the Department of Electrical and Computer Engineering at North Carolina A&T State University. His research focuses on analog circuit/MEMS design for RF communication. In 2001 James graduated with honors from Tuskegee University, with a B.S. in Electrical Engineering. While attending Tuskegee, James was involved in many activities and was recognized as an Eminent Scholar as well as University Scholar for the College of Engineering, Architectural and Physical Sciences, which honors the top ranking exemplary students from each college.

After Tuskegee, James went to graduate school at the University of Michigan, Ann Arbor where he received his Master's degree in Electrical Engineering in 2004. During his graduate studies at Michigan, James was awarded a scholarship through The National GEM Consortium, a competitive fellowship geared towards identifying highly qualified graduate students within the STEM fields. James is passionate about science and technology and decided to complete his doctoral studies in electrical engineering at North Carolina A&T State University as a Title III fellow.

Throughout his academic career James has been involved in professional and social organizations including Eta Kappa Nu (Electrical Engineering Honor Society), IEEE, and Golden Key International Honor Society.

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KEY TO SYMBOLS AND ABBREVIATIONS

AC	Alternative Current
AM	Amplitude Modulation
BER	Bit Error Rate
BW	Band-Width
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DR	Dynamic Range
DSB	Double Side Band
DUT	Device Under-Test
EIRP	Effective Isotropic Radiated Power
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
FCC	Federal Communication Commission
FET	Field Effect Transistor
FM	Frequency Modulation
FSK	Frequency Shift Keying
I/Q	In-phase/Quadrature-phase
IC	Integrated Circuit
IF	Intermediate Frequency
IGFET	Insulated-Gate Field-Effect Transistor
ISM	Industrial, Scientific and Military

IMD	Implantable Medical Devices
ITU-R	International Telecommunication Union – Radio-communications
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Loop Filter
LPF	Low Pass Filter
MICS	Medical Implant Communication Service
MiM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
PLL	Phase Lock Loop
SoC	System on Chip
TRX	Transceiver
TTL	Transistor-Transistor Logic
TX	Transmitter
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
WuRx	Wake-Up Receiver
WB	Wire-Bond
WiseNet	Wireless Sensor Network
WTMS	Wireless Telemetry Service

CHAPTER 1
INTRODUCTION

1.1 Body Area Network

As the design and development of integrated circuit technology has evolved, so has the design of medical implantable devices. The evolution of circuit technology has facilitated highly complex embedded systems and smaller medical device sizes. Current advancements for implantable medical devices (IMD) are now exploiting wireless communication technologies. These strategically placed devices can gather real time data or alert of significant changes within the human environment. These embedded systems include low power radio frequency circuits, energy harvesting techniques, system on chip design, and incorporating Micro-Electro-Mechanical Systems (MEMS) devices. The combination of these advances has contributed to the creation of Wireless Body Area Networks (WBANs). WBAN was first presented in 1996 as a viable wireless communication protocol for medical applications to improve utilization of medical devices such as pacemakers, neuromuscular stimulators, micro-drug delivery devices, cochlear implants and visual prosthesis [1]. All next generation medical devices will have the capability to be controlled remotely through a wireless network. WBAN provides a proactive approach creating a healthcare revolution that allows prevention, early detection or outpatient therapeutic treatments for diseases.

As IMD's become more prevalent there is an increasing need for these devices to support the formation of body area networks. A WBAN is a collection of miniaturized, invasive and non-invasive wireless sensor nodes that monitor the human body functions

and external environment. Each device is configured to continuous, automated and unobtrusively monitor physiological signs which can be collected and processed. The information can be relayed to a base station or PDA for diagnosis and prescription. WBAN would allow physician to monitor patients within their natural physiological state, with the ability to maintain their normal daily activities without restriction. In addition, it can be used to implement an affordable health care system that can diagnose procedures, provide maintenance for a chronic condition, allow supervised recovery from a surgical procedure and handle emergency events.

1.2 Medical Implants Communication Service Band

Use of wireless communications for some of these applications has been approved by the U.S. Federal Communications Commission (FCC). In 1999 the FCC established the Medical Implant Communications Service band that specifically applied to transmitters that support the diagnostic and/or therapeutic functions associated the implantable medical devices to enable individuals and medical practitioners to utilize potential life-saving medical technology without causing interference to other users in the spectrum[2]. The Commission set aside 402-405MHz band specifically for several reasons. 402-405MHz allows development of low-power transmitters and antennas designed for the MICS band that can be made small enough and still have reasonable performance range typically having a communication link ~3-10 meters. With 300 KHz channels spread across the MICS spectrum, enables the wireless communication of

Table 1.1 Characteristics of Wireless Network Technologies Coverage

Network	Coverage	Data Rate	Applications	Technologies
WWAN	> 10 km	< 10 Mbps	Mobile Internet, telephony	Satellite, GSM, UMTS
WMAN	< 10 km	< 100 Mbps	Broadband	IEEE 802.16
WLAN	< 1 km	< 100 Mbps	Hot spots, Ethernet replacement	IEEE802.11
WPAN	< 10 m	< 10 Mbps	Data Transfer	Bluetooth, IEEE802.15.4
WBAN	< 2-5 m	< 1 Mbps	Health Monitoring	Proprietary

medical devices to achieve sufficient transmission rates. The MICS band has signal propagation characteristics that are particularly well suited for implantable applications due to the signal propagation characteristics for the transmission of radio waves within the human body. Because the human body is not a good media through which electromagnetic waves transmit due to the body's high electric conductivity, this results in a large path loss in the transmission of energy from the implant to free air space. This characteristic is also a challenge for continuously monitoring applications; the signal may go across several access points into multiple networks such as Bluetooth, Zigbee, and WLAN. Table 1.1 shows the classification of wireless networks according to their coverage.

The MICS band does not possess a significant risk of interference to other radio operating within the band and is recognized internationally for medical device applications. MICS transceivers are expected to be used in medical implant devices such as cardiac pacemakers, implantable cardio-verter defibrillator, neurostimulators, hearing

aids, and automated drug delivery systems. Recent progress in CMOS IC technology allows wireless transceiver designs that are high reliable, cost effective, and ultra low in power consumption. The MICS band is already compatible with devices governed by European Telecommunication Standards Institute (ETSI) thus implantable medical devices can be maintained wherever they are in the world.

1.3 WHY MICS was established?

Before the implantable medical devices could communicate wirelessly, communication with the device is often done through magnetic (inductive) coupling methods. Magnetic coupling systems have data rates ~1-10 Mbps and transmission ranges of only a few inches. Also a magnetic system requires the external monitor, which consumes a lot of power, needs to be placed close to the patient, usually in contact with the skin and/or directly over the implant in order for the data communication to occur. The device using inductive coupling within the body can only support one way communication from within the body. Another limitation of medical implanted devices is that since they are magnetically coupled to an external unit, they could easily be affected by electromagnetic interference (EMI). EMI represents a major risk to patient safety and medical effectiveness due to the increasing usage of electromagnetic energy radiating devices such as cell phones and security systems. According to the reports of the Center for Devices and Radiological Health under the US Food and Drug Administration (FDA), it was estimated that about 500 incidents were suspected to be attributable to EMI affecting cardiac devices. More than 80 of these reports involved cardiac and other medical device interactions with electronic security systems. EMI represents a major risk

to patient safety and medical effectiveness due to the increasing usage of electromagnetic energy radiating devices such as cell phones and security systems [3]. WBAN technology overcome these limitations by exploiting the MICS bandwidth which offers a faster data transfer rate and longer link range. The physician can extract information quickly, and the patient benefits greatly from the expanded freedom of movement.

General Transceiver Characteristics

ITU-R Recommendation SA.1346 (7) sets out recommended characteristics for MICS devices to facilitate sharing with stations operating in the Meteorological Aids service in the band 401-406 MHz[4]. The recommendations include:

A. limiting MICS devices to a maximum of -16dBm equivalent isotropically radiated power (EIRP) in a reference bandwidth of 300 kHz to prevent interference to meteorological aids; and
B. that MICS utilizes a range of interference mitigation techniques to minimize the impact of meteorological aids on their operation.

The recommendation identifies a number of possible interference mitigation techniques that MICS devices might use including:

A. avoiding a false activation; the implanted device should use techniques such as requiring activation by a strong magnetic field;
B. when the system is used for home monitoring, the system could poll at long intervals;
C. the use of multiple error correction codes and automatic repeat requests to avoid impulsive interference and ensure sent and received data is accurate; and

Table 1.2 Characteristics of Wireless Network Technologies

Controller Unit	
Receiver noise bandwidth	200 kHz
Antenna Gain Tx/Rx	2 dBi
Power Into Antenna	-22 dBm
Tx Power	-20 dBm EIRP
Required SNR	14 dB
Noise Floor	-101 dBm
Ambient noise at receiver input	20 dB above kTB
Receiver noise figure	4 dB
Implanted Unit	
Receiver noise bandwidth	25 kHz
Antenna Gain Tx/Rx	-31.5 dBi
Power Into Antenna	-2 dBm
Tx Power at the surface of the skin	-33.5 dBm EIRP
Required SNR	14 dB
Noise Floor	-121 dBm
Ambient noise at receiver input	About kTB (due to tissue loss)
Receiver noise figure	9 dB
Transmission Losses	
Free space loss at 2 meters	30.5 dB
Fade margin (with diversity)	10 dB
Excess loss (polarization, etc.)	15 dB
Building penetration loss	20 dB

D. avoiding narrow band interference using frequency agility and techniques where the MICS equipment chooses a channel based upon the lowest ambient noise level.

This last technique also reduces the possibility of MICS equipment causing interference to other services by avoiding channels known to be in use. MICS communications sessions are required to be initiated by a programmer/control transmitter, except for a communications session resulting from a "Medical Implant Event". A medical implant event is one that requires the medical implant device to transmit data immediately in order to protect the safety of the person in whom the medical implant device has been placed.

The key technical and operational conditions proposed for the use of MICS transmitters are:

- Band of operation: 402-405 MHz.
- Maximum EIRP: 25μW – this limit to apply in any 300 kHz bandwidth.
- Operation on a non-interference basis.
- Transmitters in implanted devices to transmit only when commanded to do so by external programmers/controllers, except for medical implant events.
- Programmer/controller devices to operate on a listen-before-transmit basis to identify and use the communication channel of lowest ambient noise.
- Frequency agility to enable communication to occur on the lowest ambient noise channel determined to be available.

Based on the recommendations, a MICS transceiver should have the characteristics listed in Tables 1.2 [5] . They are the specifications for the MICS programmer unit and the MICS implant unit respectively and lists the transmission losses for overall MICS transceiver[5].

1.4 Wake-up Receiver Design Considerations

The implementation and specification for the WuRx depends on the application for which it is design for. Candidate applications of WuRx may include wireless networks such as WSN, radio frequency identification (RFID) technology, Zigbee, Bluetooth, Bluetooth Low Energy (also known as Wibree), and wireless personal area network (WPAN), wireless local area network (WLAN). There are several factors that should be considered when designing a WuRx for a WBAN device.

Low power consumption: IMDs are either battery-less and needs to have continuous power from an external portable battery, or use miniature rechargeable batteries that inductively charges on a regular basis [6]. Regardless of the method the power transmission should be highly efficient to maximize the battery lifetime. This not only preserves the power supply but also minimize the size of the battery and overall IMD thus protecting internal tissue from heat dissipating from the device and limiting the exposure to the electromagnetic field. Ultra-low power and efficient designs must be used because the power capacity is directly proportional to device size.

High Reliability: Reliability must be a very high priority, as if any failure of the WBAN device occurs it can result to inconvenience, pain, damage organs or even death. Maintenance is also high risk to the patient and costly.

Small size and cost: the size of medical devices must be as small as possible so that the device is unobtrusive and maximized portability, especially constrained depending on anatomical region in which the devices will reside. In order to make a

practical implementation using few external small-sized components will also reduce the cost of parts as well.

Minimize false wake up signals: Each WuRx must to be able to determine the difference between an unwanted signal and the wake up signal. Also should have the capability to distinguish between wake-up signals in the form of wake-up packets. This will give WBAN devices addressing abilities in order to interrogate a specific device.

1.5 Duty Cycle Control for Sensors

Power consumption reduction is a primary goal when designing WBAN systems. IMD must perform such functions as computation, sensing and actuation. However when these components have been integrated into the system, the wireless communication energy is still dominant [7]. Thus the goal of this research is to reduce the energy dedicated to communicate to WBAN devices. Within WBAN networks packet traffic rates are generally low with small bits of data exchanged. Packets themselves are short; data packets with 200 bits or less of information is typical. The amount of data to be transferred depends highly on the network traffic and network application. Typically within WBAN application most of the sensing and monitoring application follow a general form that incorporates sparse communications with long periods of idle time.

The Physical layer protocol (PHY) design requires minimizing power consumption without degradation in terms of latency, data loss and throughput. In order to reduce power consumption within medical implantable devices they are heavy duty cycled, meaning the device spends majority of its time in a low power sleep mode. For communication to begin there has to be some way for the devices to activate

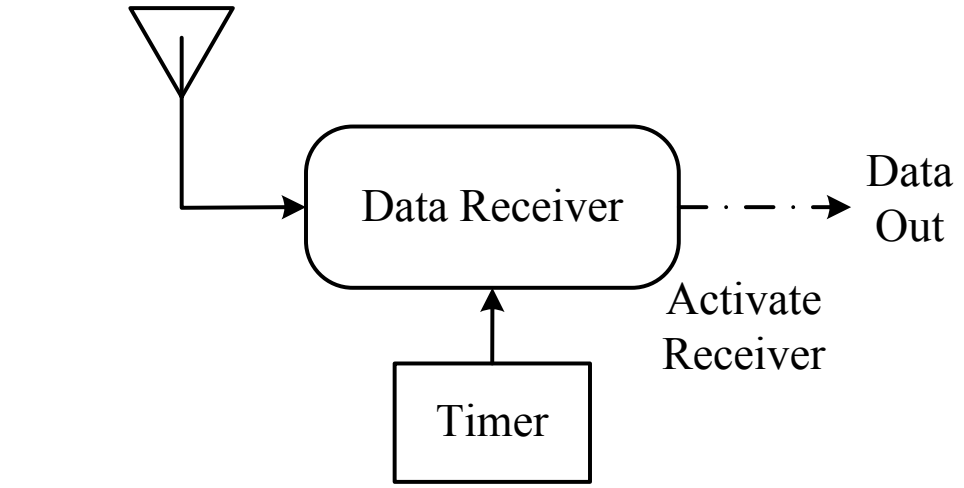
simultaneously, the communication event is referred to as rendezvous. There are two main ways for overcoming this challenge a synchronous protocol can be implemented which uses a global clock as a reference and is shared between devices that allow the communication channel to come alive only for a certain time period. By limiting the period of time the electronic device needs to perform a given function can reduce the average power consumption by orders of magnitude. The difficulty with this protocol is that to maintain a distributed clock signal within each individual WBAN device is challenging. Moreover the energy needed to maintain a global synchronization can be significant because the device will wake up even if there is no packet to transmit or receive. This results in idle listening and overhearing.

Alternatively a pseudo-asynchronous duty cycle method can be utilized; this avoids/removes the need for a remote synchronization by using a request based protocol to control duty cycle and set-up communication between devices. As shown in Figure 1.2, this request can be initiated by either the transmitting or the receiving device. With this protocol based duty cycle the receiver is set on a timer to limit the time that it is active, while active the receiver monitors the channel for communication. If there is no communication signal received then the receiver returns to sleep. For the transmitting device to communicate it sends repeated requests until the receiver is active and detects the request. When these two events coincide, then data can be exchanged, though the asynchronous protocol eliminates the need for a global clock (synchronization), a significant amount of energy has been expended by both the receiver and the transmitter; the receiver by monitoring the channel and the transmitter by sending out requests or

beacons. Both methods synchronous and asynchronous show a trade-off between power consumption and latency. Latency is the measure of time delay experienced in a system.

To create a bridge between these two tradeoffs an alternative method can be implemented by employing an addition auxiliary receiver called a wake-up receiver (WuRx) for each device thus employing a pure asynchronous rendezvous protocol. The wake-up receiver is totally dedicated to monitor the channel it is tuned for, monitoring communication requests and wake-up signals. Because the WuRx is listening continuously, the WuRx can respond more quickly thus significantly reducing latency. The power that was expended by the repeated beaconing on the transmit side and the periodic monitoring on the receiver side is replaced by the power consumption of the WuRx. Because the WuRx is not duty-cycled, its active power consumption needs to be very low to ensure that the power used does not dominate the overall power of the link. The WuRx would reduce the turnaround time from transmit state to a receive state and create a faster wakeup from sleep mode which would help with power savings.

The most elementary and lowest power consumption wake up circuit is presented in [8]. Gu et al. presents and simulates a zero-power radio-triggered hardware that uses a multiple-stage charge pump that receives energy from radio signals that initiates a wake-up signal to the network node without using an internal power supply. This approach is realized using Schottky diodes. However, it is not capable of RF filtering nor selectivity of the wake-up signals. Without this function whenever there is a RF activity event within communication proximity of the node, it can trigger a wake up interrupt for the receiver. This result would lead to a higher overall power consumption since the micro-



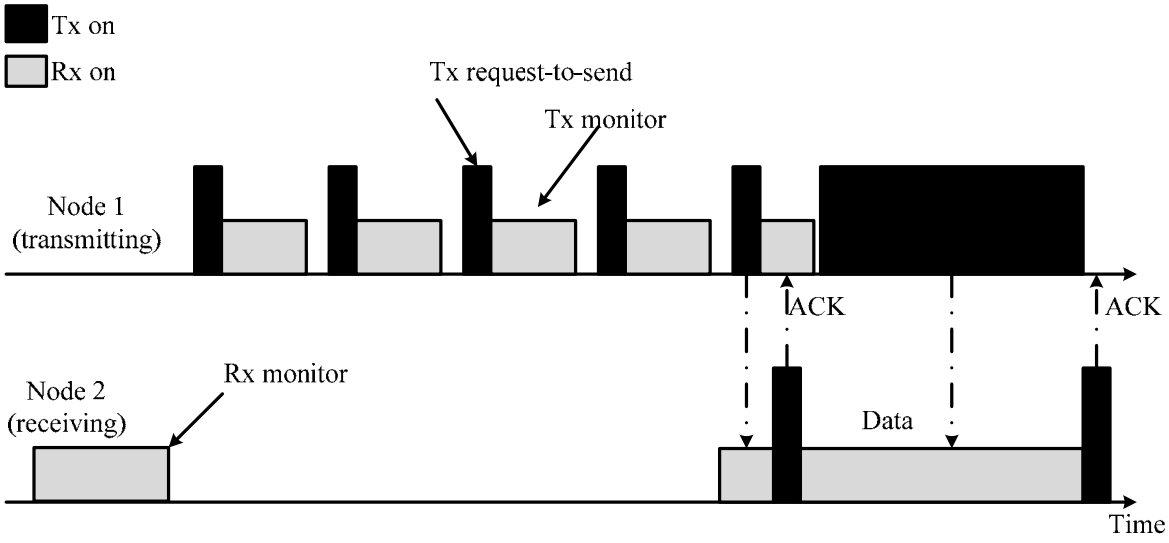
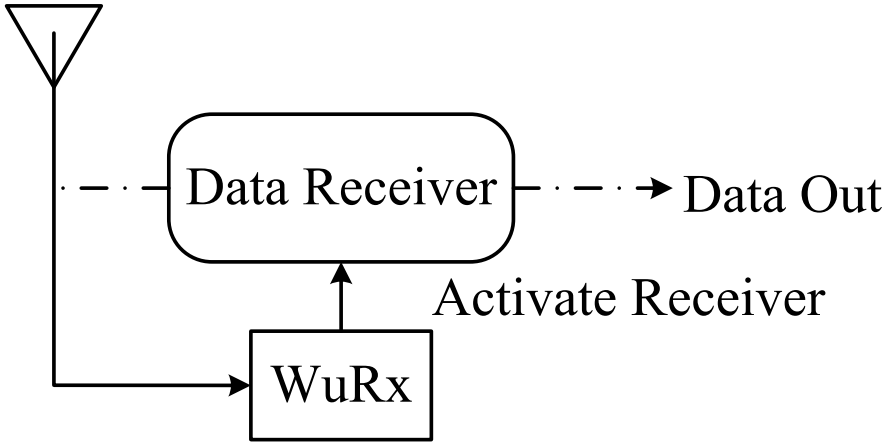


Figure 1.1 Protocol-based duty cycle control: transmitter initiated



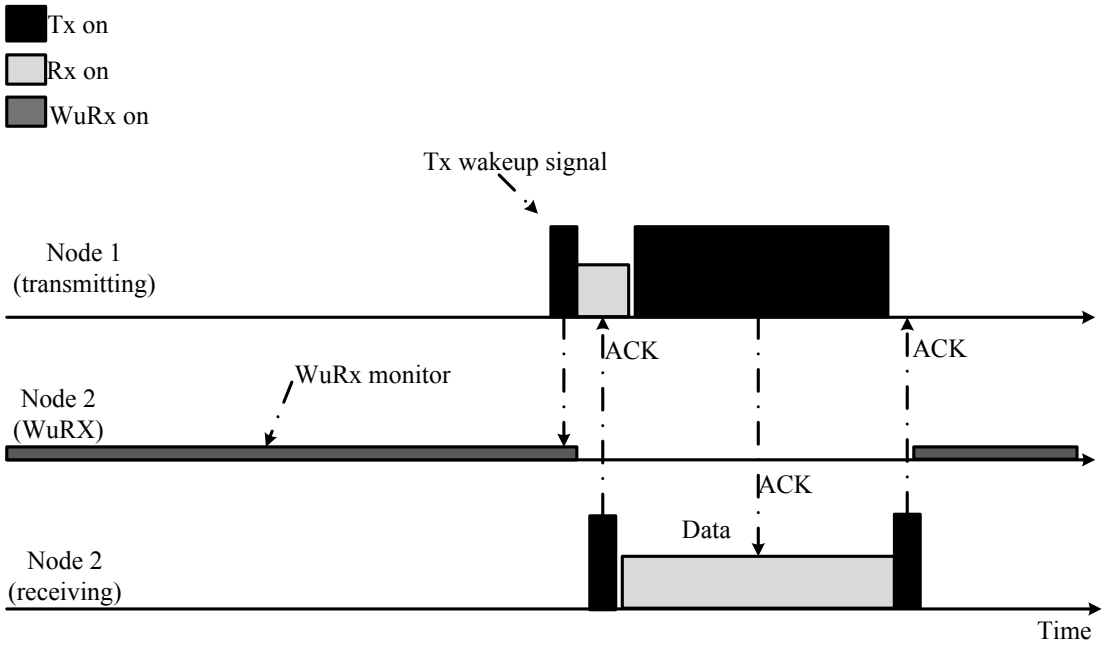


Figure 1.2 Duty-Cycle control with wake-up receiver

circuitry and the regular receiver has been awaken to decide if the wake up was intended for the sensor every time it occurs. Therefore, for each wake-up signal event, the sensor nodes in the vicinity switches on the transceiver, consuming energy to test if the signal is meant for it. Another approach similar to is based on a MOSFET with a sensitivity of −29dBm and a current consumption of 2.6 μA this work is presented in [9]. Also, a battery assisted semi-passive RFID wakeup solution also falls within this group as well. Another design with a "power on" circuit based on a multi stage charged pump is presented in [10]. A wake up circuit with static power consumption of 4.8 μW and with high sensitivity (−65dBm), is presented in[11]. Marinkovic et. al presents a WuRx that has a power consumption of 8nW with a sensitivity of -51 dBm. Within the WBAN radio spectrum, IMD are susceptible to significant interference from other various wireless network devices found in the vicinity, and as WBAN technologies grow there will be an increasing number of sensors that require wireless interlinking. Therefore, a more sophisticated WuRx, with addressing capabilities and high interference rejection is needed. A low power wake up receiver that has addressing capabilities and is closest to our implementation regarding the power consumption is presented in [12]. A different solution based on an envelope detector and a programmable amplifier is shown in [13]. It has a dedicated FPGA for digital decoding and preamble detection. The data is transmitted serially and it has no standardized connection. The static power consumption of 12.5 μW and sensitivity/data rate of −57 dBm and 100 kb/s are reported. A similar solution with an envelope detector and amplifier is reported in[13]. It has a power consumption of 96 μW, but it does not have wake up signal decoding. The design

Table 1.3 Wake-Up Receiver Comparisons

	Detector power†	Decoder power†	Operating Frequency	Data Rate	Sensitivity	Interference filtering
This work	60μW@1.0V	60µW	405Mhz	100kbs	-62dBm	resonator
Marinkovic[11]	0.27 µW@1.5V	8 nW	433.92 MHz	2 to 80 kb/s	−51 dBm	Preamble detector
Ansari [14]	2.6 μW@3V	μC dependent	869 MHz	0.75 kb/s	N/A	Microcontroller
Durante[15]	12.5 μW@1.5V	5 μW	2.4 GHz	100 kb/s	−57 dBm	FPGA
Pletcher[16]	52 μW@0.5V	N/A	2 GHz	100 to 200 kb/s	−72 dBm	BAW resonator
Doorn [13]	96 μW@1.5V	50 μW	868 MHz	0.862 kb/s	−51 dBm	SAW
Le-Huy[17]	17.8 μW @ 3V	0.8 μW	2.4 GHz	50 kb/s	−53 dBm	None
Takiguchi[18]	12.4 μW	N/A	950 MHz*	40 kb/s*	N/A	Bloom Filter

* - Simulated values; † - Static power consumption (When in listening mode)

requires an active microcontroller with constant analog to digital conversion (ADC) to do the signal decoding, which further increases the power consumption. Finally, [16] presents a high sensitivity solution (−72 dBm) and good (0.5nJ/bit) dynamic power consumption, but it has a static power consumption of 52 µW. It is mainly targeted for Wireless Sensor Networks with higher ranges than WBAN, and higher power consumption requirements. Table I presents a comparison of our receiver with low power wake up receivers with addressing mechanism both realized and tested [14] ,[15],[13] and [16] or simulated in detail [17] and [18] .

All values in the table are extracted from the referenced papers, and no assumptions were made. These wake-up receivers have higher power consumption than our WuRx. Some of them have better sensitivity or data rate, but none of them is as well-suited for WBAN as the WuRx presented here. We compared only the static power

consumption, since most of the compared works do not have a detailed analysis of dynamic power consumption and energy per bit.

1.6 Functional Specifications

A WBAN wake-up receiver must be able to communicate over the same range as the data receiver. If the transmitter and receiver are not within the communication distance then it would be impossible to wake up the node to receive data otherwise. As stated earlier for the WBAN Pico-network the data link range should be ~2m – 10m with a transmitter output data of about -16dBm.

The power consumption specification relies heavily on the maid data transceiver power, but also the on the network traffic conditions and desired latency. Different type of duty cycle rendezvous strategies are compared on the basis of average power and network latency.

$$L_{FS}= \left(\frac{\lambda}{4\pi}\right)^2 \left(\frac{1}{d}\right)^n \tag{1.1}$$

Where λ is the wavelength of the carrier frequency, *d* is the link distance, and *n* is the empirical path loss exponent. Assuming transmitter output power of -16 dBm (25μW), λ= 74.5cm and *n* = 2, Equation 1.1 gives a link distance of about ~4 meters for a receiver with an -34 dBm sensitivity. For effective WBAN channel conditions, the receiver sensitivity should be at least -51 dBm.

A wake-up receiver essentially functions as a single bit receiver that detects an event and then activates the data receiver. At its most fundamental level the wake-up event could simply detect the RF energy. For security and reliability implementation, the

WuRx should be more than just a simple energy detector. The transmitted signal would most likely be sent as a packet with a particular bit sequence, which allows selective wake-up among WBAN devices to avoid false alarm triggers by regular data communication between neighboring devices.

It is important to understand the link budget for the desired carrier frequency. A link budget is the account of the gains and losses from the transmitter through the medium (free space, body tissue, bone, etc.), to the receiver. For IMD the general link budget formula is [19].

$$P_{RX} = P_{TX} + G_{TX} + L_{FS} + L_B + G_{RX} \tag{1.2}$$

Where P_{RX} is received power (dBm); P_{TX} is transmitter output power (dBm); G_{TX} is transmitter antenna gain (dBi); L_{FS} is free space loss or path loss (dBm); power L_B is losses within body tissues (dBm); and G_{RX} is the receiver antenna gain (dBi). Assuming an MICS channel of 402.5MHz and a transmit and receive distance of 4 – 5 meters and typical implants are about 1cm below the fat layer, using [20] we can estimate the power loss within body tissue to be approximately -8dBm. Combining antenna transmitter and receiver gains which are reported to be in the range of 7-10dBm. The power for the receiver antenna can be approximated.

$$P_{RX} = (-16) + (-34) + (-8) + (7) = -51\ dBm.$$

The approximated received power level can be used as a design input for the sensitivity of the WuRx. A sensitive receiver permits communication over a longer

Table 1.4 Wake-up Receiver Target Design Specifications

Parameter	Value
Network architecture	Narrowband
Carrier frequency	~402.5 MHz
Modulation scheme	OOK
Data Rate	100 kbs
Sensitivity	~-51 dBm
Power consumption	Minimize (≤100μW)

range. However it may consume more power and hence decrease battery lifetime. Therefore the ideal wireless medical system design should balance between longer communication ranges with respect to battery longevity of the implantable devices. Therefore the goal of this research is to implement a WuRx with less that 100μW active power. The specifications are summarized in Table 1.4 Battery life can be saved by employing an optimal wake-up protocol.

1.7 System Integration

At the system level, the wake-up receiver must seamlessly integrate with the rest of the WBAN's electronics. A conceptual diagram of a WBAN device in sleep mode is shown in Figure 1.3. During sleep mode, most of the electronics may be powered off, with the exception of the WuRx and any required power management circuitry. For a system device integration perspective, it is preferred for the WuRx to share the same antenna with the other wireless blocks. To reduce hardware requirements and minimize size, the WuRx must be able to receive signals from the same transmitter used for data communications, without requiring a separate wake-up transmitter antenna. Therefore,

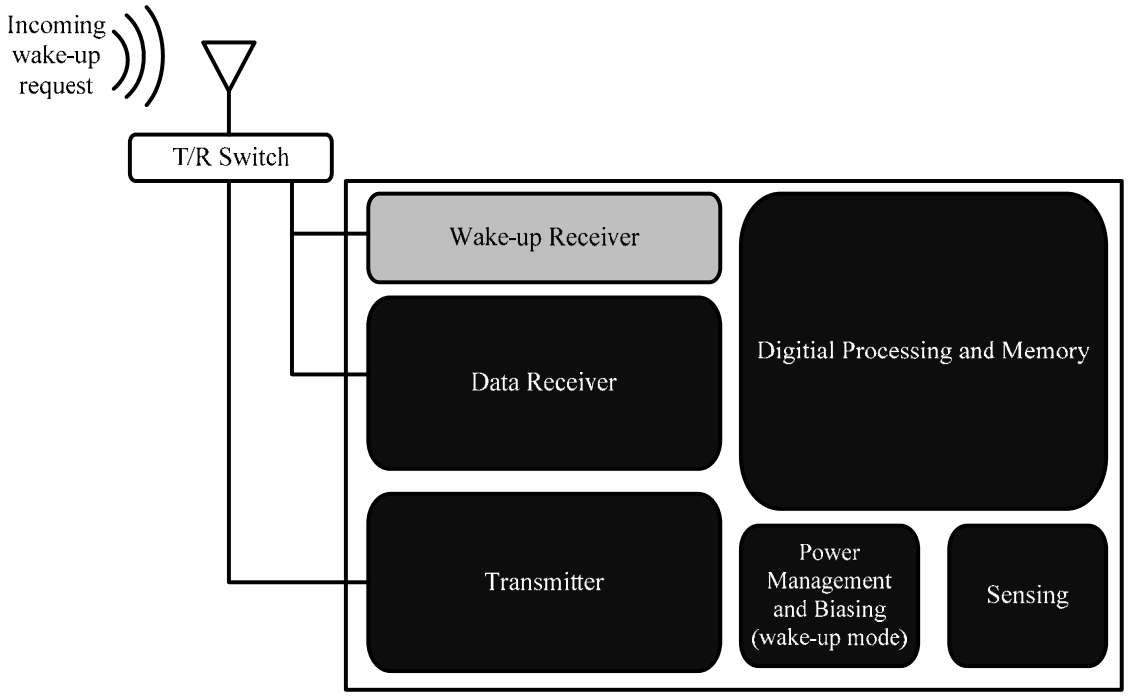


Figure 1.3 Block diagram of sensor node electronics in sleep mode

any practical WuRx implementation will use the carrier frequency and modulation scheme as the main data transceiver.

1.8 Network Environment

In a dense network environment such as the human body, the wake-up receiver is expected to operate as shown in Figure 1.4. At any given moment a wireless device will be communicating, but many will be in deep sleep mode, only monitoring the channel for wake-up requests from other nodes. In this environment, the wake-up receiver must be robust to ambient traffic in the network and avoid waking up on signals intended for neighboring nodes. From a functional perspective, the WuRx design is not concerned with bit error rate performance as in standard receiver. Instead, the performance metrics of interest are probability of detection and conversely, probability of false alarms (FA). A

missed detection means that the transmitter must re-transmit the wake-up request, increasing power and latency. A false alarm is also costly from a power perspective because the main data receiver is activated needlessly.

The two main objectives of this research are; (i) to design a general-purpose ultra-low-power Medical Implant Communication Service wake-up receiver; (ii), to explore novel design techniques provided by low supply voltages for power reduction in RF integrated circuits.

CHAPTER 2
DESIGN SPACE CONSIDERATIONS

2.1 Architecture Consideration

From the previous chapter, specifications were outlined on the functionality and power consumption for a dedicated wake-up receiver. Given that the power specification are very stringent, in the range of micro to nano-watts, in order for the WuRx to have any practical implementation both creative and novel methods have to be utilize. To move forward, one must first consider the fundamental limitations of contemporary integrated circuits while exploring other available design space. Outlined in this chapter are wireless receivers architectures available, which are used for wake-up receiver implementation, highlighting the factors limiting the power consumption for each design. With the rapid advancement of integrated circuits (ICs) fabrication technology, these developments are not limited to this specific area alone. Recent progress in the area of micro-electromechanical systems (MEMS), has developed in such a way that by exploiting this design space, along with combining the two, allows one to explore new opportunities to reduce power, and bypass the limitations poised by integrated inductors in designed to be used in RF circuits.

There are two groups of RF wake up systems and depending on the intricacies of the design determines power consumption with respect to channel sensitivity. The more complex the receiver is the higher its sensitivity to detect RF activity, but these designs suffer from high power consumption. While the more simplistic design such as an RFID

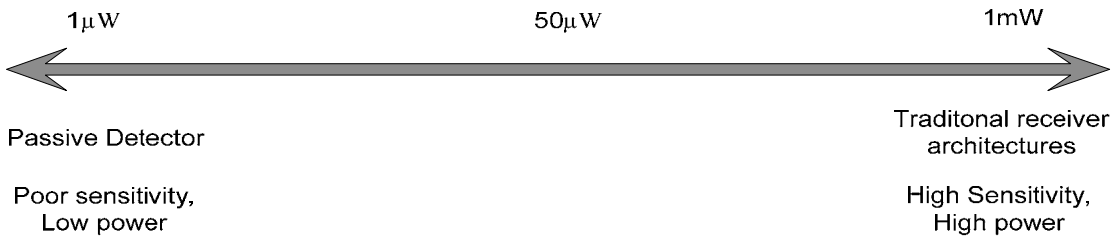


Figure 2.1: Receiver design space in terms of power consumption

system like the one in[8] which is realized using Schottky diodes uses no power but poor sensitivity and response to and RF event. Figure 2.1 shows this trade-off of power consumption versus performance.

Passive detectors are at the low end of the continuum, devices such as RFID tags are the simplest and are the lowest power receivers. These passive tags derive their power from the incoming RF waveform, and then store the energy which it uses to power up its electronics to decode the incoming signal and transmit back to the reader. However in this approach there is no RF filtering nor an addressing mechanism nor any channel selectivity for the wake-up signal. This device would activate every time there is a nearby RF event which can trigger the receiver. This unintentional wake-up event would active all the devices within its vicinity, the device activate theirs transceivers and consume energy attempting to test to see if the signal received was meant for them. The false alarm (FA) event wastes power.

For most WBAN systems the sensor network links are infrastructure nodes where all communication traffic is feed-through an access point or a base station which forwards the signal to the intended recipient. The sender and the receiver must be in range of each other thus the power of the transmitter cannot be ignored. To quantify the effective power needed for the transmitter in an RFID system let us examine the work

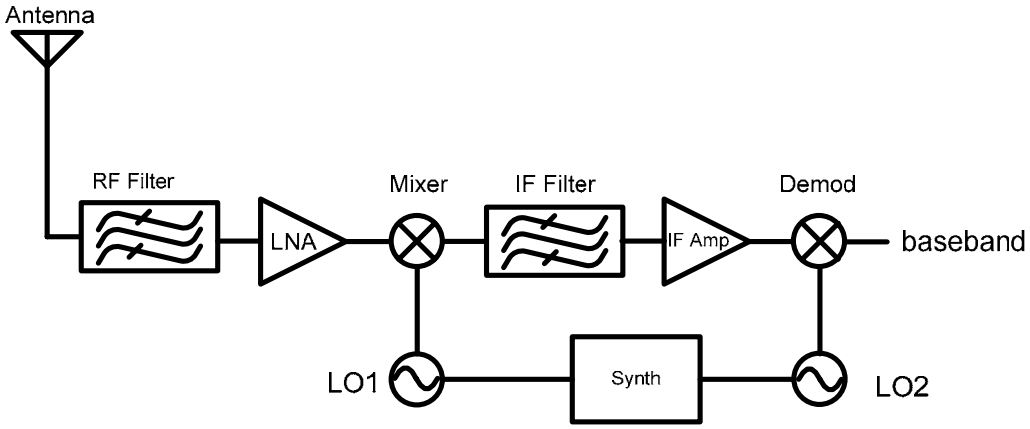
used in[21] as an example for an RFID tag design. The active power consumption for a RFID tag is ~1μW and this power is below the WuRx power budget. However the tradeoff is poor RF sensitivity, reported at -25.7 dBm on a 300 Ω antenna. In order to overcome the poor sensitivity one can simply raise the transmitting power from the reader antenna. To communicate with a tag over a distance of 10 meters, the reader must transmit 34.5 dBm output power (Pout) at the tune 2.4GHz. The average power P_{tx} is expressed as:

$$P_{tx} = \frac{P_{out}}{\eta}\frac{N}{R}\frac{1}{T_{wu}}, \tag{2.1}$$

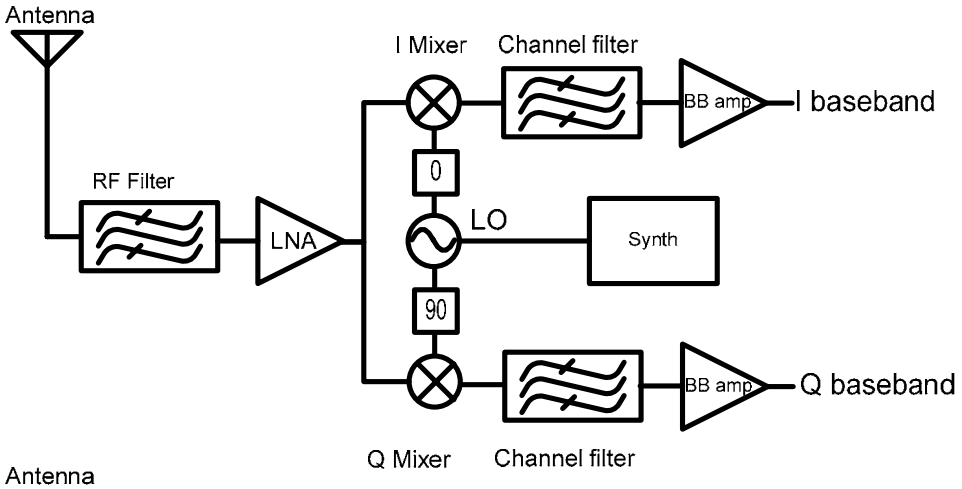
where η is the transmitter efficiency, and R is the data rate in bits per second, T_{wu} is the duty cycle for the reader sending a wake-up signal and N is bit sequence length. Assuming that the average power on the transmit side is 425μW with an BER=100kbs. For a peer to peer network this scenario where the transmitter is power-constrained, this power level is much too high. Poor sensitivity for the receiver tag is the primary cause for the high transmit power requirement. RFID receiver tags are appealing due to their low power consumption however a practical WuRX design will require a better sensitivity in order to avoid shifting the burden of power consumption to the transmitter and cause inference with neighboring bands.

2.2 Traditional Receiver

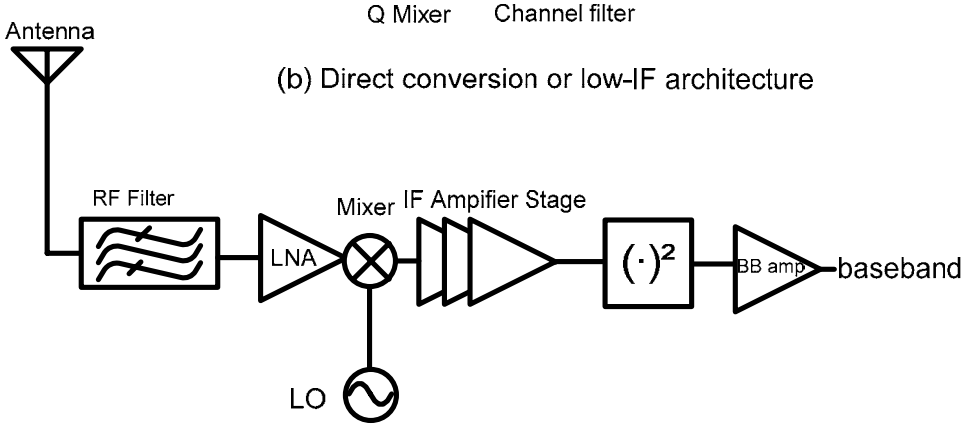
Traditional wireless receiver development is placed on the other side of the spectrum and they employ active devices that increase sensitivity and data throughput which surpasses what is possible with passive detectors. Receivers architectures can be grouped into three main categories and these architectures are marked as "traditional" or "conventional" architectures due to the fact that their basic structure have not changed substantially even though the implementation has become more complex over the years. A brief overview will be presented on narrowband receivers: To start, ultra wide band architectures are not the best fit for requirements that implements a wake–up application due to the high power consumption and long synchronization times. The most common types of receiver implement a frequency conversion, where the input signal is shifted to a lower frequency, to ease design constraints for signal processing blocks such as gain and filtering. The super-heterodyne architecture shown in Figure 2.3(a) utilizes two separate down conversion operations. First, the input RF signal is amplified by a low noise amplifier (LNA) in order to ease the noise requirements of the rest of the receiver chain. Afterwards the RF signal is converted to the intermediate frequency (IF) with a high-accuracy, tunable local oscillator (LO). This IF signal is amplified and filtered with a low pass filter to remove the image.



(a) Super-Heterodyne Architecture



(b) Direct conversion or low-IF architecture



(c) Envelope Dectector (uncertain-RF) architecture

Figure 2.2 Block comparison of popular receiver architectures

band and interferers signals. The second mixer converts the signal to DC using a fixed frequency oscillator at the IF frequency.

To avoid the image problem when using Zero-IF and low-IF receivers shown in (Figure 2.2(b)) the RF signal is mixed directly to baseband using quadrature down-conversion because in general the two side bands of the RF spectrum are different. The homodyne architecture advantage over the heterodyne is the intermediary IF stages are removed and the need for the IR filter is eliminated. The removal of the IR filter removes the LNA requirement to drive a low impedance load. Similar to the super-heterodyne architecture, an RF LO with high spectral purity and stability is required to drive the mixer. The main drawback of these architectures is their power consumption, along with super-heterodyne, each architecture is fundamentally limited by the RF oscillator and synthesizer. Due to strict frequency accuracy and phase noise performance, each structure requires a resonant LC oscillator which is usually embedded in the phase-locked loop (PLL) circuitry. Because of the limited quality factor (Q) of integrated passives this leads to a power floor of a few milliwatts.

To explore this further, a low-IF receiver implementation described in [7] is considered. To save power, the design eliminated the typical LNA and feeds the RF input directly to the quadrature down-conversion mixers. The mixer consumes DC current due to the mixing circuitry using MOSFET switches as a passive switching network. Following the mixer, the receiver circuits processes the baseband signal at the lower IF frequency (less than 1 MHz), thus these amplifiers consume little power. The last remaining system block is the oscillator which is used to drive the LO port of the mixers.

The oscillator operates near the RF channel frequency with high accuracy and stability, while simultaneously driving the gates of the mixer switches with a large amplitude signal (ideally a square wave). For quadrature operation, the voltage-controlled oscillator (VCO) must provide both in-phase and quadrature outputs. Because of all the responsibility for the LO, the LO results in more than 80% of the overall power consumption in the receiver. Despite the use of a large modulation index to eliminate the need for a complete PLL, the VCO itself still consumes more than 300 μW in single-phase, non-quadrature mode. This figure is several times higher than the power budget for the entire WuRx. For the receiver to be implemented for WBAN devices the power devoted to the RF oscillator must be drastically reduced. As an alternative to frequency conversion architectures, the simplest receiver can be implemented with just RF amplification and an energy detector, similar to the first AM receivers. This architecture, also called envelope detection receiver, reduces the power requirement for the LO and moves it to the RF front end (Figure 2.2(c)).

There are two main limitations with the envelope detection architecture, one factor is that the self-mixing operation will be insensitive to phase and frequency, selectivity must be provided through narrowband filtering directly at RF. Second, a high RF gain is necessary to overcome the sensitivity limitations of the envelope detector, usually implemented with a nonlinear element like passive devices or a diode. The envelope receiver is essentially an enhanced implementation of the simple diode rectifiers used in RFID tags, as shown they tend to have poor sensitivity and not adequate for WBAN application. The additional high frequency gain requires too much power, so the

envelope detector receivers usually exhibit inferior sensitivity compared to heterodyne mixing architectures for the equal power consumption. In [22], the authors take advantage of the simplicity of the envelope detector architecture to implement a two-channel receiver at 2 GHz for wireless sensor networks, consuming about 3.5mW. However, more than 80% of the total receiver power is dedicated to the RF gain stages, divided between the LNA at the antenna and the channel-select amplifiers. The journal paper shows the power breakdown and illustrates the critical problem with the architectures: that providing adequate gain at RF usually requires large amounts of power.

One option to enhance gain and improve sensitivity is the use of positive feedback, or regeneration, in the amplifier. This technique was used in the early days of wireless communication to increase the gain available from the vacuum tubes used at the time. A drawback of the technique is that the amount of feedback must be tuned and carefully controlled to enhance the gain without triggering oscillation. The super-regenerative architecture circumvents the need for feedback tuning by allowing the amplifier to oscillate at RF, achieving a large amount of gain from a single stage. The resulting high gain preceding the detector improves sensitivity substantially, to better than -100 dBm [23]. The super-regenerative receiver at its core is an envelope detection architecture using a super-regenerative amplifier as an RF gain stage, achieving high performance. The implementation drawback is that a high accuracy LO is now required, with performance requirements similar to those of the frequency conversion architectures described above.

In summary, simple RFID receivers are not sensitive enough for peer-to-peer links, while traditional frequency conversion architectures are inherently limited by LO power consumption. In order to significantly reduce the power of the wake-up receiver, the power contribution of the LO must be reduced.

2.3 Technology Considerations

The power and performance of any circuit is influenced by the process technology used for implementation. Choosing the proper technology is always one of the main issues before starting to design a new application. RF CMOS and SiGe BiCMOS are the two promising technologies used in RF/mixed-signal applications. The quality factor of the passives integrated on a Si BJT or CMOS processes are poor compared to the integrated SiGe or GaAs ones. SiGe and BiCMOS process, also have a relatively higher cut-off frequency, f_T, and has been preferred over the RFCMOS process for high-performance and low-noise designs most of the time.

However the recent advances in RFCMOS, especially the further shrinking of the FETs, makes conventional CMOS process a rival to previous SiGe generation as far as cut-off frequencies are concerned. Lower power consumption, shorter fabrication time and lower wafer costs further promote the RF CMOS process as the technology of choice for medical implant devices. For sensor network applications, standard digital CMOS integrated circuit (IC) is the only feasible choice for the active circuitry designed. Single-chip integration of digital, analog, and communication circuitry is mandatory to reduce the hardware cost and scaled CMOS is proven to be a good platform for RF circuits as well as digital. For analog and RF design, however, the performance of the active devices

Table 2.1 Performance Comparison of RFIC Technologies

	CMOS	Si BiCMOS	SiGe BiCMOS	GaAs MESFET	InGaAs HBT
Feature size	0.18μm	0.4μm	0.25μm	0.5μm	3μm
f_T(GHz)	40	25	75	40	60
f_{max} (GHz)	45	40	75	40	60
NF_{min}@2GHz	1.2	1.1	0.9	0.5	1
Substrate resistivity (Ohm-cm)	1	8	18	>10000	>10000
Metal layer	6	3	3	----	----
Inductor(Q)	7	8	15	25	25

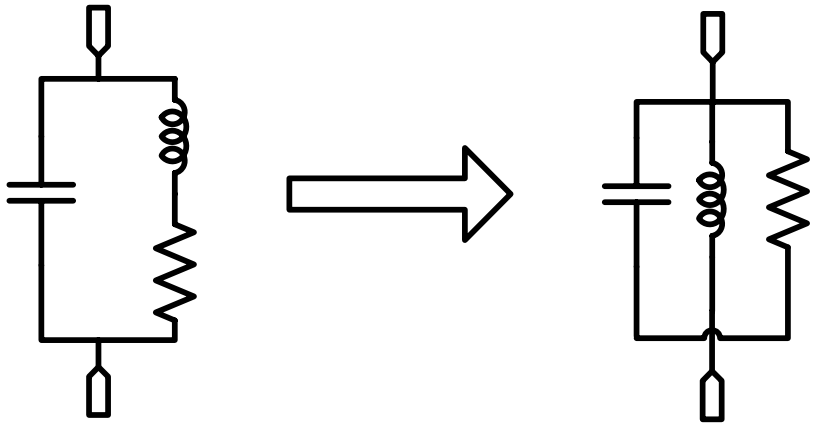
Performance comparison of RFIC technologies [24]

does not give a complete picture. The quality and implementation of passive devices play an integral role in determining the ultimate limits of gain and power consumption.

2.4 Limitations of Integrated Inductors

One of the major limitations of RF integrated circuits is the lack of high Q on chip inductors. Figure 2.3 shows an example of a basic LC tank. For this network the impedance is:

$$Z = \frac{1}{j\omega C + \frac{1}{j\omega L}} \tag{2.2}$$



Realistic model for a parallel LC

Figure 2.3 Real Model for a parallel LC

The equation shows that the impedance goes to zero both at DC, the inductor acts as a short and at high frequency the capacitor acts like a short. At low frequencies the networks impedances' is dominated by the inductor and the capacitor dominates at high frequencies. The resonance frequency incurs when the inductive and capacitive parts cancel and this is given by equation 2.3:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{2.3}$$

However pure parallel LC networks are ideal. The inductors tend to be more "lossy" than capacitors and thus the figure shown below presents a more realistic model of an LC tank.

By replacing the LR series section with a parallel one, equating the parallel and series impedance of the LR section:

$$R_s + j\omega L_s = \left(R_p \parallel j\omega L_p\right) = \frac{\left(\omega_0 L_p\right)^2 R_p + j\omega_0 L_p R_p^2}{R_2^p + \left(\omega_0 L_p\right)^2} \tag{2.4}$$

By equating the real parts given that $Q = R_p/\omega_0 L_p = \omega_0 L_s/R_s$ Solving for R_p:

$$R_p = R_s(Q^2 + 1) \tag{2.5}$$

Equating the imaginary part and solve for L_p :

$$L_p = L_s\left(\frac{Q^2 + 1}{Q^2}\right) \tag{2.6}$$

For equation 2.4 dominant factor for the frequency of resonance is determined by the series resistance of the inductor and its quality factor Q.

Therefore, in order to maximize gain, the load should be optimized for high impedance. For RF circuits, the load itself is typically implemented with a resonant LC network, where the impedance at resonance is given by:

$$R_p = \omega_0 L \mathrm{Q_L} \tag{2.7}$$

where ω_0 is the resonant frequency and it is assumed that the network Q is limited by the inductor Q_L. For on-chip inductors in the low GHz regime, R_p is practically limited to a few ohms by the size and quality of integrated passives. Figure 2.5 shows the calculated R_p at 400MHz using Equation 2.2 for inductor quality factors of 10 and 20. Large inductors (10 nH) with quality factors of 10 on chip are considered outstanding, with Q of 15 or 25 possible for smaller inductors [25]. Achieving impedance greater than 1 kΩ is difficult with integrated inductors especially at UHF frequencies which limits amplifier gain.

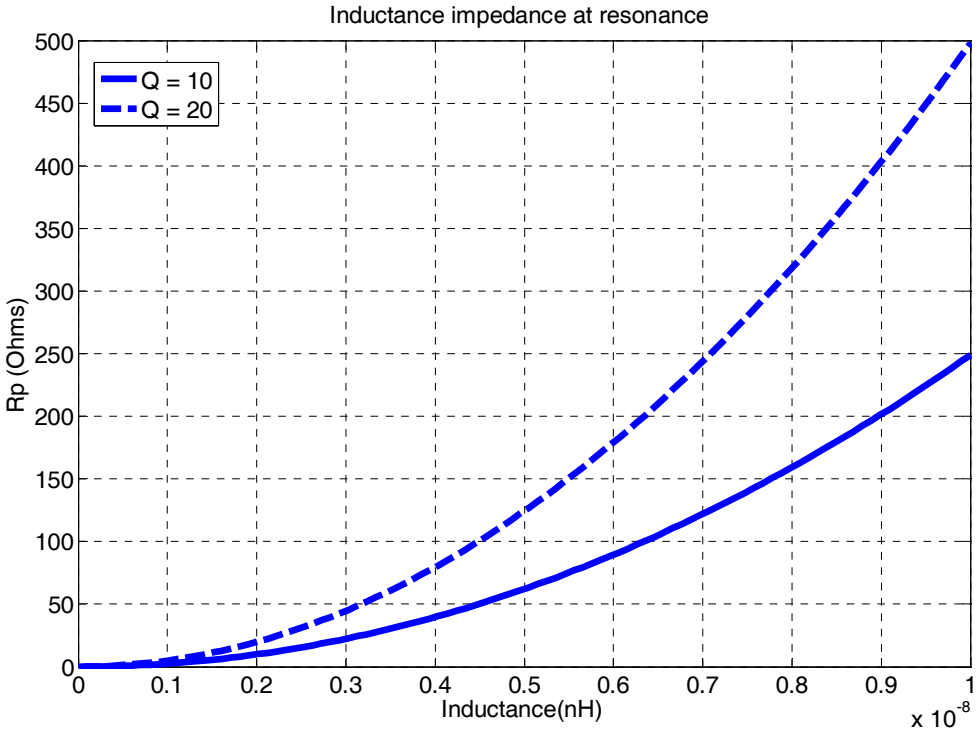


Figure 2.4 Inductor impedance at resonance

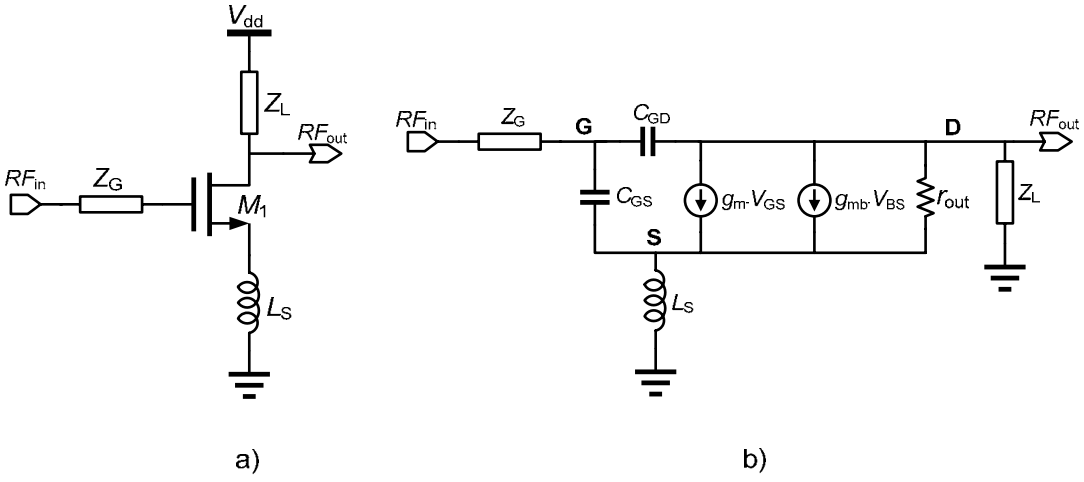


Figure 2.5 Low Noise Amplifier with Source Degeneration

From inspection of the circuit of Figure 2.5 and not considering the effect of L_s we can obtain that the gain of the low noise amplifier at the frequency of interest, the frequency of resonance, is determined by the impedance of the LC tank and the transconductance g_m of the input transistor. The obtained gain is expressed by equation:

$$G_{LNA} \propto g_m R_{Load} \tag{2.8}$$

Where g_m is the transconductance of the transistor M_1 and R_{Load} is the total parallel resistance of the equivalent circuit. The impedance at resonance is given by

$$R_{LOAD} = R_p = R_s \cdot (Q^2 + 1) = \omega_0 L Q_L \tag{2.9}$$

R_{LOAD} is practically limited by the size and quality of integrated passives.

As an example, consider a single stage amplifier with source degeneration using 100 μA of bias current. The maximum transconductance is then about 2 mS, which yields a gain of 2 with 1 kΩ load. Much higher gain will be needed to implement an RF receiver, re-enforcing the role of passives components in low power design. However with the advance of technology, scaling has little impact on the limitations of passive components because CMOS processes are optimized for digital performance and low cost, so the metallization used for the inductors must use relatively thin layers, increasing the loss and lowering Q. One of the few benefits of scaling is the continuing trend to add more interconnect layers, which helps move inductors further from the substrate and reduce loss. The logical extension of this concept is to post-process additional thick metal layers, specifically optimized for high quality inductors, on top of completed CMOS wafers. Because the additional layers do not require precision lithography, minimal cost is added to the fabrication process. An example of an “above-IC" inductor was presented

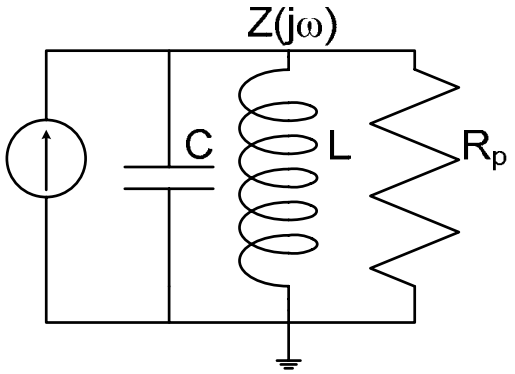


Figure 2.6 Classic LC tank

in[26] , using a 5 μm thick layer of copper above the CMOS. The combination of thick copper interconnects and larger distance between the coil and substrate results in a measured quality factor of 25 for a2.5nH inductor. Although this is almost a factor of two improvements over standard on-chip inductors, the oscillator using this coil still consumed 400 μW of power. This figure is still several times higher than the power consumption target for the entire WuRx, even with the extra processing steps and thick metals. It is therefore unlikely that the R_p available from LC networks will be improved significantly in future IC technologies.

As an alternative to resonant networks, the load impedance can also be implemented as a wideband resistive load (Figure 2.4). In this case the bandwidth is determined by the load capacitance, which is usually the input device capacitance C_d of the subsequent stage. In contrast to resonant networks, scaled CMOS technologies excel at reducing device size and capacitance. The result is that, for fixed frequencies, the impedance magnitude attainable from a wideband network is increasing rapidly with technology scaling, far surpassing resonant networks in 90 nm CMOS. Figure 2.6

illustrates this trend, comparing the impedance magnitude of an LC tank with that of transistor input capacitance at 2 GHz. For the LC tank, a very high quality inductor (L=20 nH, Q=15) is assumed to represent a best-case scenario, and as mentioned above, the impedance stays roughly constant as technology scales. In the wideband case, devices in each technology are sized and biased around moderate inversion to provide a transconductance equal to 1 mS, intended to mimic the loading due to a subsequent circuit stage. The impedance magnitude due to device capacitance in modern technologies has exceeded that of high quality resonant tank. To maximize gain, then, wideband amplifiers and active loads are a promising choice in modern CMOS technology.

2.5 Micromechanical Resonators

The field of wireless communication has dictated the need for new micromechanical RF components capable of multi-frequency low loss filtering and frequency synthesis on the same silicon chip. Because of these advancements as an alternative to on-chip passives and traditional off-chip passive components mounted on the printed circuit board (PCB), radio-frequency micro-electromechanical systems (RF-MEMS) are emerging as a viable option to break the trade-off between integration and quality of passive components. RF-MEMS take advantage of thin-film IC processing techniques to implement high quality resonant structures on the micro scale. Researchers have demonstrated structures with Q factors higher than 10,000 and resonant frequencies up to the low GHz, fabricated using a variety of materials from bulk silicon to diamond and others [27, 28].

Fortunately, the reliability and stability of these research structures are ideal for use in circuit prototypes. For that purpose, this research focuses on a type of MEMS resonator that is already ubiquitous in communication and other electronic applications. However, having a MEMS device that can simultaneously deliver monolithic, post CMOS integration for IF and RF components that can readily interface with 50 Ohm systems is challenging. Thin film piezoelectric aluminum nitride (AlN) based processing technology for RF applications is an emerging technology for realizing mulit-frequency per silicon chip, CMOS-compatible, low-loss filter, reaching to GHz frequencies. The ability to scale the lateral dimension for the structural material, allows for more mechanically robust devices that are capable of attaining lower fundamental resonant (406 MHz) frequencies with reduced motional resistance (260Ω) while maintaining a high Q (1,420). The circuit design techniques developed here to incorporate MEMS resonators will also be applicable to future MEMS devices.

2.6 SAW Structure

One common off-chip high quality resonator is the surface acoustic wave (SAW) resonator. It has long provided high performance RF filters with small form factors while showing a continuously declining cost structure. The SAW chip is a piezoelectric single crystal (e.g. quartz, lithium tantalate, lithium niobate), polished on the surface and coated with one or more comb-like, interlocking electrode fingers, so-called interdigital transducers. These usually consist of aluminum and are deposited by photolithographic means. When an electric signal is applied to an electrical transducer, an electrical field is produced between the polarized transducer fingers and, because of the (reverse)

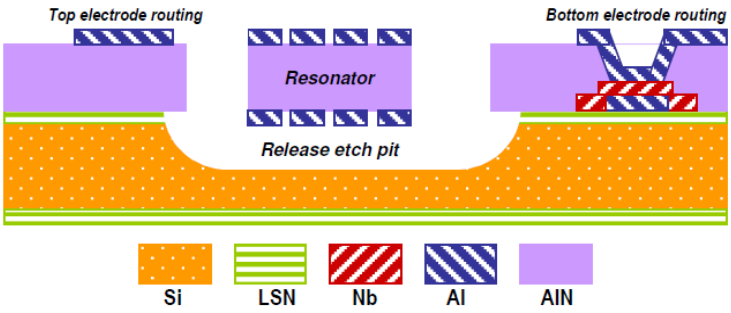


Figure 2.7 Cross-section and top view of SAW resonator (not to scale)

piezoelectric effect, the chip surface is deformed mechanically. Like tiny seismic waves, a surface acoustic wave spreads out from both sides of the transducer. The reflectors on both sides of the transducer reflect these acoustic waves and thus create a standing wave, which is converted back into an electrical signal at an output transducer (piezoelectric effect). An input piezoelectric transducer uses electrical signals to generate a longitudinal acoustic wave traveling on the surface of the piezoelectric substrate. The basic SAW structure is a thin layer of piezoelectric aluminum nitride (AlN) sandwiched between two metal electrodes and fabricated on a silicon substrate. The whole structure must also be acoustically isolated from the substrate to allow free movement.

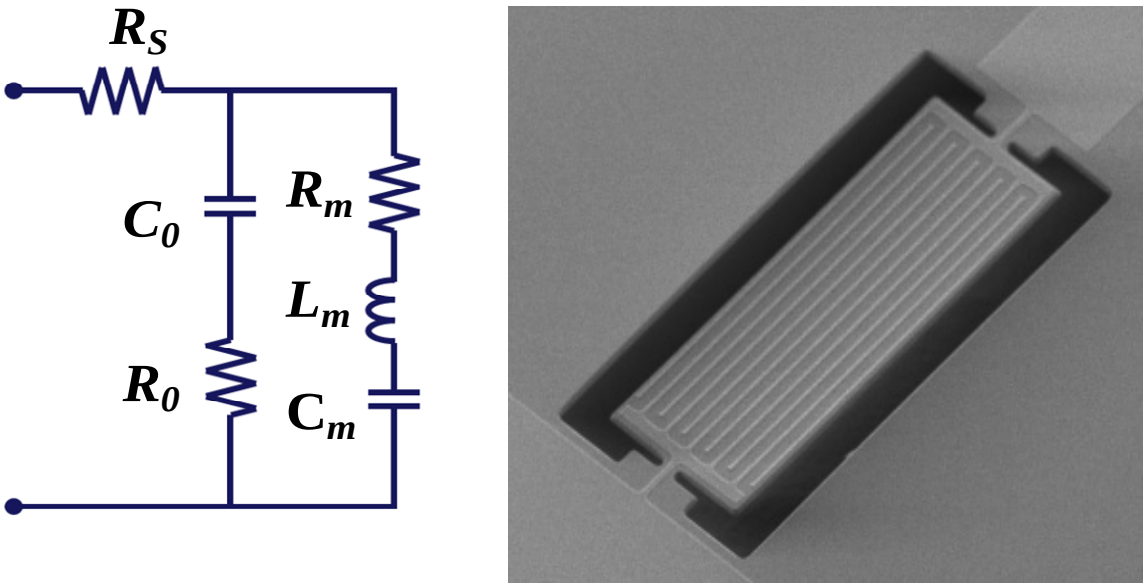
There are several variations of SAW resonators, depending mainly on the acoustic isolation method. For this research, we utilize a piezoelectric contour mode MEMS plate resonators which uses an etch pit under the resonator. Figure 2.7 shows the structure of an AlN MEMS resonator, where the resonator is fabricated on a silicon wafer using standard IC processing techniques. The bulk silicon under the resonator is etched away, allowing the structure to vibrate. Because of the novelty of this SAW resonators, its resonant frequency depends on the lateral spacing of the transducer electrodes, the

resonance design effectively uncouples the resonant frequency of the device from their overall dimensions by selectively patterning the transduction electrodes and routing the excitation wave form. Quality factors on the order of several hundred to a few thousand are typical, with resonance frequencies in the low GHz range. The standard IC batch fabrication method also results in low manufacturing cost. The combination of small size and low cost of AlN MEMS technology makes it a good fit for wireless micro-systems where, this technology permits a monolithic integration of post-CMOS compatible, with low-loss filters spanning IF to RF that can readily be interfaced with existing 50Ω RF systems [29]. Tolerances can be improved with better manufacturing methods or addressed through laser trimming.

2.7 SAW Circuit Model

A simplified circuit model for the SAW resonator is shown Figure 2.8 along with a photo showing a top view of the structure. Table 2.2 gives some typical values for the model parameters. SAW resonators are currently produced for various frequencies and various wireless applications especially as IF filters, RF resonator filters and sensors for wireless passive sensing. SAW devices are used for delay line, reflective delay line, and one-port/two-port resonator[30]. These parameters in Table 2.2 are for a SAW resonator at 404 MHz, used as a one port resonator filter for a 50Ω termination. As shown in Figure 2.9(a), a SAW structure is characterized by two different resonances one in series and one in parallel. As frequency increases, the series resonance occurs first at a frequency f_s, determined by the motional inductance L_m and motional capacitance C_m. As expected for a series resonant circuit, the impedance reaches a minimum equal to R_m at f_s.

Due to the motional resistance being a low value set to R_m it is an advantage of the SAW resonators compared to other types of MEMS devices like bulk silicon resonators. Although the polysilicon resonator published in [28] possesses a high Q (approximately ~14,000), but the motional impedance is 282 kΩ. With this high impedance it makes it very difficult to couple the energy into the structure as well as have the resonator interface with circuit.



(a) Simplified Circuit

(b) Photo of SAW resonator

Figure 2.8 Circuit Model and photo of SAW resonator

Table 2.2 SAW Resonator Parameter Values for 405.5 MHz

Model Parameter	Value
L_m	127μH
C_m	1.21fF
R_m	579Ω
C_0	0.19pF
R_0	224Ω

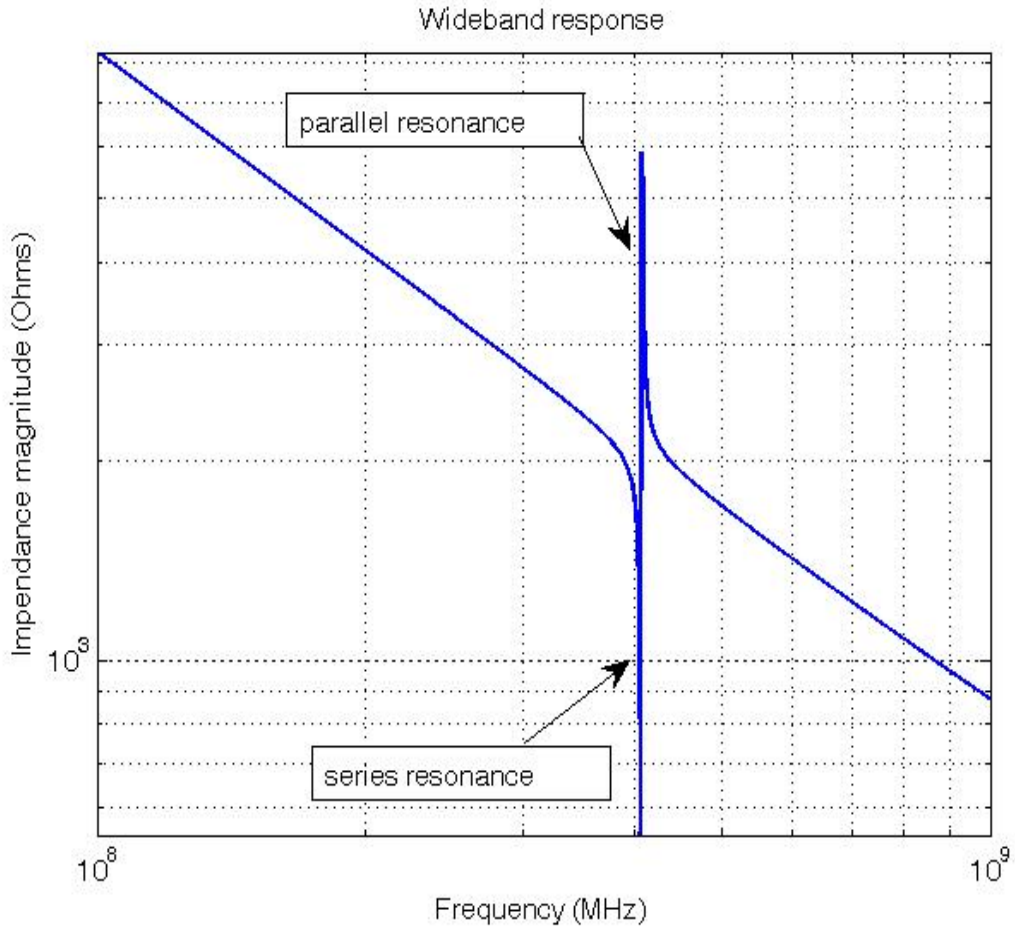


Figure 2.9 Simulated SAW resonator response (Wideband response)

series resonance, the impedance of the structure increases and then peaks at the parallel resonance fp. The resonator appears inductive between the series and parallel resonance frequencies. Outside this range, the response is dominated by the physical parallel plate capacitor Co. By varying the shunt capacitance in parallel with Co both the parallel frequency fp changes as well as the impedance at the parallel resonance (Rp), however it leaves the series resonance unchanged. Figure 2.9(b) illustrates this effect by shunting the resonator with an additional capacitance Cp in parallel with Co. The ratio of Rp to Rx falls as loading from Cp increases, although the quality factor of the resonance remains

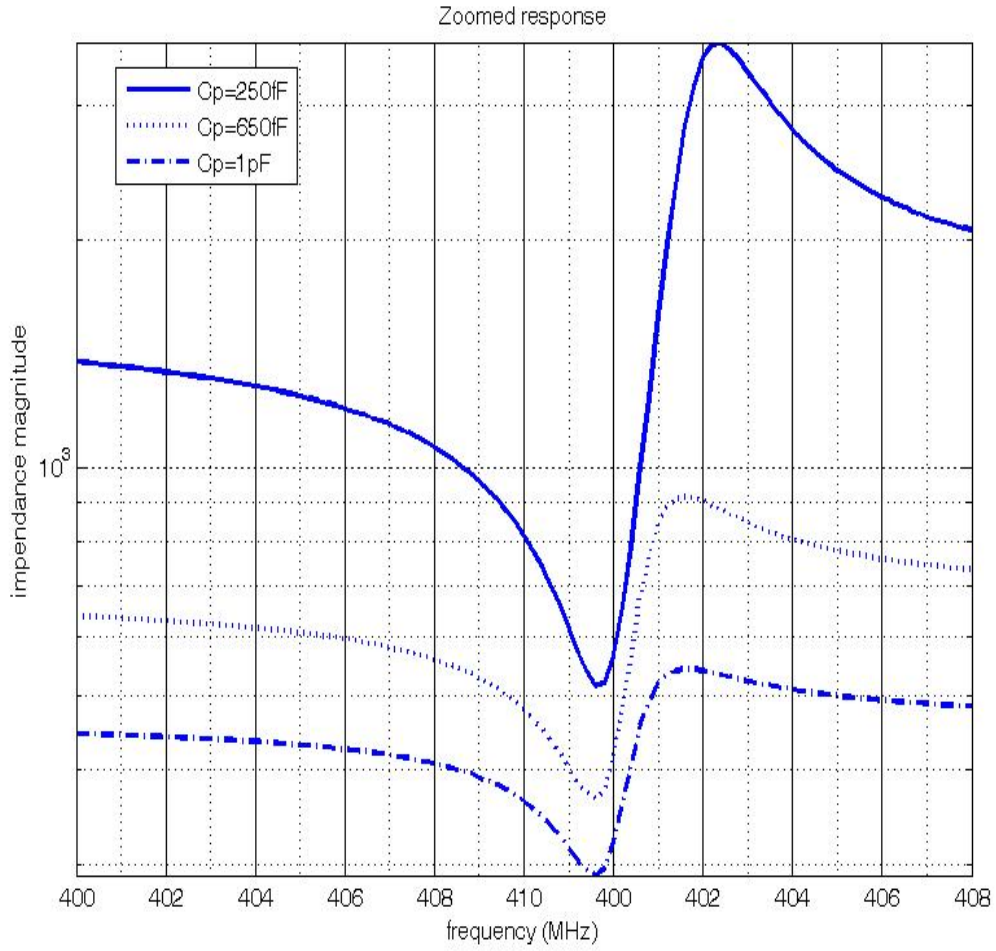


Figure 2.10 Simulated SAW resonator (Zoomed response for varying Cp)

the same if Cp is lossless. If the resonator is used in the parallel resonant mode where high Rp is desirable, it is critical to minimize the loading from Cp, which can come from external circuitry or wiring parasitics. Although SAW resonators possess high Q factor, they are nevertheless subject to similar limits in Rp and therefore power consumption. The resonator impedance plotted in Figure 2.10 reaches a maximum between 600 and 6kΩ with a realistic load capacitance. However, the Q factor and frequency stability of these resonators is still much better than what is achievable with integrated passives.

2.8 Circuit and SAW Integration

An important factor when incorporating a MEMS component is the level of integration and increased cost. SAW resonators are a favorable choice because they are fabricated on silicon substrates without the use of exotic materials. There have been several research groups that have been successful in post-processing resonators on top of finished CMOS wafers [26, 31-34]. With this extra fabrication processing step an increase in the cost will occur but the final result is a highly integrated solution. Another approach for CMOS post-processing that may reduce this cost, if the size of the resonators is manageable, they could be good for flip-chip packaging instead. This "system-in-package" technique can yield very compact implementations with high volume consuming a few cubic millimeters. Packaging for MEMS devices presents its own set of challenges and makes product integration into real world devices difficult. However, with the recent advancement in MEMS packaging the use of SAW resonators is well within reach for medical devices targeting low cost and small size[35, 36]. The use of SAW resonators for low power RF circuits has been popularized recently, using the resonator both in high quality oscillators and as a filtering element.

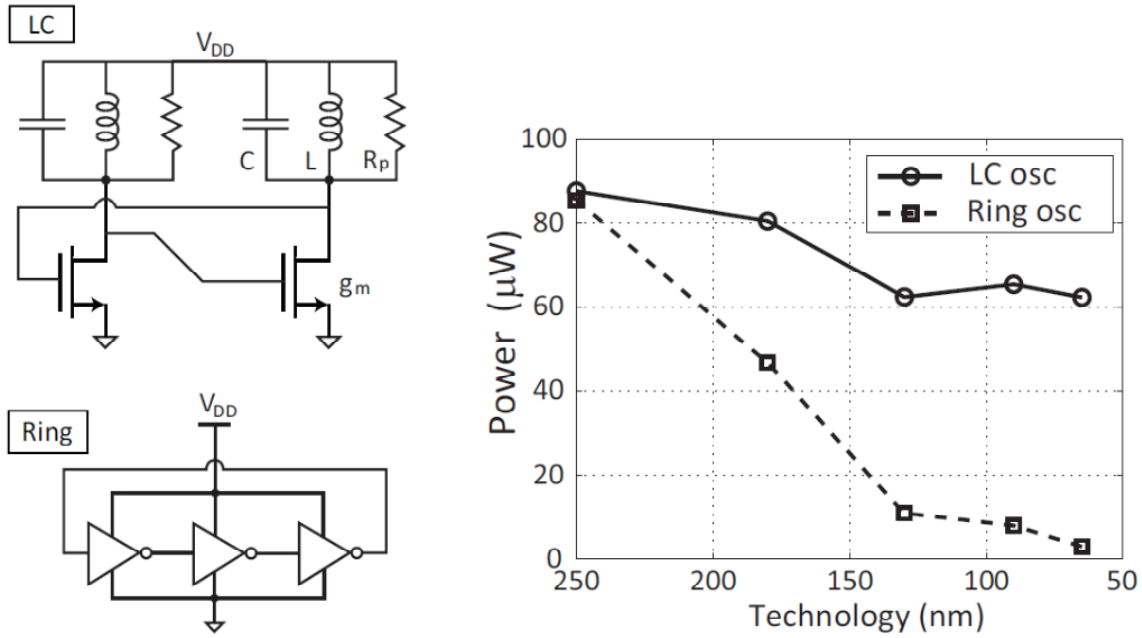
This chapter has summarized the architecture options and challenges for the design of an ultra-low power receiver. At the circuit level, the limited current consumption means that amplifiers utilizing on-chip passives will start from low gain. Incorporation of RF-MEMS technology, in particular the SAW resonator, was identified as a possible means to achieve the required receiver functionality without excessively

increasing cost or size. With this background the next chapter describes the components and implementation for the complete wake-up receiver.

CHAPTER 3
UNCERTAIN-IF RECEIVER

3.1 Design of the Ultra Low-Power Wake-Up Receiver

From the previous chapter the most challenging specification to meet in designing WuRx is the extremely low power consumption. This chapter focuses on the development of the first WuRx using a simple receiver architecture to meet the power specifications. As describe previously, the earliest receivers were very simple, consisting of just an antenna and non-linear circuit element used for demodluation. One of the most common receivers is the crystal set, this uses an antenna, tuning circuit and nonlinear envelope detector [37]. The envelope detector simply detects the amplitude of the RF carrier. The only type of amplitude modulated signals that can be used is on-off keying (OOK). OOK modulation is very popular because it has the advantage of allowing the transmitter to be idle during the transmission of a "zero" to conserve power however, a disadvantage is that OOK is more susceptible to noise and interferers. For OOK the scheme is a "one" for encoding by transmitting the RF carrier while a "zero" is simply the absence of the carrier. Though its link efficiency is inferior to other modulations such as frequency and phase modulations,(FSK,PSK) it has the advantage of simplicity of circuit implementation and low power consumption. Using the work by [16] as the main motivation by moving the application from the WSN communication band to the MICS



(a) LC oscillator and ring oscillator schematics

(b) Simulated power consumption

Figure 3.1 Effect of technology scaling on oscillator power[16]

band we developed a low power wake-up receiver. The prototype implemented in this work uses a novel architecture to achieve significant power reduction.

3.1.1 Oscillator Power Limitations

An oscillator is required to achieve an active gain sufficient enough to sustain stable oscillation. According to [16] it is showed that as technology scales the input impedance of small devices surpasses the impedance generated from integrated *LC* tanks. In order to achieve low power oscillation, implementing a simple ring oscillator consisting of wideband inverting stages would present a better alternative for oscillation than its *LC* counterpart. Power, VDD, is reduced as technology scales to maintain a constant frequency. This expectation was verified in [16], by showing the power consumption of a 3-stage CMOS ring oscillator compared with a simple LC oscillator as

technology scales Fig. 3.1. The ring oscillator power is reduced with the technology in order to maintain the constant frequency. For the LC oscillator, the power consumption required for startup diminishes slightly due to the reduced device threshold voltage in scaled technologies, enabling lower supply voltages with the same bias current. However, since the power of a CMOS ring oscillator scales with the total switched capacitance and the square of the supply voltage, its power consumption drops much more rapidly. For current technologies, a ring oscillator yields a factor of 20 power savings over an LC oscillator. This finding is consistent with the analysis presented in [38], where the power efficiency of a resistively-loaded RF amplifier at 900 MHz was shown to be superior to a tuned amplifier in 0.18 CMOS.

3.1.2 Uncertain IF Architecture

The ring oscillator addresses only the minimum power required to achieve oscillation at RF frequencies, without considering phase noise or frequency accuracy. Of course, these are important considerations for frequency conversion architectures, and the ring oscillator is known to have inferior frequency stability compared with an LC oscillator [39]. However, the receiver presented here overcomes these problems at the architecture level, by employing an "uncertain-IF" to ease the phase noise and frequency accuracy requirements. The relaxed specifications allow the use of a free-running ring oscillator for LO generation.

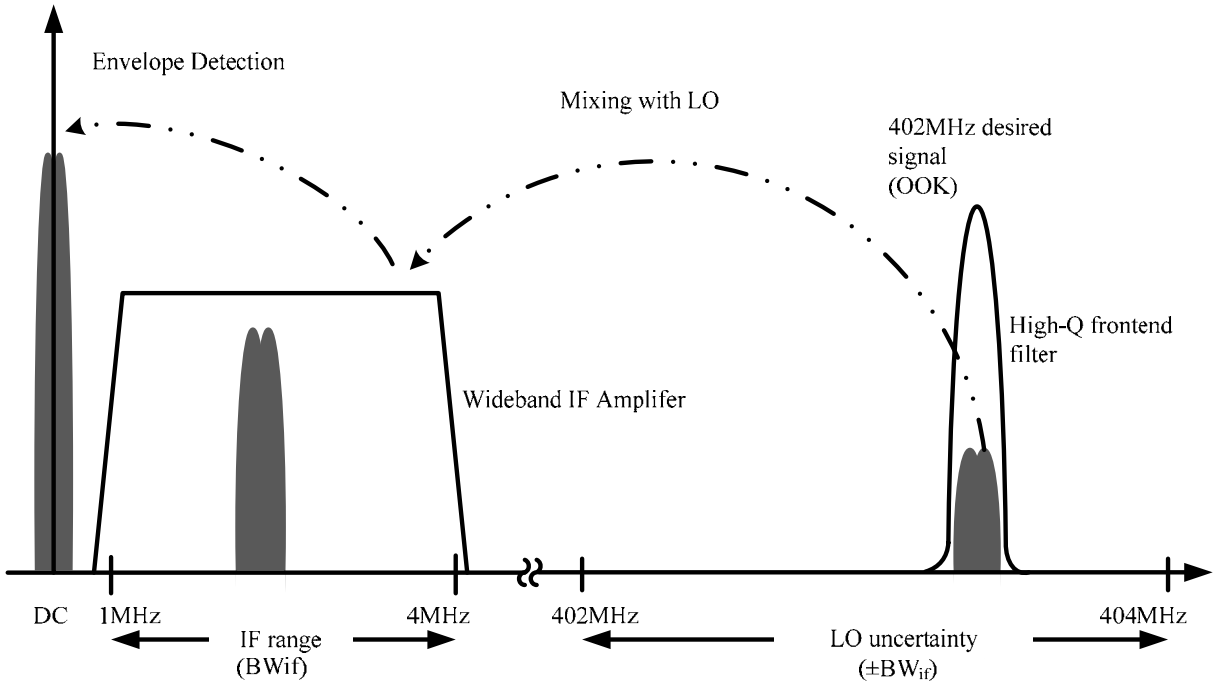


Figure 3.2 Uncertain-IF frequency plan and method of operation

The frequency plan and method of operation for the uncertain-IF architecture is shown in Figure 3.2. The desired signal is first filtered at the front-end to remove image and interferers. It is then mixed with an LO whose frequency is not well-defined. In fact, the LO must only be guaranteed to lie within some pre-determined frequency band BW_{if} (4 MHz in this implementation) around the RF channel frequency. Due to the uncertainty of the LO frequency, the exact IF frequency will vary, but the downconverted signal will lie somewhere around DC within BW_{if}. The signal is then amplified at this IF frequency, which is much more power efficient than achieving the equivalent gain at RF. Finally, envelope detection performs the final downconversion to DC. Note that the use of envelope detection again limits the receiver to the detection of amplitude-modulated

signals, most commonly OOK, because the envelope detector removes all phase and frequency content in the IF signal. As shown in Figure 3.2, AC coupling is used to limit the low end of the IF bandwidth to a frequency above the baseband bandwidth. For now, it is sufficient to mention that this bandwidth limiting is used to ensure proper operation of the envelope detector and avoid the situation where the RF signal is directly converted to DC. However, the gain roll off near DC means that the receiver cannot detect signals at the RF channel frequency if the LO frequency happens to fall on that channel frequency. The implications of this failure mode are discussed in more detail in Section 3.2.3.

The uncertain-IF architecture may be viewed as super-heterodyne, where the second downconversion is simply self-mixing, obviating the need for a precise LO at the IF frequency. For an ultra-low power receiver like the WuRx, the uncertain-IF architecture holds several advantages over the architectures described in Chapter 2. First, LO phase noise and frequency accuracy requirements are significantly relaxed. Frequency variation of the LO simply appears as IF frequency variation, to which the envelope detector is insensitive. An initial calibration step is only required to account for process variation and tune the LO within the desired range. As discussed earlier, it may also be necessary to adjust the LO to ensure that it does not coincide with the RF channel. Thereafter, re-calibration is required only to counteract frequency drift due to aging or temperature and supply variation. Furthermore, as in the heterodyne architecture, signal amplification can be performed at IF instead of RF, resulting in substantial power savings. The result is essentially performance similar to a TRF receiver with dramatically

increased gain before envelope detection, improving performance compared to receivers using only RF gain.

Like any TRF receiver, however, a disadvantage of the uncertain-IF architecture is its susceptibility to interferers. Any undesired signal within $\pm BW_{if}$ of the LO frequency that passes through the front-end filter will be mixed down and detected by the envelope detector. Therefore, a narrow and accurate RF bandpass filter is required to improve robustness to interferers. In effect, the burden of selectivity has been shifted from the LO to the front-end filter. Here in the prototype, filtering is performed by a surface acoustic wave (SAW) resonator at RF.

One important architecture-level design consideration is the tradeoff between LO tuning accuracy and IF bandwidth. If the LO can be tuned very close to the channel frequency, the required bandwidth of the IF amplifier can be narrowed and its power reduced proportionately. On the other hand, the LO must now be kept within a smaller frequency range, increasing vulnerability to oscillator frequency drift. If the IF bandwidth is made large enough, the receiver will be relatively immune to frequency drift and the LO will be able to run for long periods without calibration. For this implementation, a relatively wide IF bandwidth of 4 MHz is chosen to maximize tolerance of LO frequency drift, without requiring excessive power in the IF amplifier.

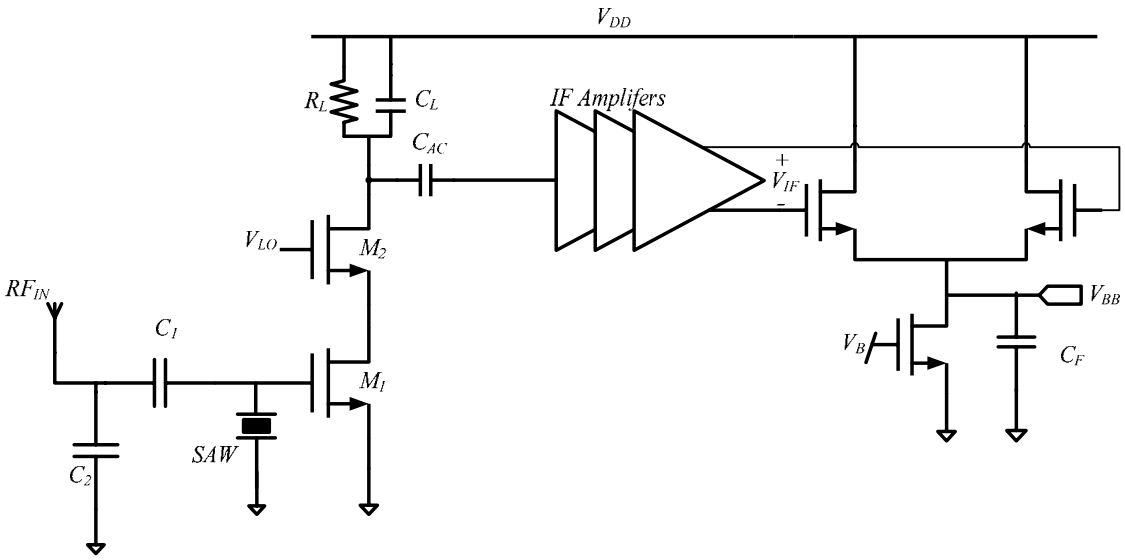


Figure 3.3 Simplified schematic of complete receiver

3.2 Circuit Design

A block diagram of the complete receiver is shown in Figure 3.3. The predetermined OOK input signal sequence is first filtered by the matching network containing the SAW resonator, followed directly by the mixer. The following stage is for the IF signal which is then amplified with a gain block covering the entire IF bandwidth range and lastly converted to DC by the envelope detector. On the LO side, a free-running digitally-controlled oscillator (DCO) drives the mixer. A 5 bit digital frequency controller is used to calibrate the LO and bring it within the desired frequency range only when necessary as oppose to maintaining it with an analog control voltage during normal operation. This section will describe the design of each component in detail. In implementing each receiver block, the primary goal is to reduce power consumption

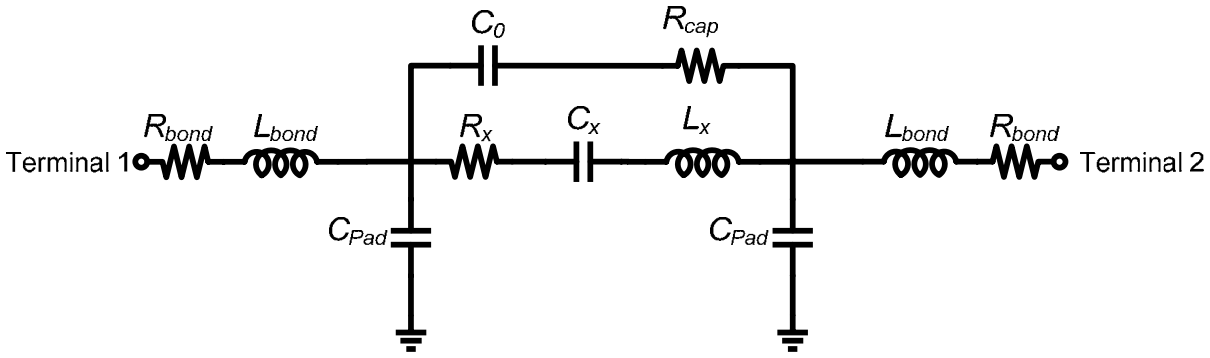


Figure 3.4 Complete resonator model including parasitics

while maintaining circuit performance. To further reduce power consumption, the entire receiver is optimized to operate from a single 1V supply.

3.2.1 Input Matching Network

The matching network serves a dual role, first it must supply a stable impedance mach to the 50 Ω input source. Secondly the network should provide a narrow RF filtering to remove out-of-band noise and interfering signals. A benefit of a high quality factor SAW resonator is an attractive choice for selective filtering. Shown in Section 2.6 the SAW circuit model contains a series resonant branch and large shunt capacitance C_O that dominates the response outside the narrow resonant frequency range. In-between the series and parallel resonance frequencies, the SAW resonator acts as a high quality inductive element. When placed in a series mode as a short, C_O will still allow signal feed-through away from resonance. Due to this affect, only a single resonator is placed in its parallel resonant mode to build a filter.

For simulation and actual design of the matching network, a more complex resonator model that includes the parasitic effects is shown in figure 3.4. With

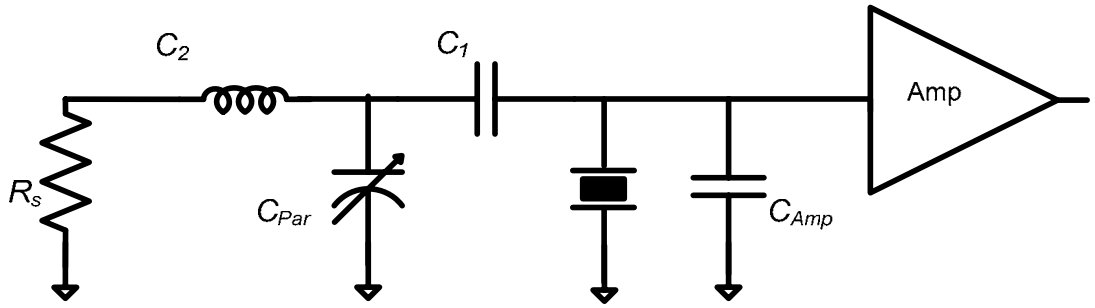


Figure 3.5 Schematic of SAW resonator input matching network

For prototyping purposes, the SAW chip is placed adjacent to the CMOS chip and wirebonded directly to contact pads on the CMOS die. Using the parallel configuration the estimated pad capacitance C_{Pad} is about 100fF and the short bonds (L_{bond}) can be modeled with about 500 pH of inductance. With these affects the quality factor of these bonds is still high due to the short length and low loss so for design a Q of 30 is assumed. Compared with other common matching networks, a capacitive transformer is fortuitous because it contains no inductors, which are typical large and lossy when integrated on the CMOS die. However the resonator provides an inductance to resonate with the capacitive network which includes the capacitive parasitics of the resonator (C_0 and C_{pad} in Figure 3.5. Off chip capacitors C1 and C2 transform the low antenna impedance up to match the resonator impedance. The input capacitance of the LNA is absorbed with the resonator capacitance; with this a real impedance at the amplifier input is not required. The resonator's C_0 is about .20pF so the C_{amp} has to be comparably smaller in order to have little influence on the network response. As describe earlier the equivalent inductance and the parallel impedance of the resonator changed with shunt capacitance.

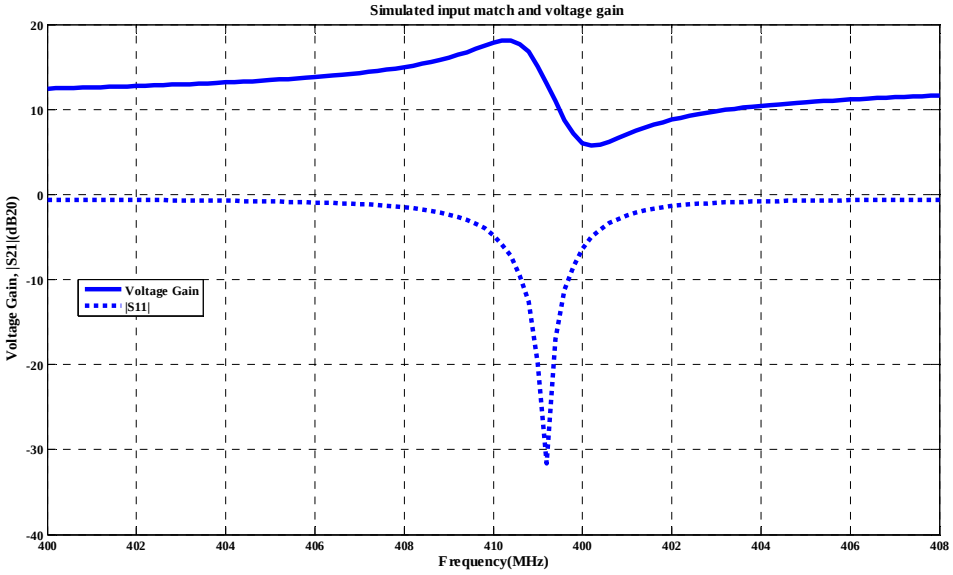


Figure 3.6 Simulated input match and voltage gain

From [40] the impedance of the resonator at its parallel resonance is:

$$R_p = \frac{1}{\omega_0^2 \, C_T^2 \left(R_x + \, R_{cap}\right)} \tag{3.1}$$

where C_T is the total capacitance in shunt with the resonator, R_x is the resonator motional impedance, and R_{cap} represents the loss from the matching network including R_s.

To optimize the input matching using the typical values for the SAW resonator model, the simulated $|S_{11}|$ is shown in Figure 3.6, including bondwires and pad parasitic. The matching network voltage gain is also shown in Figure 3.6. The amplifier input transistor is sensitive to voltage, so an additional benefit of the impedance transformation is approximately 13dB of passive voltage gain. The tradeoff for matching the resonator impedance is that it now has a real resistance, which degrades the noise figure by 3dB compared to other topologies a like single ended LNA with inductive degeneration;

however the goal for this particular implementation is maximum gain, which takes precedent over noise consideration for this amplifier.

3.2.2 Dual Gate Mixer

The Front-end Amplifier design is the most critical block within the whole receiver. Gain and power consumption of this element is the major factor and these aspects will determine the overall performance of the receiver. The effort of this work is to generate the maximum possible gain while maintaining a low power budget.

The mixer is design with two goals in mind to maximize the conversion gain and to minimize the LO drive requirements. A single-ended dual-gate topology Figure 3.7 is chosen because the LO port is being driven from a single ended ring oscillator. A single ended ring oscillator is used as opposed to a differential ring oscillator because it would require at least twice the power of the single-ended implementation. The feedthrough for the RF and LO that is inherent to the single-balanced design is filtered by the load network and the IF amplifier stages before arriving at the envelope detector. The input RF signal is coupled onto the gate of M_1 through the coupling capacitor contained within the matching network, while DC bias is applied to the gate by an on-chip 50 kΩ resistor. Devices M_1 and M_2 are sized with W/L of (30/0.18) μm/μm, with M_2 presenting only about 20 fF of capacitive load to the LO. Although the cascode device M_2 generally modulates the transconductance of M_1, the ring stage CMOS buffers drive the LO port

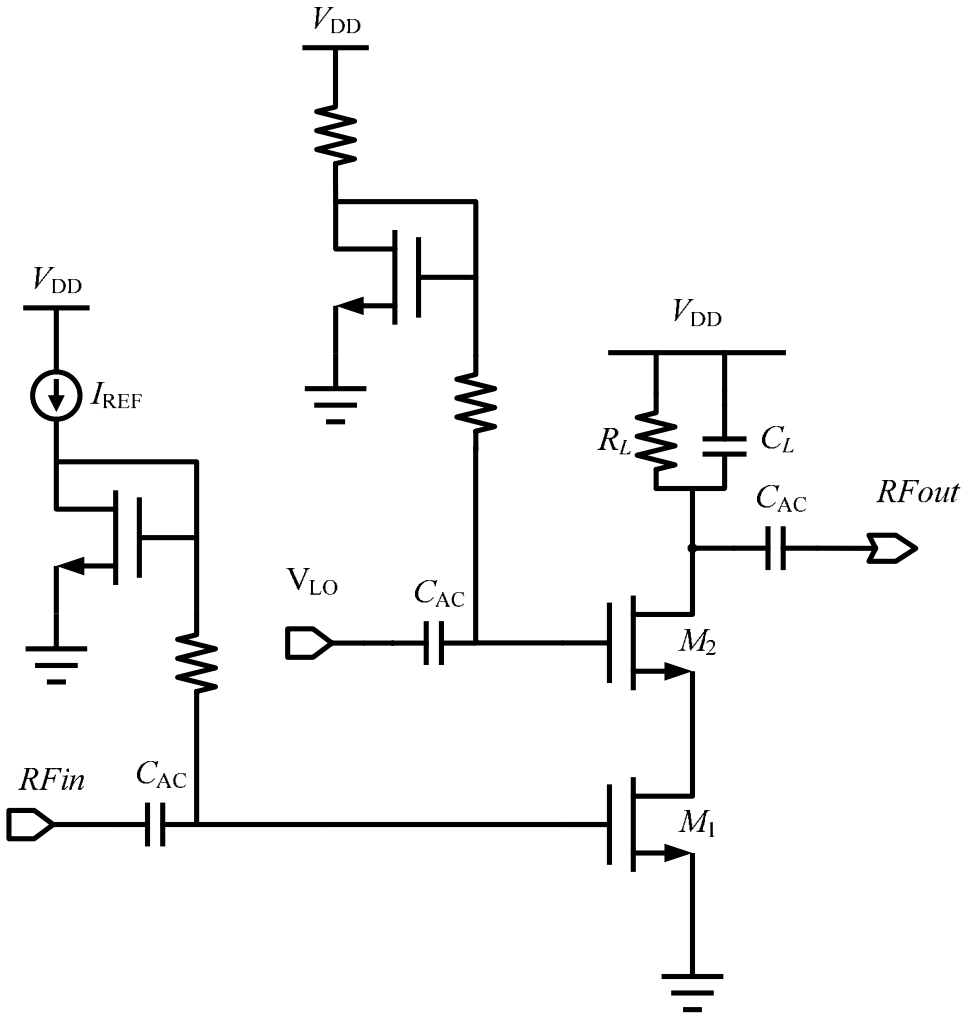


Figure 3.7 Schematic for Dual gate Mixer

Table 3.1 Transistor sizes and element values for Dual Gate Mixer

Transistors	W(μm)	L(μm)	Resistors	Values
M_1	30	2	R_1	50 kΩ
M_2	30	2	R_2	100 kΩ
M_3	9.45	4.5	R_3	148 kΩ
M_4	4	0.18	R_L	33.3 kΩ

Capacitors	Value
$C_{AC}(RF_{in})$	3.2 pF
C_L	512 fF
$C_{AC}(RF_{out})$	20 pF
$C_{AC}(V_{LO})$	3.2 pF

with a rail-to-rail signal, effectively switching the RF transconductor M_1 on and off Figure 3.7. Therefore, the output current signal i_o at the IF frequency can be calculated by approximating the time-varying transconductance $g_m(t)$ as switching between g_{m0} and zero 0 i_0 is expressed as:

$$i_0 = g_m(t)v_i = g_{m0}p(t)v_i \tag{3.2}$$

where *p(t)* is a pulse train with 50% duty-cycle (square wave). Using the Fourier series representation of *p(t)*:

$$p(t) = \frac{1}{2} + \frac{2}{\pi}\cos(\omega_{LO}t) - \frac{2}{3\pi}\cos(3\omega_{LO}t) + \cdots \tag{3.3}$$

the output current is:

$$i_0 = g_{m0}v_i\left(\frac{1}{2} + \frac{2}{\pi}\cos(\omega_{LO}t) - \frac{2}{3\pi}\cos(3\omega_{LO}t) + \cdots\right) \tag{3.4}$$

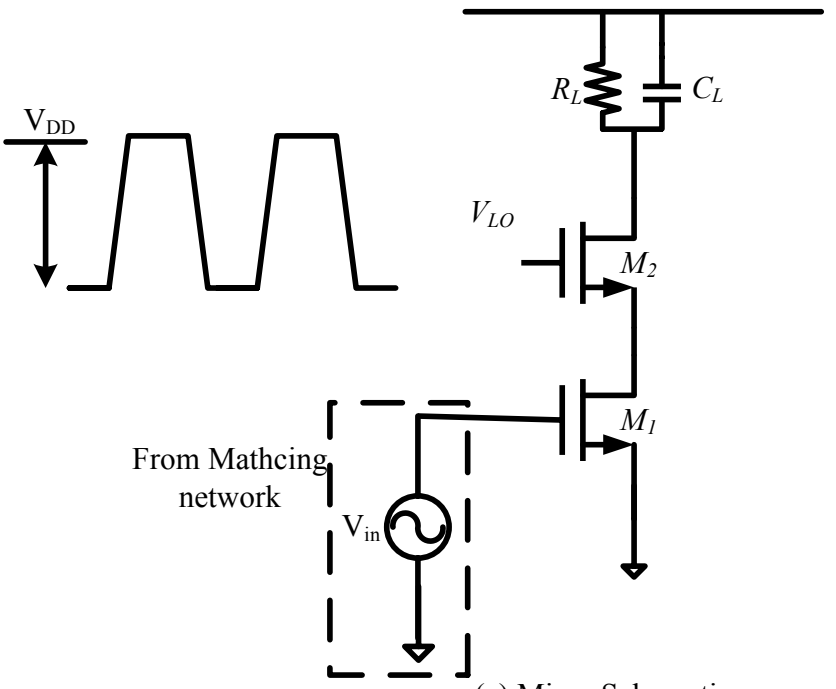
The RF input signal is $v_i = v_s\cos(\omega_s t)$, leading to the final conversion transconductance g_{conv}:

$$\frac{i_0}{v_i} = \frac{g_{m0}}{2}\cos(w_s t)m + \frac{g_{m0}}{2}\left(\frac{2}{\pi}\cos(\omega_{LO} \pm \omega_s)t\right)\ldots \rightarrow g_{conv} = \frac{1}{\pi}g_{m0} \tag{3.5}$$

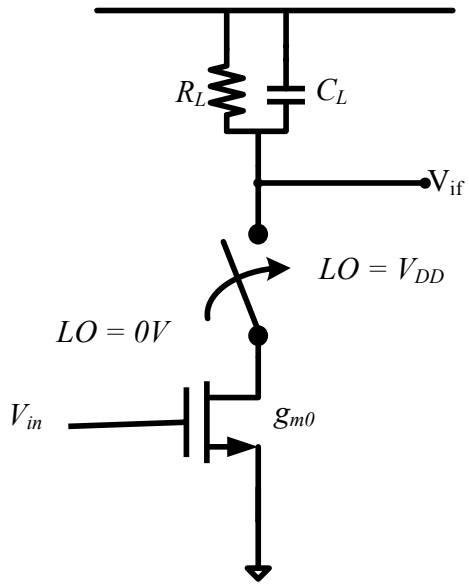
The overall voltage conversion gain G_{conv} can be calculated from RF to IF, g_{conv} is multiplied by the output resistance of the mixer at the IF frequency:

$$G_{conv} = \frac{1}{\pi}g_{m0}\left(R_L||R_{0,mix}\right) \tag{3.6}$$

where R_L is the load resistance and $R_{o,mix}$ is the output resistance looking into the drain of M_2 when the LO voltage is at V_{DD}. To maximize the conversion gain within the available voltage headroom, the mixer load resistor R_L is made as large as possible. The final resistor design value is 33 kΩ, implemented with a p+ polysilicon resistor. The quiescent



(a) Mixer Schematic



(b) Model of operation

Figure 3.8 Dual Gate Mixer Operation

transconductance g_{m0} is controlled by the DC bias voltage on the gate of M_1, which is set at 475 mV. Under these bias conditions and with the LO running, the simulated average current in the mixer is 30 µA. Including the voltage gain in the matching network and using Equation 4.5, the calculated G_{conv} is 15.6 dB, which closely matches the value of 14.4 dB obtained with SpectreRF periodic steady state response (pss) simulations. Figure 3.9 shows the layout for the dual-gate mixer.

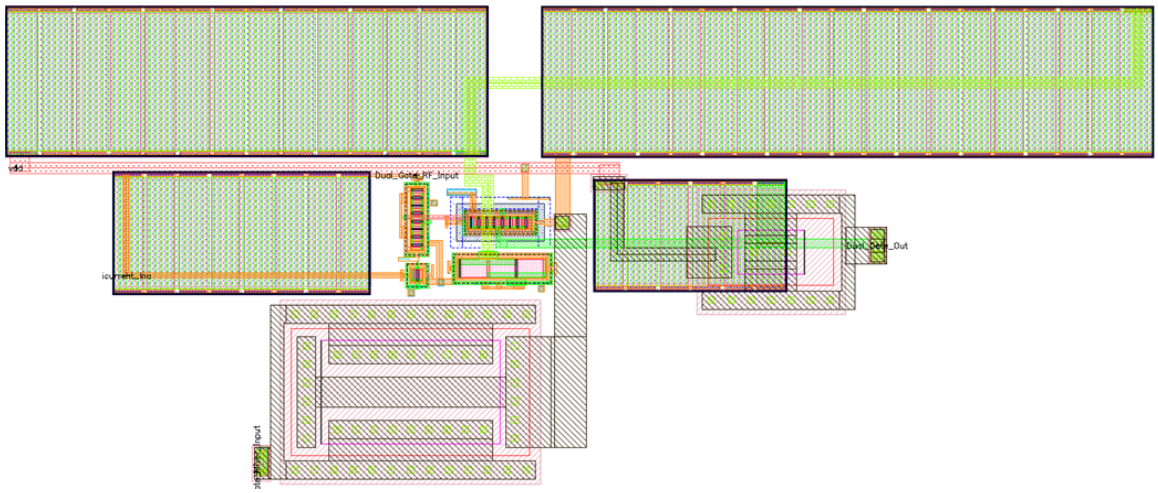


Figure 3.9 Layout Design for Dual-Gate Mixer

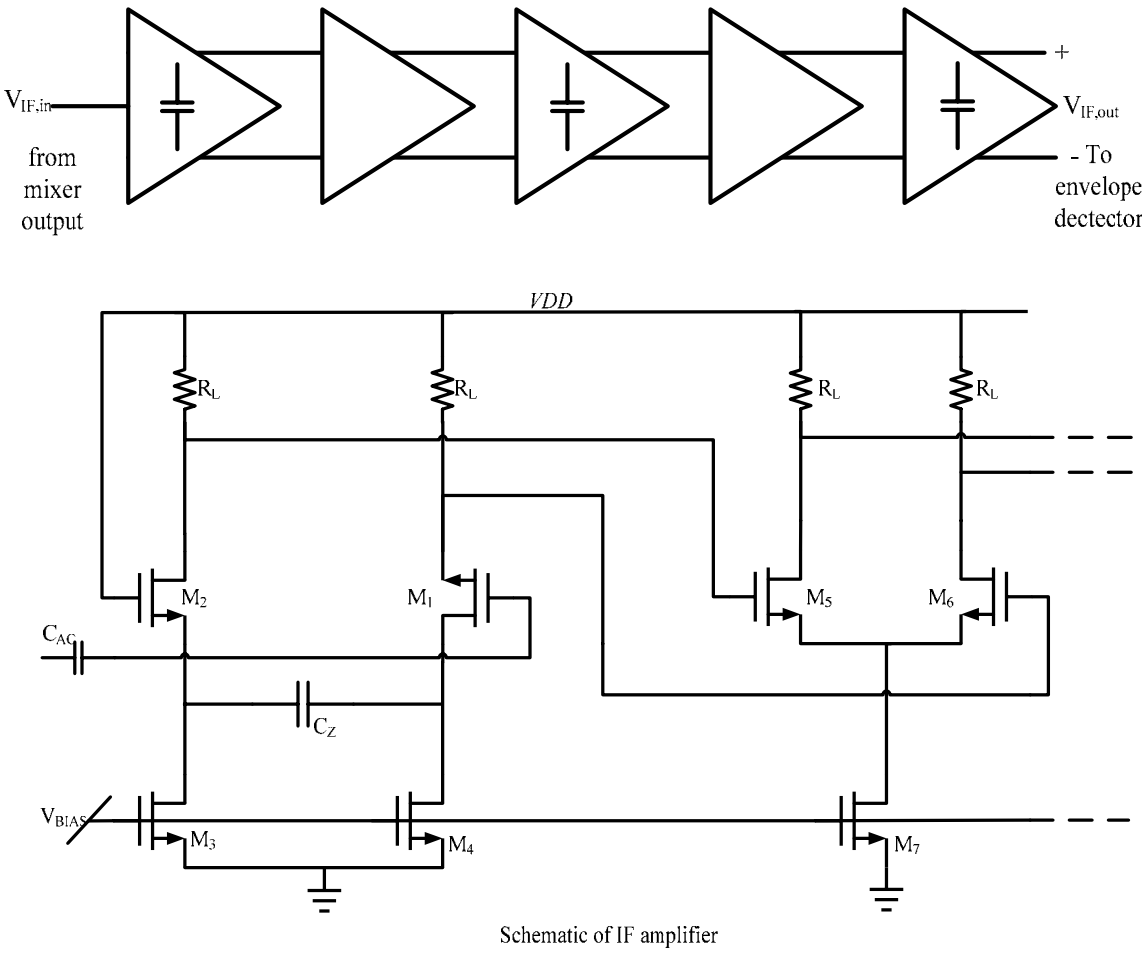


Figure 3.10 Schematic of IF amplifier

Table 3.2 Transistor sizes and elements values for IF Amplifier

Transistors	**W(µm)**	**L(µm)**	**Resistors**	**Values**
$M_{1,2}$	10.5	.360	R_L	150 KΩ
$M_{3,4}$	9.5	4.5	**Capacitors**	**Value**
$M_{5,6}$	10.5	.360	$C_{AC}(IF_{in})$	20 pF
M_7	15	2.77	C_Z	9.25pF

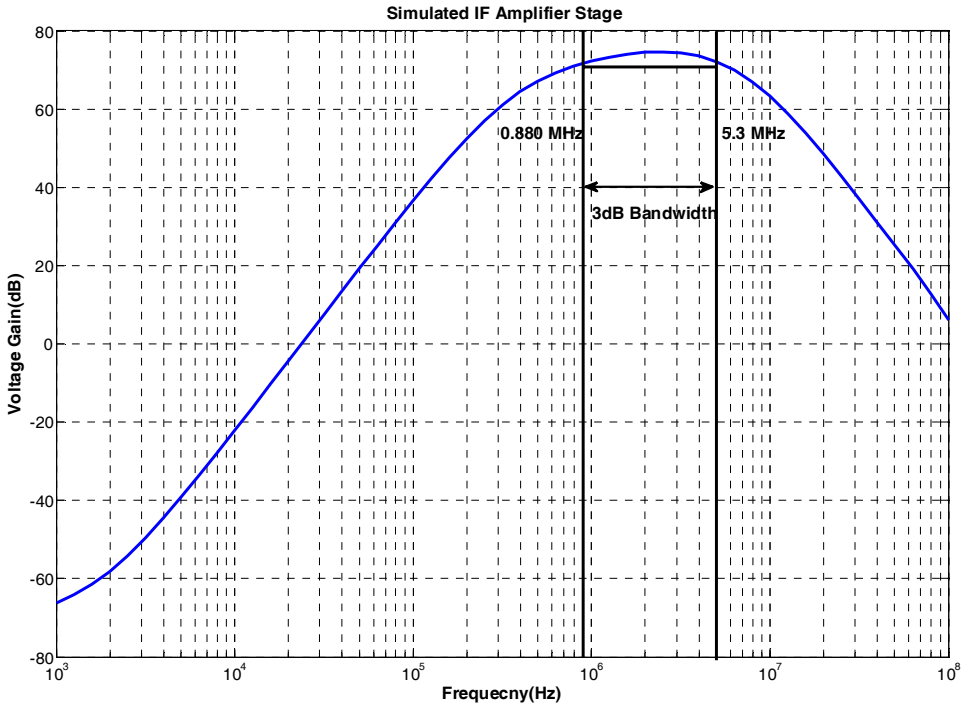


Figure 3.11 Simulated IF amplifier frequency response

3.2.3 IF Amplifier

The IF amplifier within this architecture topology is designed to provide a gain across the bandwidth of 4 MHz. For a CMOS technology, this frequency performance is met using a wideband differential pair with resistive loads. In order to operate under the low supply voltage a cascade architecture is chosen, using five differential pair gain stages optimized for maximum gain-bandwidth product for a given power consumption. Each stage provides a gain of about 15 dB [37]. The input is AC coupled to the mixer output as shown in Figure 3.10. The differential pair devices are sized to (10.5 µm /0.36 µm) and is biased in the weak inversion regime for high transconductance efficiency $\left(\frac{g_m}{I_d}\right)$. The gain stages combined to produce more than 74dB of total gain, with each stage

consuming 2μA of current. The use of identical stages and resistive loads simplifies biasing and allows simple DC coupling between stages Figure 3.10. The bias currents of all five stages are matched stages in the first, third, and fifth stages, the tail current source is split into two halves with a coupling capacitor C_z [37] of 20 pF. The coupling capacitance introduces a zero at DC in the differential transfer function. Combined with AC coupling between the mixer and the first IF stage, this technique rolls off the IF gain close to DC, where the IF signal would be too close to the baseband bandwidth. The lack of gain at DC also prevents large accumulated offsets through the IF amplifier chain [38]. The simulated frequency response of the complete IF amplifier is shown in Figure 3.11. In addition using Cadence simulation Monte Carlo statistical models were used to calculated maximum and worst-case capacitance to ensure that the amplifier would have adequate bandwidth under worst case conditions. The -3 dB bandwidth is marked in Figure 3.11, verifying that the amplifier has high gain across the band from 1 to 4MHz, with a peak gain above 70 dB. The simulated voltage conversion of gain of the combined mixer/IF amplifier front-end is about 63 dB to the IF output, with a corresponding noise figure of 35 dB. For this simulation, the LO frequency is set to about 402 MHz. As mentioned earlier, the roll-off of gain at DC causes a null in the gain response at the LO frequency. The width of this dead band is determined by the high-pass cutoff frequency of the IF amplifier, due to C_z and AC coupling to the mixer. Without the null, if the LO does happen to fall directly on top of the desired channel frequency, the input signal would be converted directly to DC, this is an undesired affect because bypassing the nonlinear function of the envelope detector will corrupt the baseband output. In order to

avoid this problem, the width of the null should be kept larger than the baseband bandwidth, but also as small as possible relative to the IF bandwidth. This will minimize the chances of the LO frequency aligning with the RF channel frequency. For this design, the allowed LO range is approximately 4 MHz and the dead band is less than 1 MHz. If in the event the LO falls directly on the channel frequency, it can also be re-tuned using the DCO therefore; the receiver could always flip to another LO frequency setting. Figure 3.12 shows the complete layout for the IF Amplifier band.

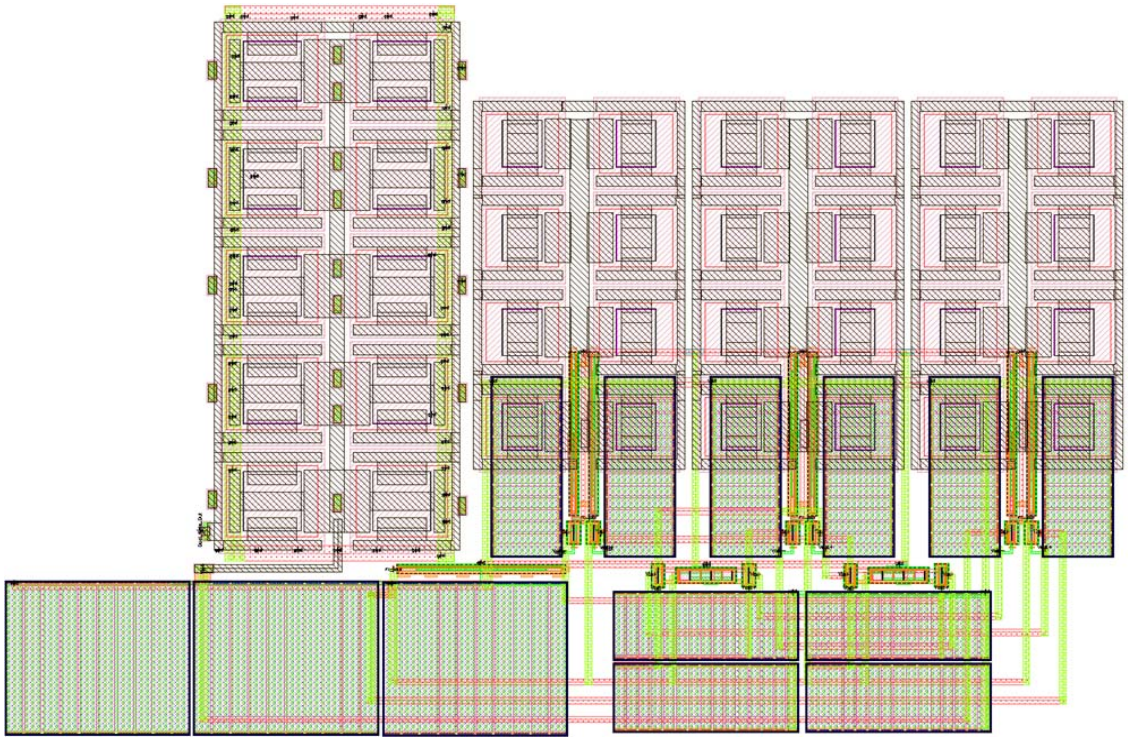


Figure 3.12 Layout for IF Amplifier

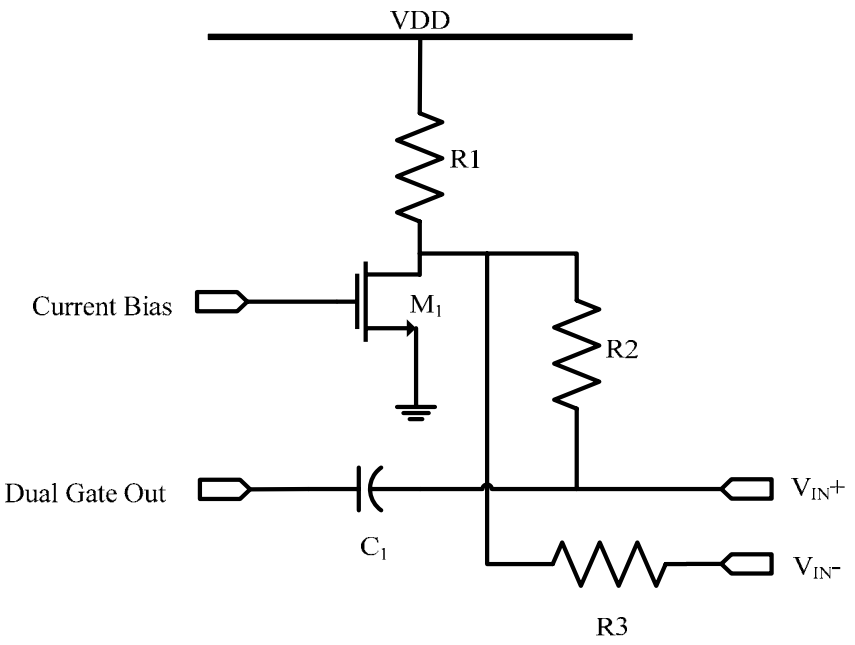


Figure 3.13 IF Bias Circuit Schematics

Table 3.3 Transistor Sizes and components values for IF Bias Stage

Transistors	**W(µm)**	**L(µm)**
M_1	9.5	4.5
Capacitors	**Value**	
C_1	20 pF	
Resistors	**Values**	
$R_{1,2,3}$	150 KΩ	

3.2.3.1 IF Bias Circuit

The IF bias circuit is shown in Figure 3.13, it is very challenging to design good constant current and bias source with high output impedance and high compliance voltage in deep submicron CMOS technology, especially at weak inversion region of operation voltages. This circuit also allows conversion from a single ended output from the dual gate mixer to a differential input for the IF amplifier stage and sets the gate bias.

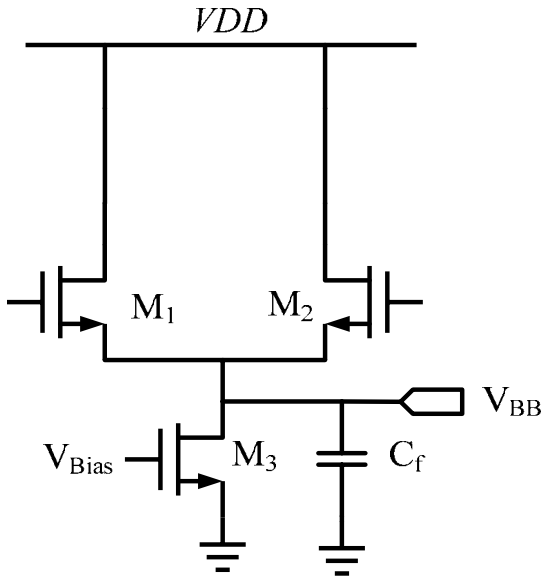


Figure 3.14 Differential Envelope Detector

Table 3.4 Transistor sizes for Differential Envelope Detector

Transistors	**W(μm)**	**L(μm)**
$M_{1,2}$	10	.20
M_3	6	1.5
Capacitors	**Value**	
C_f	20 pF	

3.2.4 Differential Envelope Detector

The envelope detection circuit is implemented with a differential pair [41]biased in weak inversion with 1 μA of current per side for maximum nonlinearity. A simplified schematic of the envelope detector is shown in Figure 3.14, including the differential detector capacitor which is connected through the PCB. The circuit common mode response functions as a traditional band-limited source follower. The envelope detector discards both frequency and phase content for the input signal and only detects the amplitude of the IF signal. A "one" is produced by transmitting the RF carrier, while the

"zero" is simply the absence of the RF carrier. OOK is inferior to other modulation methods such as frequency and phase modulation from the perspective of link efficiency [42]. However it does offer advantages in power operation compared to more FSK or PSK modulations methods.

In weak inversion the drain current is an exponential function of the gate-source voltage is expressed as 3.7 [43].

$$i_D \approx \frac{W}{L} I_{D0} exp\left(\frac{v_{GS}}{n(kT/q)}\right) \tag{3.7}$$

$$i_D \approx I_{D0}' exp\left(\frac{v_{GS}}{n(kT/q)}\right)$$

where the term n is the sub threshold slope factor and I_{DO}' is the process dependent parameter that is dependent on v_{SB} and V_T and is a constant depending on the process and device size, and Vt is the thermal voltage given by (kT/q). The subthreshold slope n factor, in .18µm process is approximately 1.5, setting the nV_t product of 40mV at room temperature. The subthershold region is very important when low power circuits are desired. For a basic envelope detector [14] shows a correlation where the nonlinear transfer function contributes a DC term at the output in response to the AC input signal; this relationship offers a simple expression which derived in [16] The voltage conversion gain for the envelope detector is given by:

$$k = \frac{V_0}{V_S} = \frac{V_S}{4nV_T} \tag{3.8}$$

Where V_S is the input AC voltage and V_0 is the DC output voltage of the envelope dectector Equation 3.8 only holds for small inputs signals where the response is

dominated by the second order current effects and is a clear representation for the detector response. More accurate expression for gain is derived in [44] using the full Bessel function representation found in [45]. Equation 3.8 also shows that the gain is independent of the device sizes and transconductance.

Other consideration for the output bandwidth which is shown by equation 3.9 determines the output pole frequency and may affect the bias for the design. Device M_3 acts as a simple current source to bias M_1 and M_2 with a constant current. When a differential IF signal drives at the gates of M_1 and M_3, the nonlinear bias point shift appears at the drain of the tail current source, converting the IF energy to a DC baseband signal. To avoid loading the IF amplifier excessively, the detector pair must not be sized too large[44]. Devices M_1 and M_2 have an aspect ratio of (10 μm /0.2 μm,) with current source device M_3 sized at (6 μm /1.5 μm). The bandwidth at the output is set by the pole at $f_{p,det}$ fashioned by C_f and the output impedance of the detector, which is approximately $1/g_{m1}$ (neglecting body effect).

$$f_{p,det} = \frac{g_{m1}}{2\pi C_f} \tag{3.9}$$

The pole should be designed to be low enough to filter out signals both at the fundamental and higher harmonics, while still having enough bandwidth to not attenuate the baseband signal. An OOK signal is a square wave with a set data rate, so in order to avoid filtering; the detector bandwidth must be higher than the desired signal. A 20 pF capacitor at the output filters any feed through from the IF signal or higher harmonics, with a baseband bandwidth of about 200 KHz. For signals inside the detector's baseband

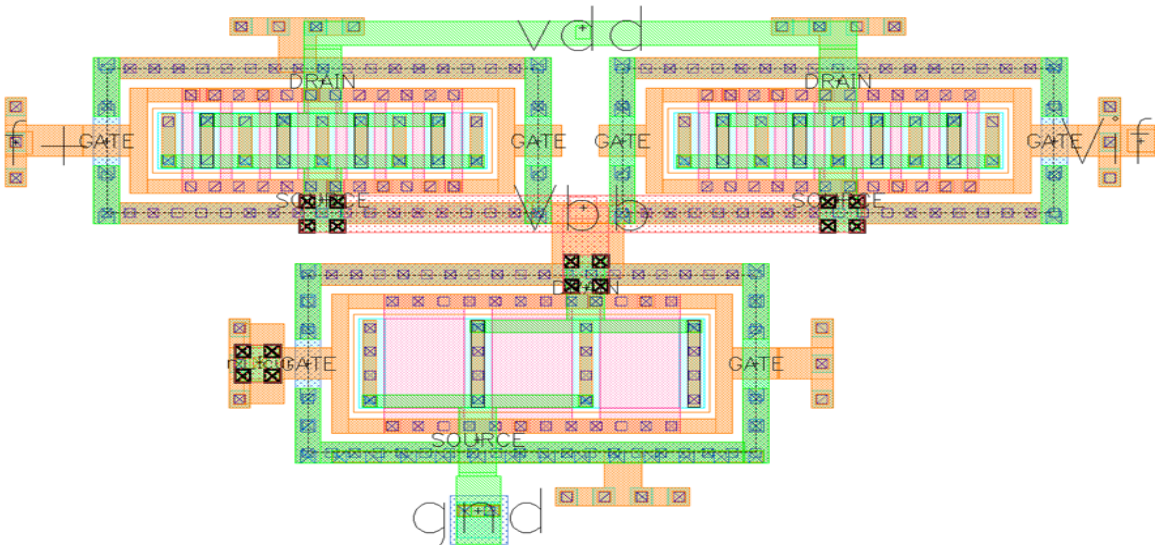


Figure 3.15 Layout for the Differential Envelope Detector

3.2.5 Digitally Controlled Oscillator

bandwidth, the differential topology rejects the differential mode, but common mode signals pass through with gain $k_{DC} \approx 1$.

The Digitally Controlled Oscillator (DCO) is implemented with the simplest type of ring oscillator, a 5-stage CMOS ring using standard library nfets and pfets. Frequency tuning is accomplished through the use of a singular resistive DACs that modify the virtual load with a CMOS varactor for of the ring Figure 3.15. Single DAC is used in order to keep the voltage swing near the middle of the range, so that the output levels can be restored to full swing using an inverter chain operating with the full V_{DD}. The scaled inverter chain serves as a non-resonant buffer to drive the mixer LO port. Low threshold devices are used to ensure sufficient speed with the 1 V supply. The 5-bit resistive tuning DACs are simple switched resistor networks. The resistor values are designed using Monte Carlo simulations to

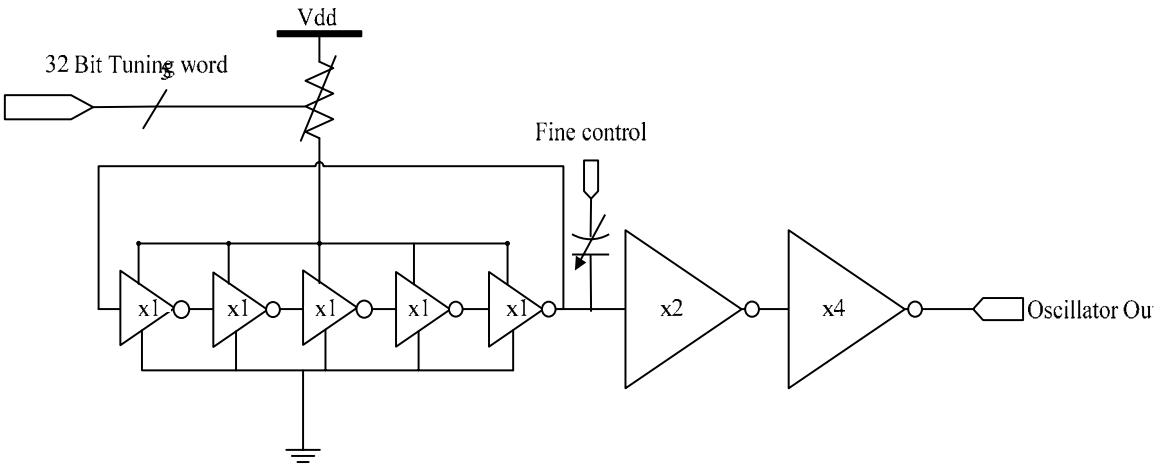


Figure 3.16 Digitally-controlled oscillator (DCO) schematic

guarantee that the LO frequency can always be tuned within the desired range across process corners and temperature variations. The frequency tuning step size, which defines the calibration precision, is approximately 100MHz. Re-calibration of the LO frequency is only required to adjust for process variations and changes in temperature and voltage that occur over time. Because calibration cycles will be relatively infrequent, the calibration power is not a significant fraction of the total power budget.

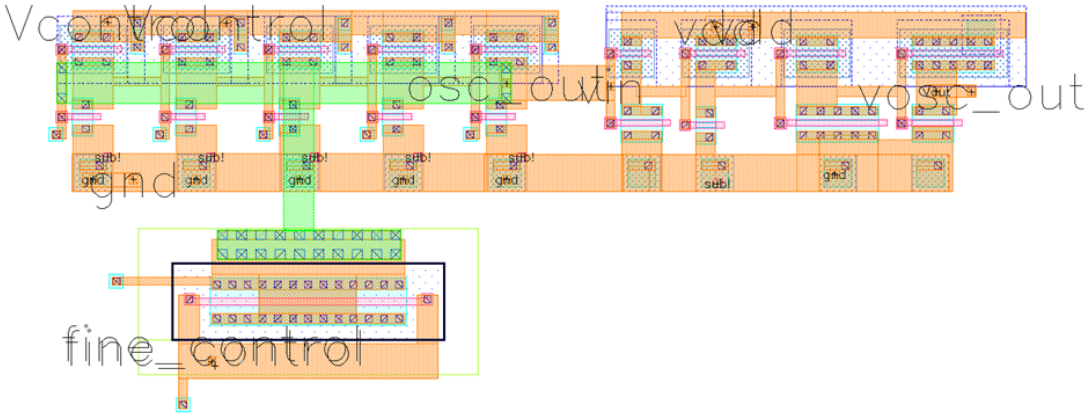


Figure 3.17 Layout for Digitally Controlled Oscillator

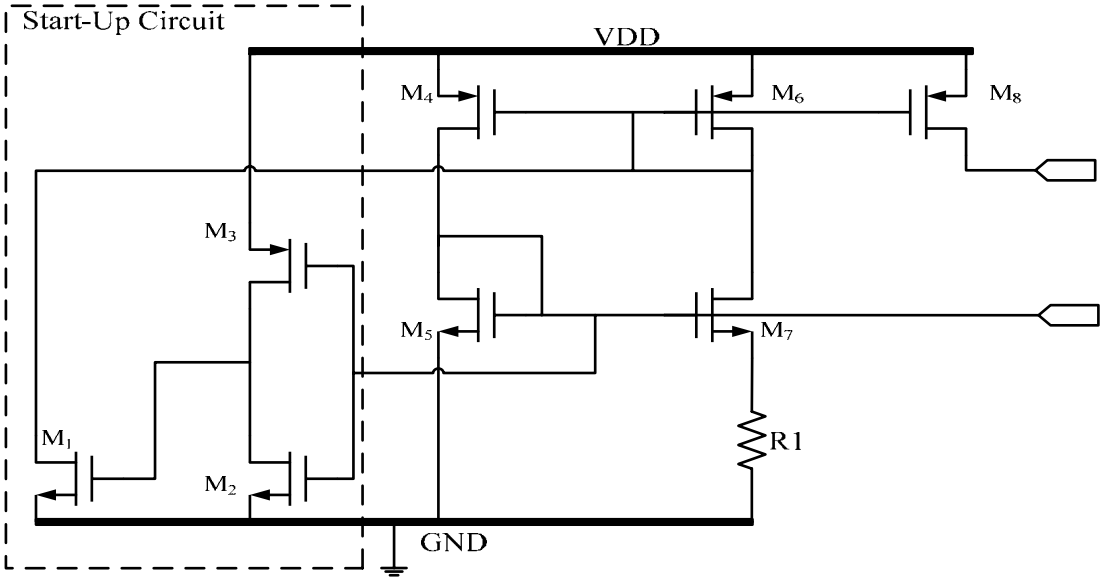


Figure 3.18 Constant Gm-Bias Circuit

Table 3.5 Transistor Sizes and Element Values for Constant Gm-Bias Circuit

Transistors	W(μm)	L(μm)	Resistors	Values
M_1	11	1	R_1	15 KΩ
M_2	11	1		
M_3	2	22		
$M_{4,6,8}$	12	2		
$M_{5,7}$	5	1.5		

3.2.6 Constant Gm-Bias Circuit

A constant Gm bias circuit is widely used in many analog integrated circuit applications, specifically for operational amplifiers and low-noise-

Table 3.6 Performance Metrics for Constant Gm Bias Circuit

Supply Voltage (V)	0.9	1	1.1
Current Consumption (μA)	1.975	2.010	2.045
DC Vref/Vbias (V)	0.460	0.461	0.463
Monte Carlo Analysis Vref/Vbias (V)	0.486	0.488	0.490

amplifiers [37]. For these types of circuits a constant voltage or constant current is often preferred. Figure3.16 shows the basic constant –gm reference with startup circuit used for biasing all the circuits (RF, IF, and Envelope Detector) of wake-up receiver.g_{m1} can be expressed as [37] :

$$g_{m1} = \frac{2\left(1 - 1/\sqrt{m}\right)}{R_1} \tag{3.10}$$

Equation 3.10 shows that transconductance is proportional to the reciprocal of the reference resistance R_1. If the transconductance and the reference voltage are process, voltage and temperature (PVT) independent then, naturally, the current generated using constant gm biasing, these parameters is also PVT independent and hence can be used as a master bias circuit on a large analog chip. This will allow stable biasing for the transconductance-sensitive circuit such as the LNA and IF Amplifier stages. Figure 3.17 shows the layout for the Constant-gm biased circuit with start-up. Table 3.6 shows the performance metrics for the Constant-gm bias circuit.

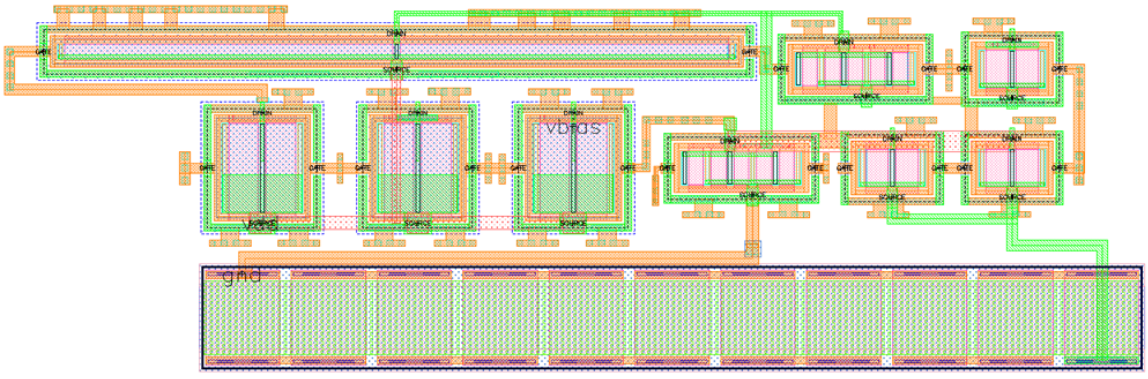


Figure 3.19 Layout for Constant-Gm bias circuit

3.2.7 Receiver Sensitivity Analysis

Due to the nonlinear nature of the envelope detector, it is not meaningful to analyze the linear noise figure (*NF*) as describe by Friis Formula.

$$F = F_1 + \sum_j \frac{F_j - 1}{\prod_{i \le j} G_i^2} \tag{3.11}$$

This analysis cannot be applied directly to the envelope detector based receiver because the envelops detector is highly nonlinear ;The receiver gain has a high dependence on the input power [45]. For the sensitivity analysis the calculation must take into account the noise it down-converts by intermodulation with the incoming signal and by self mixing and the DC noise leakage to the output. Classical cascaded stages analysis can still be applied to all the linear stages preceding the envelope detector. The RF noise at its input port can be characterized with no loss of generality by a noise factor F and a linear voltage gain G. However, these quantities do not allow one to calculate noise at the DC output of the envelope detector, so that this contribution must be taken into account separately.

For this section an example is given followed by simulation results. The sensitivity analysis considers of a front-end amplifier with a specified voltage gain (A_v) and noise factor (F_{amp}) followed by an envelope detector. The RF filter is assumed to limit the noise bandwidth to approximately the same bandwidth as the signal. With the receiver design parameters established as described above, the overall sensitivity can now be predicted with the following analysis. For the design since the filter processing happens

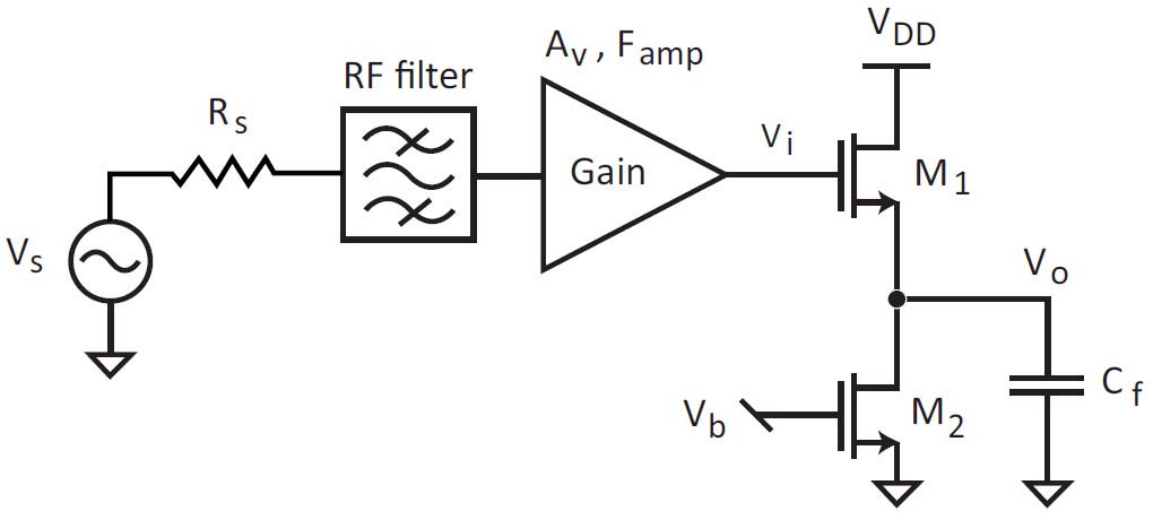


Figure 3.20 Generic receiver with envelope detector

after the nonlinear downconversion, this noise power is still spread uniformly across the whole noise bandwidth. The mixing front-end is a linear block and is modeled with its noise factor F_{amp}. The envelope detector noise is added at the output ($N_{o;ED}$), given by Equation 3.11. Noise from the IF amplifier is added at the input of the detector; the differential detector used in this receiver rejects low frequency differential noise from the IF amplifier, but common mode low frequency noise (N_{LF}) must still be taken into account, as it will pass through to the detector output with $k_{DC} \approx 1$.

Having established a simple expression for the conversion gain earlier in the chapter it was shown that the voltage conversion gain of the detector is a function of input voltage. The ultimate sensitivity can be determined by analyzing the various noise contributions and gain factors to the detector output and calculating an effective NF that depends on input signal power. For the simple receiver of Figure 3.18, there are three main noise sources:

1. Noise is added by the amplifier in front of the detector, which is captured by its linear noise factor F_{amp}.

2. The noise of the envelope detector itself appears directly at the output. This noise, $N_{o,ED}$ (V^2/Hz), can be written as [46]:

$$N_{0,ED} = 4kT\gamma \frac{1}{g_{m1}} \left(1 + \frac{g_{m2}}{g_{m1}}\right) \tag{3.11}$$

3. Any practical amplifier implementation will exhibit low frequency noise (within the detection bandwidth) at its output. This noise, N_{LF} (V2/Hz), passes through the detector with gain k_{DC} as described above, and depends on the design of the amplifier.

Each noise source is normalized to bandwidth to facilitate the calculation of an overall receiver noise factor, which is defined for a 1 Hz bandwidth. In order to take into account flicker noise and confirm calculations, circuit simulation is used.

The total noise factor F_{tot} of the entire receiver can now be written as:

$$F_{tot} = 2\, F_{amp} + \frac{N_{LF} k_{DC}^2}{N_{src} A_v^2 k^2} + \frac{N_{o,ED}}{N_{src} A_v^2 k^2} \tag{3.12}$$

where N_{src} is the noise from the source resistance ($4kTR_s$) and A_v is the gain of the front-end amplifier. Because of the dependence of k on signal level, F_{tot} increases with decreasing input power. Using $NF_{tot} = 10 \log F_{tot}$ and the detector bandwidth BW_{det}, we can calculate an input-referred noise for the receiver in dBm:

$$P_{n,in} = -174 + 10\, log(BW_{det}) + NF_{tot} \tag{3.13}$$

If the minimum signal-to-noise ratio (SNR) for reliable detection is SNR_{min}, the minimum detectable signal (P_{mds}) is the input power for which:

$$P_{mds} = P_{n,in} + SNR_{min} \tag{3.14}$$

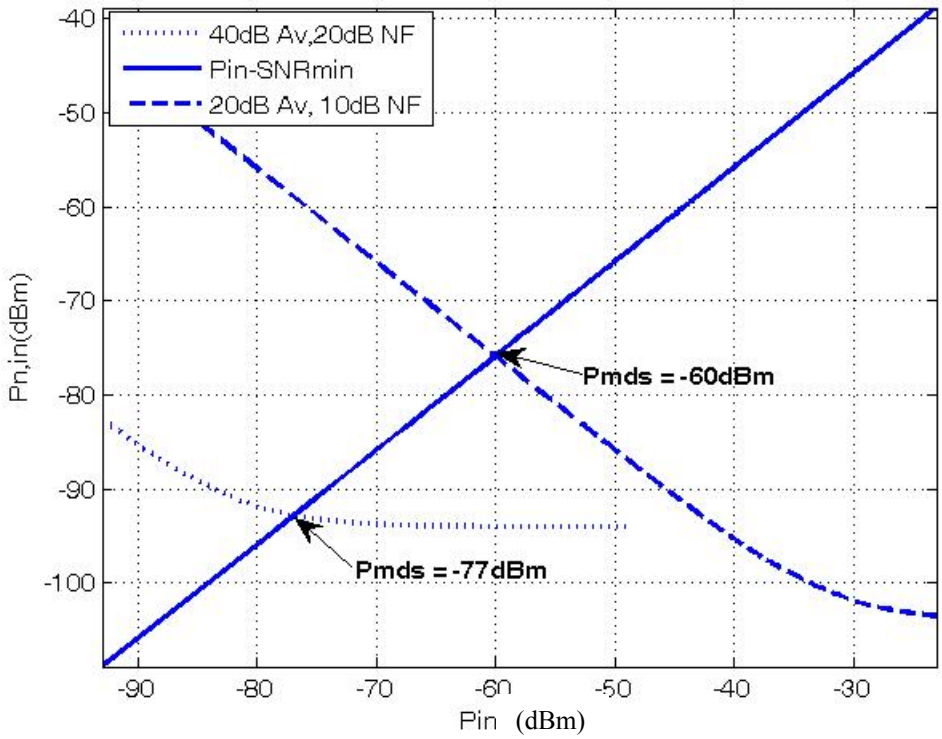


Figure 3.21 Effect of amplifier gain and NF on envelope detection receiver sensitivity

where the quantities in Equations 3.13 and 3.14 are expressed in dB. This relationship can be visualized by plotting the noise power $P_{n,in}$ and $P_{n,in} - SNR_{min}$ versus P_{in} and finding the intersection. For a typical value of 12 dB for SNR_{min}, the curves are compared for two different front-end amplifiers in Figure 3.16, one with A_v = 20 dB and *NF* = 10 dB and the other with 40 dB gain and 20 dB *NF*. For this example, the low frequency amplifier noise, N_{LF} in Equation 3.12, is ignored.

The receiver with higher gain has almost 20 dBm better sensitivity, despite 10 dB extra *NF* in the front-end. The example clearly illustrates the benefit of increasing gain in the front-end of an envelope detection receiver, even if the increase in gain results in

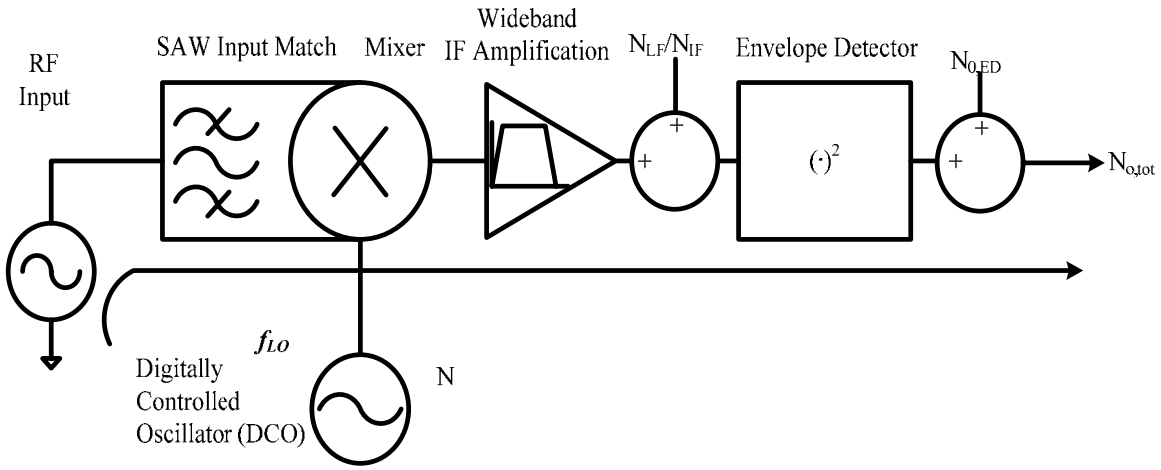


Figure 3.22 Noise sources for the uncertain-IF receiver

degraded front-end noise performance. With these general principles established, the next section describes the receiver.

The other noise source at the IF amplifier output is unique to the architecture and arises due to the wide IF bandwidth. Since the high-Q filter occurs at the input of the receiver, the noise of the front-end entering the detector is integrated across the entire IF bandwidth of 4 MHz. This noise source (N_{IF}) passes through the nonlinear transfer function of the detector with the desired signal. The noise density at the detector output due to N_{IF} can be calculated as [45]:

$$N_{0,IF} = \frac{(2\sigma^2)^2}{(4nV_t)^2}\frac{1}{BW_{if}} \tag{3.15}$$

σ^2 where is the noise variance at the IF output integrated across the entire IF bandwidth. The value of $\sigma^2$is determined by periodic steady-state simulation with periodic noise analysis.

The output noise is added as an additional factor in Equation 3.9 to arrive at the complete noise factor for the uncertain-IF receiver:

$$F_{tot} = 2F_{linear} + \frac{N_{LF}k_{DC}^2}{N_{src}G_{conv}^2k^2} + \frac{N_{0,ED}}{N_{src}G_{conv}^2k^2} + \frac{N_{o,IF}}{N_{src}G_{conv}^2k^2} \qquad (3.16)$$

where F_{linear} and G_{conv} are the linear noise figure and voltage conversion gain of the mixer/IF amplifer combined front-end. As before, final values for the noise densities in Figure 3.20 are derived from simulations and normalized over a brickwall detector bandwidth

The relative contributions to the noise factor for each term in Equation 3.16 are shown in Figure 3.17, using simulations of the final design to establish values for all noise and gain variables. The integrated IF noise (No;IF) dominates at the sensitivity limit due to the wide IF bandwidth. Reducing the IF bandwidth will proportionately reduce this noise component, at the expense of increased LO tuning accuracy and less tolerance to LO drift. The overall sensitivity is predicted by using Equation 3.16 to plot the input referred noise versus the power of the RF input signal. Since the receiver input noise level is now dependent on input level, the receiver sensitivity is found graphically. Figure 3.22 shows that the minimum detectable signal (Pmds) to guarantee 12 dB baseband SNR is -62.4 dBm. The sensitivity is high for the prototype due to the higher gain of the frequency conversion front-end. The mixer and IF amplifier combination realizes more than 50 dB gain before the detector, with corresponding Noise Factor of 35dB.

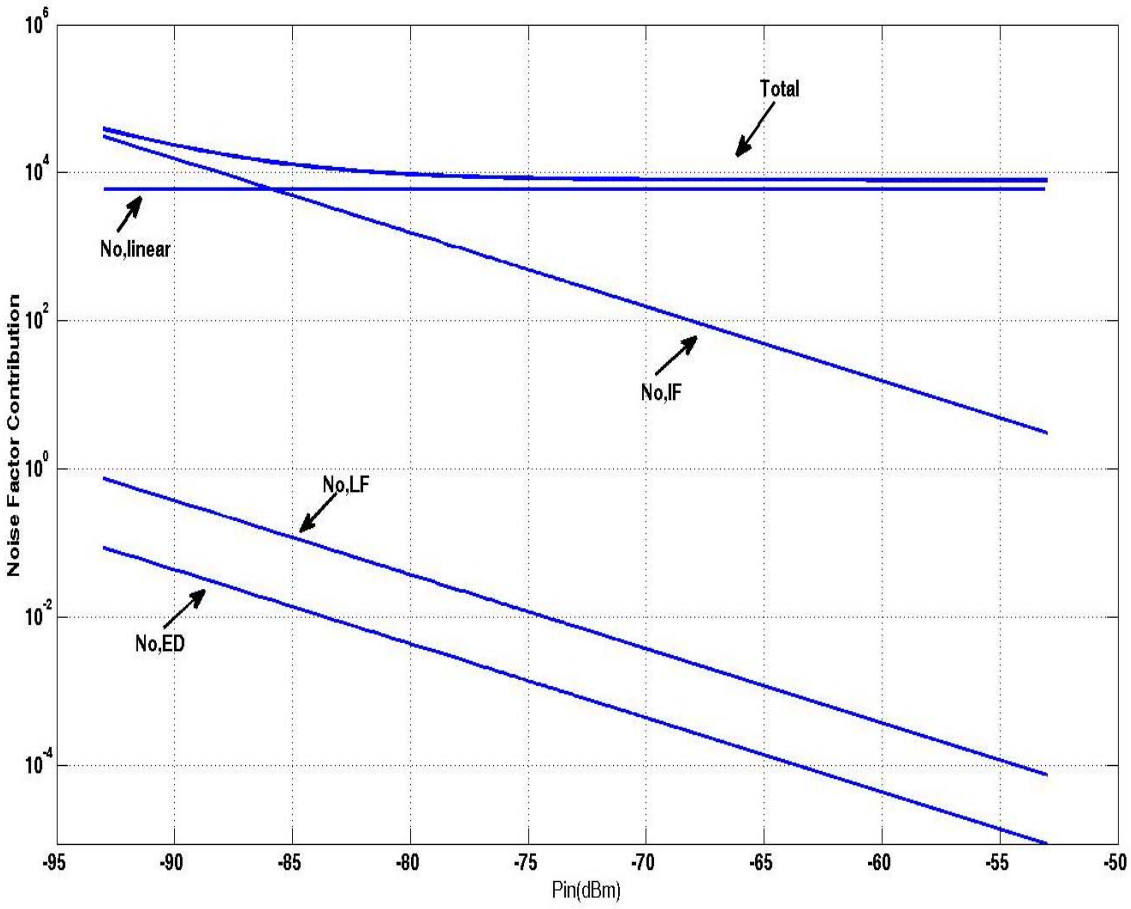


Figure 3.23 Noise Factor Contribution

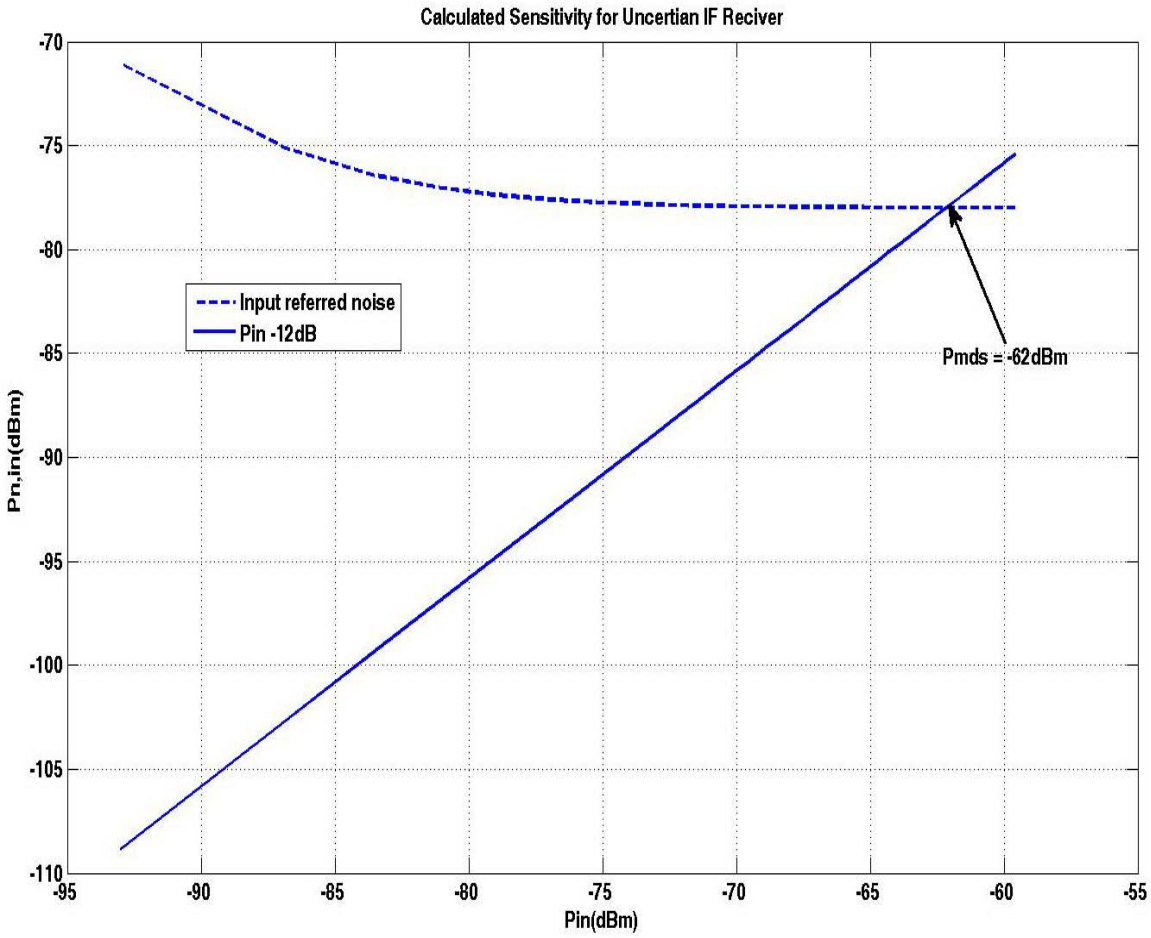


Figure 3.24 Calculated Sensitivity for Uncertain IF Reciver

CHAPTER 4
MEASUREMENT RESULTS

4.1 Introduction

In this chapter, the measurement results of the individual circuit blocks and the whole receiver are presented. The measurement setup and the necessary measurement equipment used in the experiments are discussed in detail.

4.2 Floorplan

Figure 4.1shows the Cadence Virtuoso layout of the prototype MICS Wake-up Receiver chip. The main functional building blocks of the transceiver are highlighted on the Figure 4.2. The chip is fabricated in IBM's 0.18-µm RF CMOS process (cmrf7sf) through the Integrated Circuit Fabrication Service of MOSIS. Each die has an area of 2x2 mm2 and a thickness of 250 µm.

The scope of this thesis is limited to the wake-up receiver portion of the MICS transceiver. The receiver was implemented in two different ways. Test Circuit A contains fully integrated RF front-end and baseband blocks, the Constant-gm bias circuit, the Dual gate mixer, Digitally Controlled oscillator IF Amplifier stage and differential input envelope detector. Test Circuit B is the breakaway circuit that allows for individual testing of circuit blocks, however it does not have the Constant-Gm biasing circuit.

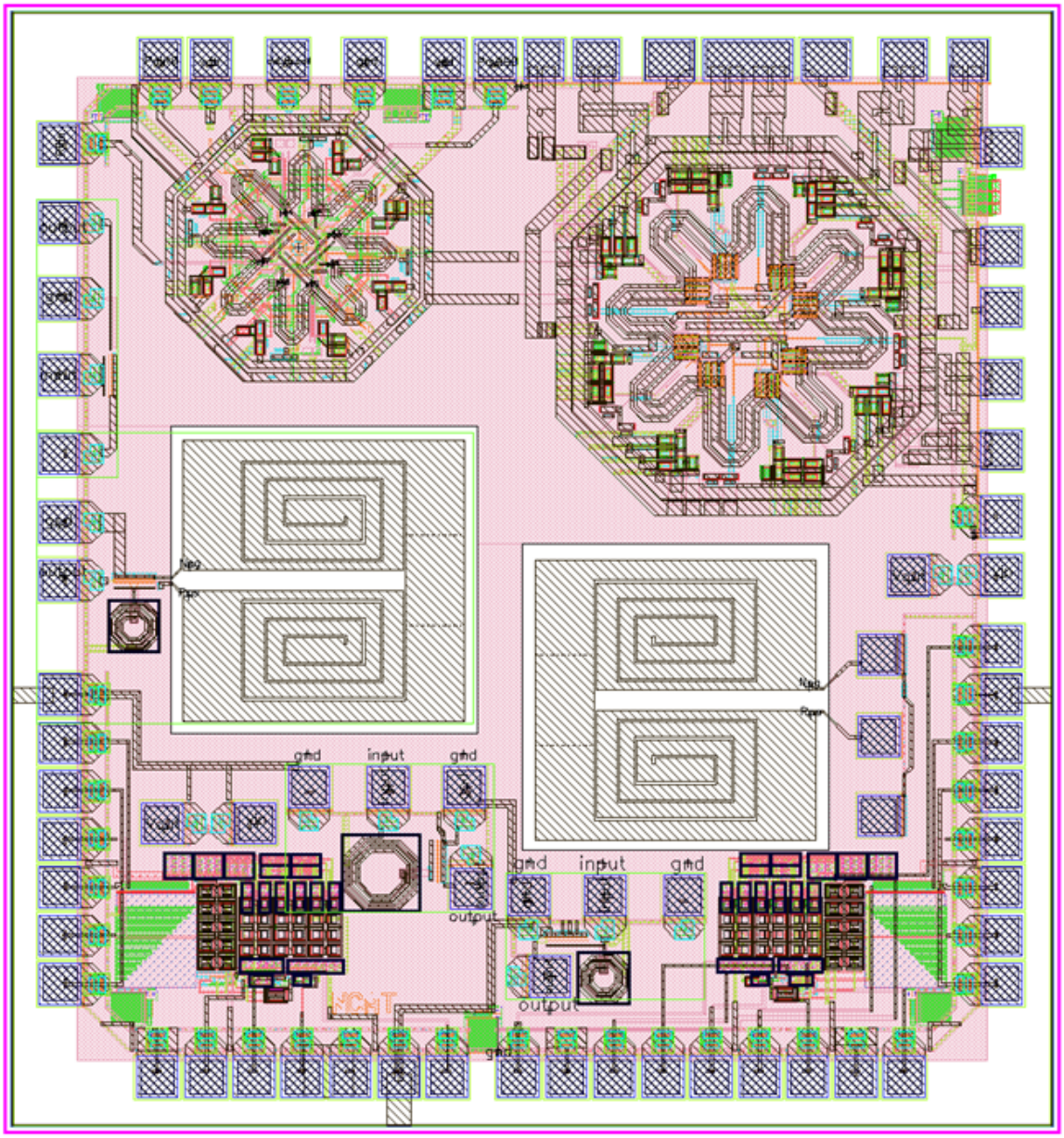


Figure 4.1Cadence Virtuoso Layout Design Floorplan

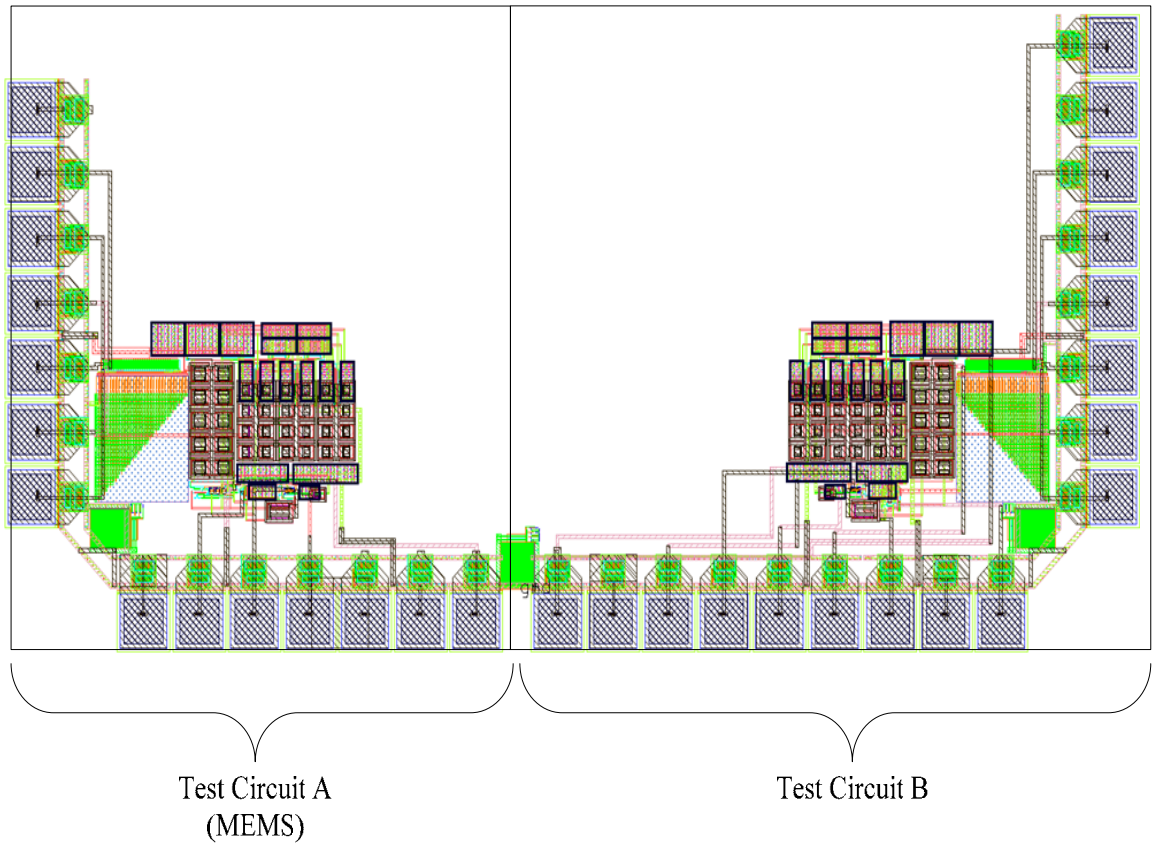


Figure 4.2 Test circuit A with MEMS device and Test Circuit B beak-out testing

4.3 Test Board and Measurement Setup

Figure 4.3shows the test board used for interfacing the chip to the measurement devices. The PCB is fabricated on an FR-4 material which has a dielectric constant of 4.6. The dielectric thickness of the board is selected to be 31 mils for smaller trace widths. The PCB has top and bottom metal layers and a dielectric layer in between. Top and bottom; solder mask and silk screen layers were also included in the PCB manufacturing process. The metal layers are chosen to be 1 oz. copper which has a height of 1.4 mil. A low-loss material could also be used instead of FR-4 for better noise performance;

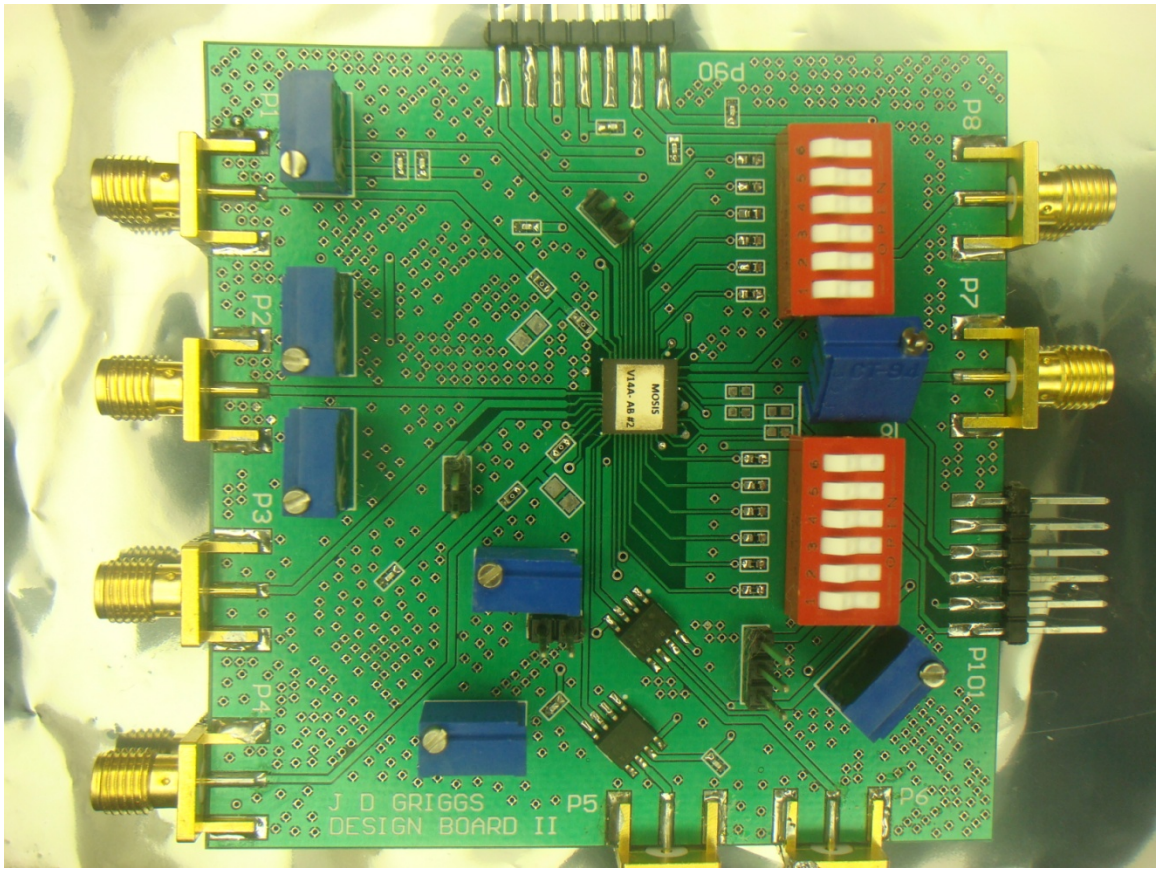


Figure 4.3 Photograph of the test board for characterization and measurement of MICS Receiver

however, in a UHF design such as this one, the board losses are not as significant as in a multi-GHz one. A ground plane covers most of the top and bottom surfaces of the PCB and it is connected to the internal ground of the chip by the exposed pad and several pins.

In order to obtain 50-Ω transmission lines on an FR-4 board with 31-mil dielectric thickness, the metal line widths was calculated for different technologies. For a microstrip implementation, the line width is calculated to be 56 mils. For grounded coplanar waveguide, however, the width of the trace should be 28 mils and the spacing between the signal trace and the ground metals should be 6 mils gap. The coplanar

waveguide technique is primarily used by PCB designers since coplanar wave guide model that presents a smaller trace width and a lower loss performance compared to its microstrip counterpart.

Measurements of different blocks have been performed on a single test board. Including all test schemes in a single board significantly increases the parasitic effects. Necessary precautions are taken in the layout, the assembly and the test phase to minimize these effects. The device under test has been electrically isolated from others by powering down the rest. All measurements have been performed under a 1-V supply. Separate power supplies are used for the PCB devices and the VDD pin that powers the chip. Potentiometers are employed for fine tuning the bias voltage values. Jumpers are used not only to power different blocks but also to monitor the power consumption thereof. In order not to load the device under test, buffers are placed between 50-Ω measurement instruments and the outputs of the circuit blocks. Initially, a commercially available hybrid amplifier, AD8045, has been used in a unity-gain buffer configuration on the PCB. The packaged resonator can be seen wire-bonded to the die similar to the prototype on Figure 5.2. The complete WuRx fits conveniently in the corner of the chip, which is appropriate for its role as an auxiliary receiver.

Agilient 1131A, InfiniiMax Active Differential Probe System is used as well. The probe system includes an amplifier with a BNC connector and is capable of making DC to 100-MHz single-ended and differential measurements. It has an input RC loading of 1 M-ohm resistance in parallel with a 10-pF capacitance, typically 450-mV or less displayed noise and 50-ohm output impedance through a BNC connector.

Table 4.1 Measurement equiptment

Model	Description
Agilent N5242A	ENA Series Network Analyzer 100kHz – 8.5 GHz
Agilent 4691B	Ecal-module 300kHz
Agilent E4438C	ESG Vector Signal Generator
Agilent E4440A	PSA Spectrum Analyzer
Agilent MSOX3054A	Mixed Signal Oscilloscope
Agilent DSO90254A	Infiniium Oscilloscope
34401A	Digital Multimeter
HP E3620A	DC Power Supply
HP 3325A	Synthesizer/Function Generator

Different laboratory equipment has been used for the performance verification. Table 4.1shows the descriptions and the functions of the test equipments in the measurement setup. The s-parameter of a two-port network has both magnitude and phase components to be measured. The measurement of the s-parameters of a device under test (DUT) is performed at fixed ports which are defined by the two-port calibration of the vector network analyzer. Due to the need for an interface between the DUT and the measurement devices, a test fixture which has traces and off-chip components is used. The length of the traces in the test fixture changes the phase information of the s-parameters of the device. It also affects the gain and the input/output reflection data. When measuring a device in a test fixture, the traces on the PCB can be considered as extensions of the coaxial cable that connect the fixture to the network analyzer. If the trace length is known, the reference plane can be moved close to the DUT with a simple calculation. Electrically moving the reference plane to the desired location can also be performed in the network analyzer calibration menu and this operation is

called port extension. By performing port extension on each port of the fixture, the measurement plane is extended beyond the calibrated port to the terminals of the DUT. Simple subtraction of the delay due to the length of the traces is generally performed for the case when the traces behave as 50-Ω transmission lines. If the test fixture is more involved and has lossy components and traces with characteristic impedance other than 50 Ω, more complex calculations and de-embedding techniques should be employed to mathematically subtract these from the measured data to find the accurate behavior of the DUT. One approach is replacing the DUT with a short, measuring the total insertion loss and phase shift, and then assigning the portions of it to the input and the output traces based on the fixture configuration. This is the simplest de-embedding technique to compensate for the component and the trace losses. A significant literature exists for proper de-embedding techniques. Abidi and Leete developed a formula based on Friis' well-known equation for de-embedding the gain and the noise figure measurements of differential amplifiers [47]. The method developed by Antonini *et al.* uses both measured and computed scattering parameters to de-embed the test fixture by avoiding a complex calibration process [48]. Another important factor during the measurement is the performance of the measurement device itself. As an example, if the internal noise of the measurement device is high and this is not taken into consideration, the measurements will never reflect the actual performance of the device under test. In [49], Belkim explains this phenomenon and describes a method for finding the proper correlation factor to de-embed the effect due to the non-ideal loss/noise figure of the measurement device.

4.4 Ring Oscillator LO measurement

Test Circuit A has a standalone ring oscillator test block included on the prototype chip for characterization purposes, consisting of a DCO and LO buffers identical to the circuits used in the fully integrated receiver, along with an open-drain buffer to drive off-chip instrumentation. For receiver functionality, the main metrics of interest for the LO are process compliance and transient stability. The first factor is addressed through frequency calibration, while the latter determines how often calibration is required. The measured tuning range of the LO is from approximately 386MHz to 470MHz, with the tuning curves for two different samples plotted in Figure 4.3.Fine tuning is performed using a varactor which results in 20MHz tuning range as shown in Figure 4.4.

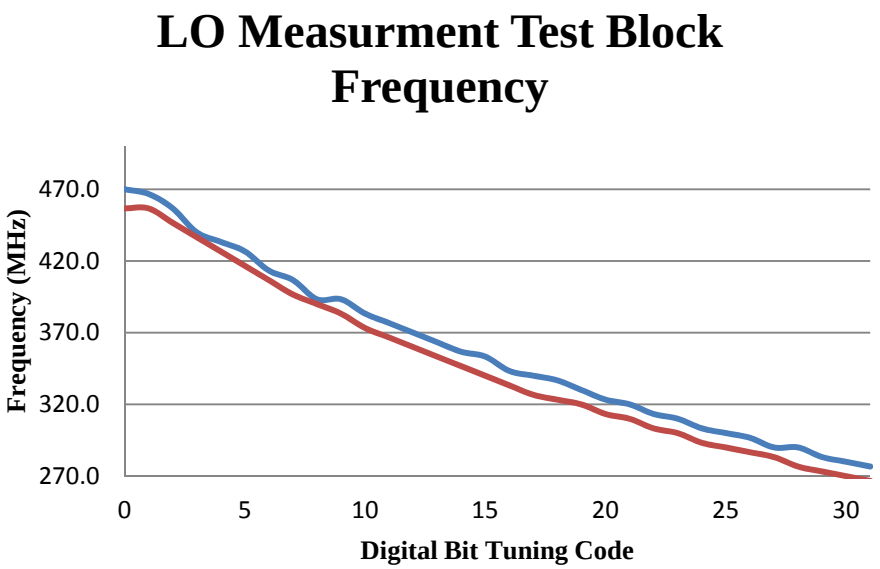


Figure 4.4 LO Tuning Range

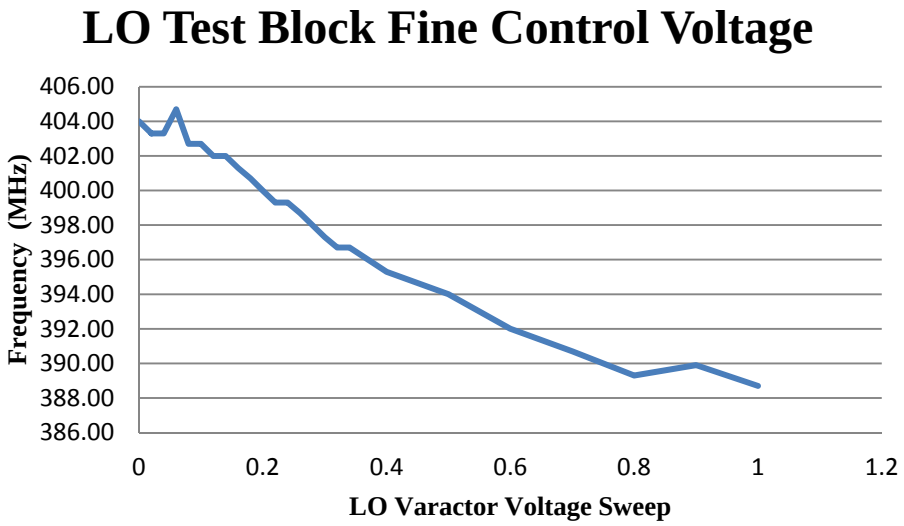


Figure 4.5 Varactor (fine tuning frequency range)

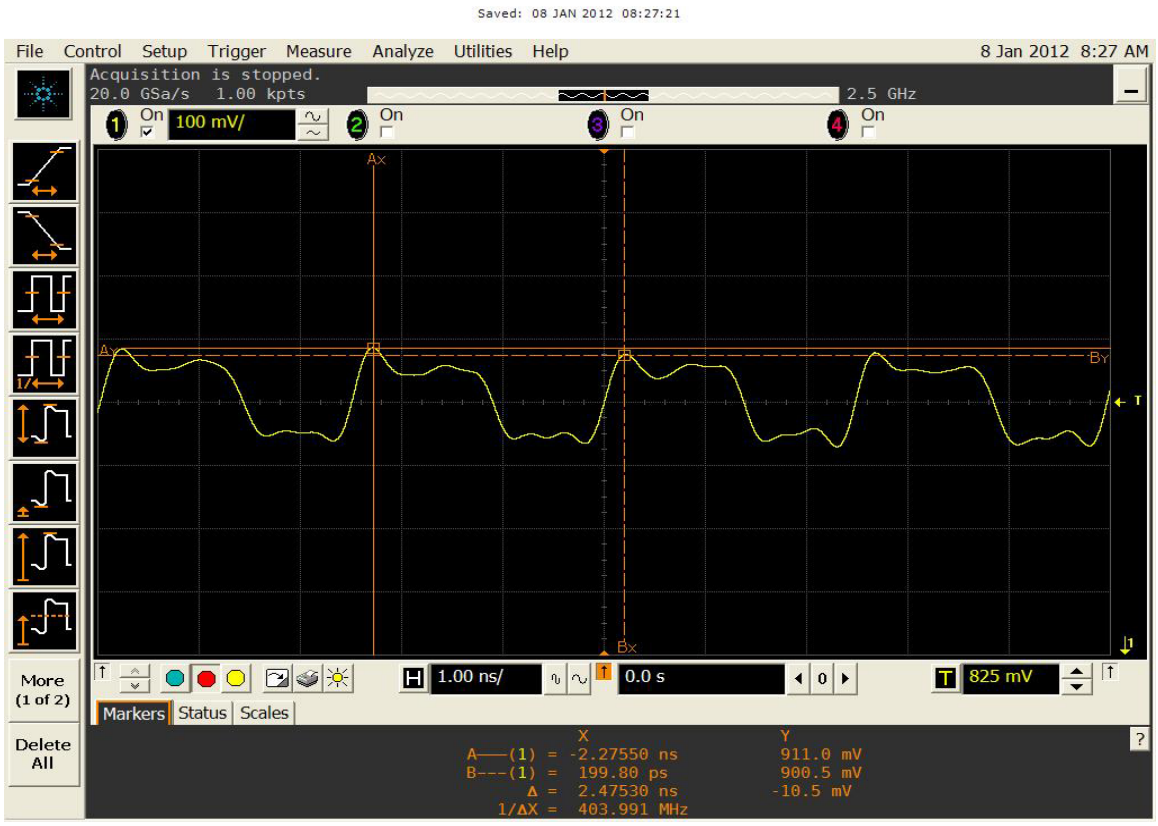


Figure 4.6 LO waveform output

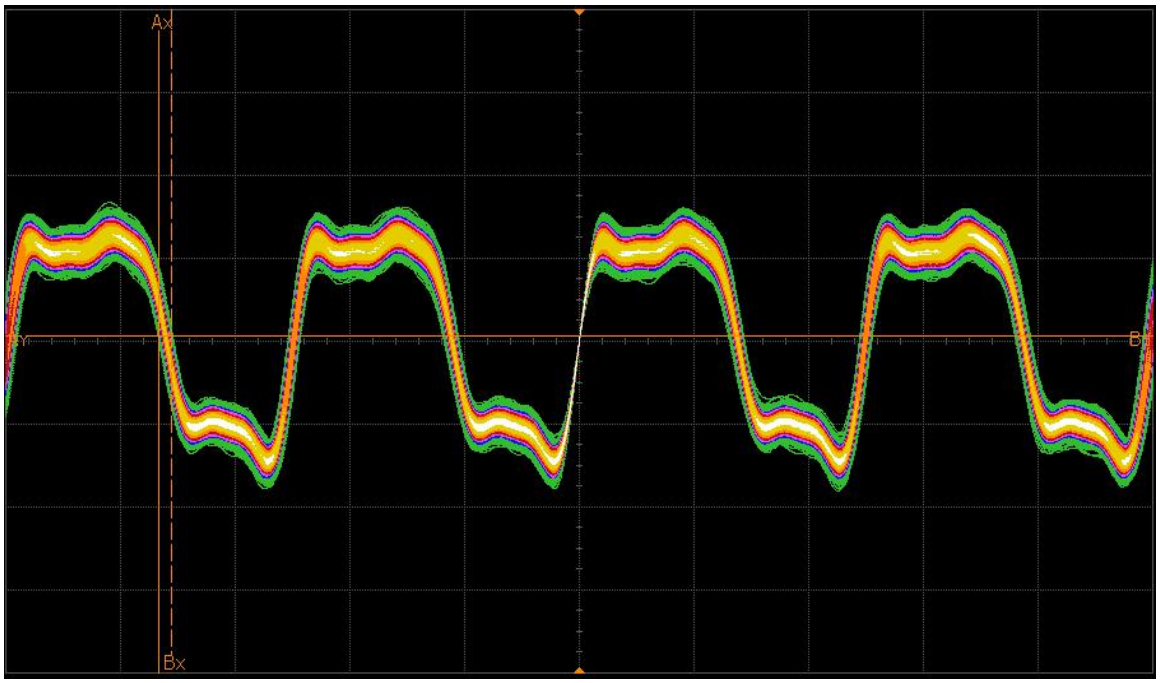


Figure 4.7 Measured Waveform Voltage peak to peak Wave Jitter

The tuning range to cover process variation should be more than enough to handle any age-related frequency drift of the ring oscillator. The receiver architecture is also robust to short-term LO frequency variation, or jitter. The measured time domain waveform of the ring oscillator LO is shown in Figure 4.6 from an Agilent Infiniium DSO90254A sampling oscilloscope. The asymmetry of the waveform shape is due to the open-drain buffer included on-chip to drive the test instrument. The period of the LO signal is 2.475 ns, with peak-to-peak jitter of about 60ps. The wake-up receiver tolerates this jitter due to large IF bandwidth.

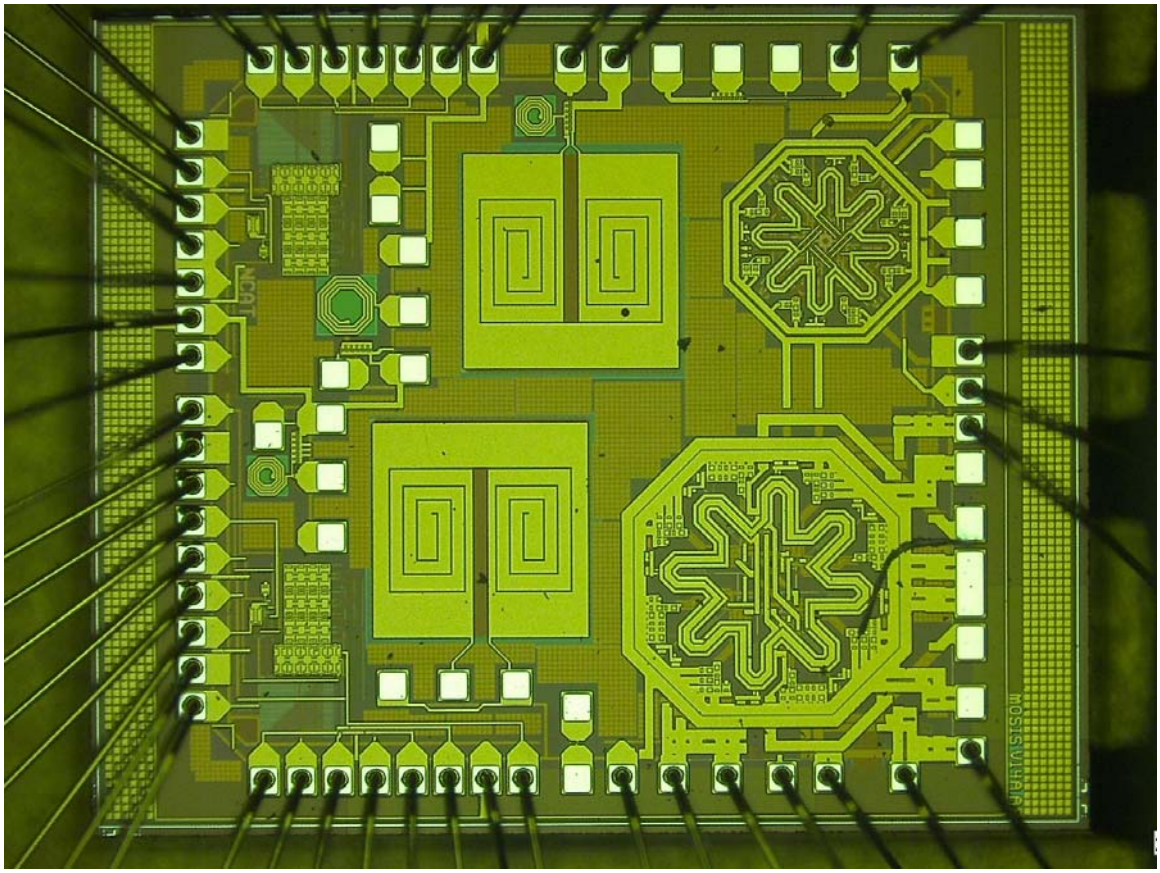


Figure 4.8 Full-Chip with wirebonding

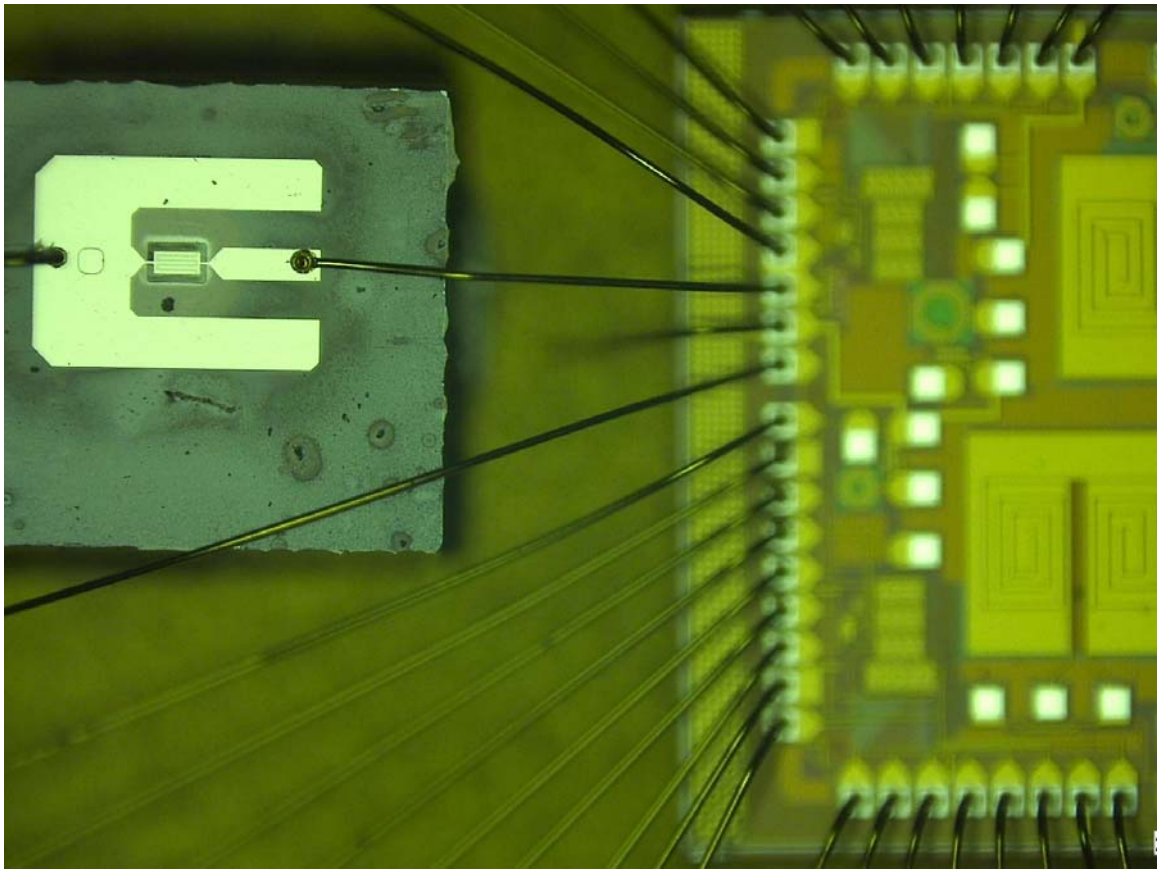


Figure 4.9 Chip with wire bonding with MEMS resonator

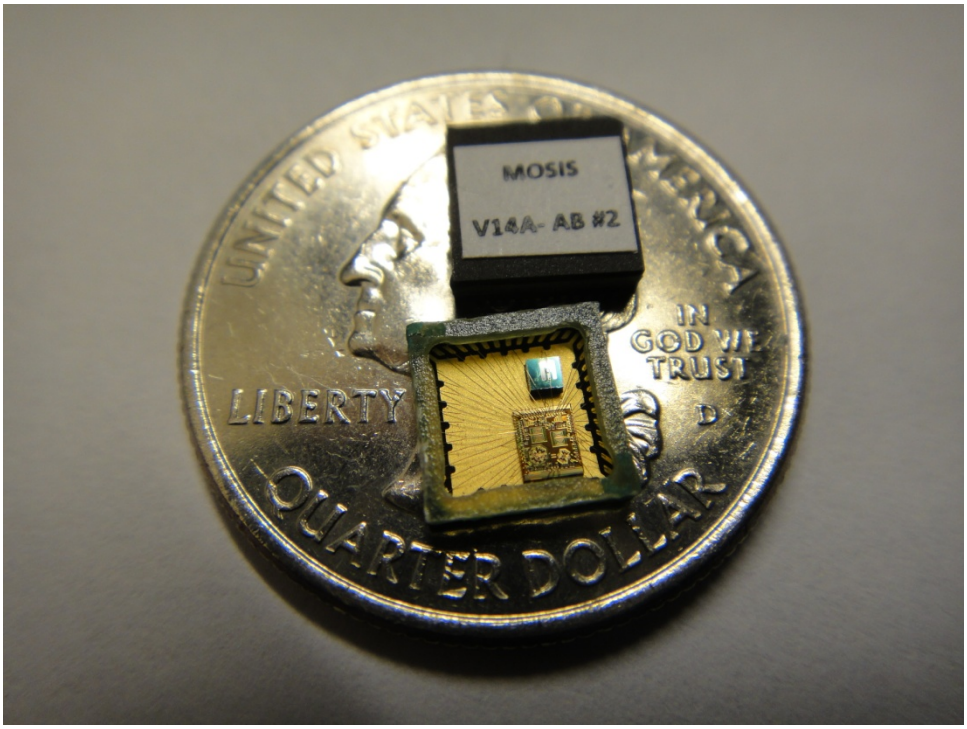


Figure 4.10 Wake-up Receiver and MEMS resonator

4.5 Performance Summary

Table 4.2 Device Performance

Parameter	Measurement
Global supply voltage	1V
Carrier frequency/modulation	406MHz / OOK
Power dissipation Mixer If amplifiers LO + buffers Envelope Detector Total (Receiver)	 8 µW 22 µW 28 µW 2µW 60 µW
Data rate (kbps)	100 kbs
Sensitivity for BER (dBm)	-62

Measurement Summary

The overall performance of the wake-up receiver is summarized in Table 4.2. The breakdown of power consumption among the different receiver blocks are shown in this table. The receiver sensitivity is -62 dBm. In order to overcome the nonlinearity of the envelope detector, the bulk of the power consumption is consumed in the RF front end (Mixer Amplifier and LO).

CHAPTER 5
CONCLUSION

This thesis presented a comprehensive investigation of a wake-up receiver and explored the limits of the ultra-low power receiver design. This chapter summarizes the work and puts the results in perspective by comparing to previously published work in the area of wireless receivers for WBAN. This work concludes with suggestions for future research on the subject of wake-up receivers. The substantial power reduction is made possible through the combination of two technology factors:

1. Scaled CMOS to realize the high speed and low energy of modern CMOS transistors makes it possible to run a ring oscillator at 404 MHz with very little power consumption.

2. MEMS technology: High Q micromechanical resonators provide RF band selection.

The uncertain-IF receiver saves power by moving the burden of band selectivity from an accurate local oscillator to the front-end filter. MEMS-based radio architectures continue to gain popularity and advances in resonator technology can open up new opportunities in circuit design. The uncertain-IF receiver is a good example of such a MEMS-enabled architecture. It is important to note that the design choices made for this receiver were strongly dictated by the very low power budget and were optimized for the minimum possible power consumption. A wide IF bandwidth was selected to minimize required LO tuning accuracy and lower complexity. The resulting design has high tolerance to LO variability and re-calibration is rarely required.

Chapter 1 gave the background as to the various wireless sensor networks that are currently implemented and the design challenges that are present for transmitting a signal into and out of the body. For medical implantable devices a specific band spectrum was allocated called the Medical Implantable Communication Service Band. For wireless sensors novel power schemes must be implemented in order to optimize the duty cycle specifically the trade-off between latency and power. The implementation and the advantage of using a wake-up receiver are presented.

Chapters 2 discussed typical RF heterodyne receiver topologies and benefits and trade-off for each one. Also shown were the limitations on CMOS technologies for passives components for inductors and reasons for low quality factors were explored. We explored the advantages of using an AlN MEMS resonator and its effect on the RF frontend that affected how we designed the LO. Chapter 2 presented the CMOS circuits used in the wakeup receiver. Finally data and measurements were presented in Chapter 4.

Certain improvements can be incorporated into the design of the wake-up receiver. Free running LO is difficult to adjust manually. For future work we strongly suggest on chip PLL to lock the frequency to an external reference signal. Once locked the PLL can be powered down for power savings, it was not consider due to power management specification however previous work from [50] shows a low power PLL implementation that could be integrated into our circuit with minimum power budget increase. For the MEMS device laser trimming is a possible option in order to maximize Q response and reduce motional resistance, however this will have a trade-off between the low IF pass

bandwidth, which will reduce noise and increase sensitivity but requires a tighter tolerance on the LO to fall into the mixer band. Future work suggests a progression towards a SoC chip design and this is possible due to the post-CMOS fabrication for the MEMS device or a implementation for flip-chip to remove or lower the parasitics present in the wirebonding implementation. This work clearly demonstrated the feasibility of a wake-up receiver operating with a 1V -60µW power budget for MICS applications. The wake-up receiver can be used in other UHF applications such as the 435MHz ISM band.

REFERENCES

1. Zimmerman, T.G., *Personal area networks: near-field intrabody communication.* IBM Syst. J., 1996. **35**(3-4): p. 609-617.
2. Falcon, C., *Inside Implantable Devices.* Medical Design Technology, 2004. **8**(10): p. 24-27.
3. Witters, D., et al. *Medical device EMI: FDA analysis of incident reports, and recent concerns for security systems and wireless medical telemetry*. in *Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on*. 2001.
4. FCC Washington, D., *"MICS band plan"*, in *rules and regulations*Jan 2003.
5. Authority, A.C., *"Planning for Medical Implant Communications Systems (MICS) and Related Devices"*, A.C. Authority, Editor Oct. 2003.
6. Ghovanloo, M. and K. Najafi, *A wideband frequency-shift keying wireless link for inductively powered biomedical implants.* Circuits and Systems I: Regular Papers, IEEE Transactions on, 2004. **51**(12): p. 2374-2383.
7. Cook, B.W., *Low Energy RF Transceiver Design*, in *EECS Department, University of California, Berkeley*2007.
8. Gu, L. and J.A. Stankovic, *Radio-Triggered Wake-Up for Wireless Sensor Networks.* Real-Time Systems, 2005. **29**(2): p. 157-182.
9. Kim, H., et al., *CMOS passive wake-up circuit for sensor network applications.* Microwave and Optical Technology Letters, 2010. **52**(3): p. 597-600.
10. Wenyi, C., et al. *Analysis, design and implementation of semi-passive Gen2 tag*. in *RFID, 2009 IEEE International Conference on*. 2009.
11. Marinkovic, S.J. and E.M. Popovici, *Nano-Power Wireless Wake-Up Receiver With Serial Peripheral Interface.* Selected Areas in Communications, IEEE Journal on, 2011. **29**(8): p. 1641-1647.
12. Malinowski, M., et al., *CargoNet: a low-cost micropower sensor node exploiting quasi-passive wakeup for adaptive asychronous monitoring of exceptional events*, in *Proceedings of the 5th international conference on Embedded networked sensor systems*2007, ACM: Sydney, Australia. p. 145-159.
13. Doorn, B.V.d., W. Kavelaars, and K. Langendoen, *A prototype low\&\#45;cost wakeup radio for the 868 MHz band.* Int. J. Sen. Netw., 2009. **5**(1): p. 22-32.
14. Ansari, J., D. Pankin, and P. Mähönen, *Radio-triggered Wake-ups with Addressing Capabilities for Extremely Low Power Sensor Network Applications.* International Journal of Wireless Information Networks, 2009. **16**(3): p. 118-130.
15. Durante, M.S. and S. Mahlknecht. *An Ultra Low Power Wakeup Receiver for Wireless Sensor Nodes*. in *Sensor Technologies and Applications, 2009. SENSORCOMM '09. Third International Conference on*. 2009.
16. Pletcher, N.M., S. Gambini, and J. Rabaey, *A 52 uW Wake-Up Receiver With 72 dBm Sensitivity Using an Uncertain-IF Architecture.* Solid-State Circuits, IEEE Journal of, 2009. **44**(1): p. 269-280.

17. Le-Huy, P. and S. Roy, *Low-Power Wake-Up Radio for Wireless Sensor Networks.* Mobile Networks and Applications, 2010. **15**(2): p. 226-236.
18. Takiguchi, T., et al. *A Novel Wireless Wake-Up Mechanism for Energy-Efficient Ubiquitous Networks*. in *Communications Workshops, 2009. ICC Workshops 2009. IEEE International Conference on*. 2009.
19. Friis, H.T., C.B. Feldman, and W.M. Sharpless, *The Determination of the Direction of Arrival of Short Radio Waves.* Proceedings of the Institute of Radio Engineers, 1934. **22**(1): p. 47-78.
20. Johnson, C.C. and A.W. Guy, *Nonionizing electromagnetic wave effects in biological materials and systems.* Proceedings of the IEEE, 1972. **60**(6): p. 692-718.
21. Curty, J.P., et al., *Remotely powered addressable UHF RFID integrated system.* Solid-State Circuits, IEEE Journal of, 2005. **40**(11): p. 2193-2202.
22. Otis, B.P., et al. *An ultra-low power MEMS-based two-channel transceiver for wireless sensor networks*. in *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*. 2004.
23. Otis, B., Y.H. Chee, and J. Rabaey. *A 400 μW-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks*. in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. 2005.
24. Kucera, J., *"RF IC Technologies for Wireless Applications".* 2000. **Infineon Technologies**.
25. Aguilera, J. and R. Berenguer, *Introduction Design and Test of Integrated Inductors for RF Applications*, 2004, Springer US. p. 1-22.
26. Borremans, J., et al. *A 400μW, 4.7–6.4GHz VCO under an above-IC inductor in 45nm CMOS*. in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*. 2008.
27. Jing, W., et al. *1.51-GHz nanocrystalline diamond micromechanical disk resonator with material-mismatched isolating support*. in *Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS)*. 2004.
28. Sheng-Shian, L., et al. *Micromechanical "hollow-disk" ring resonators*. in *Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on. (MEMS)*. 2004.
29. Stephanou, P. and A. Pisano. *PS-4 GHZ Contour Extensional Mode Aluminum Nitride MEMS Resonators*. 2006. IEEE.
30. Atashbar, M.Z., B.J. Bazuin, and S. Krishnamurthy. *Design and simulation of SAW sensors for wireless sensing*. in *Sensors, 2003. Proceedings of IEEE*. 2003.
31. Aissi, M., et al. *A 5.4GHz 0.35/spl mu/m BiCMOS FBAR Resonator Oscillator in Above-IC Technology*. in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*. 2006.
32. Carpentier, J.F., et al. *A SiGe:C BiCMOS WCDMA zero-IF RF front-end using an above-IC BAW filter*. in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. 2005.

33. Razafimandimby, S., et al. *A 2GHz 0.25μm SiGe BiCMOS Oscillator with Flip-Chip Mounted BAW Resonator*. in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*. 2007.
34. Dubois, M.A., et al. *Integration of high-Q BAW resonators and filters above IC*. in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. 2005.
35. Pieters, P., D. Qi, and A. Witvrouw. *Integration and Packaging MEMS Directly Above Active CMOS*. in *High Density packaging and Microsystem Integration, 2007. HDP '07. International Symposium on*. 2007.
36. Carchon, G.J., R. Walter De, and E. Beyne, *Wafer-level packaging technology for high-Q on-chip inductors and transmission lines.* Microwave Theory and Techniques, IEEE Transactions on, 2004. **52**(4): p. 1244-1251.
37. Lee, T.H., *The design of CMOS radio-frequency integrated circuits*2004: Cambridge Univ Pr.
38. Daly, D.C. and A.P. Chandrakasan, *An energy-efficient OOK transceiver for wireless sensor networks.* Solid-State Circuits, IEEE Journal of, 2007. **42**(5): p. 1003-1011.
39. Hajimiri, A., S. Limotyrakis, and T.H. Lee, *Jitter and phase noise in ring oscillators.* Solid-State Circuits, IEEE Journal of, 1999. **34**(6): p. 790-804.
40. Otis, B., *The design and implementation of an ultra low power RF oscillator using micromachined resonators*, 2002, Master's thesis, University of California, Berkeley.
41. Razavi, B. and R. Behzad, *RF Microelectronics*. Vol. 225. 1998: Prentice Hall Upper Saddle River, NJ.
42. Proakis, J.G., *Spread Spectrum Signals for Digital Communications*2001: Wiley Online Library.
43. Allen, P.E., D.R. Holberg, and P. Allen, *CMOS Analog Circuit Design*1987: Holt, Rinehart and Winston New York.
44. Meyer, R.G., *Low-power monolithic RF peak detector analysis.* Solid-State Circuits, IEEE Journal of, 1995. **30**(1): p. 65-67.
45. Gambini, S., N. Pletcher, and J.M. Rabaey, *Sensitivity analysis for AM detectors.* EECS Department, University of California, Berkeley, Tech. Rep. UCB/EECS-2008-31, Apr, 2008.
46. Razavi, B., *Design of Analog CMOS Integrated Circuits*. Vol. 212. 2001: McGraw-Hill Singapore.
47. Abidi, A.A. and J.C. Leete, *De-embedding the noise figure of differential amplifiers.* Solid-State Circuits, IEEE Journal of, 1999. **34**(6): p. 882-885.
48. Antonini, G., A.C. Scogna, and A. Orlandi, *De-embedding procedure based on computed/measured data set for pcb structures characterization.* Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on], 2004. **27**(4): p. 597-602.
49. Belkin, S., *Spectrum Analyzer Noise De-Embedding for Accurate Measurements*, in *High Frequency Electronics*2005. p. 18-24.

50. Wang, Z., H.S. Savci, and N.S. Dogan. *1-V ultra-low-power CMOS LC VCO for UHF quadrature signal generation*. in *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*. 2006.