Threshold Voltage and Leakage Current Variability on Process Parameter in a 22nm PMOS Device

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Abstract*—This article explains the effect of variation on the process parameters while designing a Nano-scaled planar PMOS device in complementary metal-oxide-semiconductor (CMOS) technology for 22 nm gate length. This procedure aims to meet the best combination of fabrication process parameter on the threshold voltage (V_{TH}) and leakage current (I_{OFF}) which was predicted by the International Technology Roadmap for Semiconductors (ITRS). The gate structure of the PMOS device consists of Titanium Dioxide (TiO_2) as the high permittivity material (high-k) dielectric and Tungsten Silicide (WSi_x) metal gate where it is deposited on top of the TiO_2 high-k layer. The simulation process was designed using an industrial-based numerical simulator. This simulator was then aided in design with the L9 Taguchi's orthogonal array method to optimise the best combination of process parameters in order to achieve the optimum V_{TH} value with the lowest I_{OFF}. The analysis results of the factor effect on the SNR in ANOVA analysis clearly show that the Halo implantation tilting angle has the greatest influence with 52.47% in optimising the process parameter where the implantation tilting angle is at 35°. The final results in characterizing and modelling the process parameters of the 22 nm PMOS device with reference to the prediction ITRS succeeded where the result of the V_{TH} is 4.25% closest to the prediction value of -0.289 V ± 12.7% and minimum I_{OFF} value which is 92% away from the predicted value which is 100 nA/µm.

***Index Terms*—Taguchi Method; 22 nm PMOS Device; Threshold Voltage; Leakage Current.**

I. INTRODUCTION

Advent Silicon Dioxide (SiO_2) plays an important role as an effective gate dielectric from the time when Metal Oxide Semiconductor Field-Effect-Transistor (MOSFET) begins four decades ago. According to Moore's law, reduction of MOSFET geometries to increase the speed of the device at a steady power density had led to a decreasing of oxide thickness [1]. Indirectly, the reduction in SiO_2 thickness had caused severe leakage current when the scaling of MOSFET reaches into sub-100 nm. Moreover, once the scaling of SiO_2 has come into Nano-meter regimes which are lesser than 2 nm of gate oxide thickness, a major problem occurs regarding tunnelling current and oxide failure [2]. Certain researches have been done to overcome those difficulties such as introducing Nitride/Oxynitride gate stacks, but the issues still cannot be solved. Hence, high-k gate stacks were chosen as an alternative for SiO_2 since the CMOS transistor scaling ultimatums will never stop. This high-k material is the best for lower power and high-performance logic circuit. Dennard Scaling Criteria was established to simplify the scaling process by introducing the factor α which is the ratio of the target device dimension to the original one [3]. This has also been one of the major challenges for further downscaling besides the management of process variation to keep the planar CMOS devices still on track for the 20 nm node technology.

Therefore, statistical process variations on fabrication's process parameters will play a major role in future technology of scaling and has been continuing throughout semiconductor history [4]. It has been reported that the process variation such as variation that associates with the implants and anneals; pocket implants and tiling angle were ones of the subjects that play a significant role in future technology scaling. Taguchi method was used to solve the multiple process parameter optimisation problems with less number of experiments. Taguchi method used a special design of orthogonal arrays to study the process parameter variability with less number of experiments [5]. With added noise factors called signal-to-noise ratio (SNR), process parameter variability using Taguchi method becomes more reliable. In addition, the analysis of variance (ANOVA) was executed in order to identify the most significant value of the process parameters. With the combination of the SNR and ANOVA analysis, the prediction of the best combination of the PMOS's process parameters can be achieved excellently.

To date, the V_{TH} was agreed worldwide to be one of the most important parameters that affect the power consumption of a device. This parameter was acknowledged as an output that changes due to variability in semiconductor processes and largely impacts the device operation [6]. Furthermore, accurate estimation of variability in the process parameters of scaled devices is extremely important to design a perfect Nanoscale transistor with minimum I_{OFF}. There are numbers of leakage mechanisms contributing to the total leakage current in a device which depends differently on the transistor geometry such as the gate length (L_g), the oxide thickness (T_{ox}), the doping profile, and the supply voltage (V_{dd}) [7].

In this experiment, a model of 22 nm high-k/metal gate device which utilises the TiO_2/WSi_x gate structure of planar PMOS device was designed and simulated using an industrial-based simulation tool. This is the continuation of our previous work which only studies the variation effect in

leakage current [8]. Furthermore, the work in [9] studies the variability of a process parameter in finding an optimum value of threshold voltage which only considers the SNR (Nominal-the-Best, NTB) [9]. This paper, however, studies the variability of a process parameter to find the best combination to achieve the optimum threshold voltage and minimum leakage current which considers SNR (NTB) and SNR (Smaller-the-Better, STB) besides the utilisation of different process parameters. From that, we are motivated to continue our research by optimizing the process parameter variations to achieve optimum threshold voltage (V_{TH}) with minimum leakage current (I_{OFF}) on PMOS devices as predicted by ITRS for 22 nm gate length transistors where the V_{TH} value should be within -0.289 V ± 12.7% and maximum value for I_{OFF} was limited to 100 nA/µm [10].

II. EXPERIMENTAL METHODOLOGY

A. Simulation Fabrication and Device Characterization Process Using TCAD Simulation Tools

Figure 1 shows the process flow in designing and optimising the process parameter of a 22 nm PMOS planar structure model.

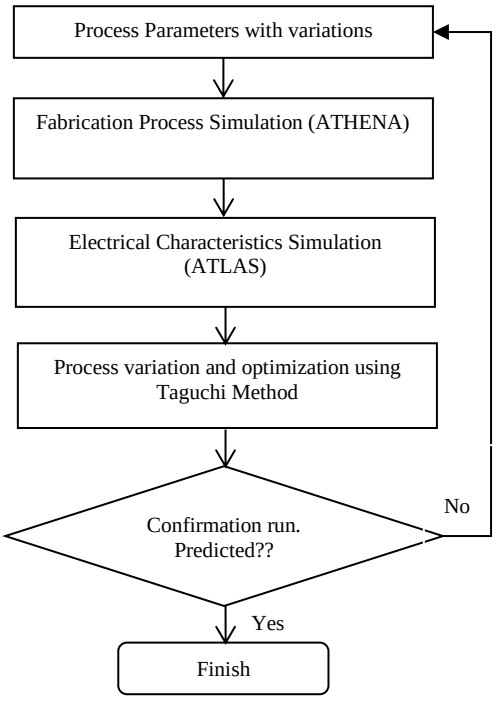

Figure 1: Flowchart of the variability process analysis

The details of virtual fabrication in designing a 22 nm PMOS planar device are summarised. The sample used in this experiment is a p-type silicon substrate with <100> orientation. N-wells are created by developing a 200Å oxide followed by phosphorus doping with a dosage of $4.5x10^{11}$ atom/cm^2 and then annealed. The Shallow Trench Isolator (STI) structure is then being produced by depositing an oxide layer with a thickness of 130 Å and a thickness of 1500 Å Nitride layer followed by the growth of a sacrificial oxide layer (PSG) with the temperature of 900 °C. The next process was to develop a layer of gate oxide with dry oxygen diffusion and annealing process with a temperature of 900 °C. Next, Boron Difluorite (BF_2) with a dosage of $1.75x10^9$ atom/cm^2 is implanted for the threshold-adjustment implantation procedure. Then the high-k layer of TiO_2 (dielectric permittivity = 80) is deposited with a thickness of 2 nm and then etched precisely to produce a 22 nm gate length. Next is the deposition of WSi_x material as the metal gate structure with a thickness of 53 nm. The Halo structure is implanted by a Phosphorus material at a doping value of $2.0x10^{10}$ atom/cm^2 with [a] tilt angle of 40 °. Then, spacers are formed followed by Source-Drain implantations, with Boron material. The next process is the PMD development with a 0.015 µm Boron-Phosphor-Silicate Glass (BPSG) layer followed by compensation implantation process. Lastly, Aluminium layer is then deposited to form the metal contacts for the Source and Drain to complete the device structure. Then the transistor undergoes an electrical characteristic measurement using ATLAS module. The complete planar structure and the doping profile of 22 nm TiO_2/WSi_x PMOS device are shown in Figure 2 and Figure 3.

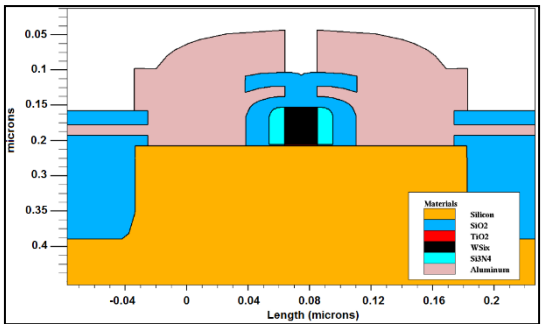

Figure 2: Completed PMOS transistor with 22 nm gate length

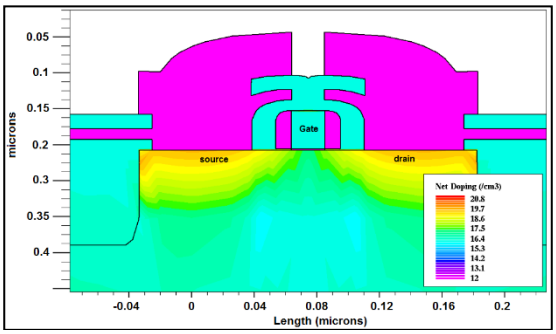

Figure 3: The doping profile of the 22 nm gate length PMOS transistor

B. Process Variation and Optimization Technique

In extension and enhancement of prior studies, this article studies the combination of two electrical characteristics. The combination of V_{TH} and I_{OFF} were studied to achieve the optimum process parameter to design the PMOS device.

The L9 orthogonal array of Taguchi method is used to study the SNR (NTB) and the SNR (STB) of ANOVA analysis to get the optimum parameter combination. There are 36 combinations of simulation runs to complete the variability process as recommended by Taguchi method which includes four main process parameters with three levels each and two noise factors with two levels each, respectively.

The process parameters that are examined are listed in Table 1. Table 2, on the other hand, shows the noise factor parameters with their levels. The reason to include the noise factors in this experiment is to get an accurate design. The simulation value of the selected process parameters is varied one by one until it is in the tolerable range predicted ITRS which is not less and more than ±12.7%. Then the minimum

and maximum results are considered as level 1 and level 3 respectively while level 2 as a middle value resulted from simulation result. Next, the Taguchi method was utilised with an orthogonal array to get the optimum parameter.

Table 1
Process Parameters

Factor	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implantation dose	Atom/cm^2	1.5 x10^{10}	2.0 x10^{10}	2.5 x10^{10}
B	Halo Implantation tilting angle	Degree	35	40	45
C	Gate Oxide growth annealing temperature	℃	890	900	910
D	Metal gate annealing temperature	℃	840	850	860

Table 2
Noise Factors

Symbol	Noise Factor	Level 1	Level 2
		℃	
X	Sacrificial Oxide Layer	900 (X_1)	905 (X_2)
Y	BPSG	800 (Y_1)	805 (Y_2)

III. Result Analysis And Discussion

A. Electrical Characteristic on V_{TH} and I_{OFF}

The L9 Taguchi method analysis for V_{TH} and I_{OFF} in this experiment consist of a total 36 running simulations. The completed simulation results for both V_{TH} and I_{OFF} are shown in Table 3 and Table 4 respectively.

Table 3
V_{TH} Simulation Results for PMOS Device

Exp. No	V_{TH} (V)			
	X1Y1	X1Y1	X1Y1	X1Y1
1	- 0.28584	- 0.28584	- 0.28584	- 0.28584
2	- 0.28014	- 0.28014	- 0.28014	- 0.28014
3	- 0.26301	- 0.26301	- 0.26301	- 0.26301
4	- 0.29200	- 0.29200	- 0.29200	- 0.29200
5	- 0.27862	- 0.27862	- 0.27862	- 0.27862
6	- 0.27694	- 0.27694	- 0.27694	- 0.27694
7	- 0.29248	- 0.29248	- 0.29248	- 0.29248
8	- 0.28910	- 0.28910	- 0.28910	- 0.28910
9	- 0.28455	- 0.28455	- 0.28455	- 0.28455

Table 4
I_{OFF} Simulation Results for PMOS Device

Exp. No	I_{OFF} (nA/μm)			
	X1Y1	X1Y2	X2Y1	X2Y2
1	11.6579	12.3213	11.6526	12.3157
2	13.2732	14.0396	13.2672	14.0333
3	19.5786	20.7195	19.5704	20.7109
4	10.0462	10.6726	10.0417	10.6679
5	13.6378	14.3949	13.6317	14.3885
6	14.4003	15.2370	14.3939	15.2303
7	9.83749	10.4297	9.83282	10.4248
8	10.8553	11.5370	10.8506	11.5320
9	11.9361	12.6022	11.9304	12.5963

B. Process Variations Analysis to Obtain Optimum Result

After the simulation experiments were completed, the next step is to analyse the process parameter that gives the most contribution to the device characteristics. One of the processes is to determine the SNR analysis. In the SNR analysis, the V_{TH} characteristic was referred to the SNR (NTB) where the aim of the analysis is to achieve the final result value as close to or same as the targeted value. In this case, the target value for V_{TH} is 0.289 V. While for the I_{OFF} characteristic, the SNR (STB) will be used where it means to achieve the minimum leakage current and the best device was 100% performed with zero leakage. However, on a real device, that is impossible to achieve zero leakage. Therefore, there has a limitation value for the working device where the maximum accepted of I_{OFF} values was 100 nA/μm.

For V_{TH}, the SNR (NTB), η_{NTB} can be expressed as [11].

$$\eta_{NTB} = 10Log_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

where: μ_{NTB} = the mean and σ_{NTB} = the variance.

While for I_{OFF}, the SNR (STB), η_{STB} can be expressed as [11]:

$$\eta_{STB} = -10\log_{10}\left(\frac{1}{n}\sum_{i=1}^{n} y_i^2\right) \quad (2)$$

where: n = number of tests and Y_i = the experimental value.

By applying the formula given in Equation (1) and Equation (2), the η_{STB} and η_{NTB} were calculated and tabulated in Table 5 and Table 6 respectively.

Once the type of analysis for V_{TH} and I_{OFF} are identified, the first condition is to determine the highest Signal-to-Noise Ratio (SNR) values for each level of the process parameter based on simulation results. From that, the highest SNR value for each process parameter level can be compared and will be selected as the possible level to achieve the optimum result. Analyzing the factor effect percentage on SNR is important as it indicates the priority of a process parameter to reduce the variation. A larger SNR value indicates better characteristic quality plus shows a greater influence on the device performance.

The second condition was to determine the dominant factor in the analysis of variance (ANOVA) results. In ANOVA analysis, the highest percentage of factor effect on variance shows that the factor is a dominant factor and the factor normally will give better influence to the process variation. Thus, the variability process on the dominant factor must not be neglected.

Finally, once the selection of the level of the process parameters has been decided, the level from the analysis will be then simulated again to achieve the optimal design.

Data from Table 5 and Table 6 will be used to compare the highest level for each process parameter, and by referring to Table 7, the highest percentage will be selected as the best level for final simulation parameter in order to achieve the optimum result.

Based on Table 5 and Table 6, Factor A which is Halo implantation dose shows that the highest SNR (NTB) is at level 3 with the value of 47.01 dB which is the same for SNR (STB) with the value of 159.04 dB. This indicates that the best level for Factor A is level 3. While for Factor B which is Halo implantation tilting angle shows that the highest level for both SNR (NTB) and SNR (STB) is at level 1 with the value of 47.06 dB and 159.33 dB respectively. Therefore, the

best level for Factor B is at level 1. It is the same for Factor C where both SNR (NTB) and SNR (STB) indicates that level 2 is the highest value. There is some conflict when comes to Factor D (Metal gate annealing temperature) where the SNR (NTB) shows that level 2 with a value of 46.79 dB is the highest level while SNR (STB) for Factor D shows that level 2 is the highest level with 157.92 dB.

In this issue, Table 7 will be used to indicate the highest percentage for both factor effect to be selected as the best level. By referring to Table 7, the percentage of Factor D for SNR (NTB) is higher than that SNR (STB) with a value of 52.22% compared to 1.01% for SNR (STB). Hence, the level for SNR (NTB) will be selected, which is level 2. Therefore, the best setting is A_3 B_1 C_2 D_1. The best setting of control factor values is summarised in Table 8. These final levels for each process parameter were then simulated with respect to noise factors to get the optimal result of V_{TH} and I_{OFF} as tabulated in Table 9.

Besides that, by referring to Table 7, the highest percentage of factor effect indicates that process parameter gives the most influence to device characteristic. Which in this case, Factor B which is Halo implantation tilting angle gives the most influence to the device characteristics with 52.47%. It was an agreement with studies from other researchers whose shows that the variability of the Halo profiles results in a better device performance where the best parameter for the Halo implantation tilting angle was between 25° to 35° [12]

Finally, the combination levels of A_3 B_1 C_2 D_1 X_1 Y_2 show the best combination where the V_{TH} value of 0.30129 V results as the closest value to the ITRS prediction by 4.25% (ITRS range: ±12.7%), and at the same time, I_{OFF} results with almost 92% away and lower than the maximum value as predicted by the ITRS which is 100 nA/µm. Well said, both values are in line with the ITRS predictions. As a result, Taguchi method is proven to be a capable method to predict the optimum solution in obtaining the optimal fabrication recipe for a 22 nm TiO_2/WSi_x planar PMOS.

Table 5
SNR (NTB) Results for V_{TH}

Factor	SNR NTB (Mean), dB		
	Level 1	Level 2	Level 3
A	46.53	46.76	47.01
B	47.06	46.77	46.47
C	46.72	46.95	46.62
D	47.18	46.79	46.32

Table 6
SNR (STB) Results for I_{OFF}

Factor	SNR STB (Mean), dB		
	Level 1	Level 2	Level 3
A	156.54	157.78	159.04
B	159.33	157.79	156.24
C	158.01	158.40	156.95
D	157.90	157.92	157.54

Table 7
Result of ANOVA

Factor	Factor Effect (NTB) (%)	Factor Effect (STB) (%)
A	15.97	34.23
B	24.03	52.47
C	7.78	12.29
D	52.22	1.01

Table 8
Optimum Setting of the Process Parameters

Factor	Process Parameter	Level	Best Value
A	Halo Implantation dose	3	2.50×10^{10}
B	Halo Implantation tilting angle	1	35°
C	Gate Oxide growth annealing temperature	2	900 °C
D	Metal gate annealing temperature	1	840 °C

Table 9
Results of Optimum Setting Parameter with Added Noise

Noise (°C)	V_{th} (V)	I_{leak} (nA/µm)
(X_1,Y_1)	0.30356	7.54604
(X_1,Y_2)	0.30129	7.98981
(X_2,Y_1)	0.30358	7.54226
(X_2,Y_2)	0.30131	7.98583

IV. CONCLUSION

As a conclusion, optimising the process parameters of a 22 nm TiO_2/WSi_x PMOS planar structure device with the nominal value of V_{TH} and at the same time achieving the lowest I_{OFF} recommended by the Taguchi method complies with the ITRS projection was successfully achieved. It has been shown that the variability of process parameters has a significant impact on the device characteristics. In this experiment, it was proven that the Halo implantation tilting angle with an angle of 35 ° resulted in the dominant factor with an influence of 52.47%.

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