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Design and implementation of 9-Level Trinity DC Source inverter using Embedded Controller

R.Sreenivasan, V.Jayakumar
Assistant Professor, M. Kumarasamy College of Engineering, Karur, India.
srini.vasan256@gmail.com
Assistant Professor, M. Kumarasamy College of Engineering, Karur, India
jk2020jv@gmail.com

ABSTRACT

Trinary DC source cascaded H-bridge multilevel inverter and the switching pattern scheme is used to improve the performance of Multilevel Inverter (MLI) which reduces the switching losses. The proposed MLI can synthesize high quality output voltage near to sinusoidal waves. This scheme significantly reduces the Total Harmonic Distortion (THD) and switching losses. The circuit configuration is simple and easy to control. For the developed technique simulations are carried out through MATLAB/SIMULINK

Indexing terms/Keywords

Multilevel Inverter, Trinary DC Source, Embedded controller

I. INTRODUCTION

Now a days multilevel inverters are widely used in power systems. Improved harmonic characteristics and ability to handle high voltage and high power are the major factors for developing such type of inverters. Also multilevel inverters have low switching stresses and high flexibility. There are several topologies which are diode-clamped, flying-capacitor and cascaded H-bridge cell [1]-[5]. Among them cascaded H-bridge multilevel inverters are used due to merits such as minimum number of components, reliability and modularity so that switching losses are reduced. In the point of obtaining a sinusoidal output voltage wave multilevel inverters may increase the number of output voltage levels. However it will need more components which results in complexity and increase in cost. To minimize these drawbacks multilevel inverters employing cascaded transformers have been studied [6]-[8]. Owing to the Trinary characteristic of output voltage they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer galvanic isolation between source and loads are obtained. However the transformer may decrease the power conversion efficiency, as well as the volume and cost will be increased. To alleviate these problems we propose a cascaded H-bridge multilevel inverter using Trinary DC input source without transformers [6] where the circuit topology is simple and easy to control .This paper presents a single phase Trinary DC source nine level inverter topology for investigation with embedded controller switching technique. Simulations are performed using MATLAB-SIMULINK.

II. BASIC OPERATION OF MULTILEVEL INVERTER

Fig. 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing Trinary DC source. The input voltage of a first bridge source will be three times that of the second bridge source. By using Vdc and 3Vdc which can produce nine output voltage levels such as: -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc. The lower inverter generates a fundamental output voltage with three levels and the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. . Here the final output voltage levels becomes the sum of each terminal voltage of H-bridge and it is given as

$$V_{OUT} = V_{HB1} + V_{HB2}$$

In the proposed circuit topology if *n* number of H-bridge module has independent DC sources in sequence of the power of 3 then the expected output voltage level is given as

$$V_n = 3^n, \text{ where } n=1, 2, 3\ldots$$

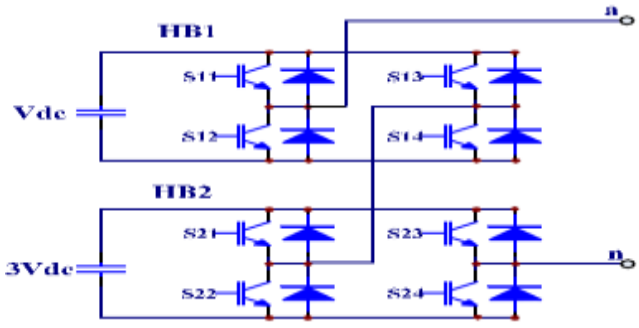

Fig1.Trinary Source MLI

III. STAGES OF OPERATION

STAGE 1: FOR 4VDC

SWITCHES ON: S11, S14, S21, S24 and the remaining switches are in off condition which produces 4Vdc.

STAGE 2: FOR 3VDC

SWITCHES ON: S12, S14, S21, S24 and the remaining switches are in off condition which produces 3Vdc.

STAGE 3: FOR 2VDC

SWITCHES ON: S12, S13, S21, S24 and the remaining switches are in off condition which produces 2Vdc.

STAGE 4: FOR 1VDC

SWITCHES ON: S11, S14, S22, S24 and the remaining switches are in off condition which produces 1Vdc.

STAGE 5: FOR 0VDC

SWITCHES ON: S12, S14, S22, S24 and the remaining switches are in off condition which produces 0Vdc.

STAGE 6: FOR -1VDC

SWITCHES ON: S12, S13, S22, S24 and the remaining switches are in off condition which produces -1Vdc.

STAGE 7: FOR -2VDC

SWITCHES ON: S11, S14, S22, S23 and the remaining switches are in off condition which produces -2Vdc.

STAGE 8: FOR -3VDC

SWITCHES ON: S12, S14, S22, S23 and the remaining switches are in off condition which produces -3Vdc.

STAGE 9: FOR -4VDC

SWITCHES ON: S12, S13, S22, S23 and the remaining switches are in off condition which produces -4Vdc.

TABLE 1 SWITCHING SEQUENCE OF TRINARY MULTI LEVEL INVERTER

V_{out}	S11	S12	S13	S14	S21	S22	S23	S24
4Vdc	1	0	0	1	1	0	0	1
3Vdc	0	1	0	1	1	0	0	1
2Vdc	0	1	1	0	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2Vdc	1	0	0	1	0	1	1	0
-3Vdc	0	1	0	1	0	1	1	0
-4Vdc	0	1	1	0	0	1	1	0

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IV. TRINITY DC SOURCCE

Fig1 shows a trinary dc source which contains cascaded H-bridge of two bridges (HB1 and HB2) having 1Vdc for first bridge and the second bridge is 3Vdc.

The value of the voltage source of first bridge will be three times that of the second bridge to produce nine level inverter output.

If the values of the voltage source in both the bridges are the same then it will produce 5-level inverter.

If the value of the voltage source in first bridge will be twice that of the second bridge then it will produce 7-level inverter.

It is compared with the conventional multilevel inverters i.e., diode-clamped, flying capacitor, cascaded H-bridge and cascaded transformer based multilevel

V. SWITCHING SIGNAL GENERATION

Switching signal generation for proposed multilevel inverter is generated using embedded controller. Fig2-9 shows the gating pattern generated using embedded controller

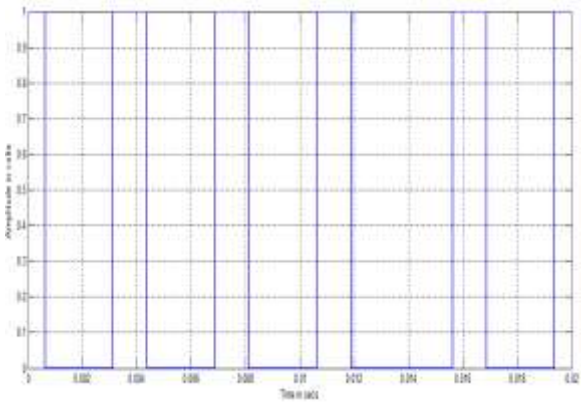

Fig2. Gating pattern of Switch S11

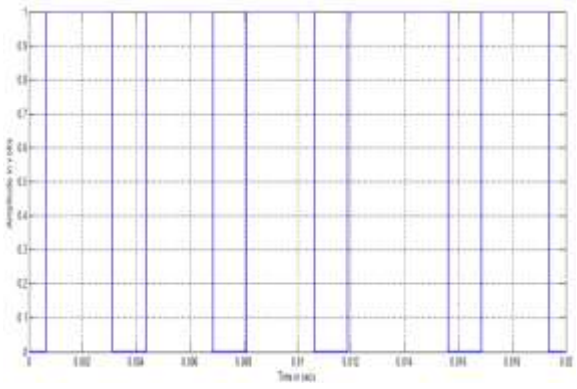

Fig3. Gating pattern of Switch S12

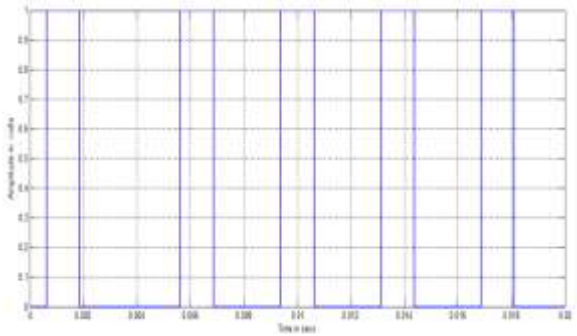

Fig4. Gating pattern of Switch S13

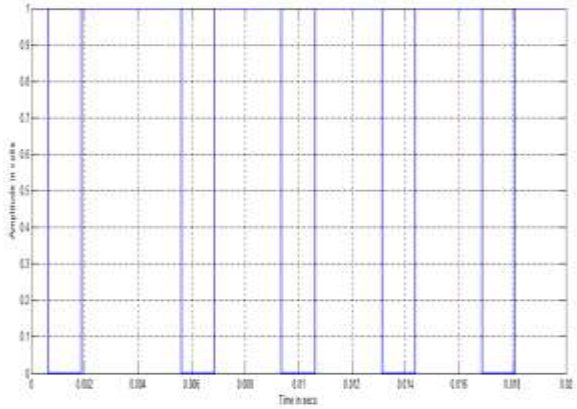

Fig5. Gating pattern of Switch S14

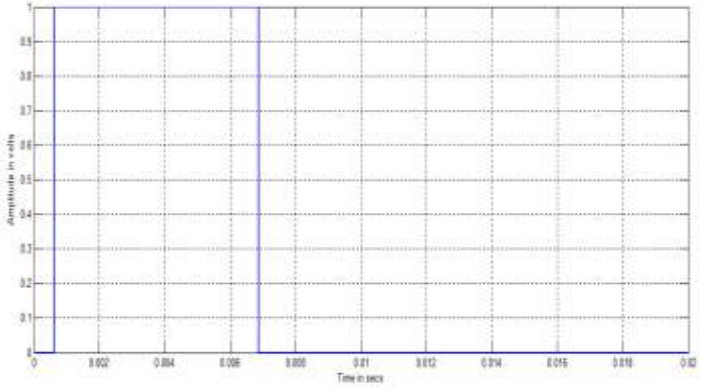

Fig6. Gating pattern of Switch S21

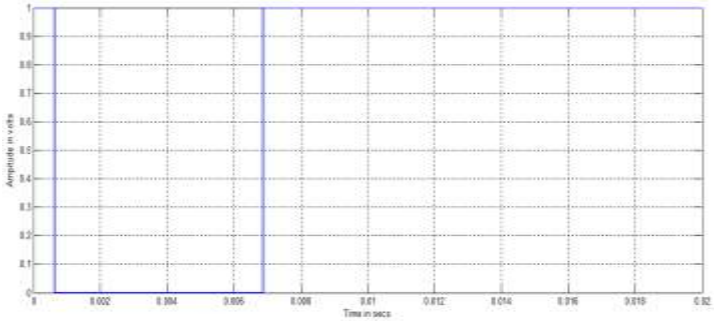

Fig7. Gating pattern of Switch S22

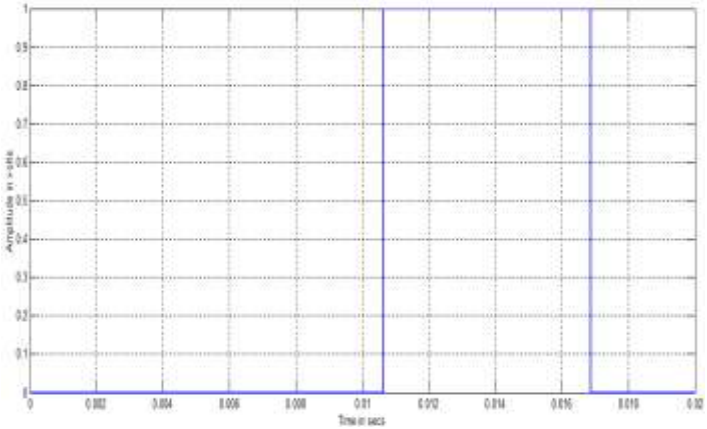

Fig8. Gating pattern of Switch S23

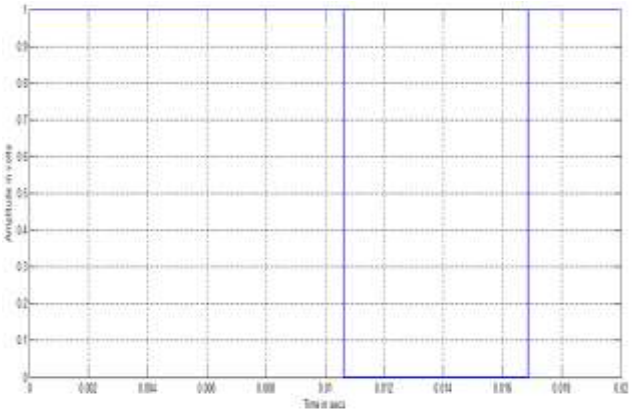

Fig9. Gating pattern of Switch S24

VI. SIMULATIONS AND RESULTS

The simulations are implemented using Mat Lab. We can notice that the lower inverter generates a fundamental output voltage of three levels and the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Fig13 shows the FFT plot for nine level inverter. The final output voltage becomes the sum of terminal voltage of H-bridge modules. The following parameter values are used for simulation: Vdc =25V, R (load) = 100 Ω.

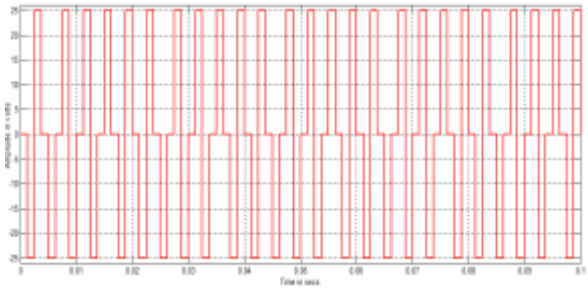

Fig10. UPPER INVERTER TERMINAL VOLTAGE

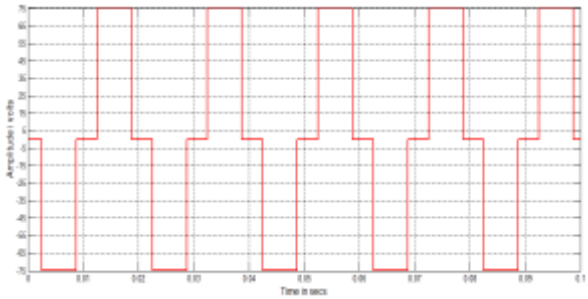

Fig11. LOWER INVERTER TERMINAL VOLTAGE

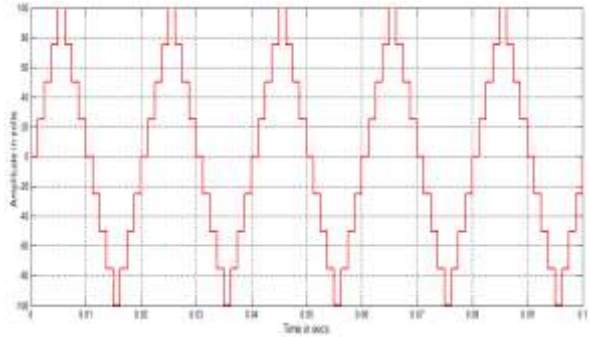

Fig12. NINE LEVEL OUTPUT VOLTAGE OF TRINARY MULTI LEVEL INVERTER

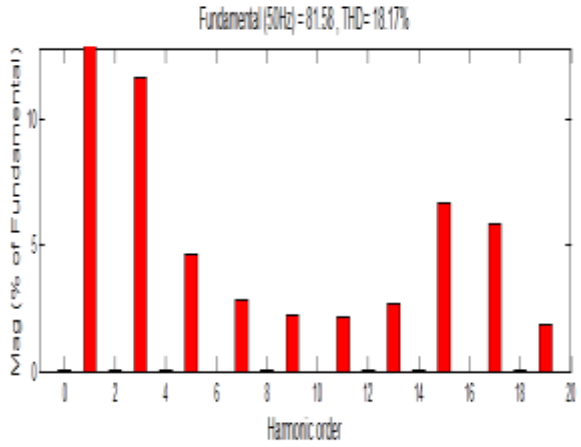

Fig13. FFT PLOT FOR NINE LEVEL OUTPUT VOLTAGES

VII. CONCLUSIONS

Thus it is proposed that cascaded H-bridge multilevel inverter employing Trinary DC sources will obtain a large number of output voltage levels with minimum devices and synthesize high quality output voltage near to sinusoidal waves. Also in this paper embedded switching scheme is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches and switching losses. It is observed that proposed topology produce THD of 18.17% which eliminates the complexity of generating gate signals when the stages are added. Valuable and presentable merits of the proposed approach are summarized as

(1) Economical circuit configuration to produce multilevel outputs by using Trinary input sources.
(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic
(3) Little transition loss of switches due to
low switching frequency and reduced EMI which is suitable for high voltage applications.

VIII. REFERENCES

[1].L. G. Franquelo, J. Rodriguez, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converter arrives," *IEEE Ind. Electron. Magazine*, pp. 28-39, 2008.

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel Inverters: A survey of topologies, controls, and applications*," IEEE Trans. Ind. Electron*., vol. 49, no. 4, pp. 724-738, Aug. 2002.

[3] J. S. Lai, and F. Z. Peng, "Multilevel Converters-A New Breed of Power Converters," *IEEE Trans. Ind. Appl.,* vol. 32, no. 3, pp. 509-517,May/June, 1996.

[4] M. H. Rashid, Power Electronics Handbook, Academic Press, 2001, pp.539-562.

[5] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Electron.,* vol.35, pp.36-44, 1999.

[6] F. S. Kang, S. J. Park, M. H. Lee, C. U. Kim, "An efficient multilevel synthesis approach and its application to a 27-level inverter," *IEEE Trans. Ind. Electron*., vol. 52, no. 6, pp. 1600-1606, 2005.

[7] F. S. Kang, S. J. Park, C. U. Kim, T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power system," *IEEE Trans. Energy Conversion*, vol. 20, no. 4, pp. 906-915, 2005.

[8] "An efficient multilevel inverter system for reducing THD with Space Vector Modulation"

R Karthikeyan, SC Pandian

International Journal of Computer Applications 23 (2), 0975-8887

[9]"Generalized Space Vector PWM algorithm for minimizing THD in hybrid Multilevel Inverters" R Karthikeyan, SC Pandian

[10] "Generalized space vector modulation schemes for cascaded multilevel inverter to reduce harmonic distortion"

r karthikeyan anna university

[11]"Reduction of Components in New Family of Diode Clamp Multilevel Inverter Ordeal to Induction Motor" RK Rathinam Angamuthu, Karthikeyan Thangavelu JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE 16 (ISSN(Online) 2233-4866

[12] "Harmonic reduction using sinusoidal pulse width modulation based flying capacitor multilevel inverterimplemented to induction motor" KT Angamuthu Rathinam

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Author' biography with Photo

R.Sreenivasan received his Under Graduated in Electrical and Electronics Engineering at Thangavelu Engineering College, Chennai and completed his Post Graduated in Power Electronics and Drives in Thangavelu Engineering College, Chennai . He has two years of Teaching experience and currently working as Assistant Professor in M.Kumarasamy College of Engineering, Karur. His area's of interest are Muliti Level Inverter, AC Machines, PLC and Control of Electrical Machines.

V.Jayakumar received his Under Graduated in Electrical and Electronics Engineering at Thiagarajar College of Engineering, Madurai, Tamilnadu. He received PG degree from Anna university,Chennai, Tamilnadu. He has two years of Industrial experience and Eight years of Teaching experience and currently working as Assistant Professor in M.Kumarasamy College of Engineering, Karur, Tamilnadu. His area's of interest are Muliti Level Inverter & Converter, AC Machines, Circuit Theory and PLC.