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Bridgeless SEPIC Converter Based Computer Power Supply Using Coupled Inductor

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ABSTRACT

Switched Mode Power Supplies (SMPS) are used as power source for computers. Conventional SMPS used in computers are suffered by some serious problems such as poor power quality, high device stress, slow dynamic response, high harmonic contents, periodically dense, peak currents, distorted input current. To minimize these problems, a non-isolated bridgeless buck-boost single ended primary inductance converter (SEPIC) using coupled inductor is introduced at the front end of the SMPS, which is operated in discontinuous conduction mode (DCM). This proposed technique reduces the Total Harmonic Distortion(THD), which results in power factor improvement. The DC output voltage of the SMPS is almost a constant voltage which is regulated by means of the proposed SEPIC converter. For obtaining different dc voltage levels for the PC applications, the output of the front end SEPIC converter is fed to the half-bridge DC-DC converter. The output voltages of the SMPS are controlled by controlling any one of the output voltages. Design and simulation of the proposed converter are carried out using the MATLAB/simulink software.

Keywords

Bridgeless converters; PFC; computer power supply; power quality; total harmonic distortion

Academic Discipline And Sub-Disciplines

Electrical and Electronics engineering; Power electronics and drives

INTRODUCTION

The classical method of ac-dc rectification having a diode bridge rectifier (DBR) followed by the large electrolytic capacitor is used in many electronic applications. The harmonic rich current drawn from the utility due to the uncontrolled charging and discharging of the capacitor goes against the international power quality standards [4-5]. The most commonly affected electronic equipment by the power quality problem is the personal computer (PC). To maintain the harmonics within the limits and also to obtain regulated multiple outputs single stage and two stage conversions of ac voltage into dc voltage have been used in computers. However the single stage power conversion is simple, cost-effective and compact, it suffers from poor dynamic response, complexity in control, large value of capacitance and the component stress is high. So, we go for two stage conversion of ac voltage into multiple dc voltage in computers [6]. Compared to the single stage conversion the number of components used in two stage is much higher. But ,it has fast dynamic response ,provides better regulation in output voltage and blocks the second harmonics(100Hz or 120 Hz) in the first stage itself , so the use of large capacitors are avoided.

For providing PFC in power supplies a boost converter is mostly used. As the input voltage range required is large it is not preferred. For an input supply of 220V, the boost converter cannot control the voltage less than 300V. So, in PCs where wide variations in input voltage and load are expected a buck-boost converter is preferred [7-8]. As the computer power supply is connected to various ICs low output voltage ripple is preferred. Single stage power supplies where power quality improvement and voltage regulation takes place in a single stage are used in many applications. However, in computers, at varying loads the single stage conversion increases the switching stress and reduces the voltage regulation. Hence, to improve the input power quality and regulation in output voltage, we go for two stage conversion. But, the efficiency of the conventional SMPS is higher than the two stage SMPS [9]. To overcome this disadvantage, a new bridgeless front end converter for computer power supplies is proposed. A bridgeless SEPIC converter using coupled inductor is used as the front end converter. A key advantage of using coupled inductor is that the regulator's ripple current is divided between the coupled inductors allowing the value to be halved. The inductive reactance is also reduced which leads to low power dissipation in the form of heat. This design leads to the smaller input capacitor and simple EMI filter. Also, the coupled inductor design provides better feedback control than the uncoupled inductors. A half bridge converter providing isolation, regulation and multiple dc outputs [10-11] is connected at the output of the front end converter.

Previously, a power quality improved bridgeless converter based computer power supply was proposed which uses single inductors having high THD value and low power factor. In this paper, we have proposed a new design which employs coupled inductor instead of single inductors in bridgeless SEPIC converter, operating in discontinuous conduction mode (DCM) which results in the cancellation of current ripple[12] is used at the front end of the SMPS. This reduces the Total Harmonic Distortion and improves the power factor of the converter. The isolated converter is connected to the output of the bridgeless PFC converter. The simulated performance of the proposed multiple-output SMPS with reduced harmonics and improved power quality is provided in the test results.

SYSTEM CONFIGURATION

The proposed technique consists of two parts, bridgeless front end ac-dc converter and multi-output isolated dc-dc converter. Based on the requirement of the user the continuous conduction mode (CCM) or the discontinuous conduction mode (DCM) of the bridgeless front end converter is selected. If cost is the major consideration, DCM is selected; if not CCM is preferred. CCM reduces the device stress, but it requires two voltage and one current sensor which makes it costlier. Therefore, a DCM operation where only one voltage sensor is needed for both sensing and control, is preferred at the front end PFC converter. Hence, for achieving inherent PFC the front end converter is designed in DCM, whereas CCM for the isolated converter. For both converters the control loops are independent of each other. The system configuration of the SMPS is described below.

Bridgeless Sepic Converter Using Coupled Inductor

The design of the proposed power supply is shown in the Fig 1. In this proposed technique coupled inductors are used instead of the single inductors at the input side of the Power Factor Correction (PFC) converter. By using two SEPICs at the input side ,Diode Bridge Rectifier (DBR) is eliminated. The SEPIC converters designed with the coupled inductors are free from leakage inductance, in which the AC current losses are reduced. For positive half cycle, the upper converter operates and the lower converter operates for the negative half cycle of the input ac voltage. For the efficient control of both the converters the switching frequency is set to 20KHz. For reducing the complexity in control, the design of the output inductors is carried out in DCM for both the converters. The wide variations in the input voltage and the load is taken care by the regulation of the output voltage. The voltage error (V_{ePFC}) is obtained by comparing the output dc voltage (V_{PFC}) and the reference voltage (V_{PFCref}) which is given to the proportional and the integral controller.

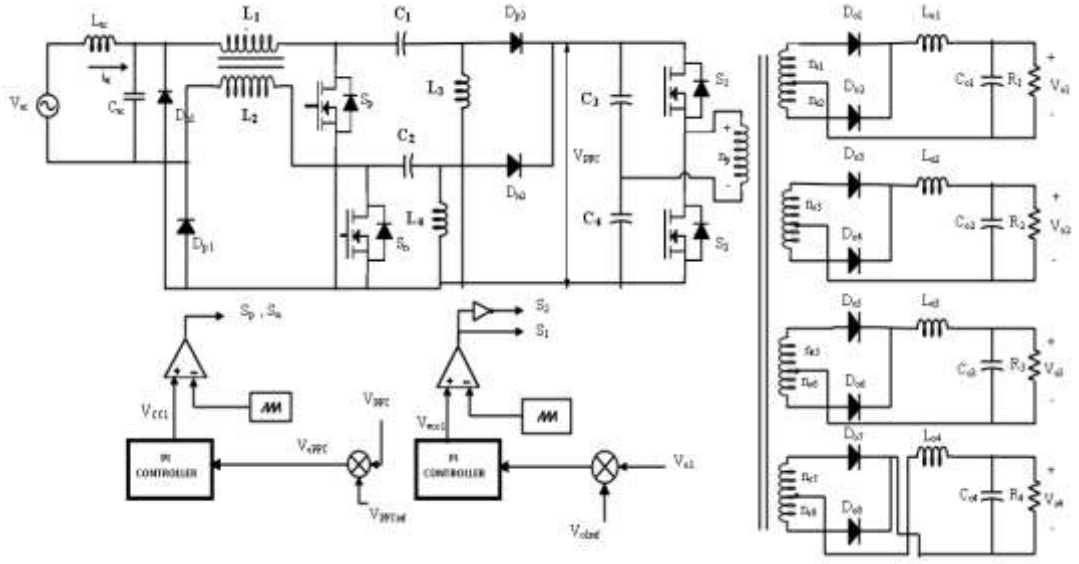

Fig 1:Schematic diagram of bridgeless converter using coupled inductor

To generate the PWM pulses that are given to both the switches the PI controller output (V_{cc1}) is compared with a high frequency saw-tooth 1 wave. If $S_t<V_{cc1}$ and V_{ac} is positive, then S_p is turned on, or else it stays off. The switching signals for the bridgeless ac-dc converter is represented by S_t. According to the output of the PI voltage controller-1 the width of the PWM pulses vary, so that the dc output voltage V_{PFC} is effectively regulated, and to obtain the multiple isolated regulated voltage at the output, it is fed to the isolated half bridge converter in the second stage. To maintain the dc output voltage V_{PFC} constant, the width of the PWM pulses changes accordingly. The multi-winding high frequency transformer (HFC) is used for isolation. To reduce the conduction losses a centre tapped configuration is chosen at the output side. One control loop is used to control all the secondary windings. For the selection of voltage sensing, the highest rated secondary winding is used. The PI controller-2 is fed by the difference between the output voltage (V_{01}) and the reference voltage (V_{01ref}) and its output is compared with another high frequency saw-tooth wave-2, which generates the second set of PWM pulses for the half-bridge converter switches S_1 and S_2. To avoid the shoot-through fault care should be taken to provide sufficient dead-time between turning OFF of S_1 and turning ON of S_2. The stress will be reduced if the isolated converter is operated in CCM. The duty cycle changes accordingly, if the load changes in any of the winding, to provide the regulated output dc voltage. The response is slower for the other outputs then the one whose voltage is sensed.

Bridgeless Sepic Converter Using Two Coupled Inductor

The configuration of the modified bridgeless SEPIC converter is same as the proposed technique in which the two input single inductors are replaced by the coupled inductor is shown in fig 2. Here the coupled inductors are in the form of series connection. If the coupled inductors are used, the ripple current is divided between the inductors, so the inductance value required is halved. So, the design of the EMI filter is simple and the

input capacitor is small. This modified configuration will leads to further reduction in Total Harmonic Distortion (THD).

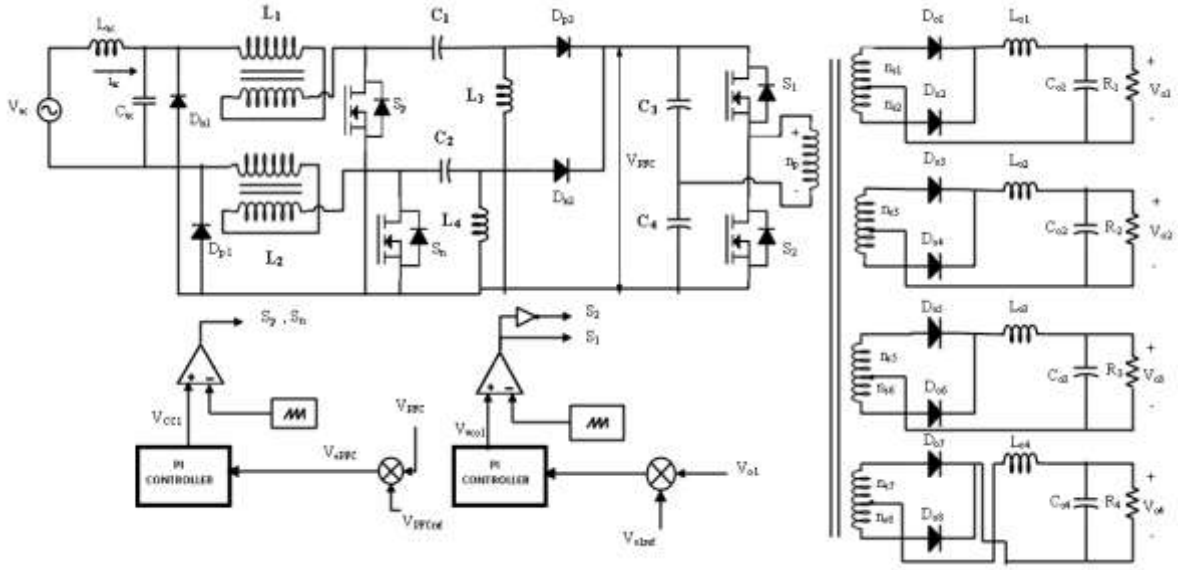

Fig 2: Schematic diagram of bridgeless converter using two coupled inductors

OPERATING PRINCIPLE

The operating principle of the front end converter and the isolated converters are described below.

Operating Principle Of Front End Converter

The upper SEPIC converter operates during the positive half cycle of the input voltage as shown in the Fig.3. In the same way, the lower SEPIC operates during the negative half way. The operation of the converter for PWM cycle is described in the following modes.

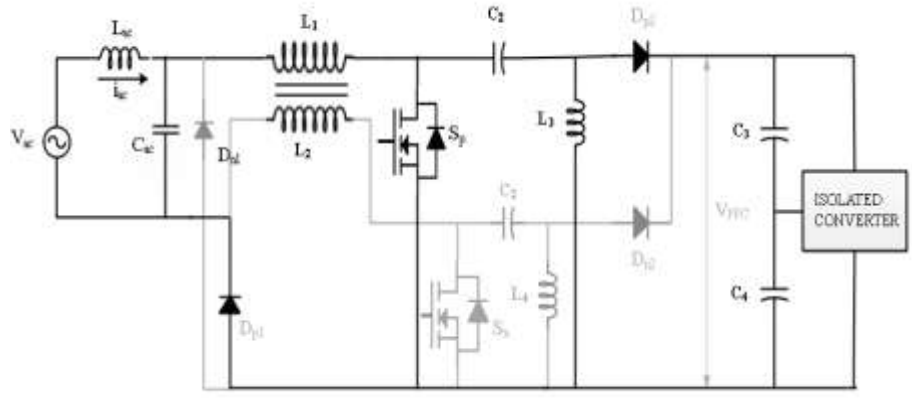

Fig 3: Operation of PFC converter when input voltage is positive

In the first mode, when S_p turns on, the inductor L_{p1} starts storing energy, transferred from the ac mains as shown in the Fig 4. The current path is completed by the diode D_{p1}.

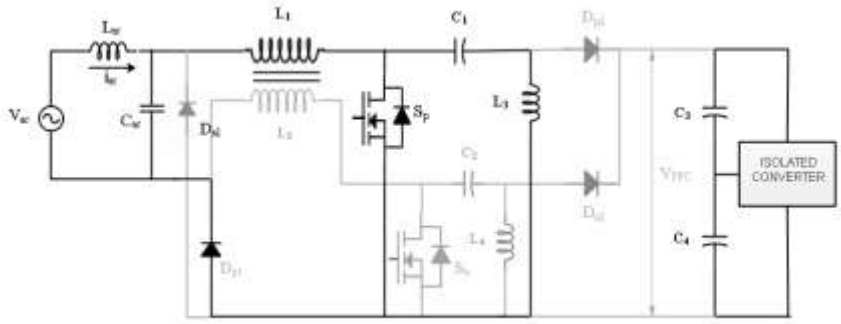

Fig 4: Operation of PFC converter during mode I

In the second mode, S_P is turned off and the diode D_{p2} starts conducting. The output inductor L_{p2} starts discharging to zero as shown in Fig 5

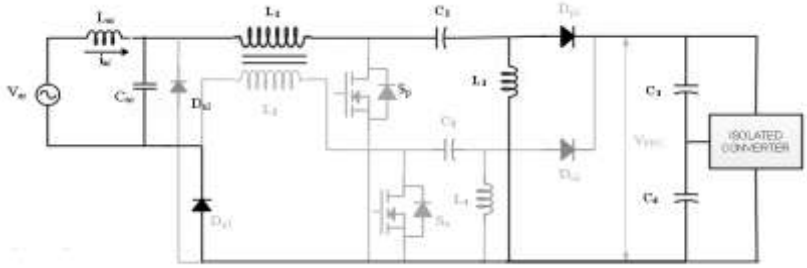

Fig 5: Operation of PFC converter during mode II

Until the next switching cycle, the current in the inductor remains zero. This mode makes sure the DCM operation as shown in the Fig 6.

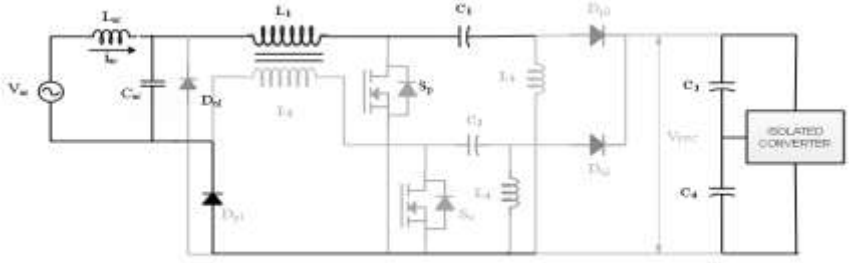

Fig 6: Operation of PFC converter during mode III

Operating Principle of the Isolated Converter

In one switching cycle two high frequency switches are turned on and off. So, the operation of the converter is same in both the half cycles. The switch S_1 is turned on during the first half cycle. On the secondary side, diodes (D_{01}, D_{03}, D_{05} and D_{07}) starts conducting and the energy gets stored in the inductors (L_{01}-L_{04}) in all the secondary winding. When the maximum value is reached by the inductor current, the switch S_1 is turned off. To maintain the constant output dc voltage, all the capacitors in the filters discharge through the load. The upper switch is turned off for the next half cycle. The inductor currents are free-wheeled through the secondary diodes (D_{01}-D_{08}). The net voltage across the HFT becomes zero, as the core flux is cancelled by the current in all secondary windings. In the next half cycle, the same inductor gets charged and discharged with the lower switches S_2.The operating principle of the front end converter and the isolated converter is same for both the proposed bridgeless SEPIC converter using coupled inductor.

DESIGN OF THE PROPOSED BRIDGELESS SEPIC CONVERTER BASED COMPUTER POWER SUPPLY

The design of the proposed bridgeless SEPIC converter using coupled inductor is described below:

Design Of The Proposed Smps System

The design for both positive and negative half cycle operated PFC is same. The average voltage V_{avg} is calculated as,

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$$V_{avg} = \frac{2\sqrt{2}V_{ac}}{\pi} = \frac{2\sqrt{2} \times 220V}{3.14} = 198V \quad (1)$$

The duty cycle D of the PFC SEPIC converter is expressed as the ratio of output dc voltage to the sum of output voltage and the input voltage.

$$D = \frac{V_{PFC}}{V_{PFC} + V_{avg}} = \frac{300V}{300V + 198V} = 0.6 \quad (2)$$

Irrespective of the input voltage variation ,the output voltage is maintained constant at 300V. The duty cycle for the supply voltages are calculated as, D_{170}=0.63, D_{220}=0.58, D_{270}=0.52 . During the DCM operation, the duty cycle of the converter is considered less than D_{270} for the efficient control.

The input inductor value is calculated for the ripple in 40% of input current.

Assume D=0.25

$$L_1 = \frac{DV_{avg}}{f \times (i_{ripple})} = \frac{0.25 \times 198V}{20KHz \times 0.58A} = 4.35mH \quad (3)$$

Where, f is the frequency .

To make sure the DCM operation, in all operating conditions the output inductor is selected as 100μH.

The capacitor value is calculated as,

$$C_1 = \frac{1}{\omega_r(L_1 + L_2)} = \frac{1}{2 \times \pi \times 20000Hz(4.35mH + 100\mu H)} = 1.78mF \quad (4)$$

Where, ω_r is the angular frequency (ω_r=2πf_r).

To reduce the higher order harmonics an L-C filter is used at the input side [22].

The calculation for the inductance of the secondary winding is,

$$L_{01} = \frac{V_{01}(0.5 - D_s)}{f_s \Delta i_{L01}} = \frac{12V(0.5 - 0.4)}{60KHz \times 0.625A} = 0.032mH \quad (5)$$

Similarly, the inductances for the other secondary windings are 9.5μH, 6.8μH, and 1.5μH.

SIMULATION CIRCUIT OF BRIDGELESS SEPIC CONVERTER USING COUPLED INDUCTOR

The simulation circuit of the bridgeless SEPIC converter using coupled inductor is shown in the fig 7. The simulated performance for both the proposed techniques are carried out using the MATLAB/SIMULINK software. The response of the simulation are shown in fig 8,fig 9, fig 10 and fig 11 respectively.

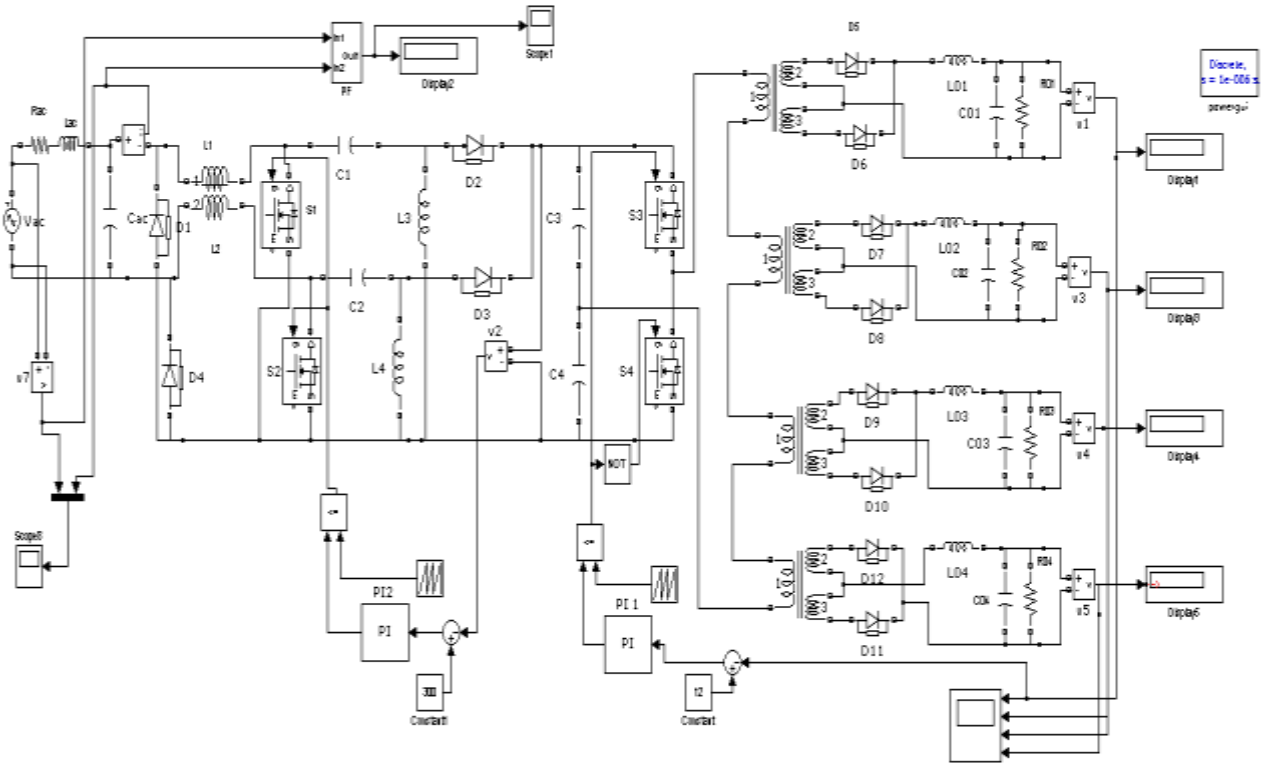

Fig 7: Simulation of bridgeless SEPIC converter using coupled inductor.

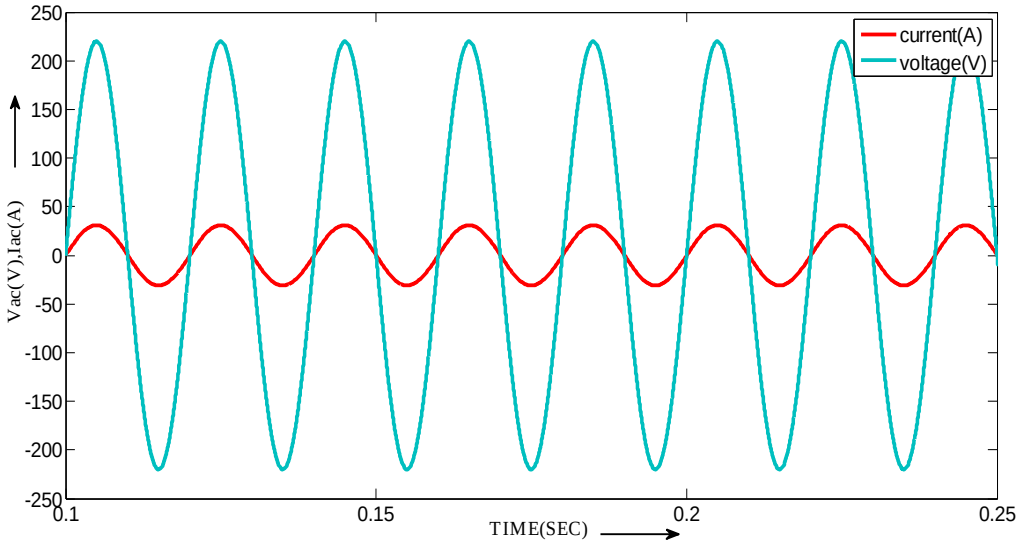

Fig 8: Supply voltage and current waveform

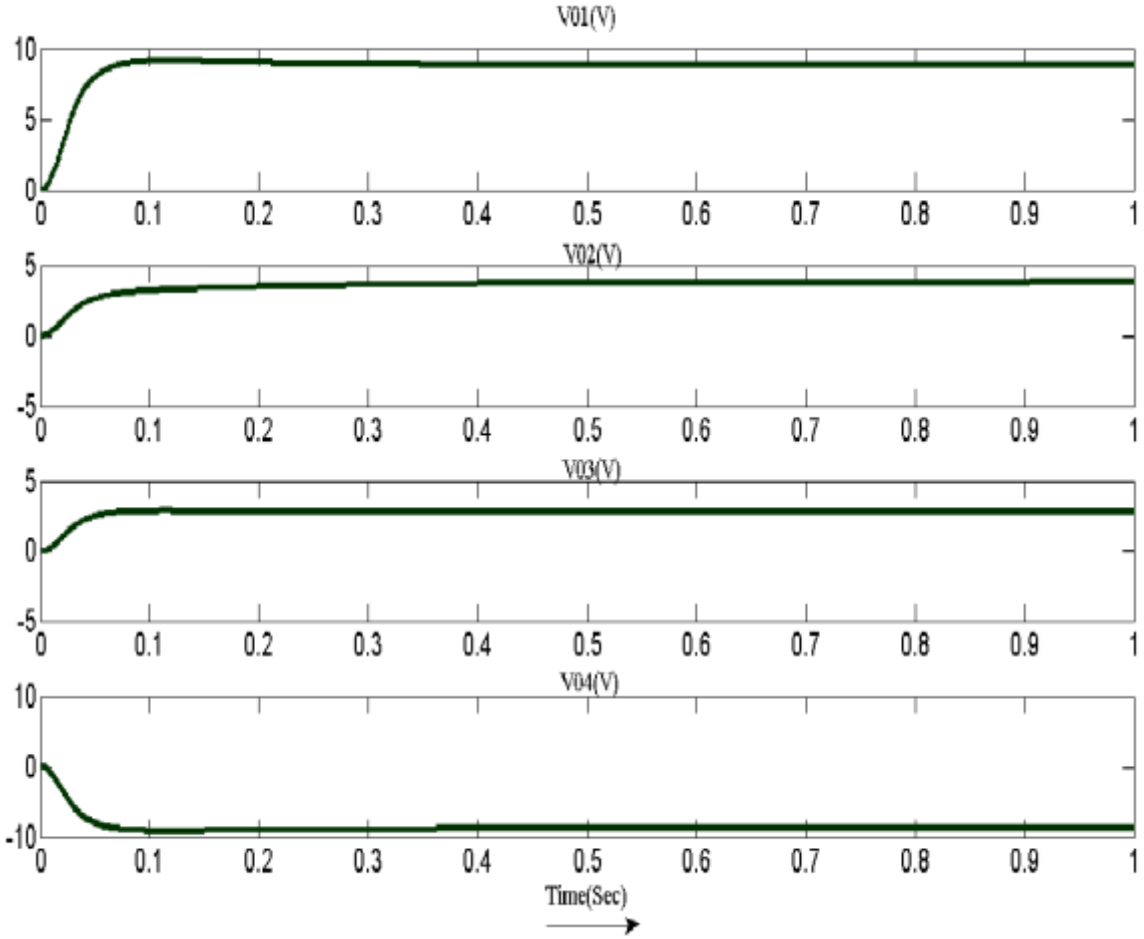

Fig 9: Output voltage waveform

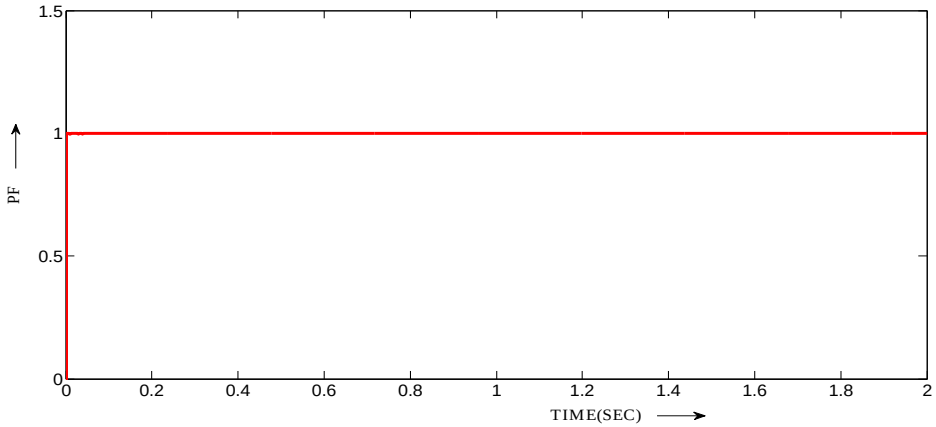

Fig 10: Power factor of the proposed technique

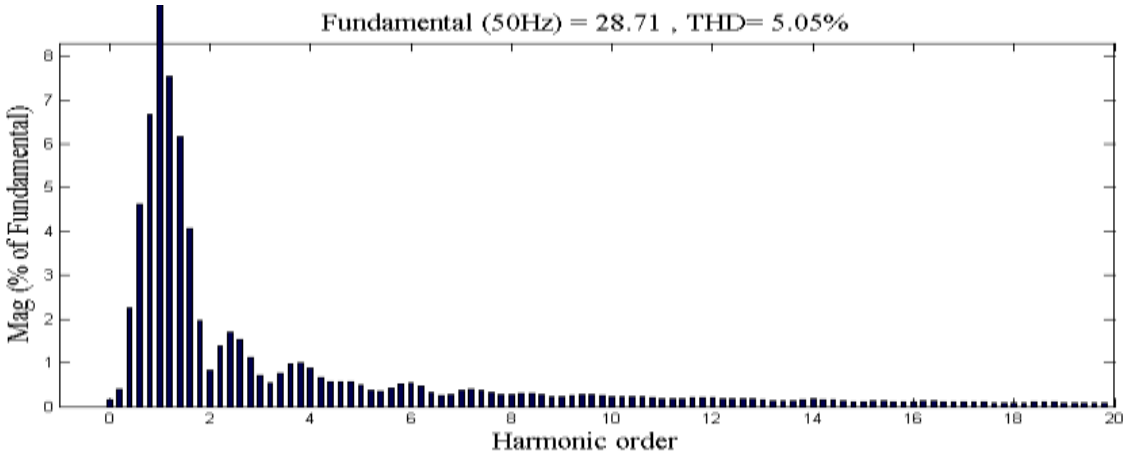

Fig 11: THD of the proposed technique

Simulation Circuit Of Bridgeless Sepic Converter Using Two Coupled Inductor

The simulation circuit of the bridgeless SEPIC converter using two coupled inductor is shown in the fig 12 and its response is shown in fig 13, fig 14, fig 15 and fig 16 respectively.

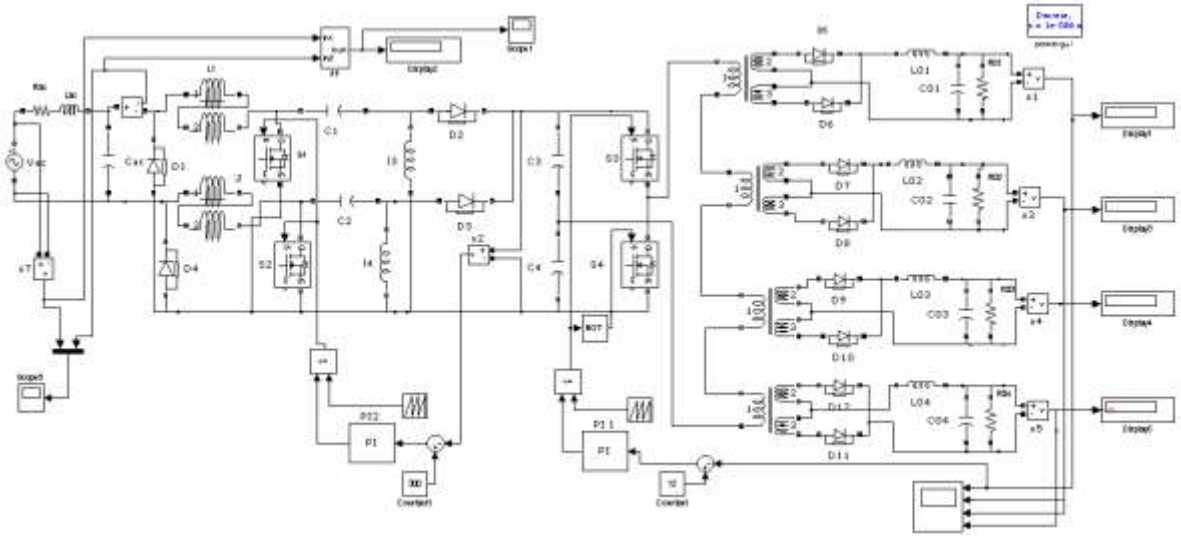

Fig 12: Simulation circuit of the bridgeless SEPIC converter using two coupled inductors

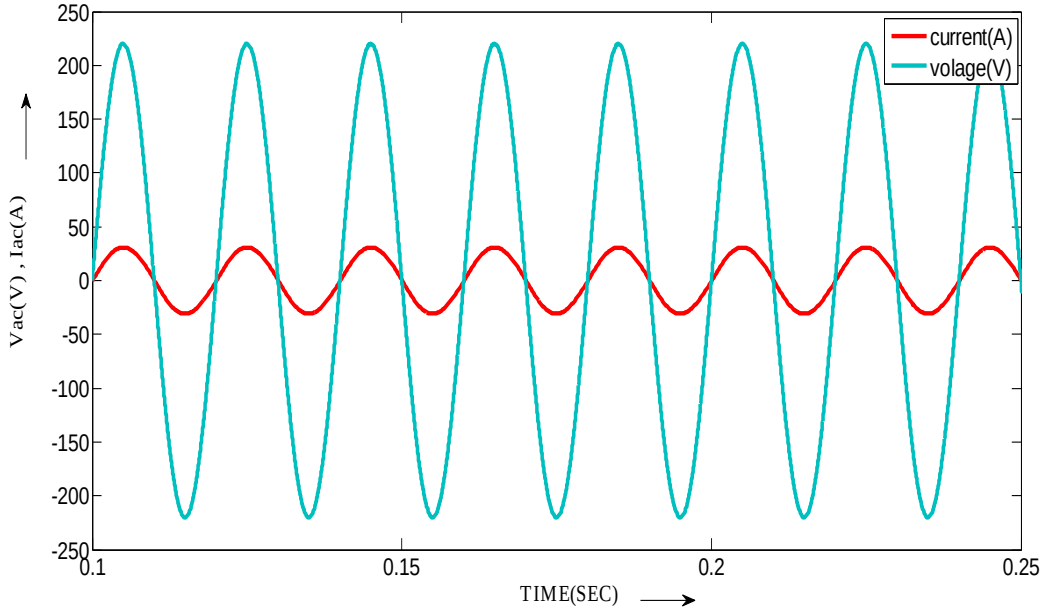

Fig 13: Supply voltage and current waveform

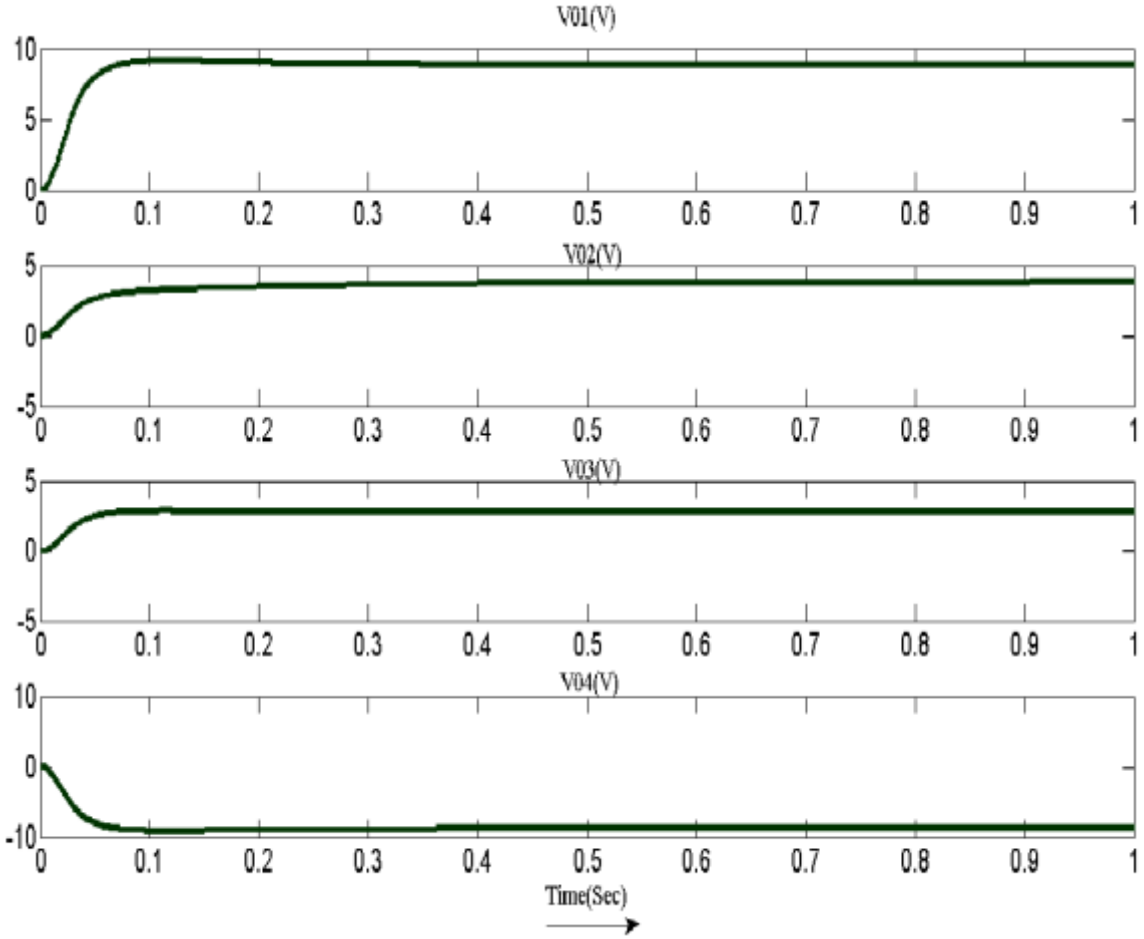

Fig 14: Output voltage waveform

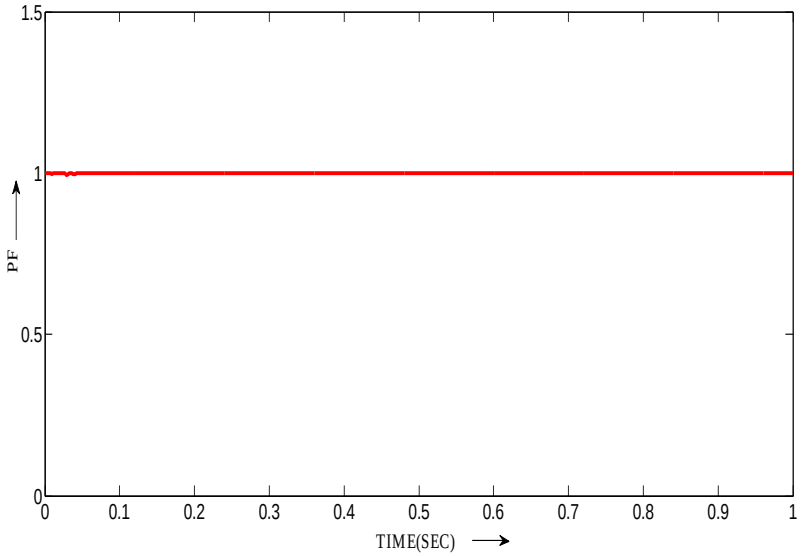

Fig 15: Power factor of the modified technique

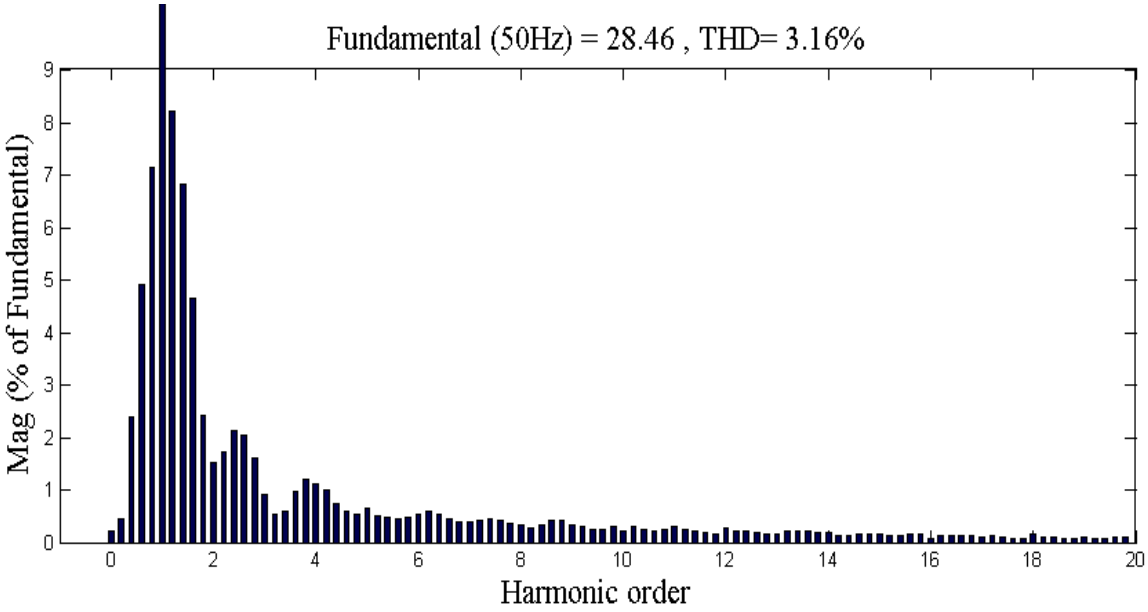

Fig 16: THD of the modified circuit

RESULT

The performance of the proposed systems are computed and the results are compared as shown in the table I. Fig 17 and fig 18 shows the variation of power factor and THD.

Table 1. Performance comparison of different SEPIC converter topologies

S.no	Techniques	Power factor	Thd
1.	Conventional PFC Converter	0.9996	5.47%
2.	PFC Converter using coupled inductor	0.9999	5.05%
3.	PFC converter using two coupled inductor	0.9998	3.16%

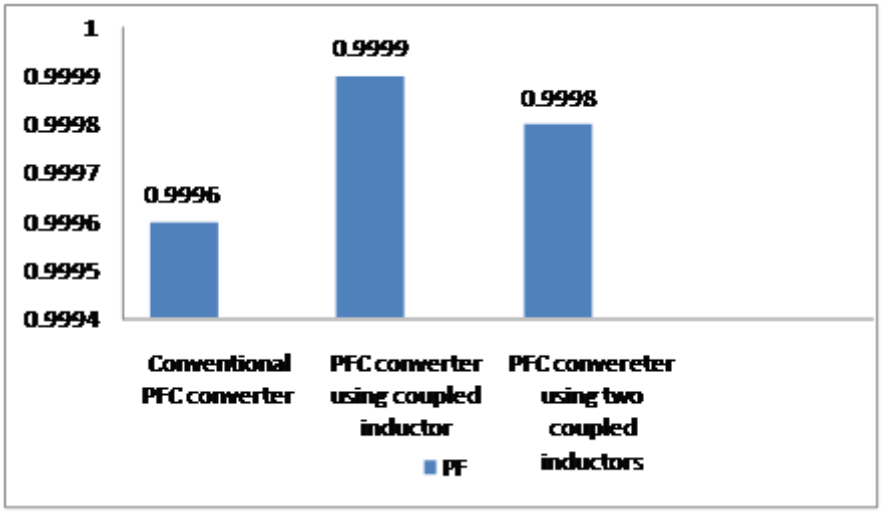

Fig 17: Comparison of Power factor

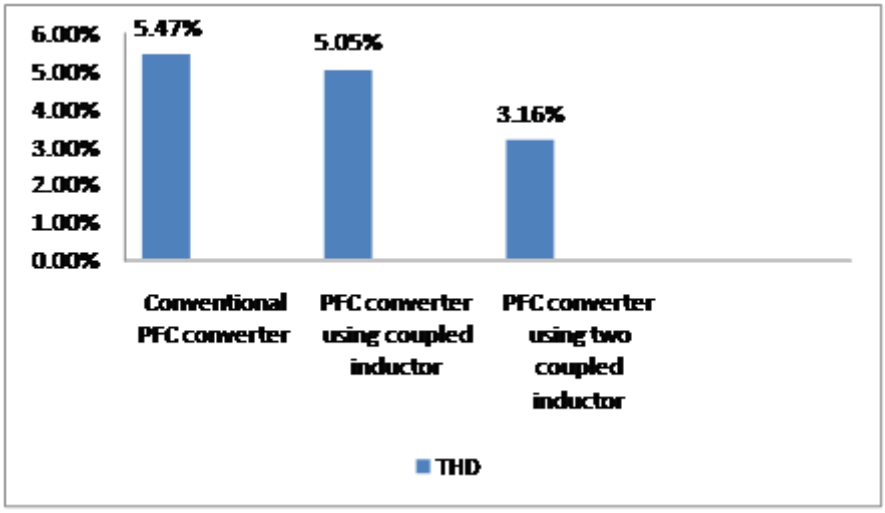

Fig 18: Comparison of THD

From the results obtained, we observe that the performance of the bridgeless SEPIC converter using coupled inductor is better than the conventional type SMPS. The power factor the PFC converter is increased to 0.9998 from 0.9996 and the THD is decreased from 5.47% to 3.16%. So, the bridgeless SEPIC converter using couple inductor proves to be the best solution for the power quality problems in the computer applications.

CONCLUSION

The power quality problems present in the conventional computer power supply is reduced by proposing a bridgeless non-isolated SEPIC converter using coupled inductor. Under the wide variations of input voltages and the loads the proposed power supply will operate efficiently. The proposed technique results in improved power factor from 0.9996 to 0.9998 and reduction in Total Harmonic Distortion from 5.47% to 3.16% when compared to the conventional power supply. They also confirm the fact that power quality problems at the front end are reduced and are recommended solutions for the power quality problems arising in the computers and other similar applications.

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