Chapter

Design and Analysis of Analog to Digital Converter System Clock Source Using Direct Digital Synthesizer

Desmond Tung and Rosmiwati Mohd-Mokhtar

Abstract

A requirement of multiple format standards by mobile telecommunication (GSM, CDMA, WCDMA, and TD-SCDMA) test set needs to be delivered possibly at lower cost. As to support its capability, phase-locked loop (PLL) frequency synthesizer has been designated as an essential part in most of the design within the box. The old design may be bulky and subject to many issues with the components' variation and aging effect. In recent years, the direct digital synthesizer (DDS) has been popularly in used to replace the PLL architecture. This chapter will focus on the DDS selection, architecture topology, prototyping, implementation technique with both hardware and software, and performance as a clock source to a sampled system as referred to receiver interest. The key parameters in the sampled system greatly rely on the jitter and phase noise specification. If they are not properly defined, the overall signal-to-noise ratio (SNR) at the sampled system output will be impacted. Eventually the receiver quality will be degraded and resulted in tremendous loss. Thus, a proper reconstruction filter design will be delivered to ensure the jitter and phase noise performance is met without degrading the existing specification by taking accountability into the matching characteristic and signal integrity.

Keywords: direct digital synthesizer, clock source, analog to digital converter, jitter, filter design

1. Introduction

Many mature products in the market utilize PLL frequency synthesizer to provide a referencing element either in radio frequency or digital application. During the beginning, there were not many options or topologies available in designing one. As a result, the released product is often found to be bulky and expensive considering the tight tolerance and accuracy requirement. As time flies by, many researchers start to explore into a possibility to implement the frequency synthesizer digitally, and there the direct digital synthesizer (DDS) was introduced [1–3].

Figure 1 shows the basic DDS block diagram. The DDS in modern days could come with multiple capabilities [4]. All of them were integrated together to provide a complete solution to customer with reasonable price. For instance, a complete DDS has both DDS core and digital-to-analog converter (DAC) integrated into

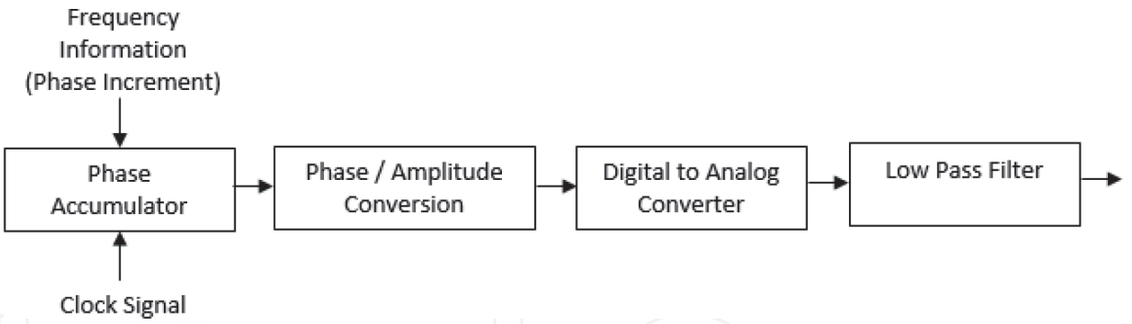

Figure 1.
General DDS block diagram.

single package. Of course, these will not come true without the advances in IC fabrication technology. In addition, a process architecture like system in package (SiP), system on a chip (SoC), and 3D stacked die also helps in providing DDS as a solution to complex design such as modulators, local oscillator (LO) clock, and chirp generator. Company like Analog Devices who has been the leader in DDS market offers a dedicated DDS IC with minimum requirement of digital signal processing (DSP) that fit the customer's need, while Xilinx, Altera, and other companies offer the solution through programmable synthesis. The trade-off of price and space requirement in a design must be made.

By programming the DDS, the desired frequency hopping, numerous modulation formats, and data rates can be achieved. Even digital modulation is possible since the processing signal is in digital. Hence, the adaptivity and flexibility of DDS make it ideal for not only radio frequency but also for many applications. Since it is digital, the thermal drift susceptibility is the least concern to a design which is favorable to most of the designers. Basically, DDS can be found in a lot of applications such as cellular base stations, wireless local loop base stations, cellular phone, and test and measurement equipment [5].

The DDS is a mixed signal device that can be analyzed as digital and analog. The DDS itself is digital, while DAC and reconstruction filter are considered as analog. In FPGA implementation, the whole design can be coded and synthesized. The DDS often comes in small package that perfectly fits in replacing bulky circuitries. The cost is significantly lower than a conventional PLL design. The only drawback is that an additional reconstruction filter is required to shape the discretized output into a comprehensive sinusoidal reference. The study will focus on the available topologies in designing a replacement clock generator with specified specifications.

As to ease the design, some of the methods were researched as explained in [6]. A tool like ADISIMDDS can be used as preliminary justification but not the actual implementation. This method suggests a proper conduct of frequency planning in order to get a usable output spectrum to fit the application. It helps to ensure the performance of DDS-based radar application.

There are many hybrid designs in wireless communication system that used DDS to work with PLL. The reason is due to that the DDS has a high-frequency resolution, has accuracy, and is easy to be implemented in PLL process control [7]. Besides, the remarkable fast frequency switching within the guard time enables time-division multiple access (TDMA) dynamic channel assignment possible [8]. The only problem with DDS is really the output spectrum. It requires a filter to pair with it, ensuring the spectrum is cleaned due to the harmonics generated upon frequency generation.

A complete DDS in the market comes with phase adjustment capability. It allows the design to associate self-adjustment knowingly to the phase delay inherited by the filter. At high frequency, the phase response may be worst due to the PCB

production process [9]. The result is a measure of jitter and phase noise that degrade the system performance [10]. These parameters are important to high-speed digital link as well as ADC system [11]. Considering a system uses DDS as global clock distribution, a time-varying noise (jitter) will impact the time available for logic operation between sequential elements [12] causing the system to fall apart.

There are some challenges that are anticipated during the research and development cycle. The constraints like tight specification in a one to one replacement, suitable techniques and topologies in clock source implementation, and phase noise and jitter specification needed to be straighten out during the concept and investigation checkpoint. Next, upon the development checkpoint, interfacing between DDS and reconstruction filter might be subjected to uncertainty. The mismatch element among components and interfacing circuitry may be a problem as well. Thus, a proper conduct of design and simulation needs to be performed.

2. Implementation and methods

The prototype was done with the aid of MATLAB, Simulink, and Altera Quartus II software. Nevertheless, Altera DE2 development kit was the hardware used. The advantage of having prototyping with FPGA is because the output can be observed by adjusting the internal module such as phase accumulator bits, look-up table design, and optimization to identify the minimum acceptable performance. From there, the Analog Devices DDS selection can take place. Once the DDS has been selected, the Analog Devices evaluation board (AD9852) will be used to evaluate the DDS. At the same time, the filter design and simulation can be performed.

2.1 Prototyping with Altera FPGA and MATLAB Simulink

Resource occupation of two look-up tables (LUTs) or read-only memory (ROM) would not meet the FPGA available resources. Thus, the approach of ROM reduction is necessary. By downsizing the LUT and shrinking the data content in the ROM, the required LUT has now reduced, down to one as shown in **Figure 2**. One solution is to replace one of the LUTs with K-bit inverters. The idea is to invert the output from the LUT as the phase accumulator reaches half of its counts. In Simulink, there is no direct inverters that can be used; however, with the addition of XOR gate, it is possible.

The whole idea of downsizing is to adjust the content stored inside the ROM. By reducing the maximum value to π/2, the steps can be remained, and therefore, the frequency resolution remained. These will change the ROM from the half-wave data

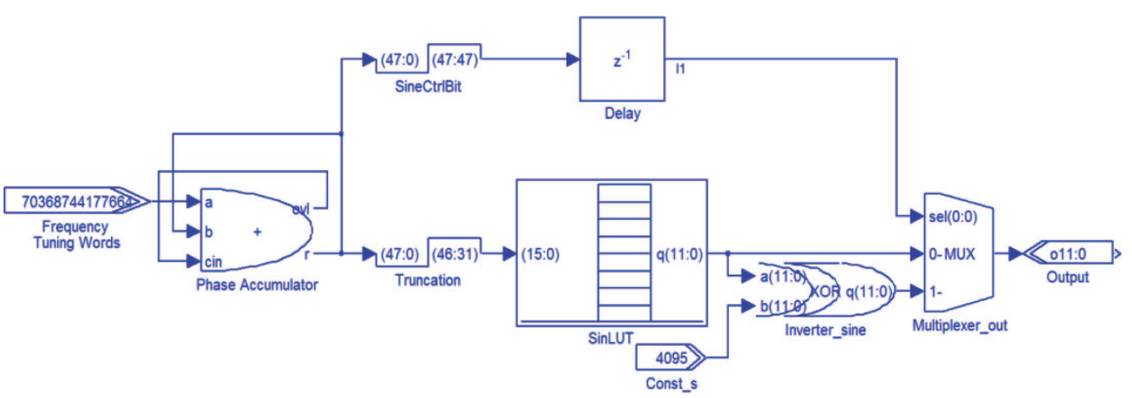

Figure 2.
Simulink model 17 bit DDS with single LUT half wave.

into quarter-wave data with successfully reducing the address bit of ROM by 1 bit, from 16 bits down to 15 bits.

2.2 Reconstruction filter design and simulation

A DDS takes two inputs, a reference frequency (f_{REF}), and tuning word M (refer to **Figure 3**). The built-in multiplier allows DDS to output a wider range of frequencies from a low reference frequency. Tuning word is essential to the DDS as it specifies the jump step of fine-resolution output frequency. The shorter the tuning word, the lower the frequency.

The reconstruction filter is needed to filter off the unwanted spurs that come with the synthesized output. By using a low reference frequency that is available in the current ADC sampled system, the multiplier within the DDS will be used. The product of multiplication can be added onto the output spectrum. Secondly, the output from LUT or ROM is driving the DAC. DAC output spectrum is anticipating the primary phase truncation spur and the second and third harmonics. **Figure 3** shows the DDS with reconstruction low-pass filter (LPF).

The specification has been defined as shown in **Table 1**. Agilent ADS simulation tool was used to design the reconstruction filter. With the spurious spectrum induced by DDS design itself, the steepness of the transition band is important to the overall quality of the performance. Elliptical response is preferable as it has a sharpen roll-off with lower order than the Butterworth and Bessel although both

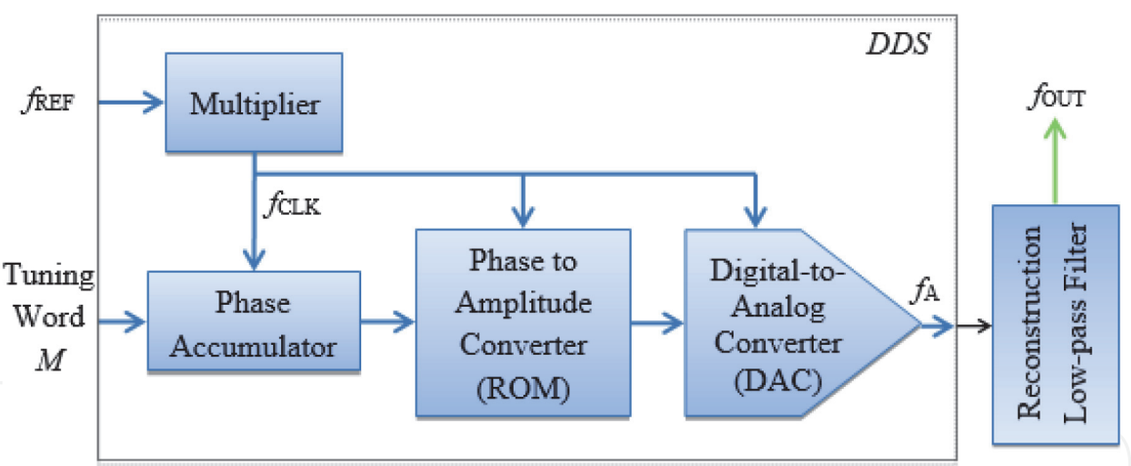

Figure 3.
DDS with reconstruction LPF.

Criteria	Target	Buffered
Cutoff frequency (f_{pass})	40 MHz	42 MHz
Passband ripple (R_{pass})	0.01 dB	0.01 dB
Stopband gain (A_{stop})	70 dB	78 dB
Response	Elliptical	Elliptical
Input/output impedance	50 Ω	50 Ω
Number of order	7	7

Table 1.
Targeted reconstruction filter specification.

offer maximal flat passband. In addition, since the comparator will be used to convert the sine wave-filtered output into square wave, an occurrence of low amount of ripple in passband will not impact the output performance.

As to utilize the internal high-speed comparator that comes with AD9852, two LPFs are required. The stopband gain for the filter specification is originally 70 dB with a cutoff frequency of 40 MHz. To cater for the tolerances and anticipated standardization of the passive component value loss between the two LPFs, a buffered margin of 8 dB (>10%) of stopband gain and 5% of cutoff frequency that is 2 MHz are added to the specification. Basically the buffered margin of 8 dB is essential due to de-normalized value to nominal value conversion loss. The result may end up with 70 dB stopband gain that is still within the specification.

On the other hand, the criticalness of the tolerance contributed by the components needs to be addressed. The total effect of conversion loss and tolerances may cause the filter to operate out of specification. The original design targeted a 40 MHz cutoff frequency. By simulating the tolerances using ADS Monte Carlo analysis, it is found out that 40 MHz gave a tight margin that even the temperature coefficient has not been included. The preliminary prototype specification is based on 78 dB stopband and 40 MHz. A total of 100 iterations is programmed in ADS Monte Carlo analysis to solve and estimate the worst-case scenario of the filter response when the tolerances are included.

In LPF design, basically the number of order is obtained with the help of MATLAB *fdatool*. With the aided design, a seventh-order LPF is advised in designing a LPF that meets the specification. Once the minimum order has been defined, designing the passive LPF can be conducted as shown in **Figure 4**.

2.3 Using AD9852A complete DDS as clock source

There are basically few steps needed to operate AD9852A as a clock source for 8960 ADC. Before that, the hardware configuration of DDS must take place. The simplified configuration is shown in **Figure 5**. In the design, there are two distinct power supplies being used to power the chip. They are digital VDD and analog VDD. The reason of having two power supplies for operation is to achieve a better isolation. This will minimize the risk of signal integrity concern such as simultaneous switching noise (SSN) or PLL ringing due to complex design within the system. As for both analog and digital ground, they are tied together.

The plan in this work is to make use of internal reference multiplier due to low reference differential clock on ADC (20 MHz) that connects to REFCLK and

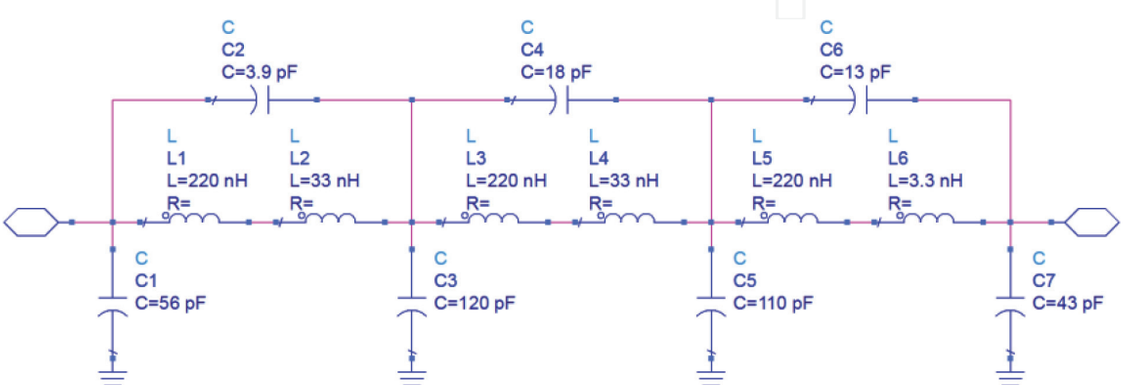

Figure 4.
Seventh-order elliptic LPF.

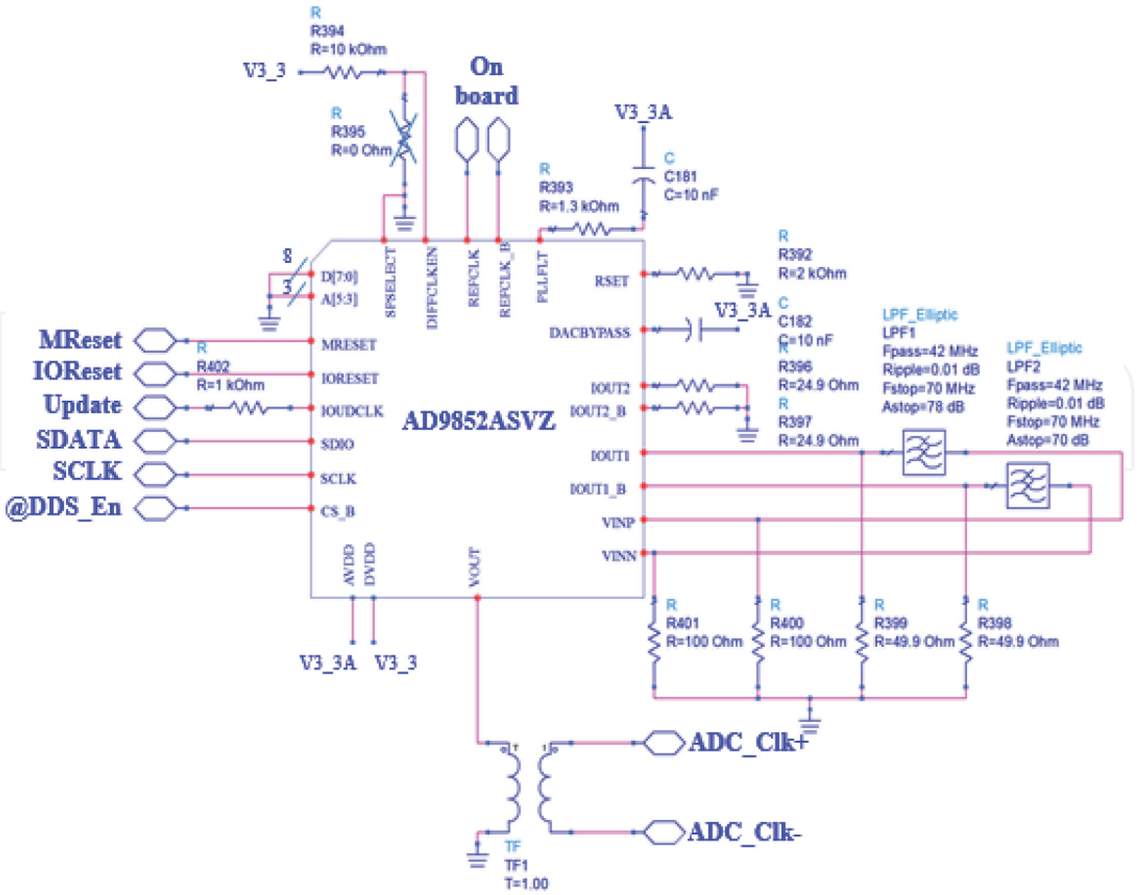

Figure 5.
Simplified DDS implementation schematic diagram.

REFCLK_B. Therefore, the internal PLL will be used. There is this pin PLL FILTER (PLLFLT) that serves as zero compensation that requires to be connected as close as possible to AVDD through RC network of 1.3 kΩ and 10 nF [13]. Nevertheless, the differential clock enable pin (DIFFCLKEN) was pulled up for differential clock application. There is also a pull-down resistor in place with no load condition. This allows future changes if the reference clock is to be used as single-ended instead of differential.

In order to improve the harmonic distortion and spurious-free dynamic range (SFDR), a bypass capacitor to AVDD is connected to the DDS's DACBYPASS pin. This pin can be left unconnected, but it may degrade the output performance slightly. Besides, there are two output channels that come with AD9852 composed of a cosine DAC and a control DAC. However, only one channel is required. Although the control DAC can be disabled programmatically, it is necessary to terminate them making sure it will not interfere with adjacent pins. With that, 24.9 Ω resistors are used for termination. The output strength of the current DACs can be controlled by the design through an external resistor.

Both channel one outputs are connected through two LPFs that have been designed in the previous section. By having both outputs filtered, a clean zero-crossing to the comparator will yield a better output. Before feeding the filtered output into the comparator, there is another 100 Ω resistor termination. They are there to ensure a 50% output duty cycle from the comparator not affected by differential input setup.

To save the pin count, serial programming has been designated in implementation. Connecting SPSELECT pin to the ground tells AD9852 to operate with serial

programming. For that, eight data bits and three address bits from MSB have connected to the ground to prevent AD9852 misbehave. With these configurations, only six control lines are needed to operate the AD9852 DDS. Basically, upon master reset, the IO update clock pin (IOUDCLK) by default is configured as an output. To avoid bus contention or any damage to the DDS, a 1 kΩ resistor is connected in a series. Even if the update pin from the host controller changes state, a constant current of 3 mA is drawn. Ultimately the output VOUT from the DDS will be connected to ADC through a balun that converts the balanced clock into unbalanced that is composed of differential output [14].

2.4 Characterization and qualification test profile

Once the first article of DDS is being produced, the characterization will take place to ensure that the design meets the specification. It can be benchmarked against the previous design to understand if the desire characteristic is achieved or otherwise. As soon as it is ready, hardware and software qualification will be started. It is meant to qualify the hardware to come out with new set of specification that could be better or tighter than the previous design. Similarly to software qualification, parameter like stability, bugs, and speed should be taken care upon, interfacing and controlling the hardware.

By replacing the DMP PLL with DDS, the characterization needs to be done thoroughly. As previously mentioned, apparently the phase noise and jitter are the major concern for an ADC sampled system. Tuning speed on the other hand will enhance user experience by speeding up the measurement. The spurious-free dynamic range is another measure of the clock signal quality. Also, since the circuit operates around other components, even with proper fence and shielding, it would be good to understand the cross-talk effects.

Agilent 8960 has a guaranteed specification that is operable at 55°C. Hence, the temperature test profile must be planned carefully. The temperature profile was used to characterize and qualify the newly developed DDS. The same temperature profile will be used upon characterization prior to specification roll-up as well as qualification. Ambient temperature within the factory is kept at 23°C. Hence, a ramping and soaking period of 30 minutes is required to allow that the temperature settled within an error band of ±1°C. Respective test point will be connected through a semirigid coaxial 50 Ω cable along with a 1 meter cable connection between the DDS output and the PXA or DSA. A set of workbench test script will be used to collect the data with previous test line limit. The actual test line limit will only reflect the DDS design after qualification. **Table 2** is constructed as the required sampling clock in Agilent 8960 ADC board.

Basically the qualification cycle will be performed using Weiss WK 1600 chamber series. As shown in **Figure 6**, there will be a switchbox being deployed to switch against different equipment. The reason being is that the probe of each instrument has its own impedances. Without the switchbox, all the measurement will become invalid as the impedances may be altered. After all, the master controller, a host will be doing the entire necessary configuration to control the equipment and perform data collection.

Agilent PXA with phase noise option feature was used to characterize the phase noise performance of DDS. The center frequency was adjusted accordingly to the frequency of interest. Phase noise is usually expressed in decibels relative to carrier power per unit Hz bandwidth (dBc/Hz). An array list of offset frequency was setup by decade to measure the phase noise. Besides of phase noise measurement, the SFDR can be measured to anticipate the strongest spur power level after the fundamental frequency.

Formats	Measurement	Sampling rate (MHz)
GSM GPRS EGPRS	PFER/PvT/EDPOW/EvM/EPOW	18.9583
	GSM IQ tune	19.9899
	EPSK IQ cal	13
	EPSK XTXP	19
	EPSK SPC	20
TD-SCDMA	TD ACLR/SEM	19.2
	TD POW/CLPC/DPOW/FDT/OLPC/OOS/TOOP/WQ/WQ cal	15.36
	TD IF cal/OBW	12.8
WCDMA	WOBW	20.48
	W-AVP	20
	W-SEM	23.04
CDMA	C-audio	16
	C-POLT	10
	C1x-other measure	14.7456
IS136	Min	2.5
	Max	40

Table 2.
Wireless mobile communication sampling frequency specification in 8960.

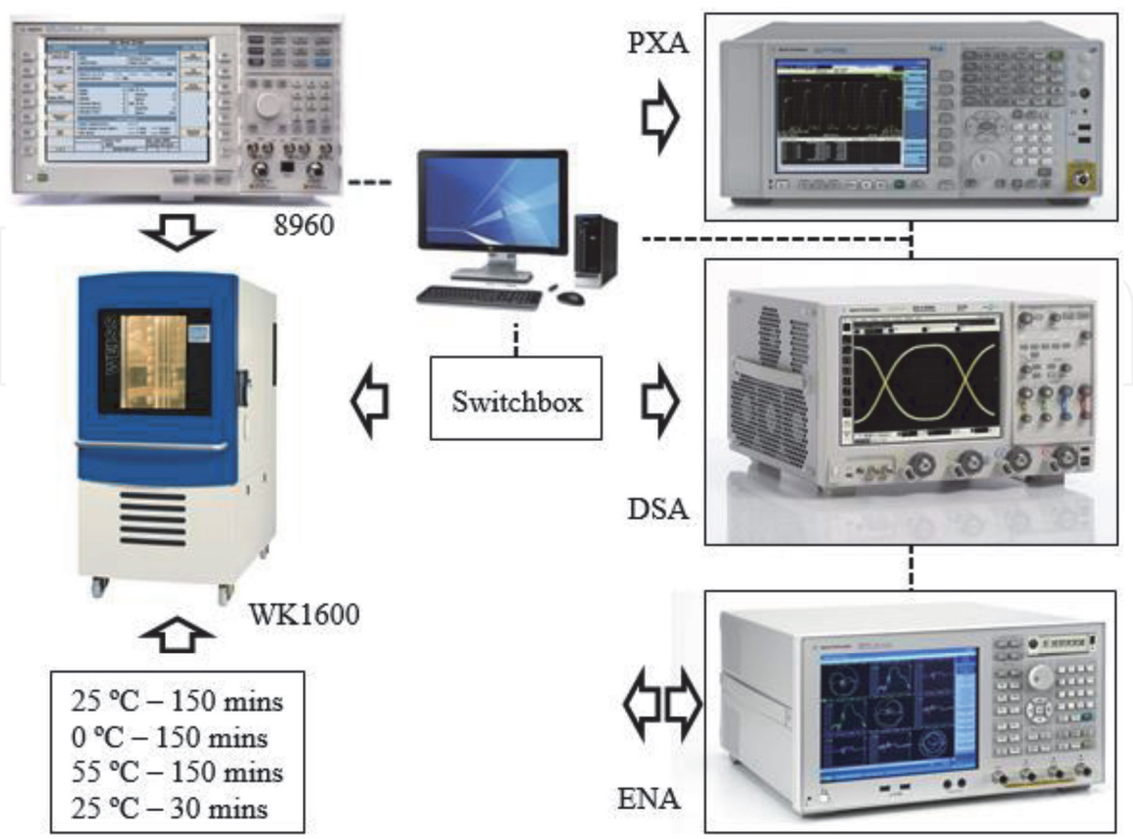

Figure 6.
Test and measurement setup.

3. Result and analysis

3.1 Software simulation

Table 3 summarizes the outcome from the prototypes. Apparently the ROM downsizing has effectively reduced the required memory bits by 80% (1–483,840/2,396,160). However, notice that by reducing the half wave from two LUTs into one may reduce the required memory but not the price. If Cyclone II is to be used, a wider user I/Os of 422 that has the same memory as of Cyclone III with 196 user I/Os is recommended but costly.

Cyclone III may seem reasonable, but notice that the available user I/Os is far lesser than Cyclone II. At around the same price, device EP2C35F484C6 provides more user I/Os than EP3C40F324C6. With successful ROM downsizing, device EP2C35F484C6 can be used, and the output performance remains as of first prototype. The advantages in terms of cost, user I/Os, and output performances have provided a satisfied outcome.

The LPF designs' comparison is shown in **Table 4**. By using two simulation tools along with their available feature, the LPF has been successfully designed. The specification is guaranteed as close as the original specification. The responses provided by MATLAB are giving the designer an idea of how the filter supposed to behave. The hand-calculated value was validated by ADS design guide. After fitting with nominal value, a worst-case analysis was done using Monte Carlo analysis by accounting all the component tolerances within the filter itself. Comparatively the final design has a promising specification at passband around 40 MHz. The only disadvantage is that the stopband gain is closed to the initial unbuffered specification. However, as expected, nominal value conversion will definitely introduce these losses, and hence, trade-off has been made.

Design	Cyclone	Simulink recommended device (User I/Os)	Minimum memory bits required	Used	Usage	Price per unit
Half wave 2 LUTs	III	EP3C55F484C6 (328)	2,396,160	1,572,864	66%	$ 212.30
Half wave 1 LUT	III	EP3C40F324C6 (196)	1,161,216	786,432	68%	$ 122.20
Half wave 1 LUT	II	EP2C70F672C6 (422)	1,152,000	786,432	68%	$ 387.20
Quarter wave 1 LUT	II	EP2C35F484C6 (322)	483,840	393,216	81%	$ 149.60

Table 3.
Comparison among different prototypes.

Criteria	Target	MATLAB	ADS design guide	Final
3 dB cutoff ($f_{cut\text{-}off}$)	42 MHz	46.2 MHz	46 MHz	46.06 MHz
Gain at 40 MHz	0 dB	−0.006 dB	−0.004 dB	−0.003 dB
Passband ripple (R_{pass})	0.01 dB	0.01 dB	0.01 dB	0.01 dB
Stopband gain (A_{stop})	−78 dB	−78 dB	−78.07 dB	−71.561 dB

Table 4.
LPF designs comparison.

3.1.1 DDS clock generator performance

Figure 7 displays the overall DDS simulation model as clock generator. By setting the DAC output current to be greater at about 20 mA, the output performance has a better slew, jitter, and phase noise performance. **Figure 8** shows example of the DDS performance at frequency of 2.5 MHz. From simulation, the higher the frequency, the LPF phase shift became obvious. As the frequency keeps increasing, the effectiveness of the LPF is noticeable as the high-frequency components from the source are being filtered off. With all the changes, the output differential clocks are still centered at 1.6 V at 1.5 V_{P-P}. Signals are the square wave by assuming the DDS output is exactly half of system clock.

As frequency increases, all nonlinearity effects have been revealed. From 2.5 to 40 MHz, obvious distortion is observed at the output from DDS. The same occurred to the filtered output. At the frequency of 14.7456 MHz, output lags its input by almost 90°. As frequency goes to 19.9899 MHz, the phase lags increased beyond 90°. When it comes to 40 MHz, the phase lag increased to approximately 270°.

The phase lag analysis shows that there is some discrepancy between the s-parameter response results against transient analysis. This is possible as the marker that is placed on transient analysis is bounded by the number of points. To increase the point resolution, longer time is required to perform the simulation. However, based on the percentage, the validation of less than 4.5% is achieved, and therefore, the LPF phase response has been verified.

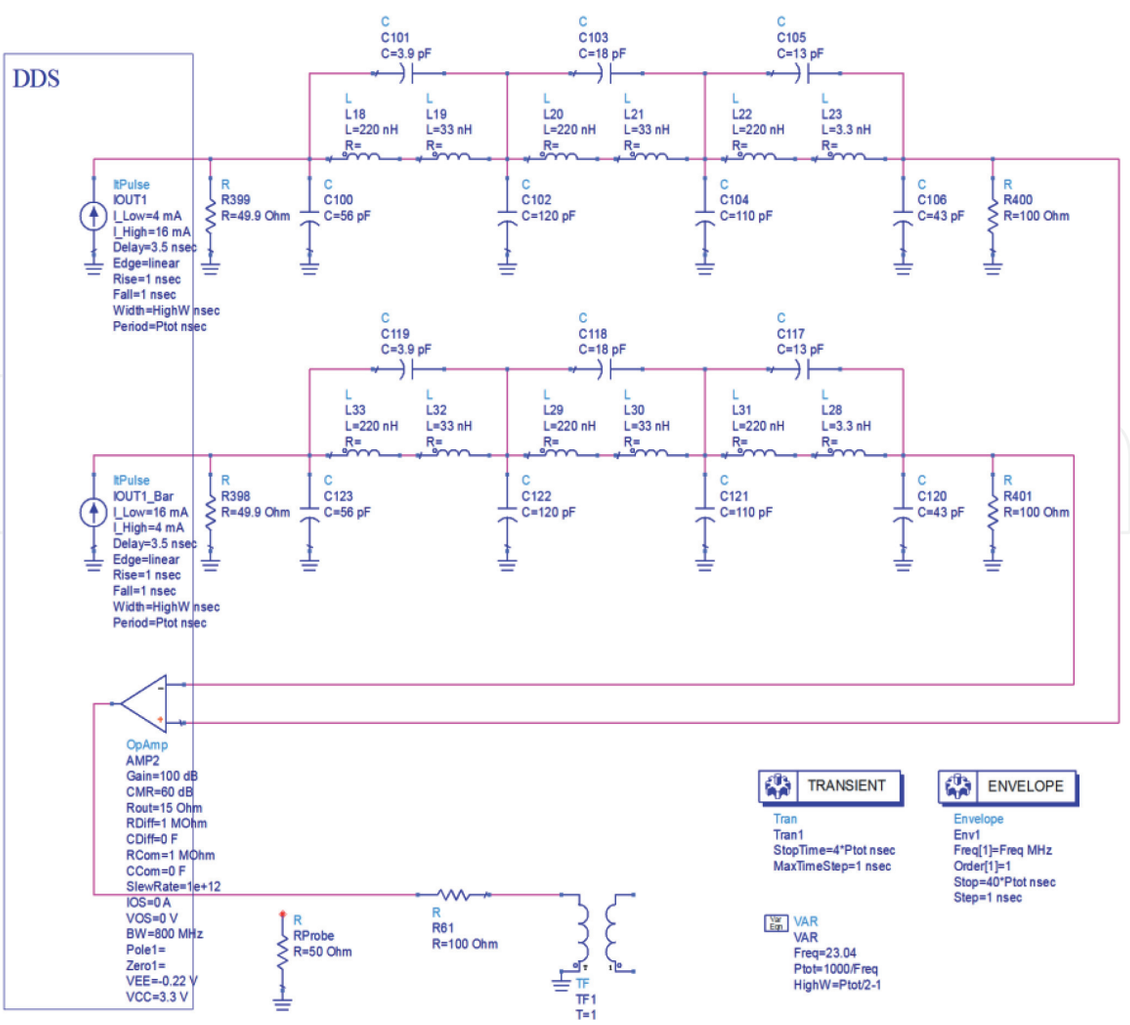

Figure 7.
DDS simulation model as clock generator.

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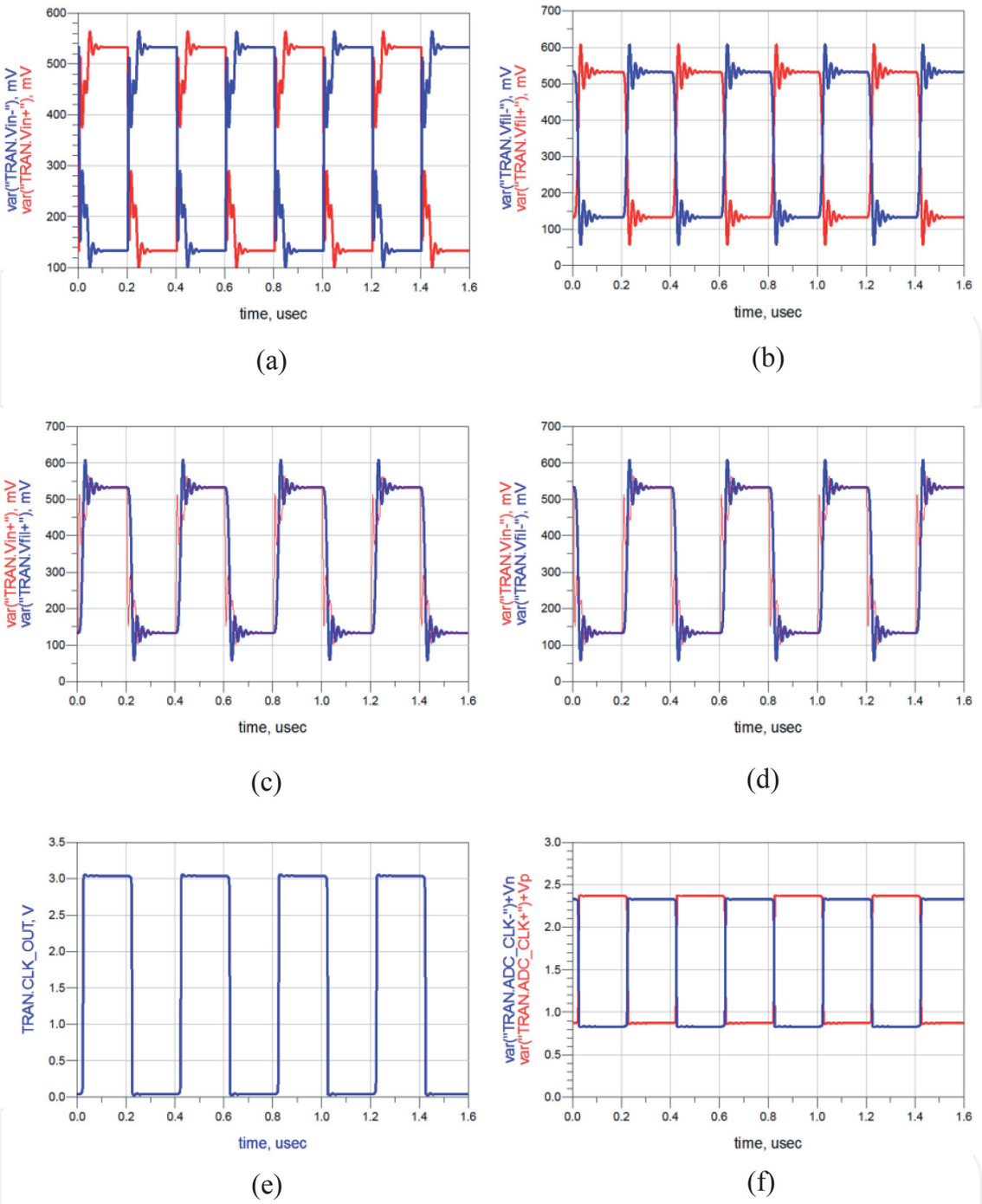

Figure 8.
DDS performance at 2.5 MHz (IS136). (a) DDS output: IOUT1 (red), IOUT1' (blue), (b) Filtered output: IOUT1 (red), IOUT1' (blue), (c) Phase response comparison: Vin+ (red), Vfil+ (blue), (d) Phase response comparison: Vin- (red), Vfil- (blue), (e) DDS clock output, and (f) ADC differential clock.

3.2 Hardware implementation

In this work, DE2 is being used as prototype implementation. Choosing it is essential as it comes with all the required peripherals and it is also inexpensive. The design was enhanced by downsizing the ROM, making DE2 a perfect fit. Apparently by having DE2, working alone is impossible to collect the time domain measurement. Therefore, an external 12-bit DAC AD7545A was used to perform the analog conversion. The basic setup of the DAC is by having the VREF connects to a 0.5 V so that the output will rail from 0 to 1 V. Together with feedback circuitry and a 50 Ω output, VOUT1 can be measured using scope.

During a 2.5 MHz output (**Figure 9(a)**), a smooth sine wave is observed. This is because the PA is extremely slow and outputting a relatively fine resolution at the

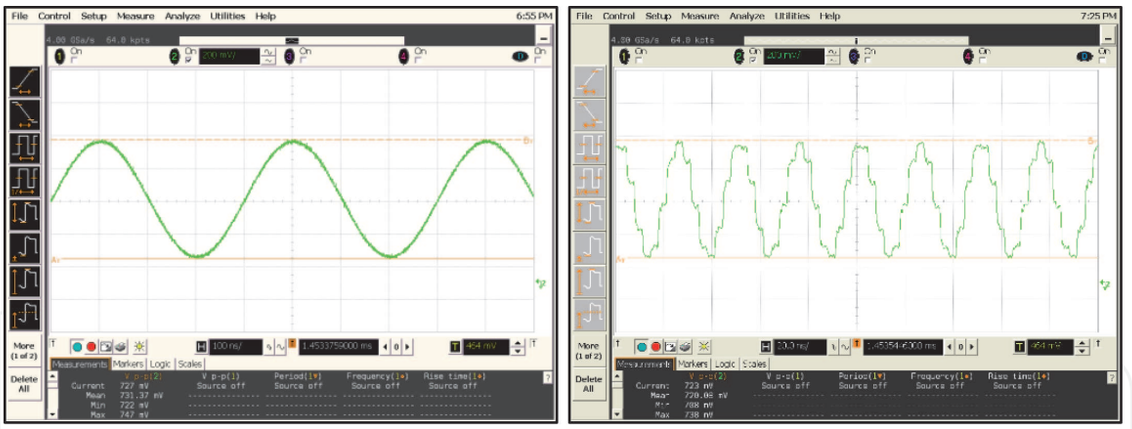

Figure 9.
DE2 quarter wave DAC output at (a) 2.5 MHz and (b) 40 MHz.

output. However, as the frequency changed from 2.5 to 40 MHz (**Figure 9(b)**), the staircase shape output starts to reveal. Hence, the comparison between simulation and practical measurement can be conducted. The results yield the same thing as of the simulated outcome. The same output response has been measured at AD9852A DDS output.

The LPF was characterized throughout the temperature profile running from 0 to 55°C. This is meant to qualify the LPF in terms of temperature coefficient introduced by passive components. **Figure 10** demonstrates a collective data for all samples. It helps to understand part-to-part variation together with temperature impact towards the LPF. From **Figure 10**, it seems that the designed filters were rather stable and consistent over the passband. The 3 dB gain can be found around the 42 MHz which follows the design specification. There is a lot of fluctuation that can be seen beyond the stopband frequency of 70 MHz by design. These variations will only contribute towards the phase response at the output of LPFs. Since the output magnitude is greatly attenuated, the phase changes will not impact DDS performance at all. By accounting part tolerances, temperature coefficient, and PCB properties, the stopband gain greater than 70 dB has been achieved. From the

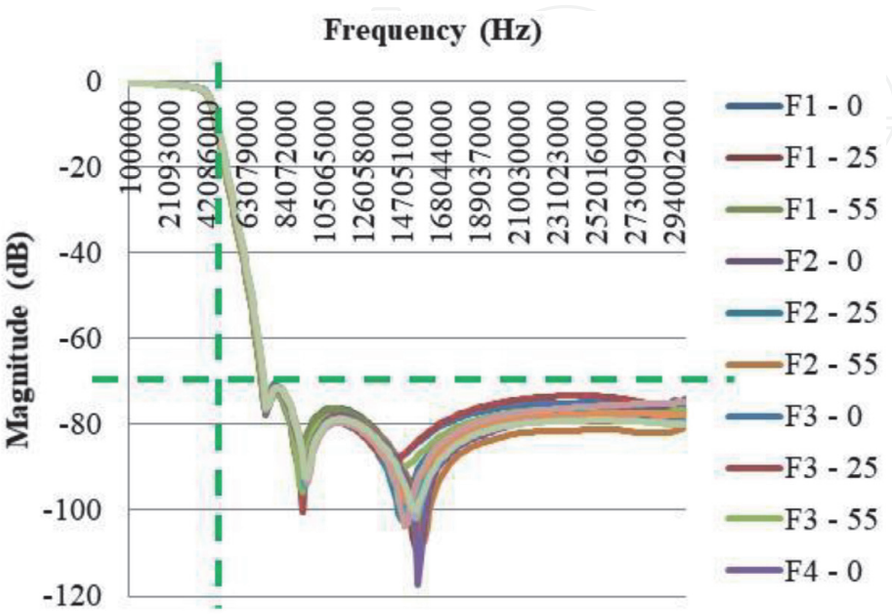

Figure 10.
Comparison among five samples across temperature.

results, the design of LPFs is meeting the specification and guaranteed stable with wide range of operating temperature.

3.2.1 DDS clock generator performance

There are five measurements being conducted for DDS clock source characterization. They are spectrum, phase noise, spurious-free dynamic range, jitter, and transient measurement. **Figure 11** shows the frequency domain measurement result at 14.7456 MHz, and **Table 5** tabulates the measured power level across temperature. It seems that over the operating frequency range, there is about 1.54 dB loss. This loss can be found at lowest frequency of 2.5 MHz. The reason for this loss may be due to the bandwidth of the comparator itself. Ideally during simulation, the comparator is expected to operate from DC up to 400 MHz that is greater than the system clock of 300 MHz. However, in practical, the bandwidth could start somewhere from 1 to 300 MHz, and therefore, a lower power level has been obtained around the corner. Beside this lowest frequency, the rest of them behave as expected. Additional 2 dB shall be attained when the load impedance is increased to a maximum of 1 MΩ that is exactly the impedance of next stage digital circuits.

The phase noise is quite consistent over temperature (**Figure 12**). From the result, it indicates that at sampling frequency of 2.5 and 20 MHz, the phase noise is as stable as little changes across temperature. On the other hand, starting from 10 to 19.9899 MHz, there is about a 3 dB shift from 0–55°C, at frequency offset of 1 kHz. The same goes to 23.04 MHz as well as 40 MHz.

The spurious-free dynamic range has only being qualified at the ambient temperature. The results that were discussed are chosen from those that are closest to the −60 dB baseline (example of 16 MHz frequency is shown in **Figure 13**). The strongest spur level has been found to be −60 dB below or 70 dBc within a frequency range from 13 to 20.48 MHz. This satisfied the wide-operating range to ensure the integrity of DDS clock source. This third harmonic spur is expected and managed to suppress the elliptic LPF since it fell out of the 42 MHz range.

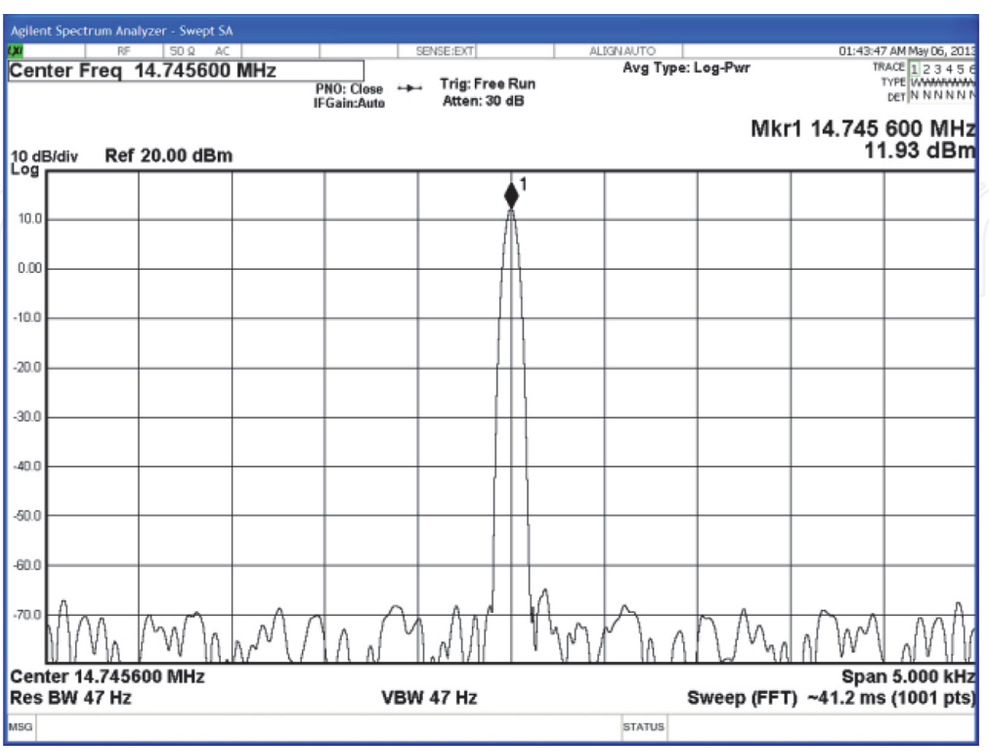

Figure 11.
Frequency domain measurement result at 14.7456 MHz.

Sampling rate (MHz)	Measured (0°C)	Measured (25°C)	Measured (55°C)
2.5	10.75	10.39	10.39
10	11.98	11.95	11.93
12.8	11.98	11.95	11.93
13	11.97	11.95	11.92
14.7456	11.95	11.93	11.91
15.36	11.95	11.92	11.9
16	11.94	11.91	11.9
18.9583	11.92	11.87	11.85
19	11.92	11.87	11.84
19.2	11.91	11.86	11.83
19.9899	11.91	11.85	11.83
20	11.9	11.85	11.83
20.48	11.89	11.84	11.8
23.04	11.85	11.8	11.77
40	11.77	11.61	11.57

Table 5.
Measured power level across temperature.

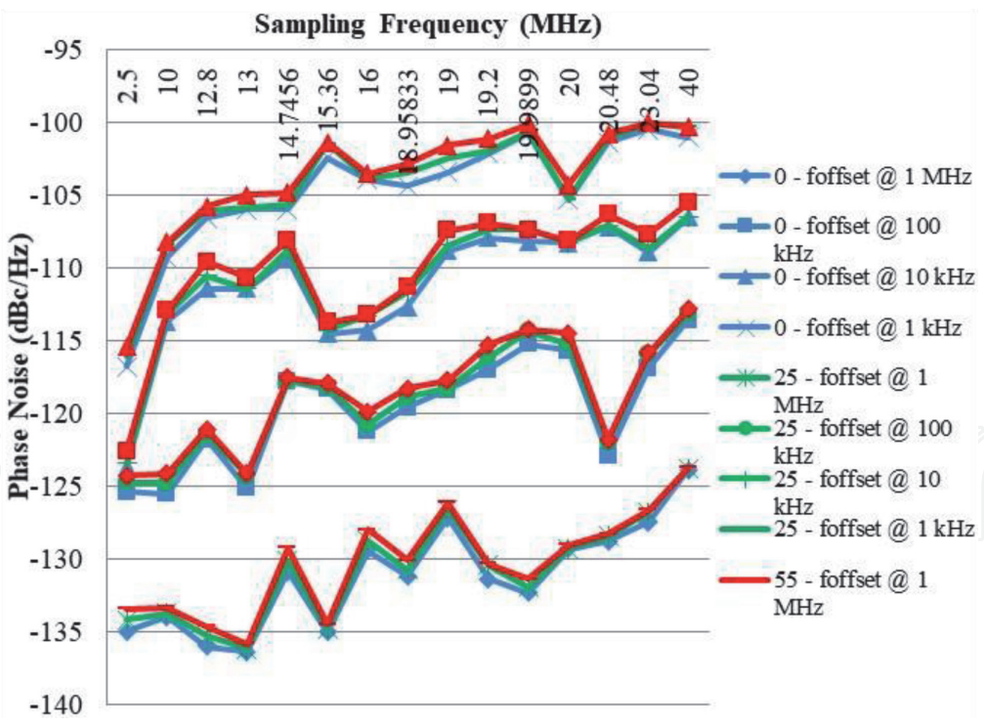

Figure 12.
Phase noise result over temperature.

There are four parameters involved in jitter analysis. Those are random jitter (RJ), period jitter (PJ), data-dependent jitter (DDJ), and total jitter (TJ) (**Figure 14**). In the second graphs of **Figure 14**, the RJ and PJ have been zoomed in. This graph is important to this work as it is a measure of how stable the clock is.

Apparently the poorest jitter fell upon a 20.48 MHz WCDMA sampling clock. The cause could be contributed by the DDS internal logic itself. Even with a

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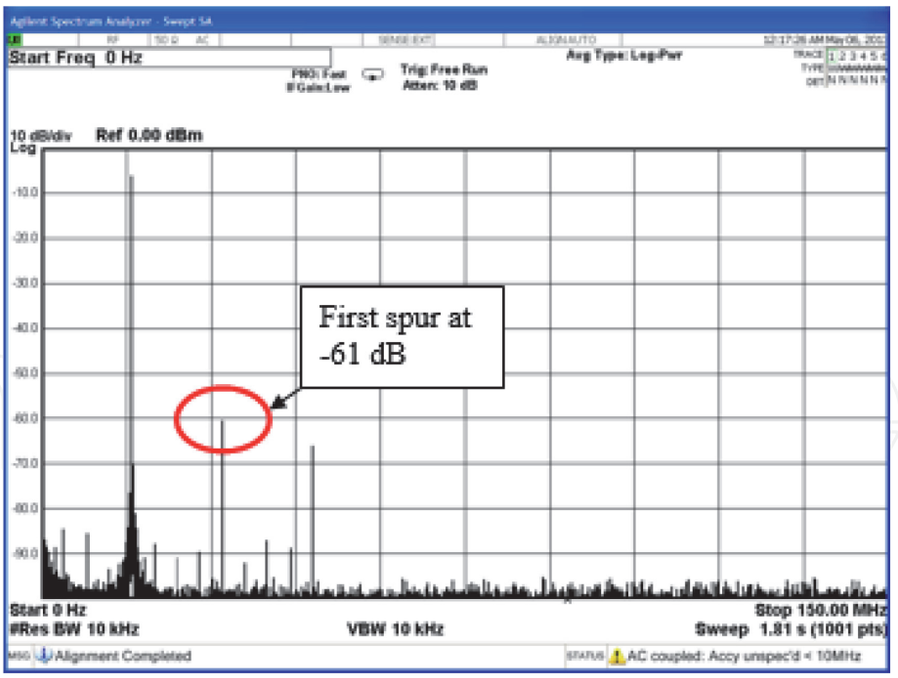

Figure 13.
SFDR at frequency 16 MHz.

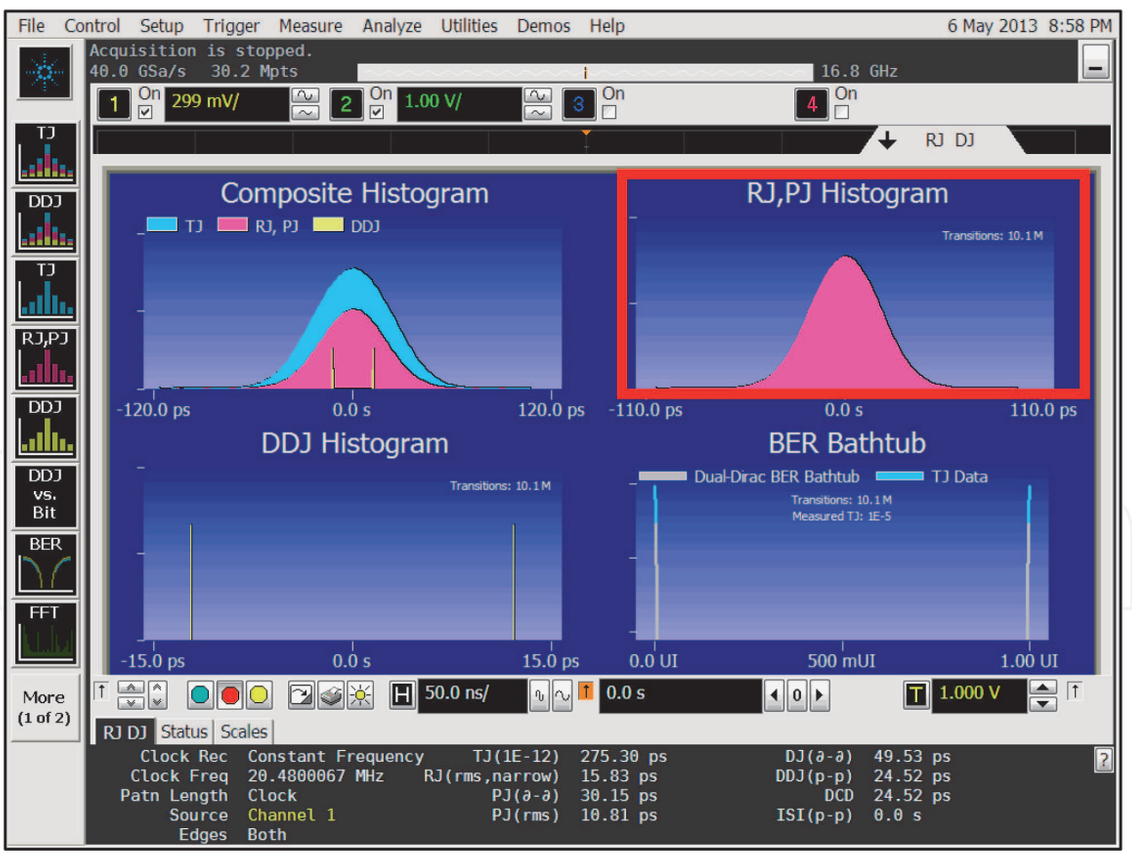

Figure 14.
Output clock jitter at 20.48 MHz.

30.15 ps, its output is far better than the DMP PLL that has a peak jitter at 150 ps. The same goes to jitter RMS. When the output frequency is at 20.48 MHz, the RMS jitter was measured at 10.81 ps. The accumulative transition of 10.1 M samples yields that the output clock at 20.48 MHz is fluctuating around the time axis. The

ADC chip has a requirement of 200 ps which makes the DDS meets the criteria. Otherwise, the output from the ADC will be subjected to nonlinearity errors.

The RMS period jitter is determined using the standard deviation of random jitter. As far as the random jitter is concerned, it is composed by the random effect of thermal, flicker, and shot noise that inherits within the DDS. Those noises are a function of temperature that will typically degrade the period jitter performance. However, in this work, the DDS has a remarkable output that remains within 12 ps PJ_{RMS} at 55°C (refer to **Figure 15**).

Both terminations with high and low impedance are performed in transient analysis. From the results as shown in **Figure 16**, it is obvious that when the measurement was made using high-impedance probe, there is a reflection which occurred at high state (3.3 V) as well as low state (0 V). The voltage overshoot can

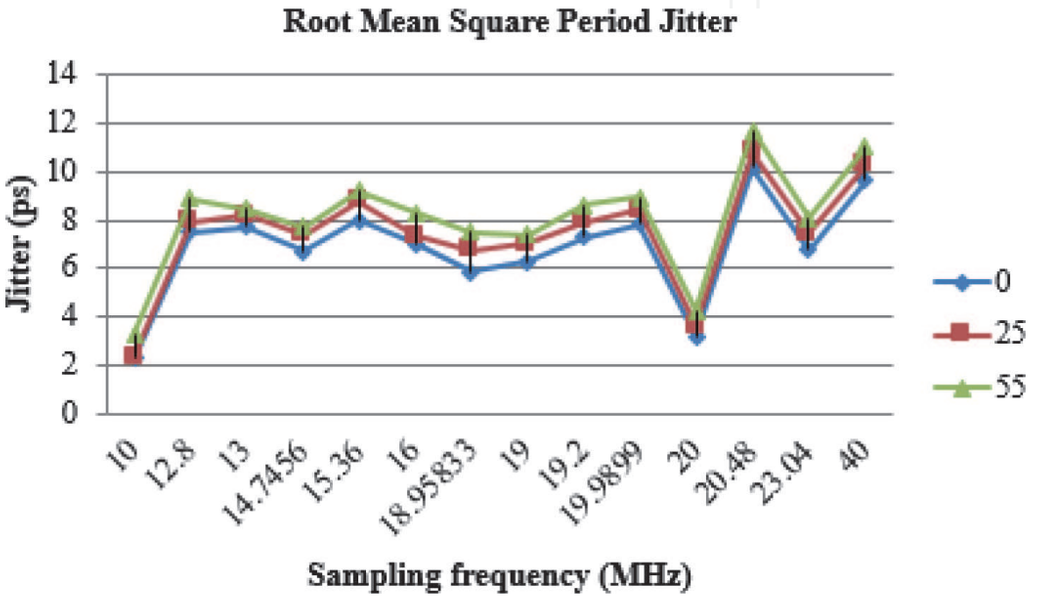

Figure 15.
RMS period jitter across temperature.

Figure 16.
Clock output waveforms comparison at 2.5 MHz.

go as high as 4.2 V and as low as 0.4 V. At low frequency of 2.5 MHz, the overshoot period is shortened and settled almost immediately. However, as frequency increased, the overshoots stay longer to settle. This is essential in order not to damage the subsequent device.

One possible solution is to connect this output to a buffer before sending it into the next stage. Alternatively, a matched load to this output will eliminate the overshoots as shown using low-impedance probe of 50 Ω. By matching the comparator output to a 50 Ω, a clean 2 V_{p-p} signal can be achieved. In any case, the final implementation utilizes a 50 Ω balun to generate an unbalanced output, and therefore, differential signal is obtained. The balanced to unbalanced signal conversion may generate ringing around two different states, but it also provides an isolation between the source and the receiver in this case, DDS output and ADC sampling clock input. Though there are ringing at both differential signals, the differential ADC clock input only accounts for the difference between two signals to define as a transition.

3.3 Comparative result analysis

The filter design has step forward from the targeted specification into the simulation and then the actual implementations. By catering the worst-case analysis through simulation, the final outcome has somewhat stratified. The measured value was retrieved from an average of five samples at ambient condition. The targeted cutoff frequency was at 42 MHz as to allow a wider design margin for the filter to shift this frequency around. The implemented design shows a 41.95 MHz unlike what the simulation preached at around 46 MHz. When subjected to temperature, the poorest corner frequency fell at 41 MHz with 1 MHz margin to designed frequency. **Table 6** tabulates the filter comparison.

Secondly, the gain at 40 MHz is relatively low compared to the simulation result. Actual LPF exhibits a −2.23 dB loss compared to targeted 0 dB. However, this loss is essential to the design in this work. Since a high-speed comparator that supports hysteresis of maximally 20 mV_{p-p} is being used, the outputs from AD9852A has been programmed as differential; these −2.23 dB loss seen at the output of LPFs will become insignificant. Though with only 77.4% strength of the original signal, as long as the output is differenced by 20 mV_{p-p}, the comparator can still produce a clean and stable clock signal.

For the stopband gain, apparently the actual measurement shows a better performance than the simulated result from the ADS. The difference between MATLAB and design guide is anticipated. The ideal value to nominal value conversion will definitely contribute that loss into the design. Of course it is far worst compared to the targeted value. As a reminder, the targeted value was buffered by 8 dB, and the original specification is 70 dB. In this case, the actual design is better in essence. Lastly, the phase response for all results yells the same thing. The designed filter has a linear phase across the passband.

Criteria	Target	MATLAB	ADS design guide	Final	Measured (25°C)
3 dB cutoff ($f_{cut-off}$)	42 MHz	46.2 MHz	46 MHz	46.06 MHz	41.95 MHz
Gain at 40 MHz	0 dB	−0.006 dB	−0.004 dB	−0.003 dB	−2.23 dB
Stopband gain (A_{stop})	−78 dB	−78 dB	−78.07 dB	−71.561 dB	−72.66 dB
Phase response	Linear	Linear	Linear	Linear	Linear

Table 6.
Filter specification comparison.

Sampling rate (MHz)	Simulation	Measured (25°C)	% diff.
2.5	11.895	10.39	14.49%
10	11.876	11.95	0.62%
12.8	11.869	11.95	0.68%
13	11.865	11.95	0.71%
14.7456	11.858	11.93	0.60%
15.36	11.855	11.92	0.55%
16	11.854	11.91	0.47%
18.9583	11.839	11.87	0.26%
19	11.838	11.87	0.27%
19.2	11.837	11.86	0.19%
19.9899	11.831	11.85	0.16%
20	11.833	11.85	0.14%
20.48	11.828	11.84	0.10%
23.04	11.811	11.8	0.09%
40	11.529	11.61	0.70%

Table 7.
Power level result comparison.

The comparison was also made in terms of spectrum analysis. Both results collected based on the 50 Ω termination are shown in **Table 7**. Generally, there are some differences from a frequency range of 10 to 40 MHz. The discrepancy occurred to be lesser than 1%. The only largest difference in magnitude is found at the sampling frequency of 2.5 MHz. The loss could be imposed by the PXA itself or even the bandwidth of the comparator itself. However, given the advantages of having balun 50 Ω matched to the comparator and a differential clock requirement for the ADC device, this loss will become insignificant.

Specifications	DDS	DMP PLL	Improvement
Frequency range	DC-42 MHz	2.5–40 MHz	12.0%
Frequency resolution	1.1 μHz	3.73 mHz	Huge
Phase noise at 1 kHz	<100 dBc/Hz	< 80 dBc/Hz	25.0%
Period jitter (rms)	12 ps	50 ps	76.0%
Period jitter (peak-peak)	121 ps	300 ps	59.7%
SFDR	70 dBc	56 dBc	25.0%
Tuning speed	<100 μs	< 4.3 ms	97.7%
Communication protocol	I^2C	SPI	—
Communication speed	2.8 MHz	1 MHz	180.0%
Number of wire	2	3	33.33%
Part counts	40	183	78.1%
Cost	$19.88	$64.90	69.4%
Size	50.8 × 38.1 mm	76.2 × 50.8 mm	50.0%

Table 8.
Comparison between DDS and DMP PLL.

Table 8 summarizes the improvements between DDS and DMP PLL. The new DDS has taken all consideration in order to ensure that the fundamental performance of DMP PLL remained without degrading the system performance. Besides, huge improvements were achieved. The DMP PLL has an operating range from 2.5 to 40 MHz, while the DDS can go as low as 1.1 μHz where it has been declared as DC. A total of 12% improvement has been achieved. On the other hand, the frequency resolution improved significantly as compared to DMP PLL.

For phase noise, the DMP PLL has a − 80 dBc/Hz, while DDS offers 25% lower than −100 dBc/Hz across temperature. With this achievement, both peak-to-peak and RMS period jitters have been improved by 59.7 and 76%, respectively. This will result in the error and improvement measurement speed by reducing the cyclic redundancy check (CRC). For SFDR, DDS offers 25% of improvement with 70 dBc as compared to DMP PLL with 56 dBc. In the tuning speed, a remarkable 97.7% speed improvement has been achieved by the improvement of communication speed with DDS. This number can go below if future development decides to increase the speed further for faster measurement. Lastly, the part counts, size, and cost were interrelated. The reduction of part counts reduces the space required and, therefore, the cost reduced.

4. Conclusion

By having every piece a part of the design, the DDS core together with the LPF in the design is connected together to perform as a clock source for ADC sampled system. Both simulation and measurement have demonstrated almost identical performance for various sampling frequency ranges across several temperature setups. Overall, the design has achieved a peak jitter of 60.5 ps and RMS of 12 ps across all sampling frequencies. Phase noise has been improved by 20 dB below the original design for a −100 dBc/Hz at 1 kHz frequency offset. Tuning speed has fastened from 4.3 ms down to 100 μs with improvement over communication speed. Total part count has been reduced by 78.1%, and the circuit space shrunk by 50%.

Author details

Desmond Tung and Rosmiwati Mohd-Mokhtar*
School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Nibong Tebal, Pulau Pinang, Malaysia

*Address all correspondence to: eerosmiwati@usm.my

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