Chapter

Line Impedance Emulator: Modeling, Control Design, Simulation and Experimental Validation

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Abstract

The variation of line impedance has always been a great concern for grid operators and industrial users. The problem is that the reliability and quality of the supplied power are influenced by this variation. Indeed, several standards and grid requirements fix strict rules and rigorous standards when connecting or disconnecting from the public grid. In this context, this chapter proposes a full study of a line impedance emulator, which includes the power design and the control. The line impedance emulator is useful for small scale laboratories that develop distributed energy generation. Developed line impedance emulator is based on a three-phase power converter. For these converters, different controls are applied, including proportional integral and resonant controllers. For the generation of voltage reference values that correspond to expected line impedance, two algorithms are studied, namely, trigonometric functions-based algorithm and voltage drop-based algorithm. The theoretical study is supported by simulation and experimental results.

Keywords: power quality, distributed energy generation, microgrid, line impedance emulation, resonant controller

1. Introduction

Nowadays, with the tremendous increase of distributed energy generation (DEG), the concept of power quality (PQ) has become a growing concern for grid operators around the world [1–4]. Many research teams working on this topic are developing small or large-scale DEG laboratories (**Figure 1**) [3–9] as well as algorithms for critical situations is the grid emulator. This grid emulator is also used to confirm the compliance with standards and different grid codes [10–13].

This chapter covers one of the functionalities of the grid emulator, which is the line impedance emulation. Indeed, line impedance deviation can be caused by several circumstances, such as, a remote grid fault, or a connection disconnection of a large load in the distribution network [14].

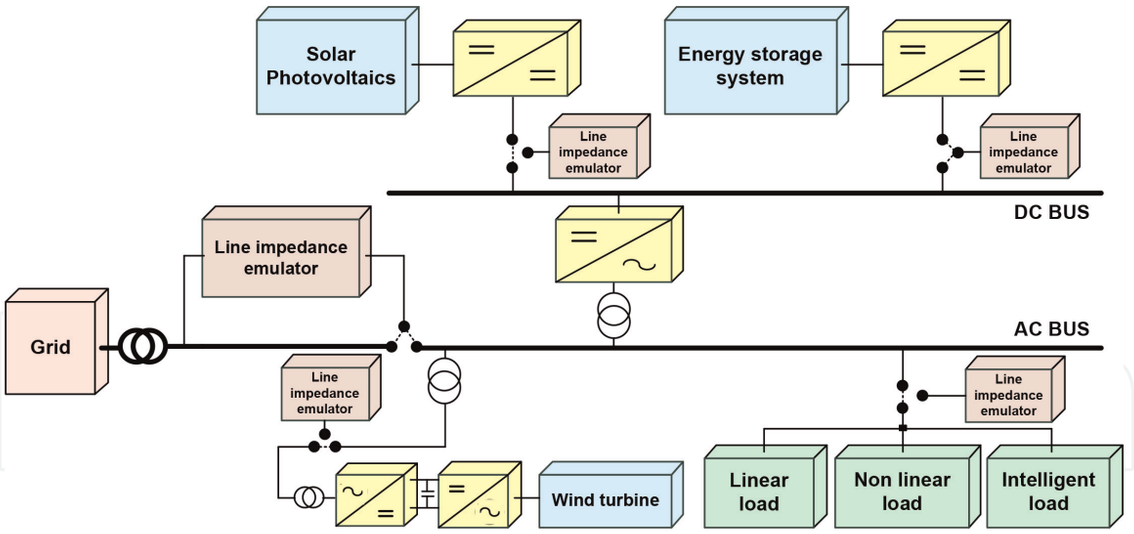

Figure 1.
Example of a microgrid including line impedance emulators.

The line impedance variation is able to considerably affect reactive power sharing between parallel loads [15, 16], and it can also induce operation instability in case of standalone microgrid [17, 19]. In addition, line impedance value has an influence on the quality of voltage and line current in the point of common coupling of the microgrid [19]. In another hand, tests introducing line impedance variation are used for the compliance with many relevant standards especially those dealing with anti-islanding.

This chapter explains in details the steps of the line impedance emulator design based on power converters. Regarding line impedance emulation algorithm, reference voltage values are deduced in view of the phase shift with the input AC grid voltage, according to the equipment under test (EUT) active and reactive power. Presented emulator guarantee flexible tests with decoupled variation range of impedance component.

This chapter first outlines modeling of line impedance emulator, followed by a description of the control methodology for the overall, simulation results and experimental validation are then developed.

2. Line impedance emulator presentation

The line impedance emulator is installed between the grid and the EUT and used for the emulation of variable line impedance. The structure of the studied line impedance emulator system is shown in **Figure 2**. It incorporates two power converters joined by dc-link capacitor: an EUT side converter (EsC) and a grid side converter (GsC). The GsC and the EsC are AC/DC and DC/AC converters, respectively. To mitigate switching harmonics, an LCL filter is employed at the output of the EsC. The EsC control aims to maintain the voltage through the LCL filter capacitor $V_{c(abc)}$ equal to the programmed references. The GsC has the intention of regulating the system power factor (PF) and the voltage at the DC bus V_{dc}. As presented in **Figure 2**, the line impedance emulator output $V_{out(abc)}$ is equal to $V_{c(abc)}$, while its output $V_{in(abc)}$ is considered comparable to the grid voltage $V_{g(abc)}$.

The flowchart of the line impedance emulator process is given by **Figure 3**. The first step of this flowchart consists in initializing the different functions and the microcontroller peripherals such as the ADC, Timers and the General Purpose Input/Output (GPIO) as well as the analog-to-digital conversion of the measured

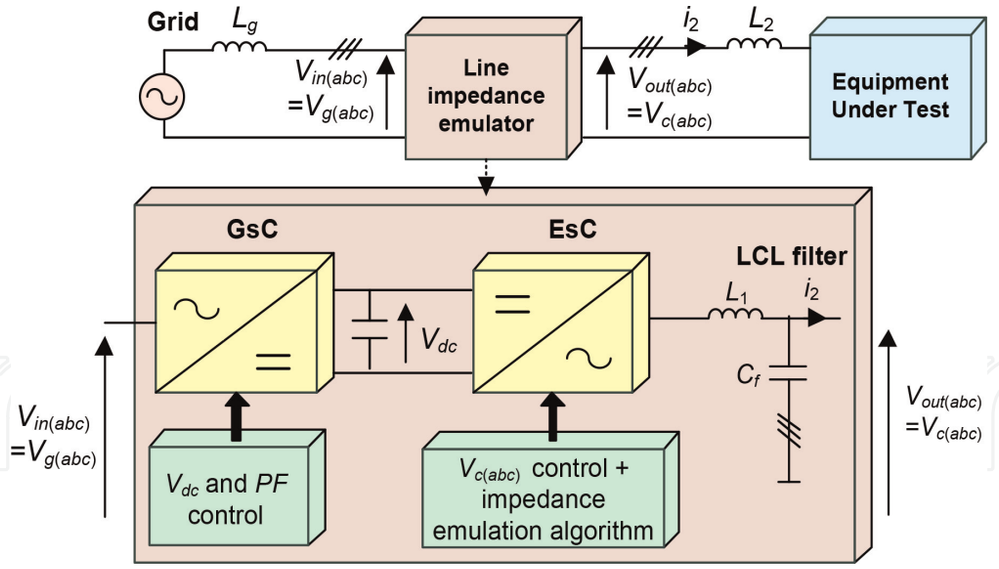

Figure 2.
Power converter-based three-phase line impedance emulator.

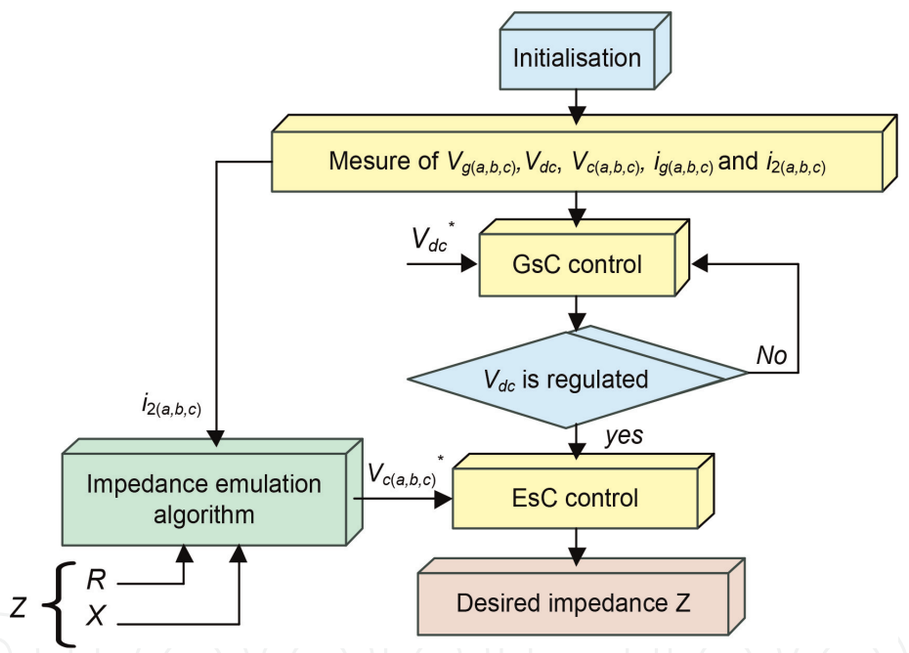

Figure 3.
Line impedance emulator process flowchart.

voltages and currents. The next step is to control of the GsC. The objective of this control is voltage at the DC bus regulation. In parallel with these steps, the impedance emulation algorithm provides the capacitor voltage references $V_{c(a,b,c)}^*$ according to programmed impedance. Once V_{dc} is equal to its reference and the capacitor voltage references $V_{c(a,b,c)}^*$ are generated, the operator proceeds to the control of the EsC. The desired line impedance is consequently achieved.

Figure 4 summarizes the different steps of the line impedance emulator design. As mentioned, the first step consists in modeling the two power converters of the line impedance emulator giving the system equations and transfer functions. After that, the operator selects the appropriate control converters control in terms of dynamic response, THD value, steady state error and sensitivity to perturbation and parametric variation. In this chapter, the control of the line impedance emulator converters employed resonant controllers and PI regulators. This choice is due to

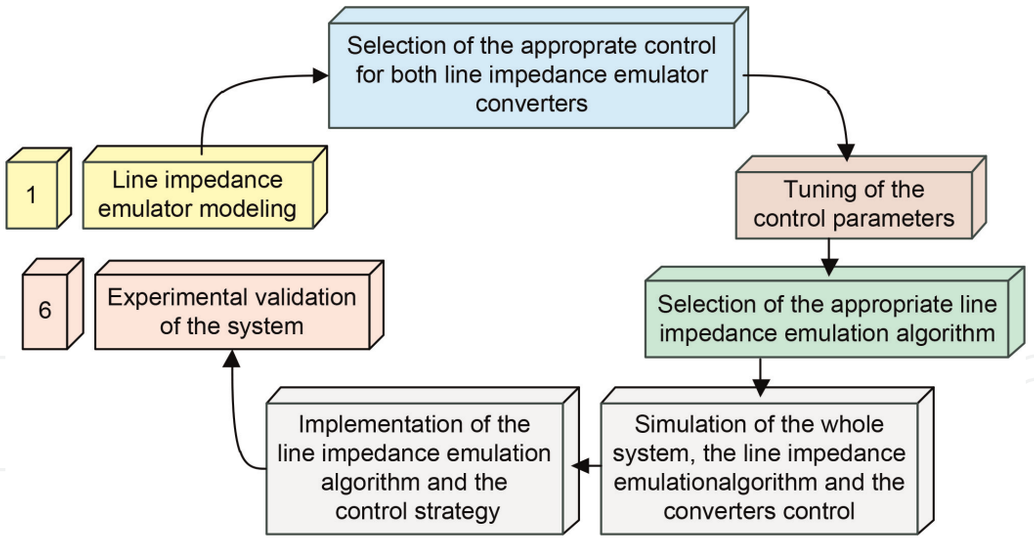

Figure 4.
Methodology of the design of a line impedance emulator.

their simple use (tuning parameters and implementation), while ensuring simultaneously acceptable dynamic response, THD value and steady state error. Then, based on the obtained system transfer functions, the control parameters are deduced. After that, the operator should select the appropriate line impedance emulator algorithm. In this chapter, two impedance emulator algorithms will be presented. The next step of the design methodology consists in simulating the whole system including the power converters, the control strategy and the line impedance emulation algorithm. When the simulation results verify the proper system operation, the control will be implemented on a digital board. The last step of the design methodology consists in the experimental validation of the line impedance emulator.

3. Line impedance emulator modeling

The GsC power circuit single phase representation is depicted on **Figure 5**, where L_g denotes the grid impedance. According to this figure, the GsC electric equation in the *abc* reference frame is given by Eq. (1).

$$U_i = V_g - L_g \frac{di_g}{dt} \tag{1}$$

The EsC power circuit single phase representation is given by **Figure 6**. Based on this Figure, the equations related to the EsC are given by Eq. (2), Eq. (3), Eq. (4) and Eq. (5). The obtained single phase simplified block diagram of the LCL-EsC is depicted on **Figure 7**.

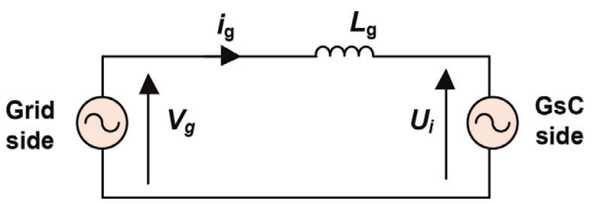

Figure 5.
GsC power circuit.

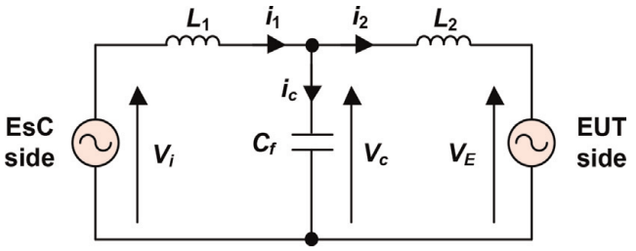

Figure 6.
EsC power circuit single phase representation.

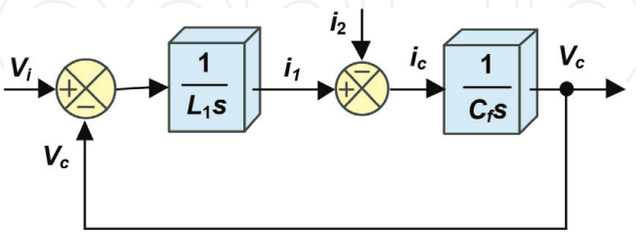

Figure 7.
LCL-EsC simplified block diagram.

$$i_1 = \frac{V_i - V_c}{sL_1} \tag{2}$$

$$i_1 = i_2 + i_c \tag{3}$$

$$V_c = \frac{i_c}{sC_f} \tag{4}$$

$$i_2 = \frac{V_c - V_E}{sL_2} \tag{5}$$

4. Line impedance emulation control

4.1 Grid side converter control

Figure 8 shows the GsC control. It incorporates two control loops. The internal loop controls in the *abc* reference frame the grid currents $i_{g(abc)}$ and it is based on

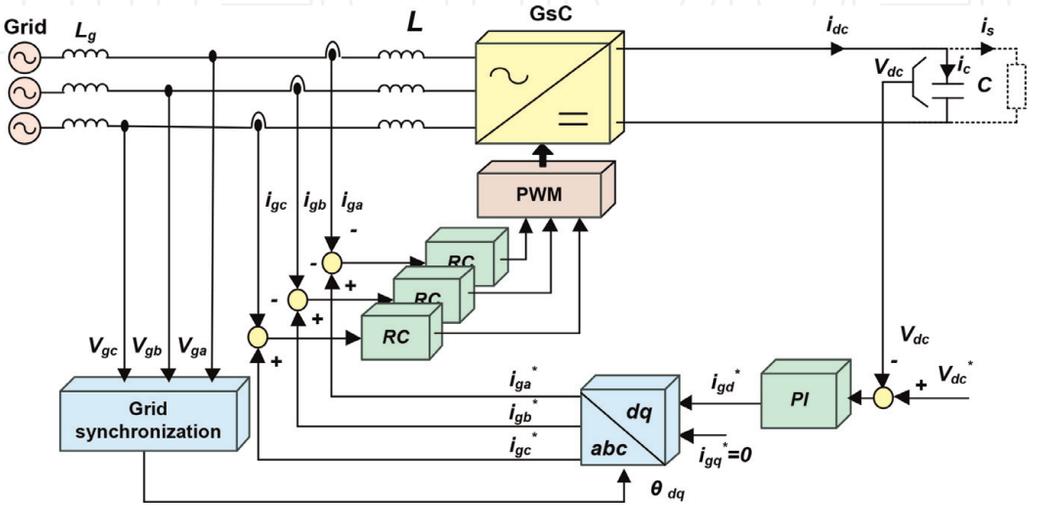

Figure 8.
Block diagram of GsC control.

resonant controller. The external loop regulates, via a PI regulator, the voltage at the DC bus V_{dc} and provides grid current reference on d axis i_{gd}^{*}. The grid current reference on the q axis i_{gq}^{*} is selected to have the desired PF. For the abc grid current reference components $i_{g(abc)}^{*}$, they are obtained via the application of Park transformation to i_{gd}^{*} and i_{gq}^{*}. In the following, the tuning of the PI and the resonant controller parameters will be detailed.

4.1.1 Tuning of the PI regulator of the voltage at the DC bus

Based on **Figure 9**, the current i_{dc} at the output of the GsC is expressed as in Eq. (6). By applying the Laplace transform to Eq. (6), Eq. (7) is obtained.

$$i_{dc} = i_c + i_s = C\frac{dV_{dc}}{dt} + i_s \tag{6}$$

$$V_{dc} = \frac{1}{Cs}(i_{dc} - i_s) \tag{7}$$

Since the current i_{dc} is instantaneously equal to $\pm i_g$ and the current regulation loop time constant is insignificant compared to the one of the DC bus voltage regulation loop, **Figure 9** gives simplified DC bus voltage regulation loop block diagram.

The transfer function of the PI regulator is given by Eq. (8). Based on this equation and neglecting the load current i_s, the closed-loop transfer function of the V_{dc} control is given by Eq. (9).

$$G_c(s) = \frac{i_{dc}^{*}}{\Delta V_{dc}} = K_{pdc} + \frac{K_{idc}}{s} \tag{8}$$

$$\frac{V_{dc}}{V_{dc}^{*}} = \frac{\frac{K_{pdc}}{C}s + \frac{K_{idc}}{C}}{s^2 + \frac{K_{pdc}}{C}s + \frac{K_{idc}}{C}} = \frac{\frac{K_{pdc}}{C}s + \frac{K_{idc}}{C}}{s2 + 2\xi_c\omega_{nc}s + \omega_{nc}^2} \tag{9}$$

The transfer function of Eq. (9) is a second-order system whose denominator can be written in the canonical form of a second-order system given by the right-hand side of Eq. (9). By identifying the terms of Eq. (9), the obtained transfer function is characterized by a damping ratio ξ_c and a natural frequency of oscillation ω_{nc} that satisfy Eq. (10) and Eq. (11).

$$2\xi_c\omega_{nc} = \frac{K_{pdc}}{C} \tag{10}$$

$$\omega_{nc}^2 = \frac{K_{idc}}{C} \tag{11}$$

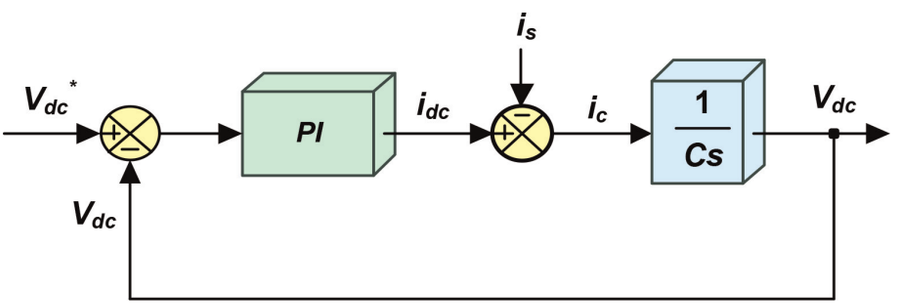

Figure 9.
DC bus voltage regulation loop simplified block diagram.

Then, the form and the dynamics of the response of the DC bus voltage V_{dc} are imposed by setting the natural frequency of the oscillations ω_{nc} and a damping coefficient ξ_c. Thus, the gains K_{pdc} and K_{idc} can be obtained based on equations Eq. (12) and Eq. (13).

$$K_{pdc} = 2C\xi_c\omega_{nc} \tag{12}$$

$$K_{pdc} = C\omega_{nc}^2 \tag{13}$$

4.1.2 Tuning of the resonant controller of the grid side current

The use of the PWM makes it possible to have a fundamental of the voltage U_i equal to its reference U_i^*. Thus, based on Eq. (1), we obtain the simplified single-phase block diagram the grid side regulation loop given by **Figure 10**.

Considering **Figure 10**, the closed-loop system transfer function (T_{cig}) is given by Eq. (14).

$$T_{cig}(s) = \frac{i_g(s)}{i_g^*(s) - i_g(s)} = \frac{K_{pig}s^2 + K_{iig}s + K_{pig}\omega_0^2}{L_g s^3 + K_{pig}s^2 + (L_g\omega_0^2 + K_{iig})s + K_{pig}\omega_0^2} \tag{14}$$

For the synthesis of the resonant controller parameters, we consider the pole placement method and more precisely the Naslin criterion [20–21]. The n order polynomial of this criterion is expressed by Eq. (15).

$$P_{Naslin}(s) = n_0\left(1 + s\tau + s^2\left(\frac{\tau^2}{\alpha}\right) + s^3\left(\frac{\tau^3}{\alpha^3}\right) + \ldots\ldots + s^n\left(\frac{\tau^n}{\alpha^{n(n-1)/2}}\right)\right) \tag{15}$$

From Eq. (14), we deduce the system characteristic polynomial given by Eq. (16).

$$P_{ig}(s) = L_g s^3 + K_{pig}s^2 + (K_{iig} + L_g\omega_0^2)s + K_{pig}\omega_0^2 \tag{16}$$

The identification between the system characteristic polynomial P_{ig} and the second order Naslin polynomial makes it possible the deduction of resonant controller parameters K_{pig}, et K_{iig} as shown in Eq. (17) and Eq. (18).

$$K_{pig} = L_g\frac{\alpha^2}{\tau} \tag{17}$$

$$K_{iig} = L_g\left(\frac{\alpha^3}{\tau^2} - \omega_0^2\right) = L_g(\alpha^2 - 1)\omega_0^2 \tag{18}$$

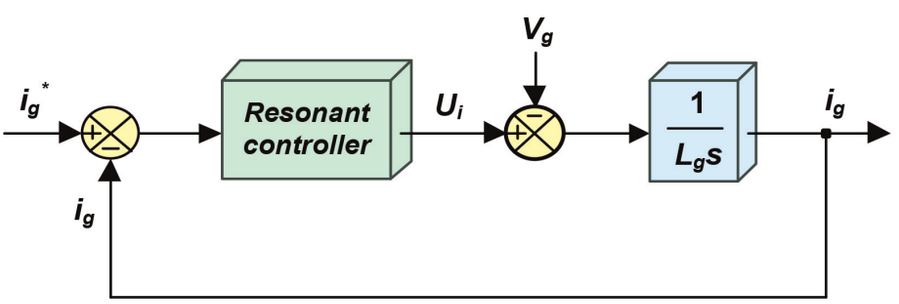

Figure 10.
Grid current regulation loop simplified block diagram.

4.2 EUT side converter control

The control based on resonant controller for the EsC is depicted on **Figure 11**. This control includes an external and an internal loops. The external one controls the voltages through the filter capacitor $V_{c(a,b,c)}$. The internal one controls the inverter side current $i_{1(a,b,c)}$ and generates then the inverter voltages references $V_{i(a,b,c)}$. For the external loop, a resonant controller is adopted. For the internal loop, the resonant controller is replaced by a constant gain (G) in order to ensure a faster loop than the external one. In the following, the tuning of the resonant controller parameters will be detailed and discussed in order to ensure good control performances.

4.2.1 Tuning of the resonant controller of the voltage through the LCL filter capacitor

For reasons of simplification, it is assumed that the internal loop of the current is faster than the external loop of the voltage. Thus, we can approximate it equal to the unity by associating the PWM function. Consequently, the block diagram of the voltage regulation loop is given by **Figure 12**.

Hence, the closed loop system transfer function (T_c) is given by Eq. (19).

$$T_c(s) = \frac{V_c}{V_c^*} = \frac{a_{2c}s^2 + a_{1c}s + a_{0c}}{C_f s^3 + a_{2c}s^2 + \left(C_f\omega_0^2 + a_{1c}\right)s + a_{0c}} \tag{19}$$

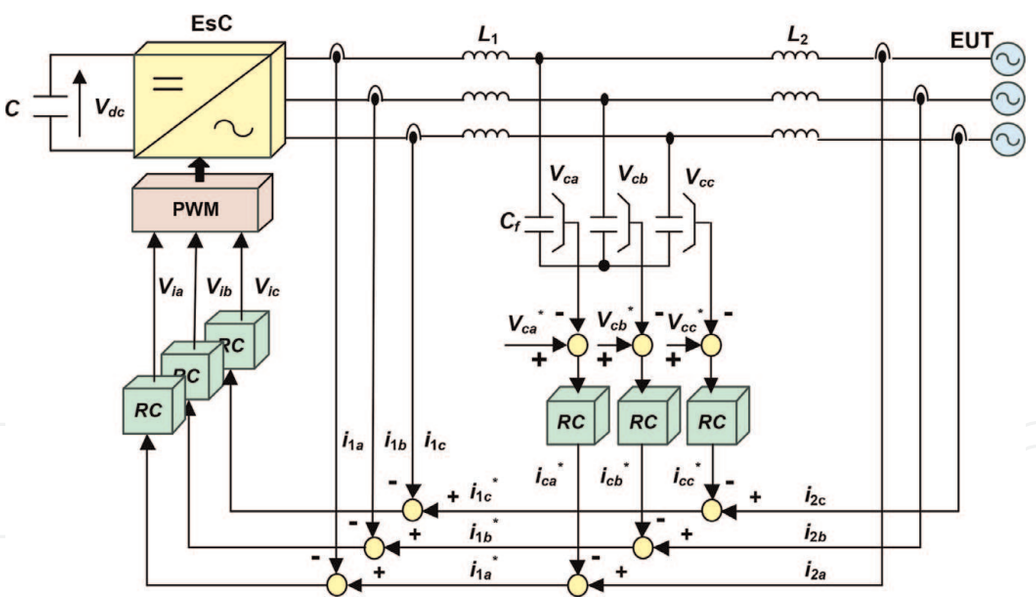

Figure 11.
Block diagram of the EsC control.

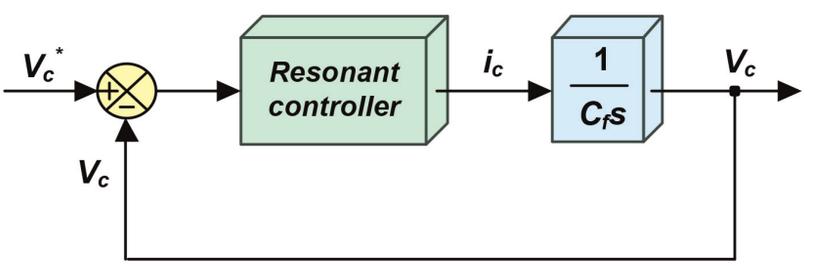

Figure 12.
Voltage regulation loop simplified block diagram.

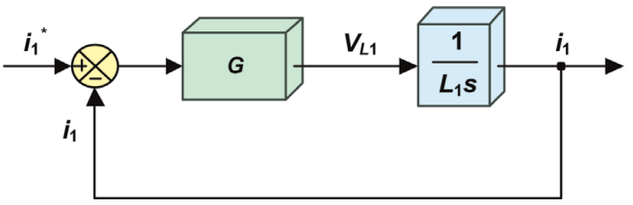

Figure 13.
Current regulation loop simplified block diagram.

The method chosen for the computation of the resonant controller parameters is based on the generalized stability criterion [22]. In this case, the n order polynomial is expressed as in Eq. (20).

$$P_{GSC}(s) = \lambda(s+r)\prod_{i=1}^{n}[(s+r+j\omega_i)(s+r-j\omega_i)] \quad \{\lambda, r, \omega_i \in \Re;\ \ i, n \in N\} \tag{20}$$

On the other hand, based on Eq. (19), the system characteristic polynomial P_c is given by Eq. (21).

$$P_c(s) = C_f s^3 + a_{2c}s^2 + \left(C_f\omega_0^2 + a_{1c}\right)s + a_{0c} \tag{21}$$

The identification of P_c and second order generalized stability criterion polynomial allows the deduction of the resonant controller parameters as shown in Eq. (22).

$$\begin{cases} a_{2c} = 3r_c\lambda_c \\ a_{1c} = \lambda_c\left(3r_c^2 + \omega_i^2\right) - C_f\omega_0^2 \\ a_{0c} = \lambda_c\left(r_c^3 + r_c\omega_i^2\right) \\ Avec\ \ \lambda_c = C_f \end{cases} \tag{22}$$

4.2.2 Tuning of the gain of the current i_1

The simplified internal current regulation loop block diagram is given by **Figure 13**.

Hence, the transfer function of the closed-loop system $T_{i1}(s)$ is given by Eq. (23).

$$T_{i1}(s) = \frac{i_1(s)}{i_1^*(s)} = \frac{1}{\frac{L}{G}s+1} = \frac{1}{1+\tau_c s} \quad \text{where } \tau_c = \frac{L_1}{G} \tag{23}$$

G is chosen so that the real part of the inverse of the closed-loop time constant $(1/\tau_c)$ is greater than the stability margin chosen for the synthesis of the voltage external loop in order to ensure that the internal loop is faster than the external one.

5. Line impedance emulation algorithms

In this section, two methods of the line impedance emulator algorithm synthesis are presented: the trigonometric functions-based algorithm and the voltage drop-based algorithm.

5.1 Trigonometric functions-based algorithm

The impedance emulation conception is based on the phasor diagram depicted on **Figure 14** According to this Figure, the apparent power S is expressed as in Eq. (24).

$$S = V_g I^* = V_g \left(\frac{V_g - V_c}{Z}\right)^* = \frac{V_g^2}{Z} e^{j\theta} - \frac{V_g V_c}{Z} e^{j(\theta+\delta)} \tag{24}$$

According to **Figure 14**, the reactive power Q and active power P are given by Eqs. (25) and (26), respectively. These equations allow the deduction of tanδ and the voltage magnitude V_{out} given, respectively, by Eqs. (27) and (28). On the other hand, the Q and P can be also written as a function of $\alpha\beta$ output current and voltage components as shown in Eqs. (29) and (30), respectively.

$$Q = \frac{V_g}{R^2 + X^2}\left[-RV_c \sin\delta + X\left(V_g - V_c \cos\delta\right)\right] \tag{25}$$

$$P = \frac{V_g}{R^2 + X^2}\left[R\left(V_g - V_c \cos\delta\right) + XV_c \sin\delta\right] \tag{26}$$

$$tan\delta = \frac{PX - QR}{V_g^2 - (PX + QR)} \tag{27}$$

$$V_c = \frac{PX - QR}{V_g \sin\delta} \tag{28}$$

$$Q = \frac{3}{2}\left(V_{c\beta} i_{2\alpha} + V_{c\alpha} i_{2\beta}\right) \tag{29}$$

$$P = \frac{3}{2}\left(V_{c\alpha} i_{2\alpha} + V_{c\beta} i_{2\beta}\right) \tag{30}$$

Figure 15 shows the trigonometric-based line impedance emulation algorithm. The first step consists in measuring the grid voltage $V_{g(a,b,c)}$ and computing its RMS value. From the obtained value, we compute the phase shifting δ relatively to the grid voltage. After that, the emulated impedance is computed based on the previous equations.

5.2 Voltage drop-based algorithm

This algorithm is based on a voltage drop V_v that matches with the emulated line impedance Z as shown in **Figure 16** This voltage is a function of programmed inductance and resistance variations as presented in Eq. (31). The voltage drop-based line impedance emulator algorithm is presented in **Figure 17**.

$$V_v = Zi_2 = (R + jX)i_2$$

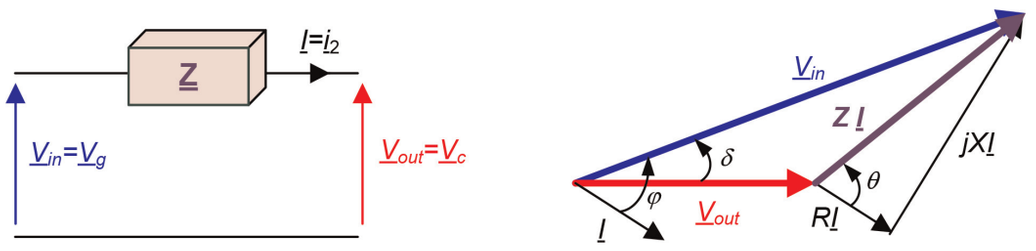

Figure 14.
Line impedance and phasor diagram.

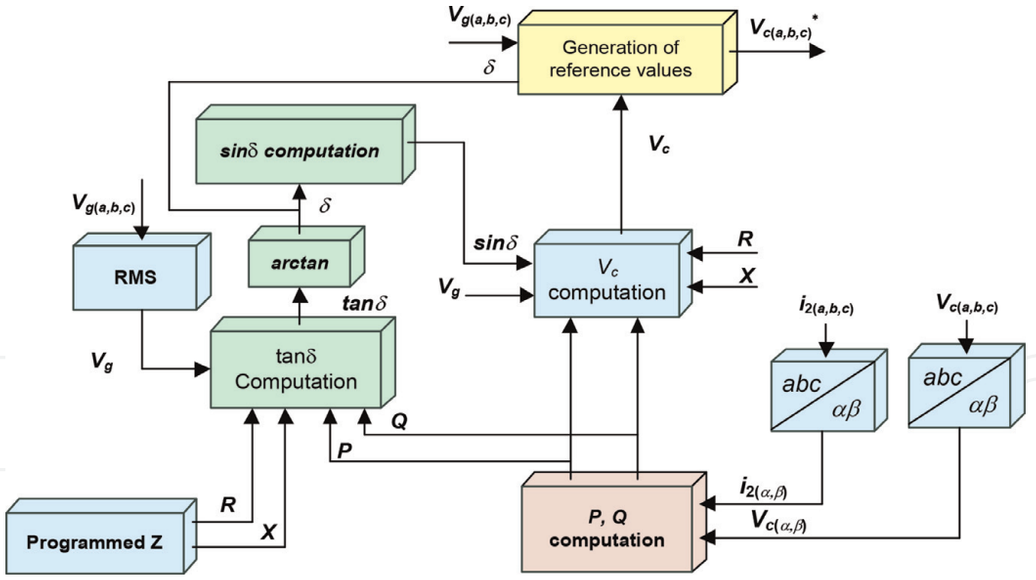

Figure 15.
Line impedance emulator algorithm-based trigonometric functions.

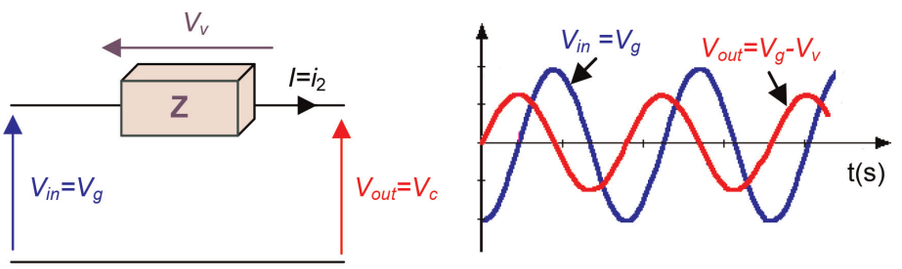

Figure 16.
Voltage drop line impedance emulator principle.

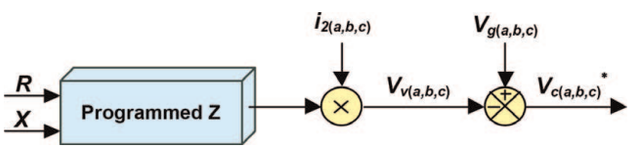

Figure 17.
Reference voltage according to fixed line impedance.

6. Simulation and discussion

Simulation tests were performed under PSIM software. The proposed control was applied to a 20kVA line impedance emulator. **Table 1** gives the line impedance emulator parameters. In **Figure 18** is presented the V_{dc} response to a step reference of 100 V. Based on this result, the steady state error of the V_{dc} voltage becomes null in the steady state, which prove that this voltage is well regulated. **Figure 19** shows that the voltage $V_{c(abc)}$ is well regulated in both transient and steady state operation even reference magnitude change at 0.9 s. To show the voltage drop-based line impedance emulation algorithm performances, a control scenario is presented in **Figure 20**. This scenario consists in imposing in the interval [0, 1 s] equivalent real impedance in series with L_2 and in the interval [1 s, 1.5 s] the line impedance emulator is activated. **Figure 21** shows results for a line impedance Z characterized by X = 1.5 Ω and R = 1 Ω in case of real and emulated impedance. As shown in this figure, the same current value is generated for real and programmed line impedances.

Description		Symbol	Value	Unit
Nominal voltage line-line		V_g	400	V
GsC nominal power		$SGsC_{nom}$	20	kVA
EsC nominal power		$SEsC_{nom}$	20	kVA
LCL filter	Converter side inductor	L_1	2	mH
	EUT side filter inductor	L_2	2	mH
	Capacitor	C_f	30	μF
Switching frequency		f_s	10	kHz

Table 1.
Line impedance emulator parameters.

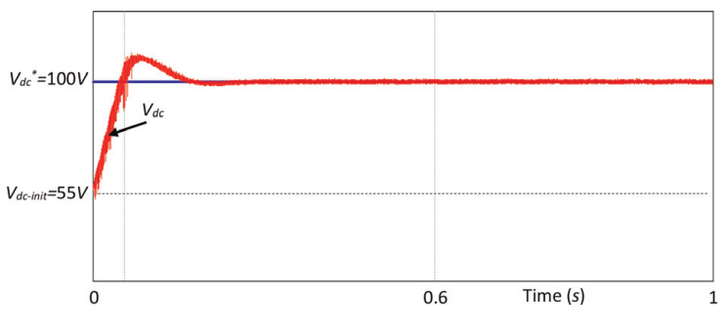

Figure 18.
V_{dc} response to a step reference of 100 V.

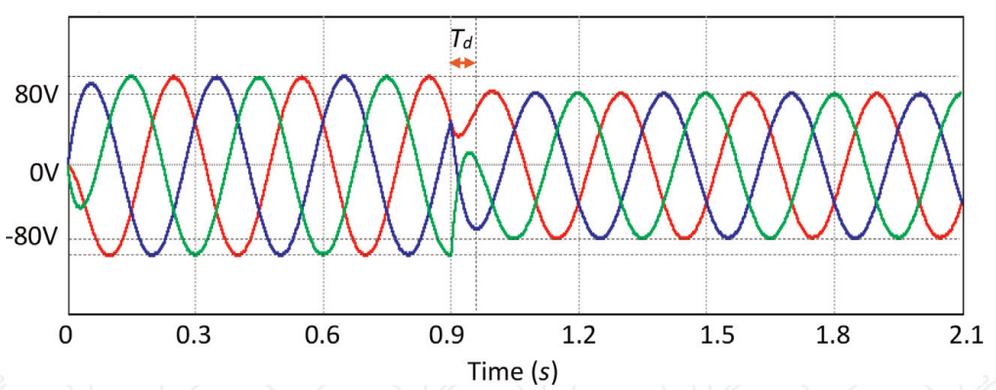

Figure 19.
Line impedance emulator output in case of voltage reference magnitude change.

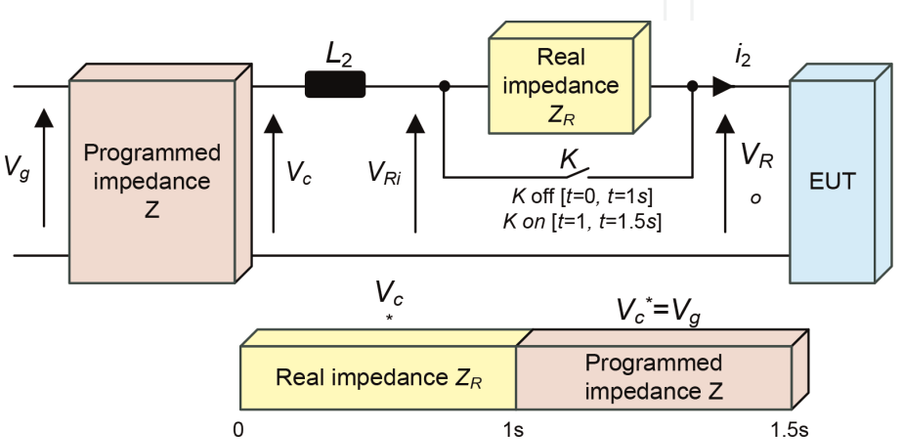

Figure 20.
Simulation control scenario.

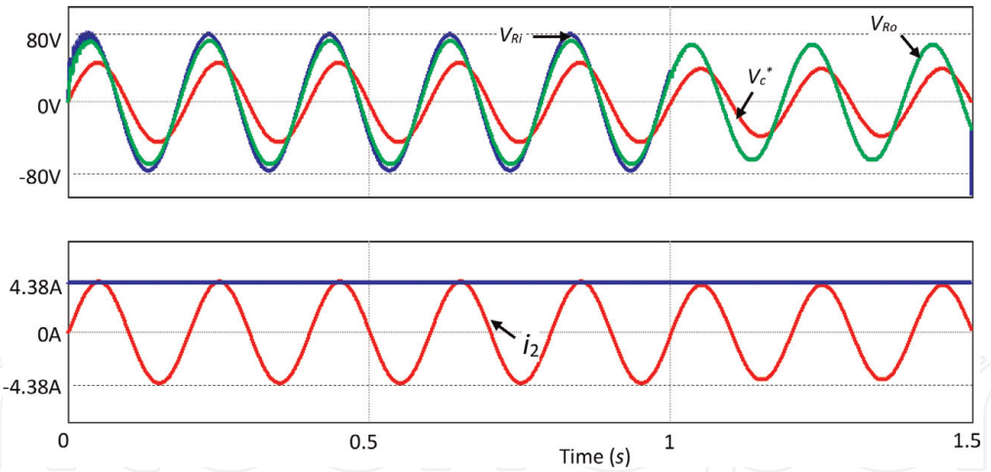

Figure 21.
System output for real and programmed impedance for X = 1.5 Ω and R = 1 Ω.

7. Experimental validation

Figures 22 and **23** show the experimental prototype and the test bench for the line impedance emulator. It includes (1) an auto transformer used in order to vary the voltage peak magnitude; (2) an L filter (composed of three inductors (20 mH/20A)

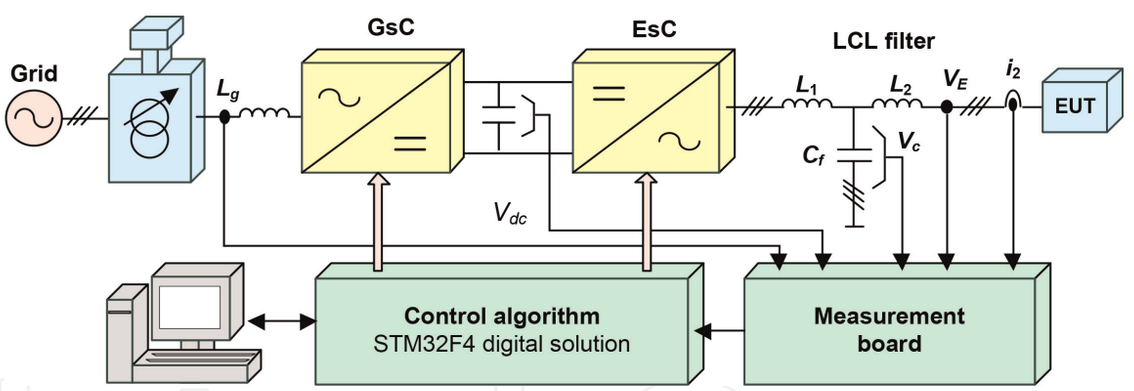

Figure 22.
Experimental prototype.

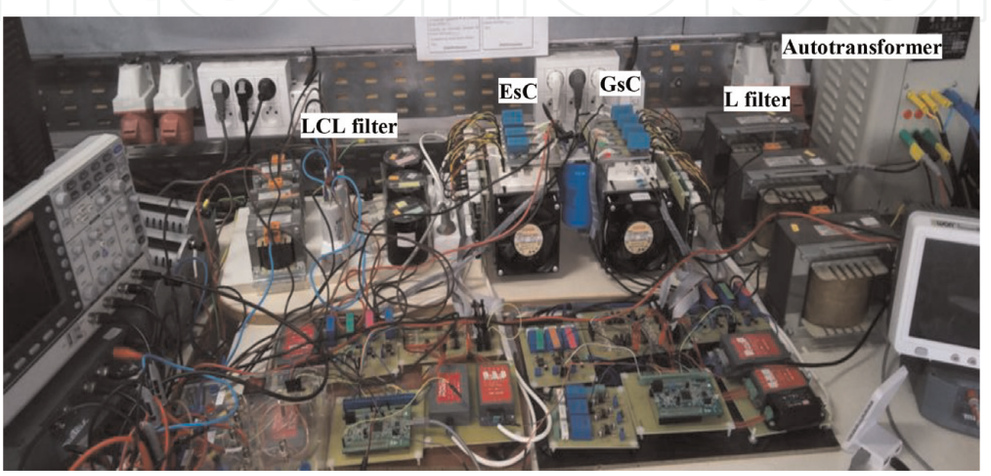

Figure 23.
Experimental test bench.

with 0.3 Ω internal resistors; (3) a 20 kVA AC/DC converter (GsC); (4) a dc-link capacitor (1100 μF/800 V); (5) a 20 kVA DC/AC converter (EsC); (6) an LCL filter (composed of three inductors (2 mH/10 A) with 0.1 Ω internal resistors, three capacitors (4 μF/400 V) and three inductors (2 mH/10A) with 0.1 Ω internal resistors); (7) a measurement board (LEM LA55 and LEM LV25 for currents and voltage measuring, respectively); and (8) the STM32F4-Discovery digital solution. It is worth noting here that two STM32F4-Discovery cards were used in the experimental test bench; the first one is dedicated to the GsC control and the second one is dedicated to the EsC control.

For both GsC and EsC controls, the switching frequency was fixed equal to 10 kHz. For experimental tests, the switching frequency is equal to 10 kHz, the voltage at the DC bus V_{dc} is initially charged at 55 V. **Figure 24** presents the voltage at the DC bus V_{dc} response. As shown is this figure, V_{dc} is well controlled during steady state operation. **Figure 25** presents the response of the line impedance emulator output for a reference change from 20 to 10 V. This test shows that the EsC control ensures an acceptable dynamic response and it is well controlled at steady state. **Figure 26** presents the line impedance emulator input and the output that matches with various values of line impedance.

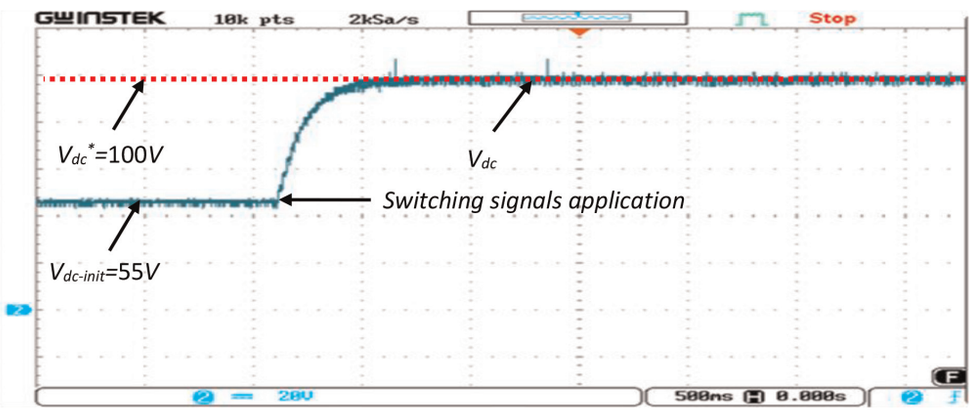

Figure 24.
DC bus measured voltage and reference values.

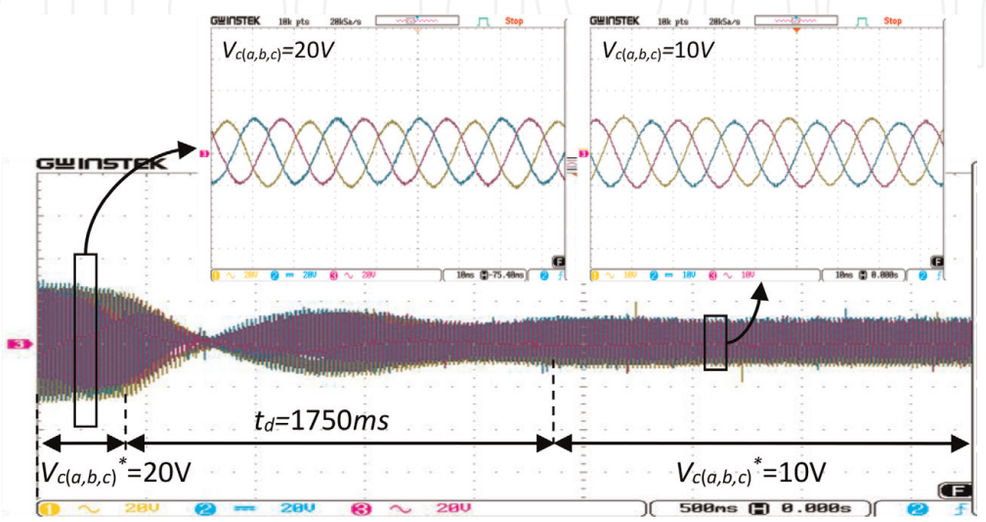

Figure 25.
Emulator output voltage $V_{c(abc)}$ for voltage reference change from 20 to 10 V.

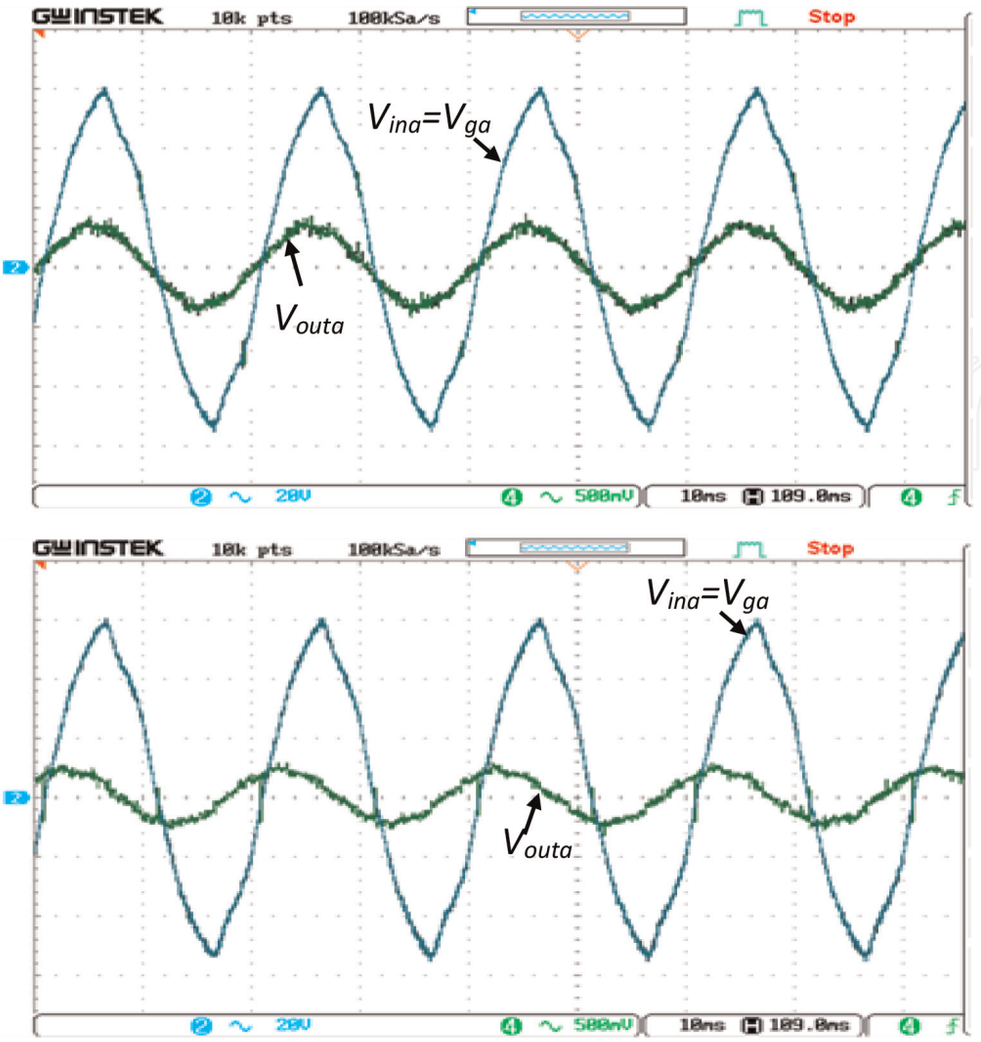

Figure 26.
Line impedance emulator input V_{ina} and output V_{outa} for different values of R and L.

8. Conclusion

In this chapter, line impedance emulator was studied. This equipment is used in small scale laboratories studying distributed energy generation. It ensures power tests with variable line impedance. Presented line impedance emulator is based on two power converters connected via a dc-link capacitor. Theoretical study is detailed and validated by simulation and experimental tests. The proposed study describes in detail the control design of each power converter. In addition, two variants of line impedance emulator algorithms were synthesized. To prove the efficiency of the presented study, a test with a real impedance and an emulated one was performed and obtained results show the similarity of system responses with both equipment.

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