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New Material for Si-Based Light Source Application for CMOS Technology

Luong Thi Kim Phuong

Abstract

In this chapter, an approach to enhance the radiative recombination of the Ge film grown on the Si substrate is presented. The Ge band gap structure could be modified by applying a tensile strain and high n-doping in the Ge epilayers. It thus becomes a direct band gap material with high photoluminescence efficiency which is compatible with mainstream silicon technology. The interdiffusion effect between Ge film and Si substrate is also mentioned in this section. We proposed a new method to suppress the Si/Ge interdiffusion to reduce the effect of Si atoms on the optical property of Ge film due to Si presence.

Keywords: Ge, Si technology, tensile strain, n-doping, photoluminescence, interdiffusion

1. Introduction

During the last decades, demands for increased performance of electronic devices have led to an extraordinary course of miniaturization of Complementary Metal Oxide Semiconductor (CMOS) devices. As this scaling law may soon reach its limit, researchers in modern microelectronics try to find solutions to extend Moore's law by using more conventional principles. Two major areas of research have been envisaged. The first aims to find solutions that will rely on the exiting existing technology and physical principles but on a smaller scale. As such, bottom-up nanoscale structures, such as semiconducting nanowires, carbon nanotubes or graphene, have been proposed as potential candidates for complementing Si technology. The second explores new concepts, which rely on introduction of novel functions, such as the development of on-chip optical interconnects or the introduction of spintronic devices in which not only the electron charge but also the electron spin that can carry information. On-chip optical interconnects imply integration of all the optical devices with the silicon microelectronic devices on silicon chips and they require an efficient Si-based optical source. In addition to the development of new generations of high-performance computation and communication systems, an integrated efficient optical source on silicon allows to bridge the gap between the microelectronic and optoelectronic industries. A Si-based optical source would allow developing silicon photonics and its diffusion toward extended new markets. It would also allow opening new possibilities with a strong economic potential by developing cost-effective devices intended for a large public diffusion. To date, numerous

approaches have been proposed to realize silicon-integrated optical sources, such as porous Si, epitaxial semiconducting silicides, Er-doped Si, Si nanocrystals or Ge/Si self-assembled quantum dots. However, all above approaches are challenged by the lack of enough gain to surpass materials losses to achieve net gain for laser action.

Semiconductor diode lasers are conventionally based on direct band gap materials due to the efficient radiative recombination of direct gap transitions. As discrete devices, direct gap III-V semiconductor lasers have achieved great success in many important applications, from telecommunications to DVD players. On the other hand, indirect semiconductors such as Si and Ge are traditionally considered unsuitable for laser diodes because the radiative recombination through indirect transition is inefficient as a result of a phonon-assisted process. However, compared to Si, pure Ge displays unique optical properties, the direct (Γ) valley of its conduction band is only 0.14 eV above the indirect (L) valleys at room temperature while it is larger than 2 eV in Si. In addition, while Si cannot be used for photodetector due to its transparency at near infrared wavelength band, Ge has strong direct band gap absorption below 1.55 μm and high-speed Ge photodetectors have been demonstrated. Of particular interest, it has been shown that application of a tensile strain in Ge allows lowering the energy difference between the Γ zone center valley and the indirect L valley. The tensile strain also lifts the degeneracy between heavy hole and light hole valence bands. On the other hand, n-type doping of Ge leads to a more efficient population of the zone center Γ valley and thus enhances optical recombination at the Brillouin zone center. The combination of both effects is expected to lead to significant optical gains at room temperature and to the demonstration of a laser.

Tensile strain can be induced in Ge via several approaches: applying external mechanical stress, growing Ge on a larger lattice parameter substrate, such as InGaAs or GeSn buffer layers, or use of thermal mismatch between Ge and Si. In the frame of this chapter, we have chosen to study tensile-strained and n-doped Ge layers epitaxially grown on Si. The motivation of our study is that this system is compatible with the mainstream Si technology. Concerning to the n-doping process, while in CVD, PH_3 molecules are currently used as a precursor for n-doping, by means of MBE we could implement a specific doping cell using a GaP decomposition source to produce diphosphorus (P_2) which has a higher sticking coefficient than tetrahedral white phosphorus (P_4 molecules).

1.1 The Moore's law or the scaling-down law

Integrated circuits (ICs, also known as microchips or microcircuits) have been a major driving force to revolutionize electronic technology in the past few decades. ICs are nowadays used in almost all electronic equipment and devices and are the foundation of the current generation of computers. An IC is a miniaturized electronic circuit consisting of active devices, i.e., transistors and diodes, as well as interconnects elements or passive components (resistance and capacity). Among all these semiconductors, silicon (Si) is absolutely the most important and widely used material in the IC and semiconductor industry owing to its superior properties and low fabrication cost. Before 2005, silicon IC had been developed in an extraordinary pace for almost four decades, known as Moore's law that the number of transistors in an integrated circuit doubles roughly every 18 months [1]. Upon the increase of the number of transistors, each transistor also gets smaller, faster and cheaper. The scalability is the main reason of the tremendous success of many Si IC based technologies, such as Si complimentary metal-oxide-semiconductor (CMOS) technology, which is used to fabricate the central processing unit (CPU) of modern computers. The scalability of Si-CMOS technology is not only about the shrinkage of the dimensions of the devices, but also a number of other factors for maintaining

the power density while boosting the performance. For an ideal constant-field scaling [2], upon the shrinkage of all the physical dimensions by α (scaling factor), the depletion depth d also has to be shrunk by α to assure the device works properly. The reduction of the depletion depth requires the increase of doping N_d and the decrease of the applied voltage V by a same factor α since $d \approx \sqrt{N_d V}$ [3]. A direct consequence of the scaling is the increased circuit density by α^2 , which dramatically reduces the manufacturing costs. A second important result is the increase of the circuit speed due to both the reduced transit time in transistors and the capacitance in RC delay. However, the applied voltage is found to be impossible to scale by α as continuously shrinking the dimensions because of constraints on the threshold bias in order to avoid rising standby power in the “off” state. Eventually, the applied voltage cannot be scaled anymore, which, unfortunately, already occurred a couple of years ago. This results in the increase of the electric field with the scaling, leading to the increase of the power density of the circuit. It has been shown that the passive power density becomes dominant below the device dimension of 130–65 nm regime [4], which effectively breaks off traditional scaling in CMOS.

In order to further increase the clock frequency without the help of the scaling, the entire architecture should be re-examined. In today’s CMOS technology, the intrinsic speed of the transistor is beyond the speed in any other components of the circuit. The intrinsic frequency of a commercial logic circuit transistor is in the order of 102 GHz [5], while other technologies can easily achieve even higher speed, such as SiGe transistors at 500 GHz [6]. Therefore, the speed bottleneck of the ICs results from propagation delay in the passive components, which is dominated by RC (resistance capacitance) delay. Thus, design a new interconnects system in ICs becomes the key to further enhancement of the speed. A couple of approaches have been investigated to replace the predominant aluminum (for electrical conduction) and silicon oxide (SiO_2 , for electrical insulation) interconnects including the use of copper and low- k dielectric materials (such as doped SiO_2 or polymeric dielectrics) to reduce the RC product.

Among all these attempts, the optical interconnect design implemented by silicon photonics is extremely promising and can be the potentially ultimate solution to this problem. As shown in **Figure 1**, according to the 2008 International Technology Roadmap for Semiconductors (ITRS) [5], with continued technology node scaling, the relative delay for logic devices and local interconnects decreases. However, global interconnects, especially global interconnects without repeaters, show a dramatic increase in delay time. All of these arguments show that the on-chip interconnects are one of the major challenges for the future IC industry.

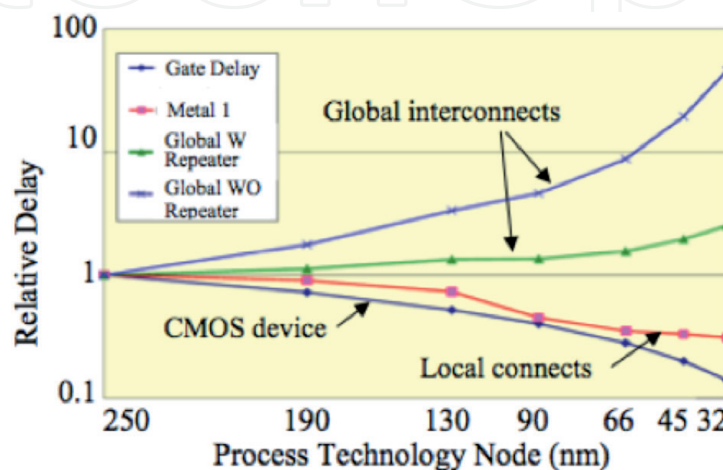


Figure 1.
Relative delay vs. process technology node from 2008 ITRS [5].

1.2 Silicon photonics

1.2.1 Photonics in optical communications

Photonics is about the science and the technology of generating, manipulating, and detecting photons. Silicon, while dominating the semiconductor electronics for decades, is naturally a challenge for developing photonics in many communication applications [7]. Silicon photonics offer a promising platform for the monolithic integration of optics and microelectronics, aiming for many applications including the optical interconnects solution to the microelectronics bottleneck [8]. Because of its importance and rapid growth, a roadmap of silicon photonics, assessed by academic and industrial experts, has been proposed [9]. Light or photon has been used to transmit information for over three decades, mainly by using optical fibers to form optical interconnection between places in distance. In the past three decades, photons have been widely used in optical fiber communication systems, especially in long-distance communications. The fundamental reason for the optical interconnect advantage is the zero rest mass of a photon, which can greatly reduce the required energy. In addition, compared to electrical interconnections, the most important advantage using optical fiber communications is the high speed. However, many challenges need to be solved to achieve on-chip optical interconnects. The first issue is to integrate all the optical devices with the silicon microelectronic devices on silicon chips. Another challenge is materials used in each device. For traditional optical components, III-V materials, such as GaAs and InP, are exclusively used due to their excellent optical properties. However, all the materials and their fabrication are not compatible with the Si exciting Si-CMOS technology.

1.2.2 Key devices for Si photonics

The on-chip interconnect system contains an integrated light source, a modulator to transfer the electrical signal to an optical signal, a waveguide or waveguide device to direct the optical signal to the destination, and finally a photodetector to convert the optical signal back to an electrical signal. Most of these devices are already developed on a Si platform with high bandwidth capability.

Figure 2 Si photonics key devices are needed to realize on-chip optical interconnects: Integrated light source, modulator, waveguide and photo-detector [10]. The only missing key device is an electrically pumped laser source, which is the compatible with the integrated CMOS technology. As we have mentioned above, numerous approaches have been investigated, including porous Si, semiconducting silicides, Er-doped Si, Si nanocrystals or Ge/Si self-assembled quantum dots but none of them could produce a high emission efficiency at room temperature. From the material point of view, in order to achieve a CMOS compatible light source, the

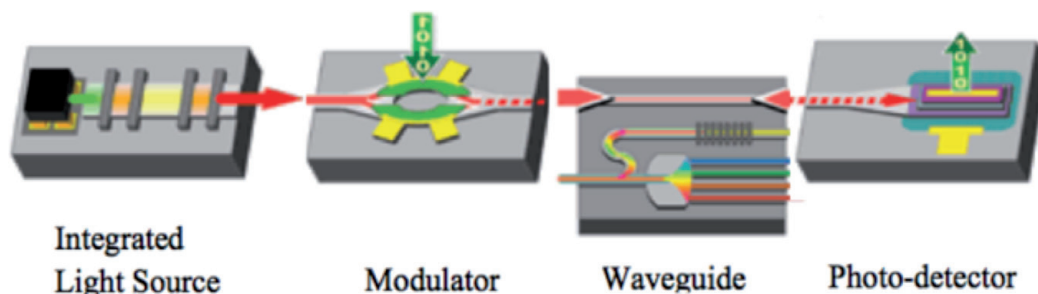


Figure 2. Illustrates several key photonics devices needed to realize Si on-chip interconnections [10].

use of group IV materials (such as Si, Ge, or Sn) is highly expected. In order to have an efficient light source, a direct band gap semiconductor is preferred. At least, a local minimum at the Γ point of the conduction band is required to accumulate electrons and achieve efficient radiative recombination. This requirement makes Si impossible to be an efficient light source because the difference between the direct and indirect valleys in Si is larger than 2 eV. Fortunately, germanium, which is a group IV material, has a local minimum at the Γ point of the conduction band. More attractively is that the lowest energy point in the Ge conduction band is at the L point, which is only 0.140 eV lower than the lowest energy at the Γ point at room temperature. Therefore, Ge has the potential to be engineered to become a direct band gap material and used as an on-chip integrated light source [11, 12].

1.3 Ge band structure engineering

As previously discussed, Ge is the most interesting group-IV material for the light emitting process. However, achieving direct band gap in Ge and improving the Ge light emitting efficiency are still huge challenges. Indeed, Ge is normally recognized as a poor light emitting material due to its indirect band structure. The radiative recombination through the indirect band-to-band optical transition is inefficient as a result of a phonon-assisted process. The direct band-to-band optical transition in Ge is however a very fast process with a radiative recombination rate of 4–5 orders of magnitude higher than that of the indirect transition [13]. Thus, the direct gap emission

Of Ge can be, in principle, as efficient as that from direct gap III-V materials. The challenge is that the number of the electrons for the direct optical transition is deficient due to an indirect band structure. Fortunately, Ge is a pseudo direct band gap material because of a small energy difference (140 meV) between its direct gap and indirect gap. It has been shown that with a combination of tensile strain and n-type doping Ge can be engineered to be a direct band gap material.

1.3.1 Ge band structure at equilibrium and under injection

The band structure of bulk Ge is shown in **Figure 3**. The valence band is composed of a light-hole band, a heavy-hole band, and a split-off band from spin-orbit interaction. The light-hole band and the heavy-hole band are degenerate at wave vector $k = 0$ or Γ point, which is the maximum of valence band.

The lowest energy point of the conduction band is located at $k = \langle 111 \rangle$ or L point. The energy difference between the conduction band at L point and the valence band at Γ point determines the narrowest band gap in Ge:

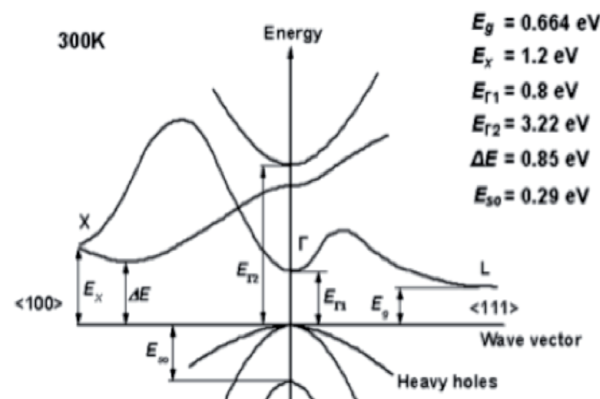


Figure 3.
 Ge band structure at 300 K.

$E_g = 0.664$ eV. Because the direct energy gap E_{Γ_2} is much larger than E_{Γ_1} and E_g , almost no electrons can occupy such high energy levels. Therefore, we refer direct band gap only to E_{Γ_1} throughout this thesis. The part of the conduction band near Γ point is called direct valley and the part near L point is called indirect valley. Since the energy is 4-fold degenerate with regard to the changes of the secondary total angular-momentum quantum number, four L valleys are considered.

Figure 4 shows the electron and the hole distributions of Ge at equilibrium and under injection conditions. At equilibrium, most of the thermally activated electrons occupy the lowest energy states in the indirect L valleys while it is worth noting that in a direct band gap material such as GaAs or InGaAs most of the electrons stay in the direct Γ valley.

Under injection conditions, there are a non-negligible amount of electrons in the Γ valley owing to the small energy difference (140 meV) between the direct band gap and the indirect band gap of Ge, as shown in **Figure 4(b)**. The excess electrons in the Γ valley lead to recombination with the holes in the valence band, which is a highly efficient light emission process because that the direct band-to-band radiative recombination is generally faster than the nonradiative recombinations, such as Auger and defect-assisted processes. But the overall light emission efficiency is very low because most of the injected electrons, staying in the L valleys, recombine nonradiatively due to a slower indirect phonon-assisted radiative recombination than the non-radiative recombinations. On the contrary, the light emission in a direct band gap material such as InGaAs is very efficient because almost all injected electrons are in the Γ valley thus recombine radiatively. To improve the light emission efficiency in Ge, more injected electrons are required to be pumped into Γ valley at the same carrier injection level. Thus, the band structure of Ge can be engineered to accomplish this goal.

1.3.2 Effect of tensile strain on Ge band structure

Efficient direct gap light emission in Ge requires a large amount of electrons in the direct valley. The ratio of the number of the direct valley electrons to the indirect L valleys electrons is determined by the energy difference between the direct band gap and the indirect band gap at quasi-equilibrium. Band structure is associated with crystal lattice, which can be changed by the existence of strain. This effect can be calculated using a strain-modified k-p formalism, which is known to provide an accurate description of the valence and conduction bands all over the Brillouin zone [14]. Such a calculation shows that strain changes the energy levels of the

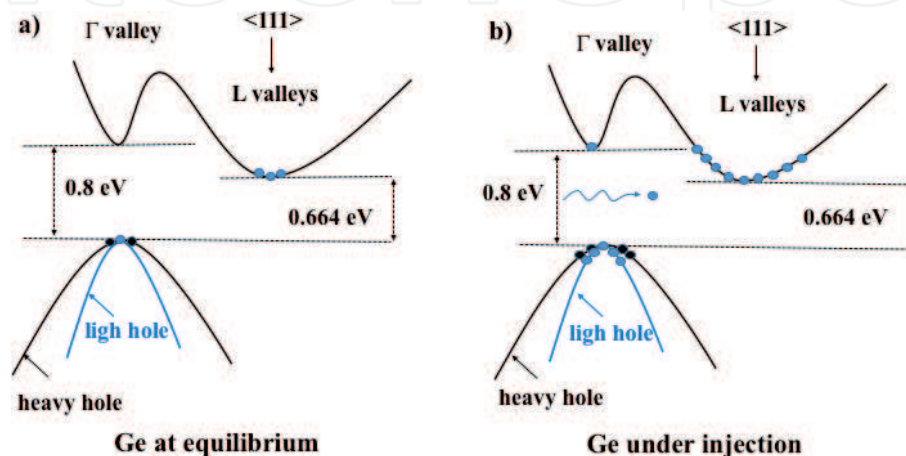


Figure 4. Distributions of electrons and the holes in Ge at equilibrium and under injection [3].

direct Γ valley, the indirect L valleys the light-hole band, and the heavy-hole band relative to vacuum level. Moreover, the light-hole and the heavy-hole band become nondegenerate and separate at Γ point. **Figure 5** illustrates the variation of direct and the indirect band gaps of Ge under strain [14]. We can see both the direct band gap and the indirect band gap shrink with tensile strain and the direct band gap shrinks faster than the indirect band gap. The direct band gap becomes equal to the indirect band gap at $\varepsilon_{//} \approx 1.8\text{--}1.9\%$ where Ge becomes a direct band gap material. The carrier distribution and the light emission properties of 1.8% tensile-strained Ge under injection are schematically shown in **Figure 6**. Since the Ge becomes a direct gap material, a considerable amount of the excess electrons occupying the direct Γ valley capable of radiative recombination leading to efficient direct gap light emission. The overall emission efficiency of the strained Ge is comparable to that of direct band gap semiconductors.

Biaxial tensile strain is thus an effective way to transform Ge to a direct band gap material, nevertheless two issues exist:

Firstly, highly strained, high-quality single crystalline Ge film is difficult to form because the large lattice change causes thermodynamic instability resulting in dislocations, surface roughness, and other lattice defects. Tensile strain can be induced either by lattice mismatch or by thermal mismatch. The former approach requires a substrate material with larger lattice constant than that of Ge. The latter approach

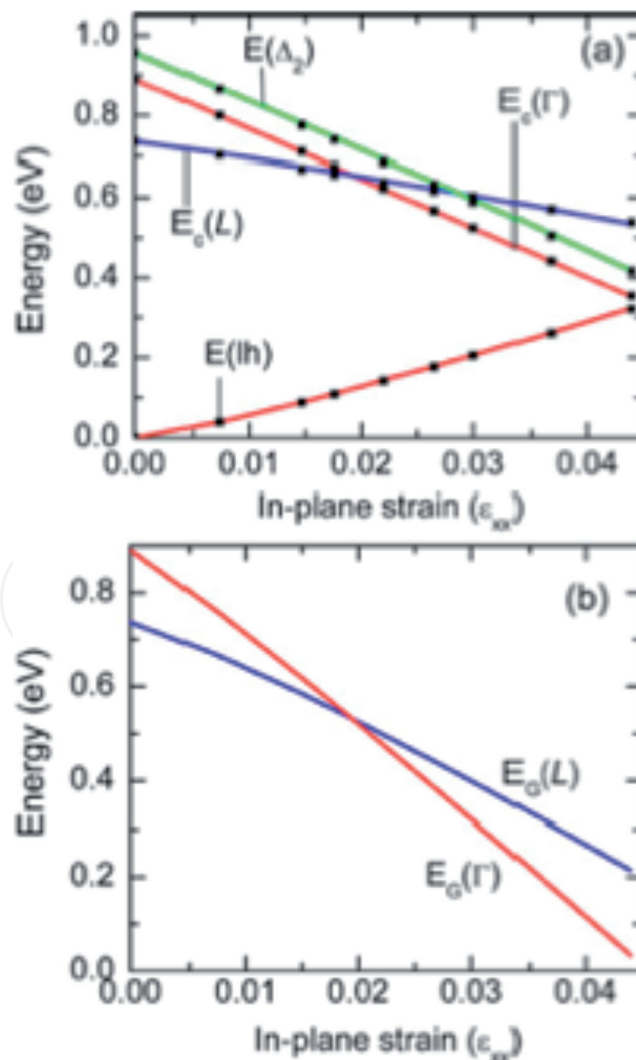


Figure 5. Energy dependence at low temperature (4 K) of the Γ , Δ_2 , L, and lh extrema as a function of the in-plane biaxial strain; (b) variations of the direct and indirect band gap energies as a function of the in-plane biaxial strain [14].

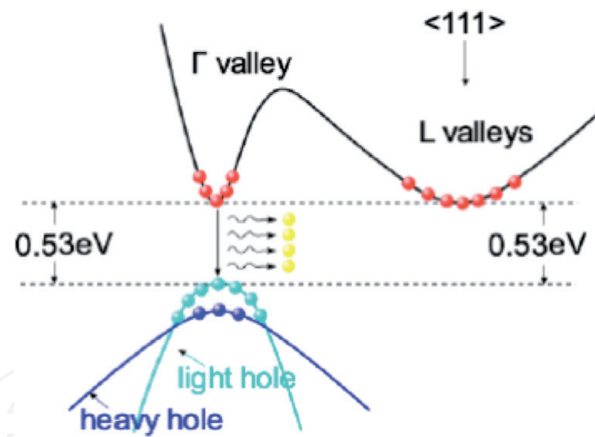


Figure 6.
Electron and hole distributions and light emission at 1.8% tensile-strained Ge.

requires different thermal expansion coefficient between Ge and the substrate material, which is adopted in this research. Up to 0.25–0.30% tensile strain has been achieved in Ge epitaxially grown on Si substrate, which will be discussed later. The second issue is the excessive change of the band gap in highly tensile-strained in Ge. Both the direct band gap and the indirect band gap become 0.53 eV at 1.8% tensile strain, as shown in **Figure 6**. This optical band gap is corresponding to an emission wavelength of about 2300 nm, which is far away from the 1550 nm telecommunication wavelength band, which is also the primary choice for Si photonics. These two issues suggest that very high tensile strains are not favorable in both material growth and photonics applications. Thus, the increase of the number of the injected excess electrons in the Γ valley owing to strain effect is limited. This problem can be solved by n-type doping in Ge.

1.4 Growth of tensile-strained Germanium on silicon substrates

1.4.1 Ge band gap engineering induced by tensile strain

Semiconductor diode lasers are conventionally based on direct band gap materials due to the efficient radiative recombination of direct gap transitions. As discrete devices, direct band gap III-V semiconductors are the main materials used to fabricate semiconductor lasers in telecommunications. On the other hand, indirect semiconductors, such as Si, Ge and their SiGe alloys are traditionally considered unsuitable for laser diodes due to their indirect band structure. The radiative recombination through the indirect band to-band optical transition is inefficient as a result of a phonon-assisted process. However, the direct band-to-band optical transition in Ge was shown to be very fast, exhibiting radiative recombination rate of 4–5 orders of magnitude higher than that of the indirect transition [13, 15]. Thus, if we can highly increase the number of electrons in the direct band gap, Ge could be used to fabricate diode lasers. Among group-IV indirect semiconductors (Si, and SiC), Ge exhibits interesting properties both from the transport and optical points of view. Regarding the transport properties, as can be seen from the **Table 1**, the hole mobility of Ge is highest in all semiconductors and its electron mobility is about 2.7 times higher than that of Si. Thus, Ge is of great interest for high mobility CMOS transistors, in particular p-CMOS transistors. Concerning the optical properties, Ge can be considered as a pseudo direct band gap material because of a small difference in energy between its direct gap and indirect gap, which is 0.140 eV or ~ 5 kBT at room temperature (kB is the Boltzmann constant). Theoretically, it has been shown that Ge can be transformed into a direct gap material with ~ 1.8 – 1.9% tensile strain

Properties	Si	Ge	GaAs	InAs	GaP	InP	InSb
E_g [eV]	1.124	0.664	1.424	0.354	2.272	1.344	0.225
μ_n [cm ² /V.s]	1450	3900	8000	30.000	200	5000	80.000
μ_p [cm ² /V.s]	370	1800	400	480	150	180	1500

Table 1.
 Values of the forbidden band gap and mobilities of holes and electrons in group-IV and III-V semiconductors.

[14, 16–18]. Indeed, upon application of biaxial tensile strain, both direct and indirect gaps reduce but the direct gap reduces faster. Thus, Ge can progressively transform from an indirect gap semiconductor toward a direct gap semiconductor with the increase of tensile strain. Furthermore, the tensile strain also lifts the degeneracy between heavy hole and light hole valence bands. The small effective mass of the light hole band reduces the density of states in the valence band, which, in turn, decreases the threshold for optical transparency and lasing [14, 18].

Tensile strain can be induced in Ge via several approaches: applying external mechanical stress [19], growing Ge on a larger lattice parameter substrate, such as InGaAs/GaAs [20, 21] or on relaxed GeSn buffer layers on Si [22, 23], or by taking benefit of the thermal mismatch between Ge and Si [18, 24–26]. An interesting result recently demonstrated by Jain et al. [27], who realized a Ge-MEMS device with 1% tensile strain introduced by a Si₃N₄ stressor. Compared to bulk Ge, the authors observed an enhancement of the photoluminescence intensity up to 260 times. In the frame of this work, we focus on the effect of band gap engineering of Ge films directly grown on Si substrates. The main advantage of the Ge/Si system is that it allows direct integration of Ge-based optoelectronic devices into the mainstream Si technology. In view of device applications, it is vital to obtain high-quality epitaxial material growth, i.e., to get Ge epilayers, which have a smooth surface and a low density of threading dislocations. To reach such an objective, the challenge is to control the Ge/Si growth process to overcome the limitation imposed by 4.2% lattice mismatch between these two materials. Thus, in the following part, we present results on the study of Ge growth on Si using a two-step method and on the dependence of the strain level on the substrate temperature.

1.4.2 Effect of the growth temperature on the value of tensile strain

After the low-temperature growth step, we have deposited another Ge film at higher substrate temperatures. In the following, we will consider the effect of the two-step growth process on the tensile strain in the Ge films. All samples have a total thickness of ~ 300 nm, which consists of a ~50 nm thick Ge film deposited at 300°C followed by a 250 nm thick Ge layer grown at various temperatures: 400, 500, 600, 650, 700, 750 and 770°C. As the tensile strain in Ge layers is induced by the difference of the thermal expansion coefficients between Ge and Si, it is natural to expect that the level of tensile strain should increase with increasing the growth temperature. **Figure 7** displays some representative θ - 2θ XRD scans taken around the Ge(004) reflection. For comparison, we report in dotted lines a XRD scan of a sample grown at 300°C of the same thickness.

As the growth temperature increases, the Ge(004) peak linearly shifts to higher angles, reaches a saturation value at 700°C and finally remains almost constant for further increasing the temperature to 770°C. The in-plane tensile strain observed in the temperature range of 700–770°C is 0.24%. The fact that the (004) peak of the 300°C grown sample is located at $2\theta \sim 66^\circ$, a value close to that measured on a Ge substrate, indicates that the corresponding Ge layer is almost fully relaxed. By using a high-resolution XRD, we estimate the rate of strain relaxation is about 95–96%. As can be seen in **Figure 7**, the 2θ angle value of the (004) peak is found to linearly increase when the growth temperature increases from 300 to 700°C then remains almost constant for further increasing the temperature up to 770°C. We note that to obtain the value of the in-plane tensile strain $\varepsilon_{//}$, we first determine the out-of-plane strain ε_{\perp} from the θ - 2θ XRD curves and then deduce the value of $\varepsilon_{//}$ using the following relationship: $\varepsilon_{//}/(\varepsilon_{//} + \varepsilon_{\perp}) = c_{11}/(c_{11} + 2c_{12})$ with $c_{11} = 12.85 \times 10^{10}$ Pa and $c_{12} = 4.83 \times 10^{10}$ Pa for pure Ge [28]. The highest value of the in-plane tensile strain $\varepsilon_{//}$ obtained in the growth temperature range of 700–770°C is 0.24%, which is in agreement with previous results reported using CVD in which the highest tensile strain was in the range of 0.22–0.25% [24–26, 29–33].

As we have already mentioned previous part, one of the unique properties of Ge is the very small energy difference between its direct and indirect band gap. Thus, Si/Ge interdiffusion represents an obstacle to overcome in order to develop Ge-based optoelectronic devices. Si/Ge interdiffusion has been shown to greatly affect the optical properties of Si/Ge heterostructures [34] and degrade the performance of metal-oxide semiconductor field-effect transistors (MOSFET) by reducing strain and carrier confinement and increasing alloy scattering [35]. To prevent interdiffusion or out-diffusion of an element (occurs when the sample was annealed at high temperature to enhance the tensile strain value in the Ge film), it is common to use a diffusion barrier and materials must be not only nonreactive but also are able to strongly adhere to adjacent materials. In electronic or memory devices, multilayers of metals, WN_2 , RuTiN , or RuTiO , are usually used to prevent out diffusion of dopants (B and P) or oxidation of devices [36–38]. Such materials are, however, difficult insert in a heterostructure where epitaxial growth is needed. It is now generally accepted that Si and Ge atoms interdiffuse via both vacancy and interstitial-related mechanisms [39]. To prevent Si/Ge interdiffusion, in particular to suppress upward diffusion of Si to the deposited Ge layer during growth or subsequent annealing, we have experimented an approach to saturate vacancies and

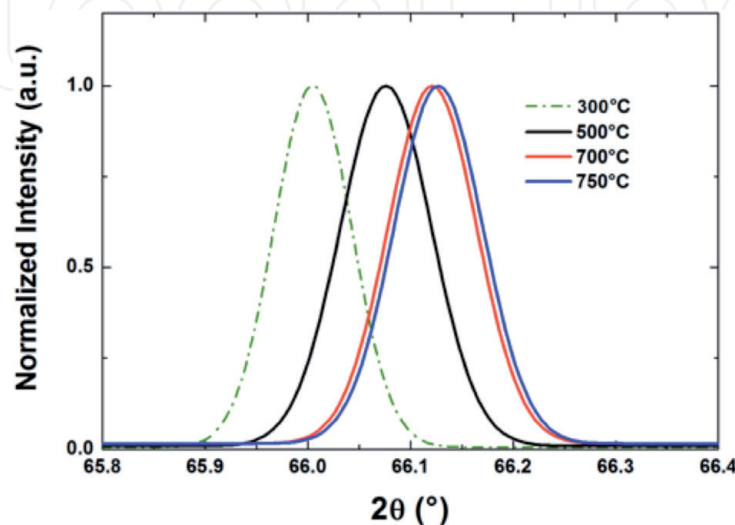


Figure 7. Evolution of θ - 2θ XRD scans around the Ge(004) reflection with the growth temperature. The dotted XRD scan corresponding to a sample grown at 300°C is shown for comparison.

interstitial sites in the Ge layer near the interface region. We have chosen carbon for its small atomic radius (twice as small as Ge), carbon atoms are thus highly mobile and can easily diffuse via interstitial mechanism [40–42].

To further confirm the effect of Ge/Si diffusion, we have used high-resolution HR-XRD reciprocal space mapping (RSM) equipped with a rotating anode to determine the Si composition and the strain level in Ge layers. 004, 224, and $-2-24$ RSMs were collected along the four $\langle 110 \rangle$ azimuthal directions. Combining the (224) map with that along (004) direction, one can measure both parallel and perpendicular lattice parameters of the Ge layer. The data obtained in reciprocal space are converted in direct space. We show in **Figure 8** the values of inter-reticular distances of the Si substrate and the Ge layer, measured along the (004) and (220) planes, of the sample annealed by 10 cycles at 780/900°C for 20 min. Note that for the as-grown sample, we obtain $a_{//} = 5.669 \text{ \AA}$ and $a_{\perp} = 5.649 \text{ \AA}$, which correspond the value of pure Ge ($a_{\text{Ge}} = 5.657 \text{ \AA}$). For the annealed sample, we obtain $a_{//} = 5.656 \text{ \AA}$ and $a_{\perp} = 5.625 \text{ \AA}$. Thus, the volume occupied by this unit cell corresponds to a $\text{Si}_x\text{Ge}_{1-x}$ alloy with a Si average concentration $x = 5\%$ (the corresponding average lattice parameter is about 5.646 \AA).

Figure 9(a) shows a TEM image taken near the interface region of a sample in which we have inserted three separate carbon layers during the first step of Ge growth. Starting from a clean and (2×1) reconstructed Si surface, we first grow a 30 nm thick Ge buffer layer at 300°C and then about 4 monolayers (ML) of carbon at the same temperature. Since epitaxial growth of the upper Ge layers should be conserved, the amount of deposited carbon is crucial. The latter can be determined using the change of RHEED patterns. Upon carbon deposition at 300°C, the (2×1) RHEED pattern characteristic of a clean Ge(001) surface remains almost unchanged up to carbon coverage of 6 MLs, beyond which a faint pattern appears. Since it is crucial to insure epitaxial growth of the upper Ge layer, a carbon amount of 4 MLs is then chosen (the corresponding carbon thickness is $\sim 0.3 \text{ nm}$). After this step, a Ge layer is deposited on top of carbon, producing therefore C/Ge stacked layers in order to increase the efficiency of carbon-induced diffusion barriers. We have experimented three multilayers of C (0.3 nm)/Ge (18 nm). **Figure 9(b)** shows

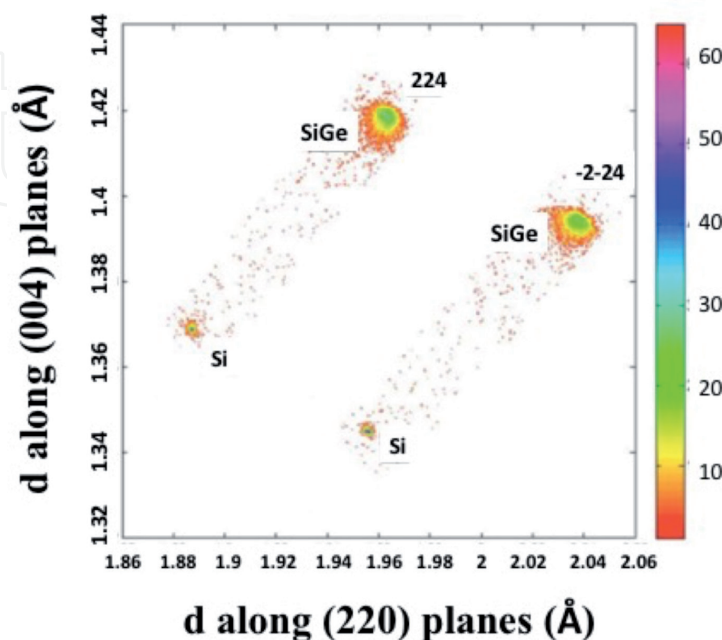


Figure 8.

Values of inter-reticular distances of Si and Ge, measured along the (004) and (220) planes of a 300 nm thick Ge layer deposited on Si at 730°C, followed by 10 cyclic anneals at 780/900°C for 20 min.

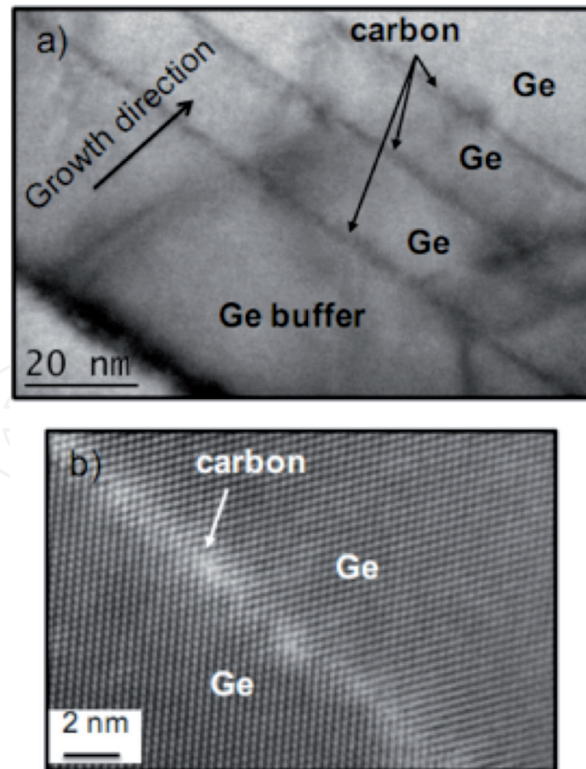


Figure 9. (a) TEM image taken near the interface region illustrating the growth of three multilayers of C (0.3 nm)/Ge (18 nm); (b) atomically resolved TEM image taken in the vicinity of the carbon layer.

an atomically resolved TEM image taken in the vicinity of the carbon layer. Clearly, the underneath Ge layers and also the upper Ge layers are perfectly epitaxial, without any detectable defects. The image also reveals that carbon atoms are distributed over a distance of ~ 2 nm, probably to occupy the interstitial sites of the Ge lattice or due to the strain generation arising from carbon insertion.

To verify the efficiency of C/Ge multilayers to prevent Si/Ge interdiffusion, we have finally grown a 300 nm thick Ge layer following the two-step growth as described previously. The high temperature step was carried out at 730°C. After growth, the sample was cyclically annealed by 10 cycles from 780 to 900°C and the annealing time was 20 min. In **Figure 10**, we display SIMS measurements of two samples: one without carbon deposition (red curve) and the other containing three C/Ge multilayers. As can be seen, the as-grown sample (black) shows a relatively sharp interface, no long-range upward diffusion of Si from the substrate was observed and the deposited Ge layer remains pure. On the other hand, the Si profile of the annealed sample, indicated in blue, reveals a pronounced Si upward diffusion. The Si content within the Ge film is highly heterogeneous, it continuously decreases from the interface to the film surface. The average Si content in the Ge film is estimated to be about 5%.

1.5 Phosphorus doping using a GaP decomposition source

Heavy n-doping of Ge films is essential to achieve efficient light emission from the direct gap transition. However, heavy n-type doping in Ge is a challenge due to a low solubility and a fast diffusivity of dopants. Three elements: phosphorus, arsenic and antimony, can be used as n-type doping in group-IV semiconductors. We report in **Table 2** the solubility of these three elements in Ge [43].

It can be seen that phosphorous has the highest solubility and at a temperature not too high. In UHV-CVD, the highest phosphorus concentration of $1.2 \times 10^{19} \text{ cm}^{-3}$

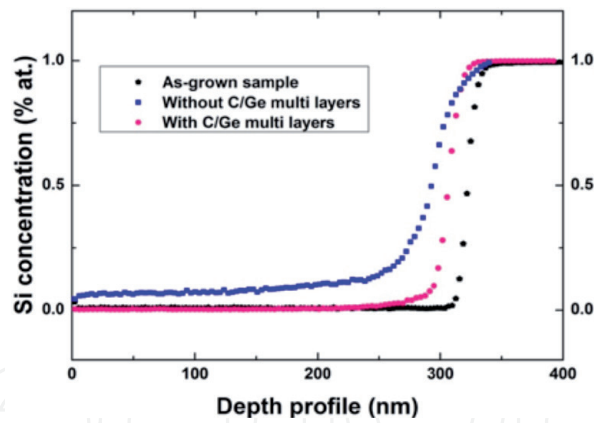


Figure 10. SIMS profiles measuring the Si content of the as-grown sample (black) and after 10 cyclic anneals at 780/900°C for 20 min (blue). The red curve corresponds to a sample in which three short C/Ge multilayers were deposited near the interface region.

Dopant	Maximum solubility	Temperature (°C)
P	$2 \times 10^{20} \text{ cm}^{-3}$	580
As	$8.7 \times 10^{19} \text{ cm}^{-3}$	800
Sb	$1.1 \times 10^{19} \text{ cm}^{-3}$	800

Table 2. Solubility of different n-type dopants in Ge [43].

was reported [44]. In CVD, the PH_3 is commonly used as a gas precursor and an activated P concentration of $2 \times 10^{19} \text{ cm}^{-3}$ was obtained at a temperatures of 600–700°C [12]. A phosphorus concentration up to $4.5 \times 10^{19} \text{ cm}^{-3}$ can be achieved by combining delta doping with diffusion barriers to reduce the P out-diffusion [45, 46]. It is worth noting that while dopant implantation is commonly used in the CMOS process, the activated P concentration is limited at about $1 \times 10^{19} \text{ cm}^{-3}$ even with the use of diffusion barriers [47], and a higher P concentration seriously deteriorates the material quality. Since tetrahedral white phosphorus (P_4 molecules) is not stable and highly volatile, we have used a specific doping cell based on the decomposition of GaP to produce di-phosphorus (P_2 molecules) [46–48], which has a sticking coefficient of about 10 times larger than that of tetrahedral white phosphorus. Thus, the phosphorus concentration in the Ge lattice could be increased and we can expect to enhance the efficiency of radiative recombination in Ge.

1.5.1 Specific GaP decomposition source

A photograph of a GaP decomposition cell is shown in **Figure 11**, which is heated by a Ta wire filament supported by PBN rings, similar to standard effusion cells. Compared to a valved phosphorus thermal cracker, the GaP cell is easy to set up, it operates as any effusion cell and is compatible with MBE environments. Using a Ga-trapping cap system, the GaP source can provide high-purity P_2 beam by decomposition of GaP. Its operation is based on the sublimation of phosphorus from GaP at an intermediate temperature range in which Ga has a very low vapor pressure. By placing a cap with small apertures on top of the cell (**Figure 11(b)**),

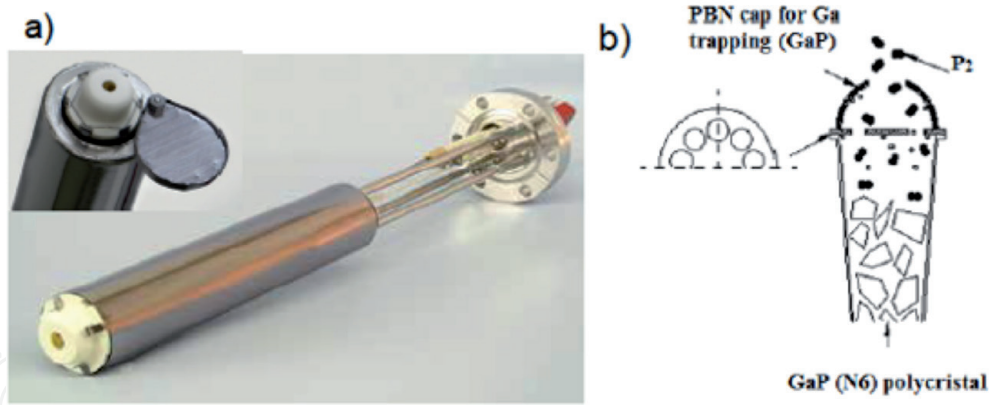


Figure 11. (a) Photograph of a GaP decomposition cell and (b) schema of the Ga trapping cap [50].

Ga atoms are trapped by the cap and only the P_2 beam can escape. According to the supplier [49], a P_2/P_4 ratio of about 150:1 can be achieved.

1.5.2 Efficiency of phosphorus doping from a GaP source

Figure 12 displays the evolution of the room-temperature photoluminescence spectrum versus the temperature of the GaP cell. For all samples, the substrate temperature is chosen to be 300°C and the film thickness is 100 nm. The temperature of the GaP source increases from 600 to 750°C . Note that based on the ref. [51], we avoid doping Ge films at 800°C . After growth, all samples were annealed in the growth chamber at 750°C during 1 min to activate dopants. As can be seen from the figure, the photoluminescence intensity increases with increasing the temperature of the GaP source temperature from 600 to 725°C and the highest PL intensity is obtained at 725°C . For the GaP source temperature at 750°C , the PL is found to decrease. Thus, the PL result, indicating that above 725°C the Ga trap from the GaP cell becomes less efficient.

1.5.3 Dependence of the substrate temperature on the doping level

To investigate the effect of the doping level versus the substrate temperature, we have therefore kept the GaP source at a constant temperature of 725°C . We display in **Figure 13** the evolution of the photoluminescence spectrum with the

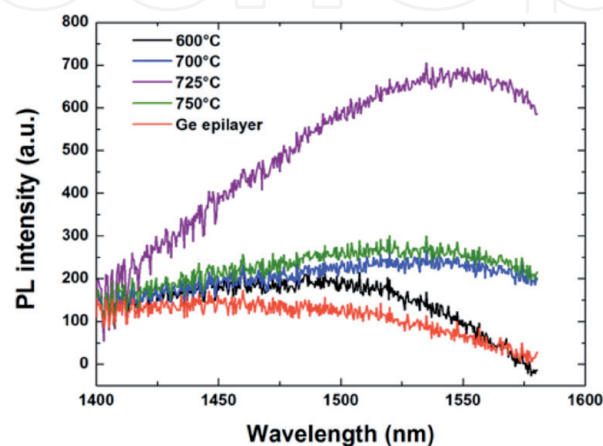


Figure 12. Evolution of photoluminescence spectrum versus the GaP source temperature. All PL measurements were carried out at room temperature.

substrate temperature. The reference sample is a 600 nm thick undoped Ge layer deposited at a substrate temperature of 170°C. The temperature of the GaP source is 725°C. The spectrum of the reference sample exhibits a very weak intensity and the emission from direct band gap is not clearly observed, as expected in an indirect band gap semiconductor. The PL intensity, which is very weak for the sample grown at 300°C, is found to increase with decreasing the substrate temperature and the highest PL intensity is obtained for a substrate temperature of 170°C. The evolution of the PL signal follows almost the same trend already observed for the electrical measurements not show here and thus confirms a high efficiency of P doping at a low substrate temperature of 170°C. The 170°C PL spectrum peaks at around 1624 nm (the corresponding energy is 0.765 eV). This transition can be attributed to arise from the direct band gap radiative recombination in the n-doped Ge layer. It is worth noting that if we compare the photoluminescence intensity of the sample doped at 170°C (blue curve) with that of the undoped sample (black curve), an intensity enhancement of about 50 times is obtained. Another noteworthy point is that when comparing the energy maximum at around 0.810 eV, arising from the direct band gap emission of unstrained and undoped Ge, we observe here a redshift of 45 meV, which can be attributed to band gap narrowing at high n-doping levels [52]. Indeed, a low temperature growth at 170°C does not induce tensile strain and after annealing at 750°C for 1 min, the corresponding Ge films only exhibit a tensile strain as low as 0.13%. Thus, the above optical redshift can be directly correlated to the effect of n-doping. According to ref. [52], a redshift of 45 meV corresponds to a doping level of $\sim 2 \times 10^{19} \text{ cm}^{-3}$. The separate investigation of the effect of the substrate temperature on the tensile strain and n-doping of the Ge layer brings fruitful information. The substrate temperature is shown to produce an opposite effect on these two properties of the Ge film. Higher growth temperatures (up to 770°C) induce larger tensile strain while low temperatures favor n doping. It is noteworthy that an activated n-doping level higher than 10^{19} cm^{-3} can be obtained at a growth temperature of 170°C. In addition, it should be pointed out that if Ge is directly deposited on Si substrates at a substrate temperature of 170°C, the Ge/Si growth does proceed via the Stranski-Krastanov mode. However, once a smooth Ge buffer has been formed on Si at 300°C, further Ge deposition on this Ge buffer layer will behave similarly as a homoepitaxial Ge growth and the growth is two-dimensional in a very large range of substrate temperatures.

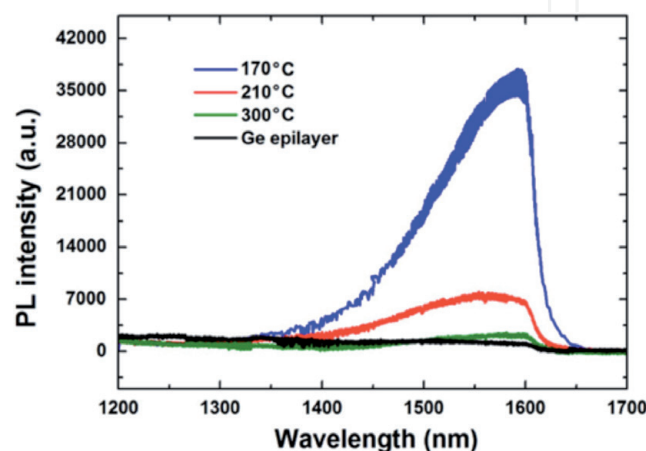


Figure 13.
Evolution of the photoluminescence spectrum versus the growth temperature.

2. Conclusion

To adopt an adequate strategy to produce Ge epilayers for optoelectronic applications, first it is important to emphasize that the thermal-induced tensile strain is limited to a value lying in the range of 0.25–0.30%, which is far from the expected value to get direct band gap Ge. Thus, it would be preferable to set up growth conditions, which favor n-doping. In other words, heavy n-doping appears to be the parameter that is more important than the value of the tensile strain. This implies that an adequate growth strategy would be to grow and to n-dope Ge films at low temperatures followed by post-growth thermal annealing. Since, Ge films, which are grown and n-doped at low temperatures, usually contain a high density of point defects (vacancies and interstitials). Therefore, the primary role of post thermal annealing is to restore the crystalline quality and to activate dopants into substitutional sites, without taking care of the value of tensile strain in the film. The efficiency of phosphorus doping may depend on two main parameters: the dopant solubility in a matrix and the sticking coefficient of dopants on the film surface. These two parameters are probably competing. The sticking coefficient of an atom or a molecule on a substrate surface increases with decreasing the substrate temperature. Since our results reveal that P doping is more favorable at low substrate temperatures, it appears that the sticking coefficient of the P₂ molecules is the dominant parameter determining the phosphorus doping level in Ge.

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