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Chapter 3

Application of Six Sigma in Semiconductor Manufacturing: A Case Study in Yield Improvement

Prashant Reddy Gangidi

Additional information is available at the end of the chapter

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Abstract

The purpose of this chapter is to outline systematic implementation of the Six Sigma DMAIC methodology as a case study in solving the problem of poor wafer yields in semiconductor manufacturing. The chapter also describes well-known industry standard business processes to be implemented and benchmarked in a semiconductor wafer fabrication facility to manage defect and yield issues while executing a Six Sigma project. The execution of Six Sigma enabled identification of the key process factors, root cause analysis, desired performance levels, and Cpk improvement opportunities. Implementing multilevel factorial design of experiments (DOE) study revealed critical input parameters on process tools contributing to defect formation. Improvement performed on these process tools resulted in in-line defect reduction and ultimately improving final yields.

Keywords: Six Sigma, semiconductor manufacturing, DMAIC, defects, yield, design of experiments (DOE)

1. Introduction

Six Sigma framework is a continuous improvement strategy that minimizes defects and process variation toward an achievement of 3.4 defects per million opportunities in design, manufacturing, and service-oriented industries [1–3]. Six Sigma practitioners often lead cross-functional teams in an organization to find and eliminate the causes of the errors, defects, lead, and cycle time delays in business processes. With rapid advancements in computers, artificial intelligence, and automotive vehicles, biomedical imaging semiconductor manufacturers find themselves constantly battling the demanding needs of the industry to sustain Moore's law and manufacture smaller chips to support next-generation software and hardware products.

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In order to manufacture nanometer range scale chips, there is a tremendous impetus toward developing advanced process control and measurement system capabilities. Defects become a big challenge in the efforts to reduce feature size in most semiconductor fabs as they negatively impact product yields [4]. Six Sigma methodology is often neglected in most fabs, and this chapter gives an overview of its importance and how it can be implemented to reduce defects with the help of a general case study. This chapter presents the step-by-step application of the Six Sigma define, measure, analyze, improve, control (DMAIC) approach to eliminate defects in a lithography process of a semiconductor manufacturing organization. This has helped to reduce defects in the process and thereby improve the final probe yields on a critical technology node. During the measure and analyze phases of the project, data were collected from the processes to understand the baseline performance and for validation of causes. These data were studied through various graphical and statistical analyses. Chi-square test, ANOVA, design of experiments (DOE), control charts, fishbone analysis, FMEA, etc. were used to make meaningful and scientifically proven conclusions about the process and the related causes [5].

2. Six Sigma literature review

The primary methodology of Six Sigma is the application of DMAIC problem-solving steps. A brief explanation for each of the steps involved is as follows:

Define (D): The first stage focuses on analysis of customer identification, feedback, and requirements along with forming the project stakeholder team [6]. The project team looks at critical to quality (CTQ) and cost of quality (COQ) improvement projects that need to be addressed keeping the end goal of customer satisfaction in mind by defining project scope/problem statement and budget scheduling. It is very critical to define an accurate problem statement along with the scope to ensure the Six Sigma project team will invest all the time, skills, and resources in the right direction.

Measure (M): This is the data collection phase where types of data, measurement scales, and sampling and collection methods are evaluated. All the initial metrics of the business case are established to measure the problem scale [2, 7].

Analyze (A): Measure and model relationships between variables, hypothesis testing, root cause analysis using cause and effect analysis tools such as fishbone/Ishikawa diagrams, 8D methodology, and 5 Whys analysis [2, 7].

Improve (I): Post root cause analysis, this phase tries to understand optimum levels of factors responsible for causing the problem via design of experiments (DOE), giving insights to determine corrective and preventative actions. This stage involves lean strategies such as the Kaizen Blitz, poka-yoke (mistake-proofing), cycle time reduction, etc. [7–9].

Control (C): Primary objective in this last phase is to maintain and sustain control over the process and suggest improvement activities to minimize variation and defects. Statistical process control (SPC), total productive maintenance (TPM), and control plan development are some key tools used in the control phase [10].

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3. Six Sigma application to defect reduction in semiconductor fabrication sites (FABS)

In this section, some business process areas have been identified to focus on benchmarking before considering Six Sigma project execution. Once these business process areas are well established, then only deploying Six Sigma teams would be beneficial to see tangible results. Motorola was one of the pioneers of Six Sigma methodology along with General Electric. Apart from Motorola, no other semiconductor manufacturing company has openly advocated the use of Six Sigma but has definitely inherited a lot of concepts and molded them into different terminologies. A big challenge to Six Sigma implementation is management support, and based on historical success rates of such projects initiated at their respective firms, the management decides to stick to their existing problem-solving methodologies or use some concepts from Six Sigma and other techniques used in industries such as aviation and automotive.

The most important goal for any semiconductor fab is to improve the final product yields [4]. Yield is directly correlated to contamination, design margin, process, and equipment errors along with fab operators [11]. **Figure 1** referenced from Integrated Circuit Engineering Corp. shows the ranking of top yield loss causing problems across various fabs [4]. Six Sigma DMAIC methodology can be used as an effective quality and reliability management tool to solve most of these issues, and several literature papers in the form of case studies have been published regarding the same.

Sources of random defects could be the equipment, fab personnel, process margins, process chemicals and gases, or cleanroom itself. Data collected from Integrated Circuit Engineering Corp. (ICE) over the last three decades have been shown in **Figure 2**.

Human and cleanroom sources of contamination have been steadily declining due to advanced training in this field being developed over the years at various universities and corporations along with rapid strides in automation and artificial intelligence that have modernized clean rooms and minimized human contact in handling wafers. Engineers and upper-level management of these fabs must adopt a systematic methodology in resolving yield losses that occur due to process and equipment variations, and in this chapter, some basic business processes

PROBE YIELD LOSS SOURCE	YIELD LOSS (%)	PERCENT OF TOTAL PROBE YIELD LOSS
Contamination	40	80
Design Margin	5	10
Process Variation	3	6
Lithography Errors	1	2
Material based defects	1	2
Total Loss	**50**	**2**
Probe Yield (100% - DIE LOSS) = 50 %		

Figure 1. Ranking of yield loss causing problems in fabs.

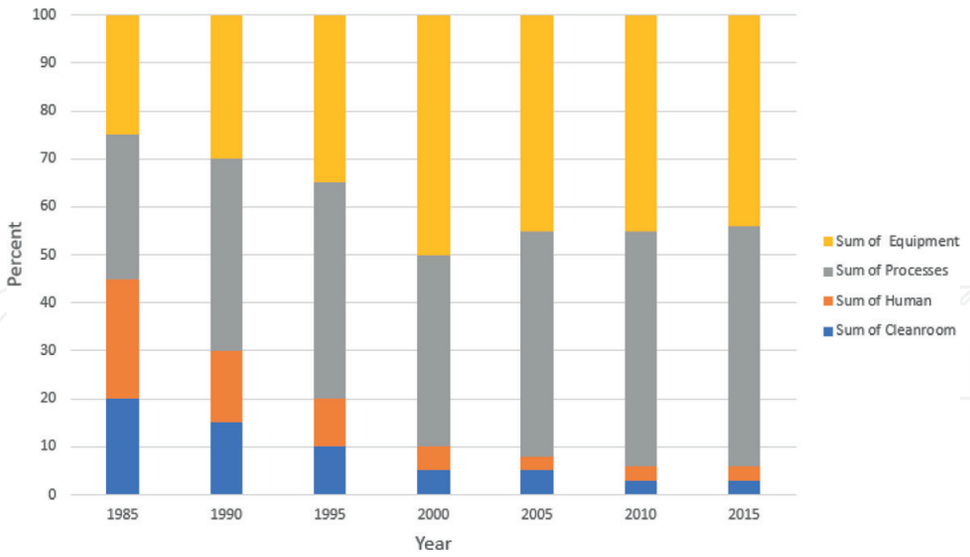

Figure 2. Bar chart showing wafer contamination source.

have been described that must exist in a fab for it to achieve maximum operational efficiency and produce high-quality chips. Six Sigma DMAIC methodology could then be used as and when required to improve these business processes.

3.1. Contamination and control protocols

Semiconductor processing involves several process fluids and gases, especially in lithography, film/metal deposition, etching, and cleaning steps. These fluids and gases contain impurity elements that can be dangerous to silicon devices [4]. These elements could be classified as the heavy metals, alkali metals, and light elements. Heavy metals such as Fe, Cu, Ni, Zn, Cr, Au, Hg, and Ag could result in wafer scraps and back end yield fallout due to corrosion in electroplating and metal deposition processing steps. Alkali metals such as Na, K, and Li and light elements like Al, Mg, Ca, C, S, Cl, and F could pose processing problems resulting in defects, which could be yield killing [4]. These elements also sometimes accumulate along the chambers, handlers, chucks, etc. of various equipment used in fabs resulting in tool downtime which greatly affects production schedules. Moreover, these elements could also pose safety problems to fab personnel. To understand potential risks and sources of these impure elements, a highly cross-functional FMEA team can be deployed to map out all the processes where source chemicals and gases are used along with identifying potential fail modes, severity, occurrence, and detection capabilities. The RPN exercise can be continued to drive improvements at each processing step where such impure elements are likely to occur.

3.2. Defect process mapping and yield management system

Defect density is defined as the total number of defects calculated per unit area on the wafer die [4]. In order to reduce defect density between processes, engineers need to identify the specific process steps, equipment, input materials, etc. that are the major contributors to the defect density. This involves the construction of a detailed process flow diagram for isolated segments of the process and the use of various problem-solving tools such as using

the Six Sigma concepts, cause and effect diagrams, design of experiments, Pareto principles, etc. to tie the total defects measured at the end of the process sequence to the likely sources in the process flow. Most cutting-edge fabs have automated scripts using machine learning principles to have correlation between in-line defects and final yield loss. Advanced data mining software can quickly scan through very large data sets involving integrated circuit parameters, processing parameters, equipment parameters, probe bins, defect metrics, etc. to come up with various models which the Six Sigma team can use to infer meaningful results during the analyze phase of DMAIC. Thus, having a good defect management and yield monitoring system while benchmarking to industry leaders will enable semiconductor fabs to execute Six Sigma projects efficiently while maintaining a competitive edge in the market.

3.3. Role of SPC in defect monitoring

Another major factor controlling line and probe yields is the ability of the fab to control process variations on critical parameters. In many progressive fabs, situational SPC is now becoming more popular as engineers concentrate more on critical processes and avoid the temptation to overuse tools such as process control charts. Two most important points that fabs must know regarding SPC charts to track in-line defects for Six Sigma scalability are:

i. Due to the high number of processing steps and the possibility of defects forming from any source, fabs must have particle monitoring (PMON) charts which are effectively attribute charts that track defects per million opportunities (DPMO) on bare silicon wafers to plot particles coming from the equipment. This helps to isolate defect sources solely coming from process equipment and can be tied with regular total productive maintenance (TPM) cycles in the fab. Process engineering/metrology experts must be able to decide the sampling frequency in this case.

ii. In-line defect metrology teams must be able to skillfully partition the line in placing SPC charts to control defect metrics based on historical learnings. Most fabs that do not have Six Sigma experts on their team usually have a hard time in determining the number of control charts and end up oversampling or undersampling. Attribute charts for key defect metrics that have downstream product yield impact or customer reliability issues should be given the highest priority in establishing control charts.

4. Case study

This section describes a case study wherein Six Sigma DMAIC methodology was used to tackle a probe yield issue due to an in-line defect contamination occurring in a lithography process step.

4.1. Phase 1: Define

This phase of the DMAIC methodology aims to define the scope and goals of the improved project in terms of customer requirements and to develop a process that delivers these

requirements. The first step toward solving any problem in the Six Sigma methodology is by formulating a team of people associated with the process [12]. For the case study in discussion, suspect of in-line process step was not known, and only the critical business impacting factor of yield loss data was known. The initial team comprised of a Certified Six Sigma Black Belt (CSSBB) who were the site quality engineering manager, yield engineering managers, failure analysis engineers, and technicians along with defect metrology engineers. Roles of the team members are shown in the project charter (**Table 1**). Next, the problem statement addressing CTQ and magnitude of the problem was identified. For a span of 13 weeks, one of the factory's key products had been failing for bin fallout along the edges of the wafer resulting in a yield loss of 7% for dies. Failure analysis team was contacted to perform extensive cross-sectional analysis of the defect location. Based on the information available to the Six Sigma team at this stage, problem statement was defined as follows:

Problem Statement: Defects occurring on about 25% of wafers around the edge result in bin failure and die loss on specific technology node.

Project title: Reduction of defects for edge die yield improvement on specific technology node wafers		
Business case for selecting the project:		
Edge die yield loss was ~7% on multiple wafers for a specific technology node. Yield loss on wafers results in microchip failure at the specified region on the wafer which impacts the customers due to poor product reliability.		
Aim of the project:		
Reduce die yield loss to ~1–2% from 7% by reducing in-line defects		
Project champion		CSSBB (quality engineering manager)
Project leader		Head—yield manager
Project team members		Engineering manager—defect metrology Engineer—failure analysis Two process engineers from defect metrology
Characteristics of product/process output and its measure		
CTQ	Measure and specification	Defect definition
Edge die yield	Reduce the number of defective dies at the final probe test by at least >50%	Defective dies at the final probe were cross sectioned and the defect measured 25 μm
Expected customer benefits		High-quality chips within expected time of delivery
Timeline		Define 2 weeks Measure 3–4 weeks Analyze 2 weeks Improve 4 weeks Control 3–4 weeks

Table 1. Project charter.

Here, the CTQ metric of die yield loss could directly be correlated to the number of such defects forming during in-line manufacturing that cause poor yields which results in delayed shipments and dissatisfied customers. The Six Sigma team's next tasks will be outlined in the subsequent sections showing measurement, data analysis, root cause drill down, and corrective action implementation.

4.2. Phase 2: Measure

In this phase, data correlation was conducted to see the correlation between in-line defect counts per wafer to the number of failing dies per wafer at the final probe and percentage of edge die yield loss. Results are shown in **Figure 4**.

It is evident from **Figure 3**, that the correlation between CTQ metric edge die yield losses to the number of in-line defect counts occurring per wafer is linear with the high R^2-adjusted value approaching close to 1. Six Sigma project team must reduce in-line defect count to less than 50 defects per wafer to have no die yield fallout at the final probe test.

4.3. Phase 3: Analyze

The analysis phase consisted of searching through brainstorming rounds, the possible factors that may be affecting the electrical performance of the product. This stage of the Six Sigma process improvement methodology is often termed as Thought Process Mapping [13] wherein process experts and Six Sigma champions assimilate existing facts and data collected so far and look for initial trends and themes to find clues to go after. The factors that were considered most important were raised as hypotheses and tested by several statistical tests.

Wafer fabrication line is partitioned into three modules—front end of line (FEOL), middle of line (MOL), and back end of line (BEOL)—where each module involves complex steps such as lithography, thin-film depositions, etching, planarization, and diffusion. Inspection sampling plans are strategically placed across several processing steps within these three modules considering cost, cycle time, and wafer throughput times. In this case, the project team was

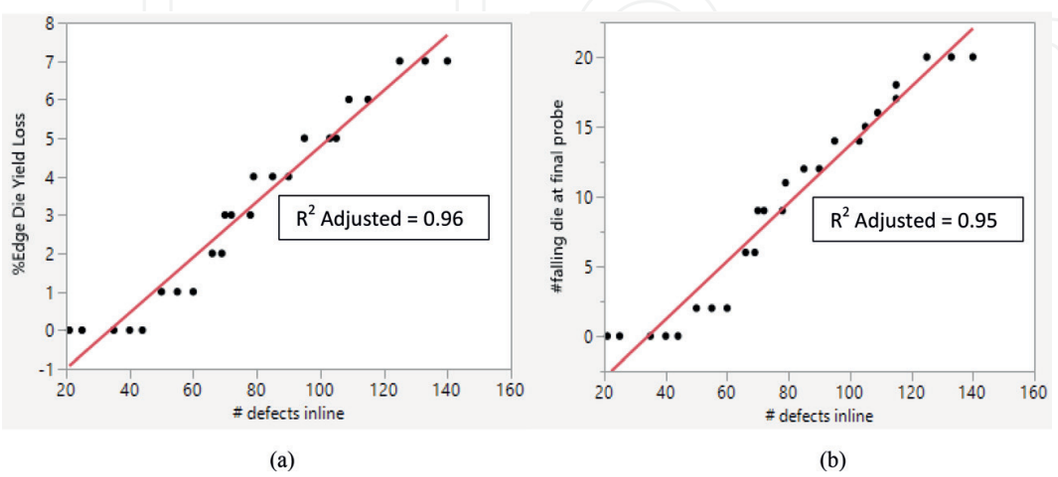

Figure 3. Regression plot of (a) number of failing die per wafer at final probe and (b) percentage edge die yield loss per wafer to number of defects per wafer in-line.

interested to see if there was any in-line defect inspection step that could replicate the defect pattern shown on probe bin wafer map. The project team decided to inspect additional sample wafers through this step and perform failure analysis on the defect locations. More in-line inspection recipes were set up strategically right after metal patterning lithography processes to study defect formation and evolution as the wafers progressed through manufacturing steps.

Through in-line inspections set up across these modules, it was observed that the defect under study was first detected after the metal patterning process. Optical image of the defect was taken along with SEM analysis post BEOL to see defect evolution. This gave an initial indication to the Six Sigma team that metal patterning process and perhaps tool variation in lithography must be analyzed further. There was a need for lithography experts to now help the Six Sigma team in root cause analysis, so lithography process engineering manager, two process engineers, and two process technicians were added to the project team. The project charter was revised to include the new members into the stakeholder team.

Since there is a strong clue of the issue coming from the lithography process area, Six Sigma project team decided to add lithography process experts into the stakeholder team. The project team's next objective was to brainstorm different failure modes that could be occurring with scanner tools in the lithography step and understand root causes from a scientific perspective. For this, the fishbone analysis was used to list several possible root causes across the six Ms—measurement, materials, method, mother nature/environment, manpower, and machine.

Different tools were used to validate the potential causes listed in the fishbone diagram, and a summary of the tools is listed in **Table 2**.

Gemba revealed that there was only one resist supplier to the patterning process, so supplier variation is not a root cause. SEM imaging did not reveal any polymer shearing defects. DOE carried out on resist coating process included a multilevel factorial design where coating speeds were varied from low to high to see if defects could be produced, but it was not the case. Fab contamination studies also showed that particles were well within control and environmental impacts to the formation of in-line defects were negligible. Careful review of all SOPs, manufacturing protocols, preventative maintenance log books, shift pass-downs, etc. did not confirm the validation of any cause. Majority of the effort was then spent in analyzing tool-to-tool variation, which was performed by ANOVA.

For confidentiality purposes, the exact supplier/tool names used in the factory are not mentioned in this chapter. There were three major tools in the factory running this product line, which will be addressed as Tools 1, 2, and 3 for analysis. One-way analysis of variation (ANOVA) of defect metric count with tool set was plotted (see **Figure 4**).

Tool 1 mean value was not only above the target defect count value of 50 but was also significantly above Tools 2 and 3, clearly indicating a problem with this tool.

4.3.1. Tool toggle statistical significance

Since there are multiple tool sets and data is non-normal, the Wilcoxon method is used for multiple tool set comparisons [14]. ($\alpha = 0.05$). H_o: Tool 1 toggle is statistically insignificant; H_a:

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Tool 1 toggle is statistically significant. It is observed that p-value is less than 0.05 when Tool 1 is compared with other two tools as per **Figure 5**.

Based on Wilcoxon test, reject H_o and accept H_a. Therefore, Tool 1 toggle is statistically significant and the toggle to defect metric is real. Next, the project team was tasked to look at SPC charts of all critical parameters of all three tools. It was found that the parameter scanner speed and exposure dosage of the immersion hood for Tool 1 were out of control (OOC) and mean value higher than Tools 2 and 3 as per the individuals and moving range (IMR) charts (see **Figure 6**).

Normal quantile plots for all three tools along with process capability index (Cpk) were calculated as shown in **Figure 7**.

SPC charts and normal quantile plots reveal a significant drift in parameter settings for Tool 1 compared to Tools 2 and 3. SPC charts show very tight distribution of points for Tools 2 and 3, but Tool 1 is not only out of spec but also has high amount of wafer-to-wafer variation for scanner speed and exposure dosage.

Out of all the possible failure modes evaluated and tested, it was confirmed that the source of defect could possibly be coming from *Tool 1 metal pattern processing step in lithography area*

Cause	Validation plan
Materials and method related to failure modes	Gemba
	Standard operating procedure (SOP) reviews
	Process engineering change notification reviews
	Process qualification white paper review
	Supplier to supplier variation studies on resist batches supplied
	Perform DOE on resist coating process
	SEM imaging for polymer shearing defect identification
Measurement	Gemba, SOP reviews for specifications, reading confirmations by multiple operators for calibration and solvent volume checks
Environment	Gemba with fab facility department, fab air quality check by reviewing contamination SPC charts, check pressure using fab pressure manometers
Manpower (human errors)	Review preventative maintenance cycle procedures
	Check shift pass-down notes
	Check if any inexperienced operator or new hires joined the team and were performing tasks
Machine	Study tool variation between tools 1, 2, and 3 by conducting ANOVA studies
	Gemba on bubble extraction seal quality and immersion hoods and resist clogging
	Check if any new recipe changes were made before and after the dates when in-line defects were first seen

Table 2. Cause validation plan.

due to significant variation in scanner speed and exposure dosage. The theory behind defect formation due to inaccurate scanner speed and exposure dosage is described below which is a commonly observed phenomenon in the industry [14].

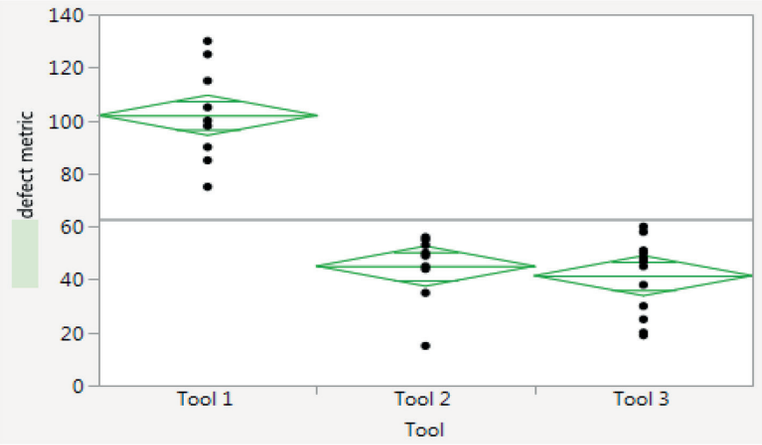

Figure 4. One-way ANOVA for defect metric by tool set.

q*	Alpha
1.95996	0.05

Level	- Level	Score Mean Difference	Std Err Dif	Z	p-Value	Hodges-Lehmann	Lower CL	Upper CL
Tool 3	Tool 2	-0.4615	2.995381	-0.15408	0.8775	-1.0000	-12.0000	8.0000
Tool 2	Tool 1	-12.9231	2.998974	-4.30917	<.0001*	-54.0000	-65.0000	-43.0000
Tool 3	Tool 1	-12.9231	2.998974	-4.30917	<.0001*	-56.0000	-70.0000	-42.0000

Figure 5. Nonparametric test data comparison.

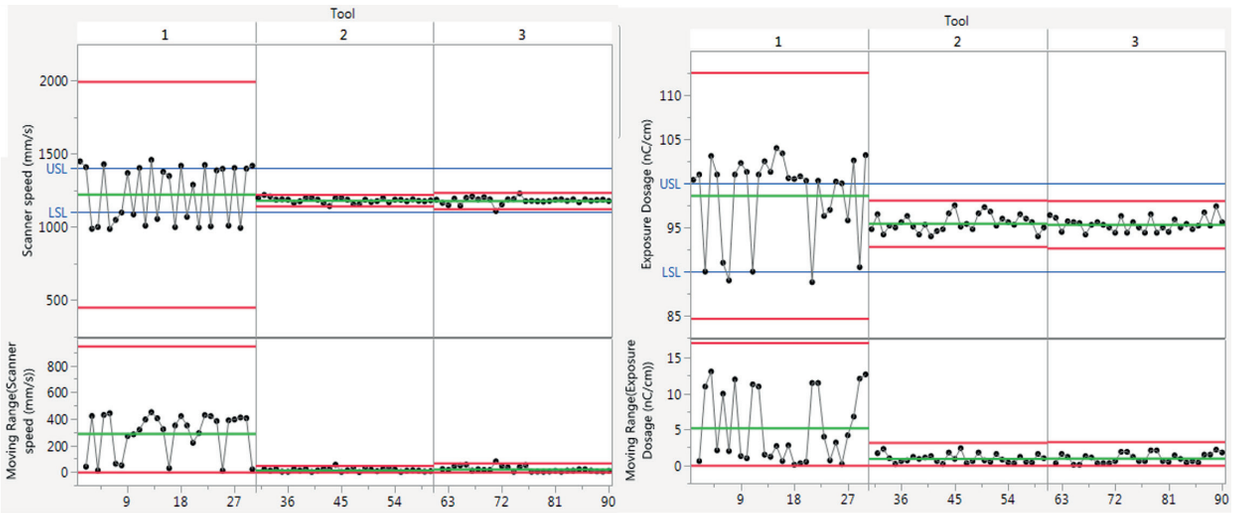

Figure 6. IMR chart comparison for scanner speed and exposure dosage by tool set.

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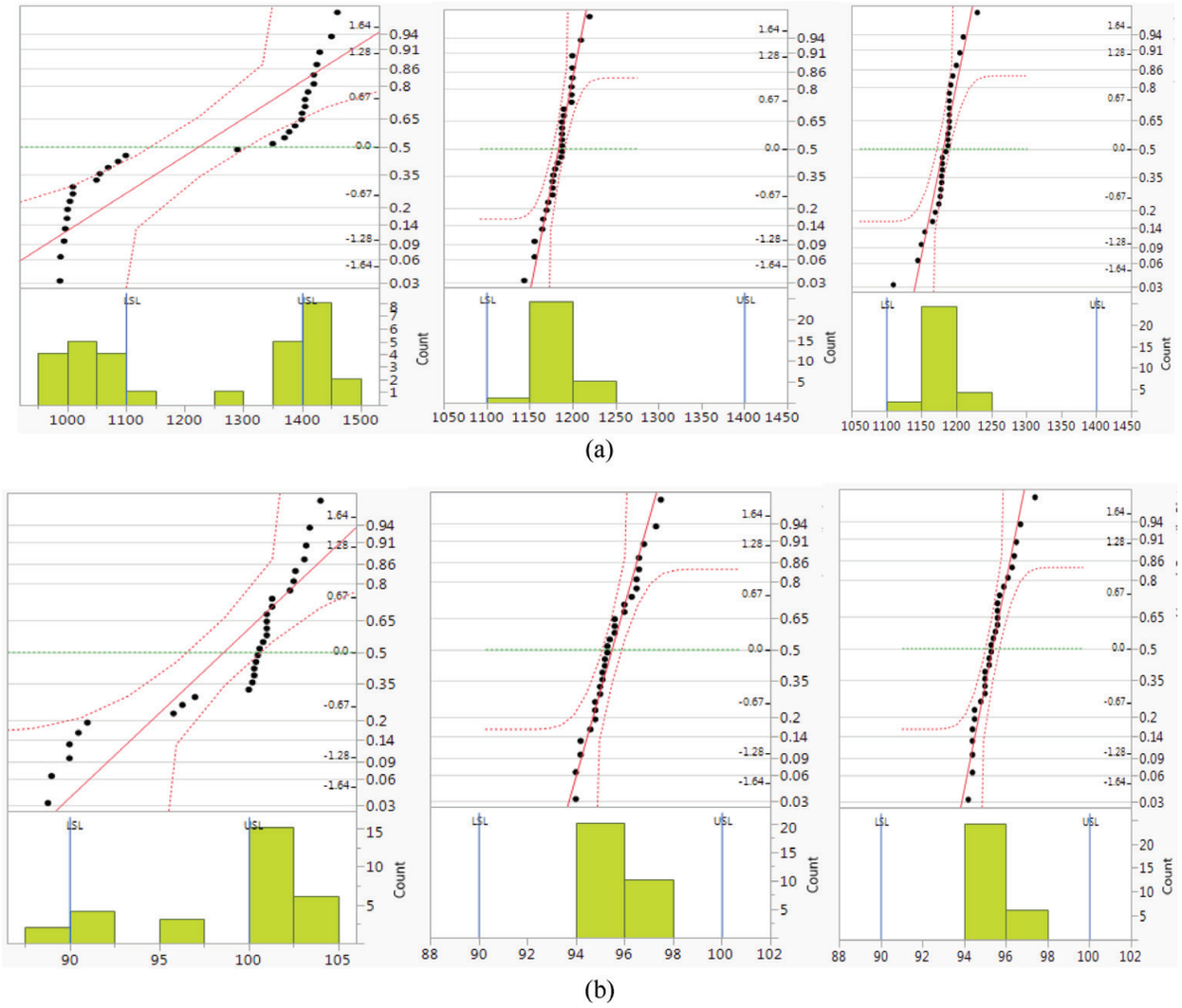

Figure 7. (a) Normal quantile plots for scanner speed and (b) for exposure dosage across three tool sets.

4.3.2. Defect formation theory

This defect is caused by a bubble forming in the scanner just prior to exposure. Light passing through the air bubble instead of the immersion water causes light refraction which creates a dipole. Attenuation of light can be seen outside of the ring as shown in **Figure 8** [14].

The system setup usually comprises a wafer placed on the scanner's robotic arm which moves at speeds varying from 1100 to 1400 mm/s per the manufacturer as shown in **Figure 9**. The space between wafer and immersion hoods (where the light source is located) is filled with water as an immersion fluid to increase image resolution by a fraction equal to the refractive index of the fluid [14–16].

The scanner speed of the stage should be optimized to increase productivity without creating defects on the substrate by losing droplets [17]. Immersion liquid level could be a source of a bubble inclusion in the immersion space. Fluid behavior in the region of the recess may cause

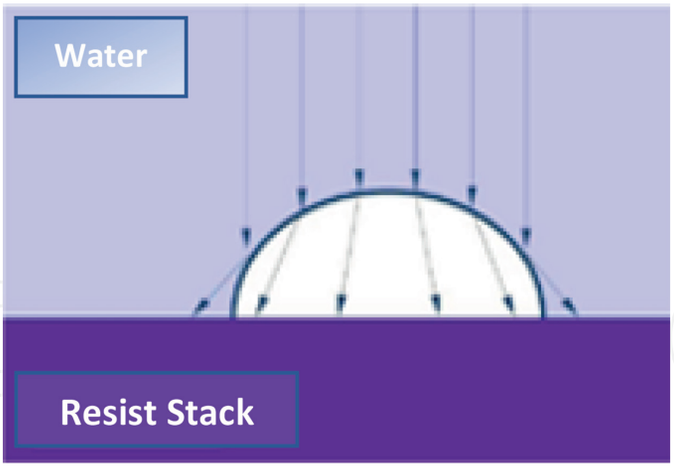

Figure 8. Light diffraction from bubble surface.

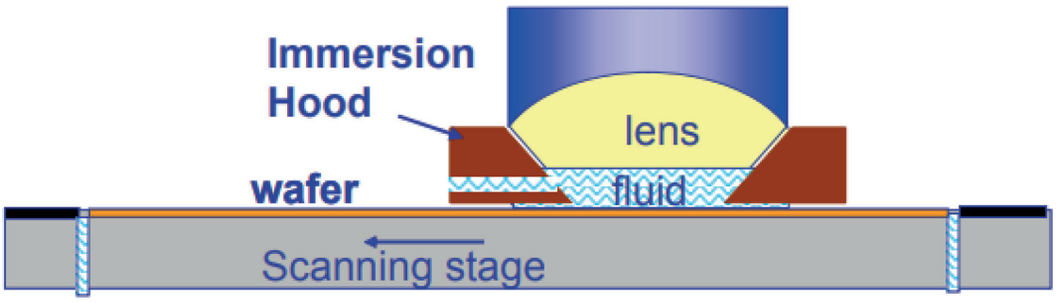

Figure 9. Schematic cross section of an immersion lithographic scanning device [17].

bubbles to form. This bubble may apply a heat load onto a surface onto which it lands, for example, the wafer surface resulting in poor lithographic imaging performance. If the exposure dosage inside the immersion hood is inadequate, bubbles could be entrapped inside the immersion fluid which is water in this case [14–17]. If the scanner moves too fast, the bubble extraction seal (BES) will not have adequate time to suck the bubble out resulting in the bubble being left on the wafer edge. BES extracts the bubbles between the scanner and wafer table.

The Six Sigma project team focused on fixing two main issues here contributing to defect formation—(1) inadequate exposure dosage resulting in air bubble entrapment inside the immersion hood and (2) inadequate scanner speed not giving enough time for BES to suck the bubbles out. Tool 1 settings have drifted significantly from other two tools and has a strong correlation to the high defect counts resulting in yield loss. The next step for the Six Sigma team is to identify optimal tool settings to minimize defect count and have all the three tools operating at these settings. This is discussed in the next phase of Improve.

4.4. Phase 4: Improve

In this phase, optimal tool settings for scanner speed and exposure dosage will be derived using the design of experiments (DOE) full factorial design. Corrective actions addressing the root cause will also be discussed in this section.

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Output response is the minimum defect count, while the input factors are scanner speed and tool exposure dosage. Scanner speed values can range from 1000 mm/s to 1400 mm/s per supplier, while the exposure dosage range is from 90 to 100 nC/cm. 16 run DOE table in JMP was created and resulted in prediction profiler obtained after the defect count values for all 16 runs were recorded as shown in **Figure 10**. Using the maximum desirability function in JMP, optimum settings were found to be the scanner speed, 1178 mm/s, and exposure dosage, 94.2 nC/cm.

Based on the above findings for scanner speed and exposure dosage, appropriate interim and long-term corrective actions were proposed and implemented.

4.5. Phase 5: Control

This is the final phase of the Six Sigma DMAIC methodology. Some of the questions that arise after the four phases of problem-solving methodology are as follows: How can one control and monitor the tool parameter settings in line? How can one monitor the in-line defect rate at multiple steps? The simple answer is via statistical process control (SPC) charts. Actual SPC charts on proprietary software have not been shown, but data was exported to JMP has been shown in **Figure 11(a)** and **(b)** post optimal setting discovery and corrective action implementation across all three tools.

It is observed that all three tools have mean values for both the critical parameters very close to the desired settings (1178 mm/s for scanner speed and 94.2 nC/cm for dosage) derived using DOE and have much tighter process control with occasional OOC points which will be addressed real time via the corrective actions implemented. To check process capability post improvements, capability analysis was plotted in JMP (**Figure 12(a)** and **(b)**).

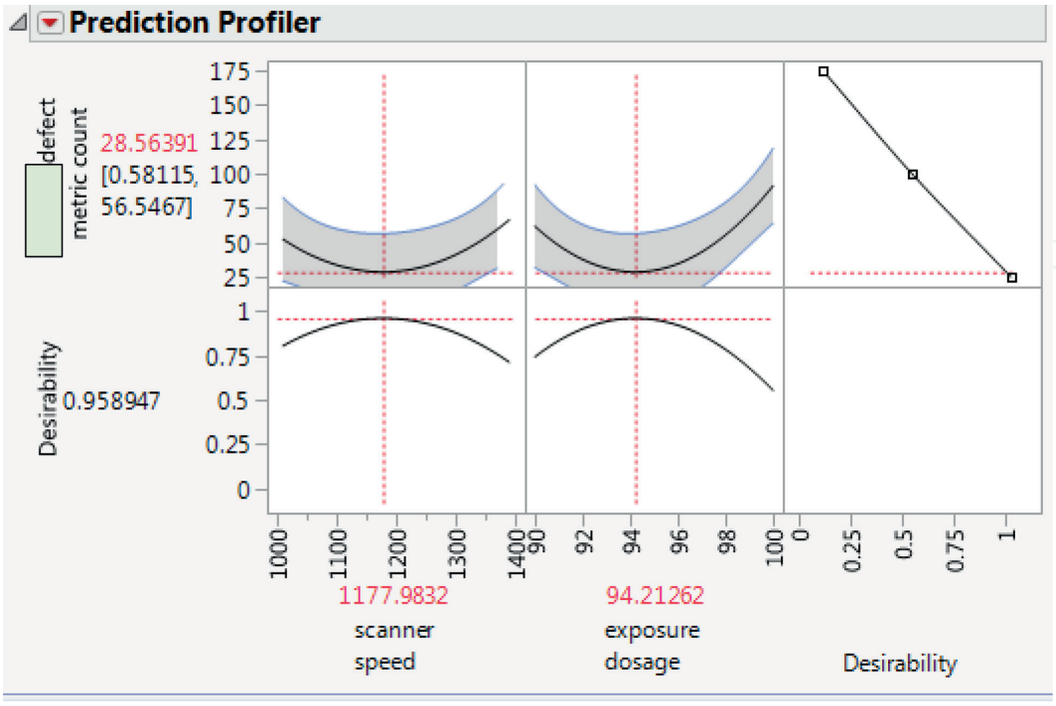
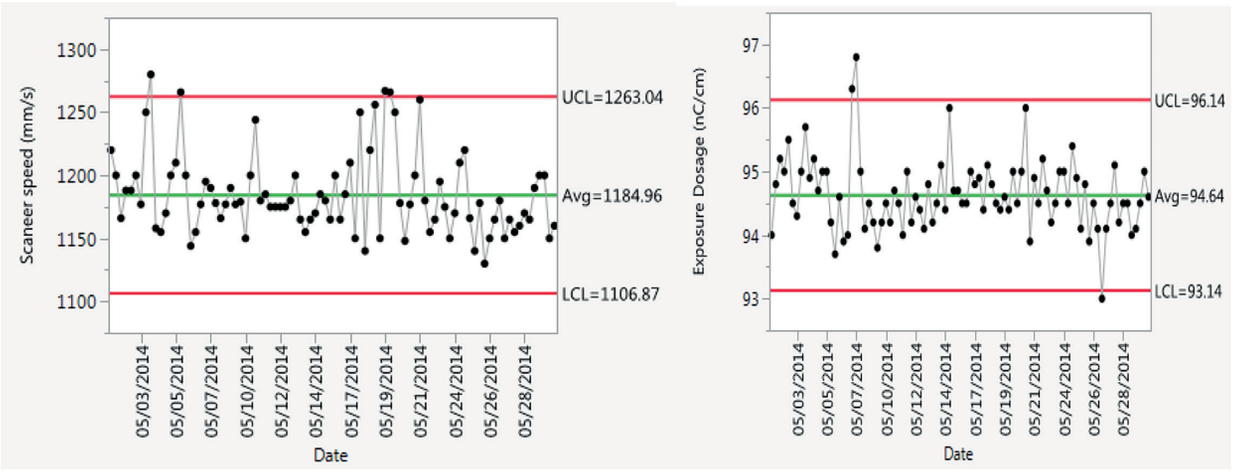


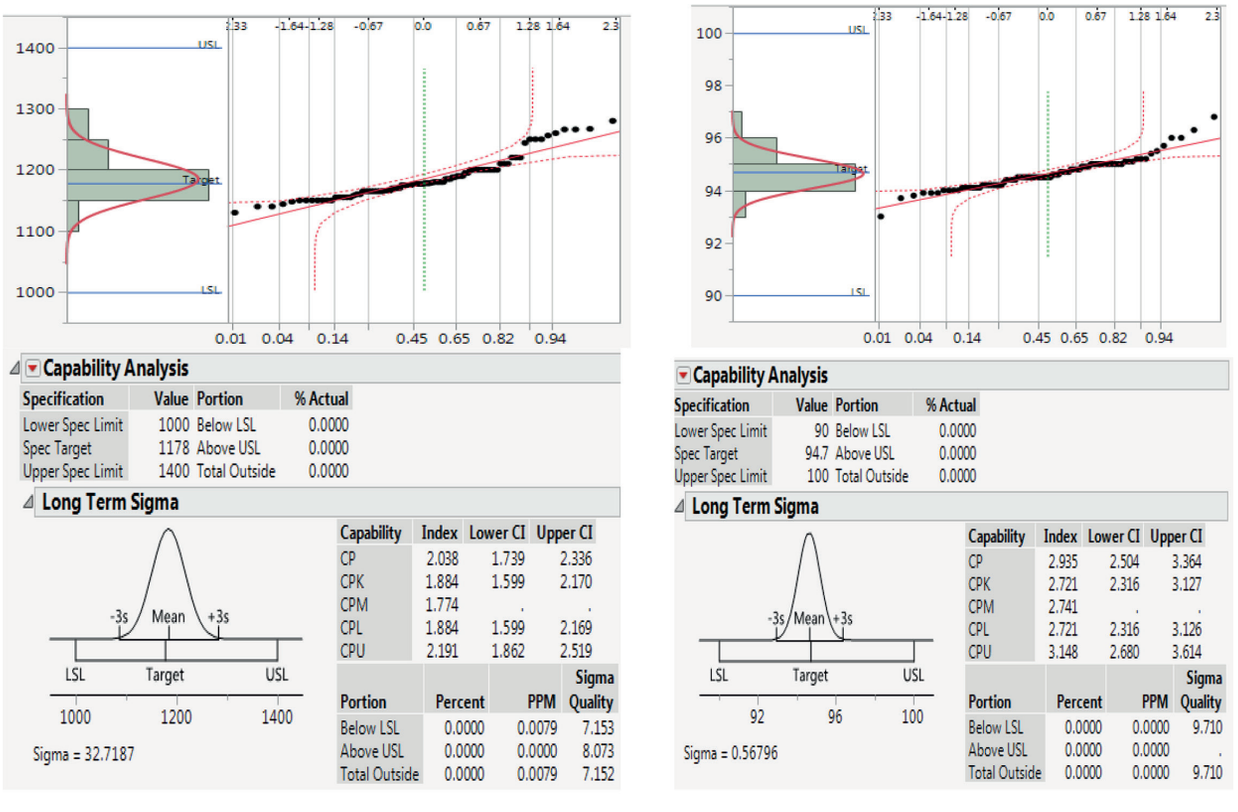
Figure 10. Prediction profiler indicating optimum tool settings for maximum desirability.

Binomial chart plots and Cpk values being >1.33 (1.88 for scanner speed and 2.7 for exposure dosage) clearly indicate high process capability and stability for the lithography metal patterning process post-tool setting optimization.



(a) (b)

Figure 11. (a) Individual chart for scanner speed and (b) individual chart for exposure dosage.



(a) (b)

Figure 12. (a) Process capability analysis for scanner speed and (b) process capability analysis for exposure dosage for Tool 1.

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FAILURE MODE AND EFFECTS ANALYSIS

Item:	Metal Patterning Litho step	Responsibility:	Quality
Model:	XYZ technology node	Prepared by:	Quality Engineering
Core Team:	CSSBB, Lithography Process Engineering, Quality Engineering		
FMEA number:	123456		
Page :	1 of 1		
FMEA Date (Orig):	1/1/2008	Rev:	A

Process Function	Potential Failure Mode	Potential Effect(s) of Failure	Sev	Potential Cause(s)/ Mechanism(s) of Failure	Occur	Current Process Controls	Detec	RPN	Recommended Action(s)	Responsibility and Target Completion Date	Action Results				
											Actions Taken	Sev	Occ	Det	RPN
Wafer Cleaning	insufficient cleaning	left over films from prior steps	7	defects	3	Operator training and instructions	3	63	Review cleaning procedures per SOP, additional training to new technicians	Lithography Shift Supervisors; WW 15-20	Have process technicians undergo certification process every 6 months; add additional inspection steps post cleaning if necessary	5	2	2	20
	high pressure cleaning	wafer breakage	10	scrap	3	Operator training and instructions	3	90	Continuous Improvement	Shift supervisors, engineers	6 month training certification process for technicians	8	2	3	48
	incorrect acid composition in cleaning tank	left over defects, film residues	7	defects	5	None	9	315	Install Composititon detectors; perform regular PM of cleaning tank	Shift supervisors, engineers; WW 15 -24	Installed detectors and establish PM cycle dates	7	3	9	189

Figure 13. PFMEA snapshot for wafer cleaning in patterning process.

4.5.1. Process FMEA and control plan development

Six Sigma project team decided to implement FMEA process and has appropriate corrective actions in place as part of control plan. Design-related failure modes and improvements were escalated to the tool manufacturer, while the fab focused on process FMEA for the metal patterning process. **Figure 13** shows the FMEA template for one of the processing steps in the patterning stage (wafer cleaning) which can be used across FEOL, MOL, and BEOL modules. Most of the corrective actions were implemented over 8 weeks, while some of them were part of continuous improvement activities. This FMEA table should be carried out for other subprocess steps involved in the metal patterning process such as resist application, BARC, etc.

Clearly, the new tool settings have greatly reduced the number of in-line defects occurring post-pattern processing steps. The line was then released to run production lots after 8 weeks of improve and control phase actions. This concludes the final step of the DMAIC methodology. The final conclusions and tangible improvement results are discussed in the next section.

5. Conclusions

Post DMAIC, as the mean defect count was continuously controlled and monitored below 50, the final probe yield test data also showed a significant reduction in die yield loss to almost 0% (100% yield) post-DMAIC implementation (**Figure 14**).

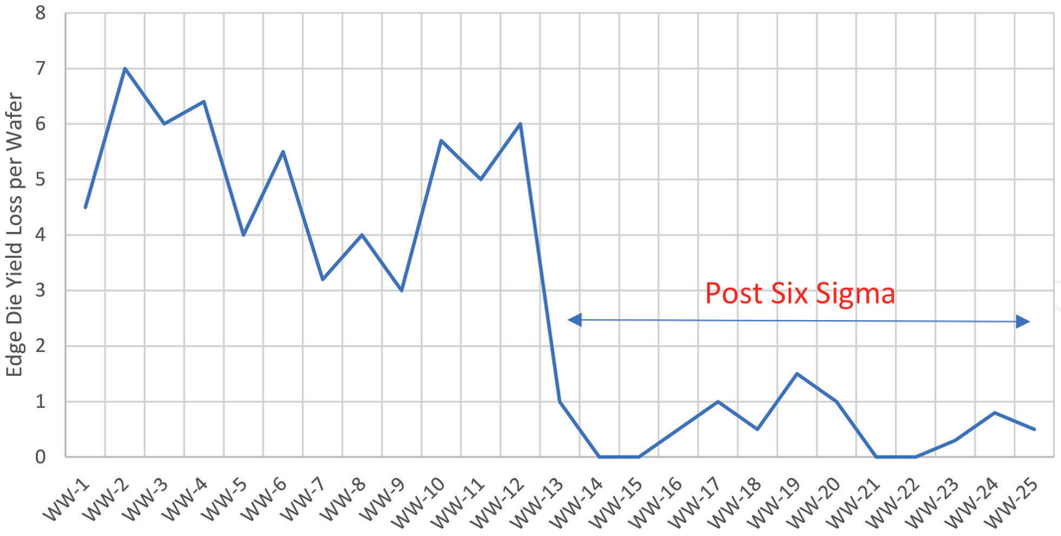

Figure 14. Edge die yield loss graph over 26-week time frame.

It can thus be concluded that DMAIC methodology properly executed under an experienced Six Sigma project team with the support of management is a powerful tool that can reduce process variations and improve product yields, eliminating waste and improving customer satisfaction which ultimately has a significant financial impact on the organization. Six Sigma can be used widely in semiconductor manufacturing environments where there is a tremendous need for defect reduction and tighter process control as the industry advances to smaller technology nodes.

Special note

The author would like to inform the readers that data represented in this paper are not the actual values and closely approximated values have been reported to give an understanding of data analysis, interpretation and application of six sigma methodology.

Author details

Prashant Reddy Gangidi

Address all correspondence to: prg4264@rit.edu

Independent Scientist, California, USA

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