Chapter

Analysis and Control of Power Electronic Converters Based on a System Zero Locations Approach

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Abstract

This chapter presents a procedure to design and control power electronic converters (PECs), which includes a zero-based analysis as a dynamical system response criterion for dimensioning converter passive elements. For this purpose, a nonideal boost DC-DC converter (converter considering its parasitic losses) is dynamically modeled and analyzed in steady state as an application example. The steady-state model is obtained from the average nonlinear model. The steady-state model allows deducing expressions for equilibrium conversion ratio $M(D)$ and efficiency η of the system. Conditions for the converter conduction modes are analyzed. Simulations are made to see how parasitic losses affect both $M(D)$ and η. Then, inductor current and capacitor voltage ripple analyses are carried out to find lower boundaries for inductor and capacitor values. The values of the boost DC-DC converter passive elements are selected taking into account both steady-state and zero-based analyses. A nonideal boost DC-DC converter and a PI-based current mode control (CMC) structure are designed to validate the proposed procedure. Finally, the boost DC-DC converter is implemented in PSIM and system operating requirements are satisfactorily verified.

Keywords: power electronic converters, boost DC-DC converter, zero-based analysis, current mode control, parasitic loss analysis, efficiency

1. Introduction

Design procedures of PECs must establish a trade-off between passive elements' values and dynamical performance because of the close dependence between them. Dynamical performance should not be deteriorated and operating requirements must be satisfied [1]. This task generally implies the construction of a nonlinear dynamical model and its implementation in any computational tool [2].

Dynamical modeling and steady-state analyses of PECs have received significant attention as tools to model system design [3]. Through dynamical modeling, it is possible to perform an analysis of the system behavior and its relation with passive elements' values [1]. Meanwhile, steady-state analysis provides expressions to determine in PEC: (a) $M(D)$, (b) η, and (c) continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundaries [3].

Multi-resolution PEC models can be constructed where parasitic losses can be taken into account [4]. However, if parasitic losses are not considered, the PEC model is simplified; but models do not adequately represent the PEC behavior in its entire operation range [5]. Moreover, a simplified model cannot predict both $M(D)$ and η nonlinearities and limitations [6].

Parasitic losses are typically modeled as appropriate equivalent series resistances (ESRs) associated with passive elements of PECs [3, 7, 8]. Parasitic losses can be included in the PEC design stage when both dynamical performance and η are taken into account [6]. Several works, [4, 7] to mention some of them, propose different PEC modeling approaches that have included parasitic losses. Nevertheless, in the reviewed literature, a consensus about what is the suitable detailed level of the model does not exist, in which PEC's dynamical behavior can be accurately represented; without the model, deduction becomes a challenge for the designer. However, the trend remains with the so-called average models which describe low-frequency and neglect high-frequency dynamics (semiconductor switching dynamics) of the system [9].

Average models that take, some or all, parasitic losses into account, have been presented by [1, 10]. Recent works [7, 10–14] show that a practical level of model detail for PECs includes parasitic losses associated with their passive elements and disregards losses due to semiconductor switching. Models with this level of detail are suitable for system design, $M(D)$ derivation, η analysis, and dynamical performance evaluation [12]. Additionally, these models are suitable for control purposes [2, 10].

It is clear that based on average models, PECs can be designed to carry out dynamical performance analysis. Notwithstanding, a design procedure is needed that comprises all necessary steps to design and control PECs and fulfills all given operating requirements. This design procedure must be simple and useful.

In the PEC field, few works that take into account dynamical characteristics of the system have been carried out [15–17]. In these works, PEC's design problem is presented as an optimization problem. In consequence, a procedure to easily design and control PECs is still needed. In this chapter, a procedure to easily design and control PECs is introduced. In this procedure, neither an optimization process is carried out nor is the control structure fixed. But, zeros' location impact over the system dynamical responses is analyzed, showing that a careful selection of the PEC passive elements could both avoid electronic device failures due to large overshoots and improve the dynamical system performance.

The structure of the chapter is organized as follows: in Section 2, both time- and frequency-domain models of the boost DC-DC converter are derived. In Section 3, the boost DC-DC converter is studied in steady state. Section 3 is composed of Sections 3.1, 3.2, 3.3, and 3.4. In Sections 3.1 and 3.2, expressions for $M(D)$ and η are derived including some parasitic losses. In Section 3.3, conditions to operate in CCM or DCM are found. In Section 3.4, both inductor current and capacitor voltage ripple analyses are carried out to find lower boundaries for inductor and capacitor values that fulfill ripple requirements. In Section 4, the value of the passive elements is selected such that operating requirements are fulfilled and system dynamical performance is achieved. Mathematical model is contrasted with a PSIM implementation of the boost DC-DC converter. In Section 5, the widely accepted current mode control (CMC) structure for boost DC-DC converters is designed.

2. Nonlinear dynamical modeling

Figure 1 shows a circuital representation of a typical boost DC-DC converter including its parasitic losses associated to the passive elements. The boost DC-DC

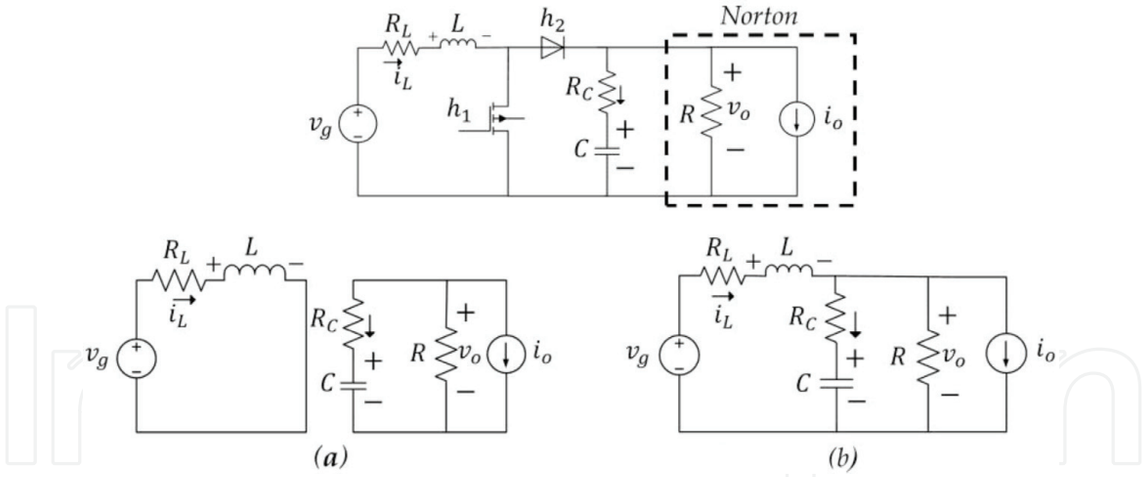

Figure 1.
Circuital scheme of the DC-DC boost converter: configuration (a) $h_1 = 1, h_2 = 0$. Configuration (b) $h_1 = 0, h_2 = 1$.

converter supplies energy to a dominant-current load represented as a Norton equivalent model. Engines and inverters are common dominant-current loads that can be supplied by a boost DC-DC converter. In **Figure 1**, L is inductor, C is capacitor, and R_L and R_C are the parasitic losses for L and C, respectively. R_L and R_C represent all parasitic losses.

The boost DC-DC converter operating in CCM can take two configurations according to the switch position as shown in **Figure 1**. First (**Figure 1(a)**) and second (**Figure 1(b)**) configurations correspond to switch $H = \{h_1, h_2\}$ being turned on $h_1 = 1$, $h_2 = 0$ and turned off $h_1 = 0$, $h_2 = 1$, respectively. Therefore, the switching function u can be defined as follows: $u = h_1$ or $u = 1 - h_2$.

State variables are inductor current i_L and capacitor voltage v_C which represent the energy variation in the system. The system inputs are u, DC input voltage source v_g, and current source i_o. Variations of i_o are useful to represent system current perturbations. The system outputs are output voltage v_o and i_L. The corresponding dynamical model of the system in **Figure 1** is given by Eqs. (1) (2), where $\alpha_C = R_C/R$ and $\phi_C = R_C/1 + \alpha_C$.

$$L\frac{di_L}{dt} = v_g - \left(R_L + \phi_C(1-u)^2\right)i_L + \left(\frac{\phi_C}{R} - 1\right)(1-u)v_C + \phi_C(1-u)i_o \quad (1)$$

$$C\frac{dv_C}{dt} = \left(\frac{1}{1+\alpha_C}\right)\left((1-u)i_L - \frac{v_C}{R} - i_o\right) \quad (2)$$

In this chapter, the widely accepted PI-based CMC structure for the boost DC-DC converter is adopted [15, 16]. PI controllers' tuning requires a frequency-domain model. From Eqs. (1) and (2), it is possible to obtain a linear state-space model of the boost DC-DC converter. Next, the frequency-domain model is obtained by means of the realization given by Eq. (3).

$$G(s) = \frac{1}{\det(sI - A)}C[\text{adj}(sI - A)]^T B + D \quad (3)$$

The linear state-space model for the boost DC-DC converter is given by Eqs. (4) and (5), where $x = [i_L, v_C]^T$, $u = [d, v_g, i_o]^T$, and $y = [i_L, v_o]^T$. I_L and V_C, D and I_o are states and inputs in their rated values, respectively. $d = \langle u \rangle_o$ (average value of u) is

the duty ratio, a continuous variable, and $d \in [0, 1]$. In this chapter, d is used as the input control, while D is d in the operation point.

$$\dot{x} = Ax + Bu \tag{4}$$

$$y = Cx + Du \tag{5}$$

where,

$$A = \begin{bmatrix} -\dfrac{(R_L + \phi_C)(1-D)^2}{L} & \dfrac{\left(\dfrac{\phi_C}{R} - 1\right)(1-D)}{L} \\ \dfrac{(1-D)}{(1+\alpha_C)C} & -\dfrac{1}{RC(1+\alpha_C)} \end{bmatrix} \tag{6}$$

$$B = \begin{bmatrix} \dfrac{\left(2\phi_C I_L(1-D) - V_C\left(\dfrac{\phi_C}{R} - 1\right) - \phi_C I_o\right)}{L} & \dfrac{1}{L} & \dfrac{\phi_C(1-D)}{L} \\ -\dfrac{I_L}{(1+\alpha_C)C} & 0 & -\dfrac{1}{(1+\alpha_C)C} \end{bmatrix} \tag{7}$$

$$C = \begin{bmatrix} 1 & 0 \\ \phi_C(1-D) & 1 - \dfrac{\phi_C}{R} \end{bmatrix} \tag{8}$$

$$D = \begin{bmatrix} 0 & 0 & 0 \\ -\phi_C I_L & 0 & -\phi_C \end{bmatrix} \tag{9}$$

The transfer functions given by Eqs. (10)–(15) are obtained by applying the realization given by Eq. (3), where $G_{i_{Ld}}(s) = I_L(s)/D(s)$, $G_{i_L v_g}(s) = I_L(s)/V_g(s)$, $G_{i_L i_0}(s) = I_L(s)/I_0(s)$, $G_{v_o d}(s) = V_o(s)/D(s)$, $G_{v_o v_g}(s) = V_o(s)/V_g(s)$, and $G_{v_o i_0}(s) = V_o(s)/I_0(s)$.

$$G_{i_{Ld}} = \frac{\left\{ \begin{array}{l} \left(\dfrac{1}{R}\right)(RC(1+\alpha_C)(2R\phi_C I_L(1-D) - V_C(\phi_C - R) - R\phi_C I_o)s \\ +(\phi_C + R)(1-D)RI_L - V_C(\phi_C - R) - R\phi_C I_o) \end{array} \right\}}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L + \phi_C)(1+\alpha_C)(1-D)^2\right]s + (R_L + R)(1-D)^2} \tag{10}$$

$$G_{i_L v_g} = \frac{RC(1+\alpha_C)s + 1}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L + \phi_C)(1+\alpha_C)(1-D)^2\right]s + +(R_L + R)(1-D)^2} \tag{11}$$

$$G_{i_L i_0} = \frac{\phi_C RC(1-D)(1+\alpha_C)s + R(1-D)}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L + \phi_C)(1+\alpha_C)(1-D)^2\right]s + +(R_L + R)(1-D)^2} \tag{12}$$

$$G_{v_o d} = \frac{\left\{ \begin{array}{l} [C\phi_C(1-D)(1+\alpha_C)(2R\phi_C I_L(1-D) - V_C(\phi_C - R) - R\phi_C I_o) + LI_L(\phi_C - R)]s \\ -I_L(\phi_C - R)(1-D)^2(2\phi_C + R_L) + (1-D)(2R\phi_C I_L(1-D) - V_C(\phi_C - R) - R\phi_C I_o) \end{array} \right\}}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L + \phi_C)(1+\alpha_C)(1-D)^2\right]s + (R_L + R)(1-D)^2} \tag{13}$$

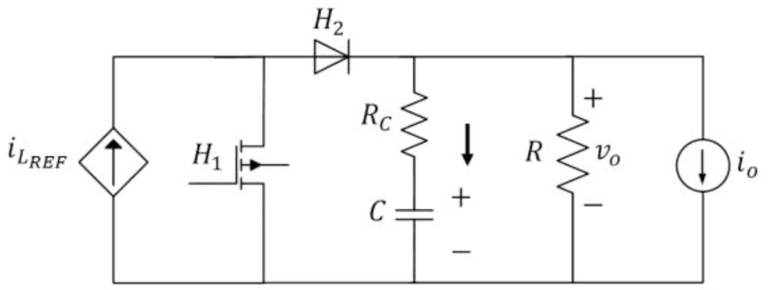

Figure 2.
Equivalent simplified representation of the boost DC-DC converter.

$$G_{v_o v_g} = \frac{R(\phi_C C(1+\alpha_C)s+1)(1-D)}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L+\phi_C)(1+\alpha_C)(1-D)^2\right]s + (R_L+R)(1-D)^2} \tag{14}$$

$$G_{v_o i_0} = \frac{R\left(\phi_C(1-D)^2 - \phi_C(1-D) - R_L\right)(\phi_C C(1+\alpha_C)s+1)}{(RLC(1+\alpha_C))s^2 + \left[L + RC(R_L+\phi_C)(1+\alpha_C)(1-D)^2\right]s + (R_L+R)(1-D)^2} \tag{15}$$

Once the current control loop in the CMC structure is closed, the equivalent simplified representation of the boost DC-DC converter shown in **Figure 2** is obtained. Large- and small-signal models of the simplified boost DC-DC converter are given by Eqs. (16) and (17), respectively. The transfer functions of the simplified model are given by Eq. (18). The numerator of Eq. (18) has two components, one for each system input, i.e., i_{REF} and i_o, respectively. In the CMC structure, Eq. (18) is employed to tune the PI controller in the outer control loop, which regulates v_o.

$$C\frac{dv_C}{dt} = \left(\frac{1}{1+\alpha_C}\right)\left(i_{L_{REF}}(1-D) - \frac{v_C}{R} - i_o\right) \tag{16}$$

$$\begin{aligned}[v_C^{\cdot}] &= \left[-\left(\frac{1}{1+\alpha_C}\right)\frac{1}{RC}\right][v_C] + \left[\left(\frac{1}{1+\alpha_C}\right)\frac{(1-D)}{C} \quad -\left(\frac{1}{1+\alpha_C}\right)\frac{1}{C}\right]\begin{bmatrix} i_{L_{REF}} \\ i_o \end{bmatrix} \\ [v_o] &= \left[\left(\frac{1}{1+\alpha_C}\right)\right][v_C] + \left[\left(\frac{1}{1+\alpha_C}\right)R_C(1-D) \quad -\left(\frac{1}{1+\alpha_C}\right)R_C\right]\begin{bmatrix} i_{L_{REF}} \\ i_o \end{bmatrix}\end{aligned} \tag{17}$$

$$G_{v_o}(s) = \frac{\begin{bmatrix}[(1+\alpha_C)RCR_C s + R + R_C](1-D) \\ -(1+\alpha_C)RCR_C s + R + R_C\end{bmatrix}}{(1+\alpha_C)[(1+\alpha_C)RCs+1]} \tag{18}$$

3. Steady-state analysis

Once the system model is obtained, the following analysis might be carried out: (1) derivation of the $M(D)$ expression, (2) losses effect and efficiency expression

derivation, (3) condition analyses of CCM and DCM, and (4) inductor current Δi_L and capacitor voltage Δv_C ripple analysis. The aim of these analyses is to determine suitable passive elements' (L and C) boundaries which satisfy the design requirements.

3.1 First step: derivation of the equilibrium conversion ratio M(D) expression

Steady-state model allows to derive expressions for average rated values for both v_C and i_L as functions of the system inputs and parameters. The steady-state model is obtained by setting the model given by Eqs. (1) and (2) to zero. Thus, Eqs. (19) and (20) are obtained.

$$I_L = \frac{V_C}{R(1-D)} \tag{19}$$

$$V_g = \left(\frac{R_L + R(1-D)^2}{R(1-D)}\right) V_o \tag{20}$$

From Eqs. (1) and (2), it is found that $V_o = V_C$ in steady state. The expression of $M(D)$ for the boost DC-DC converter is conveniently written using Eq. (21), where $\alpha_L = R_L/R$. $M(D)$ indicates the conversion gain factor in voltage in terms of D, R, and R_L.

$$M(D) = \frac{V_o}{V_g} = \frac{(1-D)}{\alpha_L + (1-D)^2} \tag{21}$$

Note that $M(D)$ does not depend on R_C due to the fact that the capacitor current in the average model is zero, leading to no voltage drop in R_C.

It is important to remark that if $R_L = 0$ in Eq. (21), this expression is in agreement with the ideal boost DC-DC $M(D)$, i.e., $M(D) = 1/(1-D)$. However, the converter reaches an efficiency equal to 100% if $R_L = 0$. Additionally, $M(D)$ tends to ∞ when D tends to 1. The above consideration is not true in a real boost DC-DC converter application and, for this reason, an analysis without including parasitic losses is not convenient.

3.2 Second step: losses effect and efficiency expression derivation

This section shows how parasitic losses affect η in the boost DC-DC converter case. Losses effect and efficiency analyses are carried out in order to find suitable values for R_L and R_C such that the designed PEC fulfills the operating requirements.

The DC transformer correctly represents the relations between DC voltages and currents of the converter. The resulting model can be directly solved to find voltages, currents, losses, and efficiency in the boost DC-DC converter [20].

Eqs. (22) and (23) are obtained from Eqs. (1) and (2). These equations establish that the average value of both i_L and v_C are equal to zero in steady state. **Figure 3** is the representation of Eqs. (22) and (23) as a DC transformer model.

$$0 = V_g - \left(R_L + \phi_C(1-D)^2\right) I_L - \left(\frac{1}{1+\alpha_C}\right) V_C(1-D)_{V_d} \tag{22}$$

$$0 = -\frac{V_C}{(1+\alpha_C)R} + \left(\frac{1}{1+\alpha_C}\right) I_L(1-D)_{I_d} \tag{23}$$

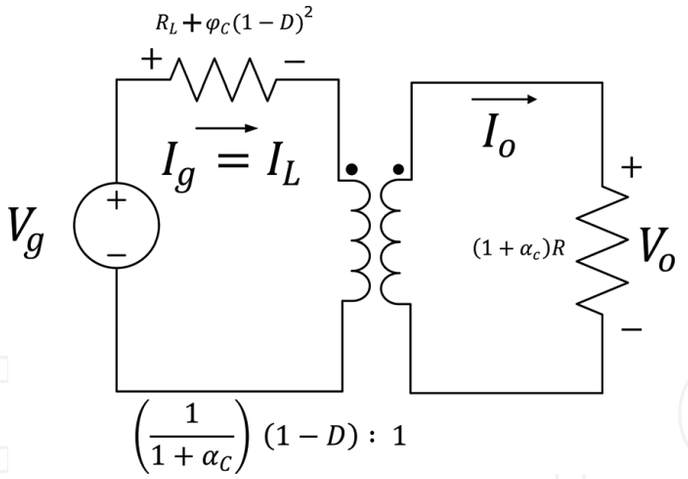

Figure 3.
DC transformer model of the boost DC-DC converter.

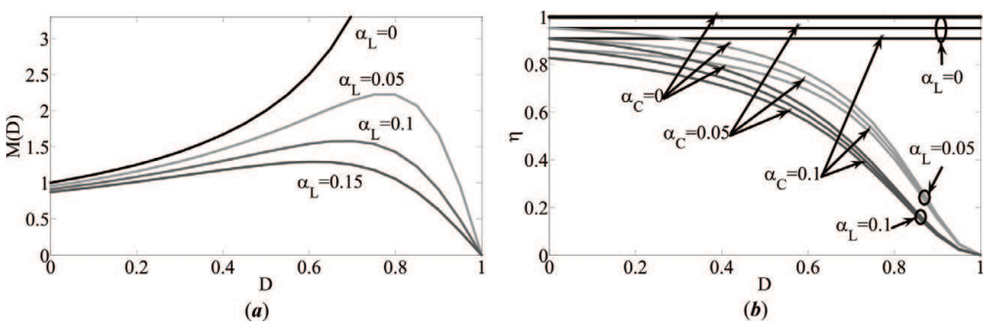

Figure 4.
(a) Conversion ratio $M(D)$ vs. duty cycle D. (b) Efficiency η vs. duty cycle D.

The equivalent circuit model in **Figure 3** allows to compute the converter efficiency η. From **Figure 3**, it is possible to deduce the efficiency expression given by Eq. (24).

$$\eta = \frac{(1-D)^2}{(1+\alpha_C)\left(\alpha_L + (1-D)^2\right)} \tag{24}$$

Simulations of Eqs. (21) and (24) are shown in **Figure 4** for several values of α_C and α_L ratios in order to test how much losses affect both $M(D)$ and η.

Figure 4(a) and **(b)** is shown together to relate $M(D)$ and η. Two different values of D can be selected to reach the same value of $M(D)$. Nevertheless, higher values of D lead to lower efficiency values. For this reason, it is recommended that the converter operates at low values of D as possible.

Figure 4(a) shows how the α_L ratio affects $M(D)$: $\alpha_L = 0$ is the ideal case for the boost DC-DC converter (without losses) and $M(D)$ in the converter has an increasing trend and eventually tends to infinity. When α_L increases (real case, converter with losses), $M(D)$ decreases and the curve has a quadratic trend. It can be observed that the higher α_L value matches to the lower converter conversion ratio $M(D)$.

From **Figure 4(b)**, it is observed that the maximum η value reached by the converter is determined by losses and it is given in $D = 0$ for every $M(D)$ curve. For the studied case, it is the combination of α_C and α_L that determines the maximum value of η, which decreases while D increases, dropping to 0 when D tends to 1.

Hence, the converter should operate as far as possible with low D values. Additionally, an increase of either α_C or α_L causes a decrease in η. Therefore, α_C and α_L should tend to zero to guarantee high converter efficiency. Values of α_C and α_L were clustered in groups of curves. For $\alpha_L = 0$ and $\alpha_C = [0, 0.05, 0.1]$ (above lines group), it is noted that while α_C increases, η slightly decreases. For curves group $\alpha_L = 0.05$ and $\alpha_C = [0, 0.05, 0.1]$ (middle lines group) and for curves group $\alpha_L = 0.1$ and $\alpha_C = [0, 0.05, 0.1]$ (below lines group), something similar occurs—η decreases while α_C increases. However, decreases in η are more notable when α_L increases than when α_C increases. The combined effect of high α_L and α_C leads to a highly inefficient system with high losses.

3.3 Third step: conditions for the converter conduction model

The CCM is suggested since DCM causes a larger voltage ripple in the boost DC-DC converter case [18, 19]. In consequence, the peak inductor current in DCM is higher than in CCM [22]. By [20], the condition for operating in the CCM is $|I_L| > |\Delta i_L|$ and the condition for operating in the DCM is $|I_L| < |\Delta i_L|$. The DCM condition for the boost DC-DC converter is given by Eq. (25), where $T_s = 1/f_{sw}$ and f_{sw} is the converter switching frequency.

$$D(1-D)^2 > \frac{2L}{RT_s} \tag{25}$$

The left side of Eq. (25) is a function that only depends on D. Here, this function is named as $K(D) = D(1-D)^2$. The right side of Eq. (25) is a dimensionless function that depends on L, R, and T_s, which is named in this chapter as $K = 2L/RT_s$. If L and R are taken as the converter parameters and f_{sw} is fixed, K is a constant and represents the converter measure to operate in CCM and DCM [20]. Large values of K lead to CCM. Small values of K lead to the DCM for some values of D. $K(D)$ is a function that represents the boundary between DCM and CCM. Then, the minimum value of K must be at least equal to the maximum value of $K(D)$, i.e., $\max(K(D)) \leq \min(K)$, if it is desired that the converter always operates in CCM, see **Figure 5**. Therefore, if values for R and T_s are given in the system specifications, a condition for the minimum possible value of L that assures CCM operation is given by Eq. (26), with $\max(K(D)) = 0.148$, that is equal to the critical value of K (K_c).

$$L > 0.148\frac{RT_s}{2} \tag{26}$$

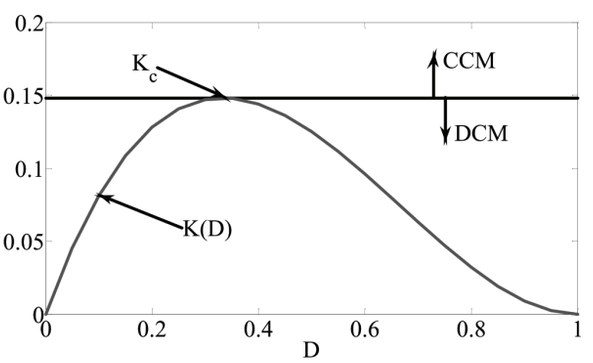

Figure 5.
$K(D)$, K, and conduction mode (CM) conditions.

3.4 Fourth step: inductor current and capacitor voltage ripple analysis

Δi_L and Δv_C analyses are carried out to determine constraint equations for a suitable choice of both L and C values. The carried out analysis in this section is suitable for the boost DC-DC converter operating in CCM. **Figure 6** shows both typical inductor voltage v_L and inductor current i_L linear-ripple approximations. The slope with i_L increasing or decreasing is deduced from the analysis of V_L at each subinterval of time taken into account. Typical values of current inductor ripple Δi_L lie under 10% of the full-load value of I_L [20]. From **Figure 6**, it is seen that i_L begins at the initial value of $i_L(0)$. After time proceeds, i_L increases during the first subinterval (DT_s) and decreases during the second subinterval ($(1-D)T_s$), both with a constant slope. Then, the switch changes back to its initial position at time $t = T_s$ and the process repeats.

As illustrated in **Figure 6(b)**, both current ripple and inductor magnitudes are related through the slope of i_L. The peak inductor current I_{pk} is equal to I_L plus the peak-to-average ripple Δi_L. I_{pk} flows through inductor and semiconductor devices that comprise the switch. The knowledge of I_{pk} is necessary when specifying the rating of the device. The ripple magnitude can be calculated through the knowledge of both the slope of i_L and the length of the first subinterval (DT_s). The i_L linear-ripple approximation is symmetrical to I_L; hence during the first time subinterval, i_L increases by $2\Delta i_L$ (since Δi_L is the peak ripple, the peak-to-peak ripple is $2\Delta i_L$). In consequence, the inductor value L can be chosen from Eq. (27).

$$L = \frac{V_g - \left(\frac{\alpha_L}{(1-D)}\right)V_o}{2\Delta i_L} DT_s \tag{27}$$

Eq. (27) is a lower boundary for the L value, where L can be chosen such that a maximum Δi_L is attained for the boost DC-DC operating condition.

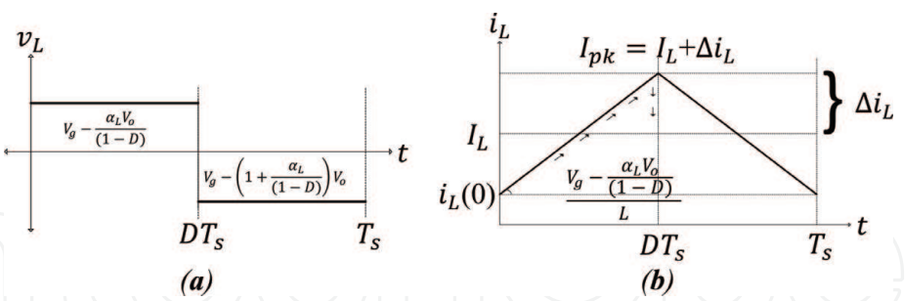

Figure 6.
(a) Typical inductor voltage linear-ripple approximation. (b) Typical current inductor linear-ripple approximation.

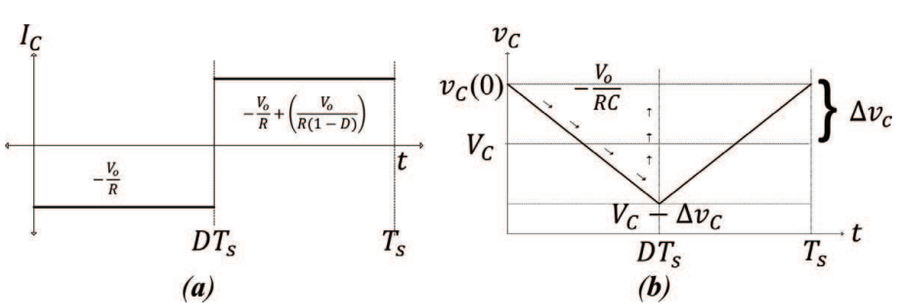

Figure 7.
(a) Typical capacitor current linear-ripple approximation. (b) Typical capacitor voltage linear-ripple approximation.

Likewise, v_C linear-ripple approximation is depicted in **Figure 7(b)**, where a relation between the voltage ripple and the capacitor magnitude is observed. It is seen that v_C begins at the initial value of $v_C(0)$. After time proceeds, v_C decreases during the first subinterval (DT_s) and increases during the second subinterval ($(1-D)T_s$), both with a constant slope. Then, switch changes back to its initial position at time $t = T_s$ and the process repeats itself. The ripple magnitude can be calculated through the knowledge of both the slope of v_C and the length of DT_s. The change in v_C, $-2\Delta v_C$ during DT_s, is equal to the slope multiplied by DT_s. In consequence, Eq. (28) can be used to select the capacitor value of C to obtain a given Δv_C. Eq. (28) is a lower boundary for C value, where C can be chosen such that a maximum Δv_C is attained for the worst boost DC-DC operating condition.

$$C = \frac{V_o}{2R\Delta v_C} DT_s \tag{28}$$

4. Passive elements' value determination

In this section, the boost DC-DC converter operating requirements are specified. Then, the values of the passive elements are determined such that operating requirements are fulfilled and system dynamical performance is achieved. Finally, the mathematical model is contrasted with a PSIM implementation of the boost DC-DC converter.

4.1 System operating requirements

In the boost DC-DC converter application, typical requirements are: input voltage range, output voltage range, output power range, output current range, operating frequency, output ripple, and efficiency. Unless otherwise noted, the continuous operating mode is assumed. The set of operating requirements for the boost DC-DC converter are specified in **Table 1**.

4.2 Zeros' location analysis

The values of the passive elements are selected to fulfill the operating requirements. The main interest is to choose suitable values for inductors and capacitors

Requirements	**Values**		
	Min	**Typ**	**Max**
Input voltage range	30 V	35 V	40 V
Output voltage range	50V	70 V	95 V
Output power range	0 W	100 W	300 W
Output current range	0A	2A	8A (At 50 V)
Operating frequency	100KHz		
Output current ripple	1%	5%	10%
Output voltage ripple	0.1%	0.5%	1%
Steady-state efficiency	90%	95%	98%
Load	25 Ω	50 Ω	100 Ω

Table 1.
Boost DC-DC converter operating requirements.

such that constraints like maximum physical admissible currents and voltages, converter efficiency, and converter CM are satisfied by keeping an acceptable dynamical system performance.

Expressions given by Eqs. (27) and (28) were deduced via steady-state analysis for lower inductor L and capacitor C boundaries, respectively. These expressions are suitable to choose L and C values as functions of Δi_L, Δv_c, states, and inputs in their steady-state value. Additionally, the expression given by Eq. (26) was deduced from the converter CM analysis, which allows to guarantee the boost DC-DC converter CCM operation in all the operating ranges by choosing suitable L and R values.

In PECs, it is desired that $\Delta i_L \leq \max(\Delta i_L)$ and $\Delta v_o \leq \max(\Delta v_o)$ should be assured in the entire operation range. Then, based on the worst condition for Δi_L and Δv_o, L and C lower boundaries can be deduced such that ripple constraints are satisfied. Eqs. (29) and (30) give lower boundaries for L and C, respectively.

$$L \geq \frac{\max(V_g) - \left(\frac{R_L}{\max(R)(1-D)} \min(V_o)\right)}{2\max(\Delta i_L)} DT_s \tag{29}$$

$$C \geq \frac{\max(V_o)}{2\min(R)\max(\Delta v_o)} DT_s \tag{30}$$

Eq. (26) also gives a minimum boundary for L value. Then, Eqs. (26) and (29) must be evaluated and the maximum L value must be selected as the lower boundary.

Eqs. (29) and (26) depend on R_C and R_L through α_C and $M(D)$, respectively. However, from the steady-state analysis, instead of calculating R_C and R_L values, it is suitable to establish α_C and α_L values. α_C and α_L values can be chosen such that the system efficiency is $\eta \geq 90\%$ in the entire operating range.

The maximum boost DC-DC conversion condition corresponds to $\max(M(D))$. Then, $\max(M(D)) = \max(V_o)/\min(V_g)$. According to the operating requirements in Table 1, $\min(V_g) = 30V$ and $\max(V_o) = 95V$, thus the maximum conversion condition in the example here presented is $\max(M(D)) \approx 3.17$. In consequence, loss ratios must be $\alpha_C < 0.05$ and $\alpha_L < 0.05$ when $R = \max(R) = 100\Omega$.

Figure 8 shows $M(D)$ and η curves for $R_L = 150m\Omega$, $R_C = 70m\Omega$, and $R = 25\Omega$, i.e., $\alpha_L = 0.006$ and $\alpha_C = 0.0034$. With these α_L and α_C values, it is assured that $\eta \geq 90\%$ and $M(D) \approx 3.17$. Two points are remarked over both $M(D)$ and η curves for the rated converter conversion condition $M(D) = 2$ and $M(D) \approx 3.17$. From **Figure 8(a)**, it is seen that the converter has sufficient boost capacity to guarantee that for $M(D) \approx 3.17$, the voltage requirement is satisfied. Additionally, from **Figure 8(b)**, it is

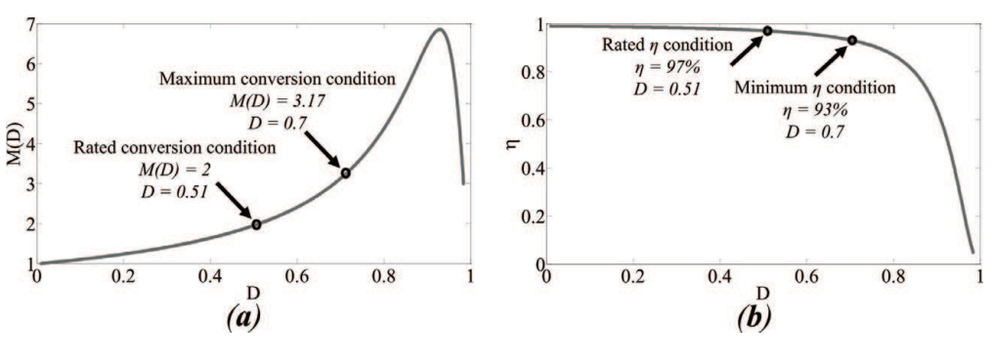

Figure 8.
(a) Conversion ratio $M(D)$. (b) Efficiency η.

seen that for $M(D) = 2$ and $M(D) \approx 3.17$, the converter has 97 and 93% of efficiency, respectively.

From Eq. (29), $\max(I_L) = \max(V_C)/\min(R)(1-D)$. Then, on the one hand, if $\max(\Delta i_L) = 0.1\max(I_L)$, $L \geq 326.34\mu H$ must be selected according to Eq. (29) in order to keep the converter in safe operation [22]. On the other hand, $L \geq 40\mu H$ to always operate in CCM by evaluating Eq. (26). The i_L ripple-based condition is a less restrictive boundary for L than the CCM-based condition. Therefore, $L \geq 326.34\mu H$ is the lower boundary for this element.

If $\max(\Delta v_C) = 0.01\max(V_o)$ in order to keep a converter in safe operation [22], $C \geq 14.120\mu F$ according to Eq. (30).

Minimum L and C values are selected as system parameters. Next, a simulation of the designed boost DC-DC converter is carried out. **Figure 9** shows the step system response for $V_g = 35V$, $V_o = 70V$, $I_o = 0A$, $L = 326.34\mu H$, $C = 14.120\mu F$, $R = 50\Omega$, $\alpha_C = 0.0034$, $\alpha_L = 0.006$, and $f_{sw} = 100kHz$.

From **Figure 9**, it is seen that, with minimum values of L and C, voltage overshoot is $O.S._{G_{vd}} = 57.4718\%$, current overshoot is $O.S._{G_{i_L d}} = 187.2323\%$, and system setting time is $ts = 3.03ms$. From **Figure 9(a)**, it is seen that the peak current value is $33.1686A$, while the steady-state current value is around $11.5477A$. From **Figure 9(b)**, it is seen that the peak voltage value is 214.5027 V, while the steady-state voltage value is around 136.2166 V.

A designed system with these overshoots needs to oversize its electronic devices such that these devices support both peak voltage and current values without system damage. However, such electronic devices can be expensive and inconvenient. For instance, in this chapter, an analysis of the boost DC-DC converter dynamical characteristics is carried out. This dynamical analysis studies the impact of L and C values over the zeros in transfer functions given by Eqs. (10) and (13), which determine overshoots and system setting time.

In a system as it is known, dynamical response is determined by poles and zeros' location [23]. Zeros are determined by the selected inputs and outputs of the system. Zeros' location is related to some system performance restrictions such as tracking limitations in feedback systems when classical control structures are employed [21, 22]. Moreover, large current or voltage overshoots in converter transient response can cause converter failures. PEC design process could take into account zeros' location due to L and C values such that the right half-plane (RHP) zeros are avoided or their impacts are attenuated. In consequence, the impact of L and C values over the zeros is analyzed to establish a trade-off between their values and the dynamical system response.

In the boost DC-DC converter d is chosen as control input, while v_g and i_o are considered disturbances. Thus, d variations' effect is of primary interest over system output. In consequence, duty ratio-to-voltage-output (G_{vd}) and duty-ratio-to-inductor-current $(G_{i_L d})$ transfer functions are studied. A simulation was carried out

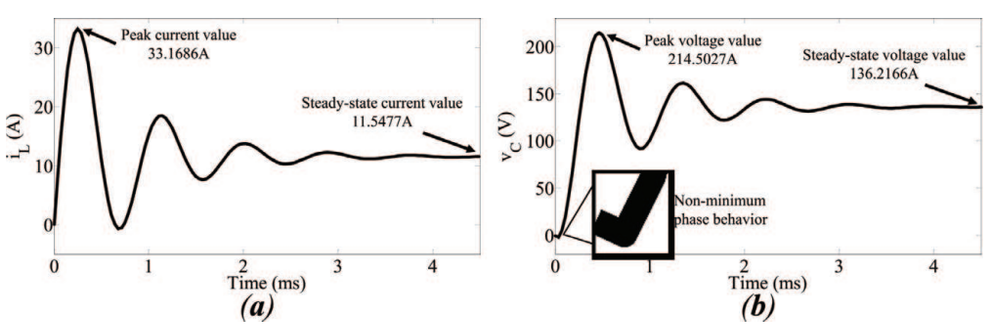

Figure 9.
(a) $G_{i_L d}$ step system response. (b) G_{vd} step system response.

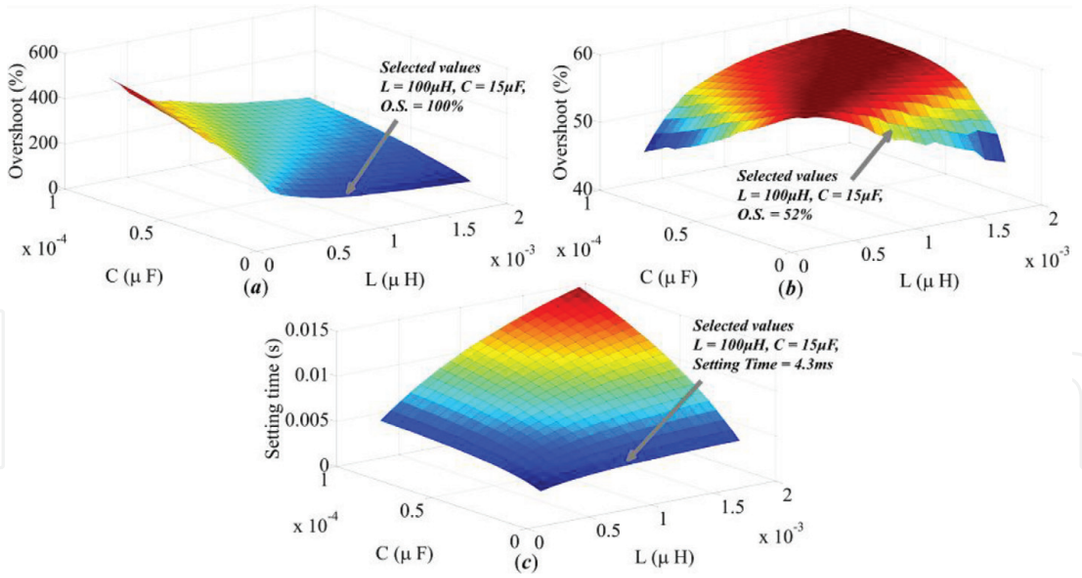

Figure 10.
(a) G_{vd} step system response for varying L and C: overshoot with zeros. (b) G_{i_Ld} step system response for varying L and C: overshoot with zeros. (c) Step system response varying L and C: setting time.

to evaluate the effects of large values for both L and C. **Figure 10** shows G_{vd} and G_{i_Ld} overshoots and setting time for $L \in [326.34\mu H, 2000\mu H]$ and $C \in [14.12\mu F, 100\mu F]$.

From **Figure 10**, it is seen that the minimum possible value of C causes maximum overshoot in v_o; while a minimum possible value of L causes maximum overshoot in i_L. Moreover, minimum C and L values give minimum system setting time.

In contrast, large values of C cause high overshoot of i_L; while large values of L cause high system setting time. In consequence, two additional design requirements are given in order to establish maximum possible values for L and C such that system overshoots and setting time are suitable: (a) maximum duty-ratio-to-output-voltage overshoot $\max\left(O.S._{G_{vd}}\right)$ and (b) maximum duty-ratio-to-inductor-current overshoot $\max\left(O.S._{G_{i_Ld}}\right)$.

From **Figure 10**, it is seen that the system dynamical response cannot be modified if the values of both L and C are simultaneously increased. Meanwhile, if either L or C values are increased, both $O.S._{G_{vd}}$ and $O.S._{G_{i_Ld}}$ decrease. Nevertheless, larger values of L have a major impact than larger values of C.

$L = 1mH$ and $C = 15\mu F$ are selected by results shown in **Figure 10** since with these values $O.S._{G_{i_Ld}} \approx 105\%$ and $O.S._{G_{vd}} \approx 53\%$, i.e., $O.S._{G_{i_Ld}}$ is approximately reduced to 82% and $O.S._{G_{vd}}$ is approximately reduced to 4%. Furthermore, $ts = 4.32ms$, i.e., the system setting time is only increased by $1.3ms$. Thus, these L and C values establish a trade-off between system overshoots and performance. It is remarked that selected L and C values are commercially available.

4.3 System frequency response verification

Frequency response of both the mathematical model and a PSIM circuital implementation are contrasted in order to validate the dynamical model of the designed boost DC-DC converter via simulation. The boost DC-DC converter was parameterized with $L = 1mH$, $C = 15\mu F$, $V_g = 35V$, $V_o = 70V$, $I_o = 0A$, $\alpha_C = 0.0034$, $\alpha_L = 0.006$, $R = 50\Omega$, and $f_{sw} = 100kHz$. In consequence, $I_L = 2.8812A$ and $D = 0.5141$ in the equilibrium point.

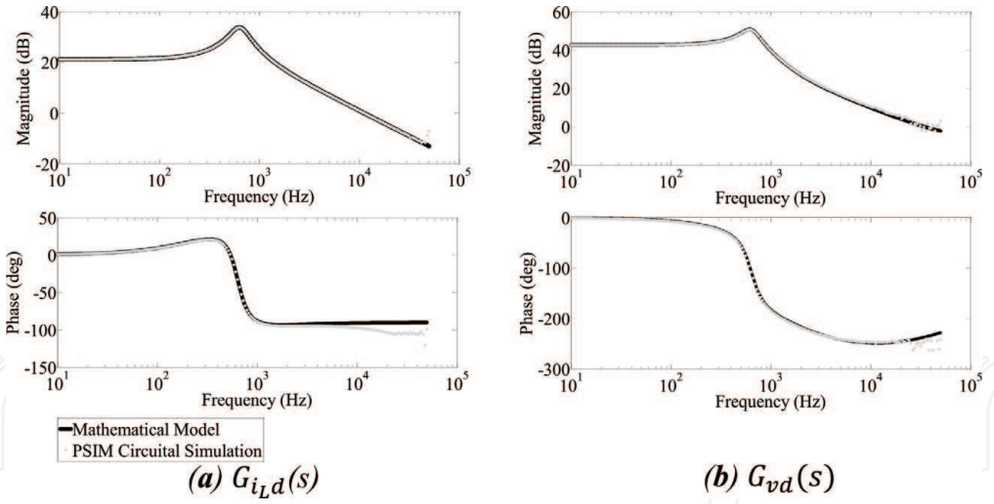

Figure 11.
(a) $G_{i_L d}$ Bode diagram. (b) G_{vd} Bode diagram.

Figure 11 presents the boost DC-DC converter Bode diagrams of the PSIM circuital implementation and the mathematical model given by Eqs. (10)–(15). The frequency response of the PSIM circuital implementation matches with the mathematical model. Then, the PSIM circuital implementation is satisfactorily reproduced by the mathematical model.

5. Control structure design

Nonminimum phase behavior is a well-known result derived from the boost DC-DC converter study [24]. To avoid this system behavior, a CMC structure has been proposed [18, 24]. Nonminimum phase behavior is avoided with this control structure since both $G_{i_L d}$ and inductor-current-to-output-voltage $G_{v_o i_{L_{REF}}}$ transfer functions have a minimum phase behavior.

The converter control design is focused on imposing a desired low-frequency behavior on the system. Here, a CMC structure for the boost DC-DC converter is designed. The aim is to tune PI controllers such that the control objective is achieved. **Figure 12** shows the CMC structure for the DC-DC boost converter. As it is seen in **Figure 12**, the CMC structure employs two PI controllers: first one for i_L control and second one for v_o regulation. These PI controllers are arranged in master-slave form; where i_L control loop is the inner loop and v_o control loop is the outer loop. This master-slave arrangement allows v_o regulation while preserving i_L within specified safety limits.

In the boost DC-DC converter which operates in a switch-mode power supply and feeds a certain variable load, the d needs adjustments in order to ensure a constant v_o for the entire operating range (voltage regulation). Besides, against any system disturbance (v_g and i_o random changes), the d value should be adjusted to drive the system back to the operating point. The PI controller in the outer loop provides the set-point of the inner loop, which acts as the control input of the outer loop. The proportional and integral (PI) controller in the inner loop generates a continuous signal for d, which by means of a pulse width modulation (PWM) is applied to the power switching gate.

5.1 Controller tuning

Controller's tuning task begins with the set of design specifications. The goal of the boost DC-DC converter controller is to maintain v_o within 2% of its rated value

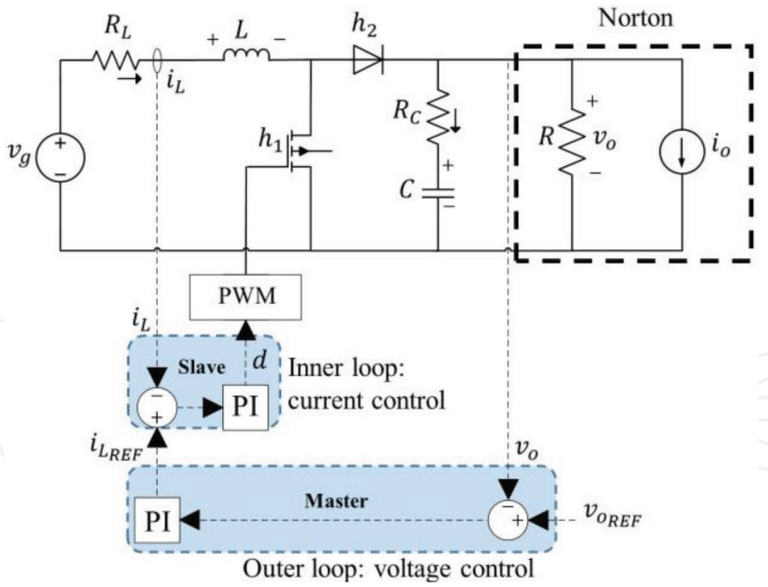

Figure 12.
Boost DC-DC CMC structure scheme.

(i.e., $68.6V$–$71.4V$) in response to random changes (disturbances) in both v_g and i_o. Also, the controller should be able to drive v_o within the tolerance for v_g variations over a range from 30 to $40V$.

The inner loop control bandwidth must be $20kHz$ or less due to the fact that f_{sw} is equal to $100kHz$, and the outer loop control bandwidth must be smaller than 1/5 of the inner loop control bandwidth [25], i.e., smaller than $5kHz$. Additionally, a robustness index of M_s<2 is desired to establish a trade-off between control performance and robustness [26].

A PI controller was tuned by acting directly on d to track the inductor current reference $i_{L_{REF}}$ since $G_{i_L d}$ exhibits a minimum phase behavior. The inductor current PI controller was tuned by means of the root-locus technique, adopting the following design specifications: damping factor ζ equal to 0.707 and a $20kHz$ closed-loop bandwidth. The tuned PI controller transfer function $G_{C_{i_L}}(s)$ is given by Eq. (31). These PI controller design specifications ensure: (a) Zero steady-state error and a satisfactory reference tracking for frequencies below $20kHz$; this is observed on transfer function $T_{i_L i_{L_{REF}}}$ in **Figure 13**. (b) Effective disturbance rejection for both input voltage v_g and current source i_o variations, which are observed on transfer functions $T_{i_L v_g}$ and $T_{i_L i_o}$ in **Figure 13**, respectively. (c) A closed-loop robustness $M_s = 1.2$.

$$G_{C_{i_L}}(s) = \frac{1.27s + 55218}{s} \tag{31}$$

A PI controller was tuned to regulate v_o since the $G_{v_o i_{L_{REF}}}(s)$ transfer function given by the Eq. (18) exhibits a minimum phase behavior. This PI controller provides the set-point of the inner control loop. The PI controller of the outer control loop was tuned by means of the root-locus technique considering a damping factor ζ equal to 0.707 and a $5kHz$ closed-loop bandwidth. The tuned PI controller transfer function $G_{C_{v_o}}(s)$ is given by Eq. (32). These PI controller design specifications ensure: (a) Zero steady-state error observed on transfer function $T_{v_o v_{o_{REF}}}$ in **Figure 14**. (b) Effective disturbance rejection for the current source i_o variations, which are observed on transfer function $T_{v_o i_o}$ in **Figure 14**. (c) A closed-loop robustness $M_s = 1.2$.

$$G_{C_{vo}}(s) = \frac{0.07994s + 235.1}{s} \tag{32}$$

5.2 Closed-loop system performance verification

The designed boost DC-DC converter with its control structure was implemented in PSIM to assess the closed-loop system robustness. Three cases were proposed to evaluate the control structure robustness against most common disturbances. (i) An experiment that simulates a change of ±35% around the nominal value of the load was carried out. Next, (ii) an experiment that simulates a change of ±15% around the nominal value of the input voltage was carried out. Finally,

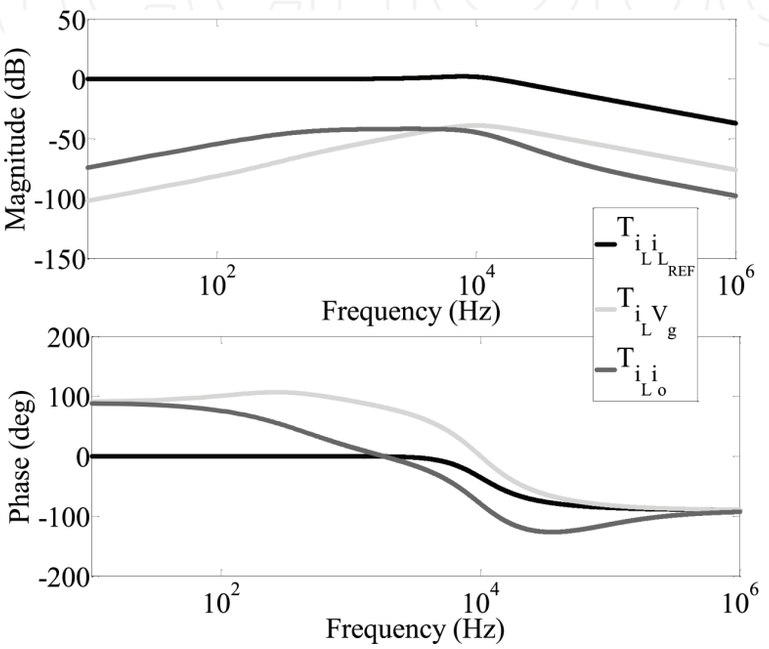

Figure 13.
Inner current control loop transfer functions.

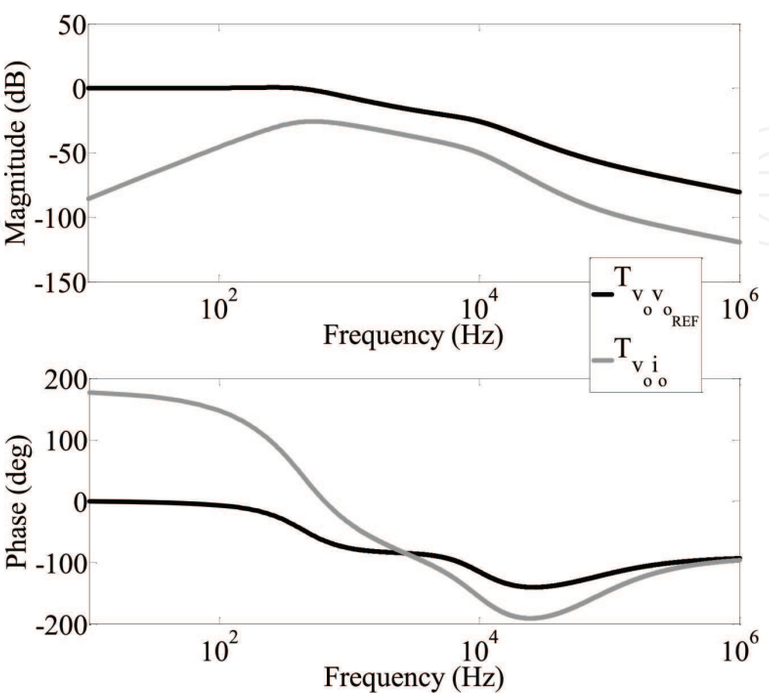

Figure 14.
Outer output voltage control loop transfer functions.

(iii) an experiment that simulates a combined change of ±35 and ±30% around the nominal values of the load and the input voltage, respectively, was carried out. **Figure 15** shows the dynamical system response against the perturbations mentioned above. From **Figure 15**, it is seen that the system stability is not affected by any of the simulated perturbations, which means that the control structure is robust against the system perturbations from both the load and the input voltage up to 35%.

Figure 15(a) shows the closed-loop behavior at unit step changes of i_o around the operating point corresponding to the full load. Two i_o unit step changes were applied to evaluate the control structure performance. The first step change was applied at $t = 10ms$ for $10ms$, then the current source returns to its rated value $i_o = 0A$. The second unit step change was applied at $t = 30ms$ for $10ms$, then the current source returns to its rated value $i_o = 0A$. In **Figure 15(a)**, a satisfactory tracking of $i_{L_{REF}}$ and regulation of v_o to reject load disturbances depicted as changes in i_o is observed.

Figure 15(b) shows the closed-loop behavior at unit step changes of v_g. Two v_g unit step changes were applied to evaluate the control structure capabilities to regulate v_o and to evaluate the capabilities of the designed boost DC-DC converter. The first unit step change was applied at $t = 10ms$ for $10ms$. This first unit step change was equal to $v_g = -5V$, i.e., the final value of the input voltage was $v_g = 30V$ that corresponds with its lower boundary. The second unit step change was applied at $t = 30ms$ for $10ms$. This second unit step change was equal to $v_g = +5V$, i.e., the final value of the input voltage was $v_g = 40V$ that corresponds to its upper boundary. In **Figure 15(b)** a satisfactory reference tracking of $i_{L_{REF}}$ and control regulation of v_o to changes in v_g is observed. It is important to remark that under the worst condition for v_g, the boost DC-DC converter was able to keep v_o in its rated value.

Finally, **Figure 15(c)** shows the closed-loop behavior at random unit step changes of both i_o and v_g. These unit step changes were applied such that the designed control structure performance could be evaluated against any random disturbance. From **Figure 15(c)**, it is possible to see that the designed control structure has a satisfactory performance against multiple disturbances within specified design requirements for the boost DC-DC converter in **Table 1**.

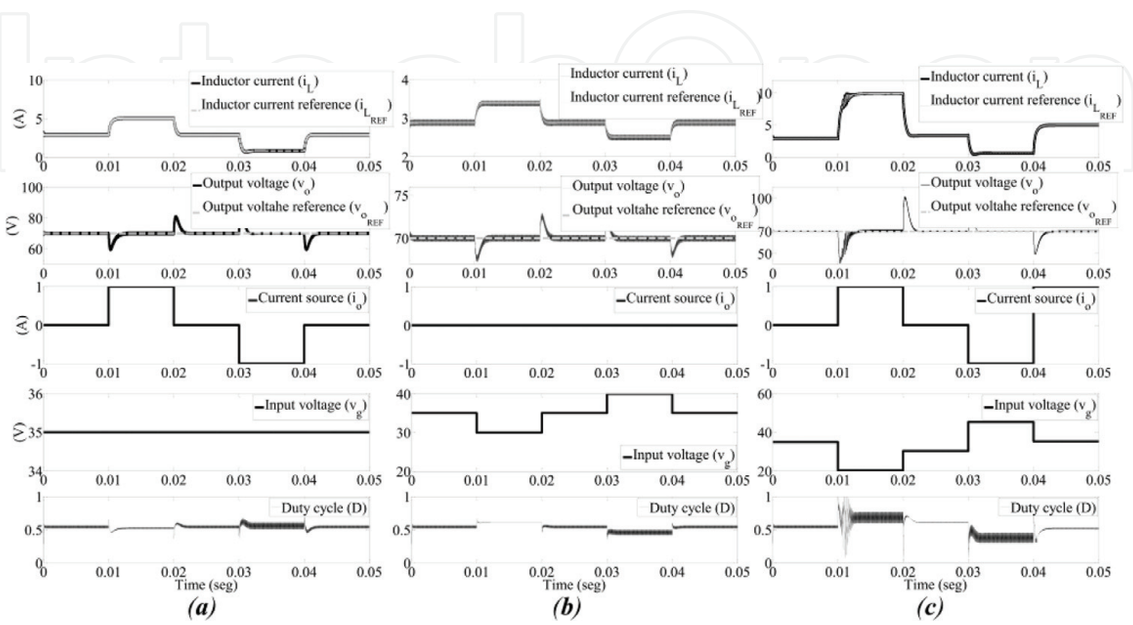

Figure 15.
Closed-loop behavior at unit steps system disturbances.

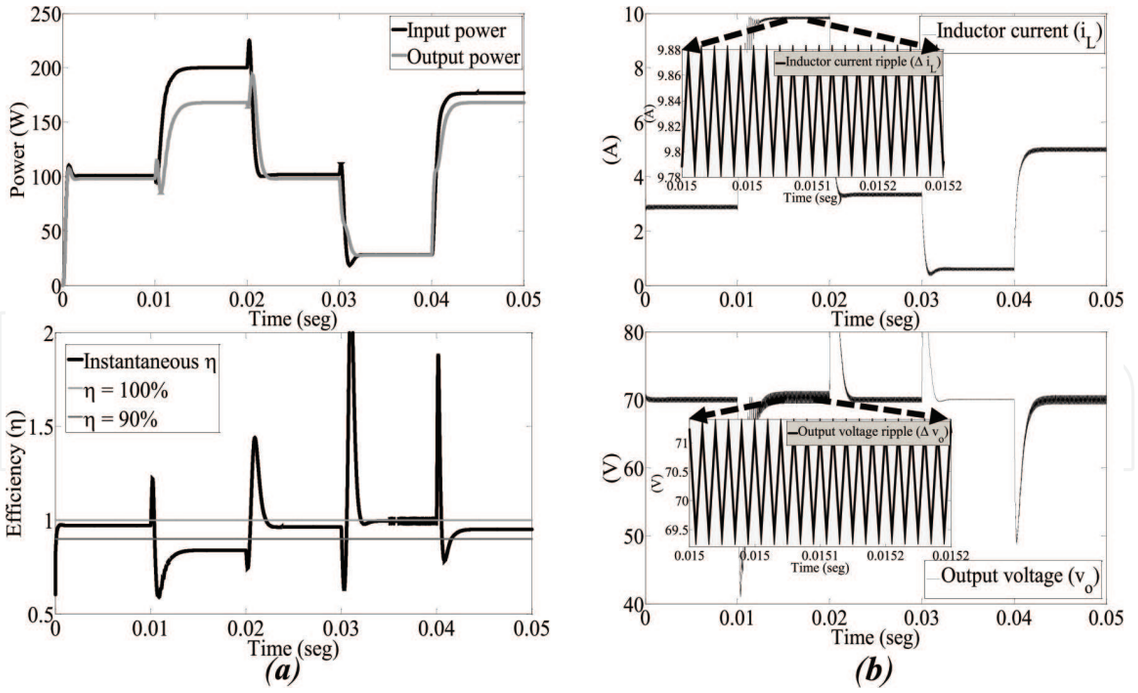

Figure 16.
(a) Instantaneous Power verification. (b) Ripples verification.

In order to carry out system operation requirements verification, case (c) of **Figure 15** is taken into account. **Figure 16** shows: (a) P_{in}, P_{out} and (b) i_L and v_o, when case (c) of **Figure 15** is considered.

From **Figure 16(a)**, it is seen that P_{out} does not exceed the maximum admissible output power in steady state and is always lower than P_{in}. (b). **Figure 16(b)** shows i_L and v_o. A zoom was made for the worst simulated system condition. From **Figure 16(b)**, it is seen that even in the worst i_L and v_o condition, Δi_L and Δv_o are below 1%. Accordingly, the designed boost DC-DC converter satisfies both Δi_L and Δv_o conditions.

In conclusion, **Figure 16** shows that the boost DC-DC converter system operating requirements given in Table 1 are successfully satisfied.

6. Conclusions

In this chapter, a procedure to easily design and control PECs was proposed and zeros' location impact over the system dynamical responses was analyzed, showing that a careful selection of the PEC passive elements could both avoid electronic device failure due to large overshoots and improve the dynamical system performance. Parasitic losses R_L and R_C were included in order to have a more realistic approach to the system. The presented procedure was composed of:

a. The nonlinear dynamical system modeling approach to obtain a mathematical tool and evaluate the system performance. The obtained dynamical model was suitable to describe the dynamical behavior of the system and to derive the steady-state model.

b. The steady-state analysis that allowed to find suitable constraints for passive elements' values. The steady-state analysis was composed of: (a) $M(D)$ expression derivation, (b) losses effect analysis and η expression derivation, (c) conditions for analysis of CCM and DCM, and (d) Δi_L and Δv_C analyses.

c. The passive elements' value determination based on the system zeros' location. A zero-based analysis allowed to choose the passive elements' values such that a trade-off between operating requirements and system transient response were achieved. This analysis reduced the system outputs' overshoot alleviating electronic devices' stress and improving the system's performance.

d. The proposal of a model-based control structure; particularly, a CMC structure based on PI controllers for automatic converter control was implemented in the boost DC-DC converter, although a control structure does not need to be fixed in this procedure.

e. The procedure was applied to a boost DC-DC converter application taking into account the parasitic losses associated with its passive elements, which allows to investigate the details of its performance, operation, and behavior. It was possible to design a boost DC-DC converter that fulfills all the operating requirements in the entire operating range, even if bounded disturbances appear. Design was based on the nonlinear dynamical model and steady-state analysis. The CMC structure was implemented for the designed boost DC-DC converter. PI controllers were tuned by means of root-locus controller design method. The boost DC-DC converter was implemented in PSIM where system operating requirements, closed-loop performance, and robustness were successfully verified.

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Conflict of interest

The authors declare no conflict of interest.

Author contributions

Jorge H. Urrea-Quintero carried out most of the work presented here, Nicolás Muñoz-Galeano was the advisor of this work, and Lina M. Gómez had a relevant contribution with her extensive knowledge about systems theory.

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