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# MOS Meets NEMS: The Born of Hybrid Devices

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Additional information is available at the end of the chapter

## Abstract

Nowadays, the semiconductor industry is reaching an impasse due to the scaling-down process according to Moore's Law, initiated back in 1960s, for the Metal-Oxide-Technology in use. To overcome such issue, the semiconductor industry started to foresee novel materials that allow the development of nanodevices with a broad variety of characteristics such as high switching speed, low power consumption, robust, among others; that can overcome the inherent issues for Silicon. A few "exotic materials" appear such as Graphene, $MoS_2$, BN-h, among others. However, the time for the novel technology to be mature is a few decades in the future. To allow the "exotic materials" to mature, the semiconductor industry requires of novel nano-structures that can overcome a few of the issues that Silicon-based technology is facing today. A key alternative is based on hybrid structures. Hybrid structures encompass two dissimilar technologies nano-electromechanical systems with the well known Metal-Oxide-Technology. The hybrid nano-structure provides a broad variety of options to be used in such as transistors, memories and sensors. These hybrid devices can give enough time for the technology based on "exotic materials" to be reliable as Silicon based is.

**Keywords:** hybrid devices, MEMS/NEMS, MOS technology, nano-electronics, exotic materials, bio-applications, aerospace, military applications

## 1. Introduction

The semiconductor industry has been paved the way for the development of science and technology for more than half-century. Within this time, the development of different sciences such as medicine, biology, archaeology, law, among others has been benefited by the semiconductor industry through the materials as well as the electronics devices/systems developed. By continuing allowing the development of such devices/systems, the semiconductor industry based whole scientific and technologic development in Moore's Law, established back in the 1960s [1]. By following it, nowadays it is possible to get high power processing computing at low cost, high definition graphics for portable video games that consider low power consumption as well as lightweight.

This romantic trend continued for a long time until the scaling-down process due to the Moore's Law became an impasse. According to the International Technology Roadmap for Semiconductors (ITRS) [2], within the "in-use" Metal-Oxide-Semiconductor technology (MOS), by continuing with the scaling-down trend, the tunnel oxide layer cannot be thinner than 7 nm in order to avoid a leakage issue. The issue should be appropriately addressed by migrating the silicon-based technology to other materials that can cope with the requirements that the semiconductor industry needs. It was found that a few materials match the requirements such as chalcogenides, Graphene, Diamond, CNTs, $MoS_2$, BN-h, among others [3–8]. However, this novel technology takes time to be developed as well as to be mature enough to be reliable. In the meantime, it is needed to fill the gap in time and technology by considering some novel structures that can be used to overcome the inherent MOS issues until the novel technology is available. An option that came across is the use of hybrid devices that encompasses the well-known MOS technology with a nanoelectromechanical systems (NEMS).

To understand the use of such technologies, this chapter is divided into a brief introduction, in Section 2 a review of MOS technology is to understand how does it work. Section 3 shows the characteristics of the nanoelectromechanical systems. Section 4 the hybrid structures are introduced as a merge between the two technologies giving several examples of the reliability of the hybrid structures. In Section 6, several examples that can be implemented for key industrial applications are exposed and finally, a resume of the hybrid devices and the importance of them for the semiconductor industry.

## 2. Metal oxide semiconductor technology

Metal oxide semiconductor (MOS) technology has been used to develop a wide variety of devices ranging from memories, sensors, clocks up to quite complicated systems such as mobile phones, personal computers, satellites or even fridges. The main aim to develop all those systems as well as the science and technology that made them possible are based on a statement made a few years back in the 1960s by Gordon Moore that is known as Moore's Law [1]. According to Moore's law, the number of devices fabricated should be twice the previous number every 24 months over the same area. By following such law, the semiconductor
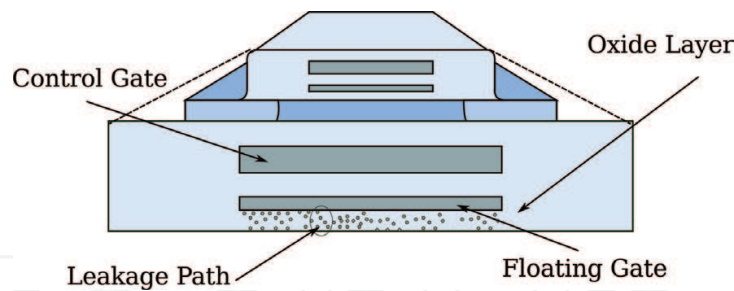
**Figure 1.** Schematic diagram of a metal-oxide-semiconductor transistor featuring the leakage path due to the scaling-down process.

industry has been capable of delivering, with small variations, this trend for a half century. However, by continuing this trend, MOS technology is reaching an impasse produced by the scaling-down process due to the tunnel oxide layer within the floating gate structure as depicted in **Figure 1**.

According to the International Technology Roadmap for Semiconductors (ITRS) [2], the tunnel oxide layer cannot be thinner than 7 nm due to leaking issues towards the substrate or to the control gate. To overcome such issue, it is required to foreseen for novel materials beyond Si or Ge. This is why, from 2007 the semiconductor industry started to search for materials that can fulfil critical requirements to develop novel devices with improved capabilities such as low-power consumption, high switching speed, scalable capabilities, robust, multi-functional, co-integration capabilities similar as for Si-based devices, among others.

As a result, several materials that present those characteristics such as Graphene, $MoS_2$, Diamond, BN-h were found [9–13]. Above mentioned materials are capable to deliver the requirements that the semiconductor industry desperately needs. However, there is a time that the "exotic materials" need to mature to be robust enough to feed the market with novel devices [8, 12, 14]. To continue feeding the market, the semiconductor industry requires using the whole set of tools and technology developed over a half-century to give enough time to improve the devices/technology for the emerging technologies.

A key technology that can allow to the semiconductor industry to give enough time to mature the emerging technologies is based on Micro/nanoelectromechanical systems (MEMS/NEMS) that can be co-integrated with the well-known MOS technology. The co-integration between those unique technologies can allow a broad variety of novel devices with the capabilities of robustness as well as maturity and improved characteristics as similar Si-based devices.

## 3. MEMS/NEMS

The micro-electromechanical systems or micro systems technology is a technology developed in the early 1980s. This technology appears as a result of a lecture given in Caltech 1959 by Prof. Richard Feynman "There's Plenty of Room at the Bottom" [15]. The lecture re-shape the Si-based semiconductor industry to foreseen novel applications for micromachines. MEMS

technology encompasses a series of materials that interact with the media allowing to move some parts within it to detect or to have a response according to the media while biased. Typical characteristics for this technology feature components between 1 to 100 $\mu$m, a complete system can range from a few tens of microns up to 1 mm. The first MEM fabricated was a large mirror array that was capable to move while bias each axes. The fabrication process developed for such technology was in early stages. From this point, novel processes were proposed and mastered to remove key layers known as a sacrificial layer to free layers within the device or to create holes for particular purposes as well as to deliver a smooth material deposition to accurately shape the features required for the proper operation of the NEM under fabrication. A process needed to be standardised is based on the etching processes that encompasses both wet etching (KOH, TMAH, FNA, …) and dry etching (RIE, DRIE, … [16–18]).

At this point, MEMS technology needed to scale-down by following the Moore's law in order to become relevant for the semiconductor market. By improving the Si-based fabrication processes as well as the etching and lithography processes, the micro-electromechanical systems became the nanoelectromechanical systems (NEMS). NEMS feature a working range from few up to hundreds of nanometres, ultra-low power consumption, reliable, scalable, robust, among others. By considering that NEMS has been scaled-down by following Moore's law, as semiconductor industry states, it is possible to co-integrate them by the well-known MOS technology due to both consider the same substrate and can be merged within the same die (Si-based).

By developing the proper fabrication processes and due to the feature size for MOS as well as for NEMS devices, the co-integration for both dissimilar technologies it is now possible. As the development for such hybrid structures are in its early stages and there is no specialised software to analyse the nanostructure but software based on physic properties that encompassed a wide variety of scientific branches. It is a drawback that is being overcome by performing an algebraic analysis of the NEM structure coupled to the MOS device. This method has been widely used delivering accurate results as measurements can confirm [19, 20].

To deliver the set of hybrid devices that semiconductor industry requires to flow the market, we require a set of novel devices that can be co-integrated within the same die to reduce fabrication cost, improve reliability as well as to overcome previous drawbacks inherent to MOS technology. A few of the nanodevices already fabricated are based on simple structures such as single/double clamp beams, membranes and pillars [20]. Furthermore, one of the main drawbacks from MOS technology, scaling-down feature, has been successfully overcome as exposed elsewhere [21, 22].

## 4. NEMS-MOS: hybrid devices

As state-of-the-art devices, in this section we are going to analyse the most common nanostructures that encompass NEMS with a MOS technology such as transistors, sensors, non-volatile memories and high-Q resonators, to name a few.

### 4.1. Hybrid transistor

In general, the MOS transistor works by biasing the source and drain, in order to generate the full channel, it is required a signal from the gate to close it up and connect both terminals as shown in **Figure 2**.
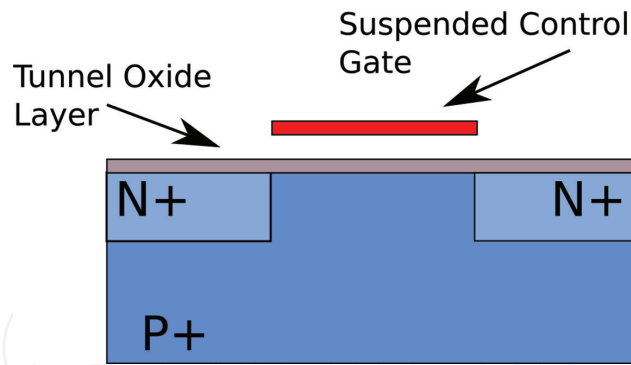
**Figure 2.** Pull-in curves featuring a scaling-down process. It is possible to observe that by reducing the key characteristics of the double-clamped beam, the pull-in as well as the applied voltage is also reduced.
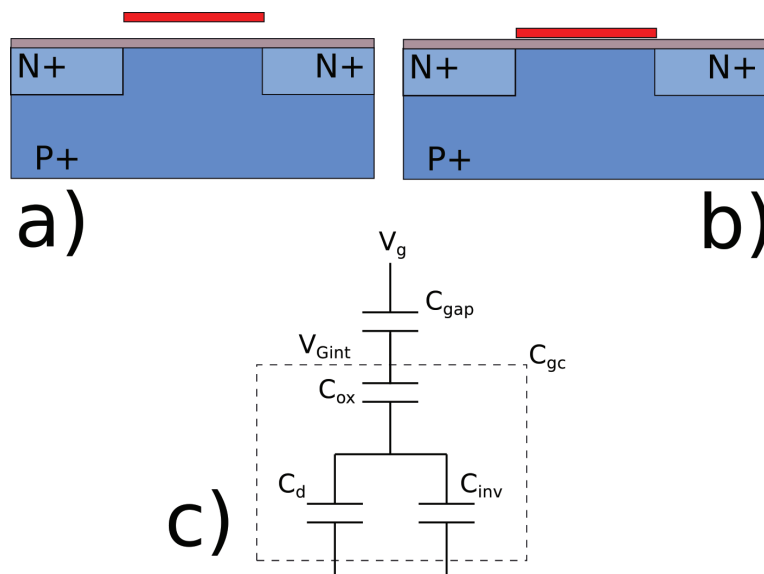


**Figure 3.** Set of images that depict the full operation of the suspended control gate transistor. a) Shows the suspended gate transistor unbiased. b) Depicts the SG-transistor biased and c) shows the equivalent model for the SG-MOS.

By performing the scaling-down process as Moore's law state, the MOS transistor will fence an impasse due to the tunnel oxide layer cannot be reduced further [2]. Therefore, the suspended gate MOS transistor (SG-MOS) reached the stage. **Figure 3** shows the schematic diagram of the full behaviour of the SG-MOS. A model that describe the full comportment of such device considers a set of capacitors.

The equation that describes the gate voltage according to the model is:

$$V_{Gin} = \frac{V_G}{1 + \dfrac{C_{gc}}{C_{gap}}} \tag{1}$$

### 4.1.1. Electro-mechanical modelling

To model the suspended gate with the bulk MOSFET, it is required to analyse it by considering the total energy between the conductive plates that store the energy defined as

$$E_{tot} = E_{elect} - E_{mech} = \frac{1}{2} C_{gap} V^2 - \frac{ky^2}{2} \tag{2}$$

At mechanical equilibrium, the displacement is zero, the gap capacitance is

$$C_{gap} = \frac{A \epsilon_r \epsilon_0}{t_{gap}} \tag{3}$$

where $A$ is the plate area, $t_{gap}$ is defined as the air-gap and $\epsilon_r$ and $\epsilon_0$ are the material and space permittivity, respectively. While biased, the voltage between gate and substrate is coupled by the capacitance gate to channel as $V = V_G - V_{int}$ and the electrostatic force is defined as

$$F_{elec} = \frac{\epsilon_0 A}{2 y^2} (V_G - V_{int})^2 = ky \tag{4}$$

where $y$ is the vertical gate displacement, $A$ is the overlap area and $k$ is the gate stiffness.

### 4.1.2. Pull-in and pull-out effect

When the transistor is biased, the gate is bent downwards due to the electrostatic force. By increasing it, the electrostatic force overcomes the material stiffness ($k$) that is function of shape defined as $F_k = ky$. By balancing both forces, the stiffness can be modelled as

$$k(t_{gap} - y) = \frac{\epsilon_0 A}{(t_{gap} - y)^2} (V_A - V_{int})^2 \tag{5}$$

where $t_{gap}$ is the initial air-gap, material stiffness is geometry dependent that is defined as

$$k_0 = \frac{192EI}{L_{beam}^3} \tag{6}$$

where $E$ is the Young's modulus, $I$ is the bending inertia moment for a rectangular beam shape. Restoring force is a linear displacement function that couples to the electrostatic force as an inversely quadratic function. Thus, there is an unstable point while the equilibrium point surpasses by biasing the structure defined as

$$y \geq \frac{2}{3} t_{gap} \tag{7}$$

The suspended gate deflection process is performed by increasing the voltage linearly until a point known as the pull-in voltage due to electrostatic force is reached. Beyond this point, the beam will collapse on the substrate due to electrostatic instability produced for the overcome of the material stiffness by the electrostatic force [23]. For a double-clamped beam, the pull-in voltage is defined as

$$V_{pull-in} = \sqrt{\frac{8 k t_{gap}^3}{27 \epsilon_0 WL}} \tag{8}$$
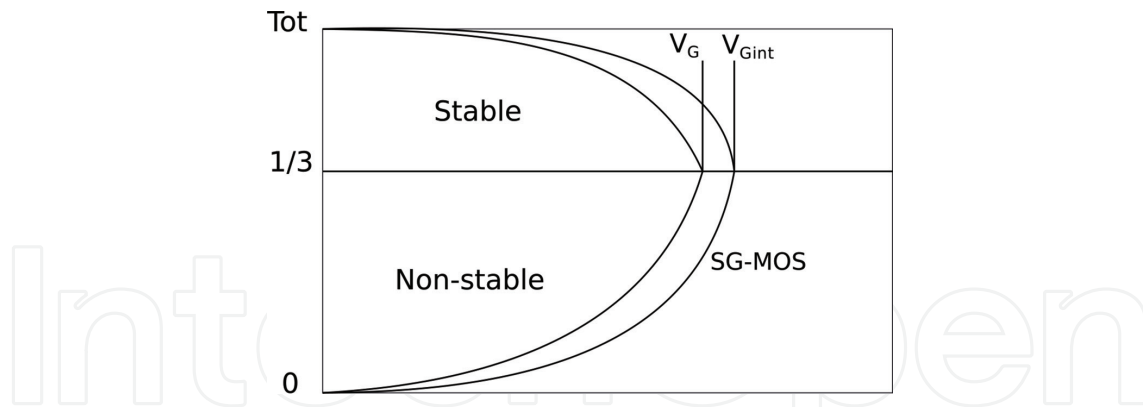
**Figure 4.** Schematic set of curves that define the stable and non-stable region for an initial air-gap. Approximately at one-third of the total air-gap the electrostatic force overcomes the material stiffness and the beam collapses producing the pull-in effect.
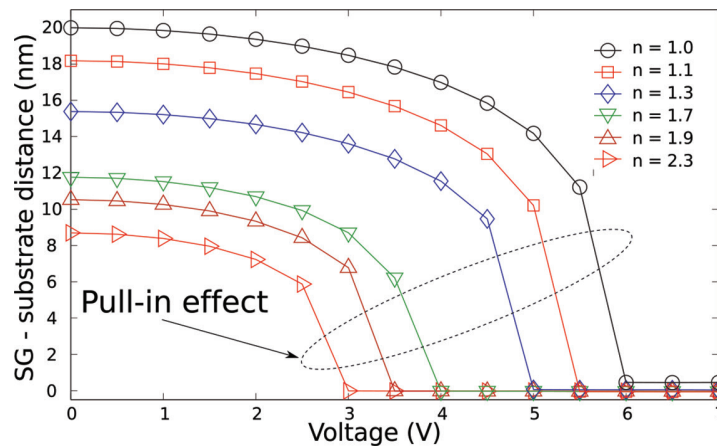


**Figure 5.** Pull-in curves featuring a scaling-down process. It is possible to observe that by reducing the key characteristics of the double-clamped beam, the pull-in as well as the applied voltage is also reduced.

where, $W$ is the width, $L$ is the channel length, $V_{pull-in}$ is the pull-in voltage. Stable and non-stable regions that define the pull-in voltage is depicted in **Figure 4**.

Pull-in voltage is strongly related to several key parameters such as beam thickness, permittivity and channel dimensions. **Figure 5** shows the pull-in effect for a set of parameters and how those are affected by scaling them down by a factor.

While the gate is collapsed on the substrate and by increasing the applied voltage, the contact area increases. By reducing it, the beam will remain attached to the substrate until the material stiffness overcomes the electrostatic force. When the beam is released due to the unbalance between those forces, the channel is interrupted. This point is it known as the pull-out effect as shown in **Figure 6**.

### 4.1.3. Low-range forces: Casimir and van der Waals forces

The electrostatic force is responsible for the suspended gate collapse on the substrate and as a consequence generate the channel when biased. To reduce the applied voltage, dimensions
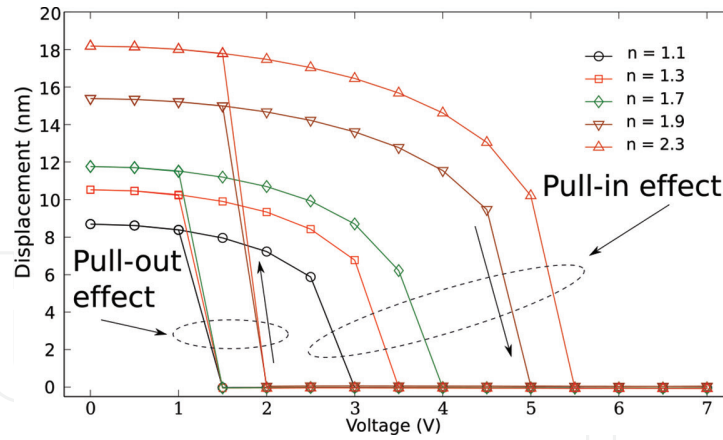
**Figure 6.** Pull-in curves featuring a scaling-down process. It is possible to observe that by reducing the key characteristics of the double-clamped beam, the pull-in as well as the applied voltage is also reduced.

are shrunk and as consequence other forces that only were considered to appear in systems with low dimensionality are now key for the optimal behaviour of the nanodevices: Casimir and van de Waals Forces.

In general terms, Casimir effect is strongly related to the field radiation pressure that can be generated by an electromagnetic field on every plate surface. While in contact, the Casimir force is stronger than the electrostatic force and the restitution force produced by the material stiffness.

$$F_{Casimir} = -\frac{\pi^2 hcA_{plates}}{480\, d_o^4} \tag{9}$$

where, $A_{plates}$ is the contact area between plates, $h$ is the Plank constant and $c$ is the speed of light. Moreover, due to the low proximity between surfaces, the van der Waals force also appears. Van der Waals force occurs at low proximity, usually between 1 and 2 nm of separation. This force is shape dependent and it is strongly related to the Hamaker constant that encompasses the material behaviour as permittivity ($\epsilon$) and refractive index (n) [24].Once the whole set of forces that intervene in the SG-MOS operation are put, it is possible to numerically analyse the hybrid device to later on, continue with the fabrication process and characterisation of the device.

### 4.2. Non-volatile memory

Another key device that has allowed the semiconductor industry to overcome a few issues such as programming/erasing speed as well as scaling-down process and low power consumption, the suspended gate silicon nanodot memory (SGSNM). The SGSNM is a hybrid device that encompasses dissimilar technologies to overcome the issues inherent to MOS technology. The non-volatile memory features a MOS transistor as readout element, a memory node fabricated with a silicon nanodots monolayer and a control gate that is double-isolated by a thin tunnel oxide layer and an air-gap as shown in **Figure 7**.

Similarly, as for the SG-MOS transistor, the SGSNM is driven by the suspended control gate to either inject or retract electrons from the memory node through the tunnel oxide layer as shown by the schematic diagram in **Figure 8**.
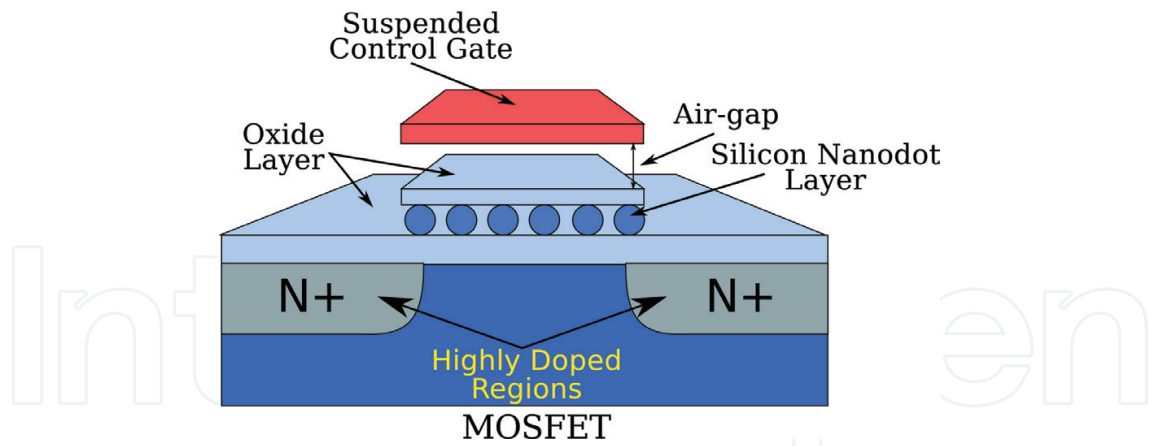
**Figure 7.** Schematic diagram of a hybrid nanostructure that features a non-volatile memory device. The memory features a MOSFET as readout element, a memory node fabricated with a monolayer of silicon nanodots embedded within a $SiO_2$ layer. The control gate is doubly-isolated by an air-gap and by a thin tunnel oxide layer.
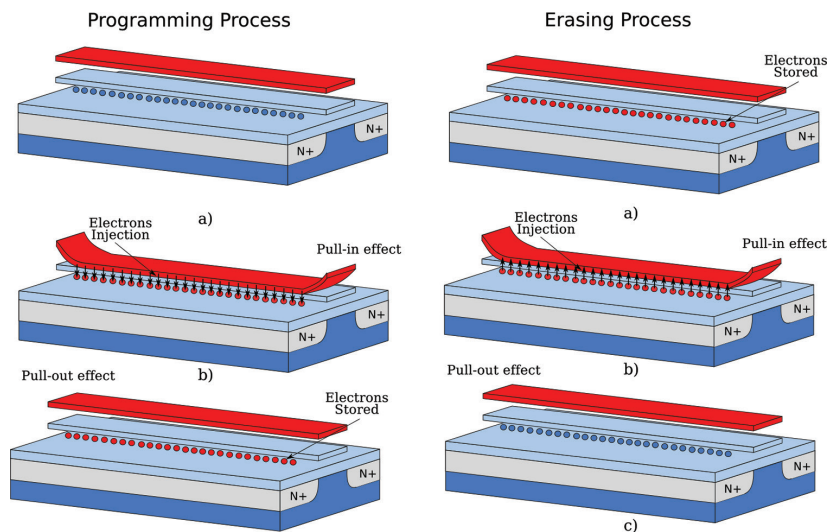


**Figure 8.** Schematic programming and erasing diagram for the hybrid nanodevice structure. In here, the programming and erasing feature of the nanodevice is defined. While applying a negative voltage, the suspended control gate will collapse on the tunnel oxide layer due to the electrostatic force (pull-in effect). Once in contact, the electrons will be injected into the memory node and by reducing the applied voltage, the pull-out voltage will allow to the control gate to return to its initial isolated position. It is possible to see that in the memory node the electrons are stored. On the other hand, by applying a positive voltage, the control gate will collapse and the electrons will be removed from the memory node until the pull-out voltage is reached. As a result, the memory node is empty.

The non-volatile hybrid device requires to improve a few of the inherent issues that MOS technology has. Therefore, a robust numerical analysis is needed. As point out elsewhere, there are not specific software available for such analysis. Hence, a combination of the commercial software available the set of numerical analyses is performed. To get the entire behaviour, it is needed to analyse the suspended control gate under different bias. The injection of electrons from the control gate towards the memory node and inversely is also considered. The above mentioned behaviour is required to be implemented as a library within a robust commercial software standard for the circuit simulation such as Spice [25].
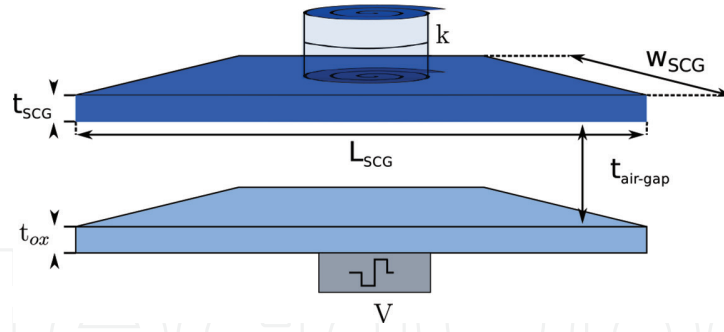
**Figure 9.** Schematic diagram of a two-plate capacitor that features the critical parameters to analyse the pull-in voltage.

### 4.2.1. Suspended control gate

The suspended control gate for the SGSNM is a double-clamped beam as featured in **Figure 9**. The beam can be modelled considering a few essential characteristics such as beam permittivity, thickness, air-gap space and substrate permittivity. As shown in **Figure 9**, a two-plate capacitor model is considered to obtain algebraically the pull-in as well as the pull-out voltages.

The key parameter is the spring constant ($k$) defined as

$$k = \frac{16\,E W_{SCG}\,t_{SCG}^3}{L_{SCG}^3} \qquad (10)$$

where, $E$ is defined as the Young's modulus, $W_{SCG}$, $t_{SCG}$ and $L_{SCG}$ are the width, thickness and length of the suspended control gate, respectively. As the pull-in equation has been obtained elsewhere (Eq. (8)), it will be modified according to the double-plate capacitor model. The pull-in equation is defined as

$$V_{pull-in} = 8\sqrt{\frac{2\,E t_{SCG}^3\,t_{air-gap}^3}{27\,\epsilon_0\,L_{SCG}^4}} \qquad (11)$$

where $\epsilon_0$ is the space permittivity, $t_{air-gap}$ is the air-gap separation. In the other hand, the pull-out effect is to be calculated. The pull-out effect considers that both plates are initially in contact. Both the electrostatic and electromechanical forces are driven by the applied voltage. By reducing the applied voltage, the double-clamped beam stiffness increases its presence. A further reduction allows to overcome the electrostatic force and is in here that the top plate detaches from the bottom returning to the initial isolated position. **Figure 10** shows the schematic diagram analysed to calculate the pull-out voltage.

The characteristics needed to obtain the pull-out effect considers, as the initial condition, that both plates are in contact as the initial spring constant. Due to the force that act is a combination of electrostatic, Casimir and van der Waals forces, the pull-out voltage is mathematically defined as

$$V_{pull-out} = \sqrt{\frac{2\,k t_{ox}^2}{\epsilon_0\,\kappa_{ox} A}(t_{SCG} - t_{ox}) - \frac{A_h}{3\pi k_{ox}\,t_{ox}}} \qquad (12)$$
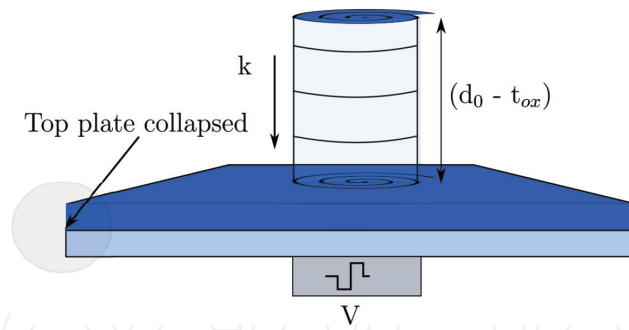
**Figure 10.** Schematic diagram of a two-plate capacitor that features the key parameters to analyse the pull-out voltage.
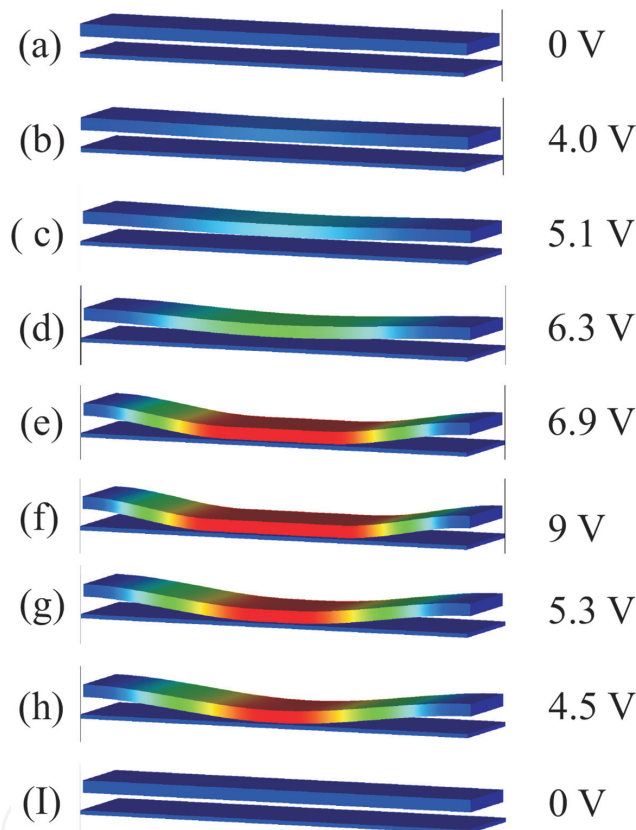


**Figure 11.** Set of images that describe the beam while bias (a) to (c) until it is being trapped by the pull-in voltage (d) and collapsed on the substrate (e). By increasing the applied voltage, contact area increases as well as the current density (f). By reducing the applied voltage, the contact area is reduced (g) & (h) until it reached the pull-out point and the beam return to its initial isolated position (i).

where, $\kappa_{ox}$ and $t_{ox}$ are defined as the dielectric constant, thickness of the dielectric material, respectively and $A_h$ is defined as the Hamaker constant. By considering the above mentioned equations for pull-in and pull-out voltages (Eqs. (11) and (12)), the voltage obtained can be used as a guide to find those voltages. Further analysis is strongly suggested by using commercial software such as Comsol or CoventorWare to corroborate the pull-in and pull-out voltages as shown in **Figure 11** [26, 27].
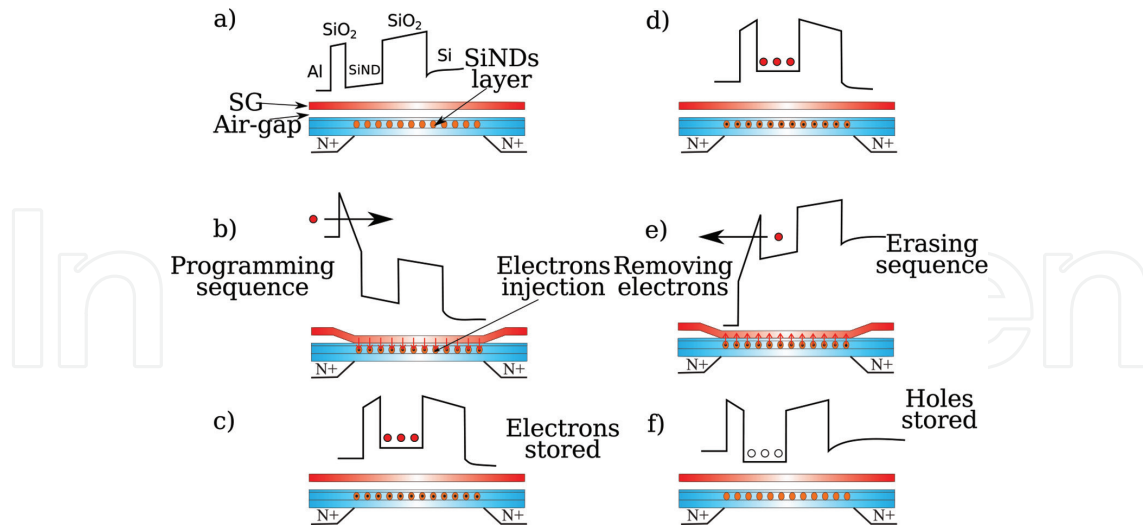
### 4.2.2. Programming and erasing processes

The programming and erasing processes occur due to a combination of the applied voltage to the control gate (pull-in effect) and the injection of electrons through the tunnel oxide layer. The injection of electrons to program and to erase the memory node are through the movement of the suspended control gate (top injection). In contrast, the typical memory devices that require the channel formation and the injection from the bottom, i.e., flash memory [28]. The tunnelling process starts once both layers are in contact (after the pull-in process occurs). **Figure 12** depicts a set of schematic diagrams for the programming and easing processes by using energy band plots.

Above figure (**Figure 12**) describes the tunnelling process that mathematically co-integrates in the transfer Matrix method, the Tsu-Esaki equations in a finite element method based in homemade algorithm. In this algorithm, the Poisson's equation and the Schrödinger equation are co-solved simultaneously to obtain the current density curve.

The model that is being considered to implement assumes that the energy and momentum are kept due to there is no energy dissipation process considered. Hence, the total energy can be divided into lateral and vertical components

$$E(\vec{k}) = \frac{\hbar^2 (k_x^2 + k_y^2)}{2\, m^*} + E_z \tag{13}$$

where, $m^*$ is defined as the effective mass of the electron, $\hbar$ is defined as the Planck constant and $\vec{k}$ represents the lateral wave vector. The Tsu-Esaki equation at finite temperature is defined as



**Figure 12.** A schematic diagram of the quantum-mechanical tunnelling process for the programming and erasing processes according to the band energy diagram. (a) Shows the energy band diagram for the SGSNM device. While applying a negative voltage the beam collapsed on the tunnel oxide layer and the electrons are injected due to the band diagram became triangular (b). By removing the voltage, the beam returns to its initial flat position and the electrons are trapped within the memory node (c). By applying a positive voltage the energy bands are bent in the opposite direction and the electrons are removed from the memory node and the removing the applied voltage, the memory node is empty as shown in (f).

$$J = J_{\rightarrow} - J_{\leftarrow} \tag{14}$$

$$J_{\rightarrow} = 2 \sum_{k_x, k_y, k_z > 0} ev_z \, T(E_z) \Big[ f_L(\vec{k}) \big[ 1 - f_R(\vec{k}) \big] \Big] \tag{15}$$

$$J_{\leftarrow} = 2 \sum_{k_x, k_y, k_z < 0} ev_z \, T(E_z) f_R(\vec{k}) \big[ 1 - f_L(\vec{k}) \big] \tag{16}$$

where, $T(E_z)$ is the transmission probability function, $f_L$ and $f_R$ are the Fermi distribution functions at barrier sides called emitter and collector regions.

$$f_{L,R}(\vec{k}) = \cfrac{1}{1 + \exp\left( \cfrac{E(\vec{k}) - E_F^{L,R}}{K_B T} \right)} \tag{17}$$

where.

$E_F^L = E_F^R + V$, $V$ is defined as an external voltage applied to the barrier Integrating over the regions perpendicular to $z$

$$J = \int_0^\infty dE_z \, T(E_z) S(E_z) \tag{18}$$

Tsu-Esaki equation and the transfer matrix method consider the Schrödinger equation as time independent and in one dimension (1D).

$$-\frac{\hbar^2}{2} \nabla \left( \frac{1}{m^*(z)} \nabla \right) \Psi(z) + V(Z) \Psi(z) = E_z \Psi(z) \tag{19}$$

where $m^*(z)$ is defined as the z-dependent conduction-band effective mass, $V(z)$ as the potential energy used and $\Psi(z)$ is defined as the wave function. The solution for the wave function has the form of

$$\Psi_{k_z^{(i)}}^{(i)}(z) = A_{k_z^{(i)}}^{(i)} \exp\left( ik_z^{(i)} z \right) + B_{k_z^{(i)}}^{(i)} \exp\left( -ik_z^{(i)} z \right) \tag{20}$$

As a result, we obtained a voltage-current density curve (V-J) for a particular substrate, in this case $SiO_2$. Figure shows a set of curves for a set of $SiO_2$ thicknesses.

### 4.2.3. Circuit simulation

Once the pull-in and pull-out voltages as well as the tunnelling process through the current density curve have been obtained, those can be implemented within a commercial simulation software such as Spice as external libraries. **Figure 13** shows the algorithm that is considered to be implemented for the correct behaviour of the non-volatile memory in particular for the memory node.

The set of libraries added to Spice are based on the models depicted in **Figure 14**. Curves are coded by using a state-of-the-art language such as Verilog-AMS [29].
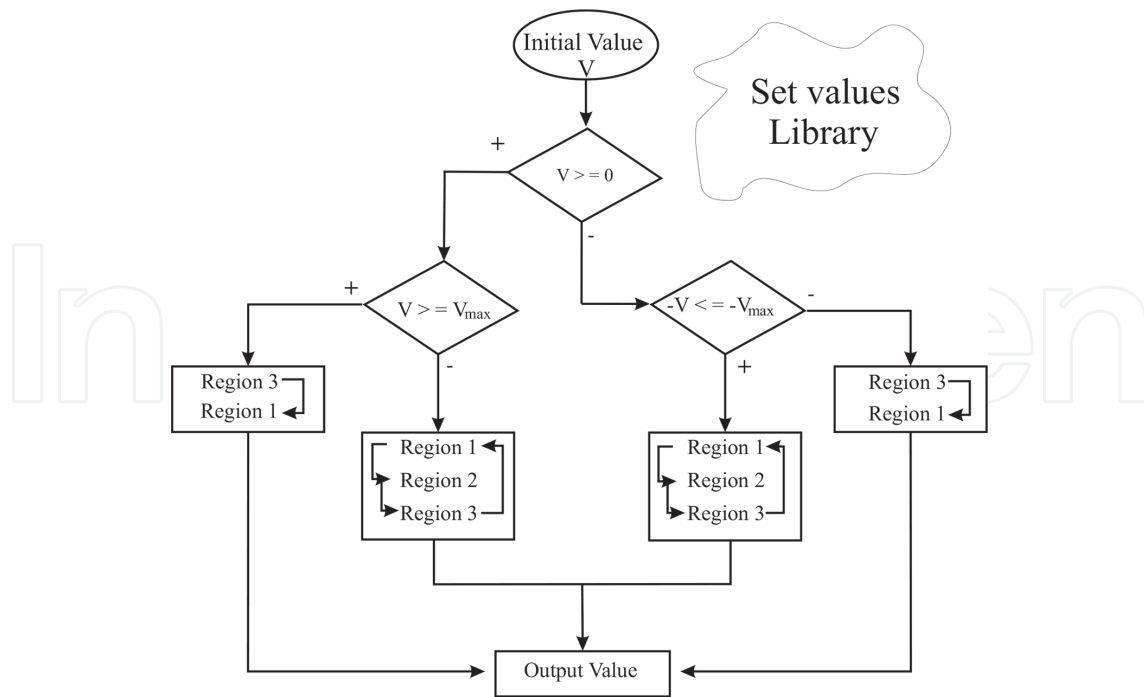
**Figure 13.** Schematic diagram of the libraries considered to be implemented within the circuit simulation.
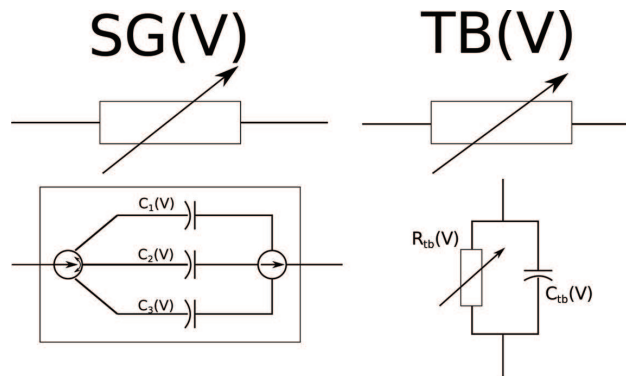


**Figure 14.** Schematic diagram of the libraries considered to be implemented within the circuit simulation.

Once both set of curves are implemented, the equivalent circuit considered is shown in **Figure 15**. Before analysing the cell, it is required to define the bias source for the suspended control gate as a piece-wise linear source (PWL) and for the MOS transistor a normal bias source.

By simulating the SG-MOS transistor cell, the set of curves obtained are displayed in **Figure 16**. The chart is divided in four arrows in which the PWL source, bias source, memory node and the readout element to identify the node state. The PWL source follows a cycle of four sections. The cycle starts with a negative voltage applied to the control gate, in the memory node it is possible to observe how the electrons are being injected from the control gate towards the thin tunnel oxide layer into the memory node. While the PWL source shows zero volts, the memory node displays a negative charge level. By biasing the MOS transistor, it shows a current level in the order of $10^{-12}$ A indicating that the memory has been programmed. On the
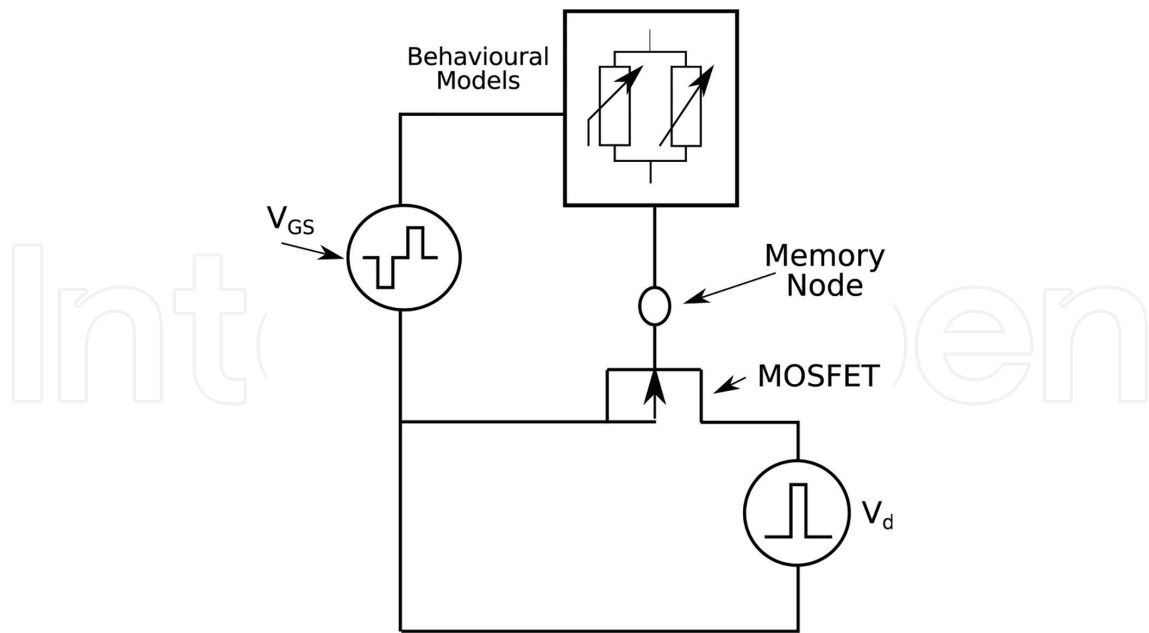
**Figure 15.** Equivalent model for the memory cell to be implemented within the commercial circuit simulator.

other hand, by applying a positive voltage on the suspended control gate, the memory node shows how the electrons are being retrieved by the gate. When the PWL source returns to zero V and the readout element is biased, in the memory node it is possible to observe a positive charge level and the current shown by the transistor is 6 magnitude order larger than when programmed. A key element that can be observed is the programming/erasing time of 1.7 ns for the characteristic of the nanostructure. Nowadays, the times for flash memory is at least over 3 magnitude order lower than the hybrid structure.

Now that the simulation shows the results for the programming and erasing times, the next step is to fabricate the suspended control gate as well as the MOS transistor.

*4.2.4. Fabrication process*

The fabrication process for the SGSNM cell, start by considering a substrate based on Si, on top of it, a high quality and thin $SiO_2$ layer is grown. As the memory node, a monolayer made of silicon nanodots is deposited even sparsely. Each silicon nanodots is isolated between them due to are immersed in a $SiO_2$ layer. As sacrificial layer, a thick polysilicon layer is used. Finally, as the suspended control gate, an Aluminium layer is deposited. Patterns are performed by using standard photoresist due to the size of the beam being used. To get the shape of the beams, a standard Al wet etchant is considered at 300 K. To release the doubly-clamped beam, a single-step dry etching process is performed. As a result, the control gate is suspended and the device is up to measure. **Figure 17** shows the process above described.

**4.3. High-Q resonators**

High-Q resonators are one of the main nanodevices to be investigated due to the wide variety of applications that can be used when implemented it. A double-clamped beam as a classical
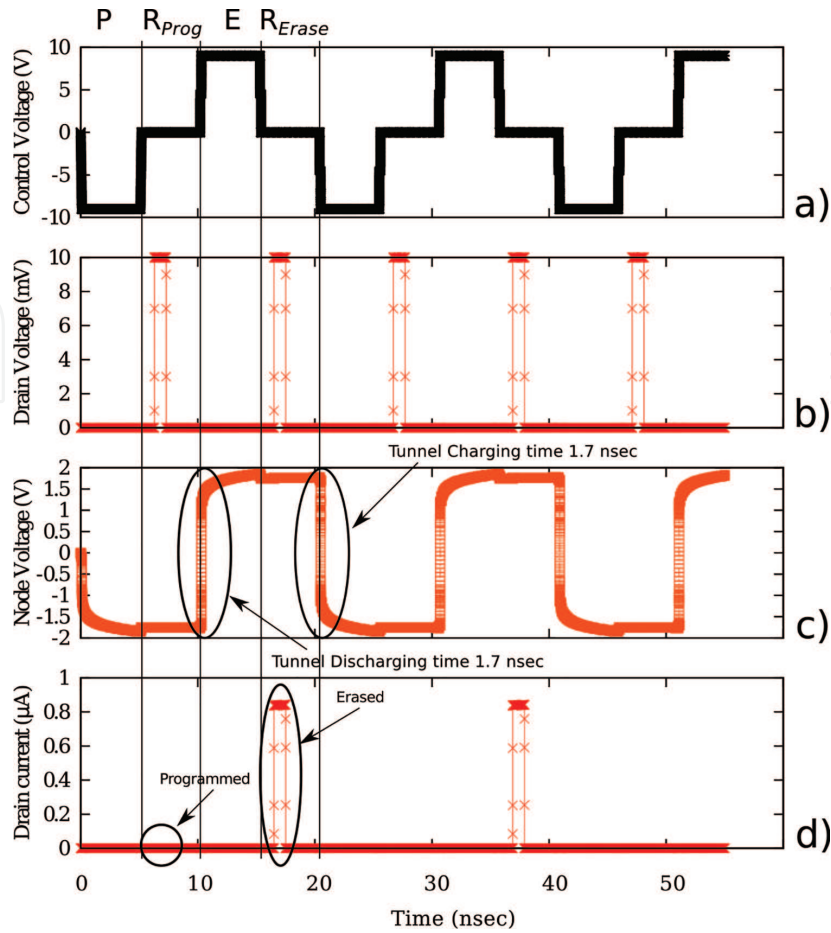
**Figure 16.** Set of curves obtained from simulating the SGSNM. The first curve defines the piece-wise-linear source that drives the memory operation. While performing a negative voltage, it is possible to see how the electrons are injected in to the memory node. When the PWL source shows zero volts and the readout element is biased, a current peak is observed indicating that the memory node had been programmed. In contrast, when a positive voltage is applied, at the memory node the electrons are retrieved towards the control gate and when the PWL source is zero, the readout element shows a current peak 6 magnitude order larger than when programmed indicating that the memory has been erased.
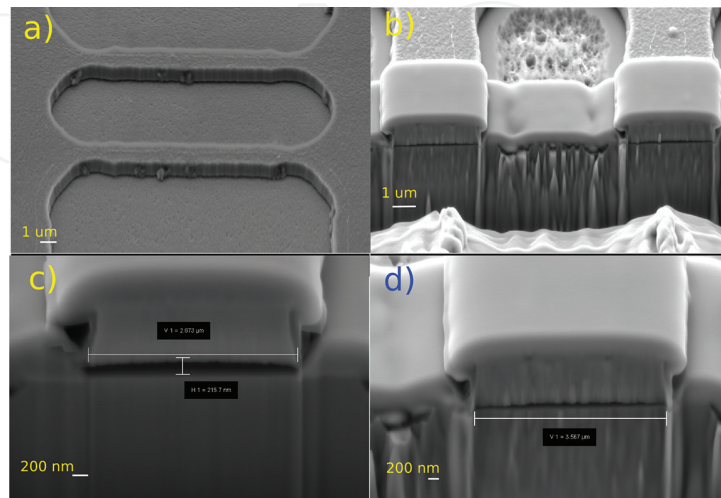


**Figure 17.** Set of SEM images that shows the doubly-clamped beam suspended. a) Shows the wet etching process result for the Al layer. b) Shows the result for the dry-etching process recipe that displays the beams successfully suspended. c) and d) show a zoom for each beam.

capacitive can be modelled with high accuracy by including non-linear terms. These key characteristics can be strongly related to a spring in which the stiffness can vary according to the electric field applied [30]. The non-linear restoring force $F_k$ can be expressed as:

$$F_k(y) = ky + k_1 y^2 + k_2 y^3 + \cdots O(y^n) \tag{21}$$

The Duffing equation for damping factor is expressed as

$$\frac{d^2 y}{dt^2} + \frac{\gamma}{m}\frac{dy}{dt} + \frac{k}{m} + \alpha y^2 + \beta y^3 = \frac{F_\omega}{m}\cos\omega t \tag{22}$$

where $\alpha = k_1/m$ and $\beta = k_2/m$. A different non-linear models does not consider the second order term due to this term have no impact on the resonant behaviour.

### 4.3.1. Quality factor

Quality factor is a reference for MEMS/NEMS resonators. It describes the ratio between the energy stored and dissipated defined as:

$$Q_{res} = 2\pi\frac{W_n}{\Delta W} \tag{23}$$

where $W_n$ is the stored energy and $\Delta W$ is the energy dissipated each cycle. A fundamental relationship among them can allow to improve for a high quality factor. The maximum energy that can be stored in an electromechanical resonator strongly depends on the vibration mode, the mass of the resonator and the displacement [13].

$$W_n = \frac{\rho}{8} V_r es\, \omega_n^2 x_{nc}^2 \tag{24}$$

According to the material stiffness is related to the quality factor that can be achieved such as poly-diamond that shows a very high Young's modulus. As a matter of fact, the material density modifies the total energy amount that the resonator can drive. Massive resonators that consider extensional or bulk mode resonance present a very high Q-factor.

## 5. Applications

Hybrid structures have a broad variety of applications being bio-applications key in the development of health services worldwide. In here, we present how the hybrid structures can be applied as bio-sensors.

### 5.1. Biological applications

The use of nanoelectromechanical systems (NEMS) has had a remarkable impact on different biological areas such as medical, food industry including food safety and analytical. The principle to NEMS development is based on the search for systems that serve as micro-reservoirs,

micropumps, valves, sensors and other structures that use biocompatible materials appropriate for chemical or biological molecules release or for their detection. The development of intelligent biomaterials as responsive hydrogels and configurationally imprinted biomimetic polymers (CIBPs) are the preferred materials for biological applications due to high adaptability and compatibility with biological molecules and cells [31]. The use of configurationally CIBPs allows the improvement of molecular recognition systems through the control of chemical functionality and the tridimensional structures.

The constructional designs of devices that operate in an intelligent way, with high sensibility to diverse analytes are capable to control the release of therapeutic or antimicrobial molecules in response to a key biological event allowing it to be used in diverse applications [32]. Medical treatments have innovated in response to the wide variety of pathophysiological conditions that require the development of more effective therapeutic agents and the use of device-integrated biomaterials that can serve as sensors and carriers. NEMS-based devices offer opportunities to address a significant number of unmet medical needs related to dosing, diagnostic and tissue engineering.

Some of the advantages of leading NEMS-based drug delivery in implant/stent have a potential impact if treatment requires local dosing, avoiding the need for injection. In the area of implant/pumps devices, those have the potential to lower total dose due to local administration, avoids the need for injection, permitting a local and systemic parenteral administration. To implant an electronic chip, it could be observed potential to lower total dose due to local administration, the capability of establishing precise timing and control, avoids the need for injection, flexibility of local or systemic parenteral administration depending on the formulation. Finally, the implant/polymer chips show potential to lower total dose due to local administration and avoid the need for injection [33].

In diagnostic applications, the ability to monitor the health status, diseases onset and diseases progression is highly desirable. To develop devices for these applications, it is necessary to know the specific biomarker associated with a health or a disease state. To count with a non-invasive approach to detect and monitor this biomarker and technological capability to discriminate between and among the biomarkers. The development of simple-to-use NEMS-based biosensors could have applications in the identification of major diseases and/or pathogens, rapid diagnosis of exposure and disease and detection of emerging pathogens which could be in parallel for multiple infectious agents, accurate assessment of disease stage and prognosis and a better management of outbreaks and emerging acute and chronic health threats [34]. In the same way, the food industry has developed research focused on food packaging and food safety through the use of NEMS-based biosensors. Nanosensors permit the detection of food-borne contaminants, detection of pathogens and capability to detect and quantify volatile or non-volatile compounds related to quality or natural physiological process [35].

Food contact materials used to monitor the condition of packaged food or the environment surrounding the food have used in both, polymer nanomaterials for food packaging (PNFP) and MEMS/NEMS-based biosensors to create "Intelligent/smart food package". This technology can inform with a visible indicator or other novel systems, the supplier or consumer that foodstuffs are still fresh, or whether the packaging has been breached, kept at the appropriate temperatures

throughout the supply chain, or has spoiled [36]. Fresh produce or meats during their maturation or spoilage exhibit odours, colours or other sensory characteristics which can be easily discerned by consumers. However, to determine that the product should be good for the determined period, consumers use information that the producers set, based on a set of idealised assumptions about the way that the food is stored or transported. Some of these assumptions are not real if it is considered that this date may no longer be applicable if this food product was stored above its optimal temperature for an hour, either in a delivery truck or a warm automobile.

Most of the development of these intelligent food packages, look for alternatives to detect small organic molecules that are the result of microbial activities or adulterants, specific gasses, and/or viable foodborne pathogens [31]. The benefits of intelligent packages are related with speed and accuracy with which industries or regulatory agencies can detect the presence of molecular contaminants or adulterants in complex food matrices [31].

Nanoelectromechanical systems used as sensors have a significant impact in the analytical field. Biosensing is a complex task that involves knowledge about the biochemical process in addition to diverse problems related to the nature of the operation medium. Some of the most popular applications for NEMS sensors in analytical chemistry permit the detection of formaldehyde vapour, water-toluene vapour, organics and inorganics, alcohols, $H_2$, organophosphorous vapour and others (in gas-phase sensing applications). In liquid-phase applications it is possible to analyse acetic acid, aminoethanethiol, retinoid isomers, metal ions and fructose among others. Finally, in biosensing applications it is possible to detect myoglobin, antibody-concentration, liposomes, thiolated single-stranded DNA (ssDNA), thiol modified single-stranded DNA (ssDNA) or the presence of pathogens or their toxins (airborne anthracis spores, Staphylococcus enterotoxin B (SEB), Salmonella typhimurium, airborne virus particles, *Escherichia coli* $O^{157}:H^7$ and others) [37].

A potential high number of applications in the biosensing or dosing could be proposed by different devices between them hybrids type NEMS-MOS.

## 6. Conclusions

As the Semiconductor industry has reached an impasse due to the scaling-down process according to Moore's Law for the Metal-Oxide-Technology in use. Alternative technologies are foreseen to allow the development of nanodevices with a broad variety of characteristics such as high switching speed, low power consumption, robust, among others that can overcome the inherent issues for Silicon. A few "exotic materials" appear as good candidates such as Graphene, $MoS_2$, BN-h, etc. However, the time for the novel technology to be mature will take time. To allow the "exotic materials" to mature, the semiconductor industry needs novel nanostructures capable to overcome a few of the issues that silicon-based technology is facing. As clearly shown, the hybrid nano-structures allow to develop a broad variety of nanodevices such as transistors, memories and sensors. As stated in the chapter, it is demonstrated that hybrid-structures are allowing the emerging technology to become mature to diversify as well as to be reliable as silicon-based technology is.

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