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Preparation and Device Applications of Ferroelectric β-PVDF Films

Liuxia Ruan, Donghai Zhang, Junwei Tong,
Jianli Kang, Yufang Chang, Lianqun Zhou,
Gaowu Qin and Xianmin Zhang

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Abstract

Organic ferroelectric materials have unique characters comparing to their inorganic counterparts in electronics because they show the advantages such as low cost, lightweight, small thermal budget, flexible and nontoxic characteristics. The ferroelectric poly(vinylidene fluoride) (PVDF) is mostly desired for memory devices due to its polar phase. To obtain the ferroelectric memory devices for data storage, ultrathin PVDF films are required to allow for low operation voltages with both small roughness and free of pin-holes. Micronmeter thick films of ferroelectric phase PVDF can be easily achieved by many preparation methods. But the nanofilms could be mainly fabricated by coating method and Langmuir–Blodgett deposition technique. Meanwhile, according to the structure of devices, four types of organic memory cells using ferroelectric phase PVDF films were introduced, such as memory based on metal/organic semiconductor/metal ferroelectric tunnel junctions, organic capacitors, field effect transistor and organic diodes. The research has been mainly done in Zhang's laboratory from September 2016 to explore the preparation and potential applications of ferroelectric PVDF films. In this chapter, we summarize several device investigations and show the PVDF films have the promising memory applications.

Keywords: PVDF films, memory devices, spin coating, Langmuir–Blodgett method, ferroelectric tunnel junctions, organic capacitors, field effect transistor, organic diodes

1. Introduction

Poly(vinylidene fluoride) (PVDF) exists five crystalline structures, α, ε, β, δ, and γ phases. Both α and ε phases are nonpolarized. The polar β, δ, and γ phases are very interesting in

various applications [1, 2]. In particular, the β-phase PVDF (expressed in TTTT conformation) is mostly desired for ferroelectric memories in the data storage fields. The dipole moments in the molecule stem from the strongly electronegative fluorine atoms predominantly, inducing the ferroelectricity of β-phase PVDF [3, 4].

A number of methods have been proposed to prepare the PVDF films with the thickness up to several microns such as electric poling, hygroscopic salts, mechanical stretching, epitaxy with KBr, and solvent evaporation [5–7]. In contrast, the spin coating and Langmuir–Blodgett deposition techniques are two main methods to obtain the ferroelectric β-phase PVDF films with the thickness down to 300 nm or more less [8, 9]. Furthermore, spin coating can be used to fabricate the large area uniform films from the industrial point of view [10]. Langmuir–Blodgett (LB) deposition technique can prepare the ultra-thin PVDF films with the thickness of several nanometers [11]. In this chapter, we firstly report the main results about the fabrications of β-phase PVDF films by spin coating method and Langmuir–Blodgett deposition techniques. Then, the typical applications of β-phase PVDF films in several organic devices are introduced.

2. Preparation

Microelectronic devices using β-phase PVDF film generally require nanoscale thickness and pin hole-free to avoid the electrical shorts [12]. Many works have been done to discuss the preparation and application of PVDF thin films. The purpose of these studies is preparation of smooth thin films or achieving a ferroelectric phase (β, δ, or γ phase) [13–15].

The high coercive field is one drawback for PVDF and its copolymers used in the devices, which determines the minimum electric field that needed to reverse the polarization state. With the coercive fields of 50 MV/m and higher [16], the thickness of β-phase PVDF films must be less than 100 nm to allow for low operation voltage. The early devices based on β phase PVDF [17], required an operation voltage up to 200 V, while the more recent reports still need 30 V or more to operate [18–20]. The ultrathin films of P(VDF-TrFE) obtained by Langmuir–Blodgett deposition on silicon wafers has produced one nanometer ferroelectric films [21] and operation voltage less than 10 V for nonvolatile memory devices [22]. The β-phase PVDF nanofilms are mainly prepared by spin coating and LB deposition.
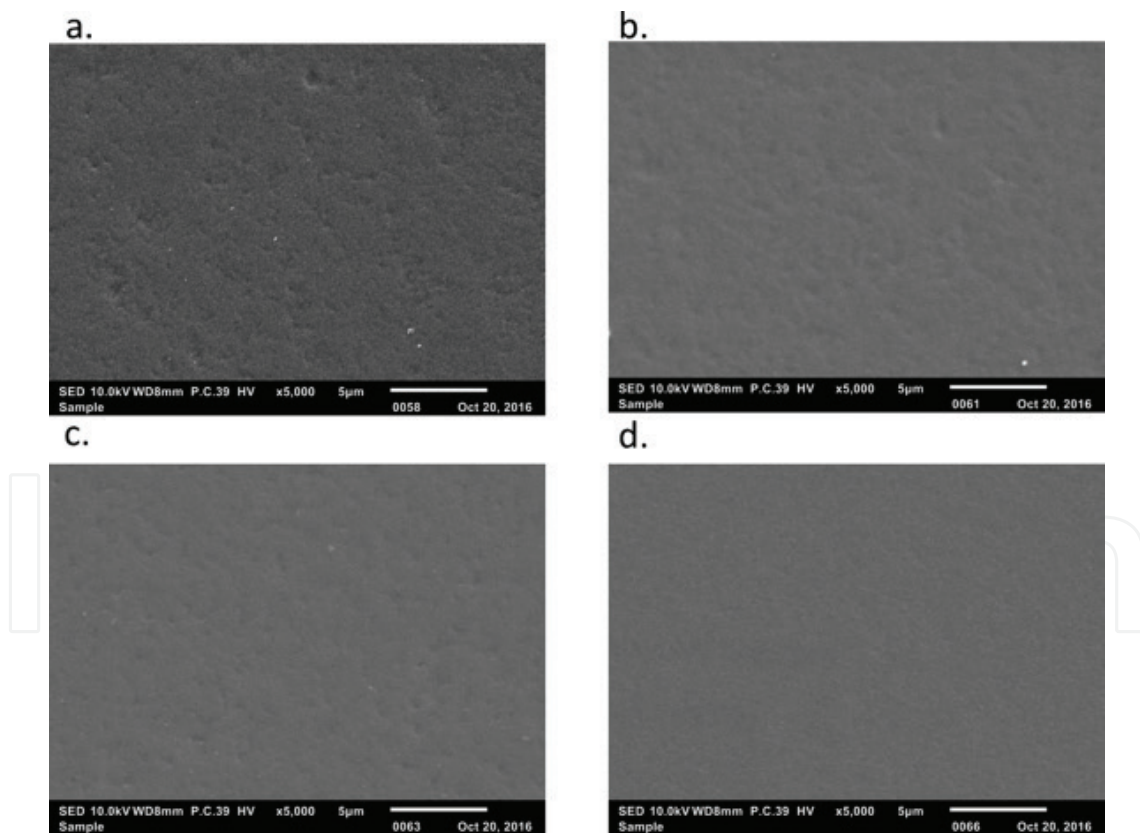
2.1. Spin coating

Spin coating is a desirable method to achieve the large area uniform nanofilms. However, the surface of traditional spin coating PVDF film is too rough for the application in microelectronics. The acquisition homogeneous and smooth PVDF nanofilms with small roughness is a major breakthrough for spin coating and electron device [10, 23, 24]. Smooth PVDF films have been obtained by humidity-controlled spin coating, dimethyl formamide (DMF), N-methylpyrrolidone (NMP), dimethyl sulfoxide (DMSO), or dimethylacetamide (DMAc)

used as polar solvents to dissolve PVDF [10, 12, 23]. The micrographs were obtained using the JEOL JSM-IT100 of thin films SEM were under different relative humidity by spin coating were evaluated, as shown in **Figure 1** [25].

The percentage of β-phase PVDF (β%) in films fabricated by spin coating method is mainly studied by Fourier transform infrared (FTIR) (BRUKER) spectroscopy and X-ray diffraction (XRD) (RIGAKU) techniques. It is found that the processing conditions such as solution concentration, spin rotation speed (rpm) and annealing temperature obviously affect the percentage of β-phase PVDF [26]. The value of β% was calculated and the different percentages for the corresponding films at different annealing temperatures were plotted in **Figure 2**.

Meanwhile, Cardoso et al. successfully prepare thin PVDF films with high β-phase content by thermally annealing at 70°C [27]. A 160 nm thick PVDF film mainly consists of the ferroelectric β phase was prepared by rapid thermal annealing and humidity controlled spin coating method [10]. Ramasundaram et al. reported the fabrication of PVDF films dominantly with β phase using a heat-controlled setup of spin coating [9].

Figure 1. Scanning electron microscopy (SEM) micrographs of PVDF films prepared by spin coating with the relative humidity at (a) 20%, (b) 40%, (c) 60%, and (d) 80% [25]. This research was conducted at Center of High Technology Materials New Mexico in 2017.
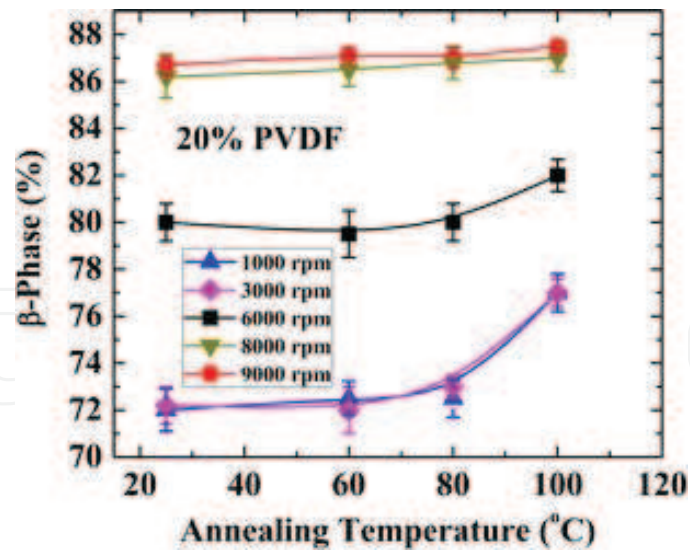
Figure 2. β-phase dependence of 20% PVDF films on annealing temperatures [26]. This research was conducted at Center of High Technology Materials New Mexico in 2017.
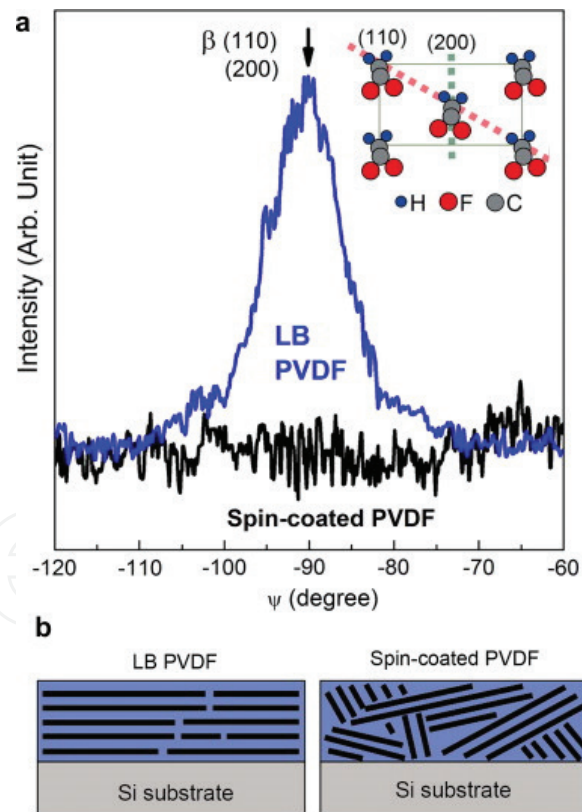

Figure 3. (a) The ψ dependence of the XRD peak β (110) (200) of the PVDF LB film and a spin-coated PVDF film. (b) Cross-sectional view to compare the molecular chain orientation of the LB PVDF film and spin-coated PVDF film. The black bars are used to denote the PVDF molecular chains [8]. This research was conducted at Agency for Science, Technology and Research of Singapore in 2012.

2.2. Langmuir-Blodgett method

As an effective technique, LB deposition was usually used to fabricate nanoscale films, in which the interaction of water with PVDF molecules is involved [8, 28]. This could deposit PVDF films at room temperature on any substrate material because the films were grown layer-by-layer [29].

The orientation of dipoles of the PVDF LB film was analyzed by the XRD peak intensity (β (200) (110)) compared with a spin-coated PVDF film using an XRD system (D8-ADVANCE, Bruker AXS GmbH, Karlsruhe, Germany) as shown in **Figure 3a**. It was found that LB deposition process can directly format β crystalline phase of PVDF, with the molecular chains parallel and the dipoles aligned perpendicular to the substrate. The results of ψ-scan XRD indicated that the molecular chains in the LB films were parallel with the substrates, but chains in the spin-coated film are randomly oriented, as schematically illustrated in **Figure 3b** [8].

Zhu et al. reported that the 5–35 layers PVDF nanofilms could be prepared by the LB method at 20°C [30]. The dependence of root-mean square (RMS) surface roughness on the thickness of PVDF nanofilms is shown in **Figure 4**. The high surface roughness of 35 and 81 nm thick films is expected to be related to a sudden decrease of polarization. A Pr of 6.6 μC cm^{-2} was acquired for 81 nm thick PVDF homopolymer film with no post-treatment. They also firstly achieved the ferroelectricity in a 12 nm thick PVDF film, indicating a potential low-voltage application of PVDF nanofilms [11]. The thickness of each PVDF layer could be thin as 2 nm. Therefore, an ultra-thin PVDF film can be expected through layer-by-layer growth using LB method. Recently, the β-phase PVDF films was reported with the thickness around five nanometers [31].
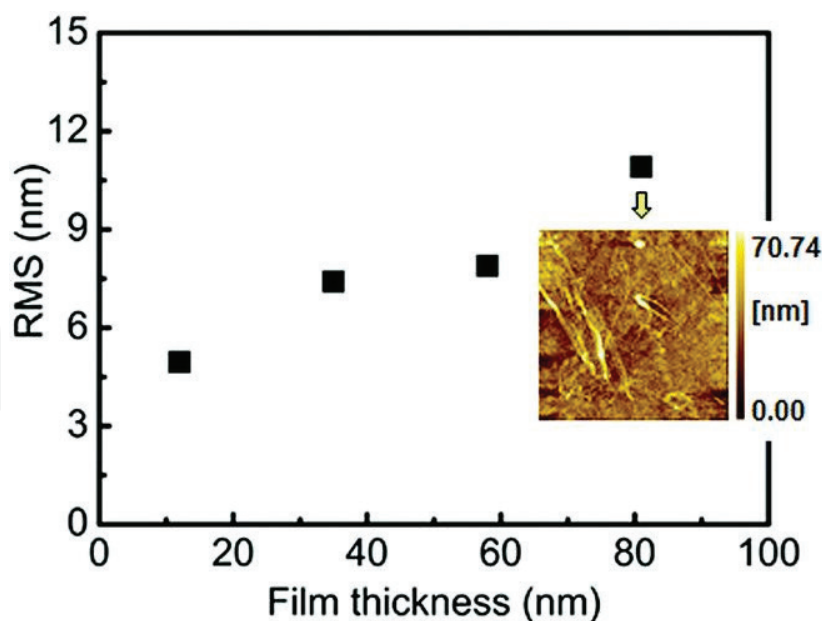
Figure 4. The dependence of root-mean square (RMS) surface roughness on different thickness of PVDF LB nanofilms. The inset is an atomic force micropy image of PVDF film at 81 nm thickness [11]. This research was conducted at Tohoku University of Japan in 2014.

3. Application in organic memory devices

In modern society, more and more electronic products are studied in both inorganic and organic electronics. Organic memory cells develop at a slow pace, but researches of organic memory devices based on PVDF and its copolymers will become extremely important to develop the future organic electronic products. In the case of copolymers including poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)), the addition of one more fluorine atom provides the delicate configuration balance and always results in the polar ferroelectric β structure [32]. However, PVDF possesses higher ferroelectric transition temperature and thermal stability of remnant polarization in comparison with its copolymers [33, 34]. PVDF has a high Curie temperature of 167°C compared to the P(VDF-TrFE) copolymers with Curie temperatures from 60 to 100°C related with the TrFE content [10]. The higher Curie temperature of PVDF as a ferroelectric layer potentially allows the higher temperature operation of polymer memory than that of its copolymers. In addition, the copolymers are unlikely suitable for mass production because their synthesis is extremely complicated and thus ineffective cost [35].

In the following report, four types of PVDF memory cells will be introduced according to the structure of memory devices. They are ferroelectric tunnel junctions, organic capacitors, field effect transistor and organic diodes [36, 37].

3.1. Ferroelectric tunnel junctions

The idea of ferroelectric tunnel junctions (FTJs) was derived from the observation of spin-dependent tunneling phenomenon. FTJ is a device with two ferromagnetic metal layers separated by insulating barrier [38]. Perovskite-type ABO_3 metal oxides (e.g., $BaTiO_3$ or $KNbO_3$) are widely known as ferroelectric materials for their excellent piezoelectric response and strong polarization [39, 40]. However, their applications are limited by brittleness, heavy weight, high cost, and large thermal budget [41]. The electric polarization of ferroelectric PVDF is comparable to that of perovskite oxides. The use of organic ferroelectrics PVDF could solve the problem of thermal budget because PVDF can be processed at 200°C or lower temperature [19]. Furthermore, PVDF films are very appealing due to their flexible, light weight, low cost, and nontoxic characteristics [41–43]. PVDF thin films are very promising and used as barriers in FTJs for these properties [44]. Ferroelectric tunnel barriers allow switching of the tunneling conductance between two stable states because their spontaneous polarization can be reversed under a bias voltage. This phenomenon is known as tunneling electro resistance (TER). In the past years, extensive studies in theory have confirmed the possibility to fabricate PVDF FTJs [45–55]. By contrast, the progress in experimental investigations is not so good owing to the challenges in the fabrication of PVDF ultra-thin films with high purity of ferroelectric active phase.

On the basis of first principles calculations, simultaneous TER and TMR effects and multiple resistance states were demonstrated [51, 56, 57]. The TMR is defined as:

$$TMR = \frac{G_P - G_{AP}}{G_P + G_{AP}} \times 100\%$$

(1)

where $G_P = G_{\uparrow\uparrow} + G_{\downarrow\downarrow}$ and $G_{AP} = G_{\uparrow\downarrow} + G_{\downarrow\uparrow}$ are the junction conductance, when the magnetizations of two electrodes are parallel and antiparallel, respectively.

The TER is defined as:

$$\text{TER} = \frac{G_{\leftarrow} - G_{\rightarrow}}{G_{\leftarrow} + G_{\rightarrow}} \times 100\% \qquad (2)$$

where $G_{\leftarrow}$ is the conductance for the PVDF polarization pointing to the left, and $G_{\rightarrow}$ the conductance for the PVDF polarization pointing to the right, and horizontal arrows indicate the polarization direction. The conductance of the Co/PVDF/O/Co(0001) MFTJ was calculated by Velev et al. using the first principles electronic structure [51]. The results are shown in **Table 1**, where also the conductance of Co/PVDF/Co MFTJ with clean interfaces is given for comparison.
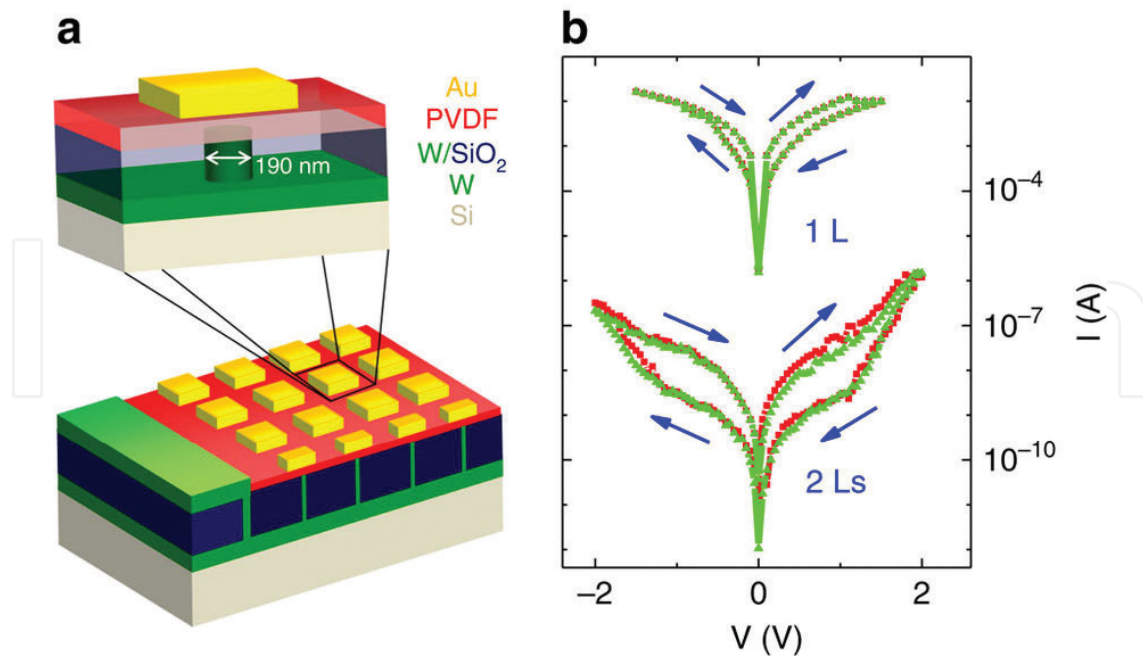
3.1.1. Au/PVDF/W tunnel junctions

Tian et al. report a robust room temperature TER of ~300% and ~1000% in organic FTJs using ultrathin PVDF films (1 and 2 layers (Ls) with the thickness of 2.2 and 4.4 nm, respectively) [58]. Three-dimensional sketch of the PVDF FTJs is shown in **Figure 5a**, and the junction sizes are defined by the bottom electrode isolated by a SiO$_2$ matrix. The deposition of PVDF ultra-thin films were performed prior to the deposition of micron-size Au as top electrodes. The typical I–V characteristics of the PVDF FTJs are shown in **Figure 5b**. A Keithley 6430 sub-femtoampere source meter with a remote preamplifier was used to perform the I–V measurements [58].

	G (10^{-7} e^2/h)			TMR (%)
	$\uparrow\uparrow$	$\downarrow\downarrow$	$\uparrow\downarrow + \downarrow\uparrow$	
Co/PVDF/Co				
←(→)	104.59	235.56	471.23	−16.3
Co/PVDF/O(hcp)/Co				
←	4.40	2.54	7.64	−4.6
→	2.74	2.11	10.04	−34.8
TER (%)		17.7	−13.7	
Co/PVDF/O(fcc)/Co				
←	4.42	8.70	11.1	8.7
→	2.43	6.21	12.33	−17.0
TER (%)		20.0	−5.6	

Table 1. Conductance per unit cell area, TER, and TMR for Co/PVDF/O/Co tunneling junction. $\uparrow\uparrow$ and $\downarrow\downarrow$ are used to represent the conductance for parallel magnetization of the electrodes. $\uparrow\downarrow + \downarrow\uparrow$ is the total conductance for the antiparallel magnetization. ← and → are the left and right polarization orientation of PVDF, respectively [51]. This research was conducted at University of Puerto Rico of USA in 2012.

Figure 5. TER in submicron Au/PVDF/W tunnel junctions. (a) Three-dimensional sketch of PVDF FTJs. (b) I–V curves in the 1 L and 2Ls PVDF FTJs. The arrows show the direction of the voltage sweeps [58]. This research was conducted at Chinese Academy of Sciences in 2016.

The transport mechanisms and electro resistive effects in the FTJs with a 5 nm thick barrier can be divided into Fowler-Nordheim tunneling, direct tunneling, and thermionic injection currents [59]. The larger TER response for thicker barriers agrees with electrostatics models based on a direct tunneling process [60, 61]. The devices show a room temperature TER effect as high as 1000%, which will open a new route for low cost, silicon-compatible, or potentially rollable organic devices.

3.1.2. $La_{0.6}Sr_{0.4}MnO_3$/PVDF/Co structures

The observation of a large 300% TMR in $La_{0.7}Sr_{0.3}MnO_3$/Alq$_3$/Co tunnel junctions is a particularly interesting result, where the interfaces of ferromagnetic metal/organic hybrid play a key role for spin injection in spintronics [62]. Liang et al. fabricated $La_{0.6}Sr_{0.4}MnO_3$(LSMO)/PVDF/Co FTJ organic structures with PVDF as a tunneling barrier to study the ferroelectric control of the spin-polarization of the spacer interfaces [57]. **Figure 6a** shows the device structure. The surface morphology of PVDF barrier investigated by AFM (Asylum Research, MFP-3D, USA) in **Figure 6b** reveals a smooth surface with 3.12 nm RMS roughness in the range of 1×1 µm². Amplitude hysteresis loops and representative local piezoresponse force microscopy (PFM) phase are shown in **Figure 6c**. **Figure 6d** shows the PFM phase image recorded on the PVDF surface.

It has been demonstrated that tuning the ferroelectric polarization of PVDF can control the spin-polarization of the PVDF/Co spinterface actively at low temperatures. Two polarization states are possibly related to either F-C-H/Co or H-C-F/Co interface (see the inset of **Figure 6e**). **Figure 6e** shows the magneto-response of the LSMO/PVDF/Co device for two different
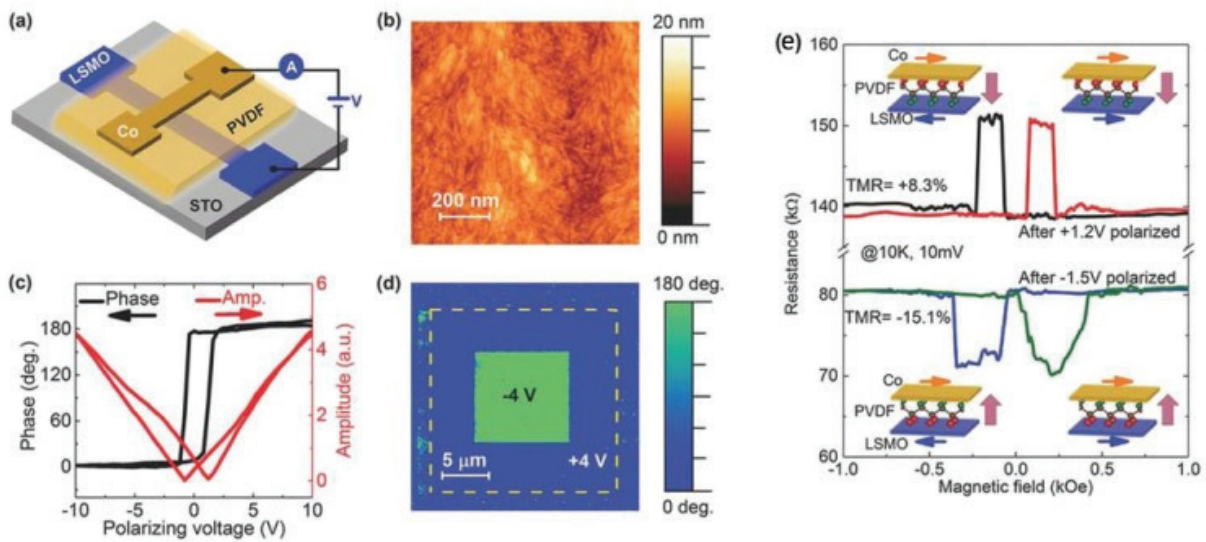
Figure 6. Morphology and characterization of LSMO/PVDF/Co. (a) Schematics of the LSMO/PVDF/Co device. (b) AFM topography of the PVDF barrier surface. (c) Amplitude hysteresis loops and representative local PFM phase measured on the PVDF surface. (d) PFM phase image recorded on the PVDF surface. (e) Tunneling magneto-resistance of the device measured after +1.2 V and − 1.5 V polarized. The insert graphs denote four different resistance states associated with the orientations of magnetization and polarization [57]. This research was conducted at CNRS-Université de Lorraine of France in 2016.

ferroelectric polarizations under 10 mV at 10 K. The positive TMR will vanish with increasing temperature up to 120 K. The negative TMR effect can survive over 250 K.

Ferroelectric PVDF was also introduced to control the magneto transport and the spin transport through the spinterface of ferromagnet/organic is studied. A LSMO/PVDF/MgO (0.5 nm)/Co device shows a much higher junction resistance in comparison with the devices without MgO layer indicating the insertion of MgO likely suppresses the diffusion of Co top layer. There is no coupling for PVDF/Co spinterface with MgO insertion layer, and the MgO/Co interface totally modifies the spin polarization [57]. The TMR sign with the MgO insertion layer is consistent with the reports of Co/MgO/Co magnetic tunnel junctions [63].

3.1.3. Fe_3O_4/AlO/PVDF/Co/Al stacking structure

Fe_3O_4 is one potential electrode because of its high spin polarization efficiency (100%) and high Curie temperature (~850 K) in theory [64, 65]. The PVDF spin devices with Fe_3O_4/AlO/PVDF/Co/Al stacking structure shown in **Figure 7a** was successfully fabricated very recently [31]. The magnetoresistance (MR) ratio at room temperature can achieve approximately 2.6% for the FTJs with 3-layer PVDF barrier (~7 nm thick). In **Figure 7b**, it is noted that the MR ratios increase with reducing measurement temperature. This is attributed to the reduction in spin scattering. The standard four-probe method is used to measure MR curves. The I–V curves were measured by A nanovoltmeter (model 2182A, Keithley Inst. Inc.) and an AC and DC current source (model 6221, Keithley Inst. Inc.). In addition, the MR response decreases with increasing PVDF layer numbers likely owing to the change of spin transport mechanism
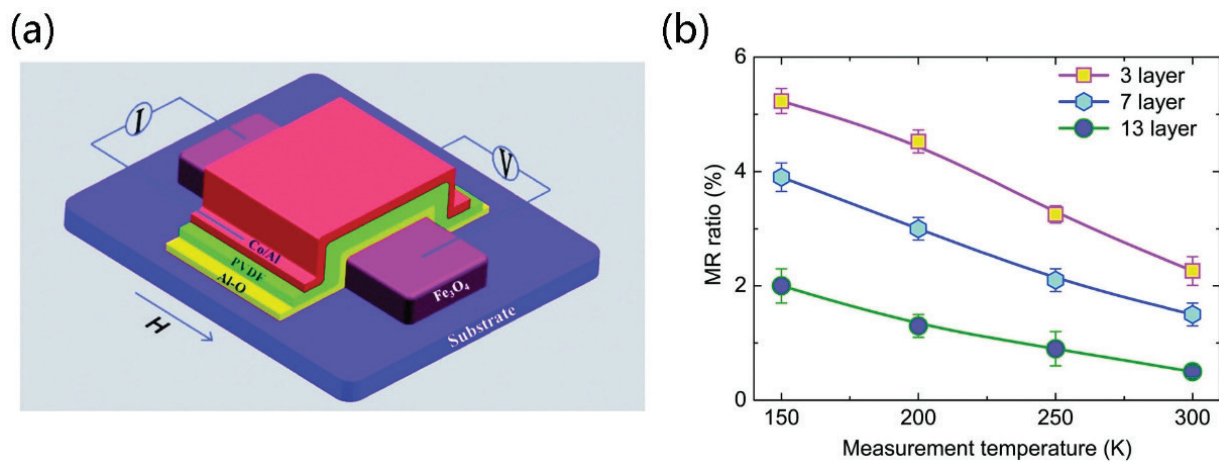
Figure 7. (a) Diagrammatic sketch of the Fe_3O_4/AlO/PVDF/Co/Al FTJs structure. The magnetic field along the long direction of the Fe_3O_4 strip was applied to measurement the magnetoresistance. (b) Magnetoresistance ratio dependence on different measurement temperature and various layer PVDF for spin valves [31]. This research was conducted at Northeastern University of China in 2017.

from tunneling to hopping transport. This study is valuable to realize the design of flexible spin devices using PVDF barriers operated at room temperature.

3.2. Field effect transistor

Recently, ferroelectric field effect transistor (FeFET) device architectures have been formed by using ferroelectric thin films as gate insulators because of the various advantages such as easily integrated structure, small cell sizes, low operating voltages, and nondestructive readout capability [14, 36]. The high ON/OFF ratio at zero gate voltage must be ensured to distinguish the different data recognition for nonvolatile ferroelectric memory. In generally, both ON and OFF source–drain current are strongly dependent on the charge density of semi-conducting layer, and the operating voltage of FeFET depends on the thickness and dielectric constant of the gate dielectric [66].

The composition of organic transistor has three main components: three electrodes including source, drain and gate; an active semiconductor layer; and a dielectric layer [37]. A FeFET was successfully fabricated utilizing 100 nm thick PVDF/PMMA (80:20) films as a gate insulator [14]. The capacitor with a 160 nm thick β-phase PVDF film exhibited the fairly large remanent polarization (Pr) of 7 $\mu C\ cm^{-2}$ with the coercive voltage (V_c) of 8 V corresponding to coercive electric field (Ec) of ~50MV/m (as shown in **Figure 8a**). A typical ferroelectric hysteresis with the drain current bistability at zero gate bias was shown in **Figure 8b** for a FeFET with the PVDF as gate dielectric and Agilent technologies E5270B parameter analyzer was used to characterize this transistor in a dark environment [10].

The Au/PVDF/SiO_2/p-Si stack is successfully prepared by Gerber et al., and the various dimension Au gate electrodes were deposited by vacuum evaporation. The inset diagram denotes the cross-section of the device in **Figure 9**. The FeFET exhibited excellent current-voltage characteristics for the various gate voltage V_g from 0 to +3.5 V [67]. The FeFET measurements were accomplished using a semiconductor parameter analyzer in a shielded metal box at room temperature.
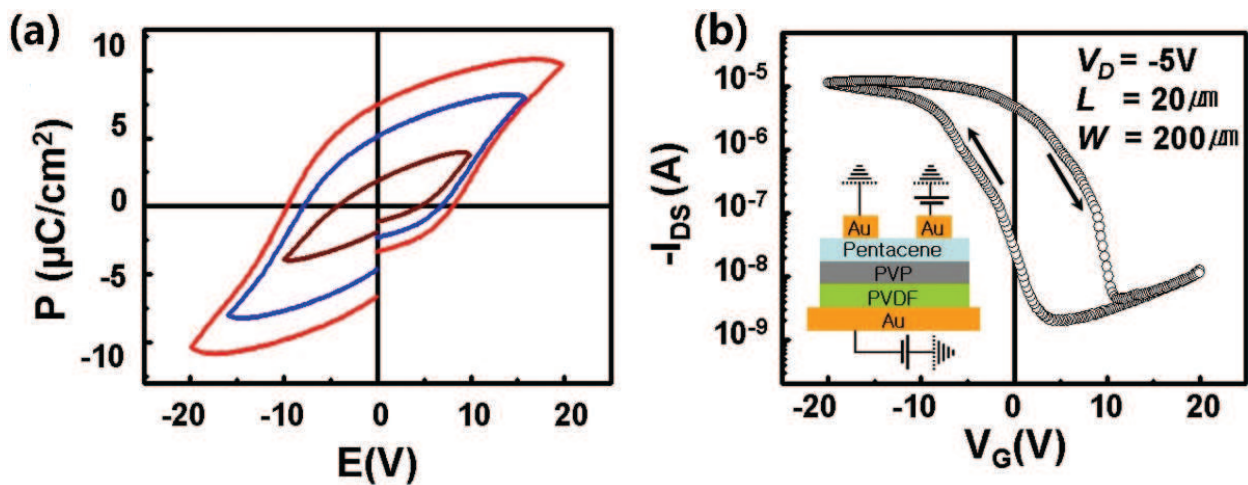
Figure 8. (a) Polarization vs. applied voltage (P-V) hysteresis loops of a PVDF film with thickness of 160 nm. (b) I_D–V_G transfer curve of organic thin film transistors (OTFTs) with PVDF–PVP as the bilayer gate dielectric. The hysteresis direction is denoted by arrows. The inset is the diagrammatic sketch of FeFET device structure [10]. This research was conducted at Yonsei University of Korea in 2008.
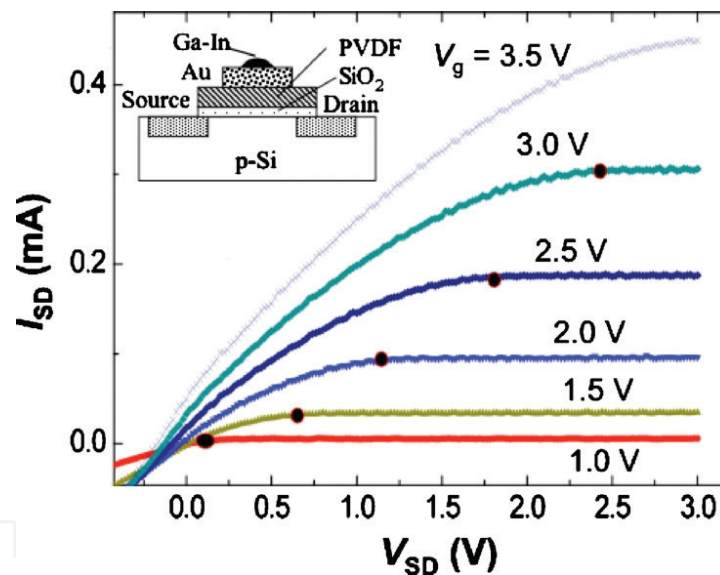
Figure 9. Source–drain current ISD curves depend on the gate voltage values for an Au/PVDF/SiO$_2$/p-Si FeFET. Inset: The cross-section of FeFET device [67]. This research was conducted at Research Center Jülich of Germany in 2010.

The high performance TFT device with a PVDF/GOnP nanocomposite as insulator has been found to have an ON/OFF current ratio of 10^5, and a field effect mobility of 1.1 cm^2 V^{-1} s, which can make the OTFTs operated successfully at voltages below 2 V [68].

3.3. Organic capacitors

The metal/ferroelectric polymer/metal (MFM) capacitor is a basic ferroelectric polarization storage component in memory storage devices, in which a ferroelectric polymer film is sandwiched between metal electrodes. Organic ferroelectric material PVDF has attracted much interest recently for its applications in low operating voltage, nonvolatile memory storage devices. Many researches are focused on MFM capacitors [69].

The structure of ferroelectric device has been shown in **Figure 10a**, in which a PEDOT:PSS layer as a hole-only (electron blocking) transport layer is inserted between the Al top electrode and the PVDF LB nanofilm. The chemical structure of PEDOT:PSS is shown in **Figure 10b**. Ferroelectricity was characterized at different voltage amplitudes (**Figure 5c**), which shows asymmetric displacement-electric field hysteresis loops. The hysteresis loops were characterized by a traditional Sawyer–Tower method. The Pr values depend on the electric field (**Figure 10d**) [70]. The Pr values increase with the increasing electric field, which is accordance with reference report [13]. The dipole moments of PVDF in the films are slightly oriented at a low electric field, and the dipole moments are highly oriented at a high electric field, thereby leading to the increase of Pr.

The asymmetric hysteresis loops for the capacitor with the PEDOT:PSS layer are different from that of the Al/PVDF LB nanofilms/Al device, which shows symmetric hysteresis loops [11]. Memory devices utilize the hysteresis by associating the positive remanent polarization (+Pr) and negative remanent polarization (−Pr) with a Boolean 1 and 0 [4]. Asadi et al. reported a diode with a Ag/PVDF:P3HT/LiF/Au capacitor, which possesses asymmetric hole accumulation properties under positive or negative polarization [22].

The low-density storage capability and slow switching speed are the major problems for most organic memory devices [71–73]. The performance of these devices can be greatly enhanced by several methods such as forming hybrid organic structures, [74] organic/inorganic
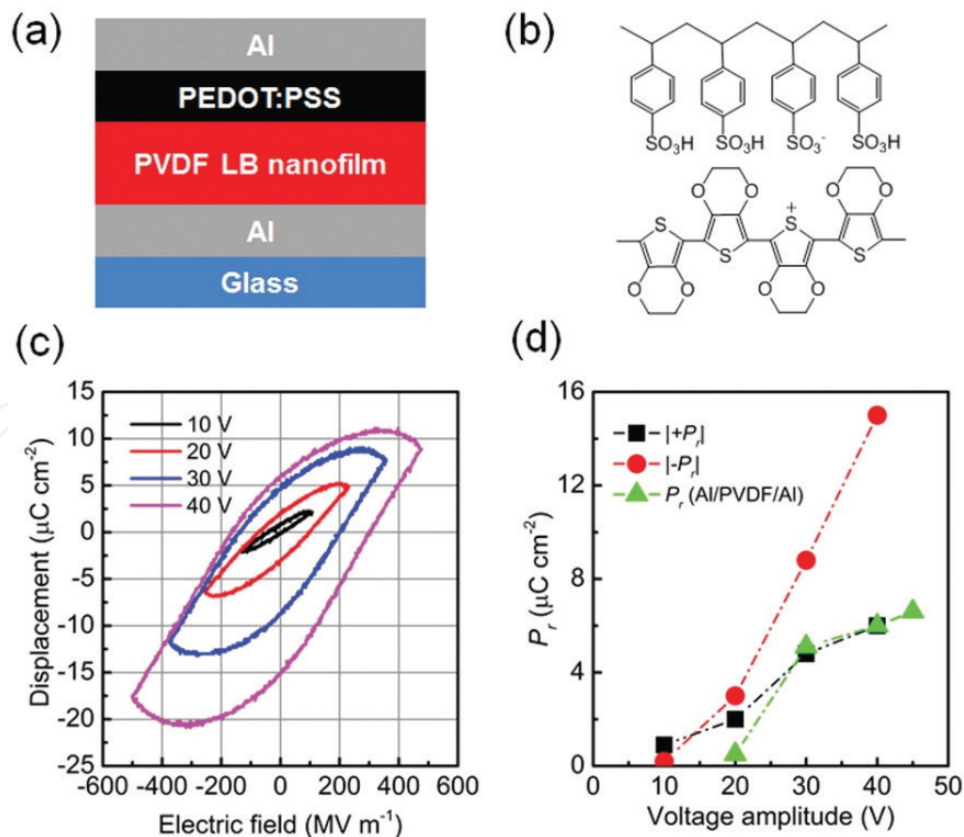
Figure 10. (a) Layer structure of the PEDOT:PSS ferroelectric device, (b) The chemical structure of PEDOT:PSS, (c) The hysteresis loops of the device at different applied voltage amplitudes, and (d) Pr values dependence of the electric field [70]. This research was conducted at Tohoku University of Japan in 2015.

composites, [75] or by dispersing nanomaterials [76]. The simple metal-insulator-metal (MIM) structure is shown in **Figure 11a**, in which the insulator part composed of graphene nano flakes (GR) embedded in PVDF layer was sandwiched between Platinum (Pt) top electrode and ITO bottom electrode. The nonvolatile resistive memory switching was investigated using this structure. The I–V characteristic curves under various compliance current of 1, 10 and 100 μA are shown in **Figure 11b**. The I–V curves were measured by a Keithley 2401 in top–bottom configuration.

The I–V characteristics of the Hg/PVDF/Au device were obtained by DC voltage sweep program (**Figure 12a**). The quick transition from high resistance state to low resistance state was realized at the set voltage. The resistance versus voltage (R-V) curves are shown in **Figure 12b**. A maximum resistance ratio of 25 may be practical for application in nonvolatile memory devices [34]. Several phenomena in capacitor structures exist in the literature used to explain the bistability using the filamentary conduction along with Schottky emission, trap charging and discharging, space charge limited current and Poole-Frenkel emission [78]. The I–V cycles were performed using a Keithley 238 SMU unit.

3.4. Organic diodes

The device structure of FeFETs would complicate the construction of a larger integrated memory technology. In addition, ferroelectric capacitors with relatively simple device structure have a limited scaling capability. Ferroelectric diodes can combine the advantages of FeFETs and capacitors. Therefore, there is an ongoing research activity in a diode structure to realize the resistive switching [4].

The semilogarithmic forward and reverse I–V characteristics of the Au/n-InP and Au/PVDF/n-InP Schottky diodes are shown in **Figure 13**. The I–V was measured using a Keithley source measuring unit 2400. The reverse leakage current of the Au/n-InP diode (6.809×10^{-5} A at −1 V)
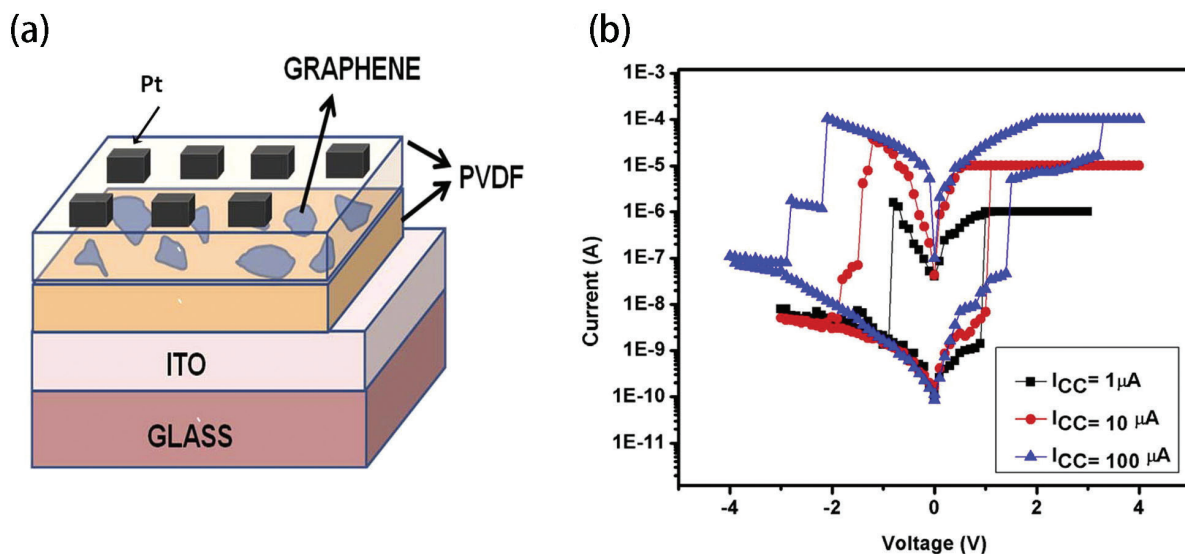

Figure 11. (a) Schematic diagram of the Pt/PVDF/GR/PVDF/ITO memory device fabricated layer by layer. (b) Typical I–V characteristic curves of the device under different compliance currents varying from 1 to 100 μA [77]. This research was conducted at University of Puerto Rico of USA in 2014.
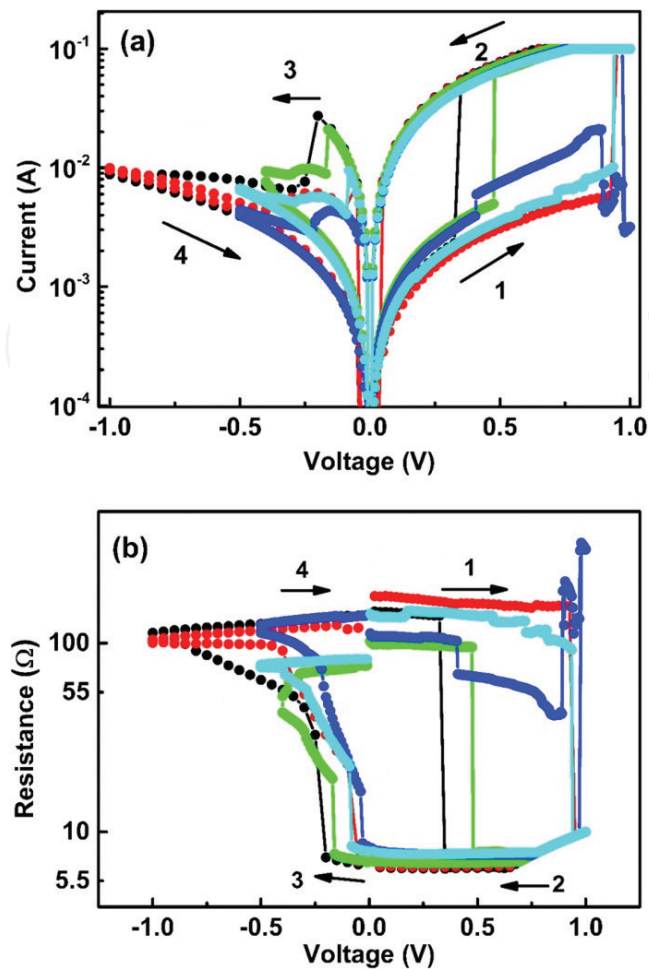
Figure 12. (a) I–V curves of the Hg/PVDF/Au device (b) R–V curves of the Hg/PVDF/Au device [34]. This research was conducted at Pondicherry University of India in 2017.

is higher than that of the Au/PVDF/n-InP diode (2.387×10^{-7} A at −1 V). This proves that the PVDF as an organic interlayer can improve the electrical characteristics of the Schottky diodes. The diode parameters are confirmed from the forward bias I–V curves, which can be described by the thermionic emission theory. The calculated barrier heights based on I–V measurements are 0.57 eV for Au/n-InP and 0.73 eV for Au/PVDF/n-InP. The increased barrier height indicated that the PVDF films can influence the space charge region of n-InP [79]. The Au/PVDF/ Si structure fabricated by Kim et al. showed good ferroelectric properties. The current density and memory window width for the PVDF film were about 10^{-6} A/cm^2 and 1.8 V under a bias voltage of 5 V, respectively [80].

The interfacial electrical properties will become very poor due to the diffusion of constituent atoms into the Si substrate, if a ferroelectric film is directly deposited on a Si substrate. In order to solve this problem, a metal-ferroelectric-insulator-semiconductor (MFIS) structure is formed with a buffer layer inserted between Si substrate and the ferroelectric film, as shown in **Figure 14** [81]. The MFIS diodes with low-voltage operation has attracted great interest because they can be used as one-transistor type nonvolatile memories [20, 82, 83]. The MFIS
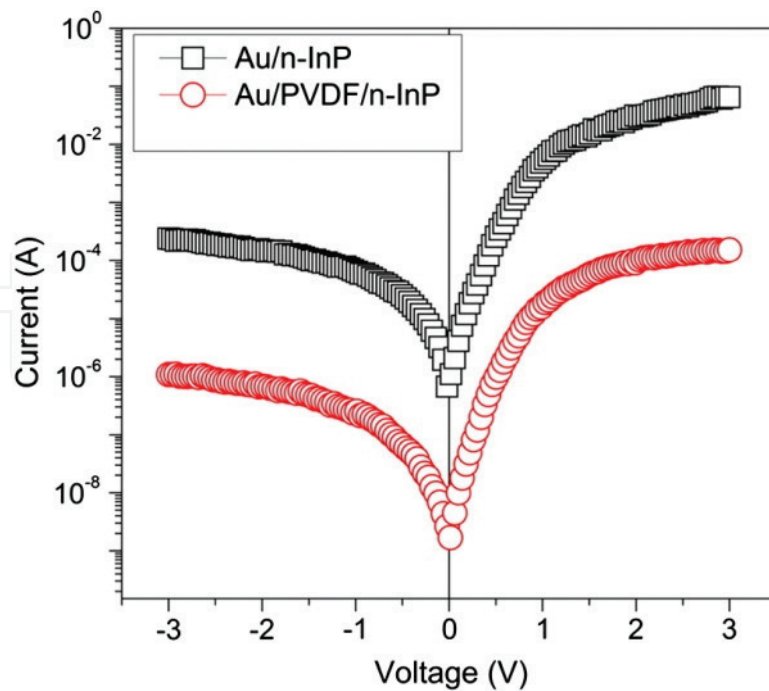
Figure 13. The forward and reverse bias I–V characteristics of Au/PVDF/n-InP and the Au/n-InP Schottky diodes at room temperature [79]. This research was conducted at Sri Venkateswara University of India in 2014.
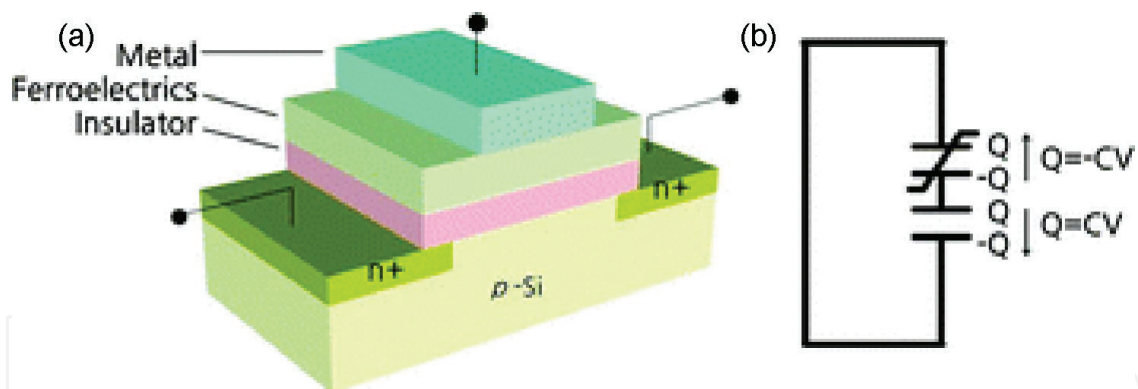
Figure 14. (a) Schematic drawings for the MFIS diodes and (b) The equivalent circuit of the MFIS structure [81]. This research was conducted at Waseda University of Japan in 2016.

diodes seem to have solved the problems of the MFS structure, but the retention characteristics of MFIS diodes are unreliable for commercialization in spite of considerable advancement in data retention time in recent reports [84, 85].

The metal-insulator-metal diode is composed of the thin layers of an n-type polymer such as PGSt as the dielectric material, and a p-type polymer such as PTMA, PVDF. The retention cycles of the ON and OFF states under open-circuit conditions persisted for more than 10^4 times [86].

4. Conclusion

Although there are still some crucial problems for PVDF applications, such as memory times, density storage, low operating voltage and so on, these are being solved. With more and more research done in this field, the more advanced fabrication method of PVDF films could be developed, and ferroelectric β-phase PVDF should have a promising future to build up the information storage units.

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Author details

Liuxia Ruan[1], Donghai Zhang[1], Junwei Tong[1], Jianli Kang[2], Yufang Chang[3], Lianqun Zhou[4], Gaowu Qin[1] and Xianmin Zhang[1]*

*Address all correspondence to: zhangxm@atm.neu.edu.cn

1 Key Laboratory for Anisotropy and Texture of Materials (Ministry of Education), School of Material Science and Engineering, Northeastern University, Shenyang, China

2 State Key Laboratory of Separation Membranes and Membrane Processes, Tianjin Polytechnic University, Tianjin, China

3 Computer Teaching and Researching Section, Shenyang Conservatory of Music, Shenyang, China

4 Suzhou Institute of Biomedical, Engineering and Technology, Chinese Academy of Sciences, Suzhou, China

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