Chapter 4

Selective Epitaxy of Group IV Materials for CMOS Application

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Additional information is available at the end of the chapter

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Abstract

As the International Technology Roadmap for Semiconductors (ITRS) demands an increase of transistor density in the chip, the size of transistors has been continuously shrunk. In this evolution of transistor structure, different strain engineering methods were introduced to induce strain in the channel region. One of the most effective methods is applying embedded SiGe as stressor material in source and drain (S/D) regions by using selective epitaxy. This chapter presents an overview of implementation, modeling, and pattern dependency of selective epitaxy for S/D application in CMOS. The focus is also on the wafer in and ex situ cleaning prior to epitaxy, integrity of gate, and selectivity mode.

Keywords: selective epitaxy, SiGe, RPCVD, CMOS

1. Introduction

Selective epitaxy of SiGe material is considered as one of the most important steps in the CMOS processing. This type of growth method was already discovered and highlighted in the 1990s with a focus on optimizing the growth parameters to improve the layer quality of Si/SiGe multi-layers [1–4]. The outcome of the initial works showed that {113} and {110} facet planes were mostly dominant, whereas other facet planes, e.g., {119} and {018}, could also appear at certain growth conditions. The activation energy for the growth rate on facet planes (Rhkl) was also calculated for growth temperature of 700–850°C. No significant change in the activation energy of deposition on {hkl} surfaces compared to (100) one was observed showing a similar kinetic growth ruled over these facet planes [1].

The facet formation results in a pileup shape at the edge of the epi-layer close to the oxide (see **Figure 1a–c**) [5–7]. The reason behind forming this pile shape is the diffusion of incoming Si or Ge atoms on the faceted surface is higher than those on the (001) surface at the central part of the oxide opening. This means that the molecules may move toward the central part, and if their diffusion length at a certain growth temperature is shorter than the opening size, a pileup shape is formed.

More detailed studies about facet formation showed the existence of chlorine during the epitaxy is the main factor dominating the growth rate for both Si and SiGe; however, the formation of the facets is correlated with the growth conditions and pattern geometry.

The application of SiGe as embedded layer source and drain (S/D) of pMOS was presented in year 2000 when (S/D) junctions were formed by a dry etch followed by the growth of highly B-doped SiGe [8]. This idea arose attention since no dopant implantation and post annealing for activation were necessary when the in situ doping of SiGe layer could provide high-quality epi-layers.

Later, the embedded SiGe layers were used as stressor material in the S/D regions to create uniaxial strain in the channel region. As the result of induced strain, carrier mobility in the channel is significantly improved. For the first time, $Si_{0.83}Ge_{0.17}$ layers were integrated by Intel in 90 nm technology node in 2003 [9], and since that year, the Ge content (or strain amount) was continuously increased in each new coming technology node up to 45% in 22 nm technology node [10, 11]. During this evolution of CMOS, a revolutionary design was introduced when the planar type of transistors was abandoned and three-dimensional (3D) transistors were implemented [12]. Such nanoscale 3D transistors were initially called Tri-Gate, but later

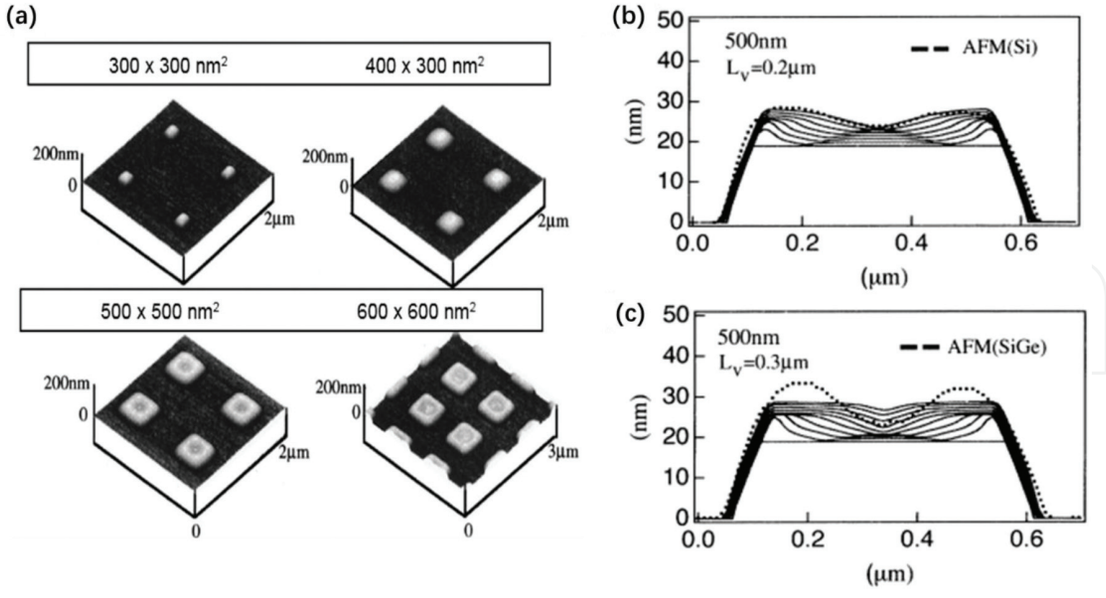

Figure 1. (a) AFM pictures of 6 nm selectively grown SiGe on 18 nm Si buffer layers grown at 740°C. The oxide layer has been removed and SiGe layers are in mesa shape. (b) and (c) show the cross section of simulated and the experimental cross-sectional profile (dotted line) for Si and SiGe layers, respectively [5].

this notation was changed to FinFETs to merge with the other groups' suggestion. In these transistors, selective epitaxy of SiGe layer was used to raise the S/D regions.

A drawback with selective epitaxy growth is that the SiGe layer profile is dependent on shape, size, and density of the oxide openings of S/D in a chip. This problem affects also the B concentration in SiGe since the incorporation of B is dependent on both the growth rate and the Ge content [13–21].

SiGe as channel material has been also proposed in the SiGe/Si vertical nanowire transistors when the lateral downscaling will finally reach the end of technology roadmap. In order to have a full control on the carrier transport in the channel region, gate-all-around (GAA) design has been proposed [22].

2. Chemical vapor deposition (CVD) technique

In the semiconductor industry, there are many different materials need to be grown during the device processing. CVD is also a process in which gaseous chemical precursors have chemical reactions on the wafer surface and deposit a layer of solid thin film. The rest of the by-products that are in gas phase can be easily pumped and leave the reaction surface. Among these CVD deposited thin films, SiGe is a key material, which offers the applications in a wide range of CMOS devices.

CVD is practiced in a variety of types, which are classified by the operating pressure:

1. Atmospheric pressure CVD (APCVD)—CVD at atmospheric pressure
2. Reduced-pressure CVD (RPCVD)—CVD at torr pressure
3. Low-pressure CVD (LPCVD)—CVD at mTorr pressure
4. Ultrahigh vacuum CVD (UHVCVD)—CVD at 10^{-8} torr pressure

Among these CVD techniques, RPCVD has shown the highest output, and it is accepted by semiconductor industry for epitaxy of Si and SiGe films for IC mass production.

For RPCVD, several precursors are available in the market for the Si growth such as silane (SiH_4), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), tetrachlorosilane ($SiCl_4$), disilane (Si_2H_6), and trisilane (Si_3H_8). Germane (GeH_4) and digermane (Ge_2H_6) are the common sources for Ge to grow $Si_{1-x}Ge_x$. The most commonly used precursors for p- and n-type doping are diborane (B_2H_6), phosphine (PH_3), and arsine (AsH_3), respectively. $As(GeH_3)_3$ is a gas source which is also used for n-type doping of SiGe layers at low growth temperature. These sources are usually diluted in H_2. For Sn growth, SnD_4 and $SnCl_4$ are the most practical and common sources [23]. Methylsilane (SiH_3CH_3) is widely used for carbon doping in Si and SiGe layers. Meanwhile, HCI and Cl_2 are the precursors used as the etch reactant to obtain the selectivity during the selective process.

3. Ex- and in-situ cleaning

The wafer cleaning process before the epitaxy has an important role for the epitaxy quality. The purpose of epitaxy is to duplicate the substrate atomic columns in deposition of a layer. Therefore, the presence of SiO_2, carbon and polymer residuals has to be removed from the Si surface [24].

As an example, **Figure 2** shows the micrographs of the samples prior and after the SiGe selective epitaxy. The presence of carbon residuals on Si surface is commonly formed during the plasma dry etch of oxide openings. The SiGe epitaxial layer can be only grown on the clean surfaces of Si, and the growth occurs through nucleation as shown in **Figure 2b** and **d**. The TEM EDS mapping analysis from the cross section of S/D areas in **Figure 2e** confirms the presence of carbon and oxygen residuals on the initial Si surface. Meanwhile, a standard chemical cleaning will remove all undesired impurities, and a two-dimensional SiGe layer could be grown successfully as shown in **Figure 2c** [25]. There are many different cleaning methods for Si wafers as following:

SPM: $H_2SO_4 + H_2O_2$ (4:1)

DHF: HF + DIW (1–2%)

HPM: $HCl + H_2O_2$+ DIW (1:1:6)

APM: $NH_4OH + H_2O_2 + DI\text{-}H_2O$ (1:1:5)

where DIW stands for deionized water. A diluted hydrofluoric acid in DIW (1% DHF) removes the native oxide, and the wafers are ready to be placed in the load locks of epi-reactor [26].

Later, an in situ cleaning in RPCVD reactor is required to remove the native oxide on the exposed Si surface. This process usually occurs at high temperature such as 1000–1100°C for monitoring Si wafers; meanwhile, for the patterned substrates, this is remarkably at lower temperatures (850–950°C).

SiGe material is grown in a recess in S/D regions in nanoscale transistors. The recess is formed by wet etch, and its shape can be rounded, sigma, or trapeze, and then the in situ is needed not only in removing the contaminants from the Si surface but also in preserving the recess shape. High annealing treatment results in Si loss and affects the recess shape. This is due to the thermal mismatch between Si and SiO_2 where Si reflows in the recess region. Si loss is a critical problem for the short-channel length transistors.

In conclusion, an appropriate low annealing temperature is sought to have a trade-off between all these requirements. **Figure 3** shows the results of in situ experiments on the quality of epi-layers and the recess shape at different annealing temperatures. In these experiments, 800°C for 7 min is recognized as the minimum temperature (and enough annealing time) to preserve the shape and improve the high quality of epi-layer [27].

The in situ annealing for three-dimensional (3D) transistors, e.g., FinFET, becomes more critical where the Si fin is small and any damage has a significant effect on the transistor performance.

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High-quality SiGe is required to be selectively grown on the S/D to induce the strain into the channel. Before the growth, the surface of Si fin has to be free of native oxide or any residual of impurities [28].

Figure 4a shows the HRTEM cross-sectional image of as-processed Si fin. Then the prepared samples were baked at different temperatures ranging from 740 to 825°C prior to epitaxy [29].

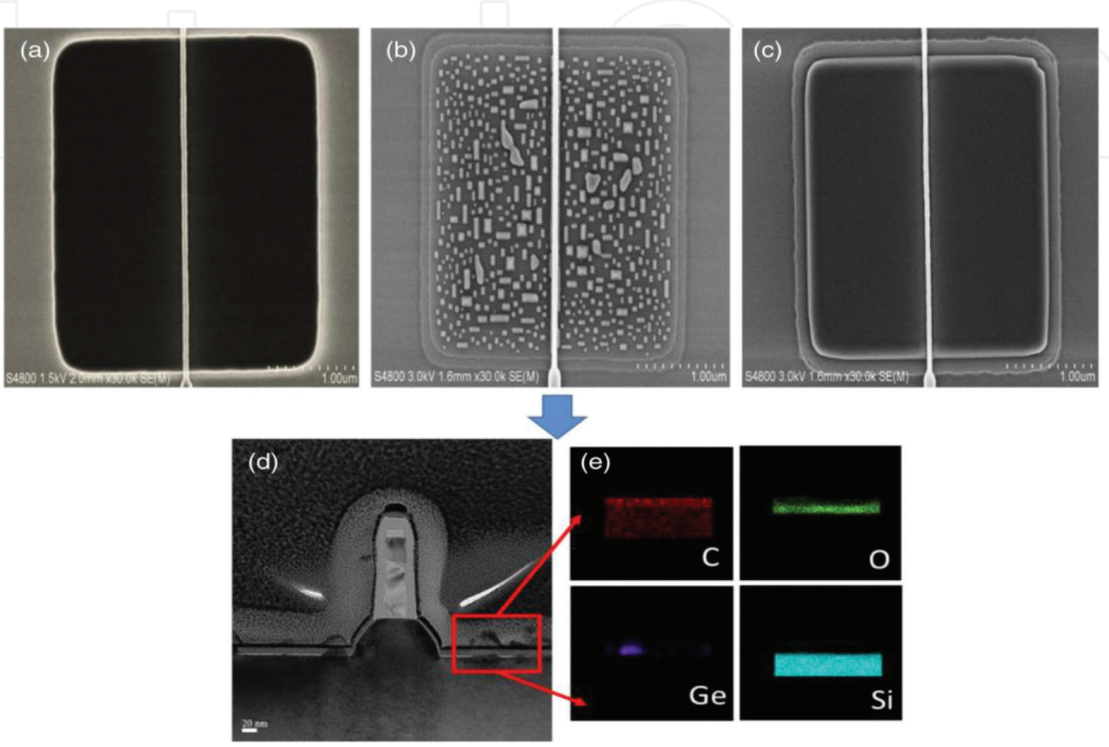

Figure 2. HRSEM images showing cross section of a planar transistor with 22 nm gate length (a) prior to SiGe growth and after SiGe epitaxy (b) with poorly cleaned Si surface and (c) with cleaned Si surface and (d) TEM cross section of sample in (b) and (e) TEM EDX mapping of sample in (b) [25].

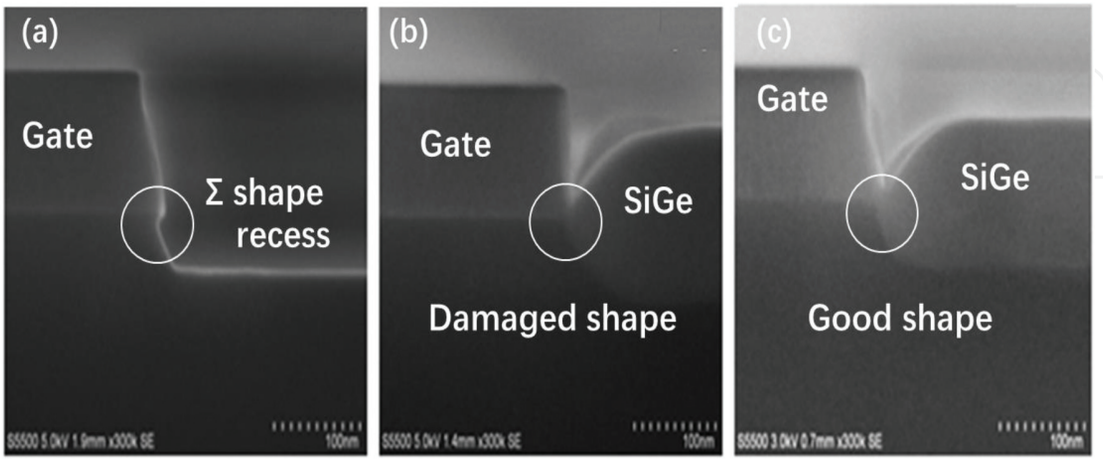

Figure 3. SEM images showing cross section of different prebaking condition samples (a) prior to prebaking, (b) prebaking temperature at 825°C, and (c) prebaking temperature at 800°C.

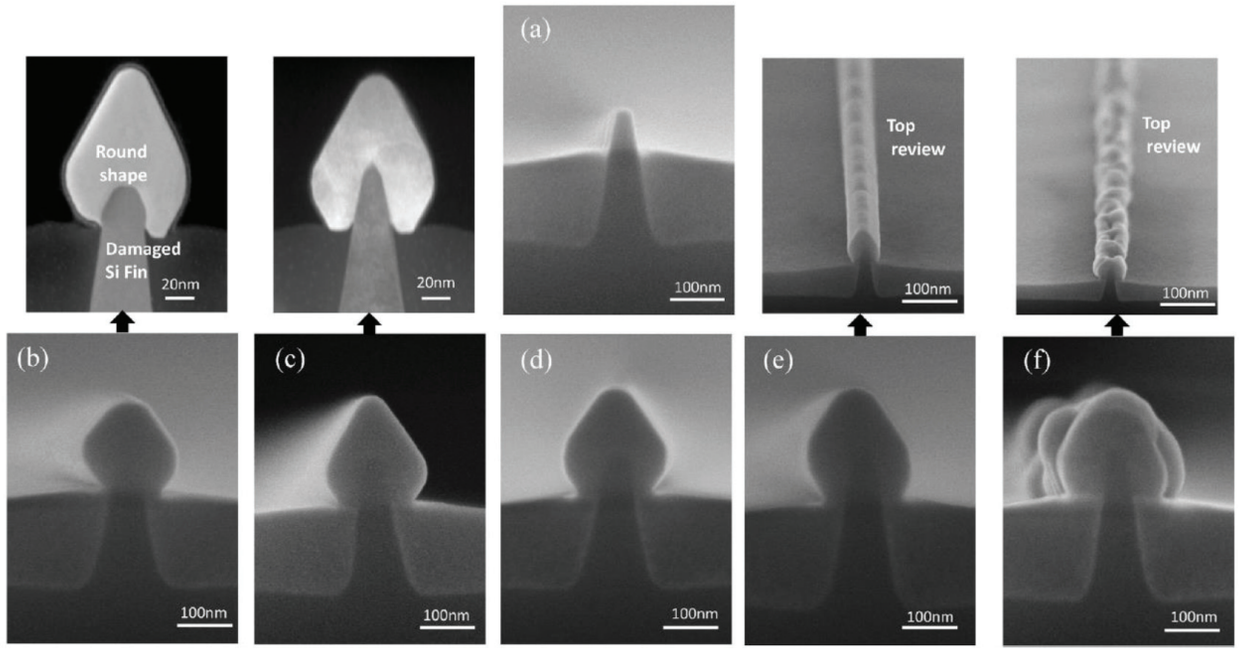

Figure 4. HRTEM and SEM cross-sectional images of the Si fins with different prebaking temperatures as follows: (a) the processed Si fin and annealed at (b) 825°C, (c) 800°C, (d) 780°C, (e) 760°C, and (f) 740°C [29].

Figure 4b reveals a serious damage on Si fin shape where the height of the fin has been shrunk and the top of the fin became rounded. Although the shape of Si fins was changed, SiGe layer could still be grown with reasonable quality. The irregularity of Si fins' shape at high temperature annealing was originated from Si migration and thermal mismatch between Si and SiO_2. Therefore, the lower baking temperature is chosen. The samples with 800 and 780°C prebaking in **Figure 4c** and **d**, respectively, had also high-quality Si fins and SiGe layers.

In general, an appearance for a successful SiGe growth is that the shape for layer coverage over the Si fin should be symmetric. The symmetry is important since it determines the uniformity of strain over the Si fins. Among the micrographs, **Figure 4e** has symmetric feature of SiGe layer, but this degrades by lowering the prebaking temperature to 760°C. **Figure 4f** shows that the surface roughness is the worst when the baking temperature is at 740°C. It is believed that asymmetric shape is a result of the residual native oxide remained on the surface of Si fins.

4. Gate integrity: HCI selectivity

The other importance of SiGe S/D epitaxy is selectivity of the growth. In the patterned structure, the surface of the gate sidewall consists of both oxide and nitride, which makes it difficult to obtain a selective growth, especially on the nitride spacer surface. However, in the worst case, at the top corners of the gate (poly-Si) would appear a "mushroom"-shaped deposition, which is difficult to be removed. To solve this issue and obtain a completely selective growth furthermore, HCl amount during the selective growth is needed.

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Figure 5 shows the cross-sectional images from SiGe S/D with long channel gates. When the HCl partial pressure is 50 mTorr, small SiGe nuclides are formed, and ploy-SiGe with a mushroom shape appeared on the top of gate sidewall (**Figure 5a**). **Figure 5b** shows how the selectivity is improved by optimizing HCl partial pressure to 65 mTorr. Based on the previous reports, the high amount of HCl results in higher Ge content and lower growth rate in SiGe epitaxy. It has also demonstrated that an increase of HCl partial pressure reduces the pattern dependency behavior of the growth. However, as **Figure 5c** shows, a ditch forms in vicinity to the gate sidewall when HCl amount is further increased to 80 mTorr. One reason of the non-planar filling of SiGe in S/D regions is due to the (311) facets close to oxide where the growth rate of SiGe on crystal direction (100) is higher than (311).

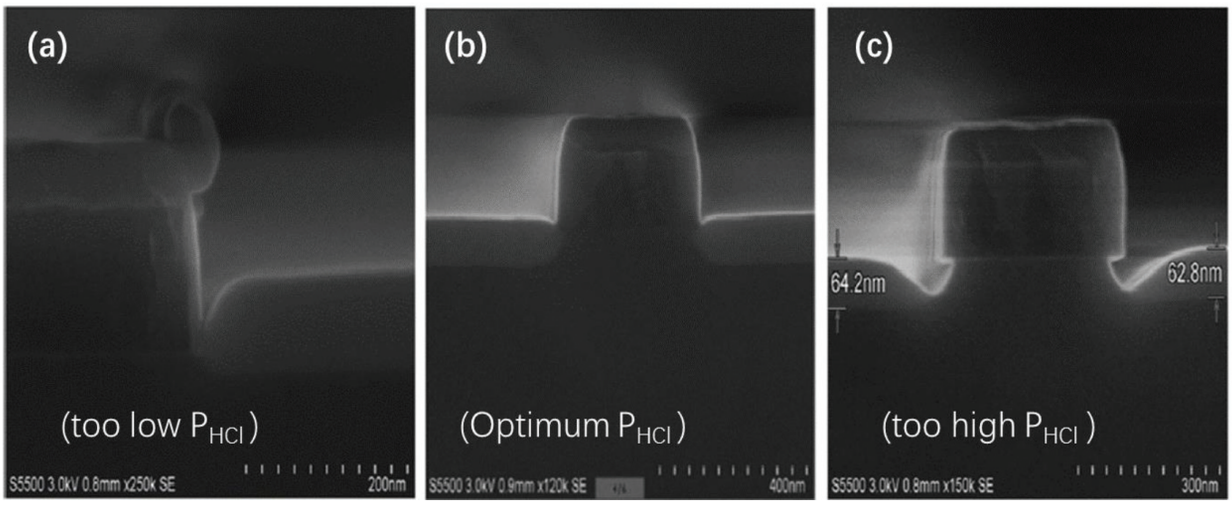

Figure 5. Cross-sectional SEM images of the gate and S/D regions after the SiGe growth when HCl partial pressures were (a) 50 mTorr, (b) 65 mTorr, and (c) 80 mTorr [25].

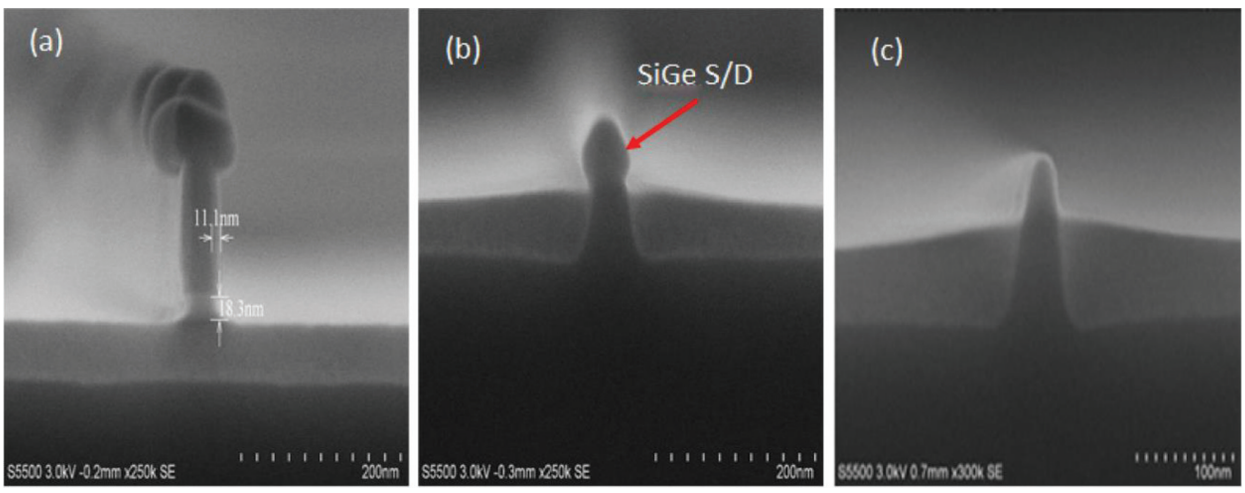

Figure 6. Cross-sectional SEM images of Si fin/SiGe samples when HCl partial pressures were the following: (a) 50 mTorr, (b) 60 mTorr, and (c) 70 mTorr [30].

Optimizing HCl partial pressure for 3D FinFETs is a more sensitive task. **Figure 6a–c** shows the SEM images from SiGe/Si fins grown with different HCl partial pressures. As the HCl amount is not enough (50 mTorr) and "mushroom" defects occur on the top of gate sidewalls (**Figure 6a**). However, when the amount of HCI was enhanced to 60 mTorr, a good selectivity for SiGe epitaxy could be achieved (**Figure 6b**). As shown in **Figure 6c**, further increase of HCl partial pressure to 70 mTorr leads to the case when the etch rate is higher than the growth rate resulting in no depositions on the Si fins (**Figure 6c**).

5. Pattern dependency of selective epitaxy

In order to provide a broad knowledge about the local and global pattern dependency, an example is pointed out here when the SiGe layers were grown selectively on S/D regions in transistors with 22 nm gate length [31]. **Figure 7a** shows a schematic of an 8-inch Si wafer containing 112 processed chips. The chips contain arrays of different transistor sizes (or coverage of exposed Si area varies) as shown in **Figure 7b**. This layout has been repeated for all the chips over the wafer.

In this figure, the blue cross marks illustrate the position of a transistor in the chip where the electrical measurements were done in all 112 chips. According to performance of transistors, at least three groups of chips (A, B, and C) with similar electrical characteristics (poor, good, and excellent) over the wafer were distinguished.

The Ge content in SiGe layers in transistors in A, B, and C groups was estimated to be 38, 40, and 35%, respectively by using energy-dispersive spectroscopy (EDS) technique. The growth

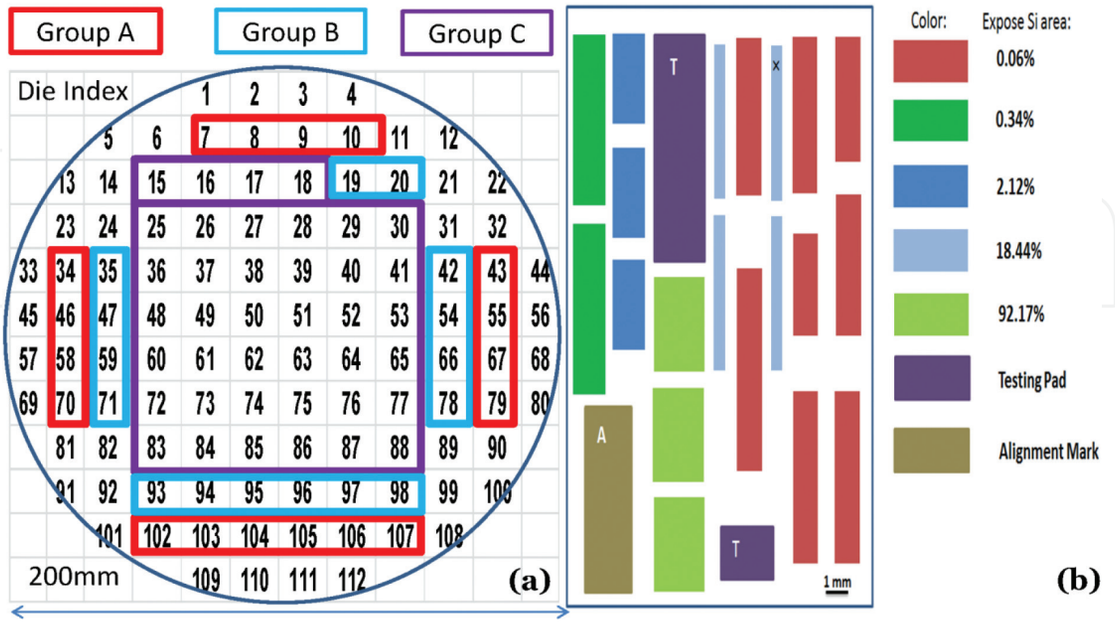

Figure 7. (a) The schematic picture of an 8-inch test wafer with 112 chips where three groups were marked after the performance of transistors. **Figure 7** (b) shows the layout of one chip where the exposed Si areas are nonuniform, and they are illustrated in different colors [31].

rate of SiGe was 0.58, 0.62, and 0.51 nm/s for transistors A, B, and C, respectively. The variation of Ge content and the growth rate affected also the threading dislocation density (TDD) in A, B, and C group transistors where TDD was estimated to be 3×10^9, 1×10^9, and 1×10^8 /cm^2, respectively. The amount of TDD is also related to strain relaxation in the epi-layers.

A more detailed information about the pattern dependency versus layout variation is demonstrated in **Figure 8**. The curves indicate that when the density of transistor arrays decreases, then both Ge content and the growth rate increase. The change of layer profile will directly affect the electrical characteristics of the transistor in the chip.

The transistor characteristics provide the data of V_{sat}, I_{on}, I_{off}, drain-induced barrier lowering (DIBL) and carrier mobility as shown in **Table 1** [31].

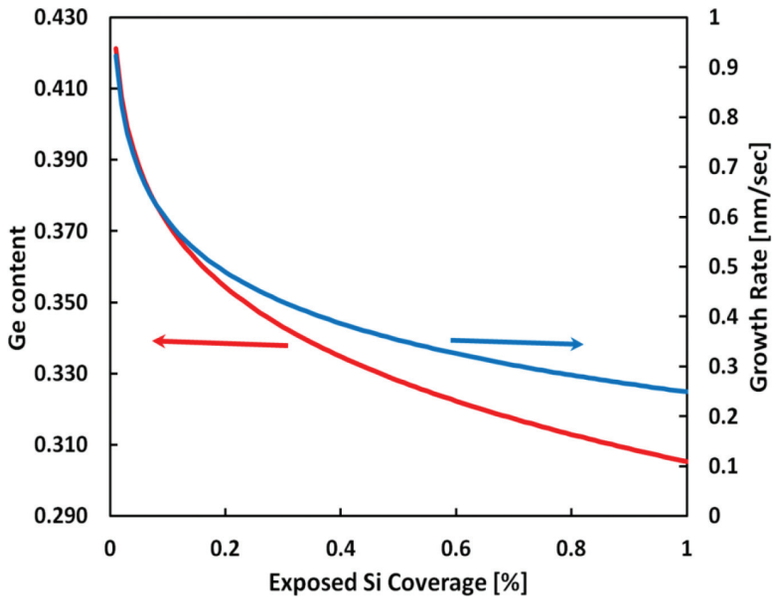

Figure 8. The calculated SiGe profiles for different exposed Si coverages [31].

Transistor group	Chip	Measured Ge content	VTsat (V) V_{DD} = 1 V	I_{on} (μA/μm)	I_{off} (nA/μm)	DIBL (mV)	Mobility (cm^2/Vs)
A	8		−0.46	263	0.34	75.4	24
	9	0.38	−0.54	111	0.24	91.3	13
	10		−0.56	86	0.47	112	9
B	71		−0.39	407	0.82	101	36
	82	**0.40**	−0.39	420	0.86	90	37
	92		−0.39	405	0.65	96	35
C	27		−0.32	598	4.8	115	65
	38	0.35	−0.30	618	9.8	123	71
	50		−0.28	619	10.2	119	75

Table 1. A summary of electrical data for three transistor groups A, B, and C.

It is well known that the presence of misfit dislocations is a sign of strain relaxation in the epilayer. In **Table 1**, transistors in group C have the best electrical performance compared to the others since the Ge content is lowest as well as the defect density. For example, the mobility values are remarkably high for this group.

It is important to emphasize here that the transistor profile is not optimized in all these groups; therefore, the electrical values are not impressive, but only the pattern dependency of epitaxy was in the interest of the discussions.

6. Kinetics of SiGe selective growth

The serious problem with integration of selective epitaxy growth is pattern dependency. The origin of pattern dependency behavior is the nonuniform consumption of reactant gas molecules over the patterned wafer [13–19, 21, 31]. The kinetics of growth is explained by gas molecules move in a laminar flow over the wafer forming boundaries [32].

In CVD, the gas steam through the reactor quartz is under a friction force with the stationary susceptor/substrate, creating stagnant gas boundaries during the gas flow. Gas molecules diffuse/are being attracted downward through the gas boundaries toward the susceptor and finally are consumed on the Si wafer. The length of the attraction force on the gas molecules over the wafer was estimated in the range of 10–15 mm for a total pressure of 20–40 torr in the CVD reactor [33].

Figure 9 illustrates a schematic view of the gas kinetics. In this figure, the black arrows illustrate the direction of molecule movement toward the exposed Si areas (transistor arrays in a chip) of a patterned substrate.

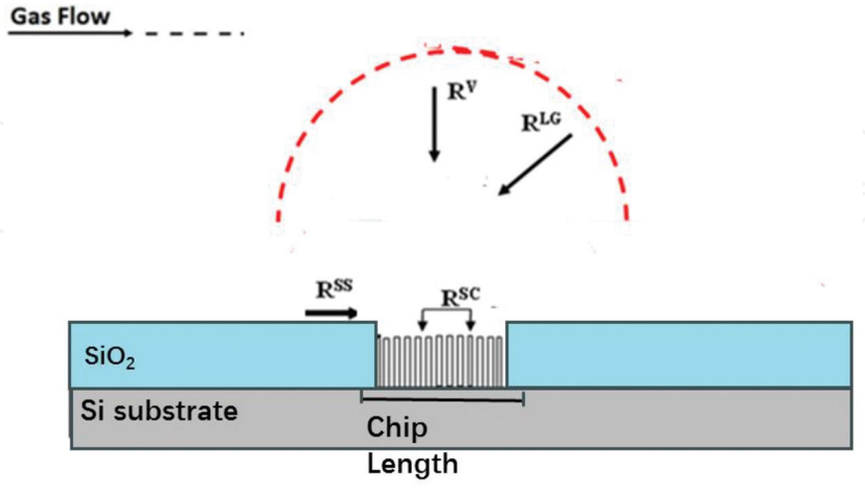

Figure 9. Schematic view of gas flow in different directions over a chip containing planar transistors.

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The gas molecules are moved in four possible directions toward the exposed Si areas in a patterned substrate and contribute to the selective epitaxy growth as follows:

a. Vertically in gas phase (R^{V})

b. Laterally in gas phase (R^{LG})

c. Surrounding oxide (or nitride) surface between the chips (R^{SS})

d. Oxide surface between the openings within a chip (R^{RC})

The total growth rate (R_{Tot}) can be written as a sum of contributions from incoming molecules from all four directions as follows:

$$R_{Tot} = R_{Si}^{V} + R_{Si}^{LG} + R_{Si}^{SS} + R_{Si}^{SC} + R_{Ge}^{V} + R_{Ge}^{LG} + R_{Ge}^{SS} + R_{Ge}^{SC} - R_{E}^{V} - R_{E}^{LG} - R_{E}^{SS} - R_{E}^{SC} \quad (1)$$

In Eq. (1), R^{SS} and R^{SB} are changed due to layout variation of the chip, and they are the main components behind the pattern dependency behavior.

Many studies have tried to decrease the pattern dependency by optimizing the growth parameters e.g., applying high HCl partial pressure or low total pressure during epitaxy [34]. The effect of high HCl is to terminate the lateral components in Eq. (1). The success to reduce the pattern dependency by increasing HCl partial pressure is good; however, it is not effective to eliminate the pattern dependency problem. This method demands high HCl partial pressure which leads to very low growth rate as shown in **Figure 10**.

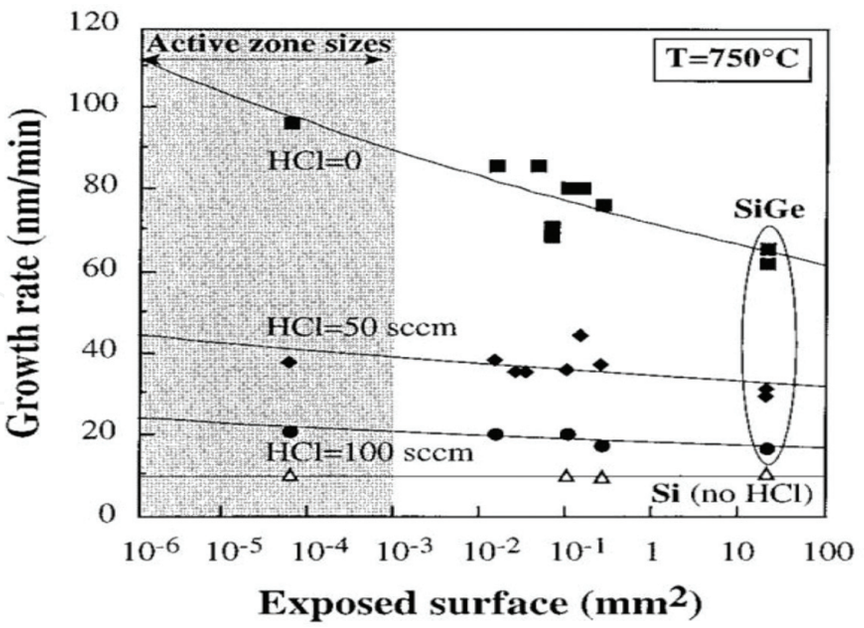

Figure 10. Growth rate of SiGe vs. exposed areas in the chip for the growth at 750°C. The precursor parameters for SiGe growth were the following: (Ge/Si) g = 0.0125, DCS = 200 sccm, and HCl = 0, 50, and 100 sccm [34].

Another method to decrease pattern dependency is proposed to increase the hydrogen carrier gas as well as apply low growth pressure. In this way the number of atoms coming laterally is decreased, but high hydrogen gas demands a better safety of the epi-tool [21].

There is another approach to deal with pattern dependency where an empirical model calculates the layer profile of SiGe and later the layout can be modified for a uniform deposition over the chip or wafer. Such a model has to calculate the components in Eq.(1) where diffusion, adsorption, and desorption of atoms during epitaxy have to considered.

7. Modeling of SiGe selective growth

One of the early works for modeling of Si epitaxy was presented by Meng Tao et al. [35]. The scaffold of the model is based on Maxwell distribution function for the molecules impinging to a surface during epitaxy. In this case, in epitaxy the number of the reactant molecules/unit time (*dn*) with an activation energy in an interval of (E_A, E_A + dE_A) incoming to a unit area according to Eq. (2):

$$\mathrm{dn} = 8\pi \mathrm{N_m}\left(\frac{1}{2\pi \mathrm{m_m k_b T}}\right)^{\frac{3}{2}} \mathrm{m_m E_A exp}\left(-\frac{\mathrm{E_A}}{\mathrm{k_b T}}\right)\mathrm{dE_K} \tag{2}$$

where N_m and m_m are the number of molecules/unit volume and are the mass of the reactant molecules in the gas. Si growth is the simplest epitaxy where dichlorosilane ($SiCl_2$) is used as precursor. For SiH_2Cl_2 epitaxy, the chemical reactions occur through Cl dissociation and are written as follows:

$$SiH_2Cl_2(g) \rightarrow SiCl_2 + H_2(g) \tag{R1}$$

$$SiCl_2 \rightarrow SiCl + Cl \tag{R2}$$

The growth rate can be calculated by integrating Eq. (2), and it is obtained by:

$$R = \frac{n}{N_0} = \beta \frac{\left(1 - \theta_{H(Si)} - \theta_{Cl(Si)}\right)}{N_0} \frac{P_{SiH_2Cl_2}}{(2\pi m_{SiH_2Cl_2} k_b T)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2}}{k_b T} + 1\right) \exp\left(-\frac{E_{SiH_2Cl_2}}{k_b T}\right) \tag{3}$$

where β is a unitless constant and θ, $P_{SiH_2Cl_2}$, m, N_0, and $E_{SiH_2Cl_2}$ are the coverage of hydrogen or chlorine on Si surface, partial pressure of DCS, molecular mass of DCS, number of Si atoms in a unit volume of crystal, and activation energy for the growth, respectively.

For selective epitaxy in the presence of HCl, the growth rate is decreased, and it can be:

$$R_T = R_{Si}^V - R_E^V \tag{4}$$

Experimental results show that the etch rate is not linearly dependent on HCl partial pressure (P_{HCl}) parameter and it has a sublinear relationship ($P_{HCl}^{0.596}$). This behavior could be referred

to the fact that all chlorine atoms may not participate during the etch process. Therefore, Eq. (3) is modified as follows:

$$\begin{aligned} R_T = \quad & \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{SiH_2Cl_2}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2}}{k_b T}\right) \\ & \times -\frac{\gamma}{N_0} \frac{P_{HCl}^{0.596}}{\left(2\pi m_{HCl} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right) \end{aligned} \tag{5}$$

where γ is a unitless S constant which relates to the HCl molecule distribution in the CVD chamber. The activation energy of etching part is estimated to be 37.5 Kcal/mol. This value lies between 22 and 44 Kcal/mol which is the needed energy to break one or two Si-Si bonds.

For the growth of SiGe layers in the presence of HCl, GeH_4 precursor has been introduced into the CVD chamber. In this case, Eq. (4) should be written as follows:

$$R_T = R_{Si}^V + R_{Ge}^V - R_E^V \tag{6}$$

The SiGe epitaxy is significantly different than Si epitaxy, since the presence of Ge atoms increases the growth rate.

The growth rate is increased due to two reasons; at first, the activation energy for SiGe deposition is lowered when Ge is added during epitaxy. The activation energy for Ge is 0.61 eV compared to 2.08 eV for Si, and for SiGe, this value should lie between Si and Ge ones. At second, the presence of Ge increases the available sites (or dangling bond sites) on the Si surface owing to increase of desorption energy of hydrogen and chlorine from Si surface. In this case, Si atoms can easily find the available sites and bind to the lattice, and therefore the growth rate is increased. The above reasons make the SiGe growth more complicated than Si, and therefore Eq. (6) cannot simply be used for SiGe epitaxy. In this case, a coefficient "m" is implemented, and the revised equation for SiGe growth in the presence of HCl is given by:

$$R_T = R_{Si/Si}^V + R_{Ge/Si}^V + mR_{Ge/Si}^V - R_E^V \tag{7}$$

The full form of equation for the SiGe growth rate can be obtained from:

$$\begin{aligned} R_T = \quad & \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{GeH_4}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2\ on\ Si}}{k_b T}\right) \\ & +\chi \frac{(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{GeH_4}}{\left(2\pi m_{GeH_4} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{GeH_4 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{GeH_4 on\ Si}}{k_b T}\right) \\ & \times -\frac{\gamma}{N_0} \frac{P_{HCl}^{0.596}}{\left(2\pi m_{HCl} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right) \end{aligned} \tag{8}$$

where χ is a constant which depends on the gas property. In above equation, the m coefficient is estimated to be 2 for growth temperatures 600–725°C [36].

A series of input parameters, e.g., Ge, Si, and HCl partial pressures, can be inserted in Eq. (8), and the etch rates during SiGe epitaxy can be extracted [37]. The experimental data show Arrhenius curves, and the activation energy can be obtained from the slope of these curves. The results show that the activation energy is decreased with increasing Ge partial pressures as shown in **Figure 11**. This outcome could be predicted since the strength of atomic bond in Si matrix becomes weaker with increasing Ge content (or strain).

The dependence of activation energy to Ge partial pressure is expressed as:

$$E_{Etching} = E_{a,\,Etching(Si)} e^{-12.535 P_{GeH_4}} \tag{9}$$

where $E_{a,Etching(Si)}$ is the activation energy for etch of Si. It is worth mentioning here that the activation energy in **Figure 11** differs from the previously reported values to etch SiGe bulk materials [38]. This difference in activation energies can be explained by the fact that the energies to etch SiGe in bulk form and during SiGe epitaxy are entirely different processes.

The Ge content, x in $Si_{1-x}Ge_x$ layers, can be obtained from Ge and Si partial pressures using the following [16]:

$$\frac{x^2}{1-x} = \sigma\left(\frac{P_{GeH_4} - (1-\eta)P_{HCl}}{P_{SiH_2Cl_2} - \eta P_{HCl}}\right) \tag{10}$$

where σ is a constant which links to chemical reactions in CVD reactor and η is a reaction rate coefficient which lies in a range between 0.9 and 1 depending on HCl partial pressure. The experimental data demonstrate that η is 1 when HCl partial pressure is lower than DCS partial pressure; otherwise it is ~0.9 for higher HCl pressures. The constant σ is related to adsorption and desorption of the main species during CVD, and it is written in the following equation below:

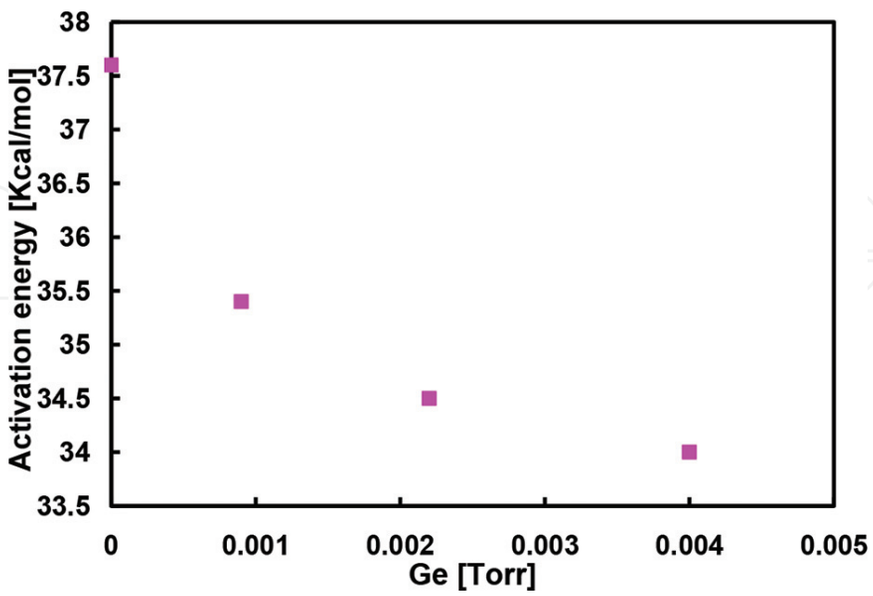

Figure 11. Activation energy vs. Ge partial pressures for etch part during SiGe epitaxy.

$$\sigma = \frac{k_{a,\,GeH_2} \times k_{d,\,H}}{k_{a,\,SiCl_2} \times k_{d,\,Cl}} = Aexp\left(\frac{E}{kT}\right) \tag{11}$$

The adsorption energy difference ($E_{a,SiCl2} - E_{a,GeH2}$) is ~0.1 eV [39], and the desorption energy difference is ~0.48 eV [40]. Then, the total activation energy is valued to 0.58 eV which is close to the derived energy value (0.697 eV) [37].

Until now, the vertical components in Eq. (1) have been discussed and calculated. The lateral components can be derived in the same way when these parameters are used for the patterned substrates [37]. A few assumptions have to be considered in order to make the calculations easier. At first, it is defined that a wafer has a global pattern when the chip layout is uniform and it is repeated over the entire wafer.

At second, the HCl partial pressure has to be enough to ensure the selectivity of the growth.

The results from Si deposition on patterned substrate have demonstrated that the growth rate is decreased when the coverage of the exposed Si areas becomes smaller. **Figure 12** demonstrates the growth rate from five globally patterned wafers with different exposed areas. The figure confirms the behavior of Si epitaxy is different than SiGe epitaxy [41, 42].

This discrepancy is due to the presence of R_{HCl}^{SC} in Eq. (1), which is formed through the lateral diffusion of Cl atoms on the oxide surface in a fully selective mode. The contribution of this component was found to be inversely related to the exposed Si areas:

$$P_{HCl}^{SC} = AP_{HCl}\ln\left(\frac{1}{c}\right) \tag{12}$$

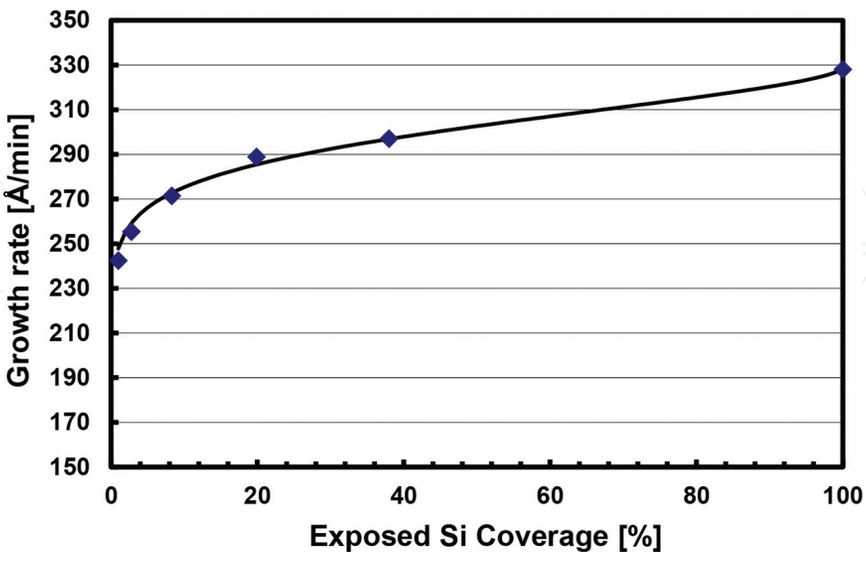

Figure 12. Growth rate vs. coverage of exposed Si for five different globally patterned wafers in total pressure of 20 torr. The P_{DCS} and P_{HCl} were 120 and 20 mTorr, respectively [37].

where c stands for the coverage of exposed Si areas of the chip and A is a parameter that depends on which type of mask is used for isolation material. Thus, Eq. (15) can be reformulated as follows:

$$R_T = \beta\frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{P_{SiH_2Cl_2}}{(2\pi m_{SiH_2Cl_2}k_bT)^{\frac{1}{2}}}\left(\frac{E_{SiH_2Cl_2on\ Si}}{k_bT}+1\right)\exp\left(-\frac{E_{SiH_2Cl_2on\ Si}}{k_bT}\right)$$
$$\times-\frac{\gamma}{N_0}\frac{P_{HCl}^{0.596}}{(2\pi m_{HCl}k_bT)^{\frac{1}{2}}}\left(\frac{E_{Etching}}{k_bT}+1\right)\exp\left(-\frac{E_{Etching}}{k_bT}\right)-\frac{\gamma}{N_0}\frac{(AP_{HCl}\ln(1/c))_{HCl}^{0.596}}{(2\pi m_{HCl}k_bT)^{\frac{1}{2}}}\left(\frac{E_{Etching}}{k_bT}+1\right) \quad (13)$$
$$\times\exp\left(-\frac{E_{Etching}}{k_bT}\right)$$

For SiGe epitaxy, GeH_4 precursor is introduced to the reactant gases which increases the Cl desorption, and therefore, the lateral diffusion of Cl becomes minor [43].

In a similar way, the later component for Ge atoms on the oxide surface P_{Ge}^{SC} can be written as:

$$P_{Ge}^{SC} = BP_{GeH_4}\ln\left(\frac{1}{c}\right) \quad (14)$$

where B is a parameter similar to Eq. (15) which is dependent on the mask material and c is the exposed Si coverage of the chip. Due to the lateral diffusion of Ge atoms on the oxide surface, an activation energy of 0.1 eV is added to the activation energy of the growth. In this case, the total growth rate for SiGe epitaxy is written as:

$$R_T = \beta\frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{P_{GeH_4}}{(2\pi m_{SiH_2Cl_2}k_bT)^{\frac{1}{2}}}\left(\frac{E_{SiH_2Cl_2on\ Si}}{k_bT}+1\right)\exp\left(-\frac{E_{SiH_2Cl_2\ on\ Si}}{k_bT}\right)$$
$$+\chi\frac{(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{P_{GeH_4}}{(2\pi m_{GeH_4}k_bT)^{\frac{1}{2}}}\left(\frac{E_{GeH_4on\ Si}}{k_bT}+1\right)\exp\left(-\frac{E_{GeH_4on\ Si}}{k_bT}\right)$$
$$+\chi\frac{(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{(BP_{GeH_4}\ln(1/c))}{(2\pi m_{GeH_4}k_bT)^{\frac{1}{2}}}\left(\frac{E_{GeH_4on\ Si}+0.1eV}{k_bT}+1\right)\exp\left(-\frac{E_{GeH_4on\ Si}+0.1eV}{k_bT}\right)$$
$$-\frac{\gamma}{N_0}\frac{P_{HCl}^{0.596}}{(2\pi m_{HCl}k_bT)^{\frac{1}{2}}}\left(\frac{E_{Etching}}{k_bT}+1\right)\exp\left(-\frac{E_{Etching}}{k_bT}\right) \quad (15)$$

The lateral contribution of Ge on the oxide surface has to be considered in the composition in Eq. (12) as well, and therefore the equation is modified as:

$$\frac{x^2}{1-x} = \sigma exp\left(\frac{0.7eV}{k_bT}\right)\left(\frac{P_{GeH_4}+(BP_{GeH_4}\ln(1/c))-(1-\eta)P_{HCl}}{P_{SiH_2Cl_2}-\eta P_{HCl}}\right) \quad (16)$$

Figure 13a and **b** show the experimental and calculated outcomes for the SiGe selective epitaxy. A good agreement between the experimental data and the calculated one is observed for patterned wafers.

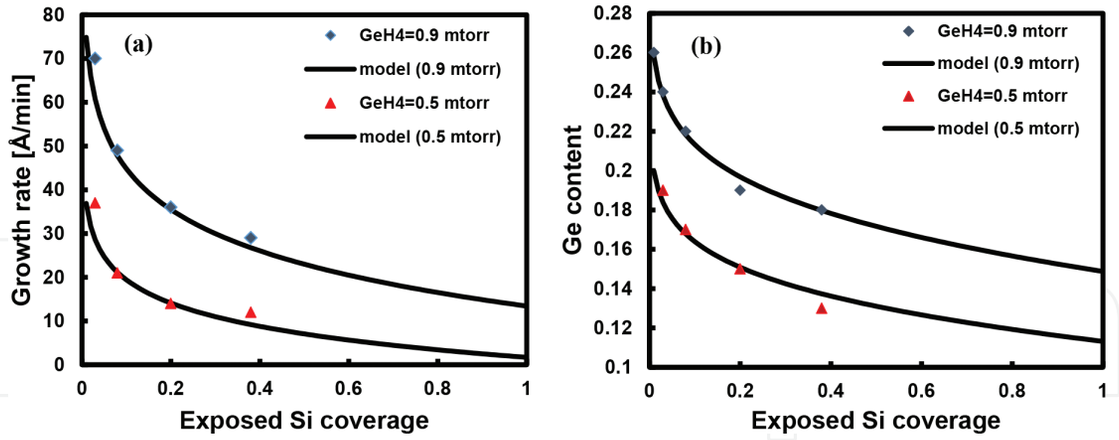

Figure 13. (a) Growth rate vs. chip exposed Si coverage and (b) Ge content vs. chip exposed Si coverage for SiGe layers grown at 20 torr on wafers with different global patterns. The applied $P_{SiH2Cl2}$ and P_{HCl} were 60 and 20 mTorr, respectively [37].

Until now, all calculations were for chips in wafers with global layout which in fact is an ideal case; however, for many cases, the layout of chips is nonuniform. When the layout varies the gas consumption over, the chip (wafer) becomes nonuniform. The part of chip with largest exposed area would attract stronger the surrounding atoms toward itself compared to the other part of the chip. This means that there is an interaction between different areas in the chip where the growth rate at part of the chip with highly exposed Si area (R_{Trap}) has an influence in neighboring parts (R_{surr}). The interaction range between two individual parts is denoted "τ(c)" where parameter "c" stands for exposed Si coverage in the chip. Then the growth rate of any part of chip which is located at a distance d (R(d)) can be written according to this interaction theory as follows [19]:

$$R(d) = R_{Trap} + \left(R_{Surr} - R_{Trap}\right)\left(1 - \exp\left(\frac{-d}{\tau(c)}\right)\right) \tag{17}$$

Parameter "τ" depends on the exposed coverage of the chip since the dangling bonds are creating an attraction force which drags the gas molecules.

Therefore, the gas consumption has to be uniformly over the chip in order for growth rate to be uniform. In this case, the trap parts have to be distributed over the chip and not isolated. As an example, **Figure 14** shows a nonuniform chip with six regions with exposed Si coverage areas of 0, 1, 3, 8, and 10%. At first, the trap regions are identified as 8 and %10 in this chip since the coverage is highest. Later, the interaction length between the six areas has to be calculated mutually. The condition for uniform gas consumption over this chip can be achieved either by inserting dummy features or by subdividing the trap areas over the chip or both methods.

The modeling of SiGe selective growth for advanced chip layout inaugurates a new window for chipmakers to deposit epi-layers with high quality and high uniformity over the wafer.

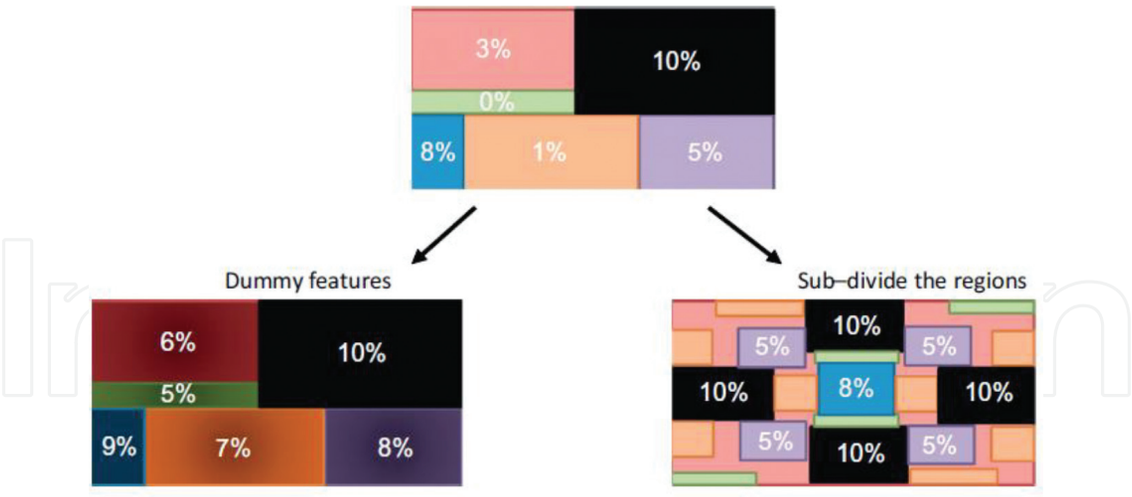

Figure 14. Design of chip layout to obtain uniform SiGe deposition.

8. Strain mechanism in group IV materials

Strain is a mechanical deformation which is resulted when a crystal with a lattice mismatch is epitaxially deposited on a substrate. The crystal of the deposited material has to align to the substrate, and as a result, the crystal is deformed. Strain is categorized in two types depending on whether the direction of the applied force is inward (compressive strain) or outward (tensile strain). Therefore, the strain is a hidden energy in the crystal which affects the electrical, mechanical, and optical properties of the semiconductor. Compressive strain, which is generated by SiGe layers by using selective epitaxy, has been the core discussion in this book chapter. Compressive strain is applied in pMOS to increase the hole mobility in the channel.

In general, the mobility is defined as:

$$\mu = \frac{q < \tau >}{m^*} \tag{18}$$

where m* stands for the effective mass and τ expresses the scattering time for the carriers [11].

The compressive strain splits the heavy and light hole (HH and LH) bands and changes the curvature of these bands. The latter effect is directly related to the decrease of effective mass for holes, whereas the first effect decreases the holes' scattering between the HH and LH bands. Both these effects have direct impact on $< \tau >$ and m* [11].

Other ways to describe the transport properties in the channel of transistor in the presence of compressive strain piezoresistance coefficients are commonly calculated. These coefficients are expressed in respect to mobility's fractional variations as:

$$\Delta\mu/\mu \approx |\pi//\sigma// + \pi_{\perp}\sigma_{\perp}| \tag{19}$$

where $\sigma_{\perp}$ and $\sigma_{//}$ are the transverse and longitudinal stresses and $\pi_{//}$ and $\pi_{\perp}$ denote for the piezoresistance coefficients in longitudinal and transverse directions. The piezoresistance coefficients can also be written in form of the three fundamental coefficients $\pi 11$, $\pi 12$, and $\pi 44$ [44].

The recent results have demonstrated that compressive strain along <110> has highest piezoresistance coefficients for both (001) and (110) wafers. As a result, <110> channel direction has been mainly applied for industrial applications [45, 46].

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