

We are IntechOpen, the world's leading publisher of Open Access books Built by scientists, for scientists

4,800

Open access books available

122,000

International authors and editors

135M

Downloads

Our authors are among the

154

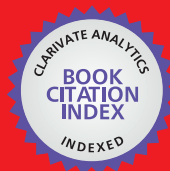
Countries delivered to

TOP 1%

most cited scientists

12.2%

Contributors from top 500 universities



WEB OF SCIENCE™

Selection of our books indexed in the Book Citation Index
in Web of Science™ Core Collection (BKCI)

Interested in publishing with us?
Contact book.department@intechopen.com

Numbers displayed above are based on latest data collected.
For more information visit www.intechopen.com



Inductive Power Transfer for Electric Vehicles Using Gallium Nitride Power Transistors

Cai Qingwei Aaron and Siek Liter

Additional information is available at the end of the chapter

<http://dx.doi.org/10.5772/intechopen.76057>

Abstract

This chapter will present the application of the GaN Gate Injection Transistor (GIT) in Inductive Power Transfer (IPT) for Electric Vehicles (EV). IPT provides significant benefits over conventional plug-in chargers but suffers from lower efficiency. A high frequency inverter using GaN GIT, which has low on-resistance and gate charge, is implemented to reduce switching and conduction loss, resulting in higher efficiency. Different gate drive strategies will be compared for driving the GaN GIT at high slew rates while ensuring cross-conduction protection. The switching characteristics of the GaN GIT are studied and the inverter is designed to ensure low switching losses, while keeping overshoot and slew rates under control. Experiment results presented will demonstrate that the system efficiency peaks at 95% at 100 kHz operation and 92% at 250 kHz operation for a coil gap of 80 mm at 2 kW output power.

Keywords: gallium nitride, enhancement mode, wireless power transfer, inductive power transfer, electric vehicles, wide bandgap semiconductor application, gate driver

1. Introduction

Development of battery technology and advancement of power electronics has allowed EVs to gain popularity in the recent years, with strong boost to greener environment.

From an environmental conservation perspective, EVs demonstrate benefits above conventional Internal Combustion Engines (ICE) vehicles. EVs provide the energy efficient solution to conventional ICE, with energy efficiencies going as high as 62% compared to 21% for internal combustion vehicles. Pollution due to EVs is lesser as it does not produce emission unlike ICE [1].

Another push for in EVs is the performance benefits. Electric motors have smoother operations and quieter than ICE, while having stronger accelerations, and lesser maintenance [2].

However, there are some battery related challenges facing EVs. Due to limited charge holding capacity of Li-ion batteries, the driving range of EVs are limited compared to ICE vehicles, being able to only travel one-third or half the distance of an ICE vehicle [2]. In addition, the battery charging time is time consuming, with a full charge taking about 4–8 h and fast charge about 30 min compared to 5 min for an ICE vehicle [3]. Despite having higher charge carrying capacity compared to other battery materials, Li-ion batteries for EVs are still very big and bulky. They are expensive and need replacement during the car's lifetime [3, 4].

Inductive Power Transfer (IPT) is the method of wirelessly transferring power. The system for static wireless charging is as shown in **Figure 1**. AC power is drawn from the grid into the system. This power is rectified using a diode bridge to supply a DC voltage. This is followed by a Power Factor Correction (PFC) stage to improve the power factor and step up the voltage to 380 V. The DC input voltage is supplied into an inverter, which converts it in high frequency AC so that power can be transmitted by primary coil to the secondary coil using IPT. The secondary coil will take in the HF AC power and rectify it using the SiC diode bridge into a DC voltage for vehicle charging. IPT for EVs provide a convenience and safety for the user [5, 6]. This system is weatherproof and difficult to vandalism like a plug-in station [4].

However, there are challenges facing wireless charging, such as low efficiency compared to plug-in chargers [4]. This is overcome by using wide bandgap semiconductor materials such as GaN, which is attracting attention for enabling high efficiency, high power density converters [7], rectifiers [8] and inverters [9, 10]. The material properties of GaN such as high critical field, electron mobility and saturation velocity [11] push the boundaries of power electronics performance such as efficiency, power density, reliability and cost [12].

The remainder of the chapter is organized as follows. Section 2 will compare various gate driving methods for driving the GaN GIT. This is followed by Section 3 which will explain the design considerations for apply the GaN GIT in WPT applications. Finally, Section 4 contains experiment results that demonstrate the advantages of using GaN in IPT.

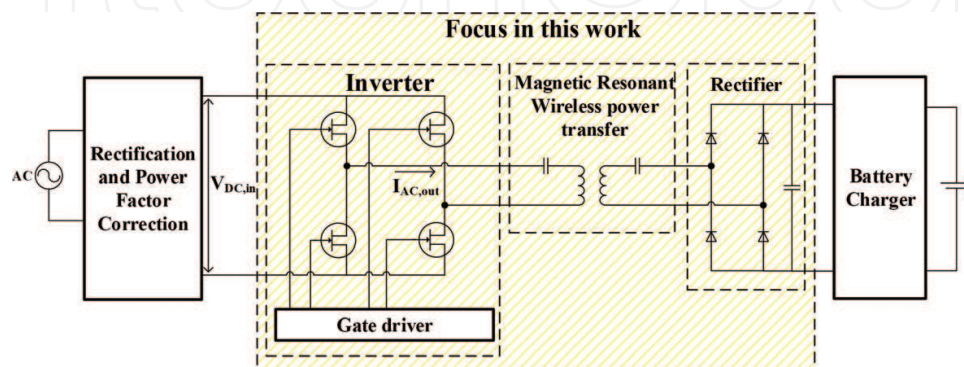


Figure 1. Static wireless charging.

2. Comparing gate drive methods for driving GaN GIT

Among the various enhancement mode GaN, Gate Injection Transistor (GIT) is one such technology, which is able to achieve normally off operation and high current driving capability [13]. The GaN GIT adopts p-GaN with recessed gate to achieve normally-off. The Hybrid Drain embedded in the GIT (HD-GIT) allows the device to overcome the current collapse [14].

Since the GaN GIT is a normally-off device, it can be driven by conventional gate drive methods like the R-type gate drive is shown in **Figure 2a**. Resistor RA1 facilitates the charging during turn on, while the path along RA2 forms the discharge path during turn off.

To capitalize on the switching performance of the GaN device, the RC-type gate drive method [15] is recommended. This gate drive strategy allows the driving of the GaN GIT's gate at a higher voltage allowing faster slew rate. It produces negative gate voltage during turn off to prevent false turn-on, while using a unipolar supply voltage.

A single channel GaN GIT gate driver Integrated Circuit (IC) (AN34092B) utilizes a novel gate drive strategy to compare against existing gate drive methods is shown in [16]. The simplified gate drive circuit for the GaN GIT gate driver IC, AN34092B [17], is shown in **Figure 3a**. The gate driver IC has 3 output pins, namely OUT1, OUT2 and OUT3. OUT1's purpose is to charge the GaN power transistor during turn ON phase and discharging the speed-up capacitor C1 during turn off. When the device is fully turned on, C1 will block current through OUT1.

OUT2 will continue to supply an adjustable DC current of 2.5–25 mA during conduction phase. Integrated within the IC is an adjustable current source, which is able to provide a constant current during turn ON, that is important for the conductivity modulation of the GaN GIT. It also provides a low impedance path using the active miller clamp function.

OUT3 is responsible for the discharge path by pulling the gate to the negative voltage VEE. The turn off slew rate can be controlled using resistor R2. Another integrated function is a charge pump to provide the negative voltage, VEE, during turn OFF, which is adjustable using an external resistor.

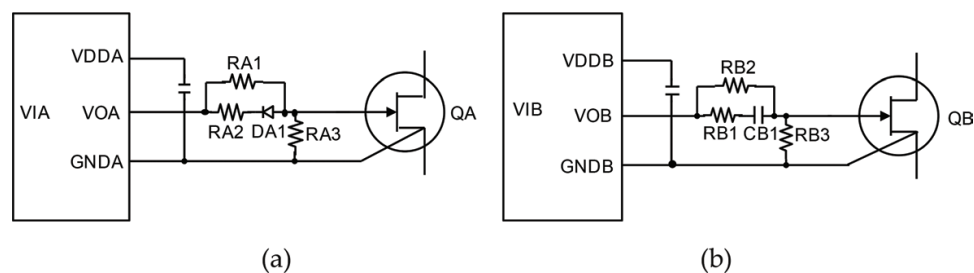


Figure 2. Various gate drive methods: (a) the R-type and (b) the RC-type.

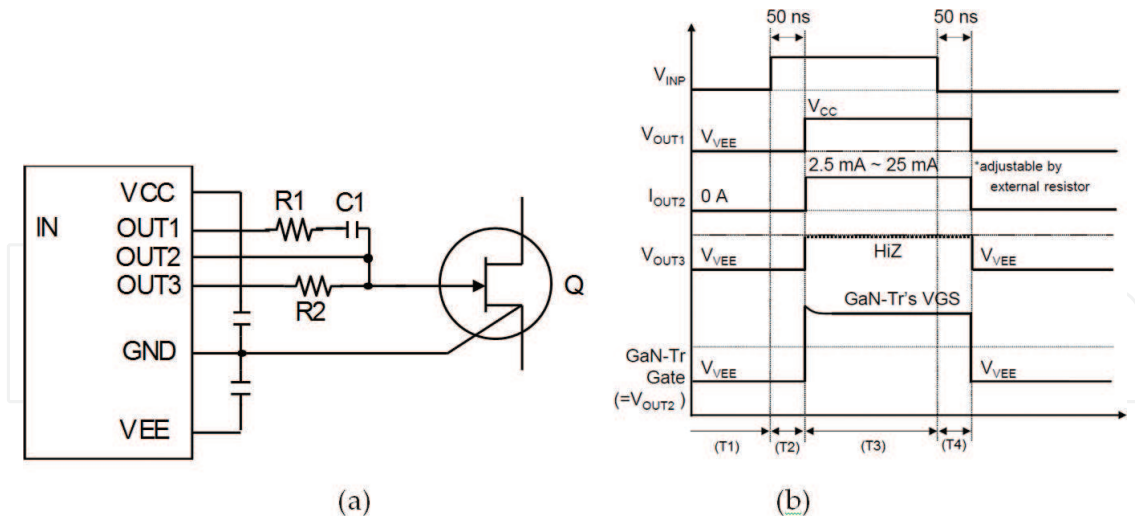


Figure 3. (a) GaN GIT gate driver IC circuit and (b) gate driver timing diagram.

2.1. High slew rate gate drive

Power density and efficiency are important metrics in power electronics. High slew rates allow high operating frequencies, which lead to higher power density due to smaller passive components. In addition, higher slew rates result in an improvement in the switching losses which result in higher efficiency.

The general equation of V_{DS} turn-on and turn-off slew rate is shown in Eqs. (1) and (2) respectively. The fall and rise in the drain-source voltage, V_{DS} , occurs during the charging and discharging of the gate-drain charge, Q_{GD} , at the plateau voltage, V_{pl} . The ability to charge and discharge faster means higher slew rates for the power device.

$$\frac{dV_{DS}}{dT_{turn\ on}} = \frac{I_{GS} \times V_{Power\ supply}}{Q_{GD}} = \frac{(V_{DD} - V_{pl}) \times V_{Power\ supply}}{R_{gate} \times Q_{GD}} \tag{1}$$

$$\frac{dV_{DS}}{dT_{turn\ off}} = \frac{I_{GS} \times V_{Power\ supply}}{Q_{GD}} = \frac{(V_{EE} - V_{pl}) \times V_{Power\ supply}}{R_{gate} \times Q_{GD}} \tag{2}$$

Based on Eqs. (1) and (2), slew rates can be improved by controlling gate current or using a device with a small Q_{GD} . The high breakdown electric field of GaN material allows the GaN GIT to have smaller die size compared to Si power MOSFETs of similar breakdown voltage, which results in smaller parasitic capacitance and correspondingly smaller Q_{GD} . To control the charging and discharging of gate current, one can choose to control the value of the gate resistor or adjust the gate driver source and sink voltage.

2.1.1. Turn-on: dual current source paths for gate protection

To protect the GaN GIT's gate from damage, it is important to keep the gate pulse current and gate pulse charge below the absolute limit. However, controlling the turn-on gate current source through a single path like the R-type gate drive method limits the peak gate current,

which is responsible for high slew rate performance. On the other hand, the GaN GIT driver IC and RC-type gate drive provide two current paths, a high current path during turn-on transients for high slew rate performance and a low current path to keep the GaN GIT in conduction. This is to prevent damaging the gate.

The high current source path of the GaN GIT driver IC and RC-type gate driver comprises a resistor in series with a capacitor. When the power device is fully turned on, the capacitor will block current flow, protecting the gate of the GaN GIT. This allows the GaN GIT driver IC and RC-type gate driver to drive the GaN GIT at a higher supply voltage, resulting in a higher gate current and larger turn-on slew rate. This is supported by Eq. (1), which shows that a higher VDD increases slew rate.

2.1.2. Turn-on: discharging speed-up capacitor to improve turn-on slew rate

For RC circuit, turn-on slew rate is affected by negative voltage of the speed-up capacitor, CB1 on **Figure 2b**. The residue voltage in the capacitor CB1 will reduce the VDDDB voltage used to charge the power device. The GaN GIT driver IC resolves this problem with a high speed discharge circuit to discharge C1. So when the gate driver charges the power device during, it is able to charge the GaN GIT gate from the full VDDDB rail.

2.1.3. Turn-off: negative voltage

The GaN GIT driver IC and RC type gate drive generates a negative voltage turn-off. The RC-type gate driver relies on the connection of the speed-up capacitor, CB1, to create a negative voltage during turn off. With reference to **Figure 1b**, during turn-on transition, the capacitor CB1 is charged up such that the left hand side is positive relative to the right hand side of CB1. During turn-off, the positive side of CB1 is connected to ground, GNDB, which presents a negative voltage at the gate. This negative voltage slowly decays as it is discharged through RB1 and RB2.

On the other hand, the GaN GIT driver IC has a built in charge pump to generate an adjustable negative rail, VEE, from -3 to -5 V. According to Eq. (2), negative voltage turn-off allows larger gate discharging current leading to larger turn-off slew rates compared to R-type gate drive circuits, which discharge at 0 V.

2.2. Cross conduction protection

Cross conduction is a false turn-on mechanism that occurs when the high side device is turned on during dead time. When the high side device is turned on, the drain of the low side power transistor is pulled up, inducing a current across the gate-drain capacitor of the low side power device. This current causes a voltage across the gate-source pin of the power device as it flows through the gate resistor. Research showed slew rates and gate resistance [18] affects the induced gate voltage. For high slew rate power devices, these are practical challenges which need to be addressed. This work aims to reduce VGS spike voltage without sacrificing slew rate performance. There are various countermeasures to reduce the effects of cross conduction.

2.2.1. Low gate impedance

A common countermeasure using the R-type gate drive for cross conduction protection is to implement a low impedance discharge path through the Schottky barrier diode (DA1) in series with a small resistor (RA2) as shown in **Figure 1a**. During the turn off, this forms a very low impedance path, which sinks the induced current to GND. In this method, the slew rate is dependent on the cross conduction protection.

Unlike the R-type gate drive, which has only one output to sink the gate current, the GaN GIT driver IC has 2 gate sink paths. One path (OUT3) to control the GaN GIT gate discharge current to control the slew rate and another path (OUT2) for active miller clamp function, which implements low gate impedance during the cross conduction period and reduces gate ringing. This unique function allows slew rate control independent of the active miller clamp protection function.

2.2.2. Negative voltage

Implementing a negative gate-source voltage during turn off creates a voltage buffer between V_{CS} and V_{th} to prevent the GaN GIT from turning on when cross conduction occurs. The RC-type gate drive creates a negative voltage across the VGS during turn-off due to the change in polarity of the speed up capacitor CB1. On the other hand, the GaN GIT driver IC has built-in negative voltage rail to create this voltage buffer. These two methods are able to create a negative voltage rail with a unipolar voltage supply, which reduce cost.

2.3. Experiment results of gate drive methods

2.3.1. Experiment setup

The driving methods are tested using a half bridge configuration based on **Figures 2** and **3a** as shown below in **Table 1**. The evaluation was conducted using 600 V, 10A SMD GaN GIT. R-type and RC-type gate drive were tested using SWEVB005-PGA26E19BA half bridge evaluation board (**Figure 4a**), while the GaN GIT gate driver IC (AN34092B) was tested using SWEVB008-PGA26E19BA half bridge evaluation board (**Figure 4b**). The purpose is to keep the parasitic inductance of the gate drive loop and power loop similar across the three evaluation setups.

	VDD (V)	$V_{Negative}$	Component 1	Component 2	Component 3
R-type gate drive	5	Nil	RA1 = 51 Ω	RA2 = 1 Ω	DA1 = SBD
RC-type gate drive	12	-5 V	RB1 = 51 Ω	RB2 = 2700 Ω	CB1 = 1.2 nF
GaN GIT gate driver IC	12	-5 V	R1 = 51 Ω	R2 = 1 Ω	C1 = 120 pF

Table 1. Design parameters and values for experiment.

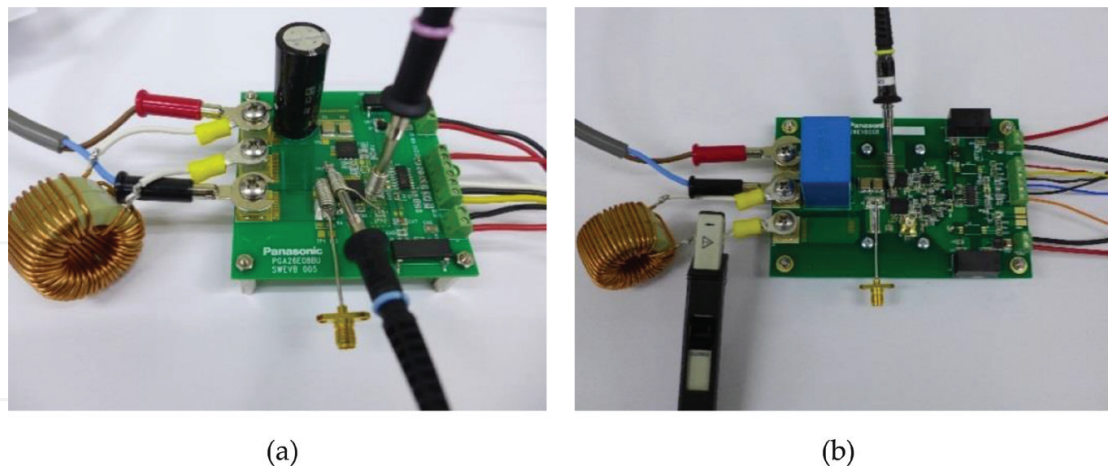


Figure 4. Experiment setup for (a) R-type and RC-type gate drive method and (b) GaN GIT gate driver IC.

Double pulse test was conducted with an inductive load and bus voltage of 400 V. It is tested for load currents at 2.5, 5, 7.5 and 10A. Since it is a half bridge circuit, the slew rates for the low side and high side GaN GIT are measured. The gate-source voltage of the low side is probed during high side test to study the cross conduction protection.

2.3.2. Slew rates results

The waveforms are taken at $I_{DS} = 10A$ and $V_{DS} = 400 V$. The results for the V_{DS} turn-on and turn-off slew rate were measured from 10 to 90% and waveforms are shown in **Figure 5**. From **Figure 5**, it is observed that the V_{GS} is charged up slower for the R-type gate drive (**Figure 5a**) compared to the RC-type (**Figure 5b**) and GaN GIT gate driver (**Figure 5c**). This is because the RC-type and GaN GIT gate driver charge the gate up with $VDD = 12 V$, allowing more charge to be supplied compared to the R-type gate drive which have $VDD = 5 V$ supply. Thus, results in a faster VDS slew rate.

With reference to **Figure 5**, it shows that VGS for the R-type gate drive (**Figure 5d**) is turned off at 0 V, while the RC-type (**Figure 5e**) and GaN GIT gate driver (**Figure 5f**) are turned off with a negative voltage. The negative voltage of the RC-type circuit is decaying to 0 V as the capacitor discharges while the GaN GIT gate driver is held at $-5 V$ until the next turn on cycle.

The results for the low side slew rates are shown in **Figure 6**, which illustrate the turn-on (**Figure 6a**) and turn-off (**Figure 6b**) slew rates. From **Figure 6a**, the GaN GIT has the highest turn-on slew rate (97 V/ns) followed by the RC-type (48 V/ns) and finally the R-type (26 V/ns). The gate drive resistor value, which is critical for turn-on slew rate, is fixed at 51Ω for all three setups to make a fair comparison with the other gate drive methods.

The RC-type and GaN GIT driver are clearly faster than R-type because they are driven at 12 V. GaN GIT driver is faster than the RC-type gate drive because of the discharging speed-up capacitor function and the choice of a smaller speed-up capacitor ($C1 = 120 pF$ vs. $CB1 = 1.2 nF$). The reason for the larger capacitor for the RC-type gate drive is to increase the RC time constant to slow down the decay of the negative turn-off voltage.

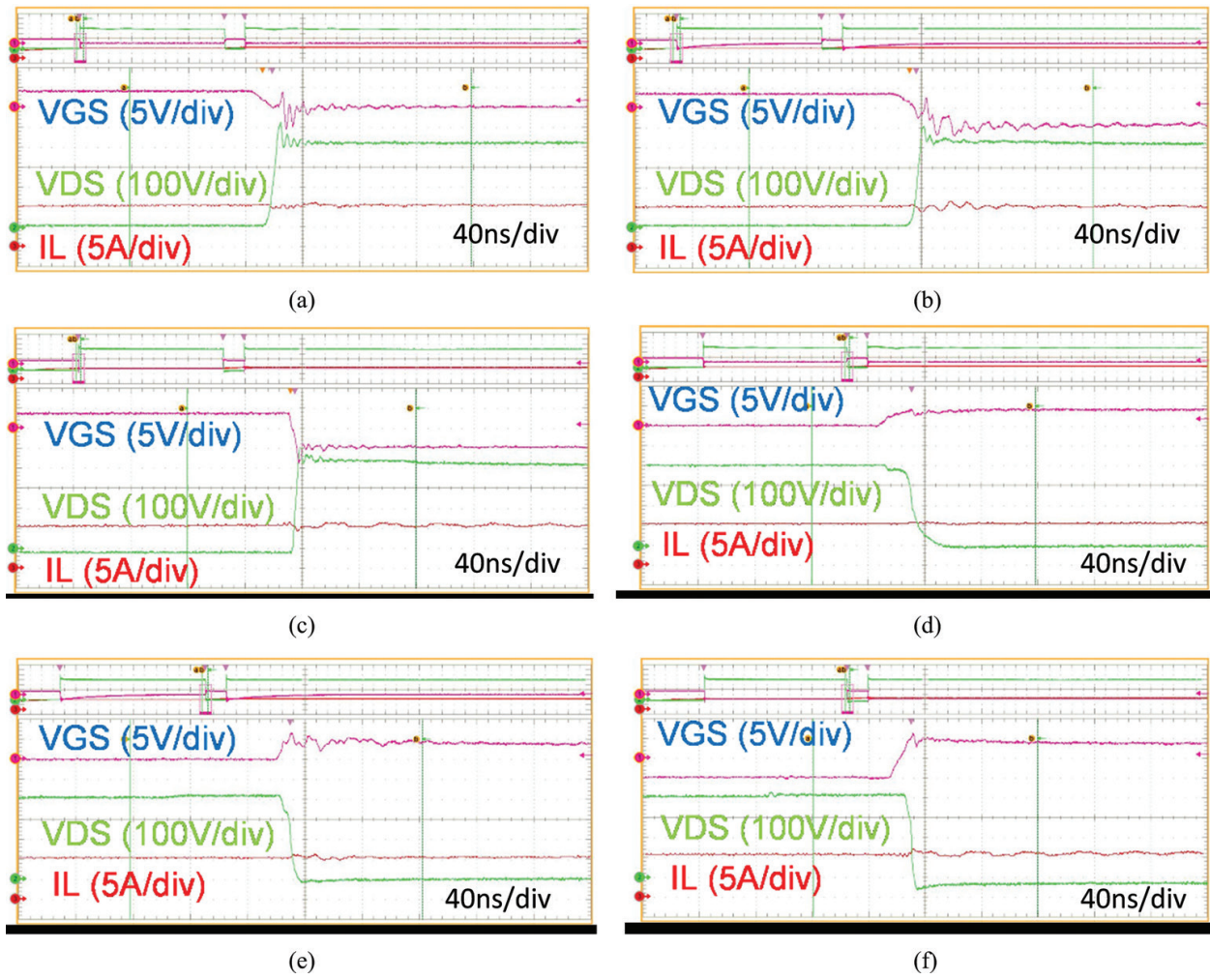


Figure 5. Double pulse waveform for (a) R-type, (b) RC-type and (c) GaN GIT gate driver during turn-off and for (d) R-type, (e) RC-type and (f) GaN GIT gate driver during turn-on.

The turn-off slew rate results is depicted in Figure 6b. From the graph, it is shown that slew rate for RC-type and R-type are close, while GaN GIT driver IC outperforms them to achieve

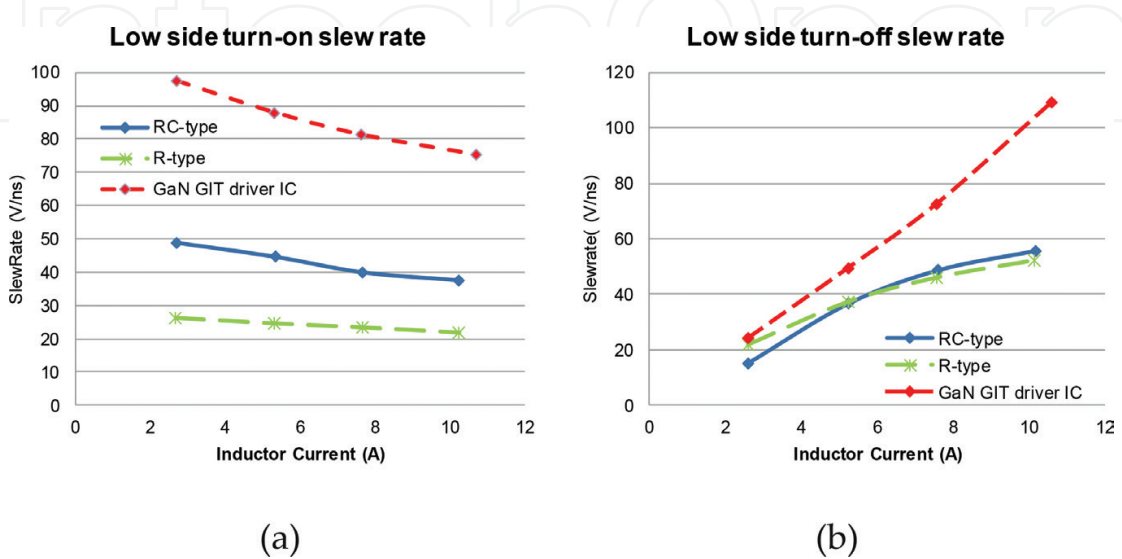


Figure 6. Slew rate measurement results for (a) low side turn-on and (b) low side turn-off.

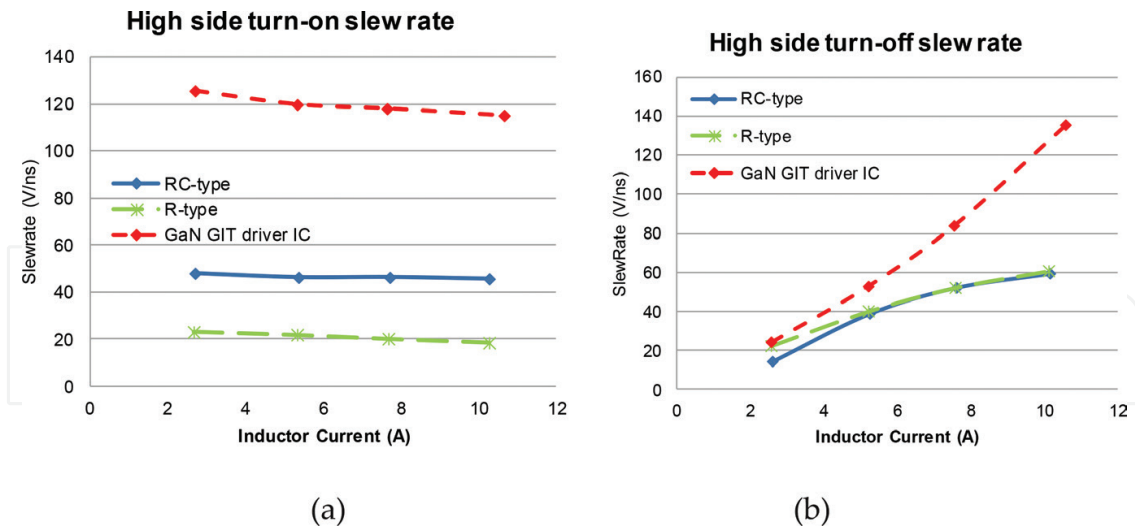


Figure 7. Slew rate measurement results for (a) high side turn-on and (b) high side turn-off.

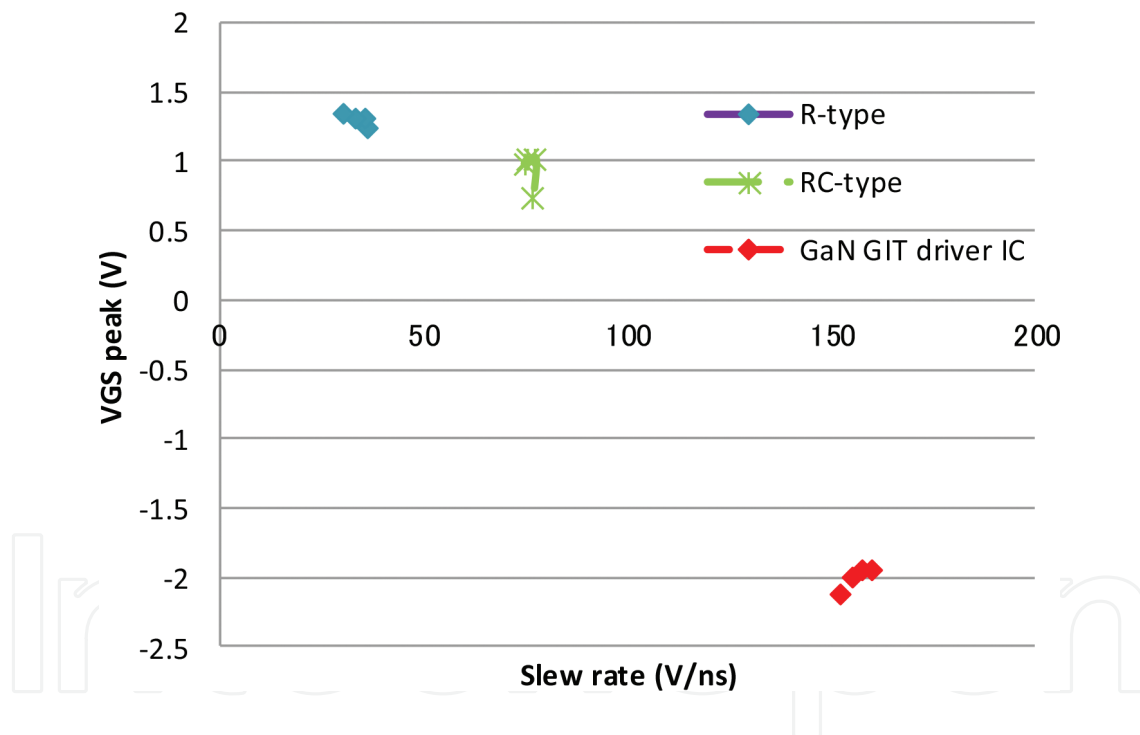


Figure 8. Cross conduction test.

a maximum slew rate of 110 V/ns. While both RC-type and GaN GIT driver IC discharges the gate with negative voltage, the RC-gate drive method has a larger discharge resistance resulting in a slower turn-off slew rate. The R-type gate drive has a low resistance to GND, but discharges to GND instead to a negative voltage. The GaN GIT driver IC capitalizes on low impedance from gate to VEE and a negative voltage to achieve twice the slew rate.

The high side slew rate is shown in Figure 7. Results are very similar to the low side results in Figure 6, except that the high side results are slightly faster. This is because of the probe capacitance loading on the VGS and VDS pin during low side test that slow down the slew rate measurement results.

2.3.3. Cross conduction protection

The low side VGS spike voltage occurs when high side is turned on is measured and plotted against the slew rates (according to **Figure 7a**) and shown in **Figure 8**. From the results, it shows that the GaN GIT gate driver has the lowest VGS spike voltage, despite higher slew rate operation than the other two methods. All three methods managed to keep this spike voltage below the threshold voltage of the GaN GIT.

3. Switching loss evaluation and gate drive optimization for IPT in EV system

3.1. Power device selection

A common Figure of Merit (FOM) adopted by power semiconductor devices is $R_{on}Q_g$. This FOM accounts for the switching and conduction loss such that the lower the FOM, the better the performance. This is a representative of the technology [19]. A comparison of FOM among three state-of-the-art transistors using GaN, SiC and Si are compared and shown in **Table 2**.

GaN GIT has the lowest FOM due to the high critical field of GaN and the High Electron Mobility Transistor (HEMT) structure. The Si vertical MOSFET performs the worst with the highest FOM. This is followed by SiC MOSFETs which perform an order of magnitude better. It is shown that Si Super Junction MOSFETs being able to outperform SiC MOSFETs for $R_{on}Q_g$. This is because the Super Junction technology is able to push beyond the theoretical limits of Si.

3.2. Half bridge circuit loss modeling

The total losses in a half bridge circuit contains conduction loss, switching loss, ringing loss and dead time loss of the top and bottom power device and is shown in Eq. (3). The subscript top and bot respectively denote the top and bottom power device.

Material	GaN	Si	Si	SiC	SiC
Technology	Gate Injection Transistor	MOSFET	Super Junction MOSFET	MOSFET	MOSFET
Breakdown voltage (V)	600	600	700	650	1200
Rated current (A)	15	6	18	29	40
R_{on} (m Ω)	65	1000	125	120	80
Q_g (nC)	11	33	35	61	106
$R_{on}Q_g$ (n Ω C)	0.715	33	4.38	7.32	8.48

Table 2. FOM comparison between semiconductor devices.

The total conduction loss is shown in Eq. (4) and is influenced by the on-resistance, R_{on} of the device and application requirements such as drain-source current, I_{DS} and duty, D . Switching loss, on the other hand, is frequency dependent as shown in Eq. (5). It is affected by the drain-source voltage, V_{DS} and current during the turn on (t_{on}) and turn off (t_{off}) switching transition. This shows the need for soft switching or fast slew rates for hard switching applications to reduce switching losses.

The ringing loss is obtained from [20] and modified for GaN GIT as shown in Eq. (6). GaN GIT does not have Q_{rr} but still has to discharge drain-source capacitor, C_{DS} which is represented by the drain source charge, Q_{oss} . Ringing losses are proportionate to frequency and DC-link voltages, V_{bulk} . The turn on ringing loss are affected by the Q_{oss} , while the turn off losses are affected by charges, Q_{Vpeak} due to the peak ringing voltage V_{peak} . High slew rates and parasitic source drain inductances increase the peak voltage.

The absence of reverse recovery diode implies that dead time, t_{SD} can be reduced. However, the GaN device will still experience a dead time loss according to Eq. (7). When a reverse current I_{SD} flows through the device, it will have a voltage drop, V_{SD} during dead time that results in dead time loss.

$$P_{HB\ loss} = P_{cond\ loss} + P_{sw\ loss} + P_{ringing} + P_{dead\ time} \quad (3)$$

$$P_{top\&bot,cond\ loss} = I_{DS}^2 R_{on,top} D + I_{DS}^2 R_{on,bot} (1 - D) \quad (4)$$

$$P_{sw,on\&off} = \frac{1}{2} f V_{DS} I_{DS} (t_{on,top} + t_{off,top} + t_{on,bot} + t_{off,bot}) \quad (5)$$

$$P_{ringing} = V_{bulk} f (Q_{oss,top} + \frac{1}{2} Q_{oss,bot}) + \frac{1}{2} f (Q_{Vpeak} (V_{peak} - 2 V_{bulk}) + Q_{Vin} V_{bulk}) \quad (6)$$

$$P_{dead\ time} = V_{SD} \times I_{SD} \times t_{SD} \times f \quad (7)$$

3.3. Experimental results and GaN GIT gate driver optimization

Double pulse switching characteristic test, using an inductive load circuit shown in **Figure 9**, is conducted to evaluate the performance of the GaN GIT under EV wireless charging conditions. The GaN GIT is evaluated based on the specifications of the design. The drain-source parameters of the device is tested based on a DC-link voltage of 400 V, with load current varying from 2.5 to 15A. The gate drive voltage is set at 12 V. The value of drain-source voltage/current overshoot, drain-source voltage slew rate and switching losses energy will be measured. The gate drive resistor R1 will be varied from 5.1 to 36 Ω . **Figure 10** shows the waveforms at 400 V and 10A using R1 = 10 Ω .

Parasitic inductance in the gate drive loop should be small to improve the slew rate of the GaN device. One should consider reduction of the source and drain inductances along the

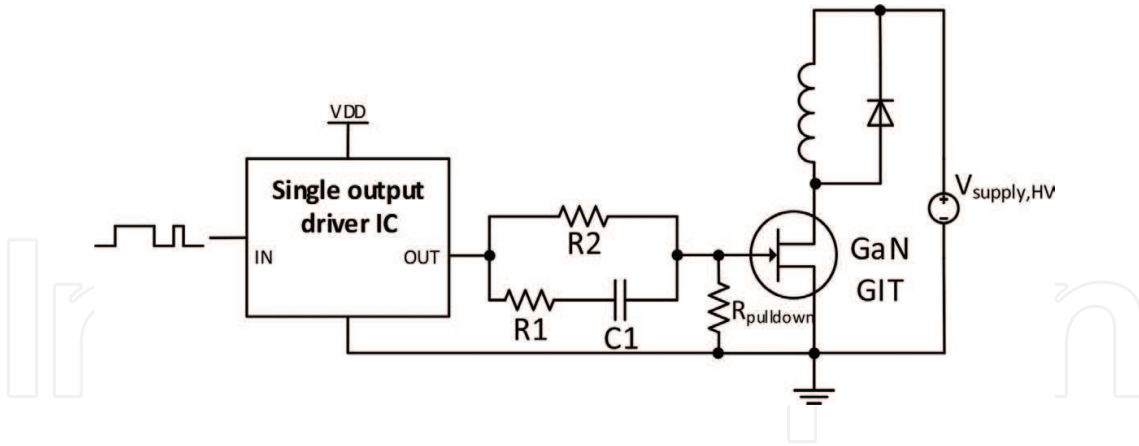


Figure 9. Experimental setup for inductive load circuit for double pulse test.

power loop to reduce the V_{DS} ringing. For realistic results, adopt a freewheeling diode that have a similar reverse recovery charge to the GaN GIT's reverse conduction Q_{DS} .

The turn-off and turn-on switching loss energy per cycle is shown in Figure 11. Reducing the gate drive resistor, R_1 , results in higher gate current, reducing rise and fall time and thus reducing switching losses. As load current increases, the switching loss also increase. These two observations agree with Eq. (5).

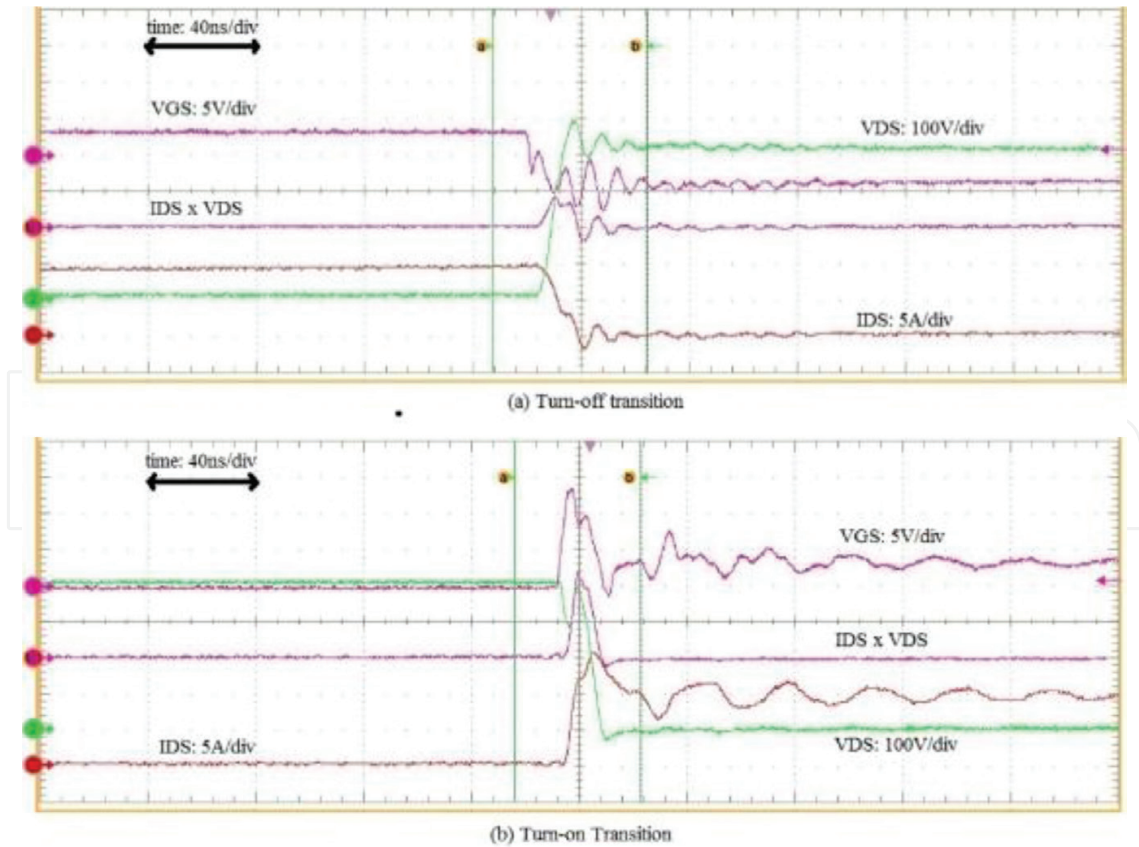


Figure 10. Switching experimental results of 2-pulse test results: (a) turn-off transition for TO-220 GaN GIT and (b) turn-on transition for TO-220 GaN GIT.

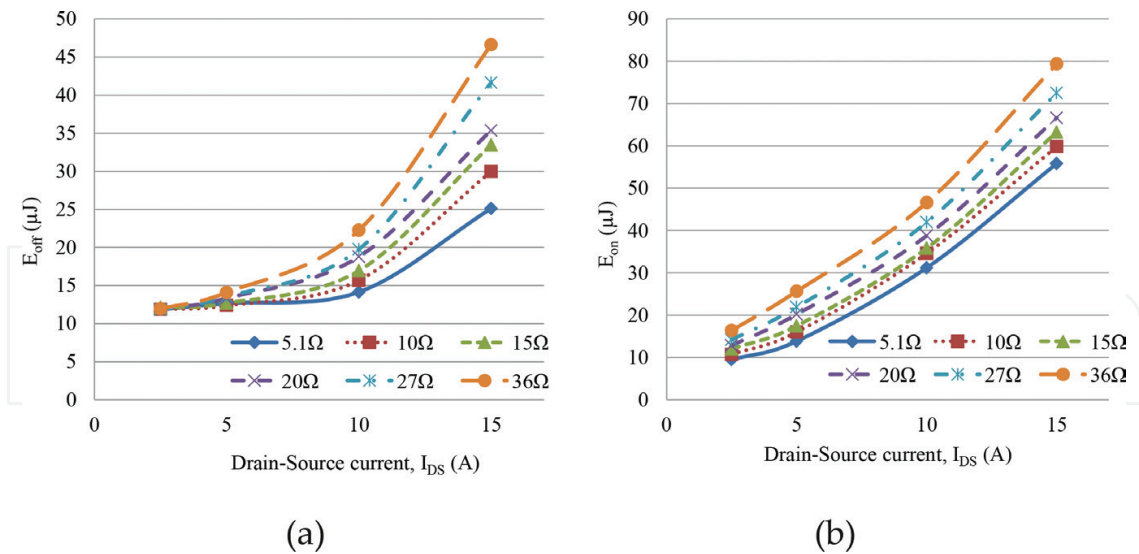


Figure 11. Evaluation results for switching energy per cycle: (a) turn-off switching energy and (b) turn-on switching energy.

The second factor for consideration is the drain-source voltage overshoot. **Figure 12a** and **b** shows the turn-off voltage peak and turn-on current peak respectively, with variation in the load current and the gate drive resistor. Voltage and current overshoot is directly proportional to load current. Reduction in the gate drive resistance increases the overshoot. From the evaluation results, it shows that the observed overshoot is below the absolute voltage and current rating and hence the device is safe.

Finally, we will evaluate the slew rate results in **Figure 13**. **Figure 13a** illustrates the slew rate during the turn off transition. The slew rate increases as the gate drive resistance is reduced and achieves a maximum slew rate of 67 V/ns at 5 Ω. This work utilizes the GaN GIT with TO-220 package which has higher parasitic inductance compared to surface mount packages, resulting in slower slew rates.

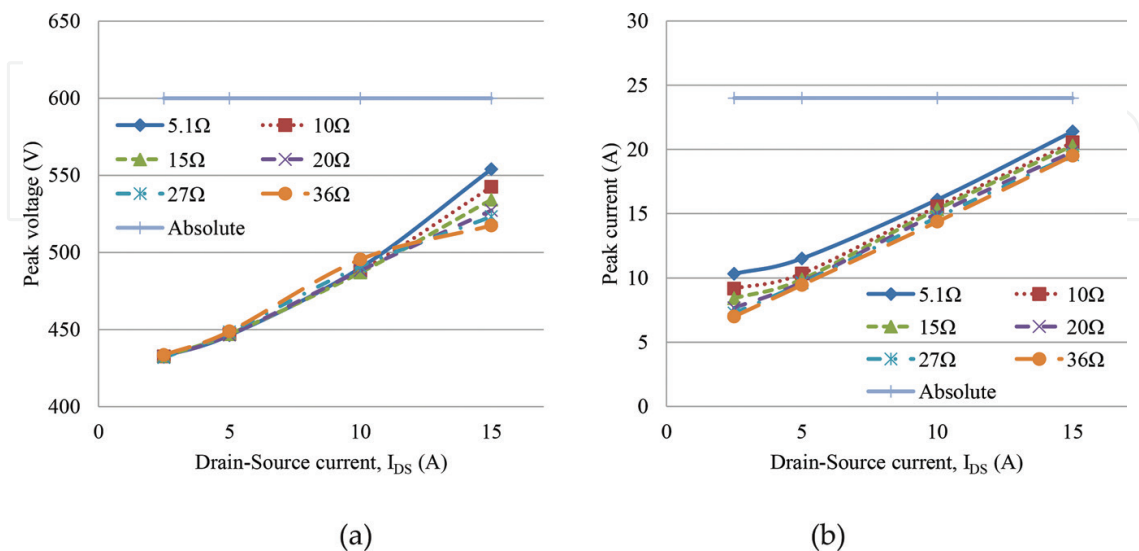


Figure 12. Evaluation results for overshoot: (a) drain source voltage peak vs. absolute rating and (b) drain source current peak vs. absolute rating.

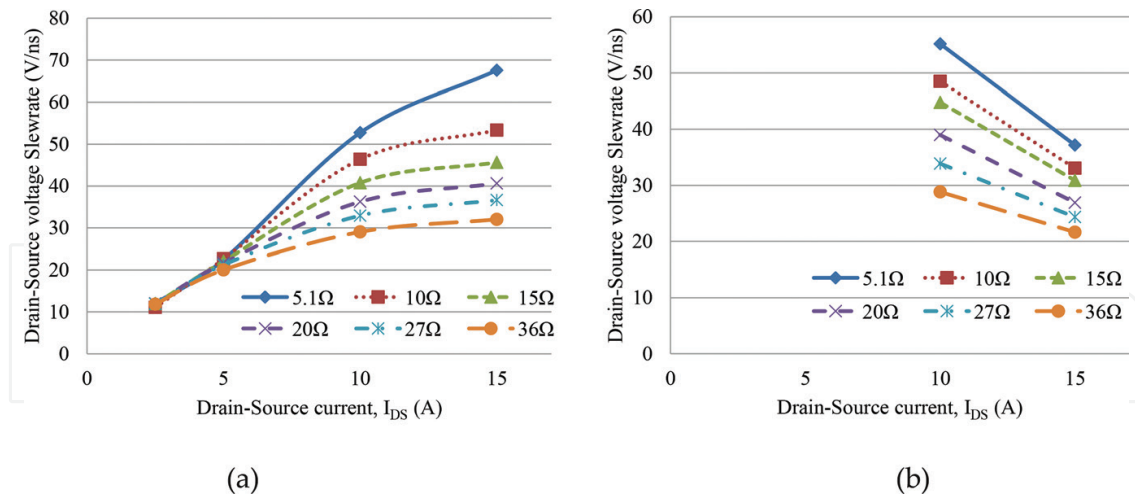


Figure 13. Evaluation results for slew rate: (a) VDS slew rate during turn-off transition and (b) VDS slew rate during turn-on transition.

Figure 13b shows the turn on slew rate. Lower gate drive resistance causes higher slew rates while slew rates drop as load current increases. Due to parasitic inductance within the TO-220 package, a voltage drop is observed across the drain to source nodes when drain source current flows through it, affecting the slew rate measurement of V_{DS} at low load (2.5 and 5A condition). Therefore, only higher load conditions (10 and 15A) are shown.

Based on the evaluation data, the choice of R1 should ensure low total switching energy and peak drain-source voltage. Although the 5 Ω results performed better, it has a slew rate above 50 V/ns. During the design, there were not many isolated half bridge gate drivers, which can handle high slew rate operations, characterized by the parameter called common mode transient immunity (CMTI). The highest CMTI was from ADuM3223 at 50 V/ns. Therefore, while 5 Ω had better evaluation results, we chose 10 Ω so that it can function within the limits of our isolated gate driver.

4. Experiment results of inductive power transfer system

The hardware for the solution is shown in **Figure 14**, comprising of a high frequency inverter, a pair of magnetically coupled coils, a high frequency rectifier on the secondary side and a resistor bank acting as a load. The system is tested from 80 to 150 mm. The input voltage to the inverter is 370VDC, which is the typical output voltage from the PFC stage. In order to ensure the inverter output current is below the current rating of the GaN GIT, the resistor load is set to 47 Ω at 80 mm and 11.5 Ω at 150 mm. This is because variation in coil gap affects the mutual inductance and hence affects the reflected load from the secondary side to the primary side.

The system efficiency from 80 to 150 mm is shown in **Figure 15**. The highest efficiency is obtained at 80 mm at 2.1 kW. As the coil gap increases, the efficiency falls as shown with the peak efficiency occurring at 90.4% at 150 mm. The reason for testing at 150 mm up to 1.5 kW is to operate the inverter below the absolute current limit of the 15A GaN GIT device.

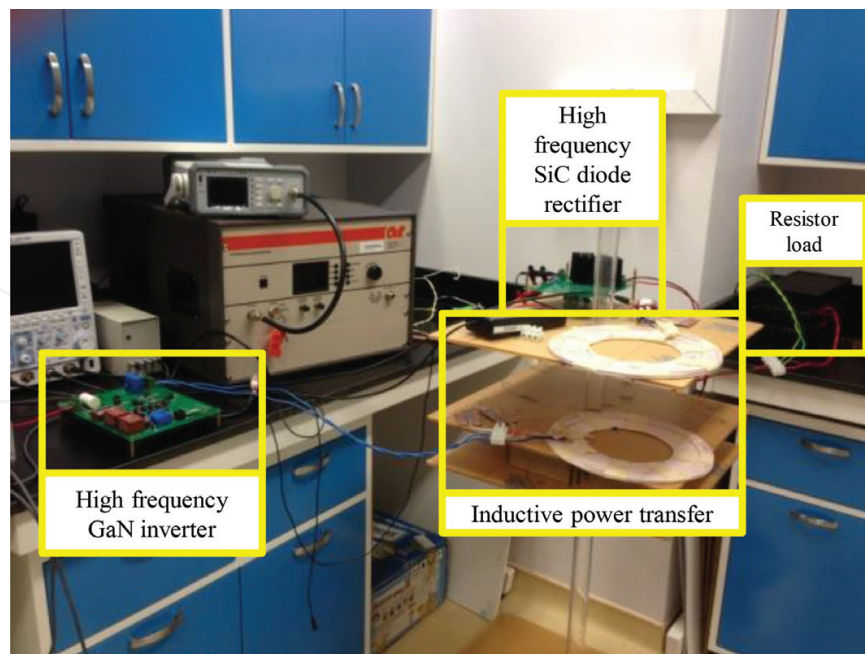


Figure 14. Wireless power transfer experiment setup.

The efficiency breakdowns of each individual stages at 150 and 80 mm are shown in **Figures 16** and **17** respectively. They are tested at an operating frequency 100 kHz. The high frequency inverter maintains its efficiency within the 97–98% region across the varying distances at 2 kW. The coil efficiency falls drastically as the coil gap increases. This is because the increase in distance results in a weaker coupling factor causing a higher secondary current and hence increases the copper loss in the coil. At 80 mm, the efficiency of the rectifier performs well. This is because the SiC diode forward voltage is small relative to output voltage. However, as coil gap increase, the secondary voltage drops, which makes the diode forward voltage loss more significant.

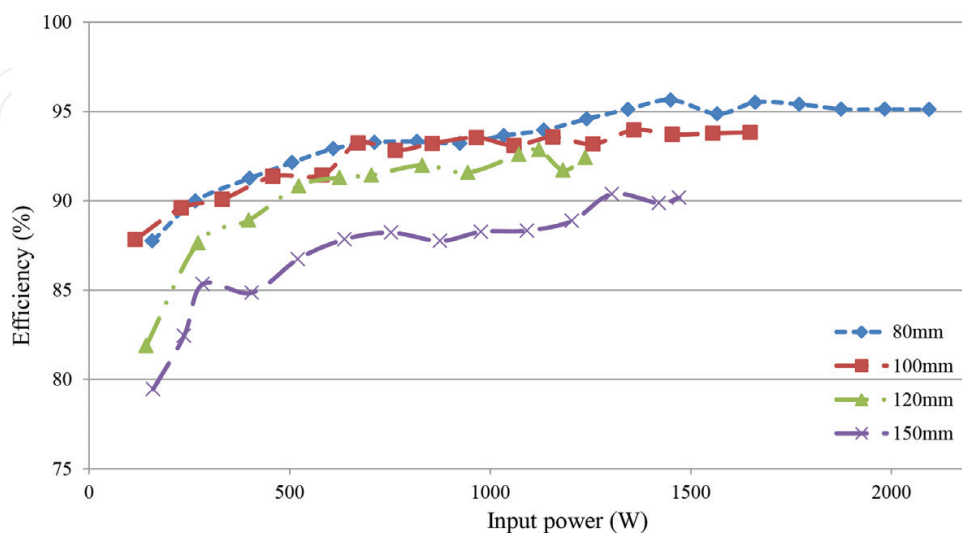


Figure 15. Experimental results: efficiency vs. distance.

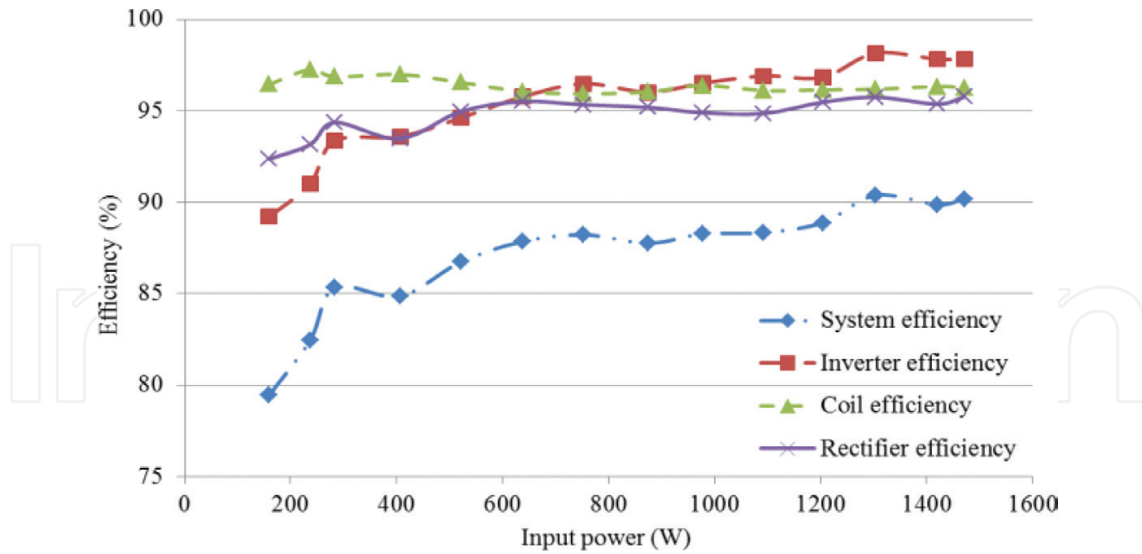


Figure 16. Experimental results: efficiency breakdown at 150 mm.

The waveform of the inverter output current (CH1), inverter output voltage (CH2), IPT output voltage (CH3) and IPT output current (CH4) at 80 mm distance, operating at 100 kHz is shown in Figure 18. The figure shows the zoom out version at 20 μs/div on the top and the zoom in image at 2 μs/div on the bottom.

The next experiment compared efficiencies by varying the operating frequency from 100 kHz to 250 kHz at a 80 mm coil gap, evaluating the system up to 2 kW. Figure 19 illustrates the results and it shows a drop in system efficiency from 95.13 to 91.7% at 2 kW. This efficiency in the inverter fell due to switching losses at higher frequency operation. The IPT coils will experience higher AC resistance due to skin effect as the operating frequency increase by 2.5 times. The rectifier suffers from higher reverse recovery loss at higher frequencies.

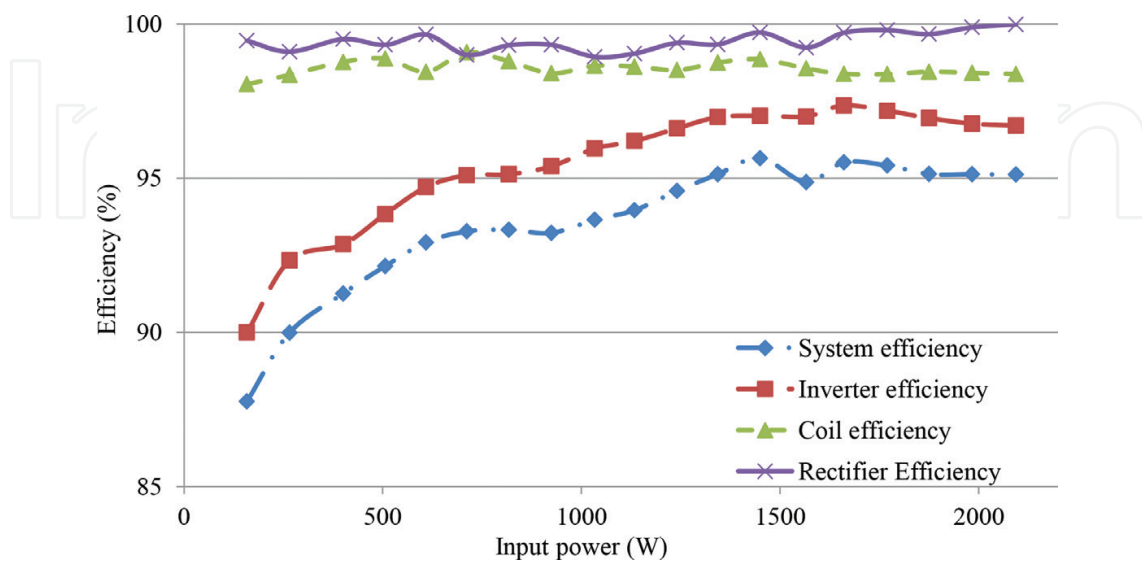


Figure 17. Experimental results: efficiency breakdown at 80 mm.

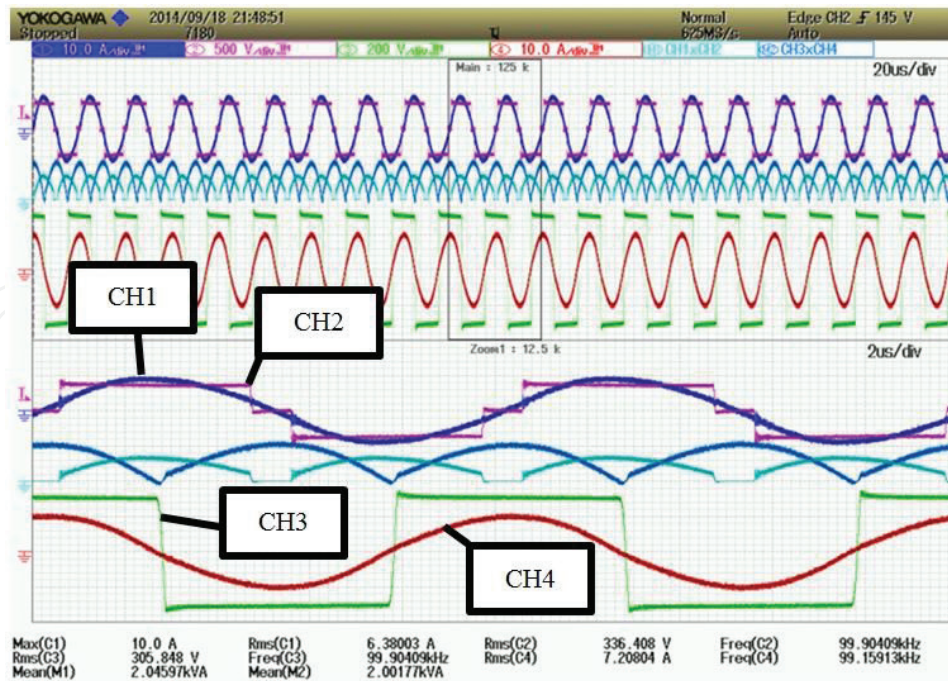


Figure 18. Experimental results of inverter and coil channel 1: inverter output current, channel 2: inverter output voltage, channel 3: IPT output voltage, channel 4: IPT output current.

A similar setup was made using a SiC based high frequency inverter. The efficiency comparison between the GaN based and SiC based system is illustrated in Figure 20. The GaN based system outperformed the SiC based system by 1% at 2 kW, which translates to 20 W less heat dissipated on the inverter. This was because of the lower on-resistance and gate charge of the GaN GIT, resulting in lower conduction and switching loss.

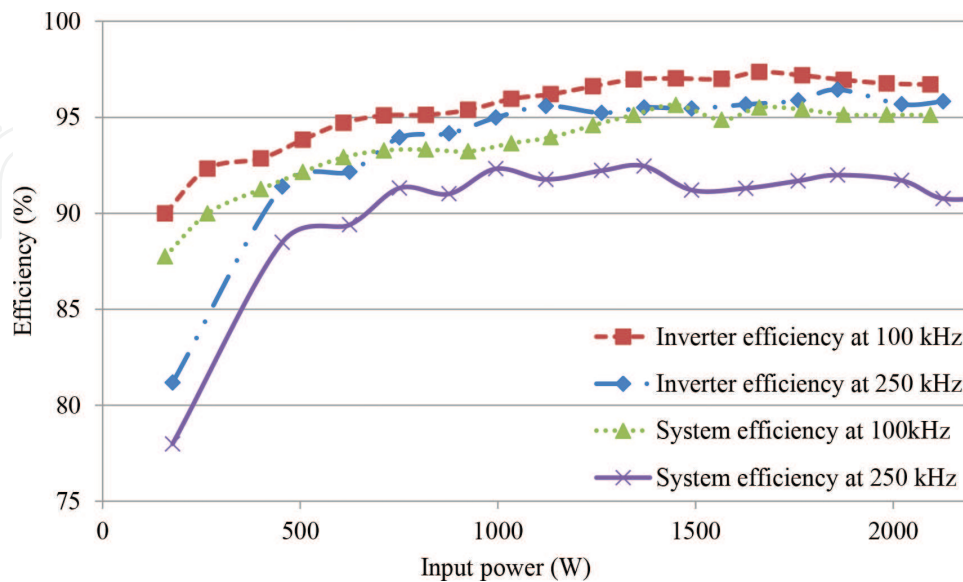


Figure 19. Experimental results: efficiency vs. input power for varying frequencies.

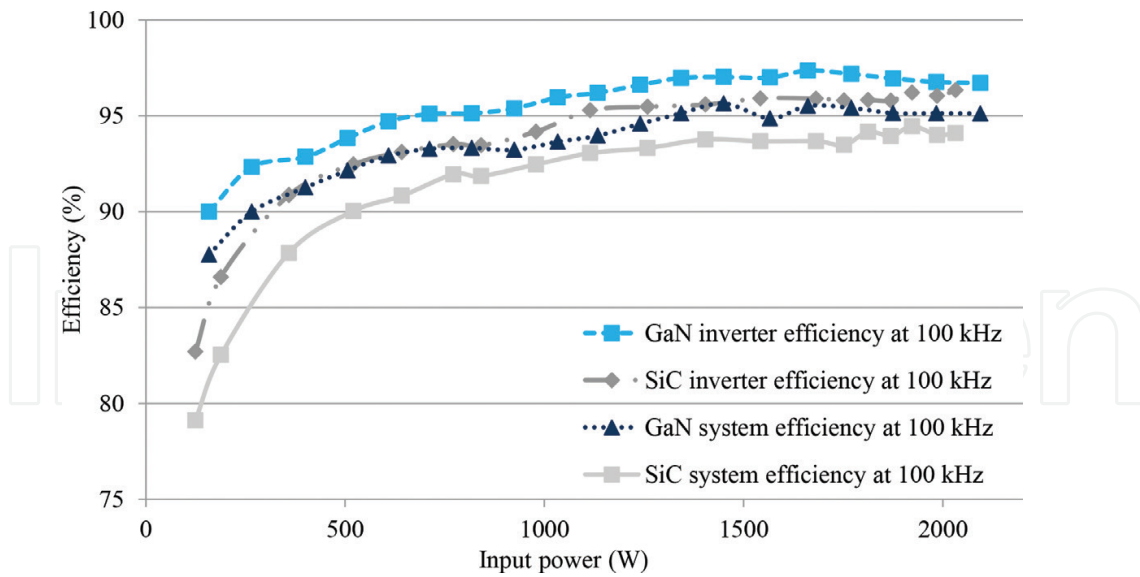


Figure 20. Experimental results: efficiency comparison between GaN and SiC.

5. Conclusion

In this work, a practical high efficiency wireless power transfer system for EV charging application is developed. The GaN GIT introduced is able to provide superior performance and system benefits. Gate drive strategies are introduced with performance evaluation showing that GaN GIT gate driver achieves high slew rate, while still providing protection from cross conduction. Application of GaN GIT is adopted to improve the efficiency of the inverter by optimizing the gate drive circuit. Experimental results prove the efficiency advantage of adopting GaN GIT in high frequency applications such as inductive power transfer for electric vehicle charging.

Acknowledgements

The authors would like to acknowledge the funding support from NTU-A*STAR Silicon Technologies Centre of Excellence (Si-COE) under the program grant No. 11235100003. The authors would like to acknowledge the provision of GaN GIT samples and the financial support from Panasonic Industrial Devices Semiconductor Development Asia (PIDSCDA). The authors are grateful for the financial support provided by the Economic Development Board (EDB) of Singapore. We would like to express our appreciation to Energy Research Institute @ NTU (ERI@N) for providing the facilities and technical support for this project. Finally, the authors would like to express gratitude towards VIRTUS IC design center.

Author details

Cai Qingwei Aaron* and Siek Liter

*Address all correspondence to: aaroncaiqw@gmail.com

Nanyang Technological University, Singapore

References

- [1] Omori H, Iga Y, Morizane T, Kimura N, Nakagawa K, Nakaoka M. A novel wireless EV charger using SiC single-ended quasi-resonant inverter for home use. In: 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC); 4-6 September 2012
- [2] US Department of Energy. All-Electric Vehicles (EVs). US Department of Energy; 08 April 2014. [Online]. Available: <https://www.fueleconomy.gov/feg/evtech.shtml#end-notes>. [Accessed: April 9, 2014]
- [3] Li S, Mi C. Wireless power transfer for electric vehicle applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2015;**3**(1):4-17
- [4] Wu H, Gilchrist A, Sealy K, Bronson D. A 90 percent efficient 5kW inductive charger for EVs. *IEEE Energy Conversion Congress and Exposition (ECCE)*; 15-20 September 2012. pp. 275-282
- [5] Onar OC, Miller JM, Campbell SL, Coomer C, White C, Seiber LE. A novel wireless power transfer for in-motion EV/PHEV charging. In: *Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*; 17-21 March 2013
- [6] Chawla N, Tosunoglu S. State of the art in inductive charging for electronic appliances and its future in transportation. In: *Florida Conference on Recent Advances in Robotics*; Boca Raton. 2012
- [7] Umeda H, Kinoshita Y, Ujita S, Morita T, Tamura S, Ishida M, Ueda T. Highly efficient low-voltage DC-DC converter at 2-5 MHz with high operating current using GaN gate injection transistors. In: *International Exhibition Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management PCIM Europe 2014*; 20-22 May 2014. Nuremberg. pp. 1-8
- [8] Liu Z, Lee FC, Li Q, Yang Y. Design of GaN-based MHz totem-pole PFC rectifier. *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2016;**4**(3):799-807
- [9] Morita T, Tamura S, Anda Y, Ishida M, Uemoto Y, Ueda T, Tanaka T, Ueda D. 99.3% efficiency of three-phase inverter for motor drive using GaN-based Gate Injection Transistors. In: *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*; 6-11 March 2011; Fort Worth. pp. 481-484
- [10] Cai A, Pereira A, Tanzania R, Tan YK, Siek L. A high frequency, high efficiency GaN HFET based inductive power transfer system. In: *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*; Charlotte. 2015. pp. 3094-3100
- [11] Ueda D, Hikita M, Nakazawa S, Nakazawa K, Ishida H, Yanagihara M, Inoue K, Ueda T, Uemoto Y, Tanaka T, Egawa T. Present and future prospects of gan-based power electronics. In: *9th International Conference on Solid-State and Integrated-Circuit Technology*; 20-23 October 2008; Beijing. 2008. pp. 1078-1081
- [12] Kolar JW, Biela J, Waffler S, Friedli T and Badstuebner U. Performance trends and limitations of power electronic systems. In: *6th International Conference on Integrated Power Electronics Systems*; 16-18 March 2010; Nuremberg. 2010. pp. 1-20

- [13] Uemoto Y, Hikita M, Ueno H, Matsuo H, Ishida H, Yanagihara M, Ueda T, Tanaka T, Ueda D. Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation. *IEEE Transactions on Electron Devices*. 2007;**54**(12):3393-3399
- [14] Kaneko S, Kuroda M., Yanagihara M, Ikoshi A, Okita H, Morita T, Tanaka K, Hikita M, Uemoto Y, Takahashi S, Ueda T. Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain. In: *IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*; 10-14 May 2015; Hong Kong. 2015. pp. 41-44
- [15] Morita T, Handa H, Ujita S, Ishida M, Ueda T. 99.3% efficiency of boost-up converter for totem-pole bridge-less PFC using GaN gate injection transistor. In: *Proceedings of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, PCIM Europe*; Nuremberg. 2014
- [16] Cai A, Herreria AC, How SB, Siek L. Gate driver IC for GaN GIT for high slew rate and cross conduction protection. In: *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg; PCIM Europe 2017*. pp. 1537-1544
- [17] Panasonic Semiconductor. GaN Power Devices. [Online]. Available: <http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/#products-document>. [Accessed: January 24, 2017]
- [18] Elbanhawy A. Limiting cross-conduction current in synchronous buck converter designs. Fairchild Semiconductor; 2005
- [19] Christian M, Guillemant O. Simple Design Techniques for Optimizing Efficiency and Over voltage Spike of Synchronous Rectification in DC to DC Converters. Austria: Infineon; 2012
- [20] Ren Y, Xu M, Zhou J, Lee FC. Analytical loss model of power MOSFET. *IEEE Transactions on Power Electronics*. 2006;**21**(2):310-319

IntechOpen