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Porous Silicon

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Abstract

Porous silicon is a sponge-like structure of monocrystalline silicon which although accidentally discovered, soon became one of the most well-researched silicon structures. Its properties and applications have been the main subject of several books and more than a dozen review articles. However, a survey of porous silicon fabrication methods has not been published even though more than 20 different routes have been developed to synthesize this material. This chapter briefly discusses the properties of porous silicon, describes its fabrication methods, and introduces its applications.

Keywords: porous silicon, fabrication, synthesis, preparation method, etching

1. Introduction

Porous silicon, solid silicon with voids therein, is one of the most important porous materials with a wide range of applications from batteries and fuel cells to drug delivery and diagnostics [1–3]. Although optoelectronics, especially light emission, has been porous silicon's primary area of interest for the last 25 years, the material has recently found its way to cosmetics, consumer care, nutrition, and food industry. The preparation of porous silicon is rather simple and inexpensive. It can be performed by several methods depending on the desired structure and properties. It shows highly tunable structural, mechanical, optical, electrical, thermal, emissive, and physiochemical properties. Some of its properties like luminescence and medical biodegradability are direct consequences of nanoscale porosification and are not observed in bulk silicon.

2. Properties of porous silicon

Porous silicon structures, like other porous materials, are classified by their dominant pore dimensions. Structures with pore dimensions below 2 nm and above 50 nm are called microporous

and macroporous silicon, respectively; those lie between are called mesoporous silicon. Due to the extremely rich details with respect to the range of variations in pore size, shape, orientation, branching, interconnection, and distribution, morphology is the least quantifiable aspect of this material. **Figure 1** schematically demonstrates the four different morphological aspects of porous silicon and their variations, and **Figure 2** shows cross-sectional SEM micrographs of different porous silicon structures.

Various morphologies and different pore dimensions give porous silicon extremely diverse structural, mechanical, optical, electrical, thermal, emissive, physiochemical, and biochemical properties. **Table 1** compares the properties of mesoporous silicon with those of bulk silicon. As the structure and surface chemistry of porous silicon can be precisely controlled during properly chosen fabrication process and appropriate post-fabrication treatment, the material's properties can be tuned according to the desired application. Tuning of porous silicon properties can be performed by manipulating its structural parameters, altering its surface chemistry, or impregnating other materials [4].

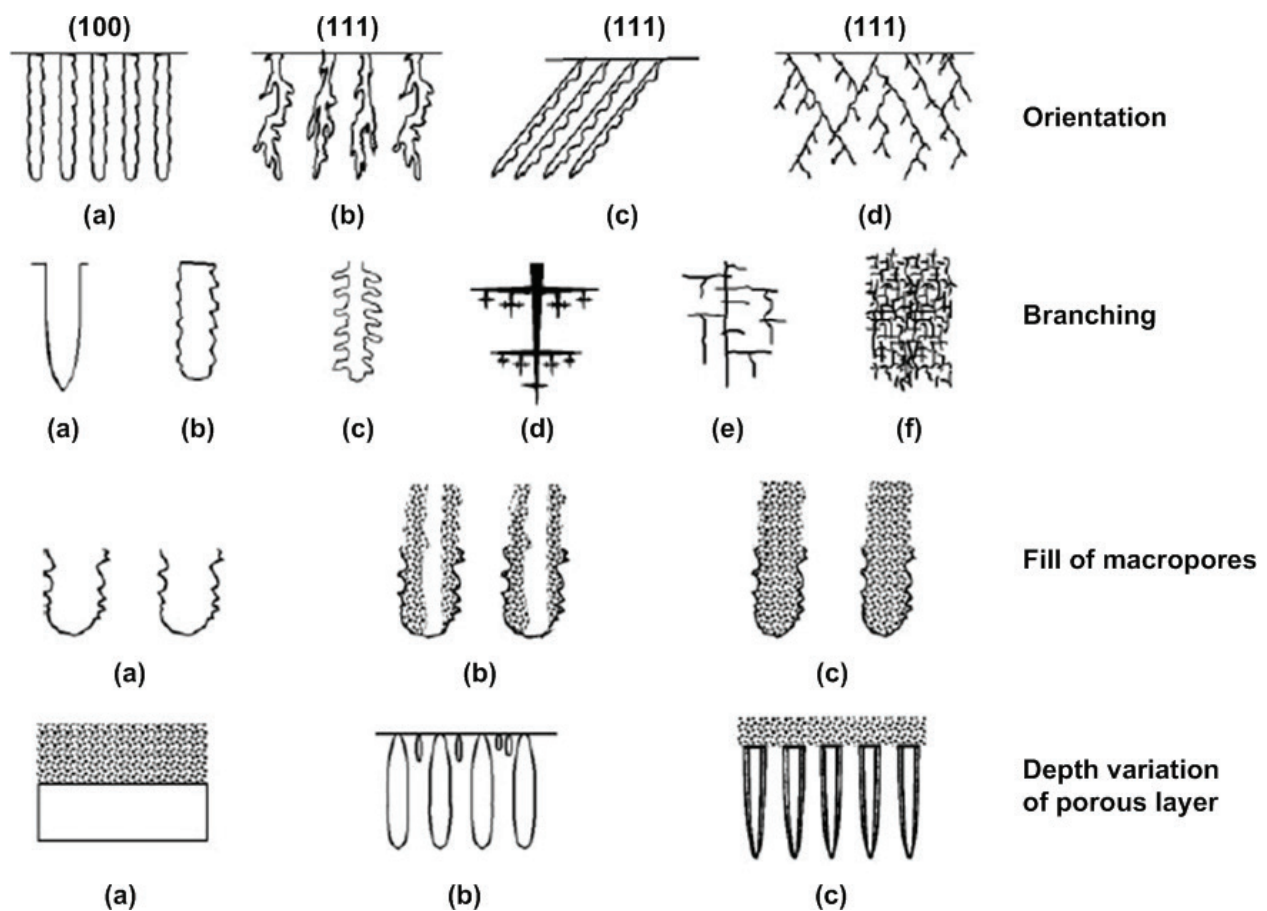


Figure 1. Morphological characteristics of porous silicon; Orientation: (a) aligned to $\langle 100 \rangle$ direction and source of holes, (b) roughly aligned to source of holes, (c) partially aligned to $\langle 100 \rangle$ direction and source of holes, (d) aligned only to $\langle 100 \rangle$ direction; branching: (a) smooth pore walls, (b) branches shorter than diameter, (c) second level branches only, (d) dendritic branches, (e) main pores with second and third level branches, (f) dense, random and short branches; fill of macropores: (a) unfilled, (b) partially filled with microporous Si, (c) fully filled with microporous Si; depth variation of the porous layer: (a) single layer of microporous Si, (b) single layer of macroporous Si with smaller pores near the surface, (c) a layer of microporous Si on top of macroporous Si (Macropores may be filled by microporous Si.) [5].

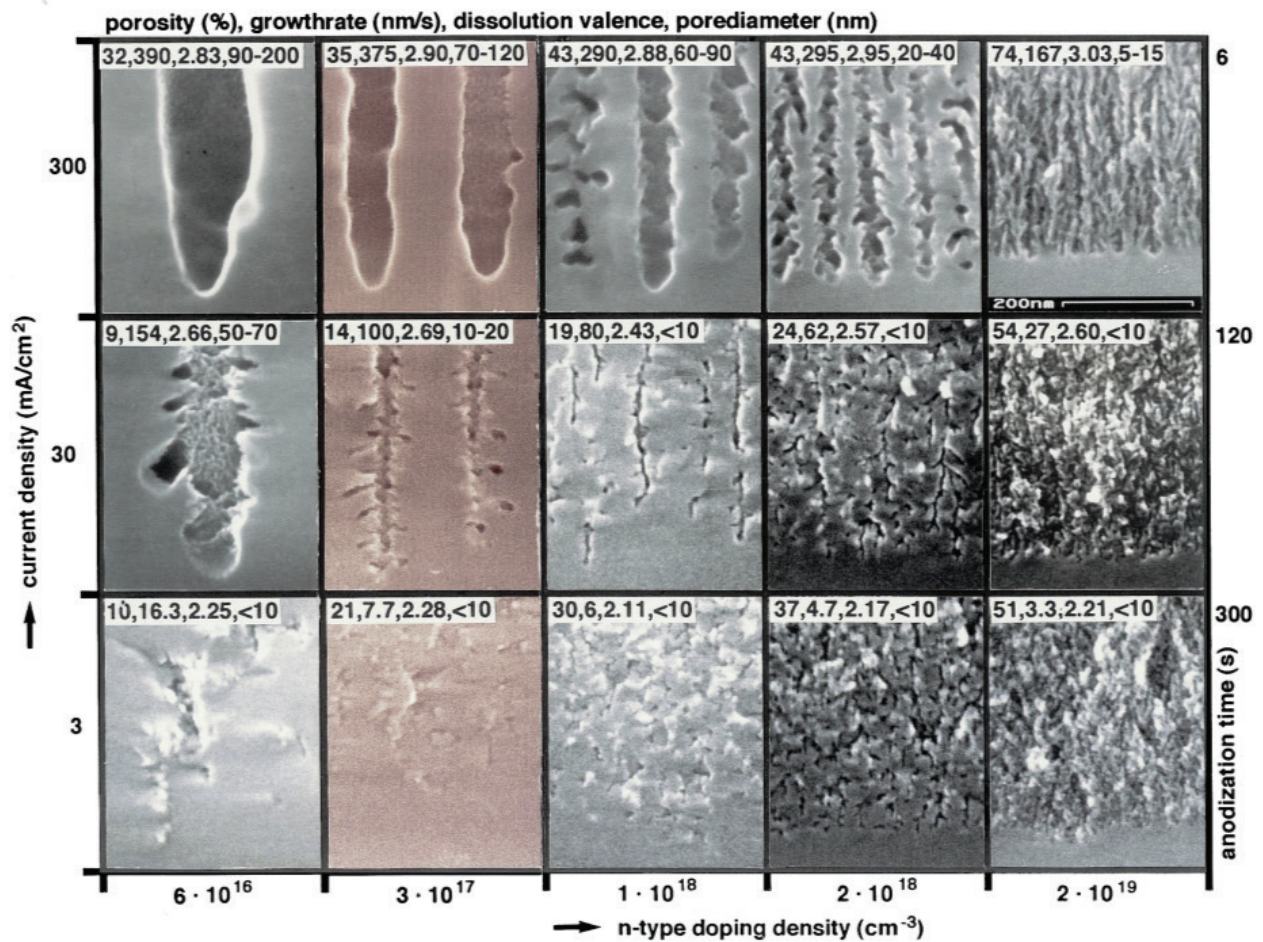


Figure 2. Cross-sectional SEM micrographs of various porous silicon structures formed by anodic etching [6].

	Property	Bulk silicon	Mesoporous silicon
Structural	Porosity	—	20–95%
	Density	2.33 g/cm ³	0.12–1.9 g/cm ³
	Pore size (diameter)	—	2–50 nm
	Surface area	—	100–800 m ² /g
	Lattice structure	Diamond	Diamond
Mechanical	Young's modulus	160 GPa	1–100 GPa
	Hardness	11.5 GPa	0.2–10 GPa (layer)
			0.05–1 GPa (composite)
	Yield strength	7 GPa	—
	Fracture toughness	0.6 MPam ^{1/2}	—
Optical	Bandgap	1.1 eV	1.1–3.2 eV
	Infrared refractive index	3.5	1.1–3.0
	Color	Gray	All colors (layer)
			Brown-yellow (particle)
Reflectivity (500–1000 nm)	10–35%	0.1–10%	

	Property	Bulk silicon	Mesoporous silicon
Electrical	Resistivity	10^{-2} – 10^3 Ωcm	10^3 – 10^{12} Ωcm
	Free electron mobility	1350 cm^2/Vs	0.1–30 cm^2/Vs
	Hole mobility	480 cm^2/Vs	2–6 cm^2/Vs
	Dielectric constant	11.5	2–8
Thermal	Conductivity	150 W/mK	0.03–20 W/mK
	Melting point	1414°C	800–1414°C
	Specific heat	0.7 J/gK	–
	Diffusivity	0.8 cm^2/s	–
Emissive	PL wavelength	1000–1200 nm	400–1300 nm
	PL efficiency	10^{-6}	0.01–0.23 (films) 0.01–0.6 (suspensions)
	EL efficiency	10^{-8}	0.01–0.1
Physiochemical	Isoelectric point	pH 1.6–2.5	pH 1.6–7.7
	Zeta potential (pH 7)	–(45–70) mV	–
	Surface wettability	5–96°	<0.5–167°
Biochemical	Medical biodegradability	–	Months (implants) Days (microparticles) Hours (nanoparticles)

Table 1. Tunable properties of mesoporous silicon in comparison with those of bulk silicon [4].

3. Fabrication of porous silicon

Since 1956 that porous silicon was discovered, more than 20 methods have been developed to fabricate porous silicon structures. These methods can be divided into two categories: top-down and bottom-up. In the top-down approach, clusters of a monocrystalline silicon wafer are removed to generate voids in an almost perfect crystal, and form a porous structure. This approach relies on chemical and/or physical removal of the atoms from a silicon wafer. The result would be a chip-based porous silicon layer. In contrary, bottom-up approach relies on putting silicon clusters together in such a way that while establishing a crystalline form, leaves empty spaces behind so that a porous structure can be synthesized. These approaches usually lead to porous silicon powders. In this section, all fabrication routes introduced for preparation of porous silicon will be discussed; however, it should be noted that among about 20 fabrication routes, less than a dozen has attracted attention.

3.1. Anodic etching

Before chemical mechanical polishing became dominant, electropolishing was used for planarization of silicon wafers. In electropolishing, a silicon wafer is placed in an electrochemical

cell as the anode, a platinum electrode is utilized as the cathode, and hydrofluoric acid as the electrolyte. Passing electric current through the silicon wafer leads to dissolution of silicon atoms and removal of surface roughness if a critical current density (J_{PSL}) is exceeded. In 1956, something went wrong during an electropolishing process at Bell Labs, and the current in the cell reduced leaving a matt black, brown, or red layer on the surface of the wafer [7]. For more than a decade, it was believed that the matt dark layer formed on the silicon surface was a sub-fluoride (SiF_{2x}) grown during the anodic dissolution. Later, it was proposed that the dark film was a dissolution/precipitation product resulted from a two-step disproportionation reaction. Finally, in 1969, it was discovered that the layer indeed has a porous structure formed by dissolution of silicon atoms in an electrochemical etching process [5].

Anodic etching, which is also called electrochemical etching, has been the most common method for the fabrication of porous silicon over the last 60 years. During these years, three electrochemical cell configurations have been utilized for the formation of porous silicon: lateral cell, single cell, and double cell. Lateral cell, which is the simplest electrochemical cell used for anodic etching of silicon, is shown in **Figure 3(a)**. Silicon wafer about to be etched serves as the anode, platinum or any other conducting material resistant to hydrofluoric acid, like graphite, serves as the cathode electrode, and the cell body is made of acid-resistant polymers like PTFE. As the wafer is soaked in HF, any silicon surface that is exposed to the electrolyte is porosified as long as the current density remains below the critical value ($J < J_{PSL}$). The main advantages of the lateral cell are its simplicity and ability to anodize silicon-on-insulator (SOI) wafers. Its drawback is the nonuniformity in both porosity and thickness of the resulting layer. This inhomogeneity is due to a lateral potential drop across the wafer which leads to nonuniform current density and therefore nonuniform porosity and thickness [8].

The second configuration, single cell, shown in **Figure 3(b)**, is the most common electrochemical cell used for porosification of silicon wafers. In order to provide uniform current density inside the silicon wafer, a back-side contact is used for the anode and the wafer is sealed so that only its front-side could be exposed to the electrolyte. Using this single cell configuration, acceptable porosity and thickness uniformity can be achieved for low resistivity silicon wafers. However, high resistivity wafers need high dose B or P ion implantation and subsequent annealing on their back-side to provide appropriate electrical contact to the external circuit. This implantation and subsequent annealing steps might be even followed by deposition of a thin layer of metal. Single cell configuration provides simultaneous control over porosity and thickness of the porous silicon film. Moreover, illumination which is necessary for n-type silicon wafers, can be easily performed in this cell. Using chemical pumps to circulate the electrolyte further improves the uniformity and minimizes the attachment of hydrogen bubbles to the silicon surface [9].

The last configuration, double cell, is designed to optimize the uniformity of porous silicon layer. It is composed of two half-cells separated by the silicon wafer about to be etched as illustrated in **Figure 3(c)**. Large platinum electrodes which are immersed in both half-cells serve as anode and cathode. The electric current flows from one half-cell to the other through the wafer. Hence, the front-side and back-side of the wafer act as local anode and local cathode. Chemical pumps are used to circulate the electrolyte between the half-cells to prevent any decrease in the local concentration of the electrolyte and remove the hydrogen bubbles. Here, electrolytic contact to the wafer reduces the nonuniformities associated with the back-side metal contact in

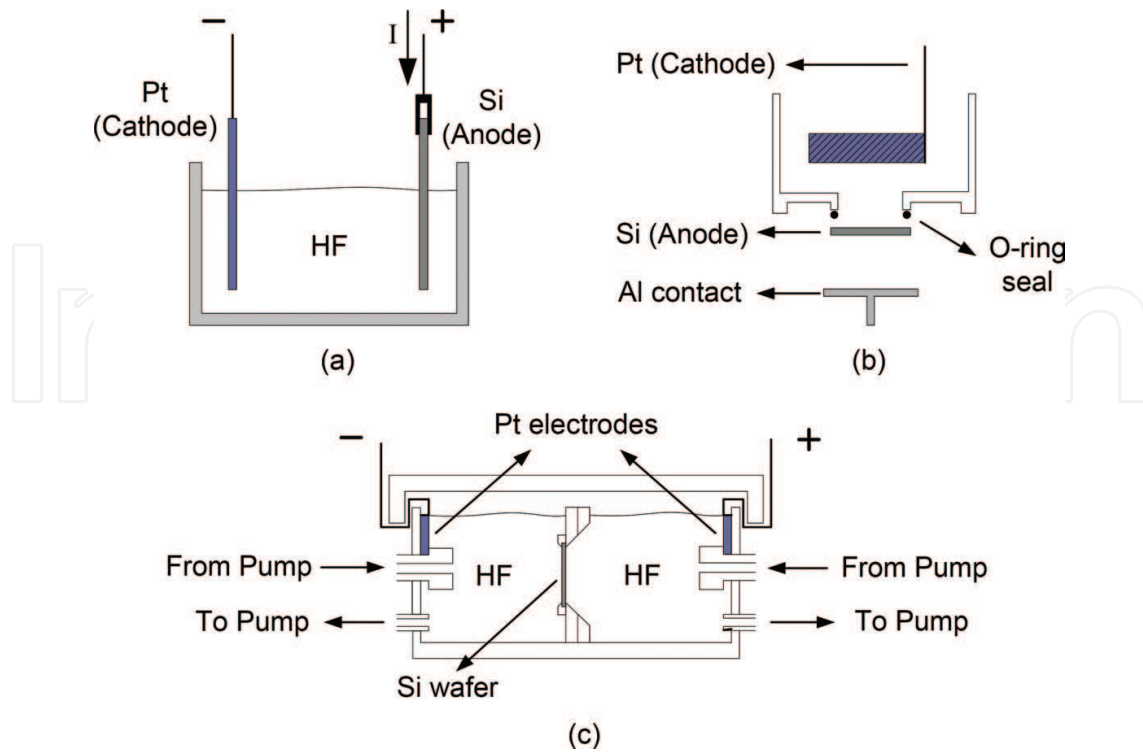


Figure 3. Electrochemical cell configurations used for the fabrication of porous silicon: (a) lateral cell, (b) single cell, and (c) double cell [8, 10].

the single cell approach. It also resolves the necessity of metallization in high resistivity wafers. By contrast, the equipment setup is complicated in comparison to the other electrochemical cells used for porosification [10]. In this configuration, if anodic etching under illumination is needed, the cell body should be made of transparent acid-resistant materials like PMMA.

The dissolution of silicon atoms by anodic etching can be controlled by either the current or the voltage of the electrochemical cell. Generally, constant current is preferred due to reproducibility and better controllability of porosity and thickness of the porous layer [11]. In the dissolution process, hydrogen gas is freed. The generated hydrogen bubbles are attached to the surface for some time preventing the electro-active species to reach the surface and interrupt the dissolution process. Addition of a surfactant like ethanol or methanol improves the penetration of the electrolyte into the pores and minimizes the hydrogen bubbles evolution [9]. Besides aqueous, ethanolic, or methanolic HF electrolytes, porous silicon can also be formed in the mixture of HF with metal oxides like manganese(IV) oxide MnO_2 , or certain organic compounds like acetonitrile CH_3CN and dimethylformamide (DMF).

Depending on the fact that electrochemical cell works either in electropolishing regime ($J > J_{\text{PSL}}$) or porosification ($J < J_{\text{PSL}}$), the charge transfer reactions that lead to the removal of the surface silicon atom, could be a tetravalent or divalent mechanism respectively. **Figure 4** illustrates the divalent mechanism which leads to formation of porous silicon structures. In situ spectroscopy of silicon samples immersed in HF-based solutions has shown that the silicon surface is passivated by Si–H bonds [12]. As the Si–F bond (6 eV) is much stronger than the Si–H bond (3.5 eV), the possibility that the surface had been passivated by fluorine and then Si–F bonds

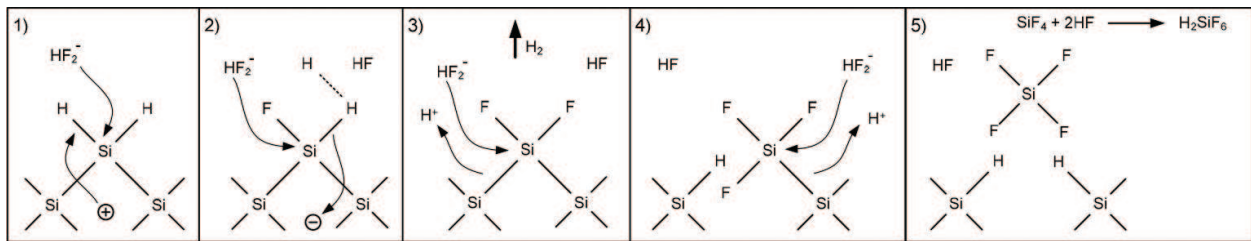
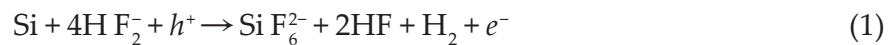


Figure 4. Divalent electrochemical dissolution of a silicon atom in hydrofluoric acid solution [13].

were replaced by the Si–H ones, is ruled out. This led to the conclusion that if a surface silicon atom establishes a bond to a fluorine atom, it is immediately removed from the surface and the surface is passivated by hydrogen [13]. The dissolution of a surface atom begins when a hole traveling inside the silicon wafer reaches the interface of silicon and electrolyte (stage 1). At this point a bifluoride (HF_2^-) ion from the solution could attack Si–H bonds replacing one with a Si–F bond. Since the electronegativity of hydrogen is close to that of silicon, Si–H bonds are effectively unpolarized; therefore, they could not be influenced by bifluoride anions unless a hole was present. After the first Si–F bond established, due to its polarizing effect, another bifluoride anion attacks the silicon atom releasing a hydrogen molecule as depicted in stage 3 of the figure. The polarization induced by the Si–F groups lowers the electron density of the silicon back-bonds and facilitates the dissolution of the loosely bounded silicon atom by HF. After the removal of a silicon atom, the remaining surface passivates with hydrides again (stage 5). The overall reaction in the divalent process can be summarized as Eq. (1):



If the dissolved silicon atom was removed from a microscopically flat surface, its removal leaves a microroughness. This small topographical alteration changes the distribution of the electric field which increases the probability of presence of the holes. Hence, the etch rate at microroughness becomes greater than the surrounding flat areas. Accordingly, surface roughness increases and eventually a porous structure is formed.

Anodic etching is the most common method for the fabrication of chip-based n-type and p-type porous silicon. All classes of porosity can be realized by anodic etching with proper control over the porosity and thickness. Although there has been success in integration of anodically etched porous silicon structures with electronic circuitry, this fabrication method is not compatible with standard ULSI technology [14].

3.2. Stain etching

Shortly after observation of the matt dark layer on silicon wafer which had been subjected to electrochemical etching, when the porous nature of the material were still unknown, similar structures were realized by electroless chemical etching of silicon in mixture of hydrofluoric acid and concentrated nitric acid solution [15]. Due to the stains formed on the surface of the silicon wafer as a result of electroless chemical dissolution (**Figure 5**), this method became known as stain etching.

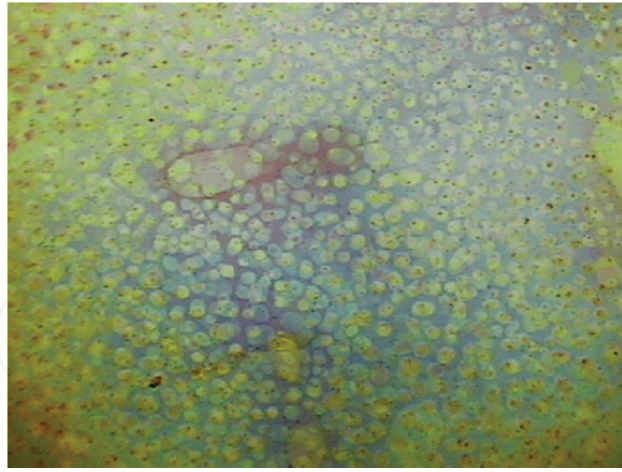
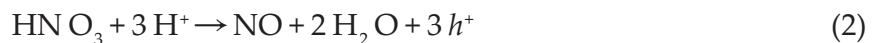


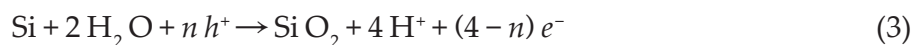
Figure 5. The stains formed on the silicon surface after being subjected to electroless chemical etching.

Although an external potential is not applied to the silicon wafer to be etched by this route, dissolution of silicon atoms has a localized electrochemical mechanism. Indeed, sites of the silicon surface temporarily act as local cathode and local anode. Complex charge transfer reactions taking place between these local electrodes lead to the removal of an atom at the local anode site. Few moments later, these local electrode sites will no longer have their previous roles; they might become neutral areas or might even turn into new local electrodes; yet, it is probable that a local anode site will become a local electrode again. When a silicon atom is removed from the surface, the resulting microroughness attracts the electric charge carriers passing by. If this charge carrier was a hole, the site would act as a local anode again. Continuation of this local electrochemical process leads to formation of a porous layer. Due to the electrochemical mechanism of stain etching, holes do have a critical role in the removal of silicon atoms and formation of pores, as they do in the anodic etching of silicon. Hence, p-type silicon which has at least thousands of holes in every cubic micrometers can be easily porosified, while n-type silicon which has negligible holes usually needs illumination.¹ Incident photons with proper energy ($h\nu > E_g$) generate holes in the n-type silicon and promote stain etching.

The reaction in the local cathode consists of a series of complicated reaction pathways that lead to the reduction of HNO_3 , generation of NO , and injection of holes into the silicon. The first stage of these reaction pathways is the formation of HNO_2 which is the rate-limiting step of overall reaction. The cathode reaction can be summarized as Eq. (2):



If the injected holes do not recombine with free electrons of the silicon wafer, they could attach to a silicon atom, which then turns to be a local anode and oxidized as depicted by Eq. (3):

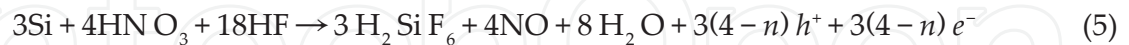


¹Stain etching under illumination should not be confused with photoetching which will be discussed in the following subsection.

The oxidized silicon atom is then removed by hydrofluoric acid (Eq. (4)), and the residual protons (H^+) at the anode site react with HNO_3 and repeat the cycle.



The overall reaction can be written as Eq. (5):



where n being the average number of holes needed to remove one silicon atom [16].

Although porous silicon formation by stain etching usually occurs in HF/ HNO_3 solution, the mixture of hydrofluoric acid with other compounds such as sodium nitrite $NaNO_2$, chromium(VI) oxide CrO_3 , iron(III) chloride $FeCl_3$, and potassium iodate KIO_3 can also lead to formation of porous silicon structures [17–19]. The reaction pathways that lead to the dissolution of silicon atoms are similar to those that occur in HF/ HNO_3 solution. The strong oxidizing agent of the solution oxidizes silicon atoms and the oxidized atoms are removed by HF, forming a soluble complex. It is also possible to use acetic acid as a surfactant. It does not participate in the chemical reactions; it only dilutes the solution and decreases the surface tension so that better wetting and a smoother surface would be achieved [16].

Stain etching is the simplest, most straightforward, and most inexpensive way to fabricate porous silicon. It almost needs nothing but a plastic beaker. It can be used to prepare porous silicon on a SOI wafer in which buried oxide layer makes electrochemical etching difficult. The main disadvantage of this method is that there is an upper limit (about 1.5 μm) for the thickness of the porous silicon layer.

3.3. Photoetching

Fabrication of mesoporous silicon by photoetching has been introduced in 1993 [20]. In the proposed method, silicon wafer is immersed in the aqueous HF solution under illumination of He-Ne laser as shown in **Figure 6**. Although coherent light sources have usually been utilized, photoetching can also be performed by incoherent sources such as Xe lamps and W lamps [21, 22]. Due to the built-in electric field existed in silicon, near its interface with the solution, formation of porous structures by this method is restricted to n-type silicon substrates. Indeed, illumination of both n-type and p-type silicon with proper photon energies ($h\nu > E_g$), breaks the Si-Si bonds and generates free electron/hole pairs. The charge carriers generated near the surface are drifted by the built-in electric field, but the direction of the built-in electric field is different for n-type and p-type silicon. In the n-type silicon, holes are pushed toward the surface where they can facilitate the removal of a nearby silicon atom, while the opposite direction of the built-in electric field in p-type silicon wafers drives the holes away. Hence, photoetching can only remove silicon atoms from the n-type silicon wafers.²

²It should be noted that it is not impossible to prepare p-type porous silicon by photoetching; however, the rate of the process is extremely disappointing [23].

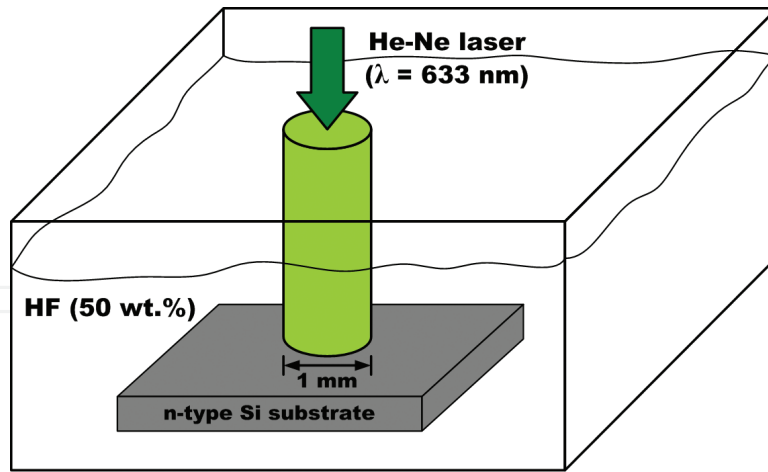


Figure 6. Porous silicon formation by photoetching.

Porosification of silicon also depends on the wavelength of the incident light. If the energy of the incident photons is less than the silicon bandgap ($h\nu < E_g$), the photons are not absorbed by the wafer and the light travels through the material. In this case, neither free electron/hole pairs are generated, nor dissolution of silicon atoms takes place. In contrast, if the energy of the photons is greater than the bandgap of silicon, the light is absorbed and generated holes facilitate the dissolution of silicon atoms and formation of porous structures. Nevertheless, the formation of porous structures does not necessarily lead to the formation of a porous layer. Indeed, the porous layer cannot be formed unless porous structures survive and porosification continues. If the energy of the incident photons is less than the bandgap of the fabricated porous structures, the light reaches the underlying substrate and generates free electron/hole pairs there (Figure 7(a)). Generated holes are then promote the removal of silicon atoms; therefore, porosification continues and the porous layer is formed. However, if the energy of the photons is not only greater than the bandgap of silicon but also greater than that of porous silicon structures, photons are absorbed in the porous structures and lead to their removal (Figure 7(b)).

Figure 8(a) shows a micrograph of a porous structure formed in HF solution under illumination of the He-Ne laser beam for 60 minutes. Part (b) of this figure depicts the relation of

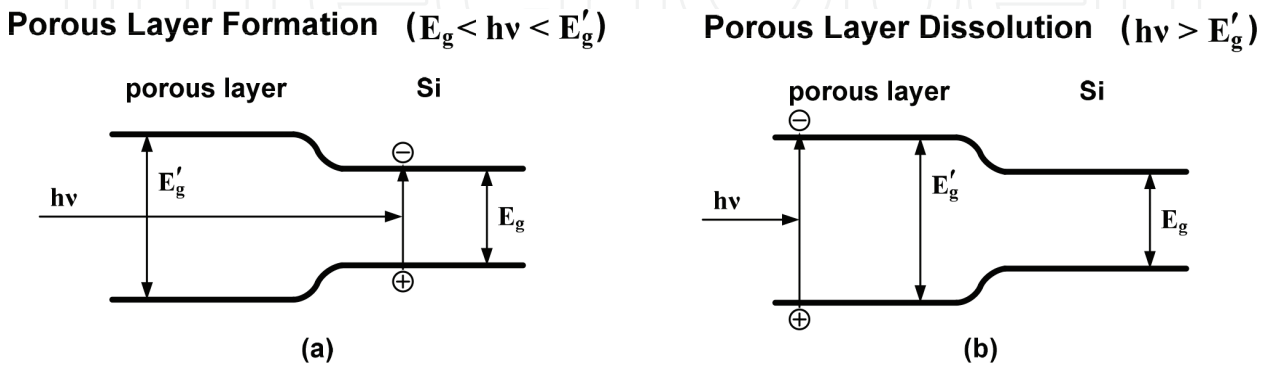


Figure 7. Formation of porous silicon layer depends on the energy of incident photons: (a) porosification continues and a porous layer is formed, and (b) porous structures are dissolved once being formed [20].

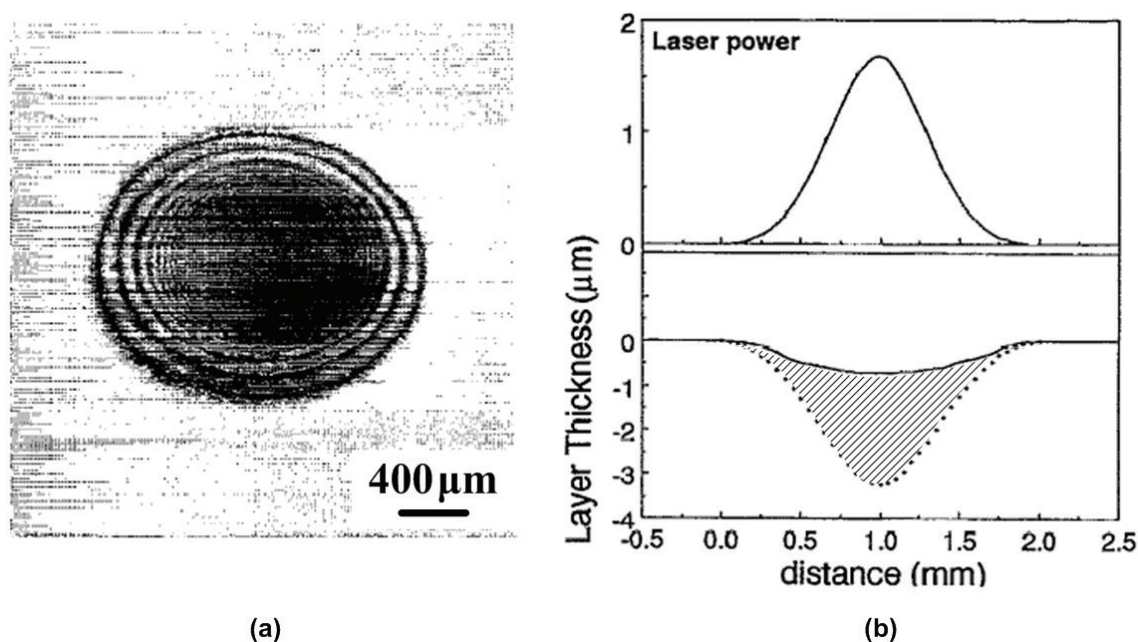


Figure 8. Porous silicon layer synthesized by photoetching: (a) micrograph, (b) relation between the power distribution of the incident beam and the synthesized porous layer [20].

optical-power distribution of the incident laser beam and the synthesized porous layer. The dip at the center shows the complete removal of silicon atoms and the marked area illustrates the porous region. It is observed that the thickness of the porous layer linearly increases with the photoetching duration regardless of the crystal orientation of the specimen [20]. Addition of a mild oxidizing agent like H_2O_2 or I_2 to the HF solution leads to stable formation of porous layers in much shorter periods of time [24].

In addition to the aqueous HF solution, porous silicon structures have been photoetched using aqueous solutions of sodium fluoride NaF and potassium fluoride KF [25]. The chemical reactions lead to the removal of silicon atoms are almost the same. For instance, potassium fluoride dissociates into K^+ and F^- ions. Due to negligible solubility of F^- , the dissociation of KF would be as follows:



The holes, generated by illumination, dehydrogenates the surface silicon atoms and facilitate the establishment of surface Si—F bonds. The atoms are then attacked by bifluoride anions and removed leading to formation of the porous layer.

It should be noted that stain etching can also be performed under illumination in which the incident light generates free electron/hole pairs and increases the etch rate. However, such a photo-assisted chemical dissolution of silicon should not be considered photoetching unless the solution was unable to dissolve silicon by itself and the light was the key factor. However, this classification has not always been followed and photo-assisted stain etching processes were incorrectly addressed photoetching [18, 19, 26].

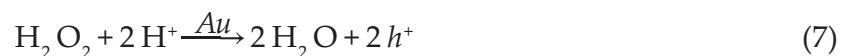
Photoetching can be utilized for the realization of porous silicon on SOI wafers, micromachined wafers and wafers with microelectronic circuitry [24]. If HF solution is used, instead of NaF and KF solutions, the technique does not introduce any metallic impurities to the substrate. One of the main limitations of this route is that it only works for n-type silicon wafers. The other is the nonuniform thickness of the realized porous layer.

3.4. Metal-assisted etching

The authors of first reports on the fabrication of porous silicon by metal-assisted etching were not aware of the catalyst role in porous silicon formation mechanism and gave incorrect speculations for the appearance of the pores [27]. It was discovered later that the catalytic behavior of metallic nanoparticles is the key factor in realization of porous silicon layers in this technique. Here, metal catalysts such as Al, Ag, Au, Pd, Pt, Fe, or Au-Pd alloy are deposited and patterned on the surface of the silicon wafer. The wafer is then immersed in a solution consisting of hydrofluoric acid and a mild oxidizing agent. The oxidizing agents used in metal-assisted etching are not strong like those utilized in stain etching, so that silicon dissolution only takes place in the presence of the metal catalyst. While hydrogen peroxide H_2O_2 is the most common oxidizing agent in metal-assisted etching of silicon, porosification can also be performed using sodium persulfate $Na_2S_2O_8$, iron(III) nitrate $Fe(NO_3)_3$, potassium dichromate $K_2Cr_2O_7$, and potassium permanganate $KMnO_4$ [28–30]. The metallic nanoparticle absorbs an electron and injects a hole into the silicon substrate. This hole injection facilitates the oxidation of a nearby silicon atom at the surface. The oxidized silicon atom is then attacked by bifluoride ions and dissolved by a divalent charge transfer reaction.

One way to perform metal-assisted etching is to deposit and pattern metal catalysts and then immerse the predeposited specimen in the etchant consisting of HF and the oxidizing agent. The other way is to immerse the bare silicon wafer in a solution composed of HF and certain metal salts such as silver nitrate $AgNO_3$, potassium tetrachloroaurate(III) $KAuCl_4$, and potassium hexachloroplatinate(IV) K_2PtCl_6 [30, 31]. Here, metal catalysts are precipitated on the silicon surface, and initiate the dissolution process.

Similar to anodic etching, stain etching, and photoetching discussed in the previous subsections, holes have a key role in dissolution of silicon atoms in the metal-assisted etching. For instance, in gold-assisted porous silicon formation in HF/ H_2O_2 solution, holes necessary for silicon atoms removal are generated from the reduction of hydrogen peroxide. Due to the enormous difference between the electrochemical potential of hydrogen peroxide and silicon, H_2O_2 injects few holes into the valence band of silicon even in the absence of a metal catalyst. Since silicon atoms removal in HF-based solutions stems from the presence of holes near the silicon surface, dissolution of silicon wafers is possible in the HF/ H_2O_2 solution; however, the etch rate is only few nanometers per hour [13]. The presence of gold catalytically promotes the reduction of H_2O_2 and significantly increases the number of injected holes as depicted in Eq. (7):



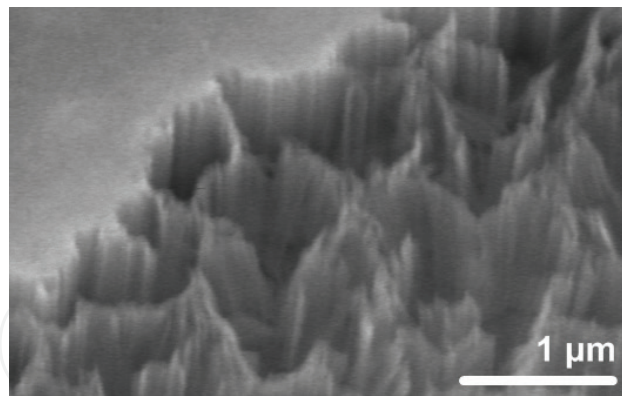
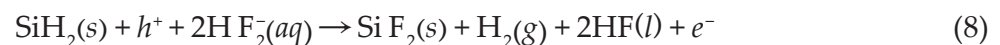


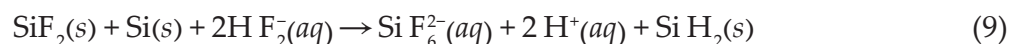
Figure 9. An SEM image of a sample subjected to metal-assisted etching after selective lithographic patterning. Only regions coated with the metal catalyst were etched [32].

The injected holes accelerate the silicon atoms removal by a practical etch rate. **Figure 9** demonstrates an SEM image of a sample in which the gold catalyst layer was selectively removed prior to be immersed in HF/H₂O₂ solution. While significant etching occurred in the metal-coated area of the wafer, there has not been any visible dissolution in the uncoated regions.

The dissolution of the silicon atom after hole injection is a divalent charge transfer reaction in which the surface Si–H bonds are replaced by Si–F bonds as depicted in Eq. (8):



The silicon atom is then removed as a result of bifluoride ions attack:



By proper adjustment in the ratio of oxidizing agent to hydrofluoric acid, it is possible to control the class of porosity and fabricate mesoporous and macroporous structures [32]. As porous silicon formation only takes place in the area coated with the metal catalysts, any desirable pattern for the porous area can be easily achieved. The introduction of metallic impurities to the substrate is the main disadvantage of metal-assisted etching.

3.5. Vapor etching

In 1999, Bessaïs and his colleagues observed that porous silicon can be fabricated on top of a solar cell structure if the device is being sprayed by HF droplets [33]. The dissolution of silicon atoms was attributed to the low velocity of HF droplets initiating the idea of etching silicon with low velocity HF/HNO₃ droplets that later became known as vapor etching. **Figure 10** schematically demonstrates the experimental setup used for preparation of porous silicon by vapor etching [34]. The polypropylene container partially filled with HF/HNO₃ solution is placed in a thermostatic bath. The silicon substrate is positioned inside the container's lid, a few centimeters above the liquid level. The lid must be sealed so that the empty space above the solution level becomes saturated with acid vapor. As the temperature

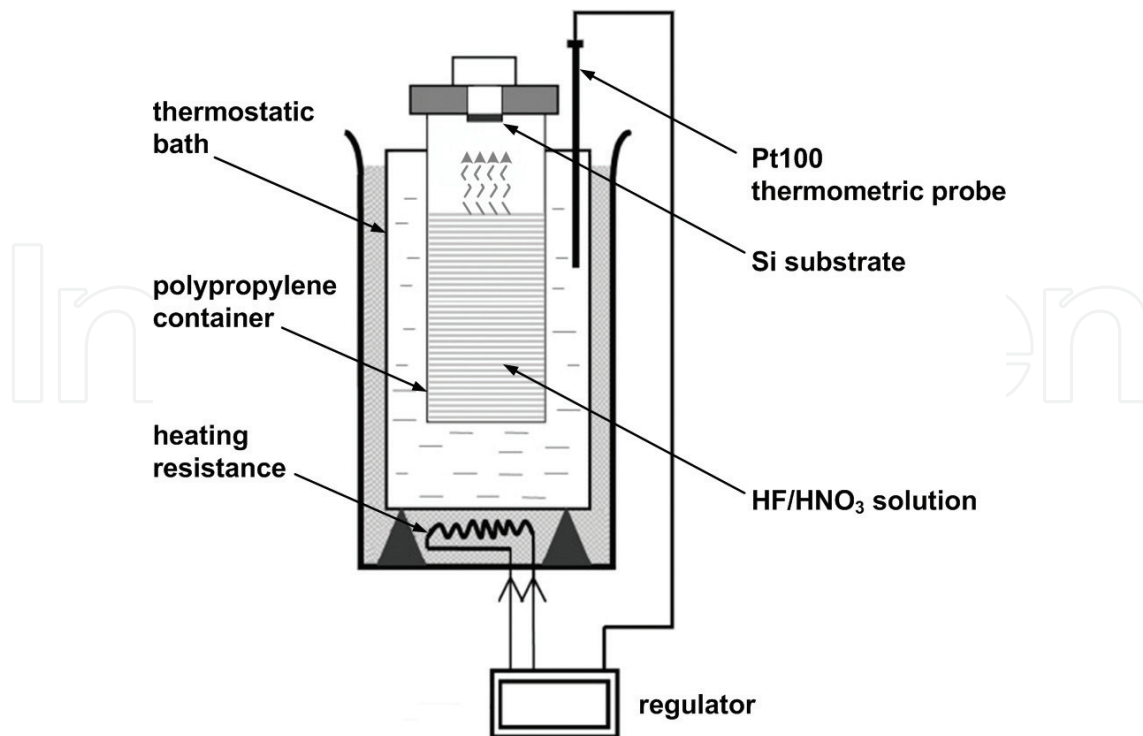


Figure 10. Schematic illustration of vapor etching setup used for porous silicon fabrication [34].

increases, supersaturation leads to the formation of droplets on the container walls and the silicon surface. In case of extremely rough silicon surfaces, the droplets will attach and form a liquid film which destroys the porous layer [34].

In order to achieve homogenous porous layers, the kinetics of the process and hence the determining factors, i.e., concentration and temperature of the solution as well as duration of vapor exposure, must be controlled. Increasing either the HNO₃ content of the solution or the temperature of the process significantly increases the etch rate. For temperatures between 20 and 30°C, the etch rate is rather low and homogenous porous layers can be achieved by exposure times up to 30 min. However, increasing the temperature to 40°C leads to speedy condensation of droplets on the silicon surface and destruction of porous layers unless the exposure time remains below 20 min. At 60°C and beyond, the speed of condensation is so fast that porous layers can only be synthesized in exposure times less than 2 min.

The vapor etching method is rather simple and inexpensive. It can be used for preparation of luminescent silicon structures and antireflection coatings in solar cells where thin layers of porous silicon are required. The concentration of the solution, temperature, and duration of the vapor etching process have to be controlled precisely or ammonium hexafluorosilicate (NH₄)₂SiF₆ and Si/SiO_x nanoparticles will be formed instead of porous silicon [35]. The method is unable to produce highly porous structures as the condensation of the droplets leads to the formation of a liquid film on the surface, which in turn results in the removal of the porous layer. The area of specimen should be chosen small in comparison to the diameter of the container or the uniformity in porosity and thickness will be lost.

3.6. Reactive-ion etching

Chemically stable mesoporous and macroporous silicon structures can be formed as a result of a maskless sequential reactive-ion etching (RIE) of silicon wafers using H_2 , O_2 , and SF_6 plasma [36]. The sequential process is composed of one etching and two passivation subsequences: oxidation and fluorination, as depicted in **Figure 11**. In the etching subsequence, SF_6 ions and radicals of the plasma remove the silicon atoms by a combination of chemical and physical etching mechanisms. During the oxidation subsequence, a very thin oxide layer is formed on the surface of the pores as a result of their exposure to the O_2 plasma. In the following subsequence, fluorination, the dangling bonds of the silicon/oxide interface are replaced by Si–F bonds, transforming the thin oxide layer into a stable SiO_xF_y passivating film. Formation of this SiO_xF_y layer stabilizes the chemical properties of the final porous structure, which always been the inevitable weakness of porous silicon structures formed by HF-based processes [37]. The porous silicon structures evolve by the repetition of these three subsequences.

By proper adjustment of the gases flow rates, plasma powers, durations of the subsequences, and repetition, it is possible to tailor the porosity and thickness of the mesoporous or macroporous material [36]. Since the fabrication process is performed at room temperature, it can be used as a post-fabrication treatment, which is very important in a technological point of view.

3.7. Spark erosion

Spark erosion that later became known as spark processing is another top-down porous silicon fabrication route introduced in the early 1990s [38]. This method can be used to prepare not only porous silicon but also other porous materials such as As, Bi, Ge, GaAs, Sb, Se,

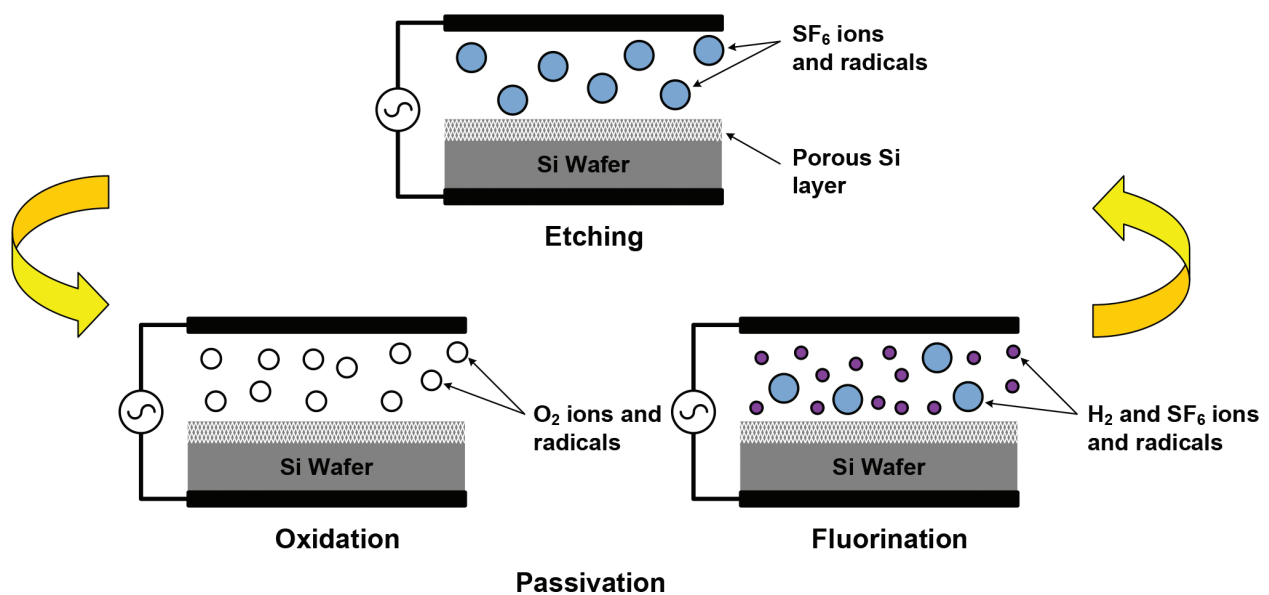


Figure 11. The sequential RIE process to synthesize porous silicon is composed of one etching and two passivation subsequences (oxidation and fluorination) [36].

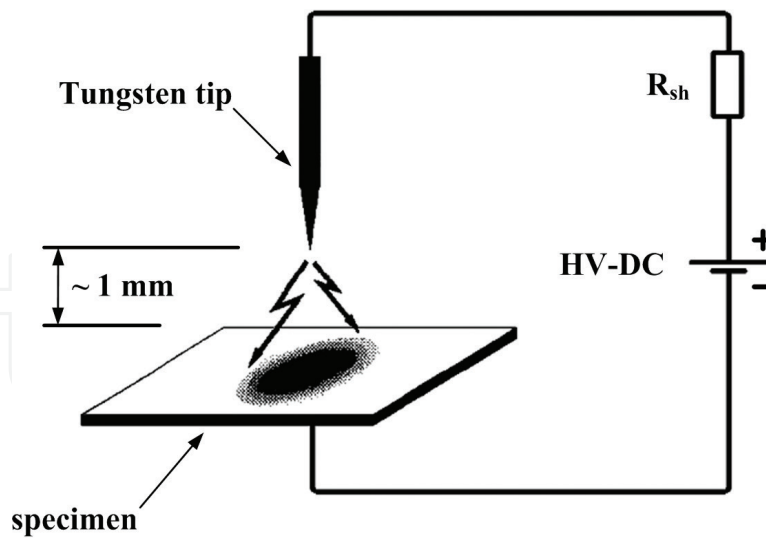


Figure 12. Schematic illustration of porous silicon formation by spark erosion [39].

Sn, and Te [39]. As demonstrated in **Figure 12**, the silicon substrate is placed near a tip and eroded by sparks for at least several hours so that porous structures are formed on its surface. Spark erosion does not involve any chemical reactions in the dissolution of silicon atoms and the removal mechanism is purely physical. The discharges between the tip and the silicon substrate ionize the gaseous environment and the silicon surface is then eroded due to the colliding ions. During their first studies, Hummel and his colleagues used silicon tips and performed spark erosion in pure N₂ to prevent unwanted impurities entering the specimen [38]. However, later studies showed that using a tungsten tip or performing the erosion in air does not increase the impurity level of the substrates [40]. The voltage used for spark processing is in the range of several kilovolts; the currents flow during erosion are in the range of tens of milliamperes; and the average time interval between the sparks is few milliseconds [41]. Although in spark processing chip-based porous silicon structures are formed, the method is incompatible with standard fabrication technology. Moreover, the nonuniform thickness of the porous layer is inevitable in this technique.

3.8. Laser-induced plasma erosion

Another physical process that has been utilized to remove silicon atoms and synthesize porous layers is the generation of the air optical breakdown plasma near a silicon target which its surface is about to be porosified. As depicted in **Figure 13**, optical breakdown is initiated by focusing a pulsed TEA CO₂ laser beam (wavelength of 10.6 μm, pulse energy of 1 J, and repetition rate of 3 Hz) by a Fresnel lens near the silicon target. The intensity of the laser used by Kabashin and Meunier was not enough to initiate the optical breakdown; however, the presence of the silicon target reduces the threshold of the optical breakdown and generates a high temperature plasma (10⁴ K) with intense currents (10⁶ A) [42]. Apparently, light action and contact of the silicon surface with such a plasma lead to localized melting, evaporation, vapor redeposition, recrystallization, erosion of silicon surface, and formation of the porous silicon layer [42].

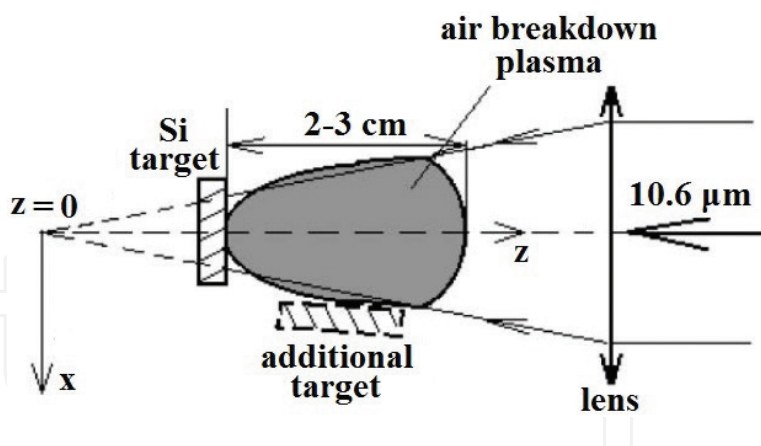


Figure 13. Schematic illustration of the experimental setup used for laser-induced plasma erosion (The additional target shown in the figure was used for control tests and was not necessary for porous silicon formation.) [42].

Using laser-induced plasma erosion, luminescent mesoporous silicon has been prepared on both p-type and n-type silicon wafers regardless of the dopant type or concentration of the silicon wafers. The porosity of the layers is typically between 40 and 70% with thicknesses up to 500 nm. However, the thickness of the porous region shows significant nonuniformity. The area of the porous region varies between hundreds of micrometers and several millimeters depending on the position of the silicon target with respect to the focal plane of the lens.

3.9. Oxidation of Rochow reaction byproduct

Macroporous silicon powders can be synthesized by acid washing and oxidation of Rochow reaction byproducts. Metallurgical-grade silicon powders are ground with Cu-based particles to form a contact mass. The obtained material then reacts with chloromethane CH_3Cl to produce organosilicon compounds (Rochow reaction³). The waste contact mass byproduct is composed of unreacted silicon, metal compounds, and deposited carbon. Recovering the metal components by acid washing leaves porous Si/C composite as depicted in **Figure 14**. Such a porous Si/C composite has been successfully used as the anode in lithium-ion batteries [44]. Porous silicon can be obtained by oxidation of the Si/C composite in air at 400°C for 1 h.

3.10. Ion implantation

Macroporous silicon structures can be fabricated by low-energy high-dose ion implantation of silver into monocrystalline silicon wafers without any thermal annealing process [45]. The implantation is carried out at the energy of 30 keV and doses above $1 \times 10^{16} \text{ cm}^{-2}$. Pore formation is presumably driven by microexplosion and voids clustering. It is believed that microexplosion initiates a void and lowers the energy required for the formation of nearby voids; the neighboring voids then cluster to minimize the dangling bonds density [45, 46]. The fabricated porous layer has an average pore size of about 120 nm. It has been observed that during ion implantation, silver atoms are agglomerated inside the pore walls forming nanoparticles with dimen-

³Rochow reaction is the most common route to synthesize organosilane monomers in the chemical industry [43].

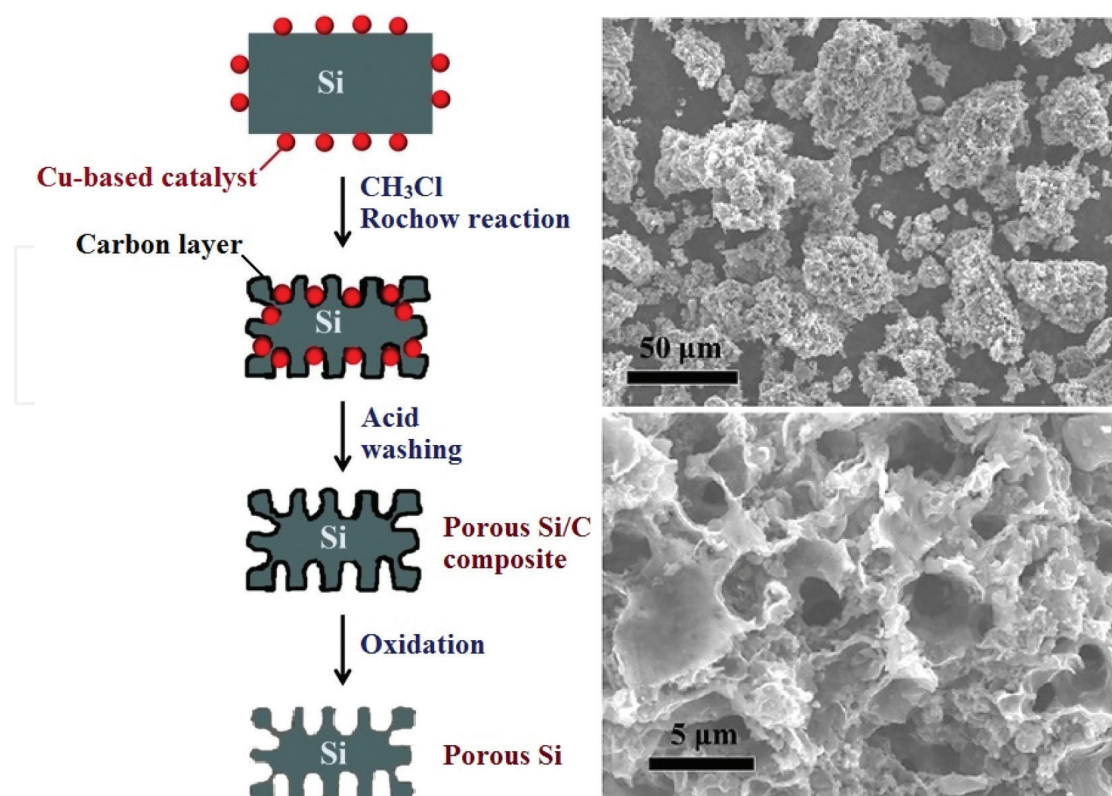


Figure 14. Synthesis and SEM micrographs of porous Si/C composite synthesized by acid washing of Rochow reaction byproduct [44].

sions between 5 and 10 nm. Although the electromagnetic coupling between localized surface plasmon of silver nanoparticles and porous silicon structures promotes the optical behavior of the material, the presence of metallic nanoparticle is undesirable in other application areas.

3.11. Plasma hydrogenation

This method has been introduced in 2005 for the fabrication of luminescent microporous and mesoporous silicon [47, 48]. In contrast to the fabrication routes already discussed in this chapter, plasma hydrogenation is a bottom-up approach. It starts with the deposition of a thin amorphous silicon (a-Si) layer with a thickness of about 200 nm. The amorphous layer is deposited by physical vapor deposition techniques like evaporation [47, 48] or sputtering [49, 50] instead of chemical vapor deposition to increase the number of voids. Later, the specimens are placed in a DC plasma-enhanced chemical vapor deposition (DC-PECVD) setup to be exposed to DC hydrogen plasma as illustrated in **Figure 15**. After the hydrogenation, a thermal annealing step is performed. It is believed that hydrogen radicals of the plasma replace the dangling bonds of the amorphous silicon layer during the hydrogenation step; then, in the annealing step, the silicon surface is depassivated and H_2 is exhausted from the specimen. The energy freed from breaking Si–H bonds promotes the rearrangement of silicon atoms of the specimen and a porous crystalline structure is formed [51]. Although porous silicon can be realized by performing one hydrogenation followed by one annealing step, breaking the process duration into three consecutive repetition of hydrogenation and annealing steps provide more controllability over the properties of the synthesized porous layer. This fabrication process is

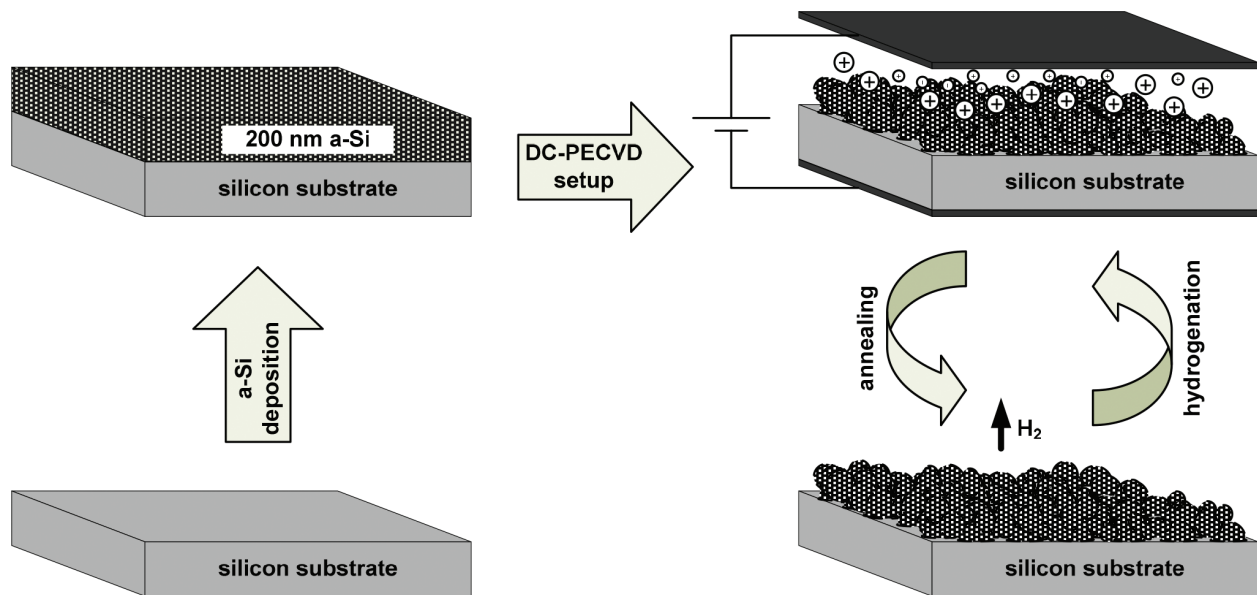


Figure 15. Schematic illustration of fabrication process of porous silicon by plasma hydrogenation.

fully compatible with standard ULSI technology. Moreover, as it is a low-temperature process (below 400°C), it can be considered as a post-fabrication treatment to implement luminescent porous silicon devices on a chip with microelectronic circuitry. The limitation of this fabrication route is that only thin layers of porous silicon can be synthesized.

3.12. Laser ablation

Another bottom-up approach to realize porous silicon is collecting laser-ablated silicon clusters [52]. In this technique, a silicon target is irradiated with a pulsed laser beam in a vacuum chamber as illustrated in **Figure 16**. The laser-ablated silicon clusters are collected by placing the substrate in the vicinity of the target where the ablation plume could reach. The substrate is usually heated to increase adhesion of the porous layer. It is also rotated to increase the uniformity of the deposited film. The porosity and thickness of the porous silicon layer can be controlled by the power of the incident laser, the distance between the substrate and the target, and duration of the ablation. This technique has not attracted much attention for chip-based applications due to its incompatibility with standard technology.

3.13. High-density plasma deposition of silicon

Mesoporous silicon structures can be fabricated by deposition of high void density crystalline silicon films using low-temperature high-density plasma. An electron cyclotron resonance (ECR)-PECVD tool with hydrogen diluted silane at about 100°C has been utilized for the preparation of thin films composed of nanoscale silicon columns in a void matrix [53]. Porous layers has been realized in the pressure ranges between 5 and 12 mTorr corresponding to microwave power between 640 and 340 W. Formation of the porous structure stems from low mobility and therefore low diffusion length of the deposition species compared to the average distance between the physisorption sites. The low mobility of deposition species can be attributed to the low substrate temperature as well as the low kinetic energy of the impinging ions

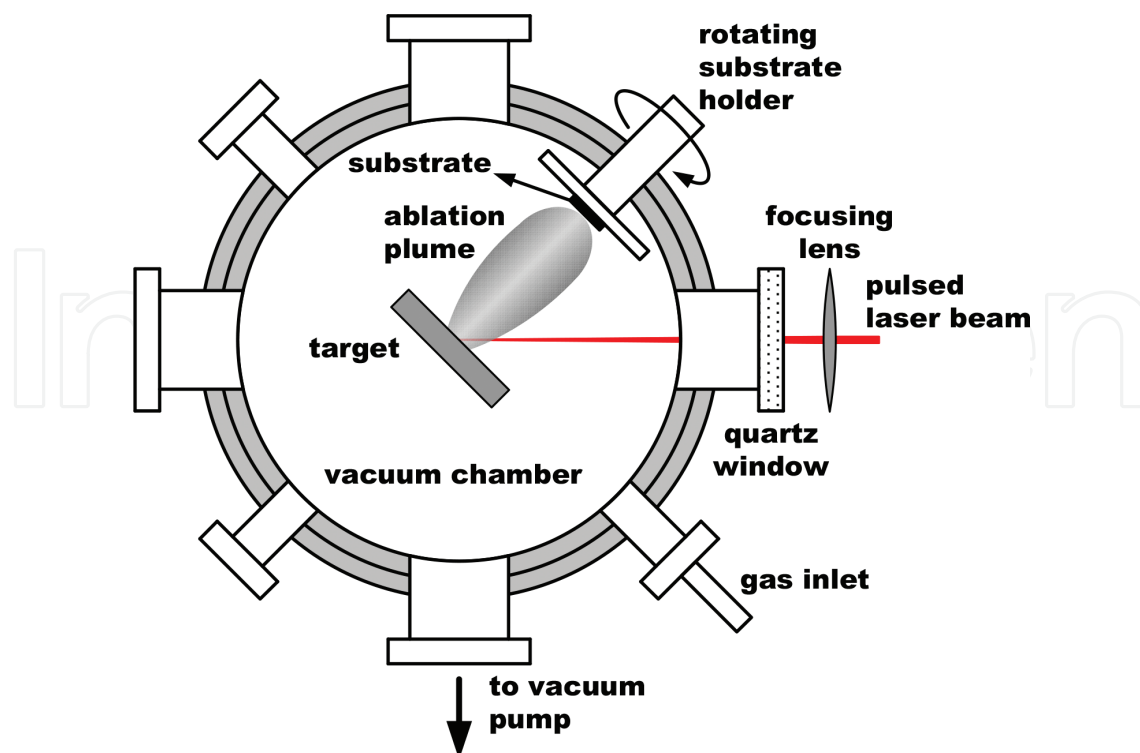


Figure 16. Schematic illustration of the laser ablation setup.

of the ECR plasma (< 50 eV) [53]. Moreover, H radicals of the plasma also have a major role in the formation of the structure. Although the deposition process is performed at low temperatures, ECR plasma has high concentrations of H radicals which promote the crystallinity of the structure. The strained regions between the crystallites cannot withstand the severe H radical etching, leading to the formation of a void volume.

Using high-density plasma deposition, uniform porous layers up to $1 \mu\text{m}$ can be realized on silicon wafers, glass and plastic substrates as well as metal foils. Increasing the plasma power lowers the void fraction of the layer and decreases the porosity. Similarly, increasing the substrate temperature also decreases the porosity. By controlling substrate temperature and microwave power, porosities between 25 and 90% can be achieved by this bottom-up method. The obtained porous silicon layers show luminescence in the red portion of the spectrum and are sensitive to water vapor.

3.14. Oblique-angle deposition

Porous amorphous silicon has been fabricated by oblique-angle deposition, aka glancing-angle deposition, using electron-beam evaporation [54, 55] or magnetron sputtering [56]. Oblique-angle deposition is performed by positioning the substrate at a steep angle with respect to the vapor flux in order to achieve geometric shadowing. As schematically shown in **Figure 17**, random growth fluctuation on the substrate surface produces shadow regions where incident vapor flux cannot reach. As deposition continues, areas of larger height variation preferentially grow. Hence, an array of oriented nanorods is formed leaving pores behind. By controlling the vapor flux incident angle during deposition, the porosity can be tailored [57]. The pores of the material realized by oblique-angle physical vapor evaporation techniques are

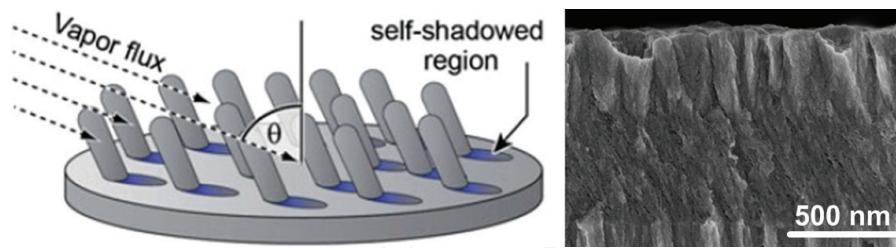


Figure 17. Schematic illustration of the oblique-angle deposition process and a cross-sectional SEM image of the obtained porous silicon layer [56, 57].

enclosed by the surrounding amorphous silicon matrix. Such structures spoil the available enormous surface area of porous silicon and restrict applications of the material. Indeed, this fabrication route has mainly been used to prepare antireflection coatings in solar cells.

3.15. Unidirectional solidification of molten silicon

Another method for realization of porous silicon is unidirectional solidification of molten silicon in hydrogen ambient. As schematically illustrated in **Figure 18**, high-purity silicon pieces are placed in an alumina crucible and inductively heated in the hydrogen atmosphere. The setup is then tilted and the molten is poured into a specifically designed mold [58]. The sidewalls of the mold are made of molybdenum and its bottom is made of copper which can be cooled down by circulated water. Due to the significant difference of thermal conductivities and heat capacities of the sidewalls and the bottom of the mold, unidirectional solidification can take place in the vertical direction. Both melting and solidification steps were performed in a constant pressure of hydrogen. It is believed that hydrogen dissolves in the molten and generates pores during solidification. Porosity and average pore size of the ingot change from 10 to 34% and 100 to 300 μm , respectively, depending on the hydrogen pressure alteration from 1 to 0.1 MPa.

Using unidirectional solidification of molten silicon in hydrogen atmosphere, porous cylindrical silicon ingots, 25 mm in diameter and about 30 mm in height, with elongated spheroidal “lotus-type” pores have been fabricated (**Figure 19**). The average pore size in the obtained ingots is at least two orders of magnitude greater than that of porous silicon structures realized by other fabrication routes.

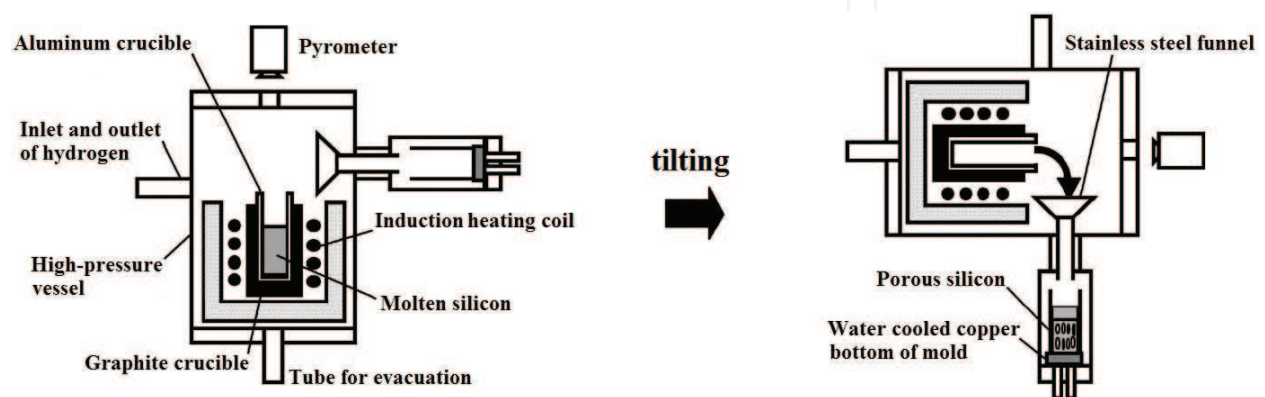


Figure 18. Setup used for preparation of porous silicon by unidirectional solidification of molten silicon [58].

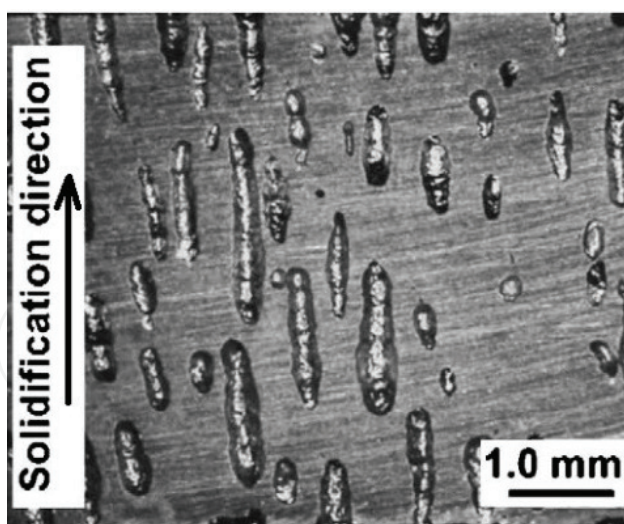
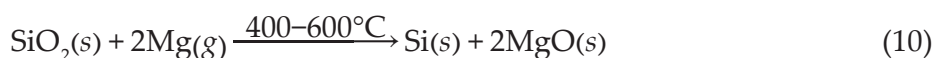


Figure 19. Cross-sectional SEM micrograph of a typical porous silicon ingot prepared by unidirectional solidification of molten silicon [58].

3.16. Porous silica reduction

Reduction of porous silica is another bottom-up route to synthesize porous silicon structures [59, 60]. This preparation method is utilized when inexpensive products are required as low-cost silica feedstocks like sand, living plants, and agricultural wastes can be used. As silica reduction generally occurs by magnesium vapor at moderate temperatures, this fabrication process is called magnesiothermic reduction of silica (Eq. (10)).



However, the reduction can also take place using other reducing agents, e.g., lithium, sodium, aluminum, and calcium [61–64]. The reaction pathway of Eq. (10) is then followed by acid leaching to remove the metal oxide byproduct and obtain porous silicon. The pore size and morphology of the synthesized porous silicon strongly depends upon morphology and moisture content of the feedstock, thermal budget of the process, and byproduct size distribution. In addition to metallothermic porous silica reduction, porous silicon synthesis has also been performed by mechanochemical reduction of SiO powder [60].

Porous silica reduction is a simple route for the realization of porous silicon. All classes of porosity can be achieved by this method. However, it is important to precisely control the process to prevent formation of magnesium silicate instead of silicon. Sintering and reintroduction of oxygen, especially in highly porous products, are also issues [63, 65].

3.17. Dealloying

Using dealloying of Al-Si eutectic system, thin layers of mesoporous silicon with ultrahigh density of cylindrical pores with an average diameter of 5 to 13 nm have been realized [66]. The Al-Si system is deposited by sputtering of an $\text{Al}_{0.56}\text{Si}_{0.44}$ target with Ar pressure of 0.1 Torr at low temperatures (below 100°C). Cylindrical pores are generated as a result of combination of nanoscale phase separation of the Al-Si system during deposition and subsequent removal of Al cylinders

by chemical etching. Indeed, by appropriate choosing of deposition parameters, especially the deposition rate, it is possible to control the structural development of Al-Si system that occurs at the surface during the film growth at low temperatures. Accordingly, by controlling the nanoscale phase separation through deposition parameters, Fukutani et al. have successfully fabricated Al nanocylinders surrounded by an amorphous silicon matrix [66]. Removing the Al cylinders by immersing the specimen in concentrated sulfuric acid solution for 24 h, a porous amorphous silicon layer with cylindrical pores is obtained (**Figure 20**). A subsequent annealing step at 800°C in H₂ atmosphere for 1 h crystallizes the porous material without any visible alteration in the average size and density of the pores [67]. Further studies are needed to determine the controllability over the shape and orientation of the pores generated by this method.

3.18. Laser-induced silane decomposition

Laser-induced decomposition of silane has been used to prepare high porosity mesoporous structures composed of silicon nanocrystals [68]. Nanocrystals have been synthesized by pulsed CO₂ laser-induced decomposition of SiH₄ in a complex apparatus illustrated in **Figure 21**. The setup consists of three vacuum chambers: a source chamber containing the flow reactor, a differential chamber encasing the chopper for size selection, and an ultrahigh vacuum (UHV) chamber that contains the time-of-flight mass spectrometer. The “source chamber” is indeed a laser-driven CVD reactor where silicon clusters are produced by pulsed CO₂ laser pyrolysis of SiH₄. The reaction products are extracted perpendicularly to both the gas flow and the CO₂ laser beam through a conical nozzle projected into the reaction zone. The extracted nanocrystals are then skimmed into a low-pressure vacuum chamber (differential chamber); they form a “molecular beam” of non-interacting clusters. The beam passes through the slits of a rotating chopper, synchronized with the pulsed pyrolysis laser and can be vertically moved from outside. The chopper is used to preselect a small portion of the initially broad cluster pulse to narrow the cluster size distribution. Immediately behind the chopper, is a sample holder that can be moved into the cluster beam to collect the nanocrystals. Thus, silicon particles with preselected size can be deposited on the substrate. If the sample holder is moved out of the path of the beam, the silicon nanoparticles enter the UHV detector chamber equipped with a time-of-flight mass spectrometer [68, 69]. Pores are automatically formed when nanocrystals are collected by the substrate. This fabrication route has not attracted much attention due to the complexity of the apparatus and poor adhesion of the porous layer.

3.19. Electrodeposition

Porous silicon structures can also be synthesized by galvanic deposition, also known as immersion plating. Addition of sodium hexafluorosilicate Na₂SiF₆ to dilute hydrofluoric acid concen-

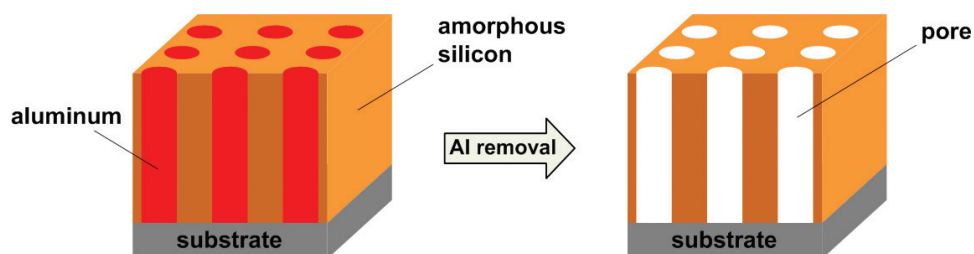


Figure 20. Fabrication of cylindrical pores by dealloying of Al-Si eutectic system and subsequent Al removal (The porous amorphous silicon structure can be crystallized by performing a thermal annealing process.) [67].

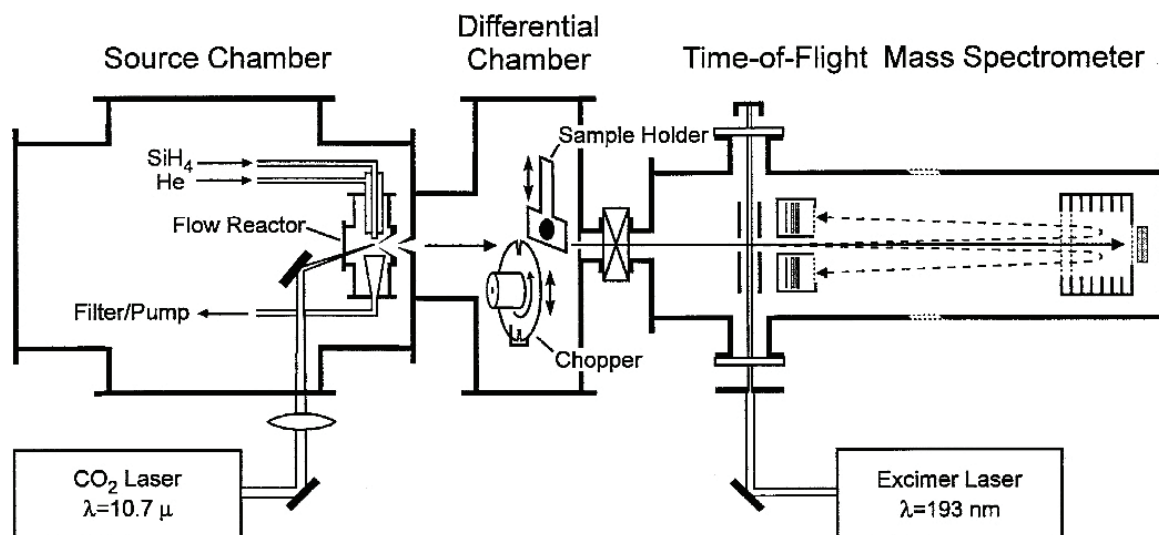
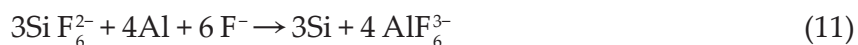


Figure 21. Schematic illustration of the apparatus used for realization of porous silicon layers by laser-induced decomposition of silane [69].

trated with nitric acid solution leads to galvanic deposition of mesoporous silicon layers on metallic substrates like pure aluminum or aluminum alloy [70]. The reaction pathway of this electrodeposition process is as follows:



in which aluminum reduces Si F_6^{2-} to silicon and forms a porous film on the substrate surface. The obtained porous layer has an amorphous structure with pore sizes between 3 and 8 nm [70]. In addition to the limited pore size achievable by electrodeposition, this bottom-up synthesis has a slow rate. Indeed, a 12- μm -thick layer is grown in 6 h. Additionally, the layer has a poor adhesion to the substrate.

3.20. Mechanical synthesis

Porous silicon structures can also be formed by compacting and sintering of silicon powder [71]. This fabrication method usually consists of a top-down stage in which silicon powder is formed and a bottom-up pressing process followed by sintering. Silicon powder is usually synthesized by grinding monocrystalline silicon wafers or polycrystalline silicon pieces by a high-energy ball mill. The milling reactor and balls can be made of either hardened steel or ceramic materials. The duration of the milling process might vary from several minutes to a few days depending on the desired particle size, degree of amorphization, agglomeration, and stress of the synthesized powder. Although high-energy ball milling is now extensively used to prepare silicon powder, the material can also be synthesized by precipitation of silicon from silane, especially when high purity powder is required [72]. Silicon powder is then pressed so that a porous green body is formed. The typical compaction pressure varies between 50 and 1000 MPa and uniaxial or isostatic pressing can be applied [73]. As milling and pressing stages generate highly defective silicon matrix, high-temperature treatment is necessary to release the strain and remove the defects. This high-temperature treatment also promotes a transition from amorphous to crystalline structure. The following sintering stage leads to porous matrices with

typical porosities up to 30%. The limited porosity is the inevitable consequence of the pressure and high temperature of the sintering stage. Indeed, as sintering enhances the strength and density of the material, porosity significantly decreases. However, it is possible to further increase the porosity of the sinter by performing an extra stage of electrochemical or stain etching [73].

All classes of porosity can be realized by mechanical synthesis. Porosity of the sinter can be tailored by tuning compaction pressure and sintering temperature. The method is capable of forming large porous silicon matrices which is impossible by top-down fabrication routes [74]. However, in addition to the limited porosity, lack of control over the morphology of the pores is the main disadvantage of mechanical synthesis. Moreover, high defect density and a great number of impurities of the mechanically made matrix are also important issues. The high compressive stress during ball-powder-ball collisions in the ball milling stage changes the Si–Si bond length, inflicts amorphization, and introduces a great number of defects [75]. Although the structure recrystallizes and most defects are removed during high-temperature treatment, the final product has still significantly higher density of defects and unwanted impurities in comparison to other porous silicon fabrication methods.

3.21. Annealing of ultrathin films of amorphous silicon

Ultrathin low porosity silicon membranes can be fabricated by rapid thermal annealing of predeposited ultrathin amorphous silicon layers [76]. The fabrication process is schematically shown in **Figure 22**. It starts with thermal oxidation in which 500 nm layers of SiO₂ are grown on both sides of the wafer. These oxide layers are not required for porous silicon formation and grown so that the membrane can be realized. After removing the front-side and patterning the back-side oxide layers, a three layer stack of 20 nm SiO₂/15 nm amorphous silicon/20 nm SiO₂ is deposited on the front-side of the wafer. The structure is then placed in a rapid thermal annealing setup and exposed to high temperature (770°C) for 30 s. As a result

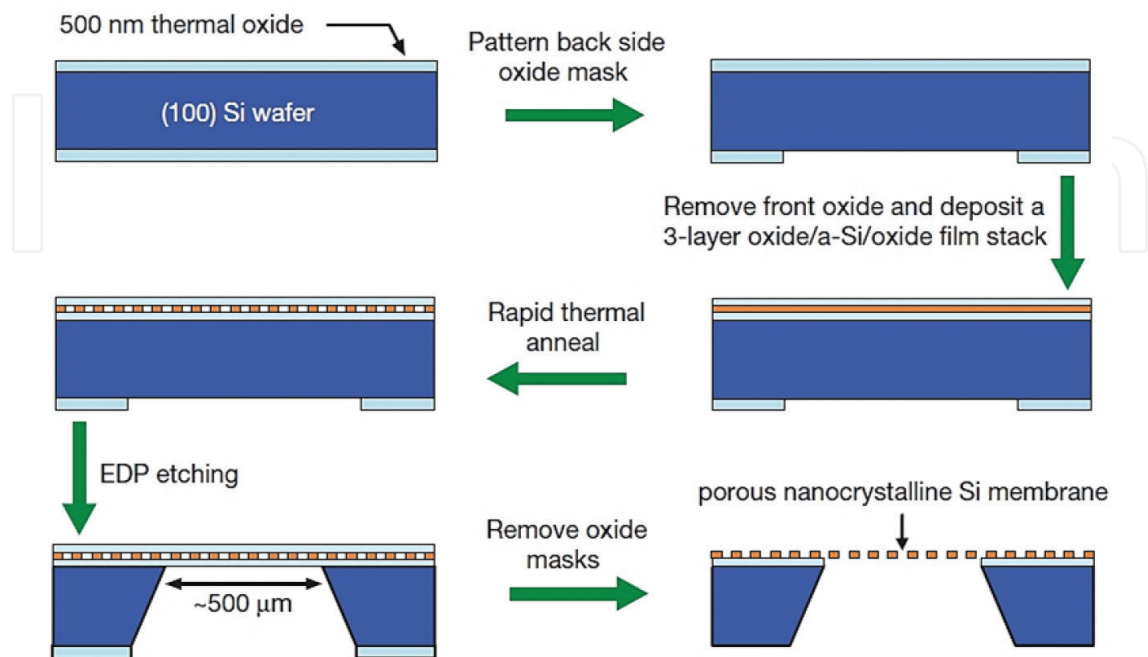


Figure 22. Fabrication process of porous nanocrystalline silicon membranes for ultrafiltration [76].

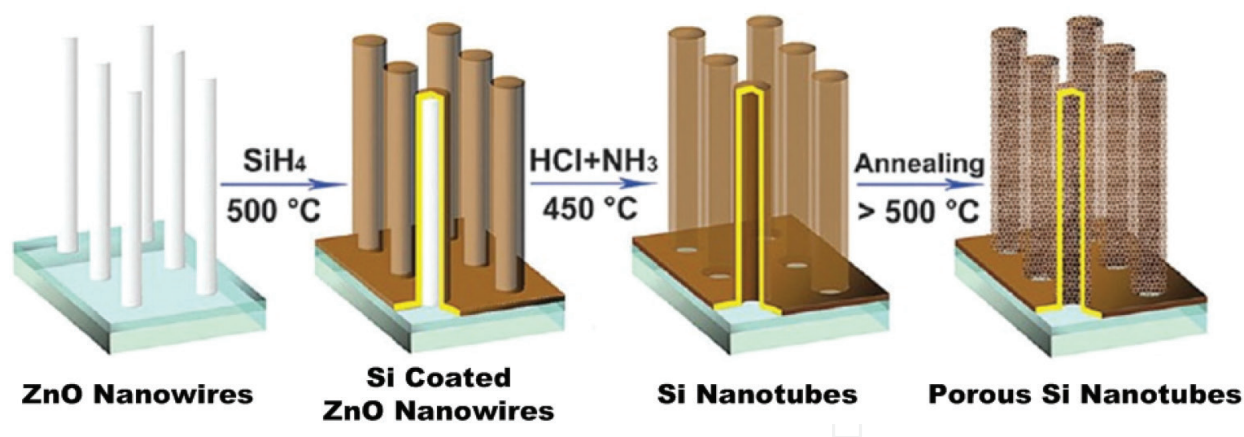


Figure 23. Fabrication of porous silicon nanotubes by using ZnO nanowire templates [77].

of high temperature annealing, nanocrystals nucleate leaving voids behind. Then, the voids span the molecularly thin membrane to create pores. Finally, the membrane is fabricated by anisotropic etching of the back-side of the wafer with ethylenediamine pyrocatechol (EDP) and removal of the protecting oxide layers. This method can only be used for the fabrication of ultrathin layers of porous silicon which is applicable for ultrafiltration. The porosity of the layers cannot exceed 7% and the pore sizes ranges only between 5 and 55 nm.

3.22. Using sacrificial template

As depicted in **Figure 23**, firstly, an array of ZnO nanowires is grown on the substrate. The specimen is then placed in a CVD reactor in which silane is used to form a silicon coating around the ZnO nanowires. The thickness of the over-coating silicon shell, which can be determined by the duration of the silane exposure, is extremely crucial for the formation of porous silicon. Indeed, only silicon sidewall thicknesses of about 12 nm or less finally lead to porous nanotubes. The temperature of the CVD process determines the crystallinity of the silicon over-coating layer. Deposition at 500°C results in amorphous silicon, while formation of crystalline shells requires at least 600°C. In order to remove the ZnO template and form silicon nanotubes, the sample is heated up to 450°C at the presence of ammonium chloride NH_4Cl . Ammonium chloride sublimates and decomposes into ammonia and hydrogen chloride gas. The latter reacts with ZnO creating ZnCl_2 liquid which is then converted into zinc amide species in the presence of ammonia. If the sidewall would be less than 12 nm, a further thermal annealing process porosifies the nanotubes. Porosification has been attributed to a strain-influenced mechanism [77]. The pore sizes of the obtained structure ranges from 5 to 10 nm. These porous nanotubes can be used for therapeutic applications due to their solubility in water at room temperature.

4. Applications

Due to its high chemical reactivity and rapid oxidation, porous silicon was being utilized for device isolation. By the end of the 1980s, porous silicon had also been used for other purposes like the realization of SOI substrates and the formation of a buffer layer in epitaxial growth of compound semiconductors on silicon substrates. However, it was only after the discovery of

strong photoluminescence in porous silicon that the material attracted broad attention. Since then porous silicon has been used for the fabrication of gas sensors, humidity sensors, biosensors, light emitting structures, optical waveguides, distributed Bragg reflectors, Fabry-Pérot resonators, photonic crystals, flat panel displays, optical and acoustic filters, ultrasound generators, and many other devices. Even though optoelectronics has remained the main research area of porous silicon, recently, the material has found application in other areas like medicine, diagnostics, cosmetics, consumer care, and nutrition. In contrast to the conventional chip-based applications, these new areas rely on porous silicon powders and independent structures. In this section, we briefly discuss the application domains of porous silicon and the reader is encouraged to refer to the literature dedicated to porous silicon applications (for example, see [78]).

4.1. Optic and optoelectronic applications

Since Canham's report on strong photoluminescence in porous silicon at room temperature in 1990 [79], the material has attracted broad attention. Indeed, most of the knowledge we now have about this material is due to the interest arose from this observation. Although bulk silicon is a poor emitter of light due to its indirect bandgap, quantum confinement effect makes radiative transition possible in porous silicon. Accordingly, light emitting devices, luminescing in the infrared, visible, and ultraviolet part of the spectrum have been fabricated. There has also been success in integrating porous silicon LEDs with electronic components offering hope for the realization of silicon-based monolithic optoelectronic integrated circuits.

Several optical components have also been realized by porous silicon. For instance, optical waveguides have been prepared using alternating low porosity and high porosity porous silicon layers. In such a structure, light would be trapped inside the low porosity layer which has a higher refractive index in comparison to the adjacent low refractive index layers due to total internal reflection. Based upon the thickness and refractive indices of the layers, the waveguide would support up to several number of propagating modes. Although the light is guided inside the low porosity layer, decaying fields existed in the adjacent layers facilitate coupling of light into and out of the waveguide. Photonic crystals, optical resonators, and diffraction gratings are among other optical applications of porous silicon.

4.2. Electronic applications

Gas sensing, gettering, lithium-ion batteries, and solar cells antireflection coatings are the main application areas of porous silicon in the field of electronics. The large amount of surface area makes porous silicon a promising candidate for realization of gas sensors. Almost a dozen structures have been proposed for porous silicon gas sensors based on alteration of the electrical and optical characteristics of the material in presence of more than 50 chemical species. Porous silicon has also been utilized as an anode in lithium-ion batteries. These anodes not only have more capacity than conventional anodes used in lithium-ion batteries but also are devoid of mechanical instability due to the expansion/contraction problem of bulk silicon with lithiation and delithiation process. Another electronic application area of porous silicon is gettering, i.e., deportation of impurities from active regions of the electronic devices. The great deal of surface area in porous silicon absorbs the impurities and makes the material suitable as a getter medium. Finally, porous silicon is an appropriate candidate to be used as antireflection coatings in solar cells due to its tunable refractive index.

4.3. Medical and diagnostics applications

Both chip-based and independent porous silicon structures have been utilized for medical and diagnostics applications. Biosensors have been realized to detect proteins, enzymes, and antibodies. For instance, porous silicon has been used to measure the prostate-specific antigen (PSA) in order to diagnose prostate cancer. Brachytherapy, insertion of radioactive implants directly into the target tissue, has also used this material to treat cancer. In this technique a medical radioisotope is placed in a porous silicon capsule and injected into the tissue requiring destruction. Meanwhile, biodegradable porous silicon is under preclinical test for drug delivery. The material's tunable pore size and modifiable surface chemistry make tunable drug load and release possible and therefore put porous silicon forward as a potential candidate for this carrier technology. Finally, porous silicon can be considered for tissue engineering due to its desirable properties. In this regenerative medicine, a temporary biodegradable scaffold is implanted in the body so that the tissue could heal itself around it. Accordingly, the scaffold should be made from a biocompatible material that could be easily synthesized, formed and controllably dissolved.

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