Chapter 10

Copper Metal for Semiconductor Interconnects

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Additional information is available at the end of the chapter

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Abstract

Resistance-capacitance (*RC*) delay produced by the interconnects limits the speed of the integrated circuits from 0.25 mm technology node. Copper (Cu) had been used to replace aluminum (Al) as an interconnecting conductor in order to reduce the resistance. In this chapter, the deposition method of Cu films and the interconnect fabrication with Cu metallization are introduced. The resulting integration and reliability challenges are addressed as well.

Keywords: Cu interconnects, BEOL, damascene, resistivity, reliability

1. Introduction

During the last about 50 years, Si-based integrated circuits (ICs) have been developed with numerous applications in the computer, communication, and consumer electronics industries. There has also been tremendous progress in the manufacturing of ICs over the past 60 years. The minimum feature size has advanced from 10 μm down to 10 nm, the cost per transistor has decreased by seven orders of magnitude, and the maximum number of transistors per chip has increased by at least 10 orders of magnitude [1]. Generally, technology node advances every 2 years with the shrinkage of the feature size by 0.7 times. Hence, the area of IC chip can be approximately reduced by 50%, resulting in doubling of the IC chips produced in a fixed area.

The main purpose of continuous scaling of the device dimensions is to improve the performance of the semiconductor microprocessors and to pack more devices in the same area. However, as the technology node is advanced to 0.25 μm, the back-end-of-line (BEOL) interconnect of ICs becomes the bottleneck in the improvement of IC performance [2]. In other words, as the feature size of ICs is continuously scaling down, the speed of the device increases due to a shorter channel length, although, resistance-capacitance (*RC*) delay produced by the interconnects

limits the chip speed. This *RC* delay is the product of the dielectric capacitance (*C*) and the conductor resistance (*R*), which can be calculated according to Eqs. (1) and (2), respectively.

$$C = k\frac{LT}{S} \tag{1}$$

$$R = \rho\frac{L}{WT} \tag{2}$$

where k is dielectric constant and ρ is metal resistivity. L, W, and T are the length, width, and thickness of metal line, respectively. S is the spacing between metal lines.

Table 1 provides the estimated critical dimensions of the BEOL interconnect from 90 to 7 nm technology nodes. As shown, with the advance of the technology node, the smaller line width and pitch result in the increased resistance of the metal lines and the increased capacitance between the neighboring metal lines. This leads to a larger *RC* delay in the advanced technology nodes, which surpasses the gate delay and becomes a limiting factor in ICs performance [3–6].

In order to slow down the increase of *RC* delay, the possible solution is to change the materials used in the BEOL interconnects. A dielectric film with the relative dielectric constant (k) lower than 4.0 (called low-k) had replaced a conventional chemical vapor deposition (CVD)-SiO_2 film with a k value of 4.0 as an interconnect insulator because it can provide lower capacitance between the neighboring metal lines. The low-k materials currently used in the BEOL interconnects are SiOF (k = 3.5–3.8), SiCOH (k = 2.2–3.2), or air gap (k~1.0) [7–11]. On the other hand, to reduce the resistance of BEOL interconnects, a metal material with a lower resistivity (ρ) than that of aluminum (Al), which is the traditional conductor used in 3.0–0.25 μm technology nodes, is considered to be a candidate to replace Al conductor. **Table 2** lists the electrical resistivity for different metals. Among all metals in the world, three kinds of metal have lower resistivity than Al with a resistivity of 2.65 Ωμ-cm: Gold (Au; 2.214 Ωμ cm), copper (Cu; 1.678 Ωμ cm), and silver (Ag: 1.587 Ωμ cm). Compared with these three metals, Cu has been recognized to be a candidate as a conductor in the BEOL interconnects for integration consideration. Additionally, higher electromigration reliability than Al by at least 10 times is another advantage for Cu as a conductor because Cu has a lower diffusivity than Al. Based on these reasons, semiconductor industries are fully transitioning toward using Cu instead of Al in future IC applications [12–15].

In this connection, this chapter is an attempt to provide an overview of Cu conductor used in the BEOL interconnects of ICs in the past, present, and future. This chapter is organized as

Technology node		Critical dimension (nm)								
		130	90	65	45	32	22	14	10	7
Interconnect	Pitch	400	280	200	126	104	88	56	40	28
	Width	200	140	100	63	52	44	28	20	14

Table 1. Interconnect dimensions with technology nodes.

Metal	Melting point (°C)	Resistivity (ρ) at 298K (μΩ-cm)
Silver (Ag)	961	1.587
Copper (Cu)	1084	1.678
Gold (Au)	1064	2.214
Aluminum (Al)	660	2.650
Tungston (W)	3422	5.280

Table 2. Melting point and resistivity of different metals.

follows: in Section 2, we describe the process flow of Cu damascene metallization. Then, in Section 3, the deposition methods of Cu metal are introduced and compared. Next, the integration and reliability issues of Cu metallization are discussed in Sections 4 and 5, respectively. Finally, short conclusion and future trend for conductors used in the BEOL interconnects are provided in Section 6.

2. Copper damascene metallization

Unlike Al metallization, Cu cannot be easily patterned by reactive ion etching (RIE) due to the low volatility of Cu etching by-products, such as Cu chlorides and Cu fluorides [16, 17]. Hence, to fabricate Cu interconnects, a different process flow which is called "damascene" process has been developed, including "single damascene" and "dual damascene" processes [18–23]. In the "single damascene" process, only trench or via is fabricated after completing the process. While in the dual damascene process, both via and trench can be fabricated simultaneously, in which both via and trench can be performed with the same metallization step. Thus, Cu interconnects are usually fabricated by cost-effective dual damascene technology.

In order to fabricate Cu dual damascene interconnects, various process flows were developed. "Via first" and "Trench first" dual damascene processes are commonly used, as plotted in **Figure 1**.

The process flow of Cu dual damascene metallization is described as below: After processing of Metal-1 (M-1), the etching stop layer (Cu barrier dielectric layer) and the Via-1 (V-1)/Metal-2 (M-2) dielectric layer (e.g., SiCOH low-*k*) are subsequently deposited. For the etching stop layer, also called Cu barrier dielectric layer, SiN or SiCN can be used, providing functions to protect Cu from oxidation and protect Cu from diffusion into the low-*k* dielectric during processing or device operation. These materials have much higher dielectric constants than that of the low-*k* dielectric. The dielectric constant of SiN film ranges from 6.8 to 7.3 and that of SiCN layer from 4.0 to 5.0, depending on the process conditions [24–26]. Sometimes, a sandwich dielectric stack film (SiCOH/Si(C)N/SiCOH) is used in order to control the depths of the

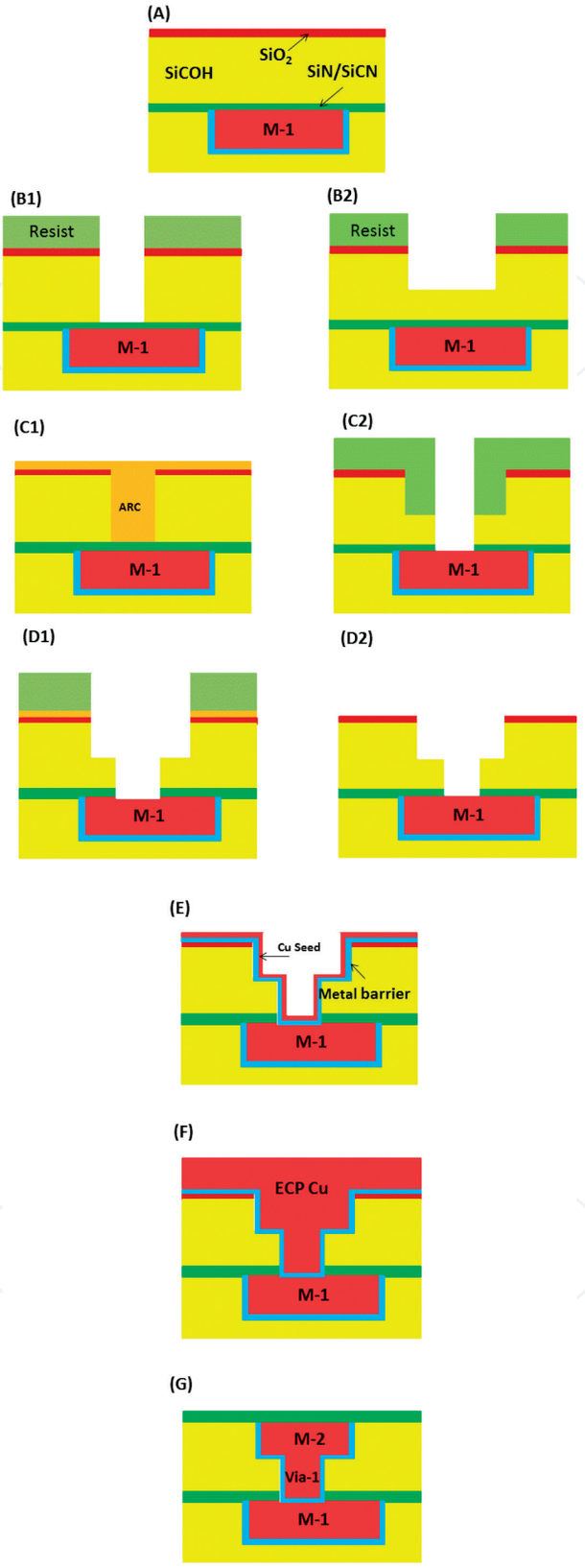

Figure 1. Via first (B1–D1) and Trench first (B2–D2) approaches for dual damascene patterning. (A) Dielectrics (SiN/SiCN, SiCOH, SiO_2) deposition; (B1) Via-1 lithography and RIE; (B2) M-2 trench lithography and RIE; (C1) ARC plug; (C2) Via-1 lithography; (D1) M-2 trench lithography and RIE and etching stop layer opening; (D2) Via-1 RIE; (E) metal barrier and Cu seed deposition; (F) electroplating Cu deposition; and (G) Cu CMP and dielectric barrier deposition.

via and metal precisely. These steps will increase the effective dielectric constant, raising the capacitance. The dense SiO_2 layer can be capped onto the SiCOH low-*k* dielectric to mitigate damage on the low-*k* dielectric caused by the subsequent process steps, such as photoresist, and Cu chemical mechanical polishing (CMP). This layer will not appear in the final structure of the fabricated Cu interconnects because it can be removed by Cu CMP process.

For "Via first" process, Via-1 is patterned first, stopping on the SiN (or SiCN) layer that protects Cu from oxidation. Then, the Metal-2 trench is patterned and the final step is the removal of the SiN (or SiCN) etch stop from the bottom of the via. For the "Trench first" process, the "via patterning" and "trench pattering" steps are reversed.

The metal deposition in the dual damascene structure consists of three steps: Cu barrier layer, Cu seed layer, and bulk Cu layer. Currently, the first two steps are performed by sputtering and the last step uses Cu electroplating (ECP) method. The used material for Cu barrier layer is a TaN/Ta barrier layer, which prevents Cu from diffusing into the dielectric, A Cu seed layer helps to the growth of electroplated Cu film. Cu electroplating provides to fill in the via and trench. After completing the metal deposition, Cu chemical mechanical polishing (CMP) process is used to remove the excess metal over the field regions. Thus, a layer of Cu dual damascene structure (via and trench) is finished. To construct multiple metal levels, these steps are repeated for each metal level. After the last metal layer is fabricated, thick dielectric passivation layer (e.g., SiO_2/SiN bi-layer) is deposited and via is opened to the bond pads.

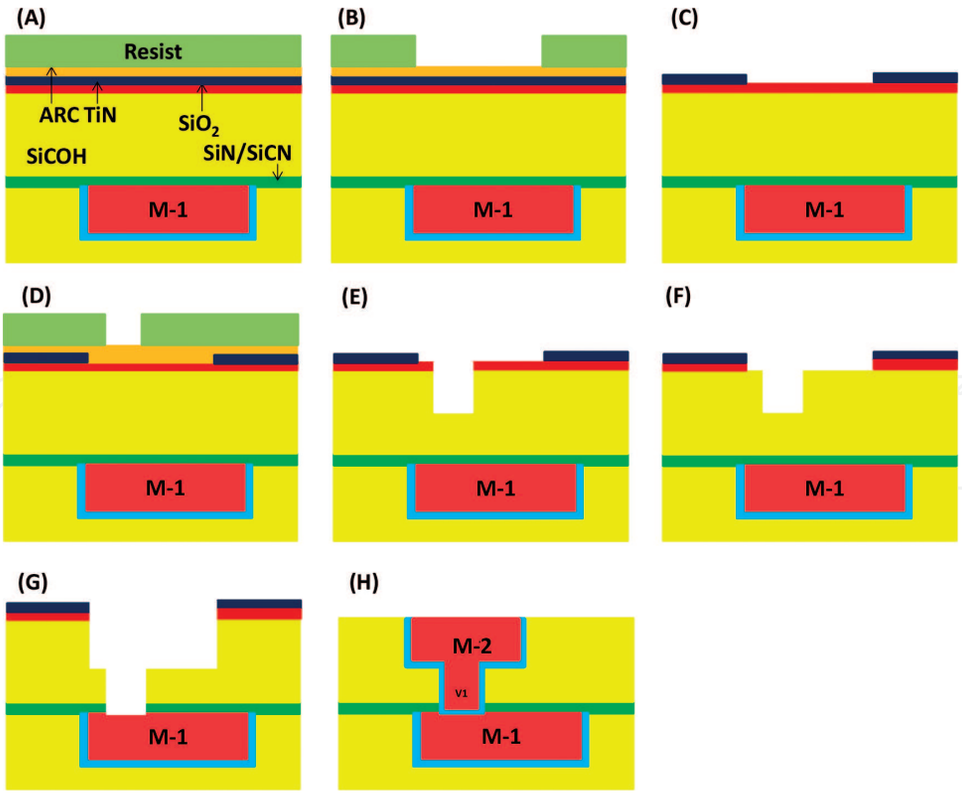

Figure 2. Metal hardmask approach for dual damascene patterning. (A) TiN, ARC, and resist deposition; (B) M-2 metal hardmask RIE; (C) M-2 trench lithography; (D) Via-1 lithography; (E) Via-1 RIE; (F) M-2 oxide hardmask RIE; (G) M-2/Via-1 RIE and M-1 capping layer RIE; and (H) M-2/Via-1 Cu metallization.

Further reduction of the capacitance between the meal conductors is required as the device dimensions are continuously scaled down. The porous low-*k* material with a dielectric constant as low as 2.2 is adopted as an interconnect insulator [9]. The porous low-*k* material can be produced by adding pores (<2 nm diameter) to the SiCOH film. The obtained dielectric constant depends on the porosity. A higher porosity results in a lower dielectric constant; however, open pore are formed (high pore connectivity). The open pore in the porous low-*k* film allows water and other contaminations to diffuse into the dielectric. Moreover, during the interconnect fabrication, the porous low-*k* material is exposed to oxygen plasma environments in the conventional resist strip step. Ions and radicals produced from oxygen plasmas can severely damage the porous low-*k* material. These issues result in an increased dielectric constant and degraded dielectric breakdown reliability for the porous low-*k* material. To minimize the damage on the porous low-*k* material, low-*k* material optimization and resist strip condition are chosen, and the process integration modification has been provided. The integration approach for dual damascene patterning is transformed to "metal hardmask" method from 32 nm technology node as shown in **Figure 2** [27]. In the metal hardmask method, the resist strip damage on the porous low-*k* material can be minimized because the resist is stripped prior to the trench and via etching. However, this method requires the extra steps and good process control to avoid the integration issues.

3. Copper deposition method

In addition to the need of lower resistivity, the other requirement for Cu film is to fill the high aspect ratio vias and trenches without voids in the dual damascene structure. After continuous research and development for many years, Cu film can now be deposited by various technologies, such as physical vapor deposition (PVD), chemical vapor deposition (CVD), laser reflow, atomic layer deposition (ALD), and plating (electrolytic and electroless) [28–33]. **Table 3** lists the properties of Cu films obtained by different deposition technologies. Evaporation and

Deposition method	CVD	PVD (Evaporation)	PVD (Sputtering)	Laser reflow	ALD	Electroplating (ECP)	Electroless plating
Resistivity (μΩ-cm at RT)	> 2	1.80~2.2	1.75~2.0	~2.5	> 2	~2	~ 2
Impurities	C, O	O	Ar	---	C, O	---	---
Deposition rate (nm/min)	100~150	> 200	>100	---	<10	~200	~ 100
Deposition temperature (°C)	150~250	melt	RT	melt	100~200	RT	50~80
Step coverage	Good	Fair~Poor	Fair	---	Excellent	Good	Good
Via-filling capbility	Good	Poor	Poor	Goog	Excellent	Fair	Fair
Enviromental impact	Good	Good	Good	Good	Good	Poor	Poor
Cost	High	Low	High	High	High	Fair	Fair
RT: Room temperature (25°C)							

Table 3. Comparison of various Cu deposition technologies.

sputtering methods belong to PVD technology, which can provide a lower resistivity as compared to other technologies. The latter method is widely used in the semiconductor industry.

In current Cu metallization, electroplating method is used to fill the high aspect ratio via and trench in the dual damascene structure. However, in order to successfully deposit Cu film during ECP process, a Cu seed layer is needed. Sputtering deposition is the preferred method to deposit the Cu seed layer because it can produce high-purity films. In the sputtering process to deposit Cu film, Ar plasma is used to sputter Cu target and then the sputtering Cu material is deposition on the wafer. The biggest challenge for Cu sputtering process is to achieve good step coverage in the high aspect ratio via and trench. With the reduction of interconnect dimensions in the advanced technology nodes, this problem is becoming thrilling. To achieve adequate conformity in high aspect ratio via and trench in the dual damascene structure for advanced technology nodes, ionized PVD [34] or atomic layer deposition (ALD) [35] technologies have been developed for Cu seed layer deposition with demonstrated good step-coverage.

After depositing a Cu seed layer, ECP process is used to fill-in via and trench dual damascene structure. ECP process is performed by immersing the wafers in a solution containing cupric ions, sulfuric acid, and trace organic additives [36]. By applying an electric current, Cu ion (Cu^{+2}) is reduced to Cu, which deposit onto the seed layer. To achieve void-free filling in the high aspect ratio feature for ECP process, the "bottom-up" or "super-filling" strategy is adopted. By means of the bottom-up (or super-filling) method, the deposition of Cu film is growing from the bottom to the top, so no void is formed in the via and trench. To meet this goal, the additives in the ECP solution play an important role. The additives must consist of both suppressors and accelerators. The former is polymers, such as polyethylene glycol, which reduce the plating rate at the top of features by blocking of growth sites on the Cu surface. While the latter is dimercaptopropane sulfonic acid (SPS) with sulfide and thiol-like functional groups, which enhance the plating rate at the bottom of features because the functional groups strongly absorb on Cu surfaces [36, 37]. Consequently, ECP process can provide a void-free filling process for via and trench dual damascene structure under an adequate combination of suppressor and accelerator additives.

4. Integration issues of copper metal

In the advance technology nodes, the critical dimensions of BEOL interconnects are continuously scaled down. Additionally, new materials (Cu and low-*k*) and a dual damascene process have been introduced. Furthermore, new technologies, such as electroplating and Cu CMP, have been used in the semiconductor fabrication line. Thus, more integration challenges are raised, as described below:

4.1. Width effect on resistivity of Cu

As the dimensions of Cu interconnects are reduced, the resistivity increases dramatically due to grain boundary scattering, surface scattering, and an increasing fraction of refractory metal liner in the trench (**Figure 3**) [38, 39].

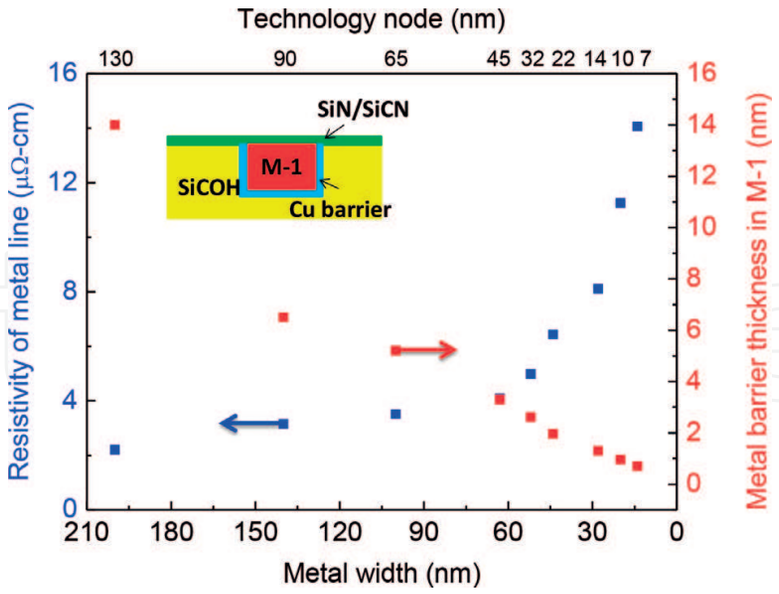

Figure 3. Resistivity of metal line and thickness of Cu barrier layer with technology nodes [40].

The first factor that increases the resistivity of the metal line is grain boundary scattering. The smaller gain size in Cu lines results in more grain boundaries, leading to an increased resistivity. Unfortunately, Cu gain size scales as the critical dimensions of the Cu line in dual damascene interconnect. It is difficult to achieve large grain size in narrow lines because grain growth of Cu in trenches is inhibited at small dimensions. Therefore, subtractive Cu method is the possible solution to increase the Cu grain size [41]. That is, Cu film is patterned by etching process. In such a case, Cu grain size would be much larger because Cu deposition is not restricted in the narrow lines. However, there remain many challenges to solve for etching of Cu including etching chemistry, hardmask, and hardware. Moreover, encapsulation of Cu line with barrier/liner materials is another issue to solve.

Surface scattering increases as the critical dimensions of the Cu line becomes smaller than the bulk mean free path of the electrons. To solve this issue, new material such as tungsten (W), silicides, carbon nanotube, or collective excitations could be an alternative to Cu as interconnects [42, 43]. Even though the bulk resistivity of W and silicide films is much larger than that of Cu film, the shorter mean free path of the electrons will lower the surface scattering effect. Another advantage of W interconnects is no-barrier process because the diffusivity of W metal is very low. The latter two materials (carbon nanotube and collective excitations) can provide a different conductance mechanism, but they are still in the research and development phase. Therefore, for these new conductor materials to successfully integrate into the semiconductor industry is a long way off.

As the dimensions of Cu interconnects are continuously scaled down for the advanced technology nodes, a larger fraction of the metal line cross-section is occupied by the refractory metal barrier film. The resistivity of the refractory metal barrier film is far larger than that of Cu metal. Therefore, the overall resistivity of the metal line is significantly increased. The direct strategy to reduce the resistance rise is to decrease the thickness of the metal barrier film. However, the accompanied problems are poor step coverage and Cu diffusion into the dielectric. The improved

sputtering method or atomic layer deposition method can be used to deposit a thinner liner layer [44–46]. The most promising method is to adopt a self-forming barrier process by depositing Mn-based film. The deposited Mn film can react with silicon-based dielectrics to form a self-forming dielectric barrier by annealing. A smooth MnO_x layer can be formed at Cu/dielectric film interface. This layer also provides a good adhesion for Cu film deposition. Furthermore, if this self-forming barrier process is controlled precisely, there is no barrier at the via bottom connecting the underlying metal line because of high diffusivity of Mn in Cu [47, 48]. This results in a lower via resistance and a better reliability for Cu interconnects.

4.2. Cu diffusion into the dielectric

Cu is easily diffused into the dielectric under a thermal and/or electric stress, causing a dielectric failure. For this reason, Cu film must be surrounded by a good diffusion barrier layer. Generally, the barrier layer in the sides and bottom of the Cu line is metal barrier film and is typically a TaN/Ta bilayer [49], while that on the top is dielectric barrier film, such as silicon nitride (SiN), silicon carbide (SiC), silicon carbonitride (SiCN), and silicon oxynitride (SiON) [24–26, 50, 51].

Both Ta and TaN are good Cu diffusion barrier layers. Besides, TaN can provide good adhesion to the dielectric, and Ta can provide a surface with good wettability of the Cu seed layer. Based on these characteristics, a TaN/Ta bilayer instead of a Ta/TaN bilayer is the best choice for a Cu diffusion barrier layer. Moreover, Ti-based and Ru-based barrier layers are alternatives to act as a Cu barrier layer for cost and resistivity consideration [52, 53]. However, the Cu barrier efficiency of Ti and Ru is not as good as that of Ta-based films. Therefore, a multilayer film of Ti/TiN/Ti is used as a Cu diffusion barrier layer; TiN can prevent excessive reaction between Ti and Cu, which can increase the resistivity of the wire. The top Ti layer can provide good wetting of Cu film because Cu wetting on TiN is very poor. Ru-based layer can provide a lower resistivity and a better Cu wettability than Ta layer; however, its Cu diffusion barrier is very poor. So, a TaN/Ru or Ti/Ru bilayer is used for Cu diffusion barrier [54–56].

The diffusion barrier layer on the top of Cu wires is typically a dielectric barrier film. However, its Cu barrier efficiency and adhesion ability with Cu film are poorer than those of a metal barrier layer. To address these issues, an extra metal layer (Ta/TaN or CoWP) is capped on the top surface of Cu wires before a dielectric barrier film deposition [57]. This extra process to deposit a metal layer is very challenging because of selectivity deposition on the Cu lines. However, control of this process can make a significant improvement on reliability for Cu interconnects if it is controlled precisely.

4.3. Cu oxidation

The other disadvantage for Cu interconnects is that Cu film can be oxidized during the water rinse and exposure to air. In addition to increasing the resistance of Cu wires, the formed Cu oxides cause reliability degradation due to the weakened adhesion at the Cu interfaces. During the fabrication of Cu dual damascene structure, there are two stages in which Cu film could be exposed to air. One stage is via-opening before Cu metallization deposition. The other stage is the completion of Cu CMP before a dielectric barrier layer deposition. Hence, to remove Cu

oxides and avoid Cu re-oxidation, an *in situ* clean is required. The mechanism to remove Cu oxides in clean process can be achieved by either physical removal or chemical reaction [58].

Ar sputtering clean to physically remove Cu oxides is a typical physical method. However, during Ar sputtering process, the corners of vias and trenches are chamfered and re-sputtering Cu atoms are trapped onto the sidewalls of the via [58]. The former phenomenon leads to an increased leakage current between the neighboring wires. The latter phenomenon results in strong degradation in dielectric reliability. Hence, the energy and time in the Ar sputtering clean process must be carefully controlled in order to alleviate these two phenomena. Moreover, a "barrier-first" process was provided to minimize the detrimental effects caused by Ar sputtering clean [59]. In this barrier-first process, a TaN layer is deposited first and Ar sputtering clean is then performed to etch through the TaN layer and the contamination at the bottom of the via. Finally, a Ta layer is deposited. Due to the presence of the TaN layer, the chamfering at the top corner of vias and trenches and the re-sputtered Cu atoms and contaminations into the dielectric can be effectively reduced during Ar sputtering clean process.

The chemical clean to remove Cu oxides can also minimize the detrimental effects caused by the Ar sputtering clean. The mechanism of chemical clean is based on the oxidation-reduction reaction. Hydrogen (H) atom is typically the reducing agent. Hence, H_2 or NH_3 is widely used reduction gas [60–62]. The chemical clean is processed under a plasma process, which increases the activity of the reaction. During chemical plasma clean process, Cu oxides can be reduced; however, the dielectric (e.g. low-*k*) is also exposure to a plasma environment. The dielectric is damaged by plasma irradiation. This leads to an increased dielectric constant and a reduced dielectric breakdown filed. Therefore, the drawback of using chemical plasma cleaning to remove Cu oxides is the plasma-induced damage on the dielectric (e.g. low-*k* damage). To minimize the damage on the dielectric and keep Cu oxide removal efficiency, a remote plasma technology has been proposed [63].

4.4. Cu chemical mechanical polishing

The chemical mechanical polishing (CMP) process has been used to polish oxide dielectric film and W plug in Al metallization since 0.35 μm technology node. As the BEOL interconnect was transferred to Cu metallization, due to the adoption of damascene structure, dielectrics do not needed to be polished by the CMP process. Instead, the excess Cu films in the damascene structure are necessary to be removed by CMP process. Cu CMP process can be regarded as a new technology and has a different consideration from oxide CMP process, hence, it is very challenging. During CMP process, the wafers are placed face-down on a rotating pad on which the slurry is dispensed, resulting in the removal of the film by chemical reaction and mechanical force. In Cu CMP process, the excess Cu film and metal barrier layer must be removed to fabricate Cu metallization. Typically, there are three main steps in Cu CMP process [64]. The first step is Cu film removal, stopping on the barrier layer. In this step, removal selectivity is not considered because only Cu film is polished. The second step is the barrier layer removal, stopping on the dielectric. During this step, both barrier layer and Cu film are polished. The last step is over-polishing to ensure that all metals are removed from the field regions in all parts of the wafer. Cu film, barrier layer, and the dielectric are polished simultaneously. In the

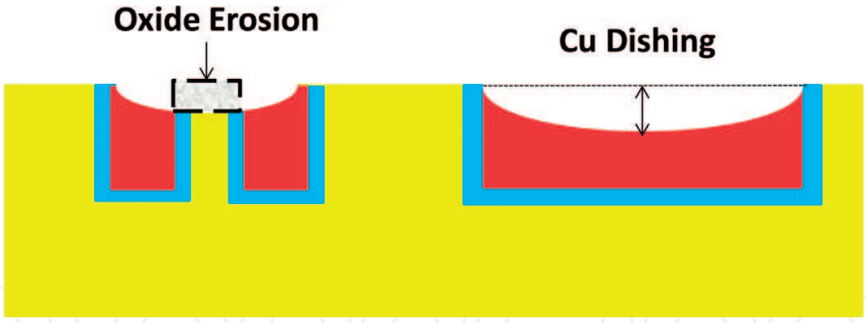

Figure 4. Side view schematic of Cu dishing and oxide erosion induced by the Cu CMP process.

last two steps, the selectivity should be considered because it is of importance to reach high-degreed planarization.

Cu dishing and oxide erosion as shown in **Figure 4** are the main problems associated with Cu CMP process [65–67]. As porous low-*k* dielectric films are used as the BEOL insulators to further reduce the capacitance between the metal lines, these two issues also become more severe. Therefore, the Cu CMP process is needed to be optimized. Since the formation mechanism of these two problems is due to the faster polish rate and lower selectivity in the slurry, reducing the down-force during Cu CMP process and/or optimizing the used slurry are feasible methods to minimize these effects.

Additionally, the pattern density of the Cu line also influences the performance of Cu CMP process. Generally, in the region of high Cu pattern density, the polishing rate is high and the thinning of the Cu line is observed due to a high polishing rate, resulting in a large variation in the resistance of the metal line. Thus, design rules to restrict the local Cu pattern density are provided for IC designers based on Cu CMP process [68]. Therefore, to reach high IC performance, inserting the dummy Cu lines to increase Cu pattern density is a general method to minimize the pattern effect of the Cu CMP process. Moreover, low downforce during the over-polish step in Cu CMP process is required to minimize this effect from the perspective of the process [69].

Moreover, cracks, delamination, scratching and contamination are the problems accompanied with Cu CMP process because the Cu CMP process is basically a frictional process. These problems can be solved through: (i) reducing the down-force during Cu CMP process; (ii) improving the adhesion between layers in the interconnect; (iii) optimizing the used slurry; (iv) depositing a relatively dense material, such as SiO_2 or nonporous SiCOH films on the top of the porous low-*k* dielectric film; and (v) performing an optimized wetting clean after the CMP process [70–72].

5. Reliability of copper metal

In the Cu interconnects, there are three main reliability items: electromigration (EM), stress-induced voiding (SIV), and time-dependent dielectric breakdown (TDDB) [18]. The first two items are used to assess metal reliability, while the last item is to evaluate dielectric reliability. However, all reliability items are related to each component of Cu interconnects.

5.1. Electromigration (EM)

The failure of interconnects through electromigration (EM) has been a long-standing concern for the development of highly reliable ICs. The first EM-related failure of Al-interconnect based circuit was observed in 1966 [73]. For the past 60 years, intense efforts have been made on either Al interconnects or the newly introduced Cu interconnects to enhance the resistance against EM.

The phenomenon of EM involves metal atoms migration in a metal conductor due to a stress with a high electrical current density (~10^5 A/cm) [74]. As an electric current is applied on a metal lead, the momentum transfer is occurred from the electrons to the metallic atoms, resulting in the migration of the metallic atoms. Therefore, the depletion and accumulation of the metallic atoms in a metal lead would be observed, which occur in the cathode and anode sides of a metal lead, respectively. As a lead is depleted at the cathode side, voids will form and the resistance will increase. If the voids grow large enough to spans the whole line, open line will be observed. At the anode end of the wire, metal atoms will accumulate, resulting in a hydrostatic stress. If the stress is high enough and the dielectrics are weak, metal extrusions may form, causing leakage between the neighboring metal lines [18, 75]. In Cu interconnects, the Ta/TaN barrier layers at the bottom of the via can act as blocking boundaries, which provide a higher EM resistance than Cu. Hence, during an EM stress, the depletion and accumulation phenomenon occur in the Cu line.

This stress produces a back flux of atoms that is opposite in the direction to the flux from electromigration, which is called the "Blech effect" or Short-length effect" [76–79]. This buildup stress causes a reverse migration process, which reduces or compensates for the effective metal material flow toward the anode side during EM. Thus, the EM failure time can be effectively improved. Moreover, this back-stress force becomes obvious as the length of the wire decreases. Therefore, the short wires that have a length below a critical threshold length (typically on the order of 5–50 μm), the back flux of atoms prevents killer voids from forming, and the wires are immortal.

To accelerate the fails and save the test time, the EM test is performed under a high-current density and a high-temperature condition. The failure time (t) of Cu line is widely described by using Black's equation [80, 81]:

$$t = Aj^{-n}\exp\left(\frac{E_a}{kT}\right) \tag{3}$$

where j is the current density, E_a is the activation energy for diffusion, k is the Boltzmann constant, T is the temperature, A is a constant, and n is the current exponent, which value is typically between 1 and 2. If n value is close to 1, the EM kinetics is dominated by void growth, whereas $n = 2$ corresponds to kinetics limited by void nucleation [82].

The activation energy for diffusion is varied by the different diffusional mechanisms as listed in **Table 4** [83]. Diffusion process caused by EM can be divided into bulk diffusion, grain boundary diffusion, surface diffusion, and interface diffusion. In Al and Cu interconnects, the

Metal	Activation Energy for different diffusion paths (eV)			
	Bulk	Grain boundary	Surface	Interface
Al	1.4	0.4~0.5	NA	---
Al/Cu (alloy)	1.2	0.6~0.7	NA	0.9~1.1
Cu	2.1	1.1~1.2	0.6~0.7	0.8~1.3

Table 4. Activation energy for different diffusion paths for Al, Al/Cu, and Cu metal.

activation energies for diffusion in different diffusion paths are different. In Cu interconnects, interface diffusion has the lowest activation energy, presenting the major path for EM. Whereas in Al interconnects, grain boundary diffusion is a fast EM path due to a lower activation energy [83–86].

In Cu metallization, the "line-via" structure is widely used for EM characterization. Two typical EM test structures: "downstream stressing" and "upstreaming stressing," as shown in **Figure 5**. In order to minimize the Blech effect on EM results, the length of the tested Cu line must be sufficiently long. Generally, the length is about 200–250 μm. During an EM test, the resistance is monitored with the stressing time. As the monitored resistance is increased by a certain value or a certain percentage, this time is defined as the EM failure time. Generally, 20–30 samples are tested for an EM test. The measured failure times are usually plotted using a log-normal distribution and analyzed [23].

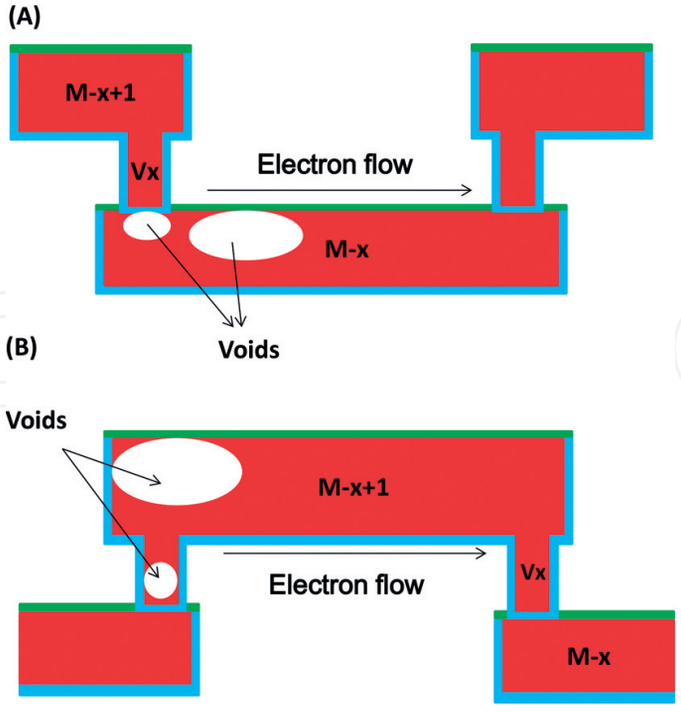

Figure 5. Side view schematic of electromigration test structures and void formation locations. (A) Downstream stressing structure and (B) upstream stressing structure.

In a "downstream stressing" test structure, electron flow is from metal-2 to metal-1 through Via-1. The EM-induced void will form under the via (early failure) and in the wire far from the via (late failure). In an "upstream stressing" test structure, electron flow is from metal-1 to metal-2 through Via-1. The EM-induced void will form inside the via (early failure) and in the wire (late failure). The early failure occurred in both test structures is related to via process or metal barrier deposition. The late failure is directly linked to Cu/dielectric interface or Cu line property. Therefore, to mitigate Cu EM phenomenon, these related processes are needed to be optimized.

Many factors, such as design related, process related, and environmental related factors, can significantly affect Cu EM reliability, as summarized below:

5.1.1. Scaling effect

As device and wire dimensions are reduced in the advanced technology nodes, it is desirable to increase the maximum required current density in Cu lines, thus a longer EM lifetime of Cu lines should be achieved [40]. **Figure 6** plots the maximum required current density at 105°C for Cu lines. The reason for this increase is that the drive current in the devices increases and the switching speed increases as the dimension of the device is scaling. Simultaneously, the dimension of the metal line is minimized. Hence, the metal line should sustain a higher current density.

The EM performance, however, could not be improved as the dimensions of Cu lines decrease. Actually, the EM lifetime decreases as shown in **Figure 7**. Two reasons can explain this result. First, as the dimensions of via and trench decreases, the void size required to cause a EM fail decreases accordingly [86]. This leads to a short time to form a "killer" void. The other reason is due to the grain size in Cu lines. Experimental results indicated that the grain size decreases with line width as the width of Cu lines is less than 0.2 μm. In Cu lines with the smaller grain

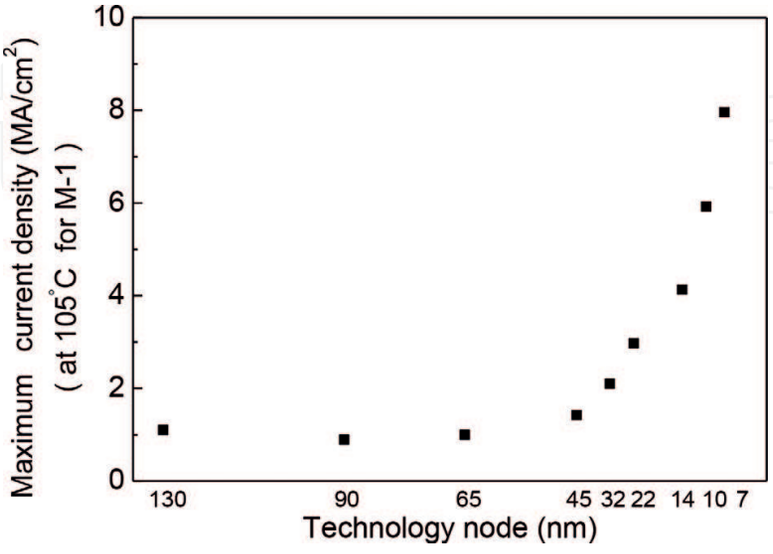

Figure 6. Maximum required current density at 105°C for M-1 Cu lines with technology nodes [40].

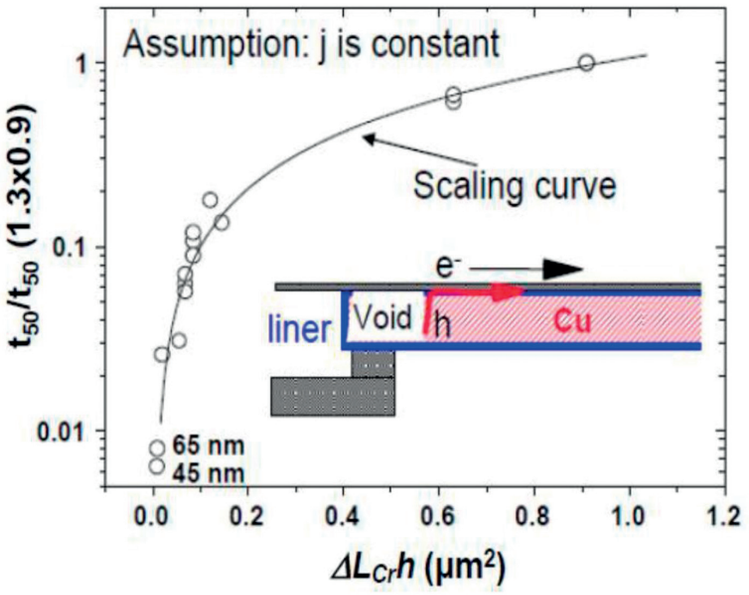

Figure 7. Experiment and model results of electromigration lifetime scaling with the reduction of interconnect dimension. Reproduced with permission from Ref. [86].

size, grain boundary diffusion can be significant during an EM stress, resulting in a lower EM lifetime [87].

For the advanced technology nodes, EM reliability is becoming a critical challenge due to a high EM requirement and a low EM performance. Therefore, a number of Cu interconnect fabrication technologies or ways to improve the EM performance for narrow Cu lines are necessary. Moreover, from the perspective of stressing method, alternative current (AC) stressing can enlarge EM lifetime of Cu lines as compared to the conventional direct current stressing [88, 89]. The improvement in EM lifetime is attributed to the effect of damage healing. Under AC conditions, the partial Cu atoms migrating in one direction at one polarity stress would migrate back to its original location at the reversing polarity stress. Consequently, the Cu line suffers less damage from EM for a given time, resulting in a long EM lifetime. Additionally, the effect of damage healing from AC stress depends on the operation frequency. As the operation frequency is above 10 Hz, the effect of self-healing becomes significant and increases with the operation frequency. When the operation frequency is up to about 10 kHz, this effect is saturated. Thus, no further EM lifetime improvement is observed at the operation frequencies above this point [88].

5.1.2. Cu interface effect

The interface between Cu line and the capping layer is the dominating EM transport path for Cu damascene interconnects due to the lowest activation energy for diffusion [83]. Therefore, to obtain a long EM lifetime, the improvement of Cu interface is the most effective method by increasing the adhesion between these layers [90]. A typical dielectric capping process consists of two main steps: plasma clean to remove Cu oxides and a Cu barrier dielectric deposition (either SiN or SiCN) [91, 92].

A plasma clean has a pronounced effect on the EM improvement as compared to a barrier dielectric deposition. This is attributed to the enhanced adhesion between Cu line and barrier dielectric layer. H_2 or NH_3 plasma clean is typically used, which can remove the Cu oxide from the top surface of Cu metallization through chemical reaction. The obtained results were contradictory [93–95] since some authors reported H_2-based plasma clean is better. These apparent contradictions may result from the wide variety of plasma chambers and the plasma conditions. Nevertheless, it is clear that both the H_2 and NH_3 plasma clean can enhance EM lifetime. Additionally, in order to strengthen adhesion, a SiH_4 exposure process is inserted between a plasma clean and a dielectric deposition processes to form a thin Cu silicide layer. This way, the EM lifetime was enhanced due to the improved adhesion [96, 97].

The effect of Cu dielectric capping layer on EM is not as obvious as compared to that of a plasma clean although it is concluded that the improvement in the adhesion between Cu line and dielectric capping layer can enhance EM. SiN and SiCN capping layers have similar EM lifetime, but have longer EM lifetime as compared to SiC capping layer [98]. The formation of Cu compound (Cu_3N) at the interface for providing a better interface is a possible mechanism.

Based on these results, an alternative to improve Cu interface is through the use of a metal capping layer in replace of a dielectric capping layer. Due to the reduction in interface diffusion, EM lifetime was found to have a huge improvement. The used metal capping layer can be Ta/TaN or CoWP [57], the latter capping layer reported to provide a larger EM improvement than the former. Moreover, in Cu damascene lines with bamboo-like grain structure (i.e., no grain boundary diffusion), the activation energies for diffusion were 1.0 eV for an SiN or SiCN capping layer, 1.4 eV for an Ta/TaN capping layer, and 2.4 eV for a CoWP capping layer [99]. This suggests that the diffusion mechanism is changed from interface diffusion to bulk diffusion for CoWP capping layer. In the cast of Ta/TaN capping layer, although the interface diffusion mechanism is still dominating, the interface bonding between the Cu and the capping layer is enhanced.

Figure 8 compares various technologies for EM improvement in terms of EM improvement efficiency (EM lifetime improvement ratio and the resistance increase ratio). CoWP capping layer is shown to be the best approach with a higher EM life-time improvement and a lower resistance increase.

5.1.3. Microstructure effect

The microstructure of Cu interconnects also plays an important role in EM performance. The important microstructure parameters include grain size (with respect to line width), grain distribution, and grain orientation. Each of these parameters influences EM performance and is impacted by Cu metallization steps. Generally, large grain size or bamboo grain structure, tight grain distribution, and (111) grain orientation are helpful for EM improvement. Experimental results indicated that electroplated Cu line has relatively large grain size and tight grain distribution as compared to CVD Cu line, resulting in longer EM lifetime [100]. Furthermore, an annealing (<400°C) step after electroplating and before Cu CMP step can increase the grain size of Cu lines due to gain growth and recrystallization, resulting in increased EM lifetime [101].

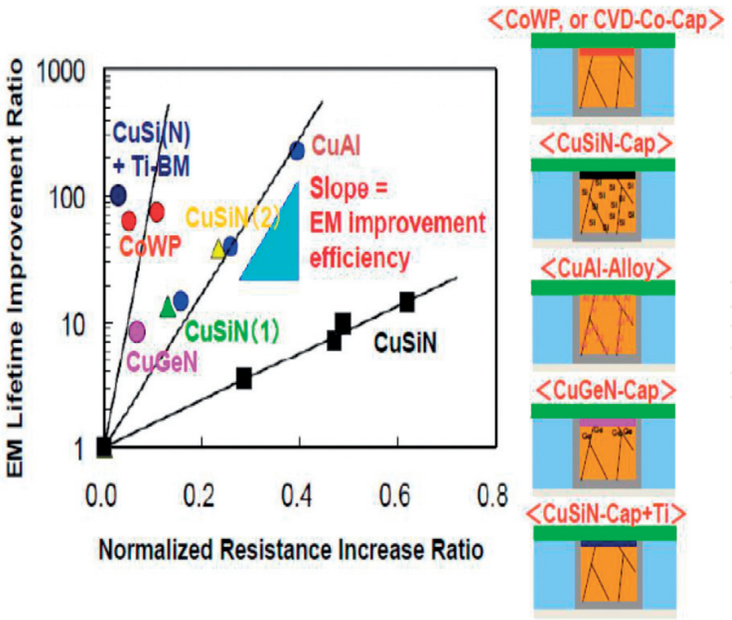

Figure 8. Comparison of electromigration lifetime improvement versus the resistance increase for various electromigration improvement technologies [40].

5.1.4. Dielectric effect

A lower EM lifetime was found when a low-*k* dielectric is used as an insulator in Cu interconnects [102, 103]. This reduction is amplified with decreasing the dielectric constant of low-*k* dielectrics. There are several reasons to explain the lower EM life-time for low-*k* dielectrics. First, the modulus of the low-*k* dielectrics is lower than that of SiO_2 film and decreases with the reduction of the dielectric constant. Because of the lower modulus, the Blech effect and the critical length for line immortality will be reduced [103]. Second, the barrier layers often have weak adhesion to low-*k* materials; the weak adhesion can result in extrusion fails during an EM stress [104]. Finally, low-*k* materials have lower thermal conductivity than does SiO_2. Hence, more joule heating is generated for a given current density [105], resulting in a higher temperature in the Cu wire, and therefore a faster diffusion rate of EM.

5.1.5. Cu seed layer doping effect

Doping impurities such as Al [106, 107], Ag [108], Mn [109–111], Magnesium (Mg) [112, 113], Zirconium (Zr) [114], and Tin (Sn) [115] into the Cu layer is an effective method to improve the EM lifetime. The main disadvantage of this approach is that the impurities increase the resistivity of Cu line. To avoid a huge increase in the resistivity, the dopant concentration is kept relatively low and the dopant is usually introduced in the Cu seed layer deposition process. Additionally, an extra annealing process is needed after completing Cu metallization. The purpose is that the dopant impurities segregate at grain boundaries and interfaces between the Cu line and the capping layer by an annealing. Thus, Cu migration rate of EM is retarded due to the reduction in the grain boundary and interface diffusions [106, 110]. The measured EM lifetime was found to be enhanced by at least one order of magnitude and is positively proportional to the doping concentration.

Among the dopants used, Al and Mn have received more attention because they have shown to increase EM lifetime significantly. Furthermore, Mn is the promising candidate for providing some advantages. Its low solubility in Cu lines allows minimum increase in resistivity by optimizing the post-metal annealing [109]. Moreover, Mn has high affinity for oxygen, resulting in the formation of MnO_x layer with the dielectric film by annealing. The formed MnO_x layer can act as a Cu barrier layer, thus avoiding depositing a metal barrier layer [47, 48].

5.2. Stress-induced voiding (SIV)

Like EM, voids will form in the metal line for stress-induced voiding. But these two reliability terms have different mechanisms. Whereas EM is induced by electron wind force under an electric field, stress-induced voiding (SIV) is due to stress migration. As a passivated Cu interconnect is annealed at moderate temperatures (200–250°C), tensile stress in the metal is established. If this built-up tensile stress is above the critical stress, voids will form in the Cu line, leading to a resistance increase or an open line. The built-up stress in the metal line is caused by two mechanisms: One is thermal stress due to thermal expansion mismatch between the metal line and the dielectric insulator; and the other is growth stress due to grain growth in the metal line [116–118].

The unique characteristic of stress-induced void is that the maximum rate of void growth in Cu line does not occur at a high temperature, as shown in **Figure 9**. To achieve large enough voids to fail the circuit, the stress built-up (void nucleation) and Cu atom migration (void accumulation) must occur in sequence. However, the temperature-dependence effect of these two mechanisms is totally different. If stress-induced void is originated from thermal expansion mismatch during the dielectric capping layer deposition, a "stress-free" temperature can be obtained. This stress-free temperature is related to the deposition temperature of the dielectric capping layer and subsequent processes. The stress-free temperature is close to the inter-level dielectric deposition temperature, generally being 300–450°C. As the stress temperatures is

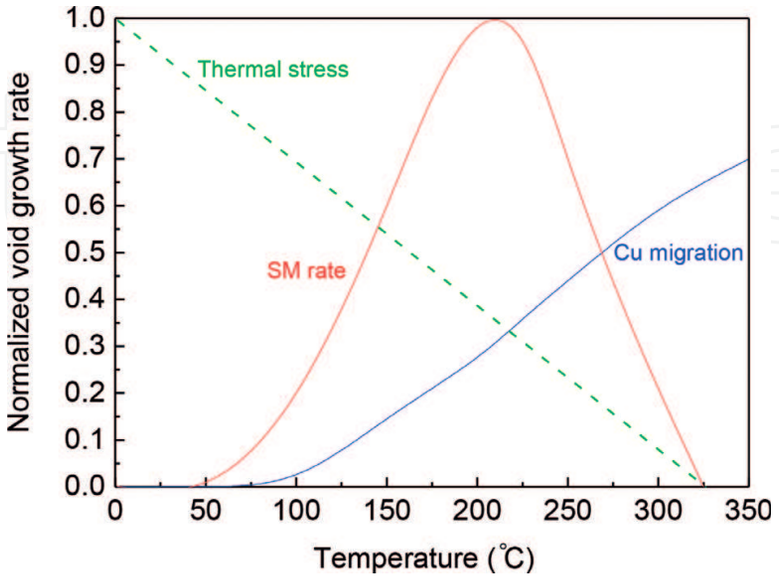

Figure 9. Void growth rate of stress-induced void as a function of temperature [116].

close to the stress-free temperature, the tensile stress (σ) in the metal line is low, so that the void growth rate is low. On the other hand, the Cu diffusivity is increased with increasing the temperature, leading to a high void growth rate at high temperatures. These two different mechanisms result in a significant void growth at intermediate temperatures (150–250°C) [116, 119, 120]. Therefore, for a newly developed process for Cu interconnects, the stress temperature for the maximum rate of void growth in Cu line should be characterized in advance.

The test structure of stress-induced void is simple via-chain structures. The resistance is monitored as a function of time at the stress temperature [121]. As the resistance is increased by a certain value (5–10%), this time is defined as the lifetime for stress-induced void.

The main affecting factors for stress-induced voids in Cu lines can be categorized as follows.

5.2.1. Scaling effect

The main failure mode of stress-induced void is void formation under vias due to the stress gradient in the underlying Cu line and the presence of the via-metal interface [116]. As the formation void is spanned the whole via, which is called "killer void," the electric current is stopped, leading to a failure of circuits. Therefore, the failure rate for stress-induced void in Cu line increases with decreasing via size (**Figure 10**).

On the other hand, the failure rate for stress-induced void in Cu line increases with increasing line width (**Figure 10**) opposite to what is observed with Al line [116, 117, 122]. Two mechanisms can explain this unique behavior. One is that the hydrostatic stress increases with increasing the width of Cu lines based on the result of stress simulation [123]. Hence, a stronger driving force for void formation is produced in wide Cu lines than in narrow Cu lines. The other mechanism can be explained by the theory of "active diffusion volume" [124]. In this theory, the formation void is related to the number of vacancies, which are available within a diffusion length of the via. The wider Cu lines can provide a greater number of

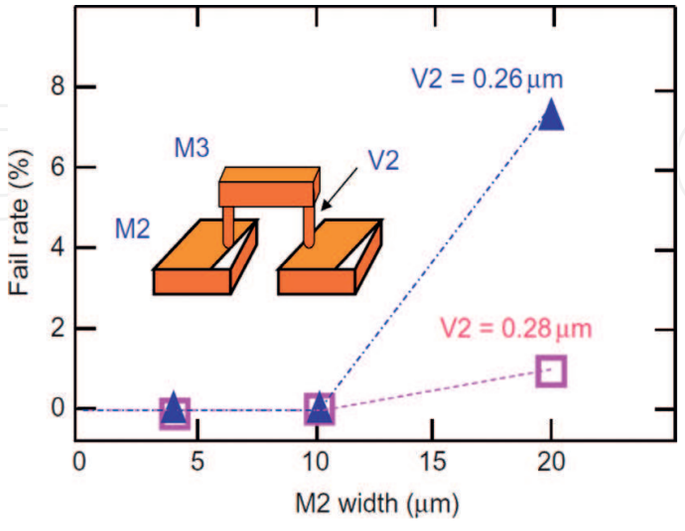

Figure 10. Failure rate of stress-induced void versus M2 line width and V2 via size after annealing stress at 225°C for 1000 h. Reproduced with permission from Ref. [122].

vacancies to form void under the bottom of the via. Thus, the wider Cu lines take less time to form a "killer void" and have a weak resistance against stress-induced void. To solve stress-induced void reliability issue on the narrow via and wide line, a design solution is provided by inserting redundant vias in the wide Cu line [125, 126]. By this approach, the stress gradient is reduced and the volume of the killer void is increased, thus enhancing stress-induced void.

5.2.2. Cu surface effect

Stress-induced void in Cu lines are mostly observed under vias [116]. A high tensile stress in the metal at the edge of the via and a weak adhesion between the barrier metal and the underlying Cu at the bottom of the via are responsible for this failure mode. A high tensile stress in the metal at the edge of the via was detected through stress simulation modeling [127, 128]. At this point, if the tensile stress exceeds the critical stress, a void will nucleate and then grow along the interface between the barrier metal and the underlying Cu at the bottom of the via. Once a void forms, the critical stress will be reduced, making the stress field surrounding the void becomes less tensile. The resulting stress gradient favors vacancy diffusion toward the void resulting in further growth.

To solve this failure mode of stress-induced void, providing a better Cu interface is the main strategy. Therefore, the approaches to optimize Cu interfaces applied for EM improvement also provide great help for stress-induced void [129–131].

5.2.3. Cu grain boundary effect

Stress-induced void can also be observed at grain boundaries in Cu lines [132]. Thus, grain boundary is another diffusion path. Decreasing the grain boundaries in Cu lines (i.e. maximizing Cu grain size) can minimize the fail rate of stress-induced void, similar to the improvement in EM reliability. The most effective method to maximize Cu grain size is by the use of an annealing process. The operation timing is after Cu plating and before Cu CMP step. It is noted that the maximum annealing temperature must be limited after dielectric capping layer deposition because high-temperature annealing after dielectric capping layer deposition can lead to high rates of stress-induced void formation due to either confined grain growth or due to increased stress in the Cu line [122, 132]. Additionally, the use of metal capping layers [133] and/or Cu alloying lines [106, 107], which are used to improve EM has also shown to reduce the failure rate of stress-induced void.

5.2.4. Via barrier effect

The early failure of stress-induced void occurs inside the via due to a defect in the via with a lower tensile stress [124]. Since Cu atoms will migrate to the regions of higher tensile stress, the vacancies will diffuse to the regions of lower tensile stress. If there is a defect in the via, then void nucleation will be further enhanced in the via. Poor coverage of seed layer and undesirable gap filling of electroplating are the precursors for void formation. As the dimensions of Cu interconnects shrink, these two processes are becoming more challenging. To ensure low resistance of the metal line in the advanced technology nodes, the thickness of Cu barrier layer is required to thin down as much as possible. However, the issues of Cu diffusion into the

dielectric, metal barrier layer coverage on the bottom and sidewalls of trenches and vias and Cu plating gap filling are important.

This failure mode of stress-induced voids can be eliminated with good metal barrier layer coverage on the bottom and sidewalls of trenches and vias and void-free Cu-filling process. To achieve these goals, pore sealing on porous low-*k* dielectrics [134], good control of the via and trench profiles [135], use of ALD barrier technology [136], and optimization of the additives in the Cu plating process [37] have been demonstrated.

5.3. Time-dependent dielectric breakdown (TDDB)

During a prolonged stress at high electric fields, electric damage can occur in dielectric materials. This induces the loss of the insulating properties for a dielectric material for which the resistance state is converted from high to low. Finally, an electrical breakdown occurs as a conducting path is formed. This loss of reliability is called "time-dependent-dielectric breakdown" (TDDB) [137–141].

The time-dependent dielectric breakdown can occur in gate dielectrics and BEOL dielectrics [142, 143]. The former has been an important reliability issue because the thickness of gate dielectrics is continuously decreased with the advance of technology node although the latter is not a key issue in Al interconnects because the applied electric field across the BEOL dielectric is low due to the relatively large spacing between the metal lines. However, as the technology node of ICs is continuously advancing, the lateral electric field across the BEOL dielectric significantly increases due to the reduction of interconnect dimension. Simultaneously, the used BEOL dielectric is transforming to low-*k* dielectrics with a lower dielectric constant than 4.0. The breakdown strength of low-*k* dielectrics is lower than that of SiO_2 film and typically decreases with the reduction of the dielectric constant. These combined effects result in a critical challenge in time-dependent dielectric breakdown for BEOL dielectrics in the advanced technology nodes [144, 145].

The test structure for the TDDB reliability evaluation has two typical configurations: comb-comb or comb-serpentine layout [146–149], as shown in **Figure 11**. Typically, metal-1 is the most commonly used metal level because it has the smallest pitch. During a test, one electrode (e.g., serpentine) is grounded and a constant positive voltage is applied to the other electrode (e.g., comb). The leakage current is measured with the stress time. The typical leakage current versus the stress time is the initial decrease in leakage current due to trapping of charge, followed by stress-induced leakage current, and finally breakdown [150]. The stress time with a sharp increase in the monitored leakage current, is corresponding to the breakdown time.

Since the time-dependent dielectric breakdown is used to assess the dielectric reliability, its performance is strongly dependent on the property of a dielectric. Additional investigations have indicated that a high density of defect sites in the as-deposited dielectric (especially for low-*k* materials) [151], damage or contamination of the dielectric from processes such as plasma and CMP processes [152–154], and patterning problems such as line edge roughness or via misalignment [155, 156] resulted in the low breakdown strength of BEOL dielectrics.

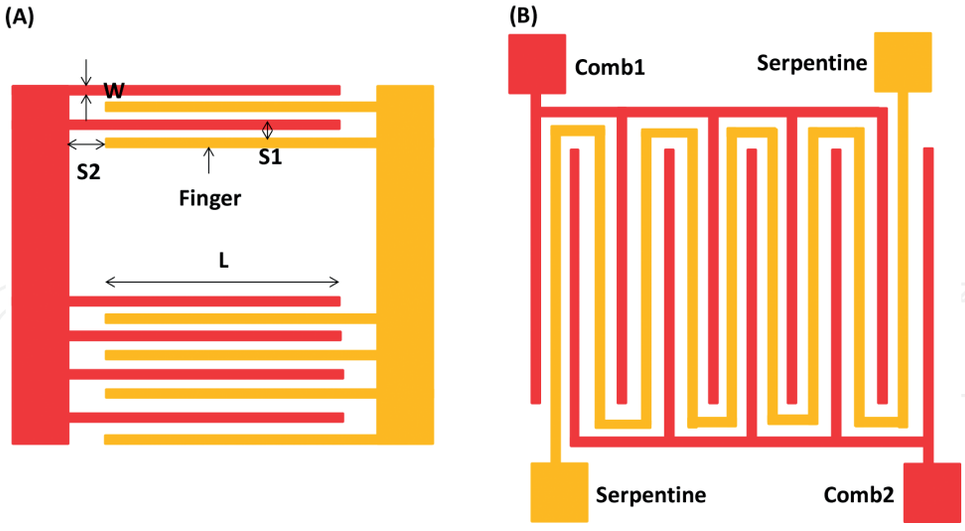

Figure 11. Top view schematic of time-dependent dielectric breakdown test structures. (A) Comb-comb structure. (B) Comb-serpentine structure.

Consequently, the optimization of the BEOL interconnect process can effectively improve time-dependent dielectric breakdown reliability.

Additionally, Cu metallization also influences the TDDB performance. Cu diffusion into the dielectric leads to serious degradation in BEOL dielectrics reliability [157–159]. Cu diffusion into the dielectric can be through the dielectric and metal barrier layers, which are interfacial diffusion and bulk diffusion, respectively. The interfacial diffusion is considered to be the dominant Cu diffusion path. This can be demonstrated by the fact that dielectric breakdown between neighboring Cu wires generally occurs at the interface between the capping layer and the dielectric [150, 160]. The interface is expected to have a higher trap density than the bulk dielectrics due to the bond mismatch between the different materials or due to contaminants from the Cu CMP process [153, 161]. Hence, the interface between the capping layer and the dielectric is the preferred diffusion and leakage path for Cu atoms. Moreover, the fabricated Cu lines are generally tapered shape (wider at the top than at the bottom), so the space is smallest at the top of the Cu line, leading to the highest electric field at this location. Due to the combination of high electric field and high-defect density, the interface is the dominant path for Cu diffusion.

Moreover, "Cu-diffusion-catalyzed breakdown" theory has been proposed to explain lower dielectric breakdown strength for Cu diffusion into the dielectric [162]. In this theory, Cu could act as a precursor for an ultimate dielectric breakdown. As the concentration of Cu in the dielectric reaches a critical value, the dielectric breakdown event occurs. Two possible mechanisms can account for Cu-induced dielectric breakdown. First, the diffused Cu atoms can catalyze the bond breakage reaction by inducing permanent bond displacement in the dielectric. The other mechanism is that the accumulated Cu atoms in the dielectric form clusters of nanoparticles. As these clusters are connected, a metallic shorting bridge or a local dielectric thinning is established, triggering a dielectric breakdown.

In addition to the reduced dielectric breakdown strength and failure time, Cu diffusion into the dielectric alters the TDDB electric field acceleration model, which is used to determine the fail rate or lifetime at the use conditions (the high-field stress data must be extrapolated to the lower fields at the use conditions). The "E-model" [163–165], which is a field-driven model and chemical bond breakage mechanism, fails to describe the low-*k* TDDB behavior with Cu diffusion. Instead, "$E^{1/2}$-model" [146, 166] is the most appropriate model. It is postulated that the accelerated electrons, injected from the cathode, transport inside low-*k* dielectric by means of Schottky-Emission or Poole-Frenkel conduction. Some electrons undergo thermalization under high field and high temperature and impact the Cu atoms at the anode. This produces the positive Cu ions, which in turn inject into the dielectric under the field along a fast diffusion path. Since the current in the Schottky-Emission or Poole-Frenkel conduction is proportional to $E^{1/2}$, the "$E^{1/2}$-model" is the possible model to describe low-*k* time-dependent dielectric breakdown with Cu diffusion. However, the TDBD model is not yet fully accepted and so it remains an open issue.

To minimize Cu diffusion into the dielectric to avoid reliability degradation in TDDB, several process strategies have been proposed including using adequate metal barrier layers [167, 168], minimizing residues after post-CMP cleaning [169], and minimizing air exposure prior to capping of the Cu [150, 153]. Additionally, alternating polarity operation method instead of direct current stress could increase dielectric breakdown lifetime, resulting from recovery effect due to the backward migration of Cu ions during the reverse-bias stress [170, 171].

6. Conclusions

To improve the performance of ICs by reducing *RC* delay, the conductor with a lower resistivity in interconnects should be rechosen. In the past two decades, better performance of ICs was achieved by using Cu conductor in place of Al conductor. Currently, although Cu metallization has been successfully integrated into ICs, a different and complex process to fabricate Cu interconnects has many remaining issues, resulting in integration and reliability challenges.

In future, the interconnect process returning to subtractive metal process from dual damascene process is one possible solution. Furthermore, looking for an alternative to replace Cu is an ongoing important topic for research and development. Silver, carbon nanotube, graphene, or photonic interconnects are possible candidates.

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