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Towards New Generation Power MOSFETs for Automotive Electric Control Units

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Abstract

Power metal-oxide-semiconductor field-effect transistors (MOSFETs) are thought to be highly robust and versatile in high-speed switching applications in power electronics design due to its intrinsic high input impedance and compact size. This chapter concerns the development of a high-performance low voltage rating power MOSFET possessing low on-resistance and excellent avalanche current capability for an automotive electric power steering system (EPS). Using industry-standard Technology Computer-Aided Design (TCAD) tools, the planar- and trench-technology power MOSFETs, have been designed, modeled, simulated and compared. We surveyed and analyzed the specific on-resistance due to the different device structures, and various methods are highlighted and compared so that their benefits can be better understood and adopted. Additionally, the device ruggedness has been investigated and its improvement was evaluated and established for that of the trench MOSFET due to gate corner smoothing.

Keywords: automotive MOSFETs, specific on-resistance, avalanche ruggedness, unclamped inductive switching, silicon carbide power semiconductor, critical breakdown electric field, Technology Computer-Aided Design

1. Introduction

When the first automobiles were invented dating back to 130 years ago, the only expectations were safe operation and durability. Over the years of continual development of the automobile, more and more "bells and whistles" were added, culminating in more innovative features and functions. More recently, driverless cars have become a reality. These features are inevitably empowered by advances in electrical engineering and automation, bringing about the rapid increase in the value of electronics in a car. Particularly, more and more electronic control units (ECUs) have been developed for automobiles and electric vehicles. In certain high-end

vehicles, the number of ECUs can be as high as 100 or so. If ECUs are akin to the organs of the car, semiconductor devices are like the cells. The latter we refer especially to those power semiconductor devices that are widely recognized as basic and vital building blocks of electrical and power electronic systems.

Discrete power semiconductors occupy a major share of the ever-increasing revenue from semiconductor devices in the HEV/EV industry over the years, and this is projected to continue beyond 2020 (**Figure 1**) [1]. Specifically, power metal-oxide-semiconductor field-effect transistors (MOSFETs) have gained a lot of popularity due to their simple drive requirements, low on-resistance and fast switching properties. Owing to their high input impedance and energy efficiency excellence in high frequency applications, MOSFETs are the preferred choice to several circuit designers [2]. Notably, power MOSFETs are able to switch high current and voltage levels with enhanced power handling capability in highly efficient power supply circuits and systems [3].

1.1. Power consumption of power MOSFET

One of the key metrics underpinning the performance of the MOSFET is on-resistance (Rdson). High Rdson restricts the maximum current capability; in addition, large power dissipation
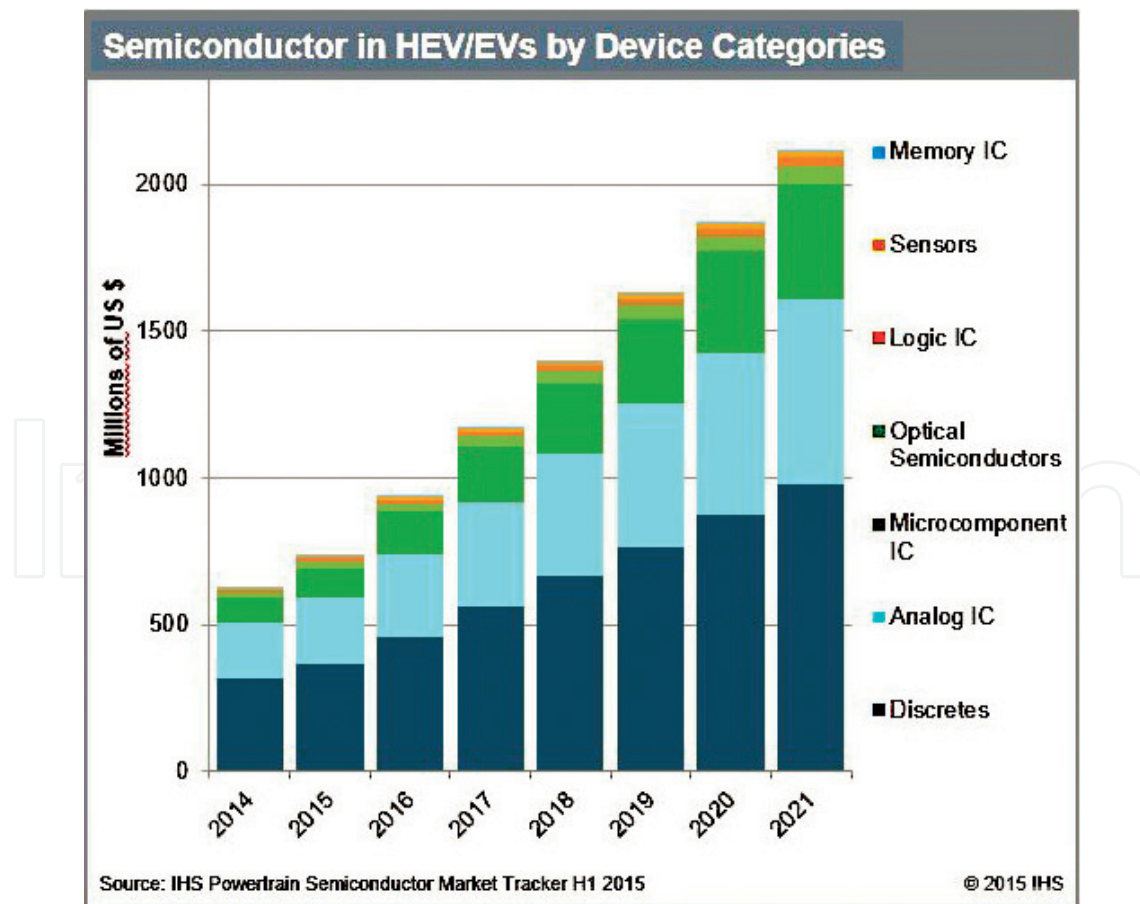
Figure 1. Semiconductors in HEVs/EVs by device categories [1].

($P = V_{dd} \times I_{d, \text{ave.}} = I_{d,\text{ave.}}^2 \times \text{Rdson}$) will lead to unwanted die temperature rise during device operation. It is understood that Rdson is inversely proportional to the cell area for many device technologies Therefore to enable comparison between different designs, e.g. 'trench' versus 'planar' types, a figure-of-merit is introduced called the specific on-resistance, i.e. the product of Rdson and the cell area.

1.2. Ruggedness of power MOSFET

Almost every application circuit has some kind of inductance, not only in the form of load inductance such as solenoids or electric motors, but stray inductances such as wiring and layout inductances.

Figure 2 shows a typical application circuit in an electric power steering system. It can be seen that instantaneous current changes could result from a short circuit in the arm of the H-bridge, a short circuit to the ground or a short circuit to the three-phase motor. When the supply current is rapidly switched off, the changing magnetic field inside the windings induces a back electromotive force. Thus, when dealing with inductive loads in ECUs, a high di/dt commutation rate during switching transitions runs the risk of a surge voltage that may destroy the device [4]. Placing a freewheeling diode anti-parallel to the MOSFET represents one approach to avoid this possible high voltage dump. However, in some applications, for instance gasoline or diesel injection [2], MOSFETs are designed with an intrinsic body diode to withstand this
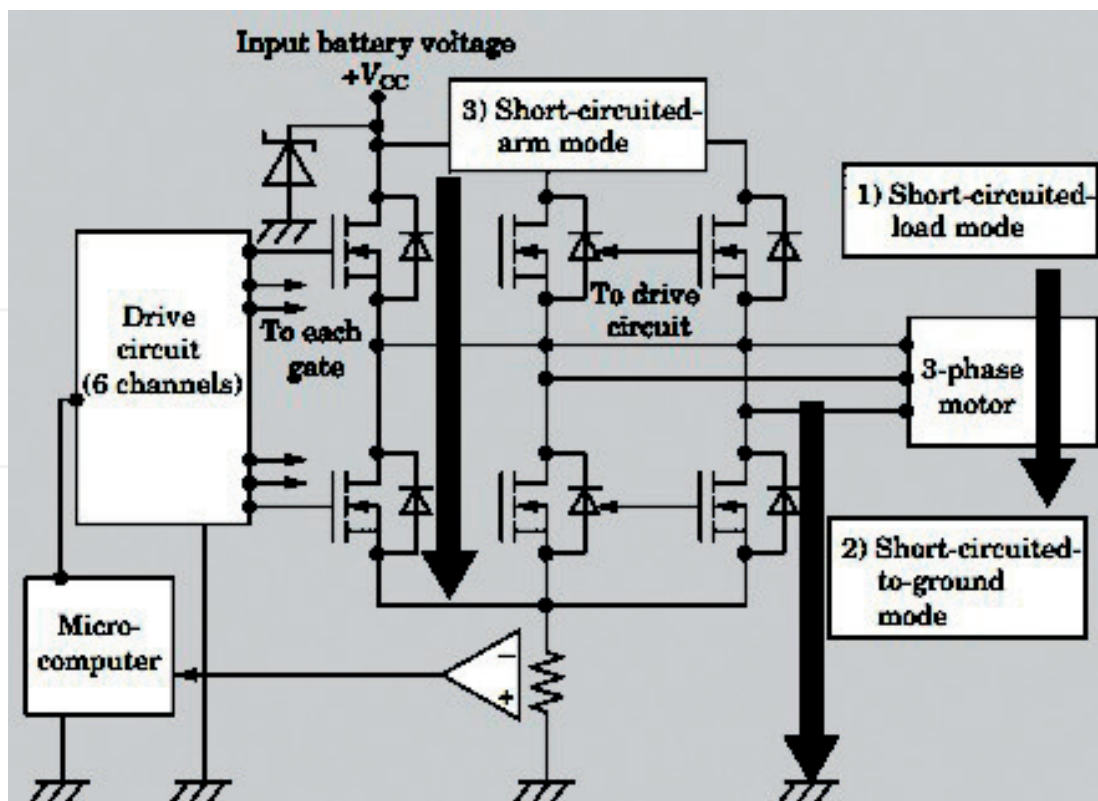

Figure 2. Typical application circuit in electric power steering [2].

possible voltage surge in order to survive any avalanche breakdown threat. Unclamped inductive switching (UIS) is so-called without support of a separate freewheeling diode, and ruggedness is the ability of the MOSFET to resist avalanche failure under UIS conditions. Electron irradiation or platinum doping may also be used for minority carrier lifetime control in the body diode to greatly improve the reverse recovery characteristics.

1.3. Overview of the power MOSFET market segments

According to the QYResearch Group, the global revenue for the discrete power device market in 2016 was valued at $ 7.277 billion, and by the end of 2022 this number was projected to rise to $ 9.135 billion, growing at a compound annual growth rate of slightly above 3.86% between 2016 and 2022 [5]. As aforementioned, the power MOSFET accounts for a significant portion of the total revenue. There are various catalogs of MOSFETs available in the market; the technology used is mainly categorized into the following three types: planar, trench and superjunction. In the low voltage category, besides automotive MOSFETs that form the main focus of this chapter, other power MOSFETs are designed for a range of other applications. Take Infineon for example, they target their commercial power MOSFETs at the following applications [6]:

- DC/DC converters

- 3D printers

- LED lighting

- motor control systems

- solar micro inverters

- battery powered applications, i.e. desktop and notebook

- audio amplifier

Further, Infineon has also developed green and robust packages for their product range, providing the highest current handling capabilities [7]. In the high voltage rating (500–900 V), a very innovative kind of MOSFET has dominated the market, called the superjunction MOSFET, which was originally commercialized by Infineon in 1998 [7]. Normally, the on-resistance is positively related to the voltage rating, which is characteristic of typical high voltage rating devices. This is due to the increase in drift region resistance to support higher voltages. However, thanks to the superjunction MOSFET, this relation does not apply. The most remarkable feature about this kind of MOSFET is the dramatic reduction in on-resistance and switching losses, thus enabling high power density and energy conversion efficiency in high power applications. Finally, the other kind of power MOSFETs is based on the laterally double-diffused short channel structure, or RF LDMOS. Due to its high operating frequency, one typical application of this MOSFET is in telecommunications, for example, in power amplifiers in television systems (especially digital television), radar systems and military communications [8]. Besides a higher gain and linearity, excellent noise-resistant properties and thermal stability are other key advantages of this type of unipolar device [8].

2. Automotive power MOSFET designs

A standard planar MOSFET was designed to meet the performance specifications of the electric power steering circuit. In order to enable better noise resilience, an appropriate threshold voltage (V_{th}) of 3 V was engineered [2]. In the current technology market, the typical supply voltage for the power steering circuit is 42 V [2]. Therefore the designed breakdown voltage of the planar and trench MOSFET should be around 50 V. **Figure 3** shows the structure of the n-channel planar MOSFET including the depletion regions. During forward conduction, electrons flow from the source through the inverted region of the p-well (or n-channel) beneath the gate, then through the JFET region before entering the drift region. Hence, there are four main types of component resistances [9]: (1) source resistance, (2) channel resistance, (3) JFET resistance and (4) drift region resistance, which will be further discussed below. **Figure 4** shows the V_{th} increase with the *p*-well dose. The *p*-well was designed with a dose of 4.5×10^{14} cm^{-2} to meet the V_{th} requirement.

Nevertheless, it is important to note that for high voltage designs, the drift region resistance is the most significant component, whereas for low voltage designs, channel resistance and source resistance are crucial, in the overall Rdson. As Rdson is negatively correlated to the drift region doping concentration, so is the breakdown voltage (BV), as shown in **Figure 5**. Hence for high voltage rating power MOSFETs, the doping concentration in the drift region should be low enough, which is the reason why the Rdson of high power MOSFETs is typically way larger than that of low power MOSFETs. Fortunately, replacing silicon (Si) with wide bandgap silicon carbide (SiC) would enable a significantly lower drift region resistance [10]. The results for this will be discussed below. Besides, the drift region epitaxial layer thickness (t_{nepi}) also determines Rdson, and **Figure 6** shows that below 5 μm, BV drops dramatically, thereby reflecting the case that avalanche breakdown occurs before the drift region is fully depleted in the off-state. Therefore the optimal t_{nepi} should be slightly larger than 5 μm for the best trade-off between BV and Rdson.
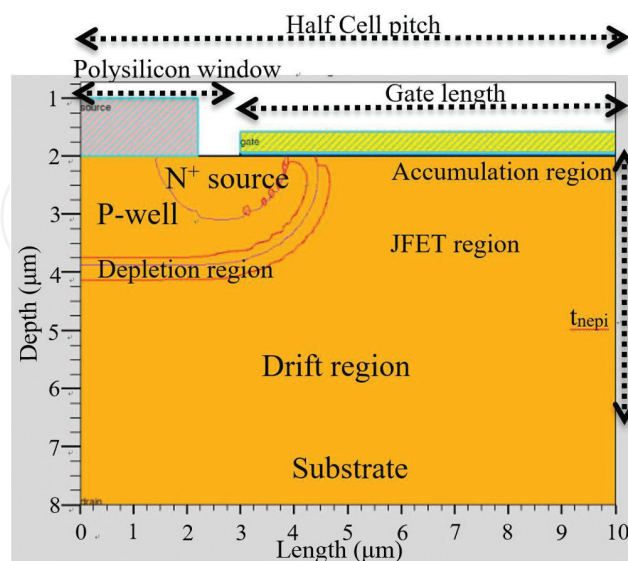
Figure 3. Structure of the planar MOSFET including depletion regions at zero bias [11].
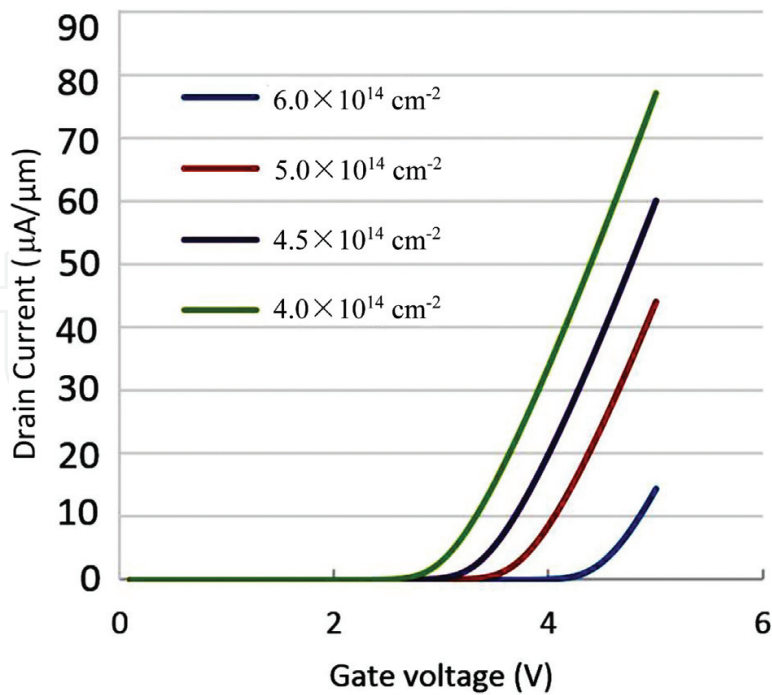
Figure 4. Transfer characteristics at a drain voltage of 0.1 V for various p-well (boron) doses [11].
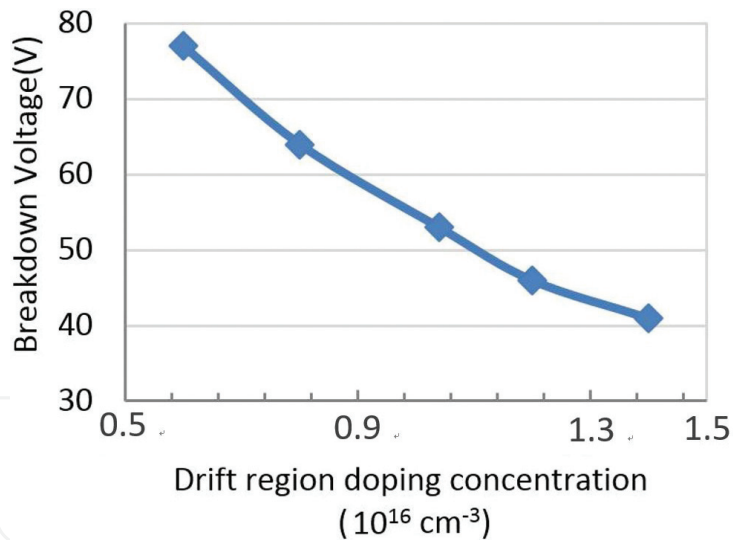
Figure 5. Breakdown voltage as a function of drift region doping concentration [11].

For a half-cell pitch decreasing from 11 to 10 μm, BV increases (**Figure 7**). Below 10 μm, no further increase in BV can occur, owing to a field plate effect that optimizes the electric field distribution at the junction curvature; the electrical field at the junction curvature approximates that of a planar junction. A shorter cell pitch would increase the JFET resistance; therefore the half-cell pitch was chosen to be 10 μm to provide the best trade-off between BV and JFET resistance. The Rdson is 1.56×10^4 Ω at a gate bias of 5 V (see **Figure 8**), and with a cell width of 1 μm, the specific on-resistance is 1.56 mΩcm^2.
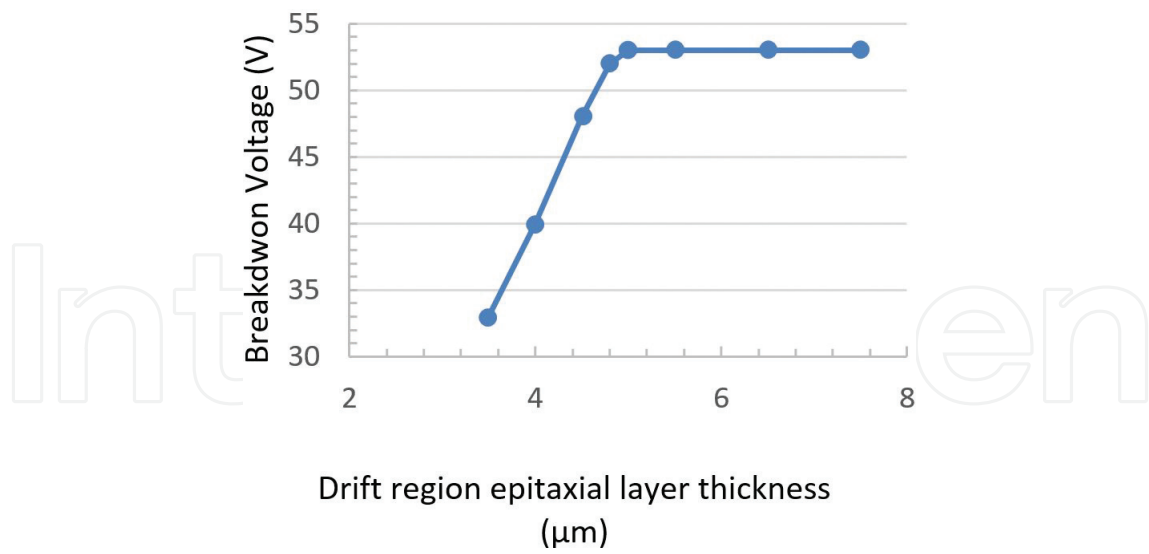
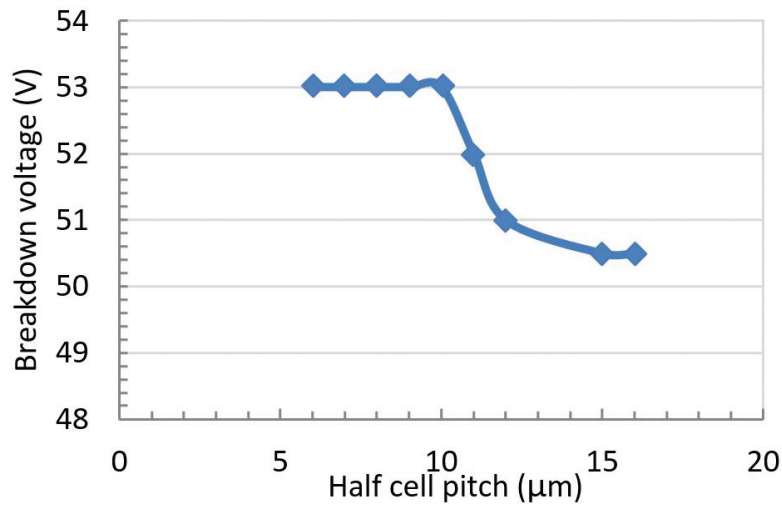**Figure 6.** Breakdown voltage as a function of drift region epitaxial layer thickness [11].

Figure 7. Breakdown voltage as a function of half-cell pitch [11].
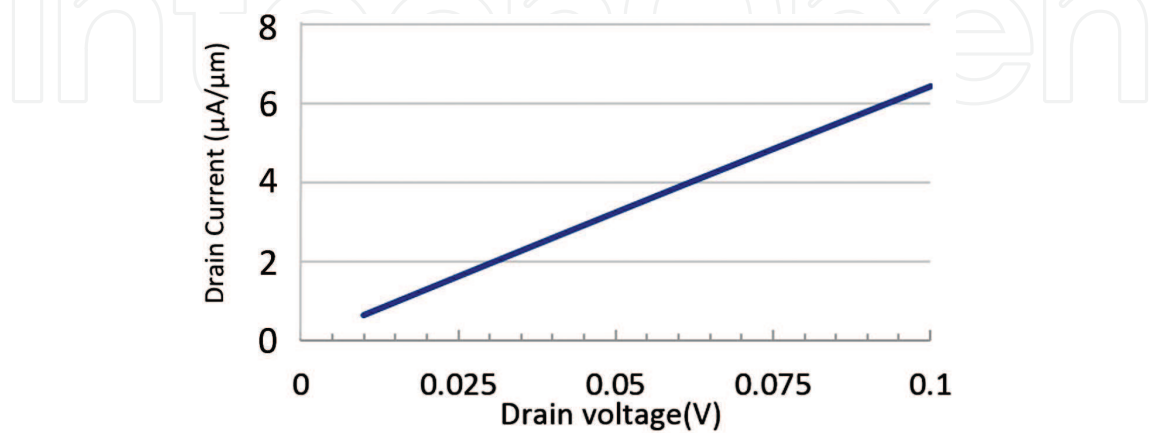

Figure 8. Output characteristics in the linear region of operation at a gate voltage of 5 V [11].

Further, a caveat should be noted that in practice, especially for high voltage devices, BV is limited by the edge termination structure used to control the surface electric field. This is because high voltage planar junctions under reverse bias exhibit significantly lower break-down voltages than one-dimensional theory predicts due to three-dimensional electric potential line crowding at the junction periphery. Therefore a good edge termination structure is critical to minimize this effect and increase the planar junction BV to near ideal values to maintain the rated BV and reliability of the high voltage power device. When the maximum specified drain to source voltage (or BV) is exceeded when the MOSFET is turned off, the intense surface fields on the field guard rings, beyond the rated design specification, can cause avalanche multiplication, thereby leading to conduction of an overcurrent that damages the device due to excessive power dissipation. This is indicated by the catastrophic damage on the field guard rings of the MOSFET bare die (see **Figures 9** and **10**).
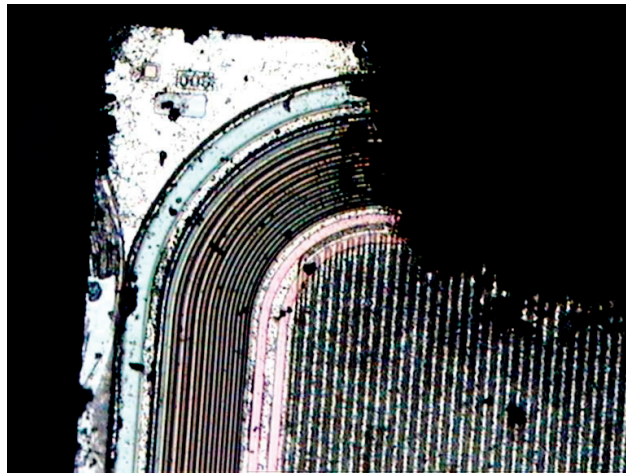
Figure 9. Breakdown damage on field guard rings indicating excessive drain to source voltage.
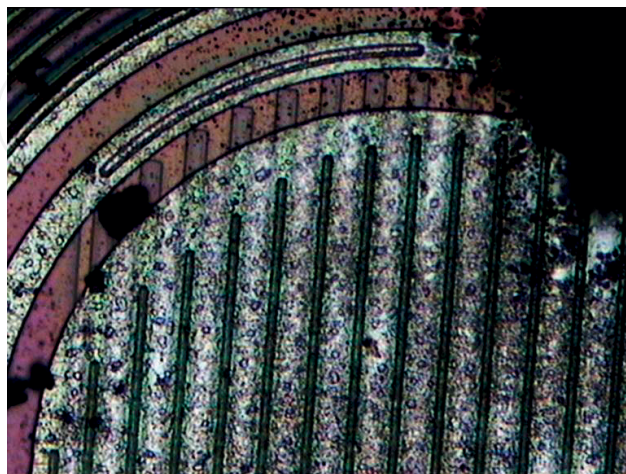
Figure 10. Breakdown damage on field guard rings indicating excessive drain to source voltage (under higher magnification *c.f.* **Figure 9**).

## 2.1. Design enhancements for low on-resistance

Having high cell densities and large die sizes can achieve lower on-resistances, but concomitantly result in significant gate and output charges, thereby increasing the switching losses. Therefore three main strategies to reduce on-resistance will be illustrated for the planar MOSFET: (1) optimization of gate width-length dimensions; (2) increased doping in the integral JFET region; and (3) adopting wide bandgap SiC as the power semiconductor material. The deep trench design is known to significantly reduce on-resistance owing to a low spreading resistance through the increased accumulation layer, and complete elimination of the JFET resistance.

2.1.1. Gate width-length optimization

Concerning the planar MOSFET, the specific on-resistance of the accumulation layer is positively related, but that of the JFET region is negatively related, to the width-length ratio of the gate electrode [12]. The optimum gate width is *ca.* 3 μm (see **Figure 11**), yielding a specific on-resistance of 1.2 mΩcm². Therefore reducing the half-cell pitch from 10 to 6 μm (for a polysilicon window 3 μm in length) reduces the specific on-resistance by 23%. As the gate width reduces below 3 μm (or cell pitch below 6 μm), the specific on-resistance rises sharply due to the short current path in the JFET region, which is pinched off during linear operation. In addition, according to **Figure 7**, when the half-cell pitch is 6 μm, the junction curvature does not lower the BV. Therefore the optimal gate length should be between 5 and 6 μm.

2.1.2. Increased doping in integral JFET region

Figure 12 shows the structure of the power MOSFET with increased doping in the integral JFET region. By increasing the JFET doping concentration ($\approx n$), the JFET resistivity reduces as $\frac{1}{nq\mu}$ where q is elementary charge and μ is carrier mobility, but the BV also lowers as shown in **Figure 13**. The optimal dose is 2.7×10^{15} cm^{-2} for a voltage rating of 50 V; and the optimized specific on-resistance is 1.43 mΩcm^{-2}, representing a reduction by 8.3%.
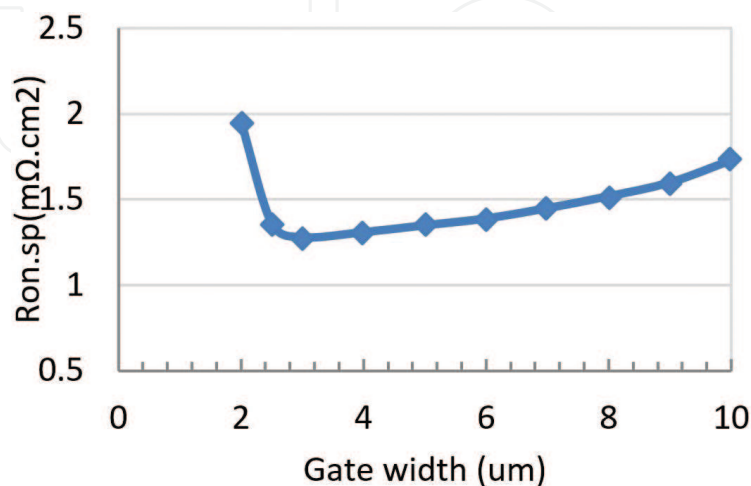
Figure 11. Specific on-resistance versus gate width [11].
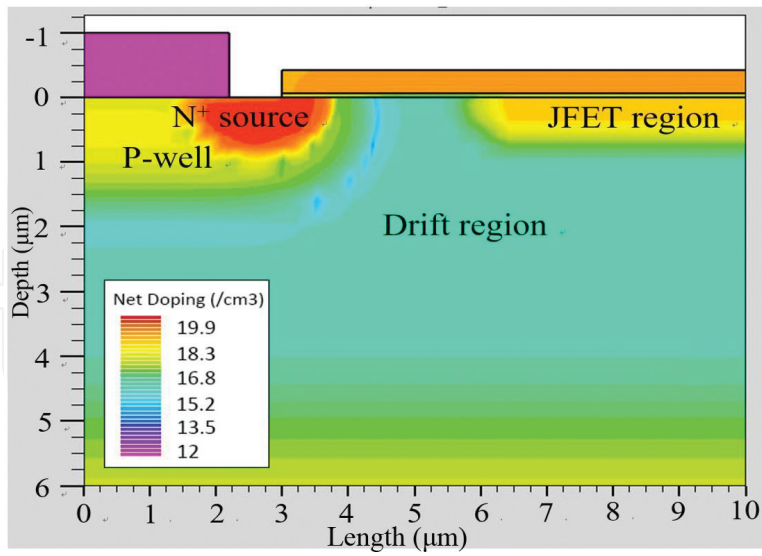
Figure 12. Doping profiles in the power MOSFET with additional dose in the JFET region [11].
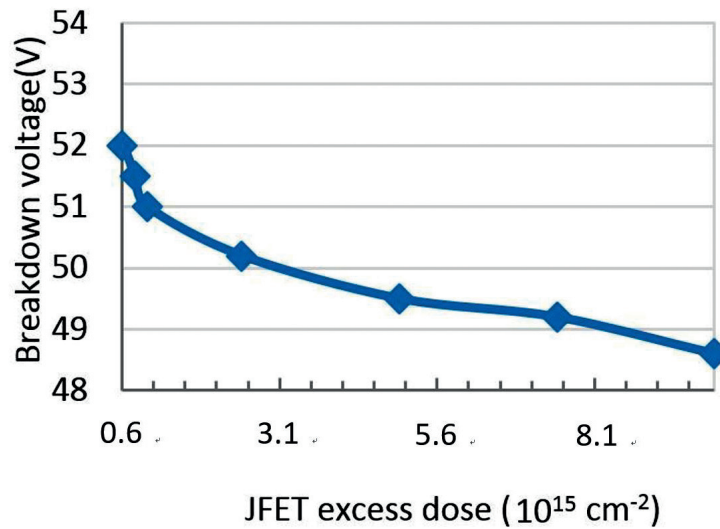

Figure 13. Breakdown voltage as a function of JFET excess dose [11].

2.1.3. Planar MOSFET based on SiC

The structure of a planar gate SiC vertically double-diffused (VD)-MOSFET being modeled is shown in **Figure 14**. The gate oxide thickness is the same as that for the Si planar MOSFET in **Figure 3**. To target a V_{th} of 3 V, the designed doping concentration is 2.6×10^{16} cm^{-3} in the *p*-well.

The critical breakdown electric field of SiC is eight-fold greater than that of Si [13]. Hence, if no reach-through is assumed, in principle a BV up to 411 V can be achieved according to:

$$V_{breakdown} = \frac{E_{critical}{}^2 \varepsilon_s}{2qN_a} \tag{1}$$

where $E_{critical}$ and ε_s are the critical electric field and dielectric permittivity respectively. N_a is the dopant concentration in the *p*-well, which should be far exceeded by that in the drift

region. The minimum *p*-well thickness is governed by the depletion width w_p in the *p*-well at the maximum drain voltage, Va. w_p is 1.46 μm according to:

$$w_n = \sqrt{\frac{2\varepsilon_s V_a}{q N_a}} \tag{2}$$

which in turn sets the minimum *p*-well thickness and channel length. However, this value may be an underestimate neglecting the effects of the junction curvature (see **Figure 15**), as according to the simulations the appropriate channel length is suggested to be at least 1.8 μm for a 50 V device. The *p*-well is designed to confer the blocking voltage capability; hence the dopant concentration in the drift region can be made very high. For example, the drift region dopant concentration may be as high as 10^{18} cm^{-3}, meaning that the depletion width in the drift region becomes extremely small, so that the drift region thickness may successfully be reduced to as thin as 0.3 μm. Hence, the ability to heavily dope and drastically reduce the epilayer thickness of
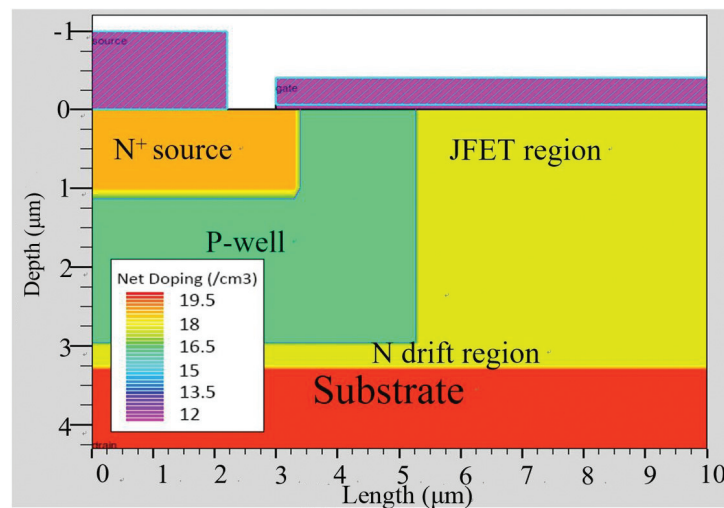
Figure 14. Structure of a planar gate SiC VDMOSFET [11].
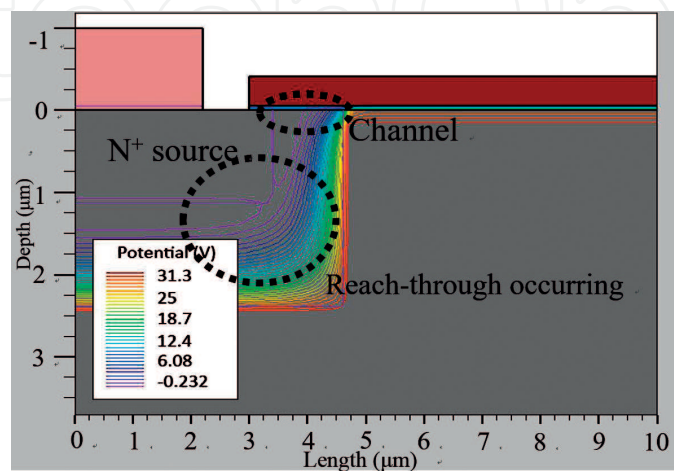
Figure 15. Potential distribution in SiC power MOSFET at a drain voltage of 36 V [11].

the drift region afforded by using SiC as a power semiconductor material mandates an exceedingly low drift region resistance of the planar MOSFET.

Moreover, the JFET region is virtually non-existent because the depletion width is significantly narrower, so that it becomes possible to make the separation between the two *p*-wells very small. As a result, the accumulation layer resistance, which would be significant in the Si planar MOSFET, may also be markedly reduced. The half-cell pitch can shrink to as small as 5.5 μm, yielding a specific on-resistance of 1.08 mΩcm^2, which represents a reduction by 31% compared to that of conventional planar technology in **Figure 3** (1.56 mΩcm^2) or by 10% compared to that of the Si planar MOSFET after gate width optimization (1.2 mΩcm^2).

2.1.4. Trench MOSFET

The cell pitch in the trench design platform can be made very small because there is no JFET region, but is limited by the current fabrication technology. **Figure 16** shows the trench MOSFET structure and current paths at a gate and drain bias of 5 V and 1 V respectively. A half-cell pitch of 2.5 μm is chosen for a typical trench MOSFET, and the gate oxide thickness is 80 nm, the n^+ source junction depth is 0.5 μm, and the dopant concentration in the substrate layer 1 μm thick is 10^{19} cm^{-3}.

To target a V_{th} of 3 V, the *p*-well dopant concentration is 2.6×10^{16} cm^{-3} for this trench design. For a 50 V rating, the designed drift region dopant concentration is 1.4×10^{16} cm^{-3}. **Figure 17** shows the drift region thickness dependence of BV. For an *n*-epilayer thickness below an optimal value of 2.2 μm, the BV reduces dramatically owing to punch-through effects. For this trench MOSFET structure, the specific on-resistance is 0.625 mΩcm^2, which is a reduction by 60% compared to the planar MOSFET (1.56 mΩcm^2).

Therefore, the underpinning reasons for such a low on-resistance of the trench MOSFET can be summarized as follows. By eliminating the intrinsic JFET component in the trench design, the
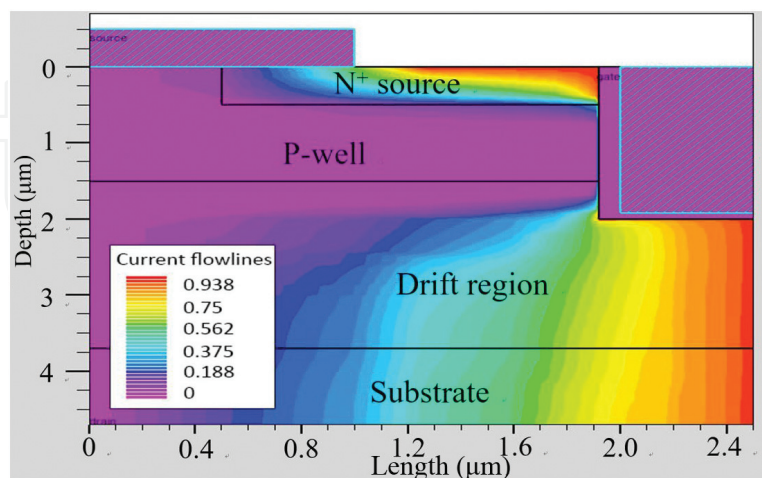
Figure 16. Trench gate power MOSFET structure and current flow lines through the n$^+$ source and n$^+$ substrate of the device with a backside contact. The current density is normalized to the maximum in the device [11].
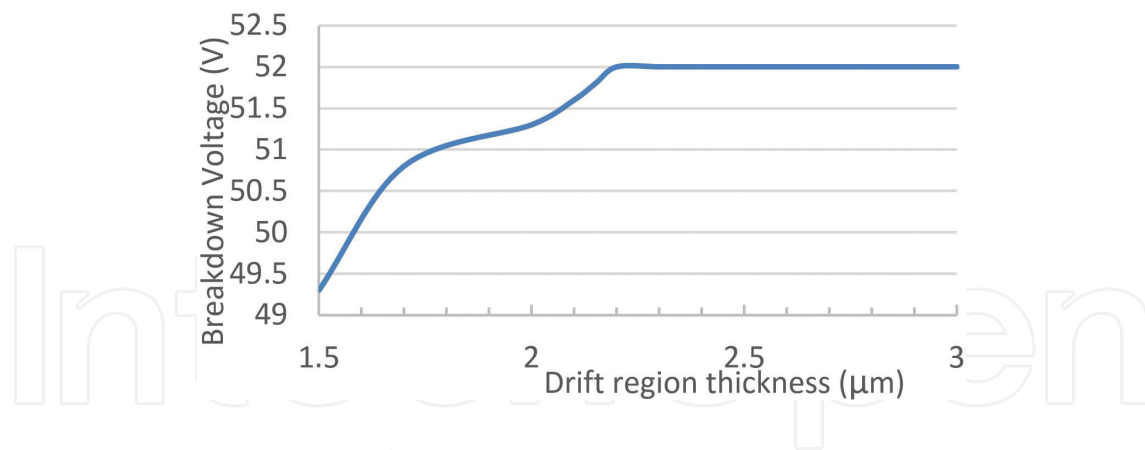
Figure 17. Breakdown voltage versus drift region thickness [11].

cell pitch can be made very small without needing to be concerned about increasing the JFET resistance. In fact, the cell pitch of the designed trench MOSFET is shorter by a factor of 2.5 than that of the planar MOSFET with optimum gate width [11].

3. Avalanche failure of power MOSFET

3.1. Avalanche failure mechanism

Basically, two types of failure modes can be identified in the avalanche condition. One is the active mode, which is caused by the turning on of a parasitic transistor intrinsic in the device through the p-well [14]. During avalanche, the body diode no longer blocks voltage; the electric field in the body diode becomes exceedingly large, above the critical breakdown field magnitudes of Si or SiC, particularly at the junction curvatures. Consequently, the process of impact ionization and avalanche multiplication occurs, thereby leading to a large current flow between the drain and source through the p-well, and power dissipation causes the associated local temperature rise. Due to the positive temperature coefficient of the resistivity of silicon, the p-well resistance (R_{b+}), and in turn, the voltage drop across the p-well (acting as the base-emitter forward bias), will increase. Once this voltage drop exceeds 0.7 V, which is the turn-on voltage of the parasitic BJT, loss of gate control and latch-up occurs, and a hot spot is formed as more current crowds into it, ultimately leading to device destruction due to overcurrent [15]. However, in other cases, avalanche failure is due to a passive mechanism, which essentially arises from a thermal effect [14]. In an avalanche condition, energy stored in the inductor is dissipated in the MOSFET, even in its off state, thereby leading to a local temperature rise within the device. This temperature rise changes the breakdown voltage, which in turn results in significantly larger current flow and increased power dissipation, and eventual thermal runaway; the current percolations through narrow regions due to the positive temperature coefficient of the silicon resistivity bring about secondary breakdown induced by ohmic heating. The secondary breakdown is initiated when the cell temperature reaches a critical value, beyond which the intrinsic carrier concentration exceeds the background doping concentration in the epitaxial layer [16];

and the thermal generation of defects that form current shunts. The avalanche failure site can be optically visualized from burnt marks on the bare die, indicating the occurrence of the hot spots that the current crowd into, eventually causing catastrophic damage.

3.2. Avalanche ruggedness evaluation

Modern day designs are focused on increasing device ruggedness, and thus avalanche testing methods were developed to validate the device avalanche rating. An example of the latter is UIS testing, which is performed using a test circuit like the one shown in **Figure 18**.

The UIS testing procedure is as follows:

1. A gate bias switches on the MOSFET.

2. Current flows through the load (whereas the MOSFET intrinsic resistance can be ignored), and the current increase can be expressed as:

$$I = \frac{VTA}{L} = \frac{VDD \times T}{L} \tag{3}$$

where VDD is the supply voltage, T is the pulse width and L the inductance.

3. When the targeted current is reached, the gate signal is reduced to zero, thereby immediately switching off the MOSFET. However, the current cannot decay abruptly owing to the presence of an inductive load; in fact, the resultant higher voltage exerted on the MOSFET forces the device into avalanche.

4. Avalanche operation is sustained till all the energy stored within the magnetic field due to the inductance is dissipated as heat.
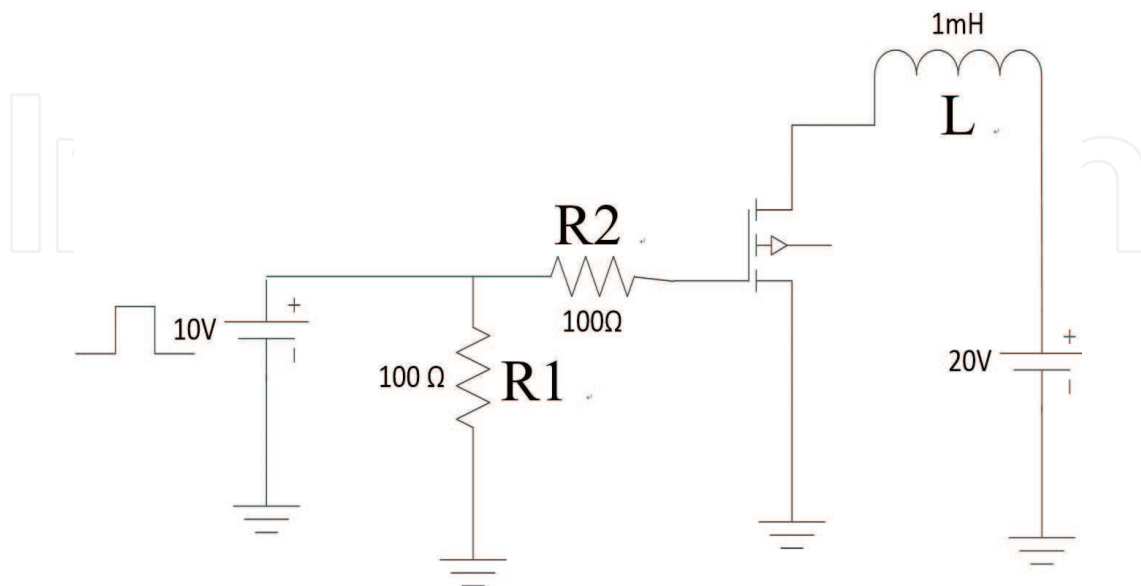
Figure 18. UIS testing circuit [17].

The voltage exerted on the device in the avalanche condition, is not BV but the effective breakdown voltage (BV_{DSS}), which is about 1.3–1.5 fold larger [4]. The avalanche voltage on the inductive load is BV_{DSS} – VDD, and the avalanche duration can be derived from:

$$t_{av} = \frac{I \times L}{BV - VDD} \tag{4}$$

Hence, we can compute the single pulse avalanche energy (EAS) from:

$$EAS = \frac{1}{2}I_{av}BV_{DSS} \times t_{av} = \frac{1}{2}L \times I^2 \frac{BV_{DSS}}{BV_{DSS} - VDD} \tag{5}$$

Since BV_{DSS} is directly proportional to temperature [18], self-heating effects are accounted for in the electro-thermal simulations of the circuit performance. As an example, VDD is 20 V and the inductive load is chosen as 1 mH, and R1 and R2 are both 100 Ω for a typical UIS simulation. The gate signal amplitude is 10 V and pulse width is 2 ms, which turns on the device within the duration when V_{th} is exceeded, but turns off the device otherwise. The 50 V rated MOSFET is designed with a V_{th} of 3 V, and for a die size of 5 mm^2, the waveforms under avalanche operation are shown in **Figure 19**.

The maximum drain current is 40 A, at which instant the gate bias drops below V_{th} so that the MOSFET is turned off and the junction temperature rises sharply from 27 to 123°C within a few nanoseconds as the energy stored in the circuit inductance is dissipated as heat in the device; the drain-source voltage also increases abruptly up to the BV concomitantly with temperature. The peak junction temperature and maximum drain-source voltage occur at the same time because the BV positively correlates with the junction temperature. Subsequently, the device reverts to room temperature after *ca.* 175 µs of avalanche operation, and at which point the drain-source
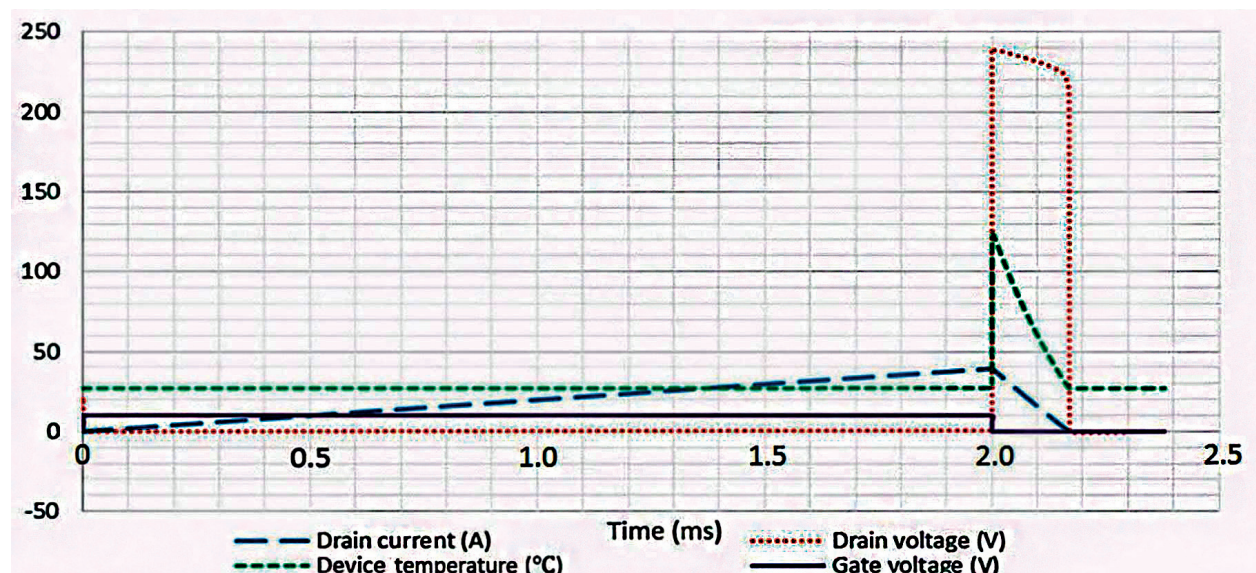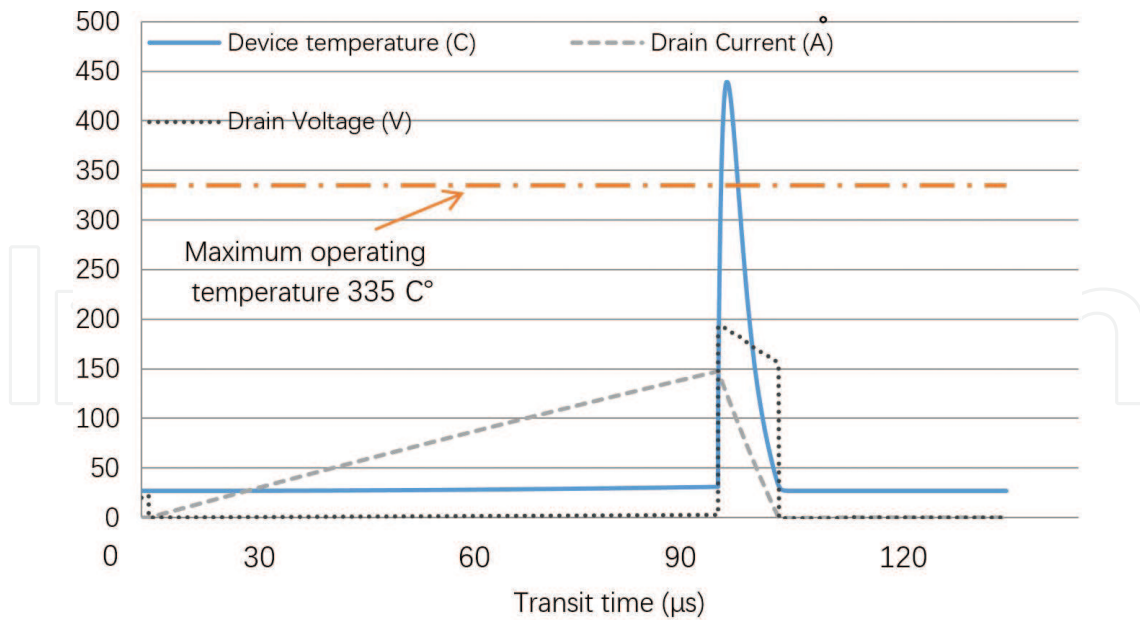

Figure 19. Waveforms under avalanche operation [17].

Figure 20. Waveforms under UIS test conditions when avalanche failure is believed to occur. The maximum operating temperature is 335°C [17].

voltage plummets to zero after the excess heat is dissipated into ambient air. According to Eq. (3), the maximum avalanche current is 40 A, which agrees with the simulation result. Also from **Figure 19**, the avalanche time is 0.18 ms, which agrees with calculation using Eq. (4) where BV is 220 V and VDD is 0 V. The EAS is 800 mJ computed according to Eq. (5), and therefore the avalanche power is 4.4×10^4 W (EAS/t_{av}).

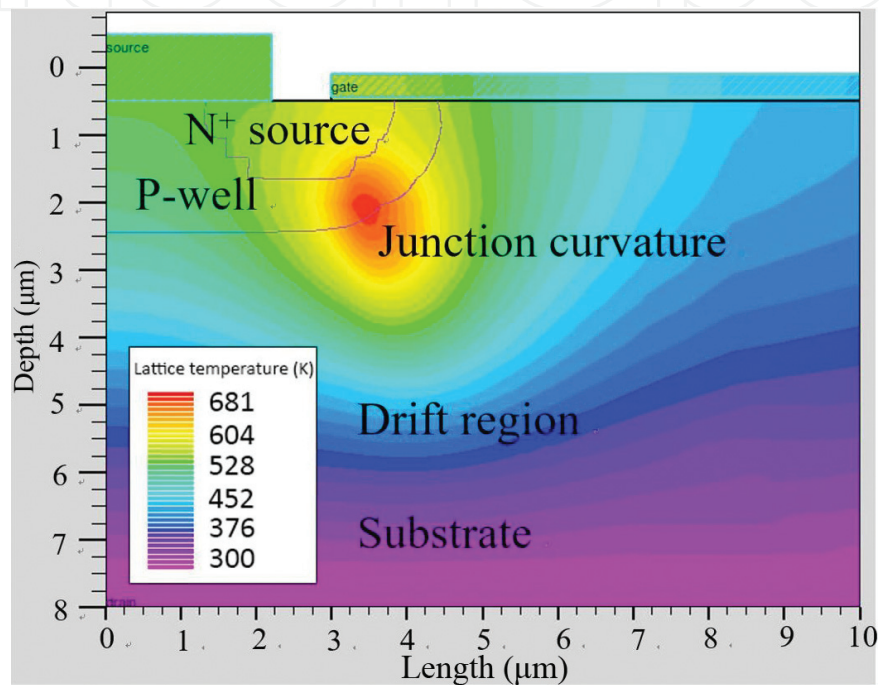### 3.3. Avalanche performance of planar MOSFET

For the Si device under testing (DUT) to survive under avalanche operation, the device junction temperature cannot exceed 335°C [16]. Otherwise, a large proportion of defects would be thermally generated in the epitaxial layer [16]. As a result, current crowding into a localized hot spot would occur on the chip, melting the aluminum around it and thus destroying the device. Upon optical inspection, the majority of the bare die reveals a catastrophic body diode melt down failure (not shown). **Figure 20** shows avalanche operation when the junction temperature exceeds 335°C. Under this condition, the MOSFET is thought to have failed to survive as the semiconductor approaches intrinsic properties at this high temperature. The lattice temperature profile shown in **Figure 21** illustrates a hot spot at the junction curvature between the *p*-well and the *n*-drift region, where avalanche breakdown occurs. A large amount of current passes through this junction curvature and in the process dissipates substantial power so that the local temperature in this region is the highest.

For a given inductance (0.01 mH), the relationship between the initial junction temperature and maximum avalanche current is shown in **Figure 22**. A linear regression of the data indicates that the maximum initial junction temperature is around 350°C, which closely agrees with the threshold for avalanche failure. For constant inductance, the maximum avalanche current is:

$$I_{av(\max)} \propto T_{jM} - T_{j0} \tag{6}$$

where T_{j0} and T_{jM} are the initial and maximum junction temperatures respectively.

Figure 23 shows the inductive load dependence of $I_{av(\max)}$ at an initial junction temperature of 27°C. As expected, the avalanche current capability becomes weaker as the inductive load increases, and this is because the proportionately large amount of energy stored in the inductance is dissipated in the MOSFET as heat, and risks avalanche failure when the critical lattice temperature is exceeded.


Figure 21. Lattice temperature distribution in the power MOSFET [17].
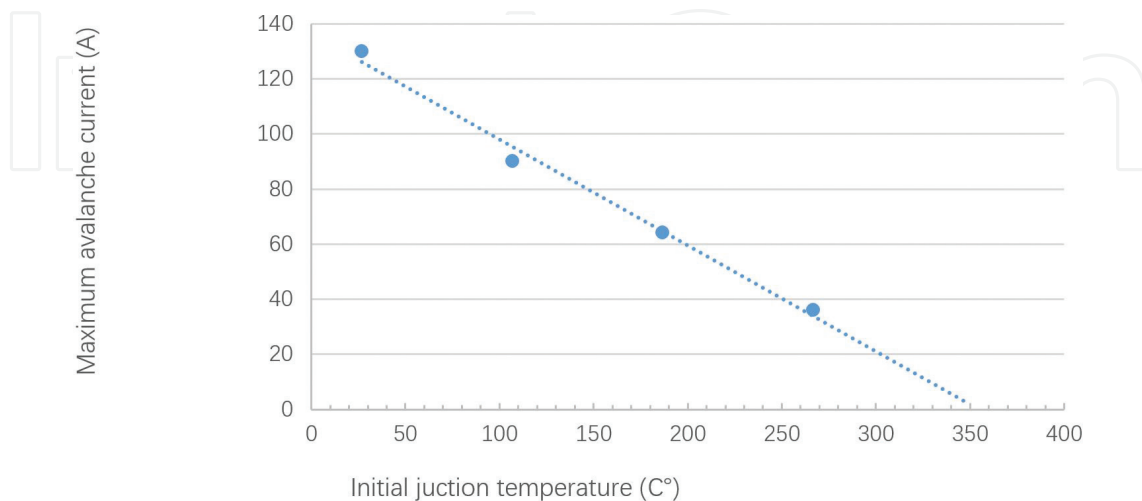

Figure 22. Initial junction temperature and resulting maximum avalanche current [17].

3.4. Avalanche performance of trench MOSFET

The cell pitch of the trench MOSFET can be reduced to 2.5 μm, from the 10 μm of the conventional planar MOSFET. And to maintain the same active area (5 mm^2), the width of the trench MOSFET can also be increased four-fold compared to that of the planar MOSFET. **Figure 24** shows the maximum avalanche current for the planar and trench platforms at an initial junction temperature of 300 K. Clearly, the avalanche current capability of the trench
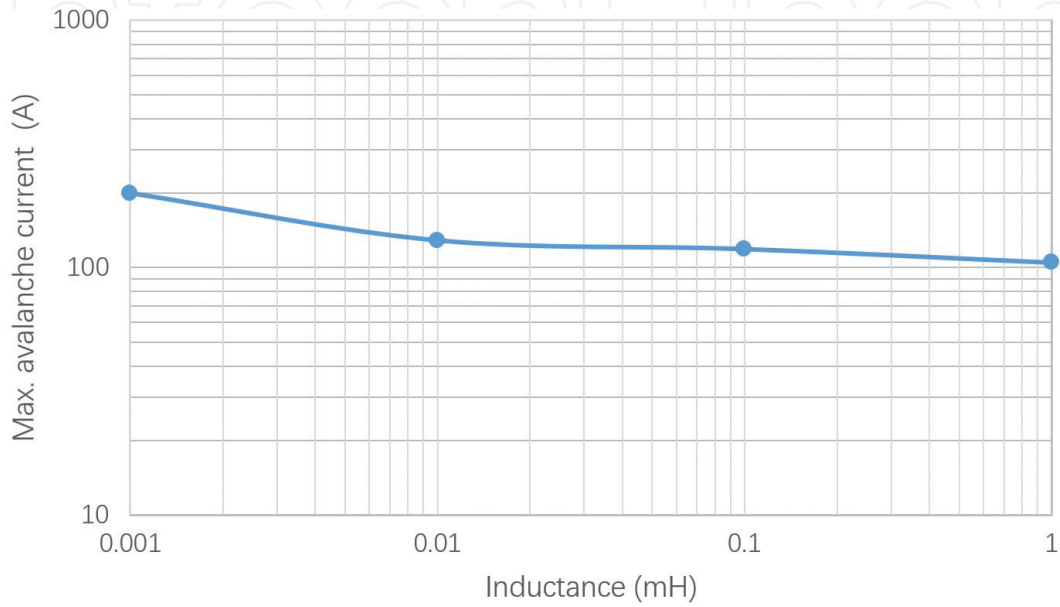
Figure 23. Maximum avalanche current as a function of total inductance [17].
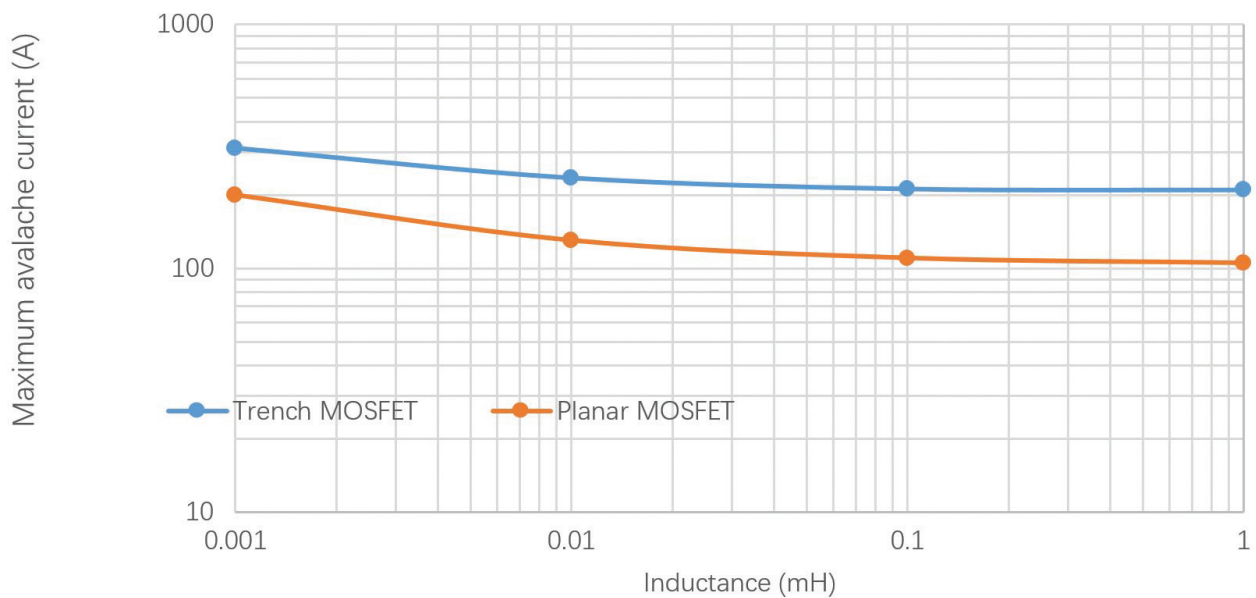
Figure 24. Maximum avalanche current in the planar and trench MOSFETs [17].

variant is 50–100% superior to that of the planar counterpart. **Figure 25** shows that the highest temperature is localized at the planar junction between the *p*-well and the *n*-drift regions, at which point avalanche breakdown occurs.
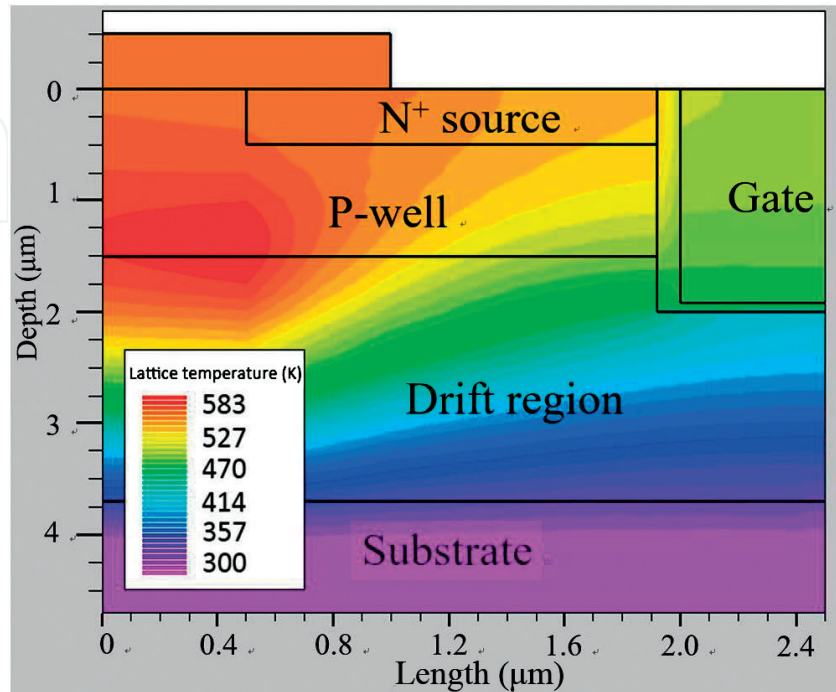

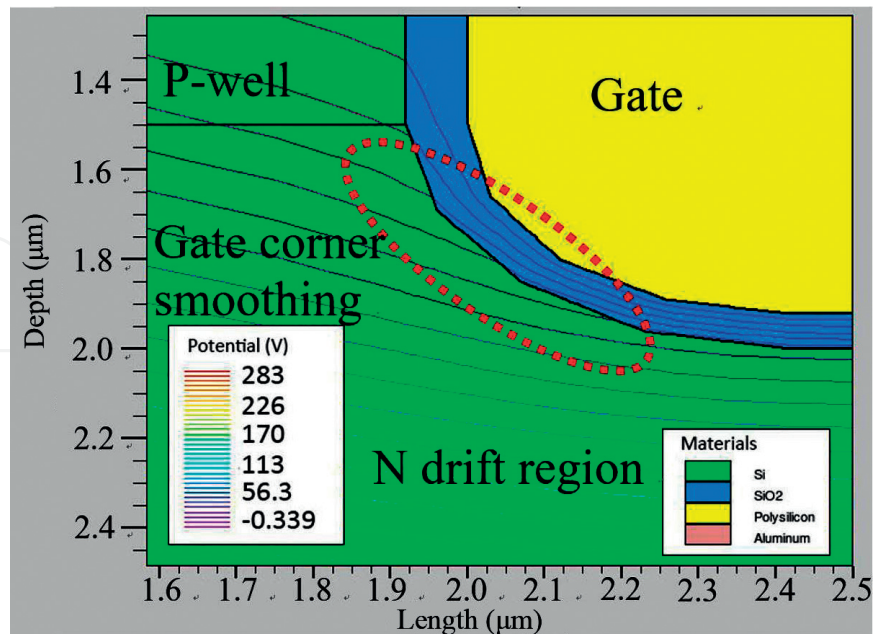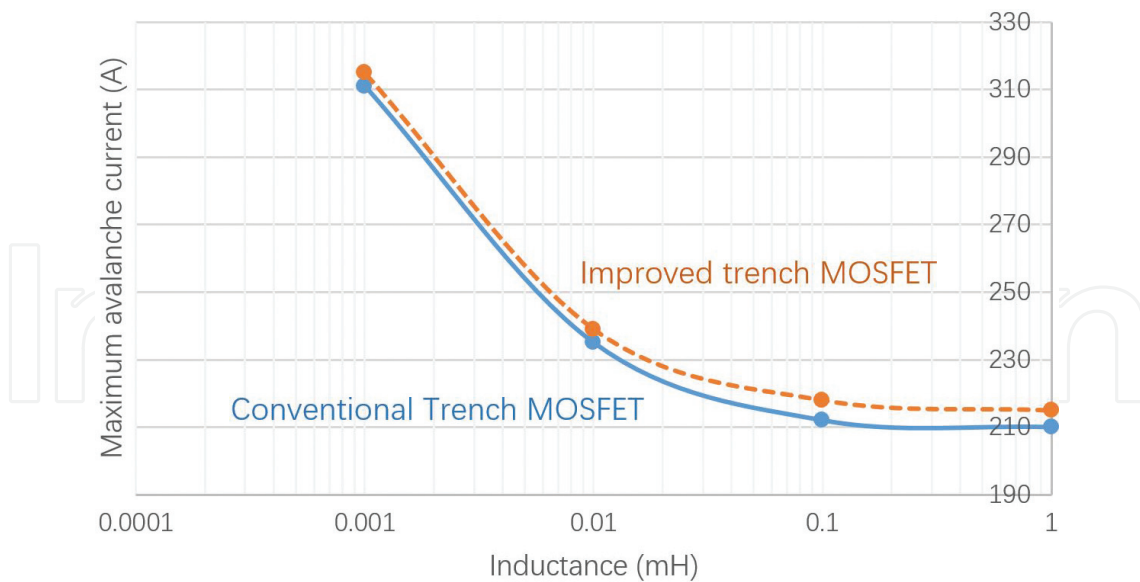**Figure 25.** Temperature distribution in the trench MOSFET [17].

Figure 26. Trench MOSFET with gate corner rounding and potential distribution during avalanche operation [17].

Figure 27. Maximum avalanche current for standard and modified trench MOSFET with rounded gate corners [17].

3.5. Ruggedness improvement of the trench MOSFET

Rounding off the trench gate corners is an approach that can avoid highly intense electric fields under UIS conditions and improve the ruggedness. The resultant potential contours exhibiting less crowding at the edges of the trench gate corner due to the modified design is shown in **Figure 26**. **Figure 27** shows that the maximum avalanche current increases by about 4–10 A per cell using the modified trench gate structure.

4. Conclusions

In this chapter, 50 V rated power MOSFETs based on the planar and trench technologies have been designed, modeled, simulated and compared using industry-standard Technology Computer-Aided Design (TCAD) tools. A survey of some methods to successfully reduce the specific on-resistance has been given. The specific on-resistance can be reduced by 23% through gate width-length optimization of the standard planar Si MOSFET. The increased doping in the JFET region decreases the specific on-resistance by about 8.3% but affects BV. Adopting SiC is more attractive and effective amongst the planar technologies studied where the specific on-resistance can be reduced by *ca.* 31% compared to the planar Si MOSFET. This arises from a shorter cell pitch and heavier doping in the drift region that substantially reduces the drift region resistance. Since the trench MOSFET has no JFET region, optimal design is achievable with a smaller cell pitch. By shrinking the half-cell pitch to 2.5 μm, i.e. reduction by 17% compared to that of the Si planar MOSFET with optimum gate width, the specific on-resistance decreases by more than two-fold. The avalanche ruggedness of the planar and trench MOSFETs has also been evaluated and compared. Experimental microscopy images show notable damage on the die due to avalanche failure. The physical mechanisms that limit

the avalanche capability including self-heating effects have been analyzed and taken into account in the electro-thermal modeling and simulations of the circuit performance. The avalanche ruggedness of the trench MOSFET is significantly better compared to that of the planar MOSFET, exhibiting a 50–100% increase in avalanche current capability. For further ruggedness enhancement, the corners of the trench gate may be rounded off to smoothen out the electric field peaks at the edges under UIS conditions. This is expected to increase the maximum avalanche current capability by up to about 3% per cell. However, it may be argued that although the benefit in rounding the trench gate corners scales with the cell density and die size to handle high current levels, it may be outweighed by the additional process costs. Further, due to model simplifications (e.g. one- or two-dimensional finite-element modeling), the simulations investigate the first order effects but do not consider the second or higher order effects. Therefore for more accurate baseline models, the designed edge termination such as the field guard ring structure (see **Figures 9** and **10**), for example, should be taken into account in the simulations and calibrated by the experimental data. Finally, it is crucial to have well designed packaging, such as the bond wires that are imperative to handle high current levels.

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