Chapter 4

A Generalized Voltage Control Algorithm for Smooth Transition Operation of Microgrids

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Additional information is available at the end of the chapter

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Abstract

The chapter proposes a generalized control algorithm that can reject the disturbances associated with microgrid transition operation to facilitate smooth microgrid transition operation. Firstly, the literature review of the state-of-the-art gives a deep analysis of the disturbances associated with microgrid transition operation and it reveals that the same controller should be adopted in the inverter control layer to prevent some harmful transients during transition. Then, a generalized voltage control algorithm in inverter control layer that can achieve smooth transition of microgrid is developed including the formulation of the problem, description of the design methodology and design procedures, and analytical study. The salient feature of the developed generalized voltage control algorithm is that the disturbances associated with microgrid transition are fully cancelled by using inverse dynamic model, and the inverter control layer can be seen as a bypass for the application layer. The practical feasibility of the proposed control algorithm is demonstrated by implementing and testing in a signal level hardware-in-the-loop (HIL) platform.

Keywords: microgrid transition operation, inverter control, inverse dynamic model, voltage control

1. Introduction

According to a survey performed by Microgrid Knowledge, electric reliability is the number one reason customers install microgrids, thanks to their ability to provide uninterrupted power supply (in particular, for critical loads) when the utility is lost. For this reason, a microgrid should be controlled to operate both in grid-connected and in islanded mode, as well as to transit seamlessly between the two [1–3]. In the transition between grid-connected and islanded mode, two types of disturbances are expected to occur and therefore the controller of the inverter may have to deal with (1) frequency disturbances related to a sudden change

of the angle/frequency reference for the inverter control, and (2) current and voltage disturbances associated with switching between different operating modes [4]. Therefore, the inverter controller should reduce the impact from those disturbances to acceptable limits, or, at best case, eliminate them completely.

For the first type of disturbance, the seamless transfer techniques focus on the application layer and the essential effort is to improve power angle/voltage transients during transition. Thanks to the smooth modifications of the references (i.e. frequency, voltage and current) for the inverter layer (voltage and current controller), smooth transition operation can be achieved. As for the second type of disturbance, extensive research works have been undertaken in the inverter controller to improve the disturbance rejection performance. However, the impact from the disturbances can only be reduced and the robustness of these controllers is not guaranteed during the transition of different operating modes.

Motivated by the research gap, a novel inverter control algorithm is developed based on the inverse dynamic model of the *LC* filter and the inverter, transforming the closed loop transfer function of the inverter control level into the 'unitary gain'. The inverter controller with the unitary gain property automatically eliminates the second type of disturbance during the microgrid transition operation; therefore, smooth transition operation is achieved.

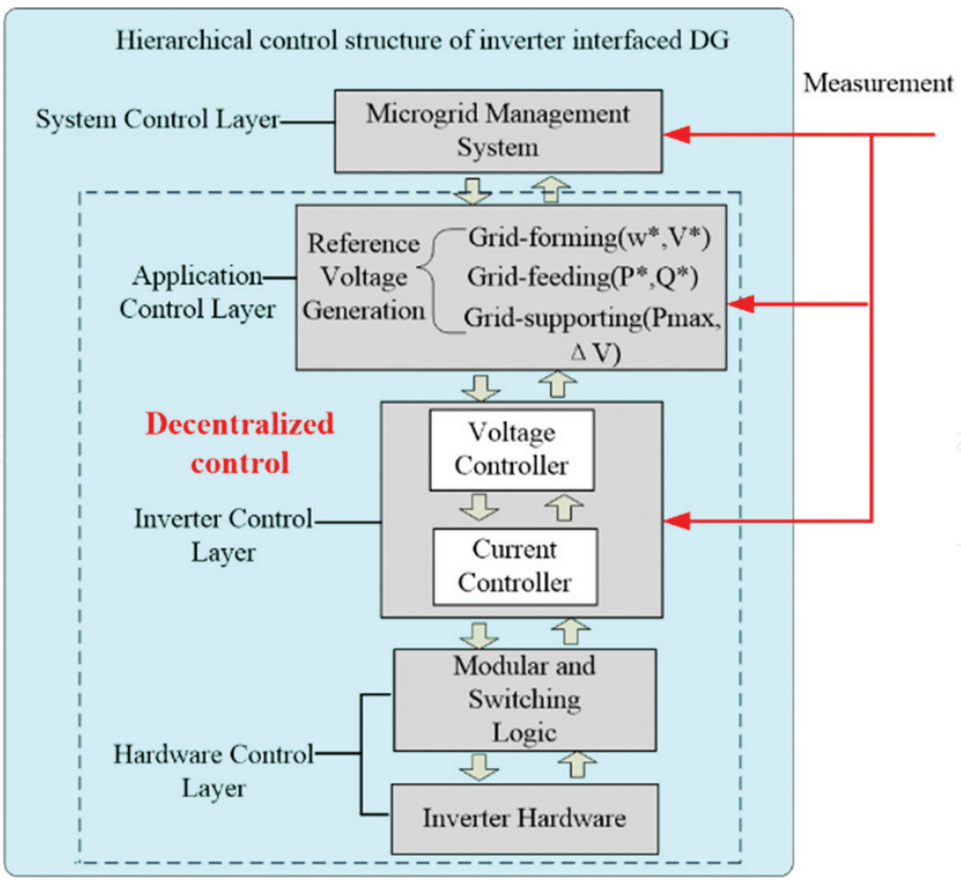

Figure 1. Modified control structure for DGs in microgrid operating in different modes.

2. A generalized control architecture for DGs in microgrid

The control structure for DG interface in microgrids is mapped in **Figure 1** according to the IEEE Std. 1676, compatible with all the microgrid operation modes [5]. The highest layer, the system control layer, is implemented in microgrid central controller (energy management system (EMS)). The lower layers are locally applied in decentralized controller of each DG unit.

The main task of the system control layer is to manage the operation modes (grid-forming, grid-feeding and grid-supporting mode) of DGs in microgrid based on the network characteristic and distribution network operator (DNO)'s request and then to send the corresponding reference signals and control commands to the application and the inverter control layers. The application control layer generates a specific voltage reference for the inverter layer according to the chosen operation. The inverter control layer executes the commands to fulfil the task set by the system control layer, and it hosts the proposed generalized voltage controller, designed to reject the current/voltage disturbances associated with microgrid transition operation. The functions of the hardware control layer of inverter can reference the IEEE Std. 1676 for PEBB system.

3. Key challenge and a promising solution: an intelligent control algorithm in inverter control layer

As stated in Section 1, the key challenge in designing a controller to reject the harmful voltage and current transients caused by the shift of microgrid operation mode is in the design of the inverter layer control algorithm. Microgrids in islanded mode and grid-connected mode applications have been considered in the past separately from the point of view of control design in the inverter control layer. This control strategy causes unnecessary harmful transients in the control system [5, 6]. Moreover, the commonly adopted control algorithm in inverter control layer has a non-negligible drawback: if the voltage is controlled, the system performance is sensitive to the output current of the *LC*/*LCL* filter and the output impedance (gain of the output current) of the inverter, which act as disturbances to the output voltage [7]. The same applies to the current control if the control variable is the output current of the *LC*/*LCL* filter. Therefore, a promising solution to solve the issues in the existing control methods is direct voltage control method adopted in the inverter control layer, and a good disturbance rejection strategy should be considered to fully cancel the disturbances in the inverter control layer. As the disturbances in the inverter control system can be measured, full feedforward compensation through inverse dynamic model can be applied to totally cancel the disturbances: a detailed methodology and principles are explained in the following section.

3.1. Principle of inverse dynamic model

The basic structure of a single-input/single-output plant using the inverse dynamic model feedforward is shown in **Figure 2**. The plant input u is composed of two parts: the feedback control input u_d and the inverse dynamic model u_f. The inverse dynamic model $G_i(s)$ is used in the feedforward path of the controller to compute the desired actuator inputs u_f to the plant.

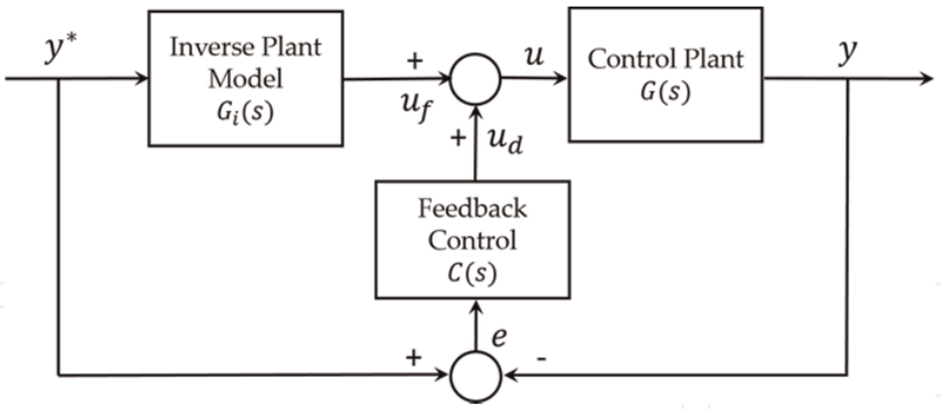

Figure 2. Control structure with inverse plant model in the feedforward path.

The feedback control $C(s)$ eliminates the tracking error. The feedforward control and feedback control can be designed separately, which follows the design concept of the two-degree-of-freedom control.

The transfer function of the above system is given by

$$\frac{y}{y^*} = \frac{G(s)G_i(s) + G(s)C(s)}{1 + G(s)C(s)} \tag{1}$$

If an accurate inverse model of the plant is obtained ($G_i(s) \equiv G^{-1}(s)$) and in a proper form, then the transfer function of the controlled system has a unitary gain for all frequencies. Thus, all the internal disturbances imposed upon the controlled output are fully cancelled.

3.2. Control strategy in the inverter control layer

Different control strategies in the application layer regulate different outputs of the DG (e.g. desirable active and reactive power generation, voltage and frequency regulation, and maximum active power injection). Essentially, these control strategies translate the various outputs into references for the injected current or the terminal voltage in the inverter control layer. To achieve universality, a new inverter control algorithm is required to control either one of these variables in a flexible way. As the impedance between the DG and the grid is a known parameter and the main grid voltage is an external measurable variable, the injected DG current can be indirectly regulated by controlling the terminal voltage [5]. Thus, universality is attained by introducing a voltage-based control algorithm into the inverter control layer.

By integrating disturbance rejection and universality of the control algorithm in the inverter control layer, a control algorithm based on the inverse dynamic model method is developed [5]. The control structure of this algorithm is presented in **Figure 3**. As seen in the figure, the control algorithm includes double loops: outer voltage and inner current loop. The inverse dynamic model 1 shows the analytical relationship between the inverter output voltage v_o and the inverter current i_i and also illustrates the input-output relationship between them. To compel the control system to achieve the target output v_o^*, the corresponding control input i_{iff}^* needs to be brutally imposed on the system. Incorporating the additional feedback control

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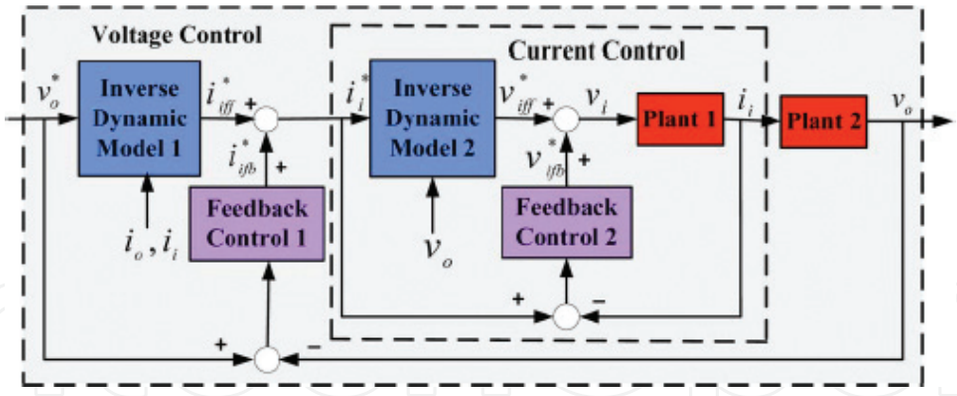

Figure 3. Control structure of the developed intelligent control algorithm using inverse dynamic model.

block 1, the closed loop transfer function of the outer loop is 'unitary gain'. The inner current loop respects the same design strategy and achieves also the closed loop transfer function with 'unitary gain'.

4. Design of the inverter layer control algorithm

The design of the generalized voltage control algorithm in the inverter control layer is based on the model of the *LC* filter and the inverter (the inverter is treated as a gain '1'). **Figure 4** shows the circuit diagram of the DG interface and *LC* filter together with the simplified structure of the control algorithm in the inverter control layer. All the variables are represented in *synchronous frame* and the dynamics of the *LC* filter are formulated in Eqs. (2)–(5):

$$\frac{di_{id}}{dt} = -\frac{R_f}{L_f} i_{id} + \frac{1}{L_f}(v_{id} - v_{od}) + \omega_o i_{iq} \tag{2}$$

$$\frac{di_{iq}}{dt} = -\frac{R_f}{L_f} i_{iq} + \frac{1}{L_f}(v_{iq} - v_{oq}) - \omega_o i_{id} \tag{3}$$

$$\frac{dv_{od}}{dt} = -\frac{1}{C_f}(i_{id} - i_{od}) + R_c\left(\frac{di_{id}}{dt} - \omega_o i_{iq}\right) - R_c\left(\frac{di_{od}}{dt} - \omega_o i_{oq}\right) + \omega_o v_{oq} \tag{4}$$

$$\frac{dv_{oq}}{dt} = -\frac{1}{C_f}(i_{iq} - i_{oq}) + R_c\left(\frac{di_{iq}}{dt} + \omega_o i_{id}\right) - R_c\left(\frac{di_{oq}}{dt} + \omega_o i_{od}\right) - \omega_o v_{od} \tag{5}$$

where i_{id}, i_{iq} ,i_{od}, i_{oq} are the inverter currents and inverter output currents in the *dq* frame, respectively, and v_{id}, v_{iq}, v_{od} ,v_{oq} are the inverter voltages and inverter terminal voltages in the *dq* frame, respectively. R_f, L_f, C_f and R_c are the per-phase resistance, inductance and capacitance of the *LC* filter.

By using Laplace transformation, we obtain the transfer functions for the inverter current and inverter terminal voltage:

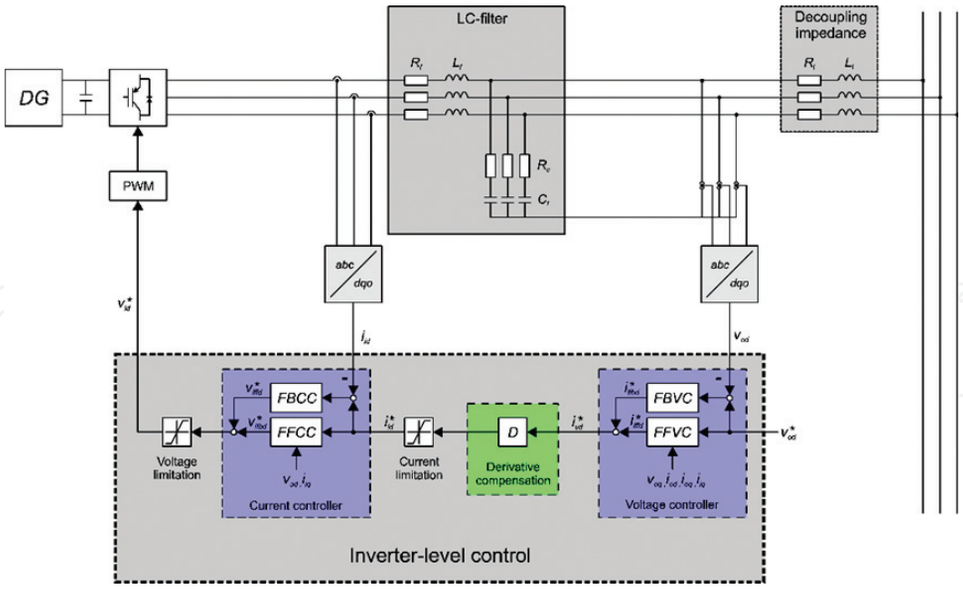

Figure 4. Circuit diagram and control structure of the inverter control layer.

$$i_{id} = \frac{1}{sL_f + R_f}(v_{id} - v_{od} + \omega_o L_f i_{iq}) \tag{6}$$

$$i_{iq} = \frac{1}{sL_f + R_f}(v_{iq} - v_{oq} - \omega_o L_f i_{id}) \tag{7}$$

$$v_{od} = \left(\frac{1}{sL_f} + R_c\right)(i_{id} - i_{od}) - \omega_o \frac{R_c}{s}(i_{iq} - i_{oq}) + \frac{\omega_o}{s} v_{oq} \tag{8}$$

$$v_{oq} = \left(\frac{1}{sL_f} + R_c\right)(i_{iq} - i_{oq}) + \omega_o \frac{R_c}{s}(i_{id} - i_{od}) - \frac{\omega_o}{s} v_{od} \tag{9}$$

It becomes evident that the system described above is highly coupled. For instance, the currents are functions of both voltages and the coupling terms of voltage, the latter of which interferes with voltage as well. The block in **Figure 5** shows the coupled system and resistance of the LC filter.

The dynamics of the *LC* filter can be expressed as one equation for the inverter current and one for the terminal voltage for each component. This structure suggests a cascaded control structure for the inverter control containing one inner current loop and one outer voltage loop. In the controller design, the inverter current i_i and the output voltage v_o are the controlled variables for current controller and voltage controller, respectively. The choice of the voltage loop as outer loop is a natural consequence of the fact that the inverter output voltage is the filter's outermost variable. The general idea is to force the controlled variables to quickly follow the reference signal and to be robust against disturbances and coupling terms. At the same time, in order to achieve maximum transparency to higher control levels, the proposed controller is designed in such a way that both the current closed loop and voltage closed loop have a unitary transfer function. Therefore, all effects of disturbances are removed and the inverter is

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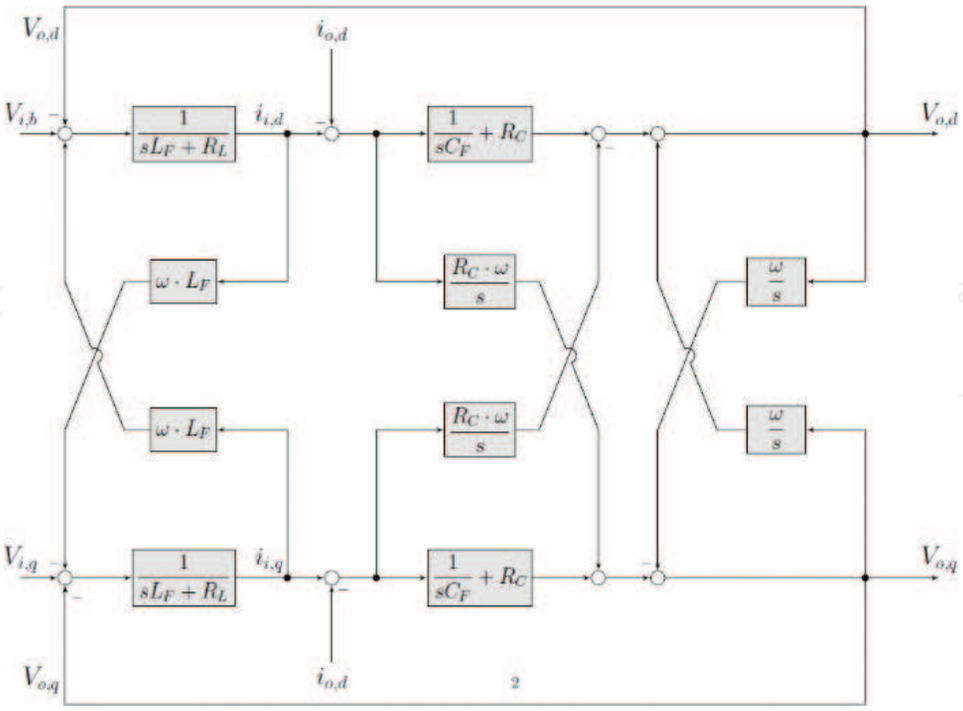

Figure 5. Block diagram of dynamics of the *LC* filter.

theoretically transformed into a virtual bypass to the current or voltage reference signal. Once this is achieved, the whole inverter can be operated as a perfectly controllable voltage source.

Figure 6 illustrates the abstract control structure of a controlled variable in d axis (i_{id} and v_{od}) containing all the blocks: the inverse dynamics feedforward control, feedforward control of disturbance, feedback control and decoupling effects. There are two different implementations as shown in **Figure 6**: the parallel and the series connection of the FF and FB blocks. As the series implementation results in more complex internal dynamics and it is more vulnerable to measurement noises, both current and voltage control have been implemented using the parallel connection. An important assumption made is that we neglected the dynamics of the inverter, thus making the inverter act as bypass ($v_i^* = v_i$) as well. This approximation is valid since advanced synchronized sampling techniques can reduce the time-delay of inverter digital implementation to $0.25T_{sampling}$ [8]; thus, the inverter can be approximated as a unitary gain without delay. If the control for inverter could be successfully implemented according to the strategy shown in **Figure 6** (top), the inverter's control algorithm would yield the closed loop system displayed in the block diagram shown in **Figure 4**.

Figure 4 shows the simplified control block of the cascaded voltage and current controller in inverter control layer, which is in line with the structure illustrated in **Figure 3**. The outer voltage loop has two components: FBVC and FFVC denote feedback voltage control and feedforward voltage control, respectively. The inner current loop consists of two components: FBCC and FFCC, standing for feedback current control and feedforward current control, respectively. The feedforward control is a crucial element in this control system, which contains the inverse dynamic model of the *LC*-filter shown in Eqs. (2)–(5) and its main effect is

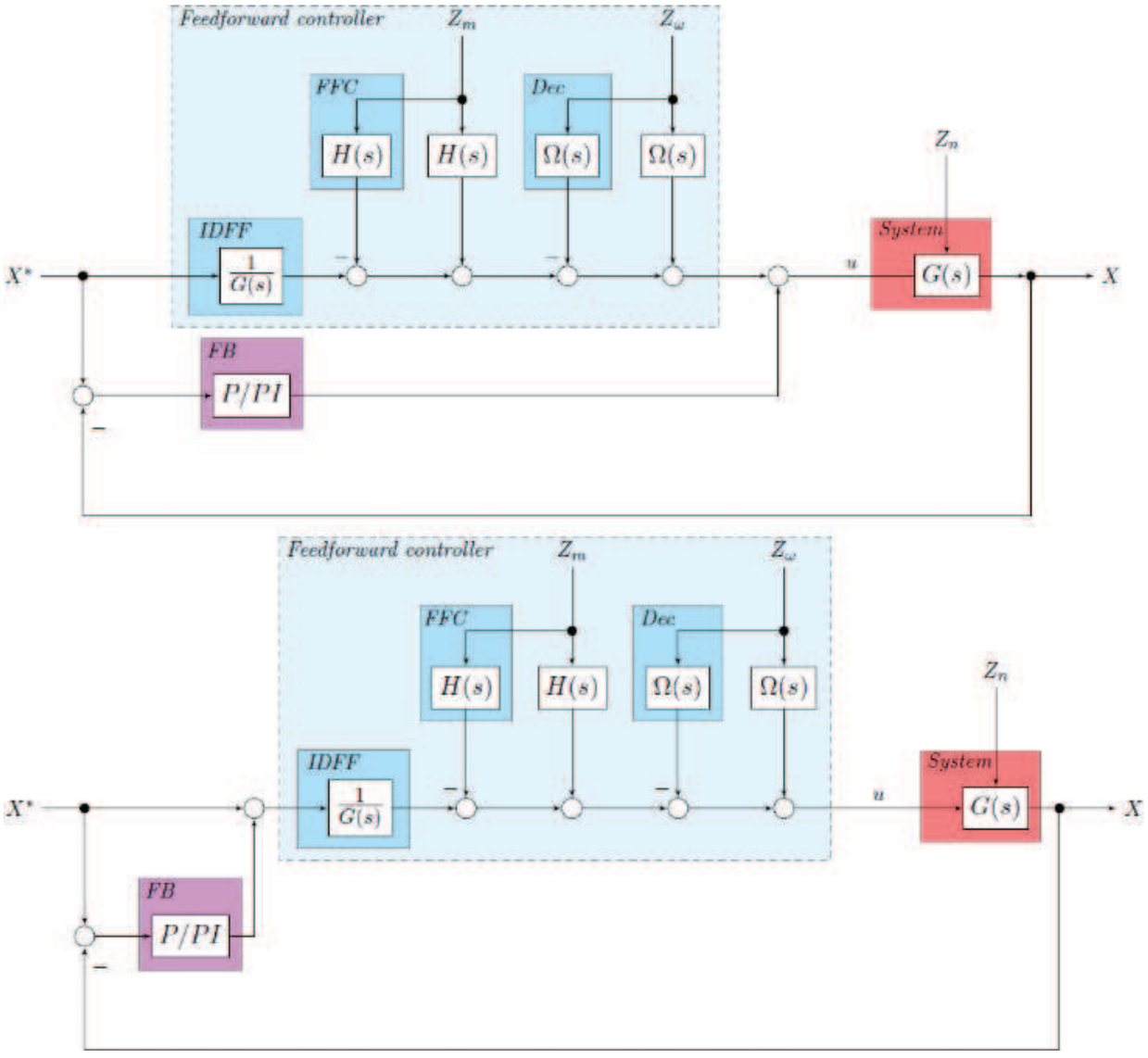

Figure 6. Abstract structure of the proposed control algorithm and its components. Parallel (top) and serial (bottom) connection of feedback and feedforward control.

to perform ideal compensation of the filter's dynamics within each loop. A deeper insight into the feedforward control indicates that there are three components in each loop. The first component consists of the decoupling elements; these remove the coupling between the d and q variables. The second is the disturbance compensation; this eliminates the effect of measurable variables acting as disturbances to each loop (including an active damping function based on back electromotive force (EMF)-decoupling). Finally, the third component counteracts the dynamics of the control path, transforming the dynamics of the controlled variable into a virtual bypass for the reference value [9, 10].

4.1. Inner current loop controller

The inner current control loop is seen as a bypass in the perspective of the outer voltage control loop. Accordingly, the following relationship should hold:

$$i_{id} = i_{id}^*,\ i_{iq} = i_{iq}^* \tag{10}$$

In order to achieve this, the feedforward component of the current control simply inverts the dynamics described in Eqs. (6) and (7) and then we obtain the following control law for the feedforward component v_{iff}^*:

$$v_{iffd}^* = (sL_f + R_f)i_{id}^* - \omega_o L_f i_{iq} + v_{od} \tag{11}$$

$$v_{iffq}^* = (sL_f + R_f)i_{iq}^* + \omega_o L_f i_{id} + v_{oq} \tag{12}$$

These equations could already be used directly as the control law for current control. They include the inverse dynamic feedforward term for the reference current signal. This feedforward term compensates the inverter disturbances including the terminal voltage and coupling elements.

Nonetheless, the first term in Eq. (11) and (12) contains a component with differential behaviour (denoted by the Laplace operator). It is not recommended to employ this control law in the inner control loops which could directly amplify and feed the high-order harmonics in the inverter system which in the end results in undesirable low-order harmonics. In the worst case, this derivative term could lead to unacceptable THD or even instabilities to the control system. Furthermore, the equations must include a feedback term to cancel the deviation between the actual output and the reference current. A P-control is parallel connected to the feedforward control. The use of a P-control instead of a PI-control can be explained by the fact that the steady-state error in the inner loop is automatically sensed and compensated by the outer control loop with the cascaded structure. The feedback controls of the inner current loop are given by

$$v_{ifbd}^* = K_{CP}(i_{id}^* - i_{id})\ ,\ v_{ifbq}^* = K_{CP}(i_{iq}^* - i_{iq}) \tag{13}$$

Therefore, after deleting the derivative element in the feedforward original control law, the updated control law for the current control including the P-control is given by

$$v_{id}^* = v_{iffd}^* + v_{ifbd}^*\ , v_{iq}^* = v_{iffq}^* + v_{ifbq}^* \tag{14}$$

where K_{cp} is the proportional gain of the feedback control.

The transfer function for the inner loop can be obtained by substituting Eq. (14) into Eq. (6) and (7), and then we obtain

$$i_{id} = \frac{R_f + K_{cp}}{s \cdot L_f + R_f + K_{cp}} i_{id}^*, i_{iq} = \frac{R_f + K_{cp}}{s \cdot L_f + R_f + K_{cp}} i_{iq}^* \tag{15}$$

4.2. Outer voltage loop controller

In an analogous manner, the closed loop of the voltage controller can be designed as a bypass for the application layer controller as well. Therefore, the closed loop transfer function of the voltage controller is expressed in the form of 'unitary gain' shown as follows:

$$v_{od} = v_{od}^*,\ v_{oq} = v_{oq}^* \tag{16}$$

Therefore, the same strategy will be applied in the design of the voltage control law. The control algorithm is obtained by substituting Eqs. (4) and (5) into Eq. (16) and rearranging in terms of the reference for the inverter current. As shown in **Figures 3** and **4**, the voltage controller includes both feedforward control and feedback control. The control laws of the outer voltage loop are formulated as follows:

$$i_{iffd}^* = \frac{s \cdot C_f}{1 + s \cdot C_f \cdot R_c} v_{od}^* - \frac{C_f}{1 + s \cdot C_f \cdot R_c} v_{oq} + \omega_o \frac{C_f R_c}{1 + s \cdot C_f \cdot R_c} i_{iq} - \omega_o \frac{C_f R_c}{1 + s \cdot C_f \cdot R_c} i_{od} + i_{od} \tag{17}$$

$$i_{iffq}^* = \frac{s \cdot C_f}{1 + s \cdot C_f \cdot R_c} v_{oq}^* + \omega_o \frac{C_f}{1 + s \cdot C_f \cdot R_c} v_{od} - \omega_o \frac{C_f R_c}{1 + s \cdot C_f \cdot R_c} i_{id} + \omega_o \frac{C_f R_c}{1 + s \cdot C_f \cdot R_c} i_{od} + i_{oq} \tag{18}$$

$$i_{ifbd}^* = \frac{s \cdot K_{vp} + K_{vi}}{s}(v_{od}^* - v_{od}),\ i_{ifbq}^* = \frac{s \cdot K_{vp} + K_{vi}}{s}(v_{oq}^* - v_{oq}) \tag{19}$$

where K_{vp} and K_{vi} are the proportional and integral gains of the voltage feedback control, respectively. The reference current generated by the voltage controller is given by

$$i_{vcd}^* = i_{iffd}^* + i_{ifbd}^*,\ i_{vcq}^* = i_{iffq}^* + i_{ifbq}^* \tag{20}$$

4.3. Unitary transfer function compensation

Based on Eqs. (16)–(20), the transfer function of the voltage controller is unitary, whereas the transfer functions of the current controller are given by Eq. (15).

In order to improve the system's stability and dynamic performance, it is necessary to make the inner current loop appear as a unitary gain from the perspective of the outer voltage loop. A derivative compensation is used between the voltage controller and the current controller to make the current transfer function also equal to unitary gain. The transfer functions of the derivative compensation are obtained by inverting the inner loop transfer functions represented in Eq. (15)

$$\frac{i_{id}^*}{i_{ivd}^*} = \frac{i_{iq}^*}{i_{ivq}^*} = \frac{s \cdot L_f + R_f + K_{cp}}{R_f + K_{cp}} = D(s) \tag{21}$$

By substituting Eq. (15) into Eq. (21), the transfer function of the current controller is equal to the ***unitary gain***. In digital implementation, the derivative compensation should operate at the same bandwidth as the voltage control. As we have $R_f + K_{cp} \gg L_f$, we have $i_{id}^* \quad i_{ivd}^*$ and $i_{iq}^* \quad i_{ivq}^*$. The derivative term would not cause significant distortion in case there is nonlinear load connected.

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5. Analysis of the voltage control algorithm in the inverter control layer

5.1. Analytical verification of the closed loop transfer function

Analytical verification is provided here to derive the closed loop transfer function of the inverter control layer, and to prove that the design target is satisfied. A simplified structure of the double-loop controller is presented in **Figure 7**. W_1 represents the control plant of the inner loop and its formula is shown in Eq. (6) and (7). W_2 represents the control plant of the outer loop and its formula is shown in Eq. (8) and (9). Only derivation process in d-coordinate is presented and it is shown in **Figure 8**. Following the steps listed in **Figure 8**, we can obtain the closed loop transfer as designed, $v_{od}(s) = v_{od}^*(s)$.

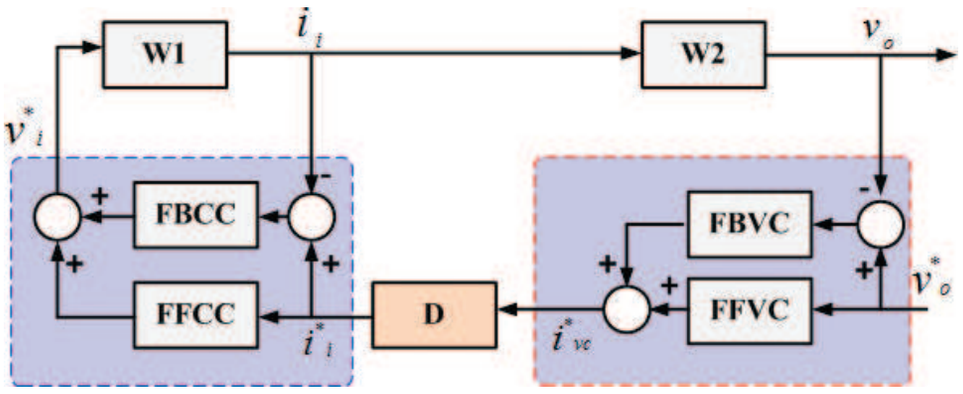

Figure 7. Simplified structure of the control algorithm in the inverter layer.

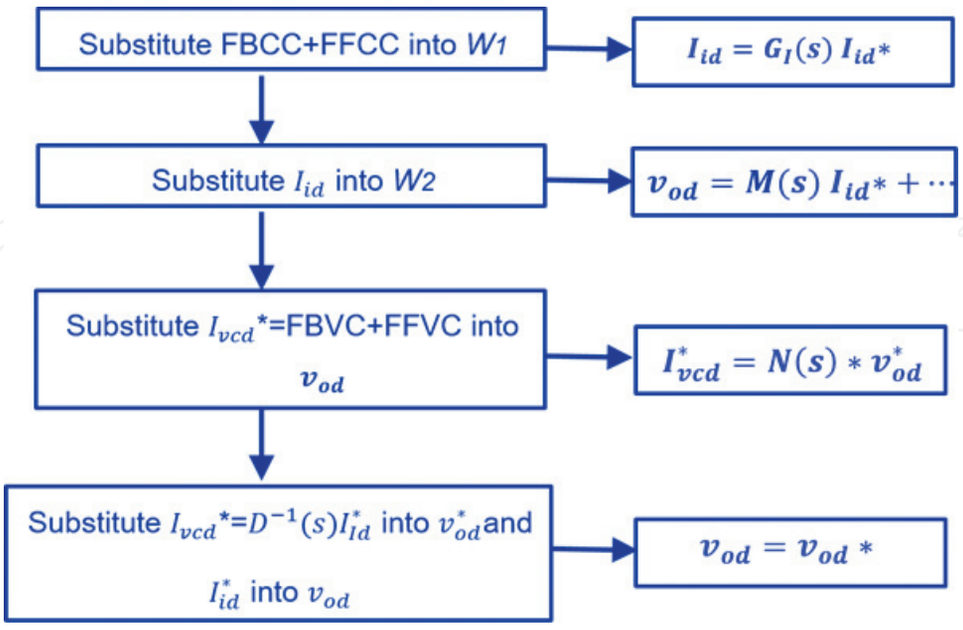

Figure 8. The derivation process of the closed loop transfer function.

5.2. Sensitivity analysis

The developed voltage control algorithm in the inverter layer is model-based control method, which requires very accurate modelling of the control plant together with correct parameters. If there is mismatch between the estimated plant parameter and the real one, the reverse model would not perfectly compensate for the plant's dynamics and transform the open loop into a unitary gain. As a result, disturbance terms would appear in the closed loop transfer function, which degrades the steady-state and transient performance. In this sensitivity analysis, how the stability and control performance of the proposed controller is affected by the variations of the control plant parameters (e.g. C_f and L_f) is investigated.

Assuming that the capacitance of the physical plant is C_f and the estimated capacitance of the inverse dynamic model for the control system is C'_f, we can derive the following closed loop transfer function:

$$v_{od} = v_{od}^* + \frac{\left(\frac{C'_f}{C_f} - 1\right)s}{(C'_f + K_{vp}C'_f R_c)s^2 + (K_{vp} + K_{vi}C'_f R_c)s + K_{vi}}(i_{id} - i_{od}) \tag{22}$$

From Eq. (22), it can be seen that the output v_{od} is a function of the reference input v^*_{od} and the disturbance i_{id}-i_{od}. The system stability is not degraded by variations of C_f as that the poles of the transfer function for the disturbance i_{id}-i_{od} are always in the left-half-plane regardless of variations of C_f. The closed loop performance is evaluated by the magnitude bode diagram of the transfer function for the disturbance for different C_f values, as shown in **Figure 9**. It can

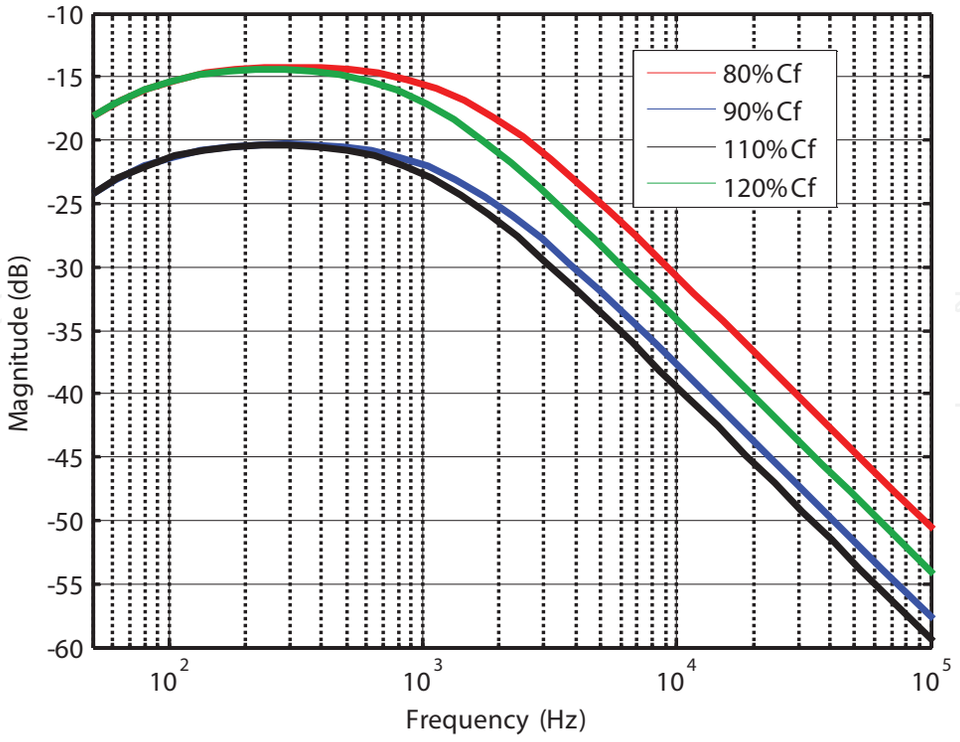

Figure 9. Gain magnitude curve of disturbance (i_{id}-i_{od}) caused by C_f variation.

be observed that the effect of modelling mismatch caused by variations of C_f is very small since the gain magnitude is below −15 dB for all frequencies.

If the inductance of the real plant is L_f and the inductance of the inverse dynamic model is L'_f, the transfer function of the inner current loop is given by

$$i_{id} = \frac{L'_f s + R_f + K_{cp}}{L_f s + R_f + K_{cp}} i^*_{id} + \frac{\omega_o (L_f - L'_f)}{L_f s + R_f + K_{cp}} i_{iq} \tag{23}$$

and the derivative compensation term is

$$D'(s) = \frac{i^*_i}{i^*_{vc}} = \frac{sL'_f + R_f + K_{cp}}{R_f + K_{cp}} \tag{24}$$

Therefore, the closed loop transfer function of the whole system is given by

$$v_{od} = \frac{A(s) + B(s)}{1 + B(s)} v^*_{od} - \frac{(1 + sC_f R_c)(1 - A(s))}{sC_f (1 + B(s))} i_{od} + \frac{\omega_o (1 + sC_f R_c)(L_f - L'_f)}{sC_f (1 + B(s))(L_f s + R_f + K_{cp})} i_{iq} \tag{25}$$

where $A(s) = \frac{(R_f + K_{cp} + sL_f)^2}{(R_f + K_{cp} + sL_f)(R_f + K_{cp})}$, $B(s) = \frac{1 + sC_f R_c}{sC_f} A(s) \frac{K_{vp} s + K_{vi}}{s}$.

The stability of the system is studied by checking the position of the poles of each input expressed in Eq. (25) (v^*_{od}, i_{od}, i_{iq}) when L_f varies from 80 to 120% of L'_f. The results show that all the components have the same dominant poles (−409) with variations of L_f. Consequently, the stability of system is not degraded with mismatches between L_f and L'_f. The closed loop performance of the system is analysed with the bode plots for each individual input in Eq. (25). It can be observed in **Figure 10(a)** that the gain for the reference tracking at the fundamental frequency is equal to the unitary gain. The magnitude of the disturbance caused by the output current i_{od} is very low over the frequency range of interest, so that it has little influence on the system's performance. The magnitude of the disturbance caused by the coupling component i_{iq} is also quite low and almost negligible over the frequency range of interest.

The sensitivity study to variations of C_f and L_f indicates that the stability of the system will not be degraded. However, variations of plant parameter make the system unable to suppress

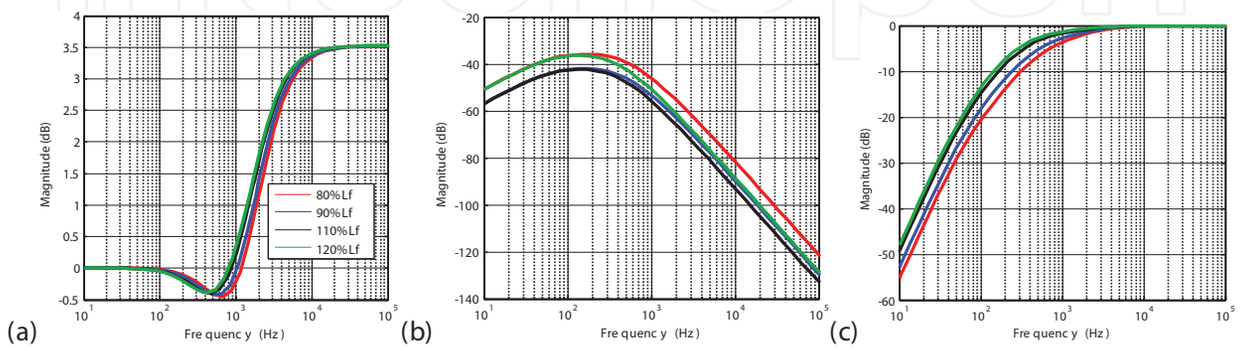

Figure 10. Gain magnitude curves of components of v_{od} caused by L_f variation. (a) Gain of v^*_{od}. (b) Gain of i_{od}. (c) Gain of i_{iq}.

completely all disturbances and degrade the system's reference tracking and disturbance rejection performance. The performance loss, however, is small and acceptable for practical applications.

5.3. Comparison with the conventional voltage controller

For comparison purpose, analysis is also carried out with the cascaded voltage controller proposed in Refs. [2, 6], which is a popularly employed controller in academic and industry. The structure of this conventional voltage controller is shown in [4]. This conventional controller requires the same number of sensors as the proposed controller. The analysis starts from the inner loop current controller. Based on $v_i = v_i^*$, we obtain the following equation (only equation in d-axis is shown here):

$$(sL_f + R_f)i_{id} - \omega_o L_f i_{iq} + v_{od} = K_{cp}(i_{id}^* - i_{id}) - \omega_o L_f i_{iq} + v_{od} \tag{26}$$

After rearranging the above equation, we obtain the closed loop transfer function of the inner loop

$$\frac{i_{id}}{i_{id}^*} = \frac{K_{cp}}{sL_f + R_f + K_{cp}} \rightarrow i_{id} = i_{id}^* \frac{K_{cp}}{sL_f + R_f + K_{cp}} \tag{27}$$

According to the control law for the outer voltage loop, we have

$$i_{id}^* = \frac{K_{vp} + sK_{vi}}{s}(v_{od}^* - v_{od}) - \omega_o C_f v_{oq} + i_{od} \tag{28}$$

Substituting Eq. (28) into Eq. (27), we obtain the following equation:

$$i_{id} = \left(\frac{K_{vp} + sK_{vi}}{s}(v_{od}^* - v_{od}) - \omega_o C_f v_{oq} + i_{od}\right) \frac{K_{cp}}{sL_f + R_f + K_{cp}} \tag{29}$$

Based on the dynamic model of the outer voltage loop, we have the following equation:

$$i_{id} = sC_f v_{od} + i_{od} - \omega_o C_f v_{oq} \tag{30}$$

Following the same logic as the inner loop, we have the following equation:

$$\left(\frac{K_{vp} + sK_{vi}}{s}(v_{od}^* - v_{od}) - \omega_o C_f v_{oq} + i_{od}\right) \frac{K_{cp}}{sL_f + R_f + K_{cp}} = sC_f v_{od} + i_{od} - \omega_o C_f v_{oq} \tag{31}$$

By rearranging the equation, we obtain the closed loop transfer function for the entire system

$$v_{od} = \frac{B_1}{A_1} v_{od}^* + \frac{C_1}{A_1} i_{od} + \frac{D_1}{A_1} v_{oq} \tag{32}$$

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where $A_1 = C_f L_f s^3 + C_f(R_f + K_{cp})s^2 + K_{cp}K_{vp}s + K_{cp}K_{vi}$, $B_1 = K_{cp}K_{vp}s + K_{cp}Kv_i$, $C_1 = -L_f s^2 + \left(\frac{K_{cp}}{sL_f + R_f + K_{cp}}K_{cp} - R_f - K_{cp}\right)s$ and $D_1 = \omega_o L_f C_f s^3 + \omega_o R_f C_f s^2$.

As seen from Eq. (32), the output voltage v_{od} is a function of the reference input v_{od}^* and two disturbance inputs i_{od} and v_{oq}. The two disturbance inputs result in static error and harmonics distortion in the output voltage. **Figure 11** shows the bode plot of the gain of each input. **Figure 11(a)** displays the bode diagram of output voltage to voltage reference closed loop transfer function. It demonstrates that the output voltage can track the reference very well at the fundamental frequency. However, it may amplify the harmonics with frequency around 550 Hz if there are harmonics in the reference voltage. This may happen due to the voltage reference in some applications generated based on some measured variables and power references rather than a fixed value. If there are distortions in the grid, the measured variables can be distorted and then the generated voltage reference can be distorted as well. The gain of i_{od} represents the equivalent harmonic impedance which indicates the main reason of the steady-state error in tracking the target reference. The bode diagram shown in **Figure 11(b)** indicates that the harmonics with frequency around 550 Hz (resonance peak) in the output current will be significantly amplified and results in large distortion in the output voltage. The decoupling

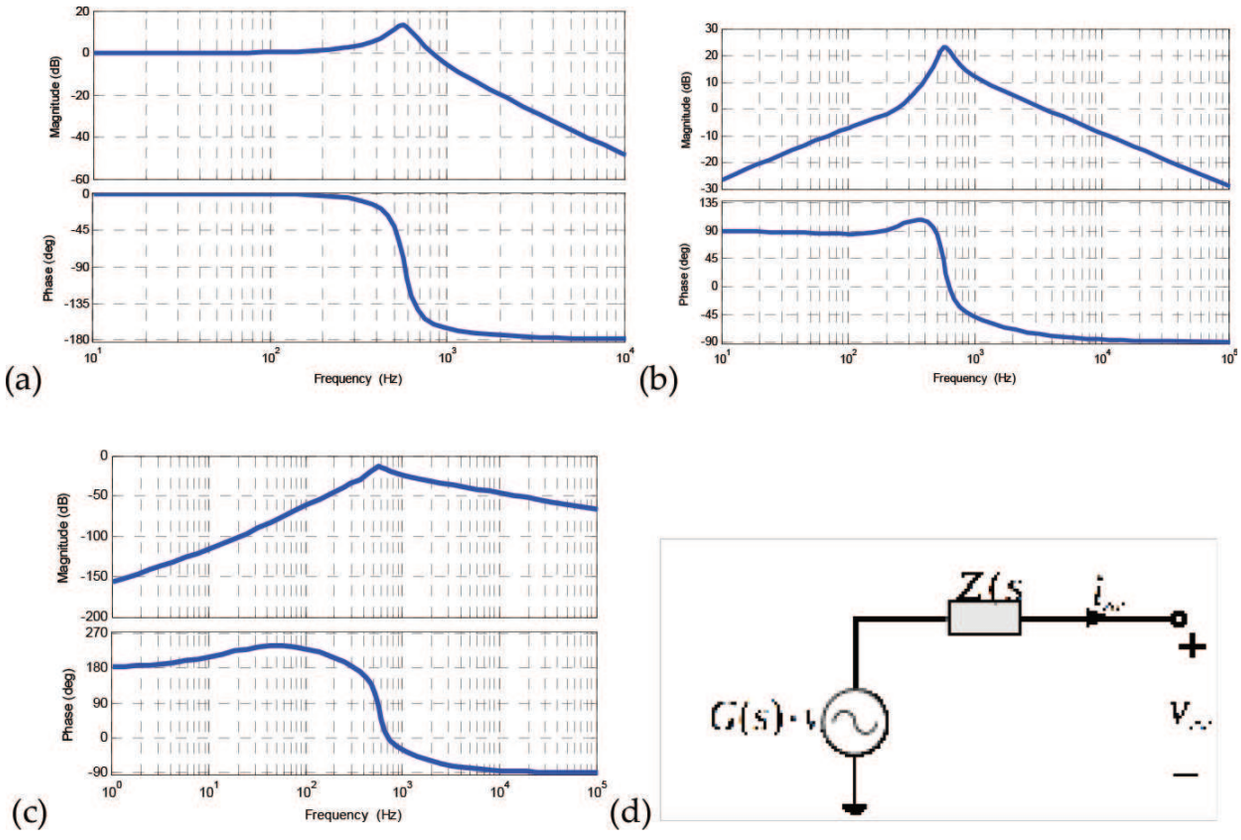

Figure 11. Analytical study of the conventional double-loop voltage controller. (a) Bode plot of the gain of v_{od}. (b) Bode plot of the gain of i_{od}. (c) Bode plot of the gain of v_{oq}. (d) Equivalent circuit of the closed loop system.

term of the output voltage v_{oq} has negligible impact on the output voltage as seen from **Figure 11(c)**. Hence, the output voltage of inverter can be treated as a voltage source series connected with output impedance, which is represented in Figure 5.9(d). $G(s)$ is equal to $\frac{B_1}{A_1}$ and $Z(s)$ is equal to $\frac{-C_1}{A_1}$. In order to achieve fast dynamic response and eliminate steady-state error and voltage distortions, the output impedance should be as small as possible [2, 11].

For the proposed voltage controller, the output impedance is equal to 'zero' which therefore predicts superior control performance compared to the conventional voltage controller. For instance, the tracking error for steady-state and transient moment is forced to be 'zero' in a symmetric and non-distorted grid. However, the proposed control method contains derivative part in the current reference generation which affects not only the feedforward term of the current controller but also the feedback controller. In fact, the analysis shown in Ref. [5] proves that the proposed method has good robustness against harmonic distortion.

6. Results and discussion

The variation of the developed control algorithm was conducted by simulating a microgrid with two inverter-interfaced DGs whose specifications are described in Ref. [5]. **Figure 12** shows the topology of the microgrid for the case study. In the application layer, the voltage reference generation algorithms for the three operating modes are running parallel to prevent the latter to start from scratch after every transition. Before connection/disconnection microgrid to the main grid, the angle difference between grid-forming and grid-supporting/grid feeding (θ_{inv}-θ_g) is compared to guarantee small phase/frequency deviations.

The European Standard EN 50160 defines standard operating conditions of frequency and voltage for islanded and interconnected power systems [12] . Assuming that the nominal root-mean-square (RMS) voltage is 230 V, the RMS value of voltage for interconnected systems should maintain between 207 and 253 V (±10%), whereas for islanded systems, it should be between 195.5 and 253 V (±15%). In terms of frequency, for interconnected systems, it should remain in the range of 49.5 and 50.5 Hz (±1%), and in the range of 49 and 51 Hz for islanded systems (±2%). These standard operating limits are used to evaluate the work in this chapter.

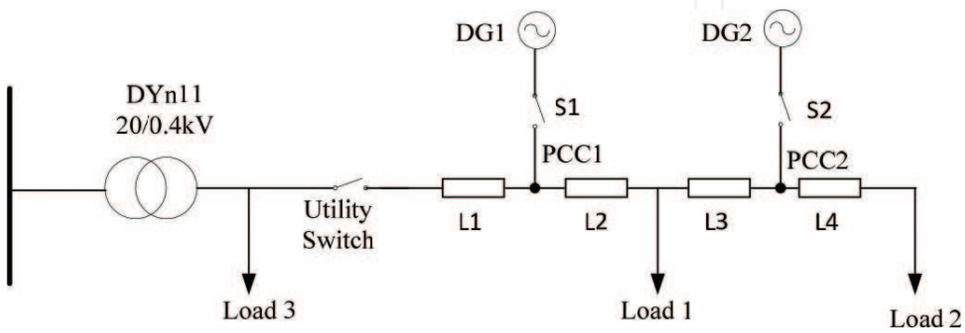

Figure 12. Microgrid configuration used as a case study [5].

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6.1. Simulation results

6.1.1. Grid-supporting to grid-forming mode

When a fault is detected in the main grid during the grid-supporting operation, it requests the microgrid to disconnect from the main grid. In this scenario, the transient behaviour of the DGs controlled with the developed algorithm is investigated. The maximum amounts of active power injections of the DGs running in grid-supporting mode are 20 kW for DG#1 and 15 kW for DG#2. The two DGs are connected to the main grid at 0.6 s to prevent the transients from the black start and phase-lock-loop (PLL) is used to synchronize each DG with the grid before connection. From 0 to 0.6 s, the controllers of DGs are pending to run in grid-supporting mode while the references P_{max} are set to be 'zero'. The DGs work in grid-supporting mode from 0.6 to 3.8 s, then they switch to grid-forming mode after the microgrid disconnects from the main grid. The transient behaviours of the DGs are presented in **Figure 13**.

Figure 13(a) indicates that the two DGs can inject maximum amount of active power (20 and 15 kW, respectively) in the grid-supporting mode, and achieve accurate power sharing (15 kW) in the grid-forming mode. The output voltages of both DGs during operating mode transition, as illustrated in **Figure 13(b)**, indicate that the two DGs exhibit neither overshooting nor harmful transient in voltage, and that both rapidly arrive at the steady state. **Figure 13(c)**

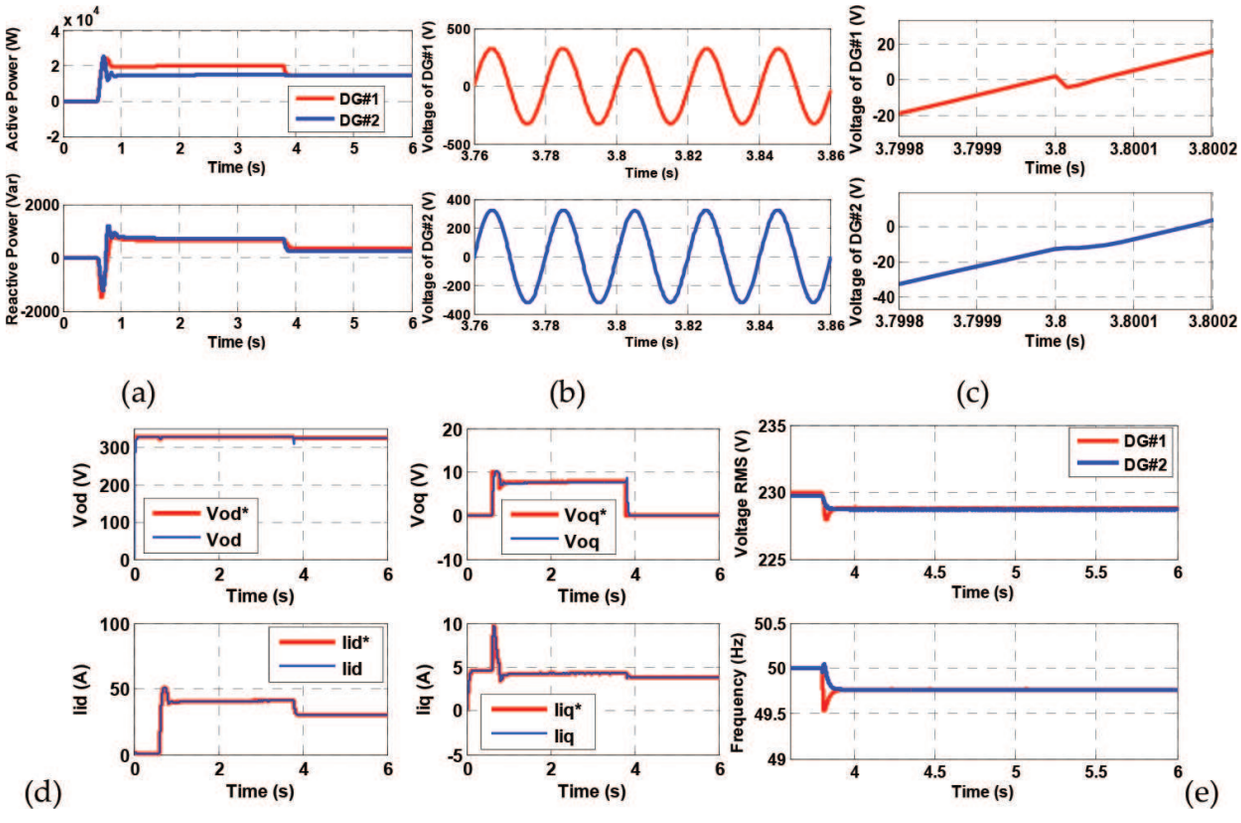

Figure 13. Transient performance from grid-supporting mode to grid-forming mode. (a) Active and reactive power of DGs. (b) Output voltage of DGs during mode change. (c) Zoomed-in plot of output voltage of DGs at transient moment. (d) DG#1: reference signal (red), actual output (blue) of voltage controller and current controller in d -q frame. | RMS voltage and frequency of DGs.

shows the zoomed-in plot of output voltage of DGs at the transition moment (3.8 s); negligible transients are observed for both DGs at the transition moment. Thus, very smooth transition performances are achieved as expected. The frequency of DGs shown in **Figure 13 (e)** also indicates the smooth transition process. The tracking performance of the inner and outer loop of DG#1 is presented in **Figure 13(d)**. The upper graph of **Figure 13(e)** illustrates that the voltages of both DGs lie inside the satisfactory limits in both grid-supporting and grid-forming mode. Moreover, the transient voltages remain within the required operating limits of the islanded microgrid. The lower graph of **Figure 13(e)** illustrates the frequency at the moment of transition. In less than 0.2 s, the two DGs accomplish accurate power sharing and arrive at the identical frequency of 49.76 Hz, which lies within the required operating limits. Furthermore, the largest frequency variation of the two DGs at the moment of transition is 49.52 Hz, which does not violate the operating range of EN 50160. The results show that the controlled variables can perfectly track their respective reference with zero steady-state error during steady state and transient. This is consistent with the specification set in Section 4 that the transfer functions of the inner and outer loops are both equivalent to the unitary gain.

6.1.2. Grid-supporting to grid-forming mode

In this test scenario, the two DGs are switched intentionally from grid-forming mode to grid-feeding mode at 2 s, when the phase differences of voltages between the main grid and the DGs are lower than 0.5 rad. In grid-feeding mode, the received active and reactive power references from the system control layer are 15 kW and 200 Var for DG#1, and 15 kW and 300 Var for DG#2. **Figure 14** shows the simulation results. **Figure 14(a)** illustrates the process of the inverters synchronizing with the grid. As it can be seen, the voltages of DG#1 and DG#2 can be synchronized with the grid voltage very rapidly and with small negligible transient after the switch is reconnected, thanks to fast dynamics and good disturbance rejection performance of the proposed method. **Figure 14(c)** presents the performance of the developed outer voltage and inner current controller. We can observe that each of the actual output variables follows the corresponding reference target perfectly; this confirms the validity of the design laid out in Section 4. The output current of DG#1 presented in **Figure 14(e)** shows the smooth transient performance of the microgrid.

The same test is investigated with the conventional method shown in Ref. [5] for comparing the controller performances (performance in steady state and transient state) with the developed control method. **Figure 14** shows the simulation results. **Figure 14(b)** illustrates that though DG#1 is able to synchronize with the main grid very rapidly, larger transient is exhibited; **Figure 14(d)** demonstrates that there are some tracking errors with respect to the reference and real output, and large transient currents shown at the transition moment, and **Figure 14(f)** further shows the undesirable transient current as well. Compared with the results in **Figure 14(b)**, **(d)** and **(f)**, the proposed method has smaller transient current during transition and better tracking and disturbance rejection performances.

The DG's output voltages in RMS values are shown at the top and the frequency is shown at the bottom of **Figure 15**. As seen from **Figure 15**, the RMS values of voltage and the frequencies

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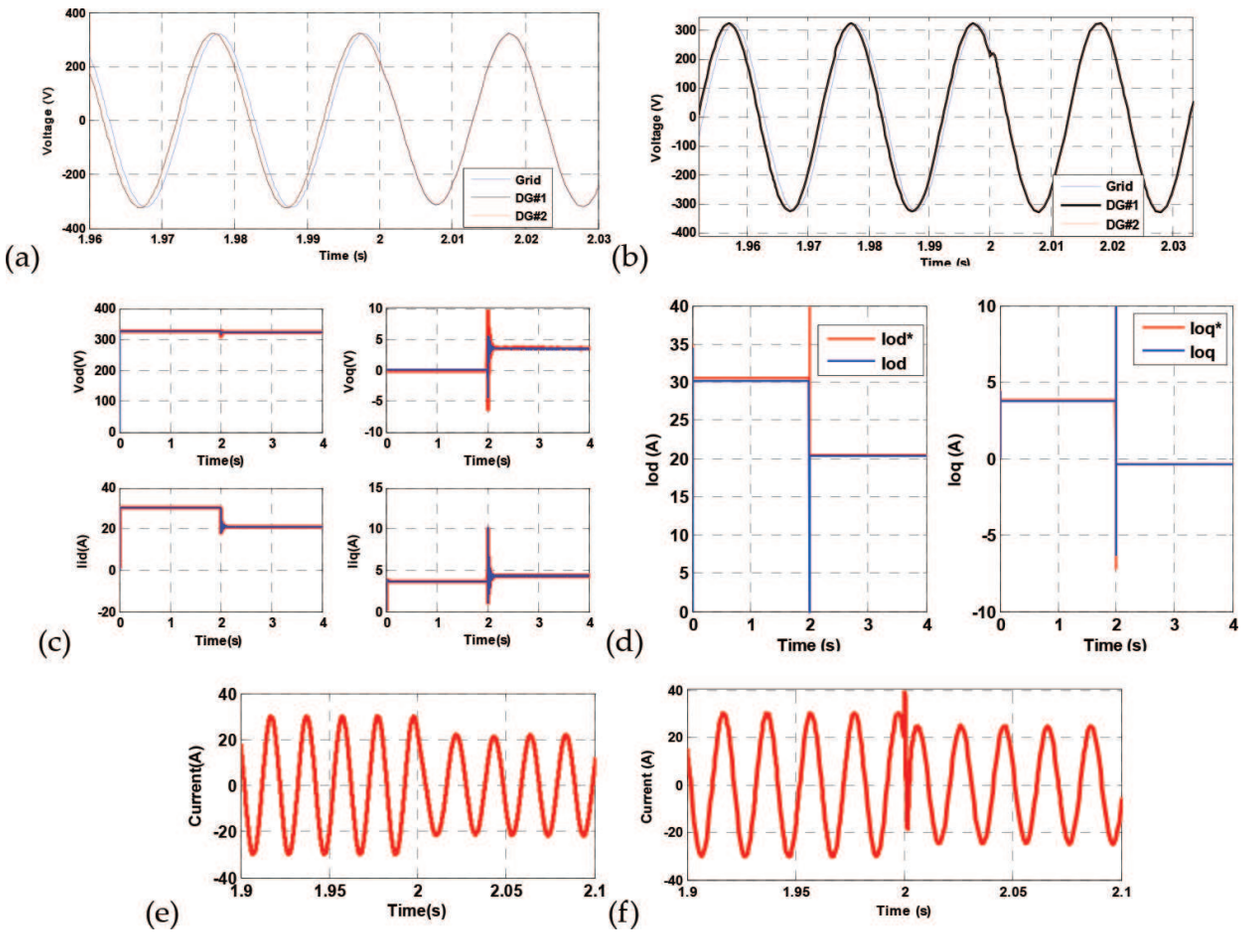

Figure 14. Transient performance from grid-forming mode to grid-feeding mode: proposed method (left column) and conventional method (right column). (a, b) Up: Grid voltage (blue) and inverter voltage (red) Down: Error between grid and inverter voltage. (c, d) DG#1: Reference signal (red), actual output (blue) of voltage controller and current controller in d-q frame. (e, f) Output current of DG#1.

of the DGs are near their nominal values pre- and post transition. As per the standard EN 50160, the DGs′ voltage and frequency both lie within the satisfactory operating ranges.

6.2. Experimental results

All simulations are performed in a hardware-in-the-loop (HIL) platform, and practical implementations such as delays caused by digital sampling, computation time and inverter switching are included. The structure including system layer, application layer, inverter control layer and switching layer is presented in **Figure 16**.

The microgrid with two inverter-interfaced DGs and the main grid model is built in a real-time digital simulator (RTDS). The application and inverter layer control algorithms have been programmed using Texas Instrument TMS28335 DSP. Each inverter is controlled using one DSP. There is a conditioning interface between RTDS and DSP to scale the output voltage level of RTDS (±5 V) to the output voltage level of DSP (0–3.3 V), and vice versa. The system layer controller is implemented in a Xilinx ML507 board; the board directly communicates with a RTDS gigahertz processor card through fibre optics to obtain measurements and transmit the

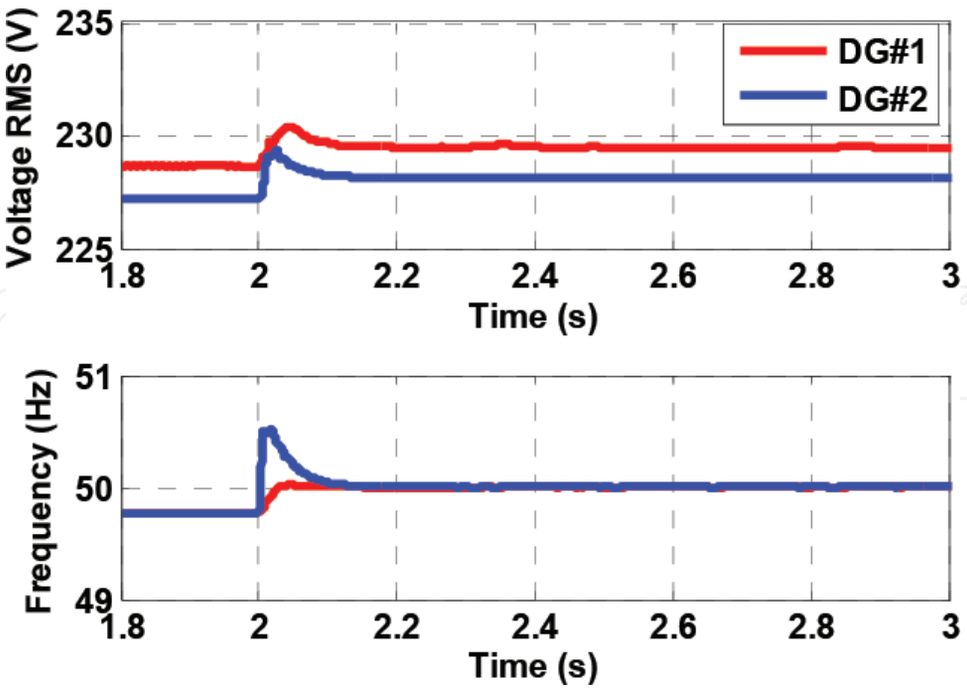

Figure 15. DGs' output voltage RMS values and frequencies.

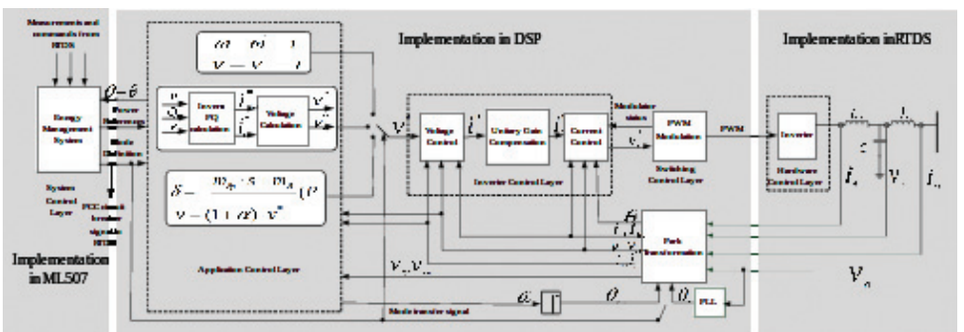

Figure 16. The structure of the universal control algorithm for flexible microgrid operation.

PCC circuit breaker control signal to RTDS. A control algorithm in the system layer, consisting of operating mode management and control reference generation, is implemented in ML507, and the operation mode signal and power references are sent to DSPs via serial peripheral interface. The algorithms implemented in the application layer are grid-forming (top), grid-feeding (middle) and grid-supporting (bottom), respectively, and the output is the voltage reference for the inverter layer. The schematic diagram and setup of HIL platform are presented in **Figure 17**. In this signal HIL platform, both the ML507 board and DSP board are controlled under test. The oscilloscope panels related show 5 V for 400-V voltage and 5 V for 50-A current.

6.2.1. Transition from grid-supporting to grid-forming mode

The two DGs begin in grid-supporting mode (the command signal sent from ML507 to RTDS is '1' and from ML507 to DSPs is '10'). The algorithm of grid-supporting mode in application

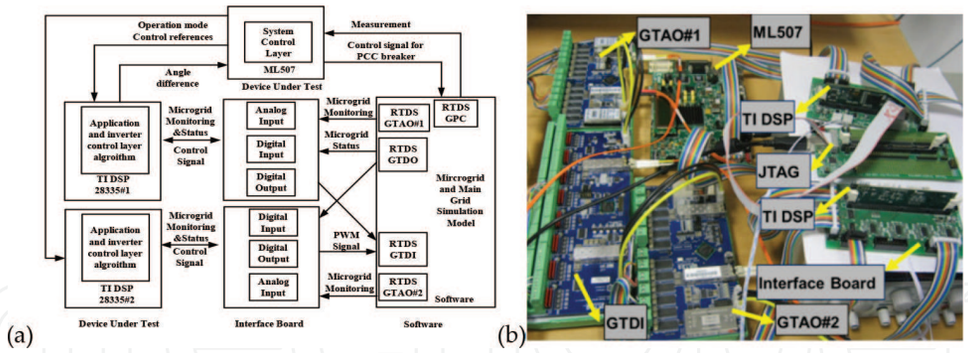

Figure 17. (a) Schematic diagram of the signal level HIL platform. (b) Set-up of HIL platform.

layer is selected and the voltage reference is passed to the inverter control layer. After letting the system run for a pre-defined time, the microgrid is intentionally switched to islanding mode by transmitting '00' to DSPs and '0' to RTDS from ML507. Then, the grid-forming mode in the application layer algorithm is selected to produce the voltage reference for the inverter control layer, and a new angle θ_{inv} for Park transformation is also transmitted to the inverter control layer. **Figure 18** presents details of the DGs' performance, showing the responses of the voltage and current during the transition between the two operating modes [5].

No transient change is shown in the voltage waveform and only very slight transients are exhibited in the current waveform. The calculated frequencies of both DGs are approximately 50 Hz in grid-supporting mode and 49.7 Hz in grid-forming mode, with the largest deviation during transition being 0.35 Hz. The calculated RMS values of voltage remain within the acceptable range around the rated value of 230 V during the transition process, with negligible deviations. Therefore, the expected smooth transition from grid-supporting mode to grid-forming mode is achieved with the proposed control algorithm, and the operating range of DGs' frequencies and voltages is within the range as per EN 50160.

6.2.2. Transition between grid-forming and grid-feeding mode

Two scenarios are studied in this case: the transition from grid-forming to grid-feeding mode requested by the DNO, and the opposite situation, the transition from grid-feeding mode to grid-forming mode caused by intentional islanding of the microgrid. During the first transition, the system controller sends operating mode signal '0' to RTDS and '00' to DSP, after which the voltage reference from grid-forming mode and angle θ_{inv} is calculated and sent to the inverter

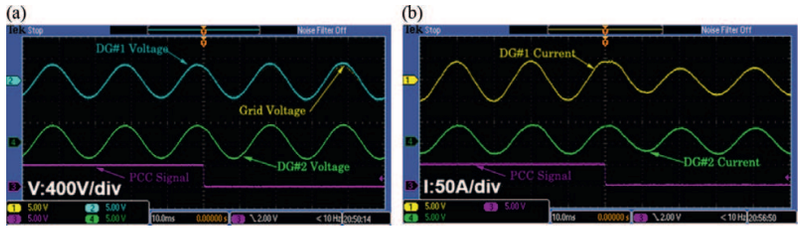

Figure 18. Transition from grid-supporting to grid-forming mode. (a) Voltage response during transition. (b) Current response during transition.

control layer. In addition, the difference in angle between the main grid voltage and DG#1 output voltage is compared. The microgrid will only be connected (reconnected) to the main grid when an 'enable' signal ('1') is transmitted from the system controller to the main grid (modelled and controlled in RTDS) and also the difference in angle is equal to or less than 0.5 rad. When these conditions are met, the system layer controller transmits '1' to RTDS, and '01' and power references to DSPs, which commands the inverters to operate in grid-feeding mode. Then, after a pre-defined time, the system layer controller transfers intentionally the microgrid to islanding mode, and the corresponding command signals are transmitted to DSPs and RTDS.

The control performance of the developed control algorithm is compared to the popularly used control algorithm presented in Ref. [6]. To attain valid simulation results, the operating conditions for the two algorithms are made identical. The microgrid is connected to the main grid when the phase difference between the grid voltage and the voltage at the terminal of DG#1 is equal to or less than 0.5 rad. Then, the two DGs transfer from grid-forming to grid-feeding mode [5]. After certain time (235 s), the microgrid is disconnected from the main grid, switching the two DGs back to grid-forming mode. The waveforms of voltage and current for both scenarios are different during transition moment because the DSP boards don't start to run at the same time after RTDS is running. However, the switching conditions (e.g. phase difference between main grid voltage and DG#1 output voltage) are maintained the same for both scenarios.

Figure 19(a) and **(b)** denotes that both control methods cause negligible distortion of the grid voltage at the moment of transition. This is expected, since the main grid is strong. **Figure 19(c)** and **(d)** shows a less distorted current waveform after transition when the proposed control algorithm is applied.

Figure 20 illustrates that at the moment of disconnection, both control algorithms swiftly generate a clean voltage waveform, with a marginally better performance than the conventional

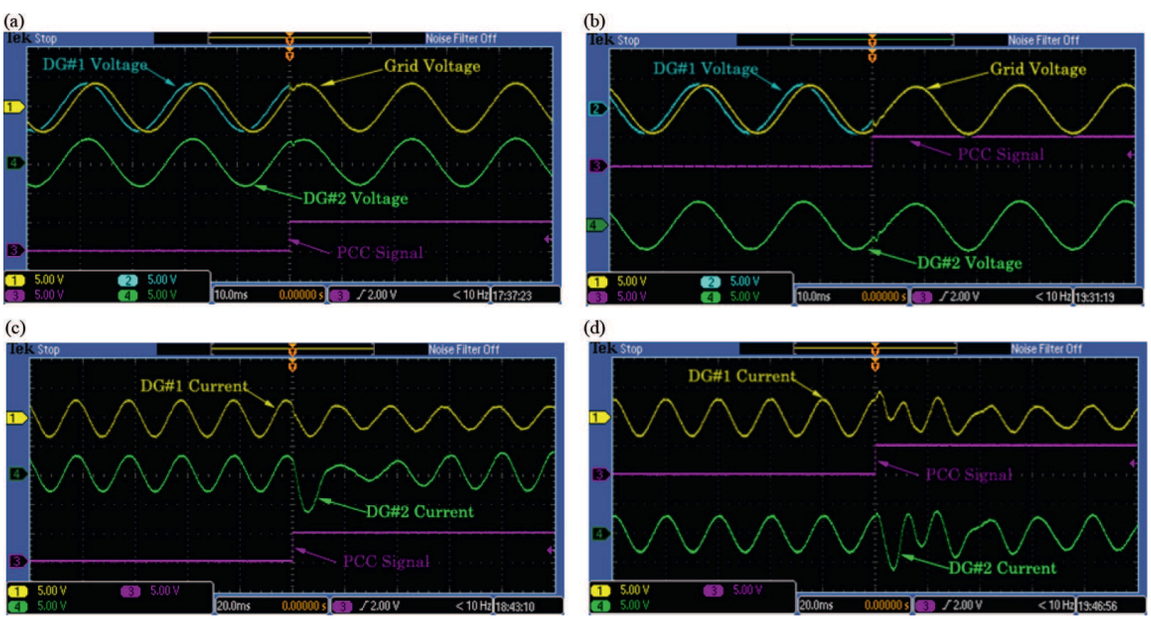

Figure 19. Transition from grid-forming to grid-feeding mode. (a) Voltage response with the proposed method. (b) Voltage response with the conventional method. (c) Current response with the proposed method. (d) Current response with conventional method.

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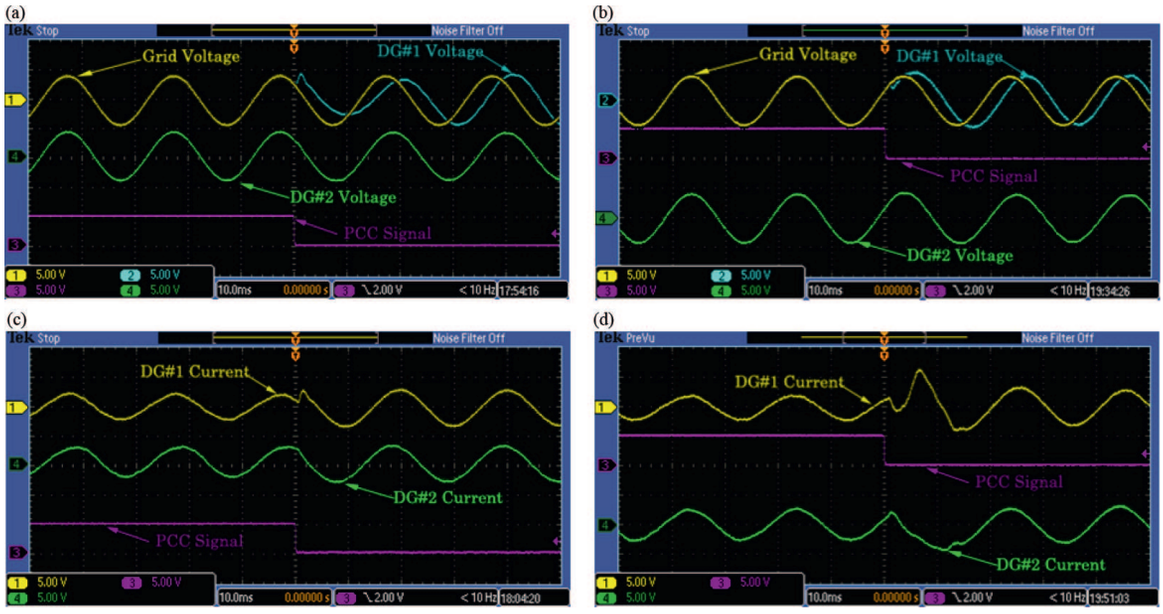

Figure 20. Transition from grid-feeding to grid-forming mode. (a) Voltage response with the proposed method. (b) Voltage response with the conventional method. (c) Current response with the proposed method. (d) Current response with conventional method.

method. In addition, the output currents of the developed control algorithm exhibit considerably superior qualities with fewer overshoots and quicker dynamic responses.

The calculated RMS values of voltage and frequencies of the two DGs with the developed control method during the transition process between grid-forming and grid-feeding modes are summarized as follows: in transition from grid-forming to grid-feeding mode, the calculated frequencies of the two DGs are approximately 49.7 Hz in grid-forming mode and 50 Hz in grid-supporting mode, with the largest deviation during transition being 0.45 Hz, from DG#2 [5]. The calculated RMS values of voltage remain within the acceptable range around the rated value of 230 V during the transition process, with the largest deviation being less than 5 V, from DG#2; in the transition from grid-feeding to grid-forming mode, the calculated RMS values of voltage and frequencies of the two DGs are within the acceptable operating range. Note that the largest deviations of frequency and voltage are 0.6 Hz and 7.5 V, respectively, from DG#1. The results indicate that the standard EN 50160 is respected and smooth transition behaviours of DGs are achieved. A small test is performed to compare the computation time of the proposed method and conventional method. The results show that the total sampling and calculation time is 48 μs for the proposed controller and 37 μs for the conventional controller. This indicates that the control complexity of the proposed controller is comparable with that of the conventional controller. The sampling interval is 300 μs which is long enough for both controllers to accomplish the sampling and computation.

7. Summary

The developed generalized control algorithm in the inverter control layer of DGs facilitates the seamless transition of microgrids. This is obtained by designing the multi-loop controller in the

inverter control layer in such a way that the closed loop dynamics of the inverter together with the *LC* filter present unitary gain. Thus, the current/voltage disturbances associated with the mode transition are fully cancelled. The proposed voltage control algorithm and the conventional double-loop voltage controller are compared with analytical study and experimental implementation. The output (harmonic) impedance is the cause of the tracking error and distortion caused by the output current. With the proposed voltage controller, the output impedance is '***zero***' which theoretically eliminates the tracking error and reduces/eliminates the distortion (can only reduce the distortion in the practical implementation due to the measurement noise, digital quantization errors, etc.). The work has shown that the developed voltage control algorithm has superior control performance than the conventional controller, and it is a high-performance controller, easy to be implemented in the practical application.

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