Chapter 4

Analog-to-Digital Conversion for Cognitive Radio: Subsampling, Interleaving, and Compressive Sensing

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Additional information is available at the end of the chapter

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Abstract

This chapter explores different analog-to-digital conversion techniques that are suitable to be implemented in cognitive radio receivers. This chapter details the fundamentals, advantages, and drawbacks of three promising techniques: subsampling, interleaving, and compressive sensing. Due to their major maturity, subsampling- and interleaving-based systems are described in further detail, whereas compressive sensing-based systems are described as a complement of the previous techniques for underutilized spectrum applications. The feasibility of these techniques as part of software-defined radio, multistandard, and spectrum sensing receivers is demonstrated by proposing different architectures with reduced complexity at circuit level, depending on the application requirements. Additionally, the chapter proposes different solutions to integrate the advantages of these techniques in a unique analog-to-digital conversion process.

Keywords: analog-to-digital conversion, cognitive radio, compressive sensing, interleaving, multistandard receivers, software-defined radio, spectrum sensing, subsampling

1. Introduction

Analog-to-digital conversion (ADC) stage is one of the main bottlenecks of the high-speed telecommunications systems. This chapter presents a survey of different feasible analog-to-digital conversion techniques that are suitable to overcome these difficulties and to get the software-defined radio (SDR) paradigm [1], where most functionalities, instead of being performed in the analog domain (i.e., filters and mixers), are performed in the digital domain. In SDR, the analog-to-digital conversion is implemented immediately after the antenna, and the radio frequency (RF) signal is directly converted to digital without any previous mixing

stage. Since it is not possible to approach this idea with traditional analog-to-digital conversion from current commercial devices, this chapter describes some techniques that may be employed instead. Although the proposed systems have more restrictive specifications, these solutions reduce the final complexity, as will be detailed in this chapter. This work explores three different promising techniques: subsampling, interleaving, and compressive sensing (CS).

The proposed techniques are an appealing solution to approach the cognitive radio (CR) objectives [2, 3], which are conditioned by the physical implementation of the SDR receiver. Due to the necessity of several wireless standards coexisting in the same device, a high flexibility and programmability will be an important requirement for the proposed architectures, with the objective of being employed in multistandard receivers.

With these objectives in mind, this chapter describes in detail three different approaches for implementing the analog-to-digital conversion stage. The choice of one or other of these approaches will depend on the environment, the properties of the received signals, and the parameters that have to be optimized. For receivers where the main requirements are a high-resolution and a high-analog bandwidth that covers a maximum number of communication standards, we propose a system based on subsampling techniques. For applications where the main requirement is to maximize the data acquisition rate, the proposed system is based on interleaving techniques, that is, the interconnection of several analog-to-digital converters in parallel. Finally, compressive sensing techniques will be preferred for scenarios where the spectrum can be considered sparse, that is, for a wideband spectrum with a low spectral occupancy, where it will be possible to recover the received signal and implement an estimation of the radio channel by using a reduced number of samples from the ADC. This emerging technology will be presented at architectural level, so that it will be studied from the point of view of its integration with the two main techniques detailed in this chapter, that is, subsampling and interleaving techniques, with the objective of exploiting their advantages for sparse spectrum sensing applications.

2. Subsampling techniques

2.1. Overview of the subsampling concepts

2.1.1. Subsampling idea

Subsampling-based systems, whose conceptual diagram is illustrated in **Figure 1**, are a feasible alternative to the classic mixing-based receiver architectures. The received signal is filtered by an RF band-pass filter that can be a tunable filter or a bank of filters. The incoming band-pass signal is sampled below the Nyquist rate [4, 5], being possible to avoid aliasing using some sampling properties. This sampled signal is converted to digital using an ADC at intermediate sampling rate. The main advantage of this scheme is its simplicity, because the number of components is reduced, being possible to place the data conversion very close to the antenna. As a consequence, many operations like filtering, frequency translation, and demodulation can

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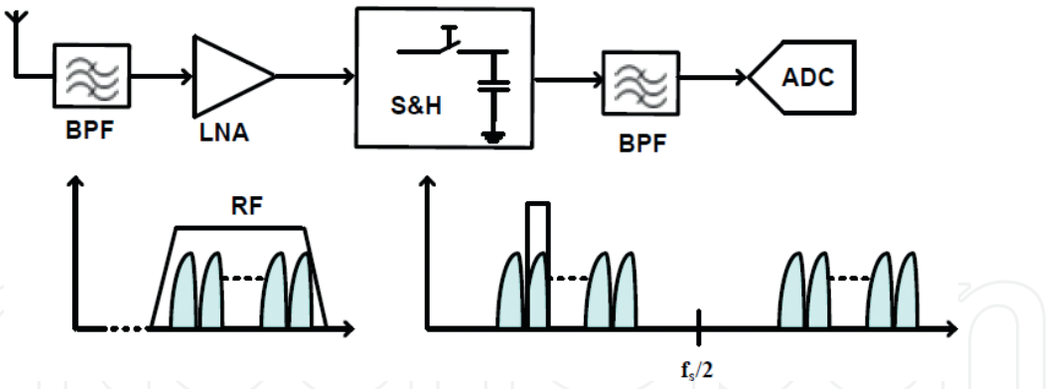

Figure 1. Conceptual diagram of the subsampling receiver architecture.

be implemented in digital domain, taking advantage of low-cost digital very large-scale integration (VLSI) solutions, and leading to a high integration while eliminating problems such as DC offset and 1/f noise.

In addition to system cost reduction, pushing these functions in digital domain eliminates many of the sensitivities of analog solutions, such as device matching, environmental sensitivity, and performance variation over time. The flexibility and reconfigurability required by SDR applications are also increased by moving the ADC into IF stage and, moreover, it is possible to use this architecture for wideband and multistandard applications because of its large analog bandwidth. In this architecture, a single ADC can sample multiple signal channels, which are then separated and demodulated in parallel in digital domain.

In **Figure 1**, the Sample & Hold (S&H) after the low noise amplifier (LNA) downconverts the RF signal to intermediate frequency. This enables us to relax the constraints on the S&H inside the ADC: if the bandwidth of the ADC is required to include the RF carrier frequency, it may not be possible to simultaneously fulfill the conditions on the required dynamic range and resolution of the ADC using the current technologies. To mention other problems, subsampling receivers have several noise sources, such as the jitter and thermal noise folded in the band of interest, which will be detailed in the subsequent sections.

Finally, RF band-pass filtering is required when avoiding overlap between folded signals is necessary. These BP filters, especially on-chip filters, are difficult to implement at high frequencies. Although external filters, such as SAW filters, can be used, they are only available at limited number of frequencies, so this is not a practical solution to design multistandard receivers. Alternatively, increasing the sampling frequency can decrease the selectivity of the filter. However, this solution has some drawbacks, such as the high technology and high cost required by the ADC, whose resolution and dynamic range will be degraded as compared to lower sample rate ADC alternatives. Also, power consumption increases with sample rate. Therefore, the cost, performance and power consumption of other devices (such as ADC clock sources or digital circuits after the ADC) also depend on the ADC sample rate. In this section, we address the problem of planning the sampling frequencies with the objective of avoiding

this overlapping between signals and reduce the complexity of the RF filtering. Note that we do not consider additional adjacent interferers not overlapped with the desired signal since they can be suppressed by additional channel filtering in digital domain.

2.1.2. Selecting the optimal sampling frequency

For an input signal with carrier frequency f_c and analog bandwidth BW, the minimal sampling frequency f_s is established by the Nyquist theorem, $f_s > 2B$, being $B = f_c + BW/2$. However, if we are processing band-pass signals, aliasing can be avoided with a lower f_s when Eq. (1) is satisfied [5]:

$$\frac{2f_c - BW}{m-1} > f_s > \frac{2f_c + BW}{m} \tag{1}$$

where m is an integer number representing the number of replicas of the original signal that appears in the range $[0, f_c - BW/2]$. Note also that f_s has to be higher than two times BW. The maximum number of copies needed to avoid aliasing is calculated by Eq. (2) [5]:

$$m_{\max} = floor((f_c + BW/2)/BW) \tag{2}$$

A suitable value in the range given by Eq. (1) is the one that produces a copy on $f_s/4$. This frequency is given by Eq. (3) [5]:

$$f_s = \frac{4f_c}{m_{\text{odd}}} \tag{3}$$

where m_{odd} is an integer odd number greater than 1. Moreover, if this value is 5, 9, 13,…, there is no spectral inversion. Sampling at $4f_c/m_{\text{odd}}$ results in a larger subsampling frequency bandwidth and relaxes the filtering requirements after the S&H.

2.1.3. Subsampling nonidealities

This section is centered in the main nonidealities of the S&H illustrated in **Figure 1**, which is the most critical device in the subsampling-based systems, as it processes high-frequency signals.

2.1.3.1. Jitter noise

Ideally, the time interval between samples is a constant value equal to $1/f_s$. Nevertheless, in practice there are fluctuations due to jitter. This jitter produces an increment of the output total noise, thus limiting the effective number of bits (ENOB). Jitter is produced by two different sources: the phase noise associated to the oscillator and the aperture jitter of the S&H. At a first approach, we can consider both sources of jitter as noncorrelated Gaussian stochastic processes. When the input is a sinusoidal signal like $y(t) = A\sin(2\pi f_{\text{in}} t)$, signal-to-noise ratio (SNR) at the S&H output is determined by [6, 7]

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$$\mathrm{SNR} = \frac{\frac{A^2}{2}}{\overline{N_\tau}} = \begin{cases} \dfrac{1}{4\pi^2 f_{\mathrm{in}}^2 \sigma_\tau^2} : 2\pi f_{\mathrm{in}} \sigma_\tau << 1 \\ \dfrac{1}{2(1 - e^{-2\pi^2 f_{\mathrm{in}}^2 \sigma_\tau^2})} : \text{otherwise} \end{cases} \tag{4}$$

where $\overline{N_\tau}$ is the average noise power and σ_τ is the jitter standard deviation. Note that the SNR is degraded when the input frequency increases.

2.1.3.2. Folded thermal noise

The S&H can be modeled as illustrated in **Figure 2a** [6], where the switch introduces a thermal noise with a power spectral density (PSD) equal to $S_{\mathrm{in}}(f) = 2kTR_{\mathrm{on}}$, where k is the Boltzmann constant, T is the temperature, and R_{on} is the on-resistance of the switch. This noise is AWGN (additive white Gaussian noise) and is folded in the band of interest by the subsampling process (**Figure 2b**).

R_{on} and C model a low-pass (LP) filter (**Figure 2a**) with transfer function $H(f) = 1/(1 + j2\pi f R_{\mathrm{on}} C)$, whose 3-dB cutoff frequency is equal to $f_{3\mathrm{dB}} = 1/(2\pi R_{\mathrm{on}} C)$. The output PSD will be [7]

$$S_{\mathrm{out}}(f) = S_{in}(f)|H(f)|^2 = 2kTR_{\mathrm{on}} \frac{1}{1 + 4\pi^2 f^2 R_{\mathrm{on}}^2 C^2} \tag{5}$$

Being the total noise power (by a two-sided representation):

$$P_{\mathrm{out}} = \int_{-\infty}^{\infty} S_{\mathrm{out}}(f) df = \frac{kT}{C} \tag{6}$$

For modeling purposes, the output noise can be considered to be a Gaussian thermal noise filtered by a brick-wall filter of bandwidth equal to B_{eff} (i.e., the noise bandwidth in **Figure 2c**) [7]:

$$B_{\mathrm{eff}} = \frac{1}{4R_{\mathrm{on}}C} = \frac{\pi}{2} f_{3\mathrm{dB}} \tag{7}$$

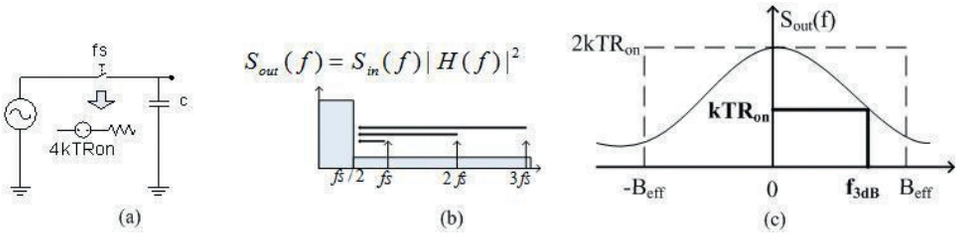

Figure 2. (a) S&H model, (b) noise folded in the band of interest, and (c) effective noise bandwidth.

Therefore, the noise power can be rewritten as follows [7]:

$$P_{\text{out}} = \frac{kT}{C} = 2kTR_{\text{on}} \cdot (2B_{\text{eff}}) \tag{8}$$

On the other hand, the SNR in $[-B_{\text{eff}}, B_{\text{eff}}]$ is defined as [6]

$$SNR = \frac{P_s}{N_i + (m-1)N_o} \tag{9}$$

where P_s is the signal power spectral density, m is the number of replicas, and N_i and N_o are the in-band and the out-of-band noise power spectral densities, respectively. Setting $2B_{\text{eff}} = mf_s$, when $m = 1$ the Nyquist theorem is met and the SNR is not affected by the folded noise. Otherwise, if $m > 1$, and assuming $N_i = N_o = N$:

$$SNR = \frac{P_s}{mN} = \frac{P_s}{N(2B_{\text{eff}}/f_s)} \tag{10}$$

Thereby, the out-of-band folded noise reduces the SNR by a factor $2B_{\text{eff}}/f_s$. From Eq. (10), we can observe that the SNR increases around 3 dB when the sampling frequency is doubled. Thus, regarding the noise, it is convenient to select the largest sampling frequency among the set of possible sampling frequencies defined by the digital signal processing block specifications.

2.2. Noise performance optimization: multiple clocking techniques

This section describes a method for improving the resolution that employs two consecutive subsampling stages, with the objective to reduce the folded noise effect. The use of two subsampling processes enables us to increase the sampling frequency of the first stage, resulting in a lower contribution of the first S&H to the folded thermal noise.

Figure 3 illustrates two different alternatives to implement a subsampling-based receiver. **Figure 3a** shows the scheme for a unique clock, whereas **Figure 3b** shows the scheme with two different clocks. The scheme illustrated in **Figure 3a** was employed in Ref. [8] by using the S&H Inphi 1821TH and the ADC E2V AT84AS001, with a maximum sampling frequency of 2 GHz and 500 MHz, respectively. Therefore, the unique sampling frequency for this architecture is limited to 500 MHz. However, the sampling frequency of the first S&H in **Figure 3b** can be selected up to 2 GHz, obtaining a band-limited signal at the output [9]. As the first sampling frequency is very large, the folded thermal noise added by this stage is reduced. After filtering, the resulting signal is sampled again by a second S&H at 400–500 MHz.

Figure 3 also illustrates the folded noise (dotted line) for the single clock (**Figure 3a**) and the multiple clock (**Figure 3b**) cases, considering for both cases the same thermal noise level at the input of the S&H (solid line) and from the ADC (dashed line). Since the effective noise bandwidth of the S&H is typically much larger than that of the ADC, the improvement achieved at the S&H in **Figure 3b** is usually dominant. In **Figure 3b**, a BP filter is necessary to select a proper band and decrease the out-of-band noise folded by the second subsampling process, while an LP filter with a cutoff frequency equal to $f_s/2$ may be enough in **Figure 3a**.

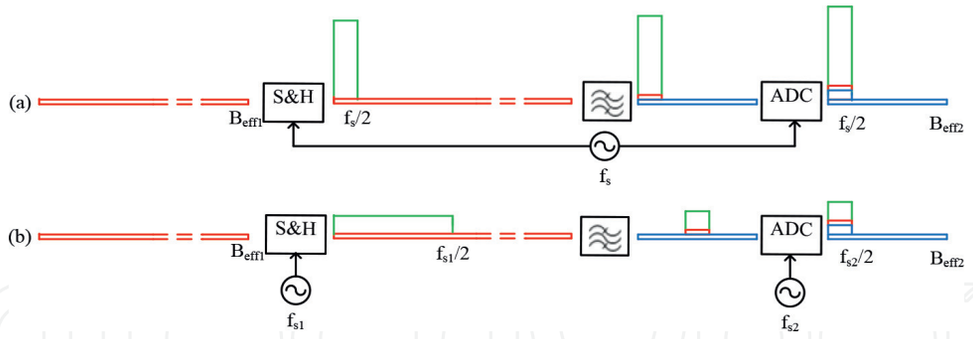

Figure 3. Folded noise effects using single clock (a) and multiple clock (b).

Assuming that the noises of both S&Hs in **Figure 3** are uncorrelated, from Eq. (10), the output power spectral density due to the S&Hs white noise in **Figure 3a** and b, respectively, is [9] as follows:

$$P_{N(a)} = \frac{2B_{\text{eff1}}}{f_s}N_1 + \frac{2B_{\text{eff2}}}{f_s}N_2 \,;\, P_{N(b)} = \frac{2B_{\text{eff1}}}{f_{s1}}N_1 + \frac{2B_{\text{eff2}}}{f_{s2}}N_2 \tag{11}$$

Where N_1 and N_2 are the noise power introduced by S&H$_1$ and S&H$_2$, respectively, and B_{eff1} and B_{eff2} their respective noise bandwidths. Note that there will not be folding of N_1 during the second sampling process because the signal is filtered at IF in both cases using a BP filter. Therefore, the SNR improvement obtained with this multiple clocking method is given by [9]

$$\frac{SNR_{(b)}}{SNR_{(a)}} = \frac{P_s/N_{(b)}}{P_s/N_{(a)}} = \frac{B_{\text{eff1}}N_1 + B_{\text{eff2}}N_2}{\frac{f_s}{f_{s1}}B_{\text{eff1}}N_1 + \frac{f_s}{f_{s2}}B_{\text{eff2}}N_2} \tag{12}$$

As the first S&H processes high-frequency signals, $B_{\text{eff1}} >> B_{\text{eff2}}$. In addition, we can consider the noise power spectral densities of both S&Hs with the same order of magnitude. Then, Eq. (12) can be approximated by [9]

$$\frac{SNR_{(b)}}{SNR_{(a)}} \approx \frac{1}{\frac{f_s}{f_{s1}} + \frac{f_s}{f_{s2}}\frac{B_{\text{eff2}}}{B_{\text{eff1}}}} \tag{13}$$

The most influential term in this improvement is f_{s1}/f_s, that is, a higher value of this ratio will mean a better SNR improvement. The experimental results obtained for an analog input signal bandwidth of 20 MHz are given in **Figure 4**, where it is possible to observe the improvement over the ENOB by using the proposed technique.

2.3. Subsampling-based systems for cognitive radio applications (I): approach for nonlinear and multi-band environments

2.3.1. Studied scenarios

The benefit of using a subsampling-based receiver for cognitive radio is, besides its simplicity and reconfigurability, that the capability of hopping between different spectrum spans only requires

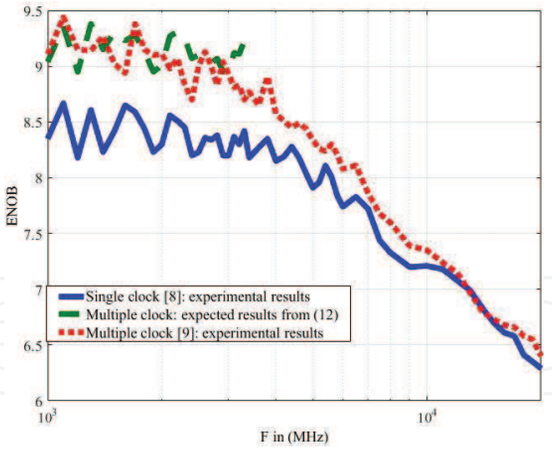

Figure 4. ENOB obtained using single clocking and multiple clocking techniques.

adjusting the sampling frequencies and selecting the appropriate band-pass filters. However, there is a challenge when using subsampling concurrently in a multi-signal environment and/or nonlinear conditions, because the replicas of the generated harmonics are folded back in the band of interest and may overlap with the desired signals. This issue was addressed in Ref. [10] where a universal formula for subsampling in nonlinear systems was developed for single-band applications. In dual-band receiver applications, the main problem of subsampling is the possible overlapping between the replicas of the two desired signals in the IF frequency band. This problem was studied in Ref. [11] for multi-band linear and noninterfering environments.

As one example of application, a dual-band subsampling receiver has been proposed for use in a feedback loop of a dual-band transmitter for linearization purposes using digital predistortion [12]. In Ref. [13], a subsampling receiver for dual-band applications was proposed, due its simplicity, to implement a cognitive radio sensing different bands and checking if they are in use. In Ref. [13], the designed subsampling receiver does not consider any interferers, harmonics, or intermodulation effects.

This section extends the above study [12, 13] by optimizing the SNR of concurrent dual-band signals at the receiver in a multi-signal or nonlinear environment. The requirement of increasing the analog bandwidth and reducing the effect of the folded noise leads to propose new receiver topologies with the objective of improving these features for a larger number of communication standards. Interferences and spurious signals in the received spectrum can be treated as intermodulation products using the same optimization technique that will be described later, so when these signals are subsampled the resulting aliasing components with these unwanted and spurious signals do not overlap with the desired signal.

As an additional benefit, these extra conditions used in the sampling frequency selection can lead to more relaxed RF filter requirements, since the known unwanted signals in the spectrum will not affect the desired signal bandwidth at IF and, therefore, they will be filtered more easily after being subsampled.

Figure 5 illustrates a basic scheme for a concurrent dual-band subsampling-based receiver. It consists of LNA, S&H, ADC, and band-pass filters (located in different parts of the receiver chain to filter out unwanted signals).

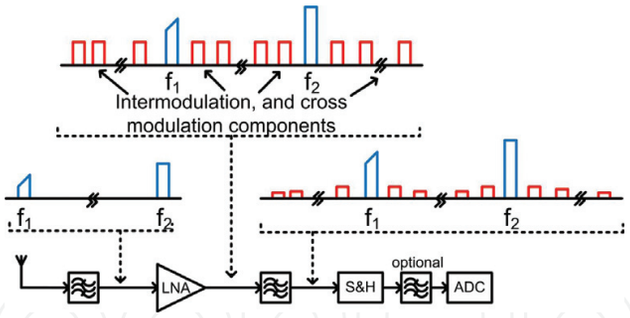

Figure 5. Subsampling receiver in multi-band nonlinear environment.

In concurrent dual-band applications, the LNA may introduce intermodulation and cross-modulation components at the receiver path right before the S&H block. Proper filtering at the receiver may attenuate the level of unwanted intermodulation components, without completely removing them all. In subsampling-based receivers, these intermodulation and cross-modulation leakage signals could be a significant source of noise for the in-band signals. In fact, it depends on the selected subsampling frequency, and proper and careful subsampling frequency selection could avoid the overlapping between the desired in-band signals and the unwanted intermodulation and cross-modulation signals leakage through the band-pass filter. **Figure 5** also illustrates the signal spectra at different points of the receiver. The purpose of the first band-pass filter is to remove the out-band undesired spectrum. Because of the nonlinear nature of the concurrent dual-band LNA, intermodulation and cross-modulation components are generated in the receiver path. The second band-pass filter attenuates these unwanted components as much as possible. The signals at the input of S&H are the two desired signals plus those unwanted spurious components with a signal level higher than the noise floor.

The signals produced by the LNA nonlinearity can be overlapped when subsampled by the S&H. The architectures proposed in this work to avoid this overlapping are based on single and multiple clock techniques, where the objective is to optimize the noise performance and the flexibility of the system for its use in multistandard applications. The work presented in this section encompasses an analysis of the multi-signal subsampling receiver from noise and nonlinear distortion perspectives, and proposes optimized architectures to mitigate these aspects and to improve the overall performance of the subsampling receiver in multi-signal environment in terms of signal quality and subsampling speed, along with an experimental validation.

2.3.2. Subsampling in nonlinear environments

When an input signal centered at f_1 (**Figure 6a**) [10] drives a nonlinear system, the output signal may produce multiple spectra, with different bandwidths, centered at integer multiples of f_1 (see **Figure 6a**). Let us consider any two intermodulation products at frequencies if_1 and jf_1, with respective bandwidths B_i and B_j and $j > i$. It can be easily shown (see Ref. [10]) that the range of the sampling frequencies that guarantees that those intermodulation products do not overlap in the sampled output spectrum is given by

$$\frac{kf_1 + W}{n+1} < f_s \leq \frac{kf_1 - W}{n} \tag{14}$$

where $k = j - i$, $W = (B_i + B_j)/2$ and $n = \text{floor}((jf1 - if1)/fs)$.

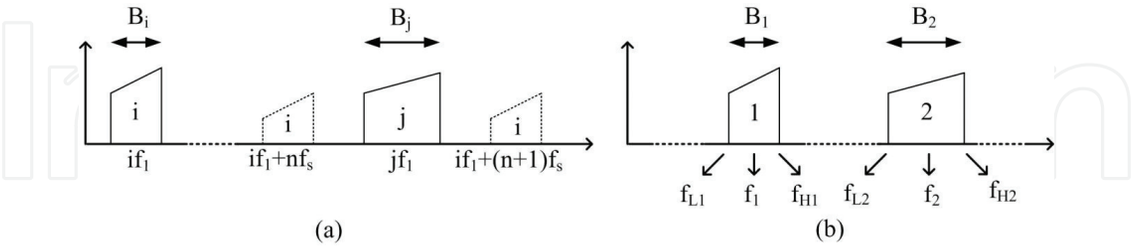

Figure 6. Frequency locations for nonlinear (a) and dual-band (b) scenarios.

2.3.3. Subsampling for multi-band systems

An algorithm to find the range of valid subsampling frequencies for multi-band systems is presented in Ref. [11]. For the particular case of a dual-band input spectrum (**Figure 6b**), the subsampling frequency f_s must be chosen to ensure that the two signals do not overlap in the subsampled domain. From the general equations presented in Ref. [11] and considering a dual-band case, it follows that f_s satisfies the following equation:

$$n_1 = \left\lfloor \frac{f_{L1}}{f_s} \right\rfloor \leq \left\lfloor \frac{f_{L1}}{2((f_{U1} - f_{L1}) + (f_{U2} - f_{L2}))} \right\rfloor \tag{15}$$

where $f_{L1}$and f_{U1} are the lower and upper limits of the lower band and f_{L2} and f_{U2} are lower and upper limits of the upper band, being n_1 the maximum replica order of the lower band. Denoting $R_1 = f_2/f_1$, we have that f_s must also verify [11]:

$$\lfloor R_1 n_1 \rfloor \leq n_2 \leq \lfloor R_1 n_1 + R_1 \rfloor \tag{16}$$

where $n_2 = \text{floor}(f_2/f_s)$.

2.3.4. Subsampling for multi-band systems in nonlinear environments

This section describes the algorithm employed to integrate both scenarios previously described, that is, multi-band and nonlinear systems which utilize subsampling techniques. The final sampling ranges will be given by the following expression:

$$F = F_{\text{db}} \cap F_{\text{imd}} \cap F_{\text{cmd}} \cap F_{\text{hmd}} \tag{17}$$

where F is the intersection of all the valid ranges calculated from Eqs. (14)–(16), being F_{db}, F_{imd}, $F_{\text{cmd,}}$ and F_{hmd} are the valid sampling frequency sets for the fundamental signals, intermodulation, cross-modulation, and harmonic distortion, respectively.

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In order to find *F,* an algorithm has been developed in MATLAB [14]. This algorithm calculates these ranges and the location of the replicas, where the input parameters are the signal frequencies, the signal bandwidths, and the number of harmonics (i.e., order of the nonlinearity). Therefore, knowing the signal frequencies and the number of harmonics, it is possible to calculate the location of the intermodulation and the cross-modulation products. An example of the results obtained from this algorithm is illustrated in **Table 1** [14], showing the three first valid ranges immediately lower than 2 GHz for the input signals at 1.82 and 2.4 GHz, considering five harmonics and a signal bandwidth of 25 MHz. The subsampled spectrum is illustrated in **Figure 7** [14] for a sampling frequency equal to 2 GHz, showing that there is no overlapping between signals.

2.3.5. Optimization of dual-band receivers in nonlinear environments

An analysis focused on optimizing the noise performance is presented in this section. Independent clocks for the S&H and ADC are proposed to limit the noise effects, and a bank of band-pass filters is used to filter out most of the aliased nonlinear and interfering components. Several different subsampling architectures and filter configurations are analyzed in theoretical and measurement environments.

Lower frequency bound (MHz)	Upper frequency bound (MHz)
1995	2000
1837.5	1978.33
1801.67	1802.5

Table 1. Valid sampling frequencies below 2 GHz.

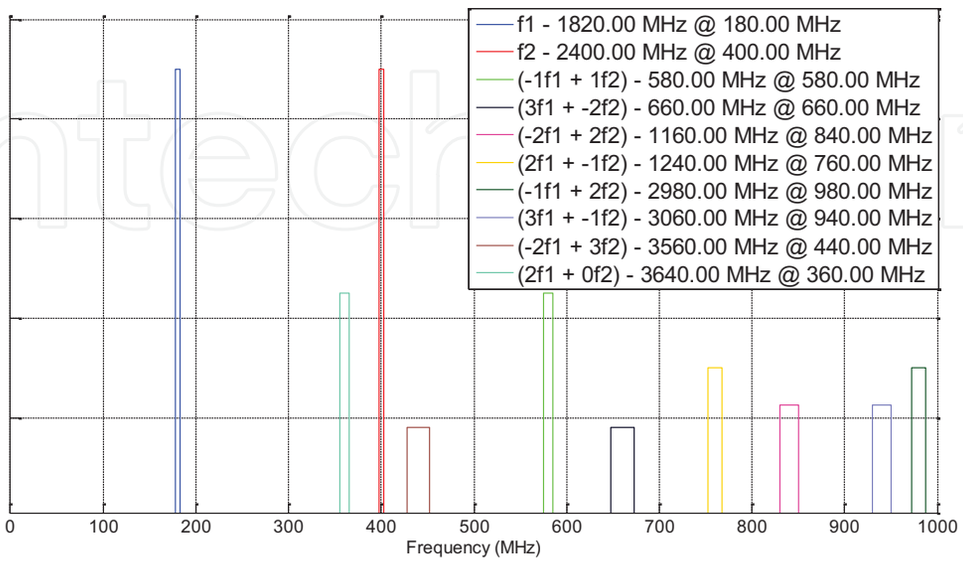

Figure 7. Subsampled spectrum for 1.82 and 2.4 GHz input frequencies.

2.3.5.1. Subsampling for concurrent dual-band and nonlinear systems using multiple clocking techniques

This section is focused on an optimized concurrent dual-band subsampling receiver for noise performance and versatility, in order to cover most wireless communication standards. The optimization takes advantage of the flexibility of subsampling, as it is possible to study different valid alternatives to clock the receiver in order to maximize its noise performance.

As described in Section 2.2, clocking the S&H and the ADC with the same clock limits the maximum sampling frequency of the system to that of the ADC, which is usually significantly lower than the maximum sampling frequency of the S&H. As a better alternative, employing an additional higher frequency to clock the S&H it is possible to increase the SNR of the receiver. Moreover, for this dual-band application, additional degrees of freedom can be obtained using a multiple clock scheme, so that we can cover a higher number of dual-band combinations of wireless communication standards. However, the BP filter used in **Figure 3b** might reduce the flexibility of the receiver when it is used in multi-band applications and in a nonlinear environment. This section tries to find the optimal filter bandwidth that reduces the folded noise, while avoiding a significant reduction in the number of valid sampling frequencies.

Figure 8 shows the effects of a third-order nonlinearity when a dual-band signal passes through a nonlinear subsampling receiver. In the first scenario (**Figure 8a**), the S&H and the ADC are clocked at the same rate. In the second scenario (**Figure 8b**), the clock rates of S&H and ADC are different. Both carrier frequencies at 880 MHz and 1.82 GHz are sampled at 400 MHz, where this frequency has been calculated by the algorithm described in Section 2.3.4. Using this sampling frequency, **Figure 8a** shows the different Nyquist bands along which the input signals and their harmonics and intermodulation products are distributed at the S&H input. All of them are folded to IF. After subsampling, the signal is filtered and converted to digital domain, where the Nyquist theorem is met. Similarly, **Figure 8b** presents the scenario where the S&H and ADC use different clock rates. In order to reduce the folded noise effect, the S&H sampling frequency is increased to 2 GHz, while the input RF signal at the S&H is the same as in the case of **Figure 8a**. The second sampling frequency is still 400 MHz. Both frequencies also satisfy the criteria detailed in the previous sections, so that aliasing between the target signals and their harmonics and intermodulation products is avoided. Finally, it is observed in **Figure 8b** that it is possible to relax the specifications of the filters, as desired, because of a higher first-sampling frequency

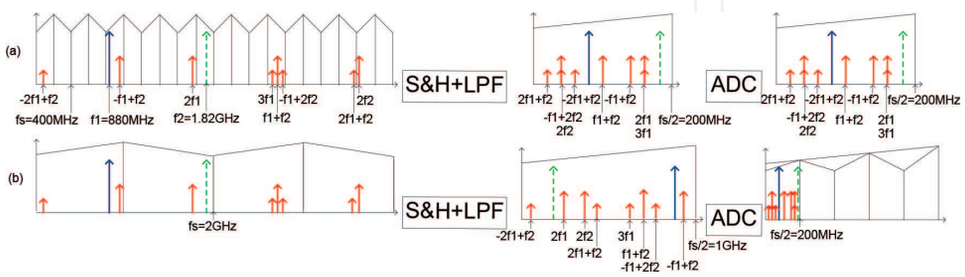

Figure 8. Folded effects for harmonics and intermodulation products using a single clock (a) and multiple clock (b) techniques.

places the IF components more separately in the spectrum, while maintaining at the same time the objective of removing the maximum number of the undesired components.

2.3.5.2. Experimental results

An experimental validation using realistic wireless communication scenarios is presented below to demonstrate the robustness and appropriateness of proposed technique in multi-standard environments. The seven input frequencies chosen to study the selective combinations for different dual-band applications correspond to the standards studied in Ref. [14]; the grouping for two given bands is shown in **Table 2**.

The experimental setup is illustrated in **Figure 9** [15]. The dual-band signals are continuous wave signals to demonstrate the peak SNR that can be achieved, and each signal band is generated by independent Agilent PSG E8257D signal generators. A power combiner combines both signal sources into a dual-band signal is amplified using a LNA ZX60-6013 from Minicircuits, and subsampled by an S&H Inphi 1821TH, and a ADS5474 ADC from Texas Instruments. The signal generators used as clock sources for the S&H and the ADC are the Agilent E8663D and the Rohde & Schwarz SMIQ. The implemented receiver architecture's design is shown in **Table 3**.

	Dual-band signal scenarios											
Standard	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
WCDMA (V) 880 MHz	x	x	x	x	x	x						
GSM-DCS 1.82 GHz	x						x	x	x	x	x	
WCDMA (I) 2.12 GHz		x					x					x
Bluetooth 4 GHz			x					x				x
WiMAX 3.5 GHz				x					x			
802.11a 5.2 GHz					x					x		
WiMAX 5.8 GHz						x					x	

Table 2. Dual-band signal construction table.

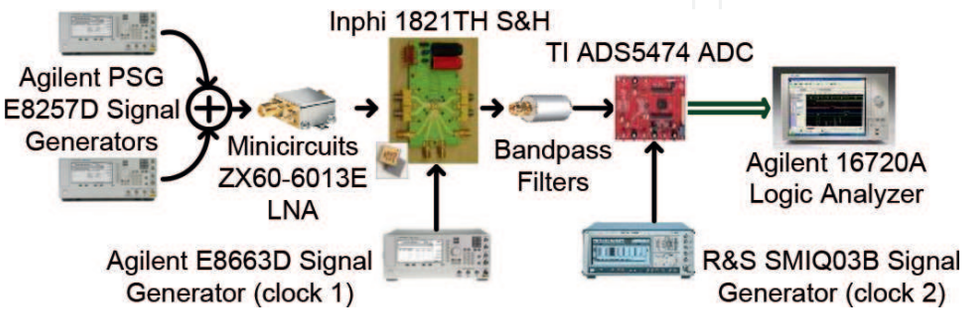

Figure 9. Experimental setup for dual-band subsampling receiver.

The simulated subsampled spectra for RF signals at 2.12 and 2.4 GHz (dual-band scenario 12, Receiver Design 4) are shown in **Figure 10**, where the expected bandwidth of each dual-band signal is 5 MHz, and we assume a fifth nonlinearity order. The S&H subsampling frequency was set to 1900 MHz, and the ADC subsampling frequency was set to 400 MHz. **Figure 11** shows the

Receiver design (RD)	Receiver's architecture
2	$f_{s1} = f_{s2} < 400$ MHz, without bank of filters
4	$f_{s1} < 2$ GHz, $f_{s2} < 400$ MHz, without bank of filters
5	$f_{s1} < 2$ GHz, $f_{s2} < 400$ MHz, with a bank of two filters in [0–400] and [400–800] MHz
6	$f_{s1} < 2$ GHz, $f_{s2} < 400$ MHz, with a filter fixed in [0–400] MHz
7	$f_{s1} < 2$ GHz, $f_{s2} < 400$ MHz, with a filter fixed in [0–400] MHz
8	$f_{s1} < 2$ GHz, $f_{s2} < 400$ MHz, with a filter fixed in [0–200] MHz

Table 3. Subsampling receiver's architectures.

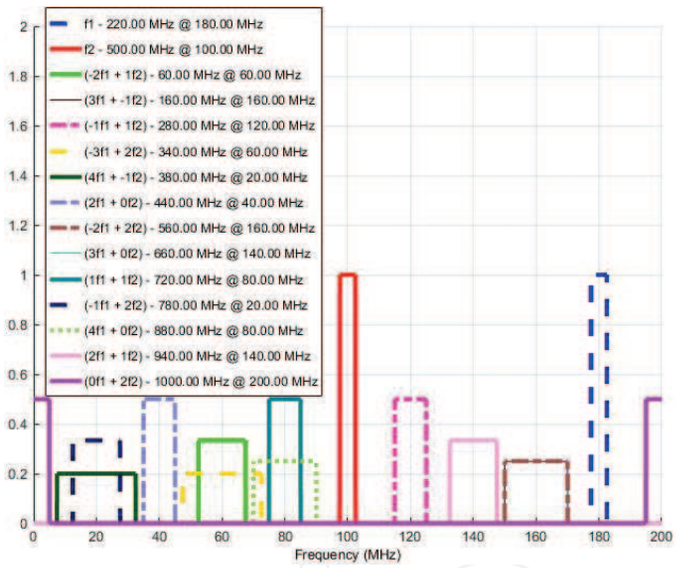

Figure 10. Simulated spectra after two-stage subsampling process.

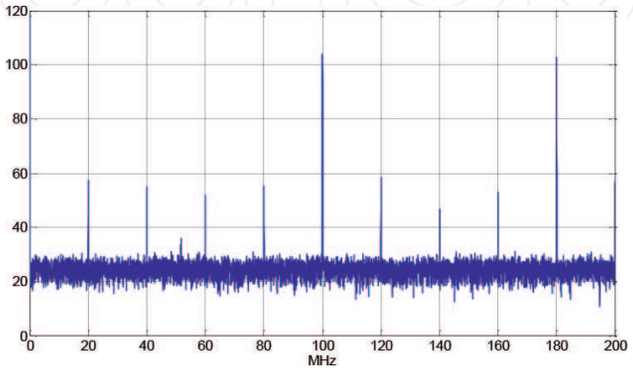

Figure 11. Experimental spectra after two-stage subsampling process.

captured output spectrum using the experimental setup. Observe that, after the first S&H, the RF signals have been down-converted to 220 and 500 MHz. After the second S&H, they are translated to 180 and 100 MHz, respectively. The subsampled signals, their harmonics, and intermodulation products are located as predicted by the simulation illustrated in **Figure 10**.

Finally, **Figure 12** shows the measured SNR for 12 different dual-band signal scenarios [15].

Using a multiplexed bank of filters (RD 5) presents more advantages and leads to better signal quality than receiver designs that use fixed filters (RD 6/7). The pros for these filter architectures (either fixed or multiplexed) are the elimination of a higher number of nonlinear components and the reduction of the out-of-band noise in the input ADC. However, when the carrier RF separation for the two bands is relatively small, it is difficult to find a large sampling frequency that folds both bands into one band-pass filter and, therefore, the effect of folded noise increases. It is possible to observe this problem in some dual-band scenarios using RD 8. Taking into account all these considerations, dual filter band-pass architecture seems to be an effective solution that offers reasonable performance without a sharp increase in the complexity (number of filters) for well-frequency-spaced dual-band wireless applications.

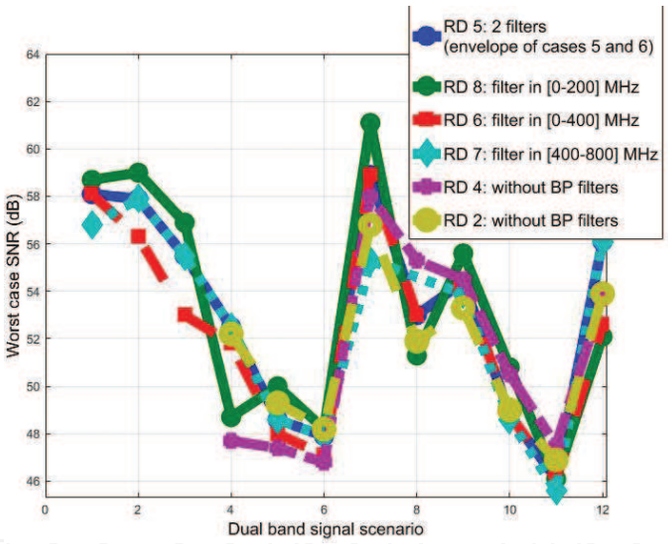

Figure 12. Experimental SNR for the proposed architectures.

2.4. Subsampling-based systems for cognitive radio applications (II): integration with compressive sensing techniques

2.4.1. Fundamentals of compressive sensing

Compressive sensing is an emerging alternative to Nyquist sampling for the acquisition of sparse signals [16]. The general idea is that the spectral information of a signal is not necessarily as large as its bandwidth occupation. This paradigm has been also named analog-to-information (AI) conversion [17], since the receiver is designed considering the mathematical structure of the signals rather than their bandwidth. The AI converter output is not the

received waveform, but the minimum number of data to encode the information of interest, that is, its compressed version.

By using CS principles, it is possible to implement a reliable reconstruction of the signal of interest (SOI) from a reduced number of samples. Instead of taking periodic samples, CS measures products with M properly chosen measurement vectors, where M is much smaller than the number of Nyquist rate samples. Mathematically, let $X = [x_1, x_2, \ldots, x_N]$ be the input signal, where x_i are its individual samples and N is the number of samples. The CS measurements y_k are the projections of X onto a measurement vector φ_k. Formally, $y_k = (X, \varphi_k)$ for $k = 1, 2, \ldots, M$, where M is the number of measurements [18]. For this technique to be useful, the signal has to be sparse in the basis $\{\varphi_k\}$, that is, the signal is expected to have a limited number of nonzero components when they are represented or projected in that basis. Although real-world signals are not totally sparse, as they cannot be completely band-limited and there is always noise embedded in the bandwidth, in many cases it is possible to obtain accurate approximations. In the end, CS enables us to reduce the requirements at the receiver and operate at a low data rate. However, CS also has two important challenges: (1) to select the appropriate number M of sub-Nyquist samples and measurement vectors, and (2) the need to carry out computationally expensive algorithms to recover the signal from its projections. Note, however, that we do not need to implement these algorithms with analog circuitry; rather, they can be performed in the digital domain.

2.4.2. Optimization of compressive sensing architectures: integration with subsampling-based systems for scanning of wideband spectrum application

Due to the underutilization of the radio spectrum, its occupancy can be usually considered sparse. Under this assumption, CS technique is a feasible alternative to many cognitive radio applications, where a reaction in real time is necessary, such as dynamic spectrum sensing [19, 20], interferer's mitigation [21], power spectrum estimation [22], or sparsity order estimation [23]. All these applications are focused on identifying spectrum opportunities over a wideband spectrum rapidly and accurately, so that we can share and exploit these limited radio resources in real time.

Although the computational burden is pretty high for CS techniques, there are many research works that aim to reduce this complexity, mainly at signal processing level. As an alternative, in this section, we address some ideas to reduce the complexity at circuit level, proposing the integration of compressive sensing with the subsampling algorithms proposed in the previous sections. The final objective is to integrate the advantages of both techniques, that is, a few number of samples for each SOI by using a cost-effective and flexible alternative receiver and avoiding the use of high-speed ADC circuitry.

Originally, the basic considered options to implement the CS receiver architectures for spectrum sensing applications have been homodyne and heterodyne receivers. A homodyne receiver with a wideband front end is able to implement rapid detections, but it implies the use of high-speed ADCs, which make these solutions impractical. A heterodyne receiver, where the signal channels are selected individually for downconversion to baseband, can be implemented by using a lower data-rate ADC, but they are impractical for spectrum sensing applications because the time to detect idle channels is higher than the homodyne case [19],

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due to the fact that heterodyne receivers consume time for switching to a new channel, apart from the time required by the detection algorithm, once the channel is selected. As a compromise solution, subsampling-based receivers enable us to use a low-cost ADC and provide a fast spectrum scanning [19].

Previously to the idea of using subsampling-based systems for CS applications, several receiver architectures have been proposed, which can be classified into two classes: nonuniform samplers and random (or pseudo-random) pre-integrators (**Figure 13**) [17, 24]. However, the performance of these sub-Nyquist schemes depends on the sparsity level, that is, the employed reconstruction algorithms will only work accurately if most of the channels in the spectrum are idle, leading in many cases to higher computational complexity and longer signal-processing times. Furthermore, although the ADCs in **Figure 13** work at a sub-Nyquist rate f_s, the detector requires analog components capable to work at Nyquist rate: for the nonuniform sampler, a Nyquist rate clock is required for the shifters (φ_i in **Figure 13a**); for the random pre-integrator, a Nyquist rate random generator ($p_i(t)$ in **Figure 13b** before the integrator $h(t)$) is required as well [19]. Besides the high-rate requirement for high bandwidth, a higher frequency of the digital parts in a mixed-signal system involves a higher injected noise into the analog parts. Consequently, subsampling-based systems emerge as a feasible alternative to implement CS receivers that avoid the operation at Nyquist rates.

In Ref. [19], a subsampling-based receiver is proposed to overcome the constraints detailed before, by sampling under Nyquist the input signal with a multiple branch architecture (**Figure 14a**), where there is a compromise between the number of branches and the scanning time. Although the results presented in Ref. [19] constitute a middle solution in terms of low-complex circuitry and fast detection, the proposed architecture improves the efficiency when searching idle slots. To this end, the methodology described in Section 2.3.3 for multi-band scenarios can be used with two main objectives:

1. Minimization of the number of branches in **Figure 14a**. As described in Section 2.3.5, applying the methods proposed in Ref. [15], it is possible to find the optimal band-pass filtering architecture, by searching the valid set of sampling frequencies in order to avoid aliasing with the interferers (**Figure 14b**), and also attending to requirements of folded noise reduction by using the principles of multiple clocking techniques (Section 2.2). Therefore, a similar scheme integrated in **Figure 14a** could minimize the number of branches, since the possibilities of aliasing in multi-band scenarios are reduced.

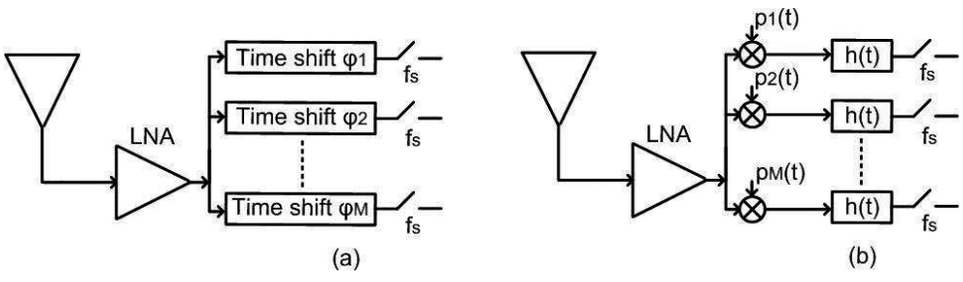

Figure 13. Nonuniform samplers (a) and random pre-integrator (b) architectures.

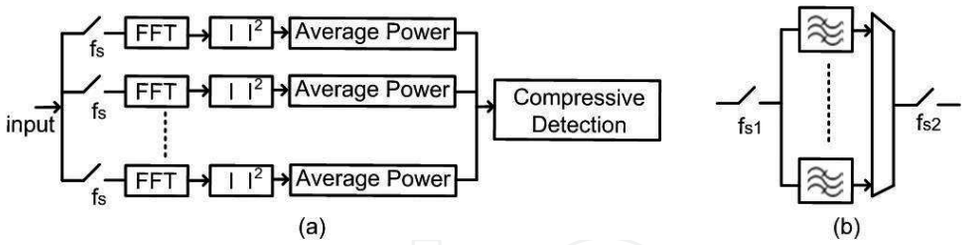

Figure 14. Subsampling architecture proposed in Ref. [19] (a) and Ref. [15] (b).

2. From the predefinition of these sets of valid frequencies, it would be possible to reduce the scanning times of idle slots, improving the efficiency of the architecture proposed in [19].

Finally, this approach is extensible to more realistic scenarios, by introducing the equations for nonlinear environments described in Section 2.3.4.

3. Interleaving techniques

3.1. Overview of the time-interleaved ADCs concepts

Time-interleaved ADCs (TI-ADC) are an effective approach for achieving very high sampling rates. A TI-ADC time-multiplexes M parallel ADCs with slightly delayed sampling instants, which is equivalent to a single ADC operating at a much higher sampling rate. The concept is illustrated in **Figure 15**. Ideally, the ith ADC, $i = 0,\ldots, M - 1$, samples periodically the input signal at time instants t_i, t_{i+M}, t_{i+2M}, … with sample rate f_s/M, where $t_m = mT_s$ and $T_s = 1/f_s$ is the sampling period of the TI-ADC. The final output is created by multiplexing all the individual ADC outputs in the proper order (e.g., ADC_0, ADC_1, …, ADC_{M-1}, ADC_0, ADC_1, etc.). Thereby, the final effect is as if the input signals were sampled once every T_s seconds, that is, with sample rate f_s. This approach has been widely adopted in many communication systems for wideband spectrum applications, since the converters can work at lower speeds without sacrificing the overall system performance. However, it should be noted that each individual ADC deals with the entire analog input signal, and, therefore, its S&H circuit must be able to preserve the full input signal bandwidth.

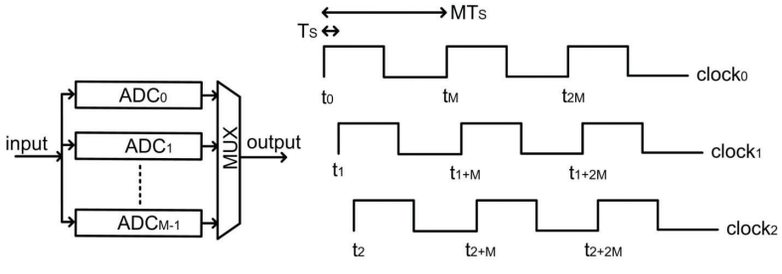

Figure 15. Architecture of a TI-ADC.

3.2. Analysis of time-interleaved ADCs: mismatch errors and calibration techniques

3.2.1. Mismatch errors in interleaving-based systems

Let $x(t)$ be an analog signal with Fourier transform $X_a(\omega)$ and consider that the TI-ADC produces the sequence:

$$x(t_0), x(t_1), x(t_2), \ldots, x(t_m), \ldots, x(t_M), x(t_{M+1}), \ldots \tag{18}$$

The discrete-time Fourier transform is defined by[1]

$$X(\omega) = \sum x(t_k)\exp(-j\omega t_k) \tag{19}$$

Ideally, the samples are spaced $T_s$seconds apart. Then, it can be shown that

$$X(\omega) = f_s \sum X_a\left(\omega - k2\pi f_s\right) \tag{20}$$

which is the well-known spectrum representation of a uniformly sampled signal. It results in a periodic spectrum with a period equal to the sampling rate [25]. In practice, however, there are deviations from the ideal behavior that are caused by the mismatches between the individual ADCs. There are three main possible sources of error in TI-ADCs: *clock timing errors*, *gain errors*, and *offset errors*. A brief review of all of them is included in the subsequent sections.

3.2.1.1. Clock timing errors

Clock timing errors occur when the digitization clocks of the individual ADCs are not appropriately synchronized. As a result, the input signal $x(t)$ is sampled in such a way that the sampling time instances are not necessarily uniformly spaced in time. Errors may be systematic (skew) or random (jitter). Taking this factor into account, Eq. (20) becomes [25]

$$X(\omega) = f_s \sum H_k(\omega) X_a\left(\omega - k2\pi f_s/M\right) \tag{21}$$

where

$$H_k(\omega) = \frac{1}{M}\sum \exp(-j[\omega - k(2\pi/MT_s)]\, r_m T_s)\exp(-jkm(2\pi/M)) \tag{22}$$

where $r_m = (t_m\text{-}mT_s)/T_s$ is a ratio that measures the timing errors (ideally, $t_m = mT_s$). It can be noticed that, in contrast with the ideal case, the spectrum is repeated in Eq. (21) every integer multiple of the frequency f_s/M (not f_s). In other words, spurious replica spectra (called *image spurs*) will appear at

[1]In the literature, it is a common notational practice to replace $\omega t_k$with a single variable $\omega' = \omega t_k$, called *normalized frequency.* Since ω represents ordinary frequency (radians per second), ω' is expressed in units of radians (per sample). Recall also that by sampling the discrete-time Fourier transform, we obtain the discrete Fourier transform (DFT).

$$f_{\text{imagspurs}} = \pm f_i + k\frac{f_s}{M}, \quad k = \pm 1, \pm 2, \pm 3, \ldots \tag{23}$$

These replicas hamper the interpretation of the spectrum of the input signal, as they may be confounded with true signal's frequency components. In addition, even if the image spurs are eliminated, we find that the spectrum of the signal reconstructed from the given samples is equal to $H_0(\omega)X_a(\omega)$. This is equivalent to passing the original input signal through a filter of transfer function $H_0(\omega)$, which introduces distortion and must be corrected by an equalizer. Assuming that the input signal is a pure tone of frequency f_i, and that f_i is a Gaussian variable with zero-mean and variance σ^2 for all *m, th*e signal-to-noise and distortion ratio (SNDR) is approximately found to be [25]

$$\text{SNDR} = 20\log\left(\frac{f_s}{2\pi f_i}\right) - 10\log\left(1 - \frac{1}{M}\right). \tag{24}$$

3.2.1.2. Gain errors

The gains of each ADC may be different, implying that, for example, even for a DC input each ADC may produce different output codes. The analysis is similar as for timing errors. Gain errors also produce image spurs at

$$f_{\text{imagspurs}} = \pm f_i + k\frac{f_s}{M}, \quad k = \pm 1, \pm 2, \pm 3, \ldots \tag{25}$$

where f_i is the input frequency. A formula for the SNDR, taking into account the contribution of gain and offset errors, will be given a few lines below.

3.2.1.3. Offset errors

The offsets of each ADC may be also different and then, as with the gain mismatch case, even a DC input may produce different outputs. Offset errors cause noise peaks (*offset spurs*) at

$$f_{\text{offspurs}} = k\frac{f_s}{M}, \quad k = 0,\ 1,\ 2,\ 3, \ldots \tag{26}$$

Assuming that the gain and offset errors are Gaussian distributed, with respective variances σ^2_{g} and f_i, and that the input signal is a sinusoid with amplitude A, the SNDR equals to [26]

$$\text{SNDR} = 10\log\left(\frac{A^2}{A^2\sigma_a^2 + 2\sigma_b^2}\right) \tag{27}$$

which is independent of the degree of interleaving M. The image and offset spurs are illustrated by the example shown in **Figure 16**. The input signal is a sinusoid at a frequency of 2.3 GHz that is sampled at f_s= 6 GHz, and the TI-ADC has three channels (i.e., three individual ADCs in parallel). In practice, clock timing errors are the most critical (gains and offsets can be

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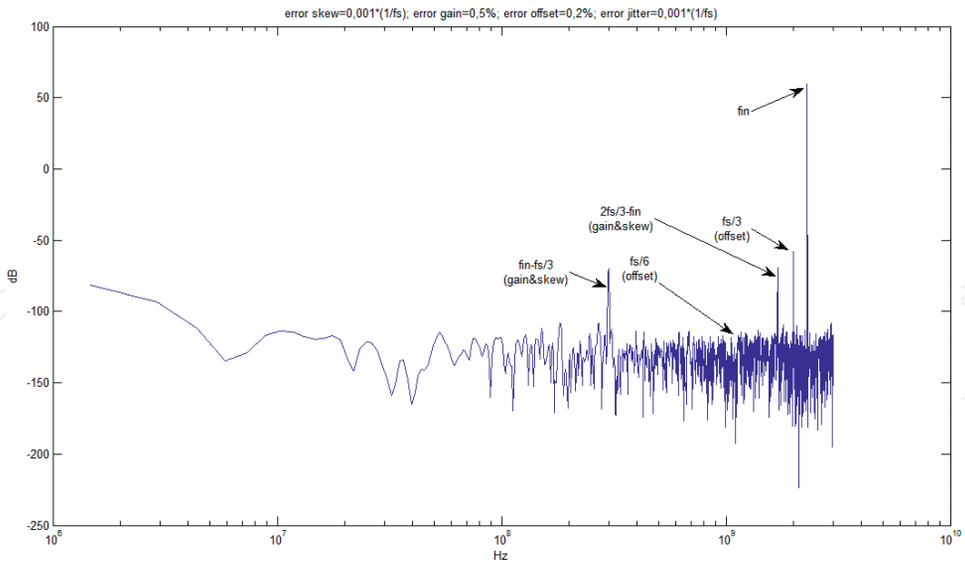

Figure 16. Output spectrum of a three-channel TI-ADC.

calibrated more easily). Several approaches have been proposed to deal with mismatches between individual ADCs. Some of the most relevant are presented in the subsequent section.

3.2.2. Calibration techniques

The mismatch errors described in the last section need to be corrected in order to maximize the benefits of interleaving systems and increase the ADC resolution, avoiding the degradation of the SNDR of the analog-to-digital system. To implement interleaving systems, several approaches, which differ in the calibration method and in the intended application, are possible. This section begins with a brief summary of the most prevalent calibration methods, discussing their advantages and disadvantages. Then, a review of several approaches for designing SDR, ultra wideband (UWB), and multistandard systems will be presented.

In Ref. [27], where an ADC system for UWB is described, two basic (nonexclusive) options to calibrate the system are presented: (1) controlling the ADC mismatches in the integrated circuit fabrication process and (2) using digital preprocessing or postprocessing techniques to mitigate the impact of image and offset spurs. The first one consists of reducing the electrical and physical differences between the channels. The gain is typically controlled using a common reference voltage and carefully designing the layouts. Phase matching is achieved by ensuring that all the clock paths are as similar in length as possible. Nevertheless, unlike approaches based on digital processing, these techniques are not well suited for implementations based on COTS (Commercial Off The Shelf), which is very convenient for SDR designs due to its flexibility and ease of programming.

Digital processing techniques have several advantages, including technology scaling, flexibility, the ease of portability to the next technologies generation, a low power consumption, and the possibility of being implemented through a cheap CMOS process. Moreover, digital techniques are more efficient for the compensation of timing skews than analog techniques, due to

the fact that they are more stable with the temperature and the wide bandwidths used in SDR applications. Digital processing techniques are also easier to implement, can be designed with more precision, and take advantage of the last advances in high-speed and configurable digital hardware platforms (DSPs, FPGAs, CPLDs, and ASICs) [28].

In spite of the previously stated digital processing advantages, analog calibration techniques have benefits as well. For example, one advantage of analog offset calibration is that the correction values do not suffer from quantization [29]. Thus, the ADC offset can be corrected to less than one LSB without adding the extra bits needed when the offset correction is performed in the digital domain [30]. Furthermore, analog gain correction can be implemented by simply adjusting the reference voltage (so that using high-speed multi-bit digital multipliers to scale the ADC outputs becomes unnecessary).

Calibration techniques can be also classified into "background" and "foreground" techniques [31–33]. Sometimes, they are also named as, respectively, "online" and "offline" calibrations. Offline calibration requires less circuitry, but interrupts the normal operation of the ADC. It is usually applied when the parameters of the circuit do not vary much with environmental parameters (e.g., voltage or temperature). On the other hand, background techniques enable continuous calibration, with the ADC running in normal operation, and are suitable to be used when disconnecting the ADC is not an option [34].

A particularly appealing background approach is the one based on randomization [32]. In this approach, the ADC channel is selected randomly for each sampling instant. This can be performed using a digital circuit (thus avoiding the need for new analog circuitry), which constitutes the main benefit of this approach. Considering $M + X$ individual ADCs, we can choose at each time instant among $X + 1$ channels without violating the sampling rate of each individual ADC. This is illustrated in **Figure 17a** and **b**. In **Figure 17a** [35], a 3-ADCs system is presented with $M = 3$ and $X = 0$: noting that each ADC samples every 3 T_s seconds, where T_s is the sampling period of the total system, the only possible outputs are *A B C A B C A B C*… or *A C B A C B A C B*… For example, considering the first case, after the three channels (*A, B, C*) have taken a sample we can only choose *A* without violating our sampling constraint. Next, only *B* can be selected and so on. Therefore, to enable the randomization process, one or more extra ADCs (i.e., $X > 0$) must be employed [35]. In this way, there always exist at least two available ADCs at each sampling time. This case is illustrated in **Figure 17b**, which considers the case $M = 2$ and $X = 1$: after the first two channels have been selected, for example, *A* and *B*, we can decide between *A* and *C* and so forth.

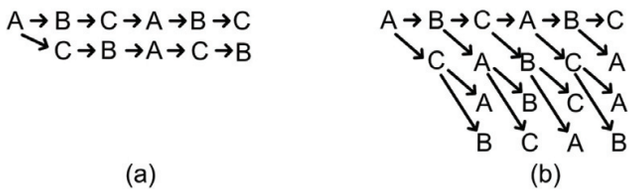

Figure 17. (a) 3-ADCs (*ABC*) for three times sampling rate and (b) 3-ADCs (*ABC*) for a double sampling rate.

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An example of this architecture is illustrated in **Figure 18a**, where ΔM extra ADCs have been added.

Although this structure implies an additional hardware cost, Dyer et al. [35] demonstrates that as X tends to zero (in order to reduce the cost), noise becomes non-white (it is not flat). Therefore, a trade-off between the value of X and the cost of having nonactivated ADCs (note that it is not convenient to have largely underutilized ADCs, which occurs when X is much larger than M) is necessary. A clock diagram for $M = 4$ and $X = 1$ is shown in **Figure 18b** [35]. The sequence of randomly chosen ADCs is shown at the top of the figure.

Apart from the use in randomization techniques, an extra ADC might be employed in other background approaches. Doris et al. [33] use an additional ADC to implement an analog background circuit which calibrates the gain and offset mismatch. The basic idea of this technique is to use $M + 1$ ADCs so that M ADCs are always active while the remaining one is being calibrated. When the calibration cycle is finished, another ADC is selected for calibration, being replaced in the conversion mode by the previously calibrated ADC. The calibration of these ADCs is performed using another ADC as a reference, in order to match gain and offset with it. Therefore, an analog calibration is implemented. Since this method is based on a background process, it is not necessary to stop the analog-to-digital conversion and, in addition, it is more efficient as the number of ADCs increases. However, the main drawbacks are the noise introduced by the additional analog circuitry, and the degradation in speed when extra ADCs are used to substitute the ADC under calibration [36].

Moreover, there are also calibration techniques specifically devised either for static (i.e., gain and offset) or dynamic errors (i.e., clock skew). For example, an alternative method for calibrating the static mismatches is to employ a DAC (digital-to-analog converter) with enough resolution to meet the requirements [37], using one of these DACs for each ADC in the interleaved structure. A common alternative to reduce the cost of the extra circuitry due to the added DACs is to implement the gain and offset calibrations after a FFT (fast Fourier transform)

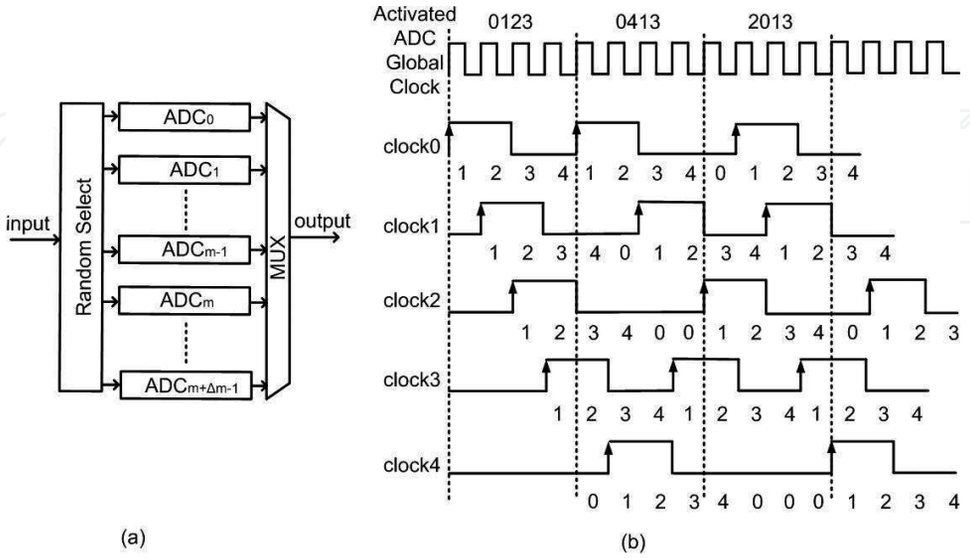

Figure 18. (a) Example of a structure with extra ADCs and (b) random clock for 5 ADCs.

evaluation, via software, achieving the compensation from the study of the output spectrum [38]. An additional benefit of this technique is to take the advantage of the repetition and symmetry properties of the FFT [39].

On the other hand, clock skew errors are difficult to correct and lead to more stringent limitations on interleaved architectures [40], especially for SDR and UWB applications as explained in Ref. [27]. Unlike static errors, dynamic errors depend on the input frequency and can be theoretically characterized from the aperture jitter and aperture delay of the internal S&H of each ADC. Although the aperture jitter affects high-frequency systems, its value (less than 1 ps) is usually much lower than the delay jitter (a few nanoseconds) and, therefore, it may be ignored in many interleaving-based systems. Moreover, the aperture delay strongly depends on the temperature. As a consequence, there are many unknown factors affecting these timing mismatches that make the estimation of the spurious component level even harder.

Some traditional ideas for correcting the skew errors are to add programmable delay lines or to implement a signal postprocessing. Dyer et al. [35] propose this method to reduce the spurious level though additional hardware is required. Another specific technique for timing errors correction is the one based on polyphase digital filter blocks [41], which can be easily implemented using an FPGA and, therefore, results highly suitable for SDR applications based on COTS. An example of this structure is illustrated in **Figure 19**, where the FPGA includes, as well as the filter implementation, a precision voltage reference, a low jitter clock distribution circuit, and a digital sensor to control the effect of temperature on the skew [28].

The filter structures used to calibrate these dynamic errors are designed as a function of the number of channels (i.e., number of ADCs). Reference [41] gives the ratio (R) between the number of channels (M) and the number of necessary filters (N), this ratio being lower when the number of channels is increased. For instance, in this work $N = 3$ for $M = 2$ ($R = 0.75$), $N = 5$ for $M = 3$ ($R = 0.556$), and $N = 27$ for $M = 8$ ($R = 0.422$). As a consequence, for a high number of ADCs this method is not efficient. Another inconvenience is that this technique is limited to a

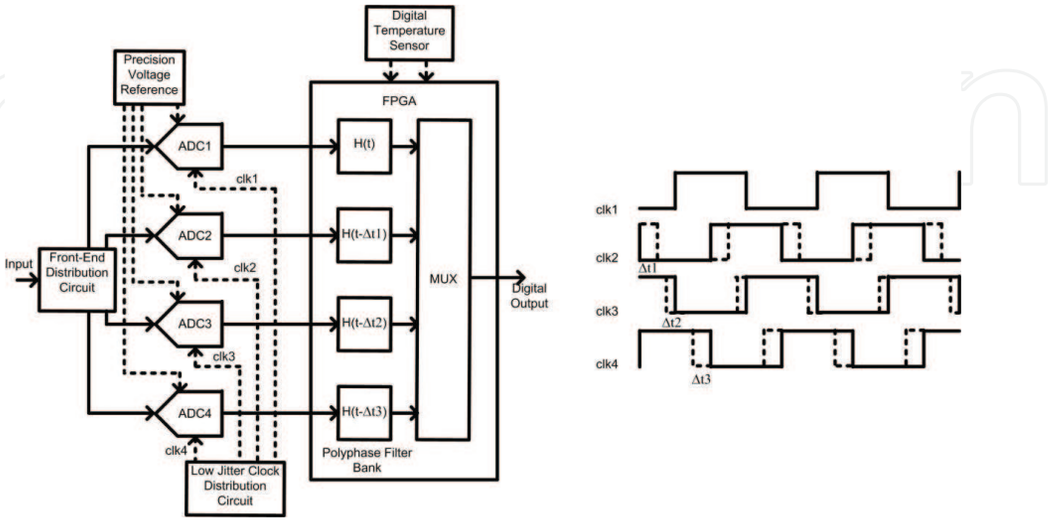

Figure 19. Functional diagram using digital filters blocks.

single-frequency input signal, and the filter coefficients would have to be frequently recalculated, thus increasing the calibration process complexity [42]. Lastly, an additional drawback of this method is that conventional filters do not have enough resolution to tune the group delay in the highest frequency systems, where the calibration precisely has to be more accurate [43]. Thus, designing these filters is an important challenge in their own.

3.3. Interleaving for cognitive radio applications: implemented systems and integration with subsampling and compressive sensing techniques

Placing the ADC interface as close to the antenna as possible in the signal path enables direct sampling of broadband multi-carrier signals of different standards with complex modulation schemes. Interleaving-based ADCs are a feasible alternative in order to achieve these objectives of cognitive radio, mainly for the base-station receivers, where the whole bandwidth has to be converted.

Many research works have been published in order to implement receivers and ADC systems based on interleaving techniques, most of them with application in SDR. Some of these systems are implemented in IC, whereas others are implemented with COTS, leading to some benefits for SDR applications, such as significant time and cost savings compared with developing an integrated circuit.

A very relevant time-interleaving system based on COTS is presented in Ref. [27]. In this system, eight ADCs MAX104 sampled at 1 GSPS are connected to obtain a total sampling frequency equal to 8 GHz, although, since the digital processing is implemented on a FPGA, the final frequency is equal to 6.4 GHz, due to speed restrictions of the device. Even though this is an inconvenience for high-speed circuits, the FPGA provides the necessary flexibility for SDR and UWB applications. Moreover, this solution means a reasonable tradeoff between cost and complexity. The proposed system presented in Ref. [27] employs a digital calibration scheme based on filters, obtaining an SNR around 30–35 dB (i.e., around 5–6 bits) at the maximum operation frequency.

Other systems based on interleaving techniques are not implemented by COTS but integrating all the system, including the calibration part (calibration on-chip). This solution is more convenient for analog or DAC-based calibration, reducing the power consumption [32, 44]. In [32], four ADCs are connected to obtain an SNDR around 48 dB for a total sampling frequency of 2.6 GHz. In Ref. [44], two ADCs are combined to achieve an SNDR higher than 54 dB for a sampling at 1 GHz.

There are other TI-ADCs which combine analog and digital calibration. For instance, Tamba et al. [34] use DACs to correct offset errors in the analog domain and background digital calibration to reduce the clock-skew effects. Using both methods, this work implements an 8-ADCs array to obtain a resolution of 5 bits at 12 GS/s operation rate. A similar work with cognitive radio applications is described in [45], where a resolution of 5.1 bits is obtained with 8 TI-ADCs operating at 10.3 GS/s.

Finally, there are some TI-ADCs that have applied successfully background digital calibration for dynamic and static errors compensation, as [46], which obtains 6 bits at 16 GS/s for eight

different channels, and [47] that presents a wide-band analog-to-digital system for cognitive radio applications as well.

On the other hand, an important issue about the implementation of TI-ADCs is the connection between the S&Hs and ADCs. There are two possible structures, which are illustrated in **Figure 20** [40]. One of them uses only one S&H connected to several ADCs (**Figure 20a**). In this case, the main inconvenience is that the number of ADCs connected to the S&H is limited and, therefore, since this number of ADCs is directly proportional to the total sampling rate, the scalability will be limited as well. When each TI-ADC is preceded by its own S&H (**Figure 20b**), the scalability is theoretically increased because this architecture is not limited by a maximum number of ADCs connected to the S&H. However, the clock skew effect between the different S&Hs will degrade the final SNDR and, therefore, the final number of TI-ADCs will also be limited in this case, as it is shown in Eq. (24).

With the objective of reducing the number of S&Hs, Gupta et al. [40] propose a structure based on double sampling (**Figure 21**). Since using this solution the loading of the S&H is not directly dependent on the number of TI-ADCs, the scalability is increased with respect to the structure shown in **Figure 20a**. Besides, the mismatch errors and the power consumption are reduced with respect to the scheme shown in **Figure 20b**.

Additionally, interleaving techniques can be integrated with the previously detailed sub-sampling techniques with the objective of implementing SDR receivers that exploit the advantages of both technologies. For example, a high-resolution and high-analog bandwidth multiple clock subsampling-based system can improve its folded noise performance (Section 2.2) by using TI-ADCs to increase the second sampling rate f_{s2}. This solution would allow a higher intermediate frequency, which is folded by a higher first-sampling rate f_{s1}, reducing the thermal noise effect.

Integration of both techniques also can be used with other objectives. Louwsma et al. [48] propose a time-interleaved multichannel track and hold for a subsampling-based SDR receiver, with 48 dB of SNDR at 1.35 GS/s. This technique can be used to increase the total sampling rate as well. In this case, Louwsma et al. [48] propose to apply subsampling directly at the first track and hold. Furthermore, digital calibration techniques are usually employed only for band-limited signals in the first Nyquist band, so that they cannot be directly applied for band-pass-sampling schemes. Therefore, some research works are dedicated to calibration algorithms focused on undersampled signals. An example is Ref. [49], which validates the

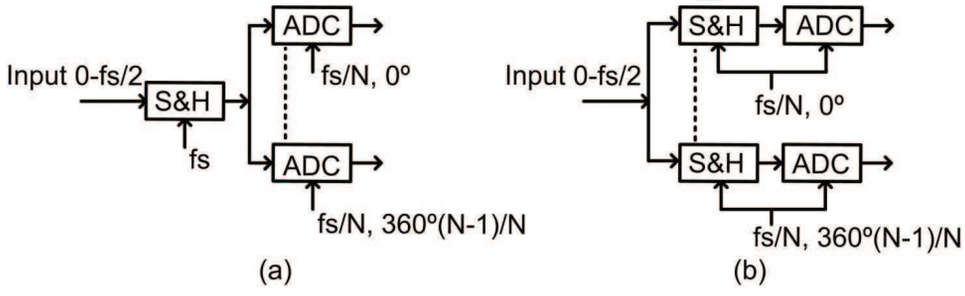

Figure 20. Architectures based on (a) one S&H and (b) several sub-S&H.

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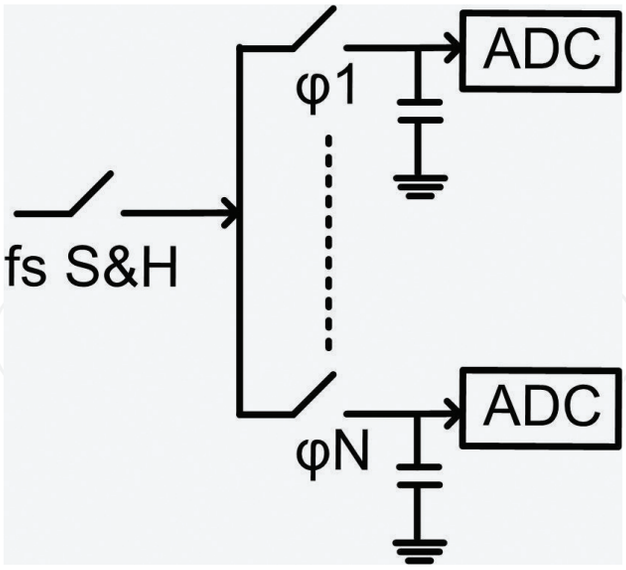

Figure 21. Architecture based on double sampling.

precision and convergence of its proposed digital background calibration method for clock-skew calibration of a two-channel subsampled TI-ADC. More recently, Duc et al. [50] has presented a novel digital background calibration for clock skew, by using a polyphase-filtering technique, which is applied to a four-subsampled channel TI-ADC. The system is clocked at 2.7 GHz, achieving an 11-bit resolution in a 5.3-GHz analog bandwidth, that is, the proposed calibration method is extended to the fourth Nyquist band. Since these receiver architectures are designed for SDR applications, the calibration efforts are usually focused on clock skew errors, since they increase with the input frequency and overshadow the effect of other mismatches for broadband inputs.

Finally, it is also remarkable that interleaving techniques have been recently incorporated to the compressive sensing systems described in Section 2.4.1, with the main objective of implementing fast spectrum sensing for cognitive radio applications. For example, Moon et al. [51] present some novel reconstruction algorithms for a 2-TI-ADC wideband sparse-based receiver, without requiring an accurate clock skew calibration and reducing the number of detection channels. However, other works are focused on calibration techniques, such as Ref. [52], where a clock skew adjustment method is proposed for sparse spectrum applications, or Ref. [53], which studied the influence of the mismatch errors, described in Section 3.2.1, in the quality of the reconstructed signal.

4. Conclusions

This chapter reviews several methods for implementing the analog-to-digital conversion stage to achieve the objectives of SDR and CR paradigms, becoming efficient alternatives to conventional receivers. In a first part, we describe how a subsampling-based system is an appealing option in order to implement tunable and cost-effective multistandard receivers for dynamic spectrum

access applications, detailing a multiple clocking technique in order to reduce the folded noise effect. We extend this idea to nonlinear and multi-band environments for spectrum sensing applications, proposing an algorithm to find the optimal sampling frequency in order to avoid the nondesired interferences. As a second cognitive radio application, we introduce techniques based on compressive sensing for the cases when the occupancy of the spectrum is very low, meeting the sparsity property. We propose the integration with subsampling architectures to implement a compressive sensing-based receiver and reduce the complexity of the receiver. Therefore, with the objective of addressing the spectral underutilization problem, we apply the algorithms proposed for nonlinear and multi-band scenarios to reduce the computational burden and the searching time of idle channels for spectrum sensing and spectrum sharing applications. The second part of the chapter is dedicated to interleaving techniques, which are based on several ADCs connected in parallel with the objective of maximizing the sampling frequency. Although the resolution is decreased by using these techniques, due to the generated mismatch errors, their effects can be minimized implementing calibration techniques such as those proposed in this chapter. Finally, we describe the benefits of integrating interleaving-based systems with architectures based on subsampling and compressive sensing, with the objective to combine the advantages of these techniques in a unique analog-to-digital system.

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