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Chapter 1

Introductory Chapter: VLSI

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1. Introduction

Back in the old days about 40 years ago, the number of transistors found in a chip was, even at its highest count, less than 10,000. Take, for example, the once popular Motorola 6800 microprocessor developed in the mid 1970s. Fabricated based on the 6.0-μm feature size, the 6800 consisted of merely 4100 transistors in it. Nowadays, the number of transistors in a very large-scale integration (VLSI) [or some refer to it as the super large-scale integration (SLSI)] chip may possibly reach 10 billion, with a feature size smaller than 15 nm.

There is little doubt that the electronics world has experienced a significant advancement for the past 50 years or so and this, to a large extent, is due to the rapid technology improvement in the performance, power, area, cost and 'time to market' of an integrated circuit (IC) chip. To provide readers with an overall view of VLSI, this chapter gives a concise but complete illustration on the historical evolution, design and development of VLSI-integrated circuit devices.

2. A brief history

When transistors were first introduced in early 1900s, they were actually made of vacuum tubes. These transistors were relatively large in size and cumbersome to be used. In December 1947, however, three physicists working in the AT&T Bell laboratory attained a remarkable breakthrough in their design, changing the perception one used to have on transistors. Dr. John Bardeen, Dr. Walter Houser Brattain and Dr. William Bradford Shockley, Jr., invented the first point-contact semiconductor transistor using germanium. As shown in **Figure 1**, the point-contact transistor comprised an n-type germanium block and two gold contacts (i.e. the emitter and collector leads) placed in close proximity. When a small current was applied to one of the contacts, the output current at the other contacts was amplified.

Being much smaller in size, consuming much lower power, operating at relatively lower temperature and giving quicker response time, the semiconductor transistor is clearly more

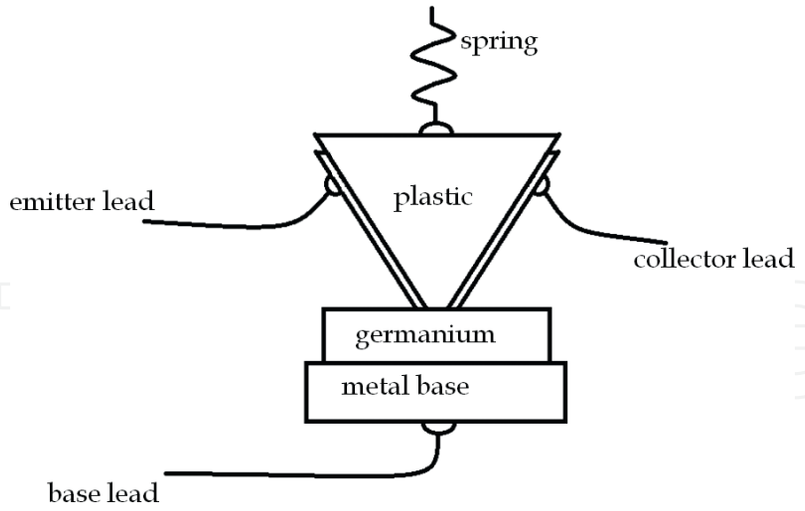

Figure 1. An early model of the point-contact transistor.

superior to its conventional vacuum tubes brethren. It was these advantages and its viability that resulted in the replacement of vacuum tubes by the solid-state electronic devices. The rapid widespread usage of the semiconductor transistors in electronic circuits has triggered a dramatic revolution in the electronic industries, kicking off the era of semiconductor. Because of this significant contribution, Bardeen, Brattain and Shockley shared the Nobel Prize in Physics in 1956.

It may be worth noting that when this germanium solid-state device was initially introduced, it was not coined the term 'transistor'. Instead, it was generally referred to as the 'semiconductor triode'. According to the 'Memorandum For File' of Bell Telephone Laboratories [1], six names had been proposed for the device, namely 'semiconductor triode', 'surface states triode', 'crystal triode', 'solid triode', 'iotatron' and 'transistor'. Although the device had initially been referred to as the 'semiconductor triode', the word 'transistor' (which originates from the abbreviated combinations of the words 'transconductance' and 'varistor') had ultimately turned out to be the winner of the internal poll [1].

The first commercially available silicon transistors were manufactured by Dr. Gordon Kidd Teal in 1954. Since silicon gives much better performance than germanium transistors, the substrate material for transistors was gradually changed to silicon. In 1955, the first diffused silicon transistor made its appearance. To reduce the resistivity of the collector, the transistor with an epitaxial layer added onto it was developed in 1960. It was also in the same year the planar transistor was proposed by Dr. Jean Amedee Hoerni [2].

In 1958, Jack St. Clair Kilby who was then an engineer in Texas Instruments successfully developed the first integrated circuit. The device was just a simple 0.5-inch germanium bar, with a transistor, a capacitor and three resistors connected together using fine platinum wires. About a year later in 1959, Dr. Robert Norton Noyce from Fairchild Camera (also one of the co-founders of Intel Corporation) invented independently his own integrated circuit chip. The interconnection in Noyce's 4-inch silicon wafer was realized by means of etching the aluminium film which was first deposited onto a layer of oxide [2]. Both Kilby and Noyce shared

the patent right for the invention of the integrated circuit. In 2000, Kilby was awarded the Nobel Prize in Physics 'for his part in the invention of the integrated circuit'.

Since the advent of the semiconductor transistor and the demonstration on the workability of the integrated circuit chip about some 70 years ago, the electronic industries have been prospering hitherto. Electronic devices are now closely interwoven with human's life. They have, in many aspects, become indispensable to mankind. Indeed, one can easily find traces of electronic circuitries integrated into areas which intertwine seamlessly with the fabric of mankind's living hood. Some of these areas include transportation, telecommunication, security, medicine and entertainment, just to name a few.

3. Moore's law

In April 1965, one of the co-founders of Intel Corporation, Dr. Gordon Earle Moore, predicted that the number of components (i.e. any electronic components which include not just transistors but capacitors, resistors, inductors, diodes, etc. as well) in an integrated circuit would double every year [3]. Ten years later in 1975, he revised his prediction to a doubling of every 2 years. Moore's prediction, which is more commonly known as Moore's law nowadays, has been widely used in the semiconductor and microelectronic industries as a tool to predict the increase of components in a chip for the coming generations [4]. To date, Moore's law has been proven to have held valid for more than half a century. **Table 1** depicts the progressive trend of the integration level for the semiconductor industry. It can be observed from the table that the number of transistors that can be fabricated in a chip has been growing continuously over the years. In fact, this growth has complied closely with Moore's law. To distinguish the increase of transistors in every 10 years, each era is designated a name, that is, the SSI, MSI, LSI, VLSI, ULSI and SLSI eras. During the VLSI era, a microprocessor was fabricated for the first time into a single integrated circuit chip. Although this era has now long passed, the VLSI term is still being widely used today. This is partly due to the absence of an obvious qualitative leap between VLSI and its subsequent ULSI and SLSI eras, and partly, it is also because IC engineers and experts working in this field have been so used to this term that they decided to continue adopting it.

Integration level	Year	Number of transistors in a chip
Small-scale integration (SSI)	1950	Less than 100
Medium-scale integration (MSI)	1960	Between 100 and 1000
Large-scale integration (LSI)	1970	Between 1000 and 10,000
Very large-scale integration (VLSI)	1980	Between 10,000 and 100,000
Ultra large-scale Integration (ULSI)	1990	Between 100,000 and 10,000,000
Super large-scale integration (SLSI)	2000	More than 10,000,000

Table 1. Integration level of an integrated circuit chip.

4. The field effect transistors

Today, the transistors fabricated in an IC device are mostly metal oxide semiconductor field effect transistors (MOSFETs). The earliest paper describing the operation principle of a MOSFET can be traced back to that reported in Julius Edgar Lilienfeld's patent in 1933 [5]. In 1959, Dr. Dawon Kahng and Dr. Martin M. (John) Atalla at the Bell Telephone Laboratories successfully invented the MOSFET [6]. In 1963, two engineers from the Radio Corporation of America (RCA) Princeton laboratory, Dr. Steven R. Hofstein and Dr. Frederic P. Heiman, presented the theoretical description on the fundamental nature of the silicon planar MOSFET [7]. In the same year, Dr. Frank Marion Wanlass of Fairchild Semiconductor invented the first complementary metal oxide semiconductor (CMOS) logic circuit [8].

4.1. The MOSFET

The MOSFET is basically a device that operates like a switch or an amplifier in electronic circuits. **Figure 2** depicts the basic structure of the MOSFET. The device consists of four terminals, namely the drain (*D*), source (*S*), gate (*G*) and substrate or bulk (*B*) terminals. Basically, the device is composed of three layers—a poly-silicon layer (i.e. the gate terminal), an oxide layer (i.e. the gate oxide) and a single-crystal semiconductor layer (i.e. the substrate). In the early days, the gate terminal was made of aluminium. It is from these three layers of materials that the FET device derived its name. In mid 1970s, however, the gate material was replaced with polysilicon. The high-temperature stability of the polysilicon gate is used as a mask to form the self-aligned source and drain terminals via ion implantation, rendering higher accuracy for the formation of these two terminals. Although the gate today is no longer made of aluminium, the term MOSFET has been so widely accepted that it stays until today.

The operation principle of a MOSFET is actually quite simple. When a voltage is applied in between the drain and source terminals, a conducting channel is required to be formed between the two terminals to close the circuit (i.e. to allow current to flow). A voltage connected to the gate terminal acts like a switch. Given sufficient magnitude (and the correct

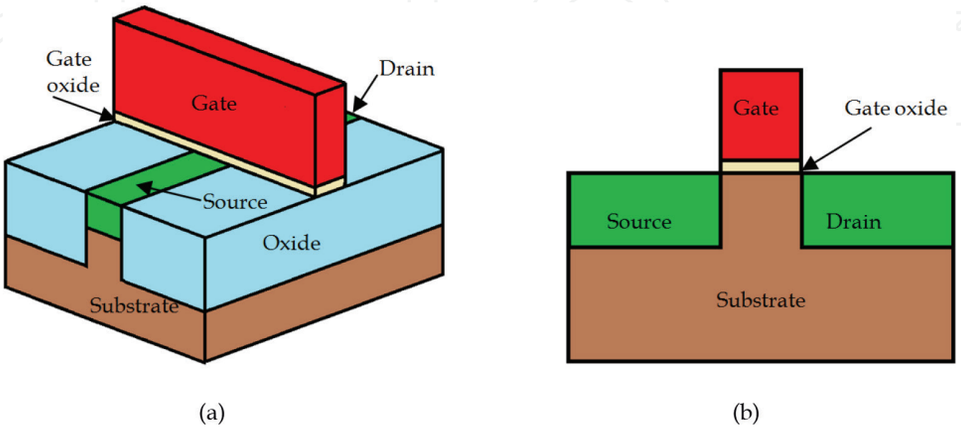

Figure 2. The (a) basic structure and (b) cross section of a MOSFET.

polarity), the gate voltage is able to attract carriers to the gate oxide-substrate interface, forming a channel which connects the source and drain terminals.

A MOSFET can be categorized into two types, depending on the dopants of the drain and source terminals, as well as the substrate. When both the drain and source terminals, in a p-type substrate, are heavily doped with donator ions (such as phosphorous or arsenic), a negative channel is to be formed in between them to conduct current. On the other hand, when both terminals, in an n-type substrate, are heavily doped with acceptor ions (such as boron), a positive channel is to be formed. The former device is therefore known as a negative-channel MOSFET or an NMOS transistor, while the latter is known as a positive-channel MOSFET or a PMOS transistor. **Figure 3** shows the circuit symbols of both PMOS and NMOS transistors.

The size of a MOSFET transistor is measured by the gate length, which is also commonly known as the feature size or feature length *L*. The feature size *L* has been shrinking tremendously over the years. Transistors with the size of 50 μm in the 1960s have been scaled down to less than 15 nm in 2017. The reduction of size allows a higher density of transistors to be fabricated in a single die. Overseen by the Taiwan Semiconductor Industry Association (TSIA), the United States Semiconductor Association (SIA), the European Semiconductor Industry Association (ESIA), the Japan Electronics and Information Technology Industries Association (JEITA) and the Korean Semiconductor Industry Association (KSIA), the International Technology Roadmap of Semiconductor (ITRS) is produced to forecast how the technology is expected to evolve. The purpose of the ITRS is to ensure healthy growth of the IC industries. **Table 2** lists the progressive reduction of the feature size published in ITRS 2.0 [9].

4.2. The FinFET

As the feature size reduces to the submicron regimes, fields at the source and drain regions may become comparatively high, and this may give certain adverse effects to the charge

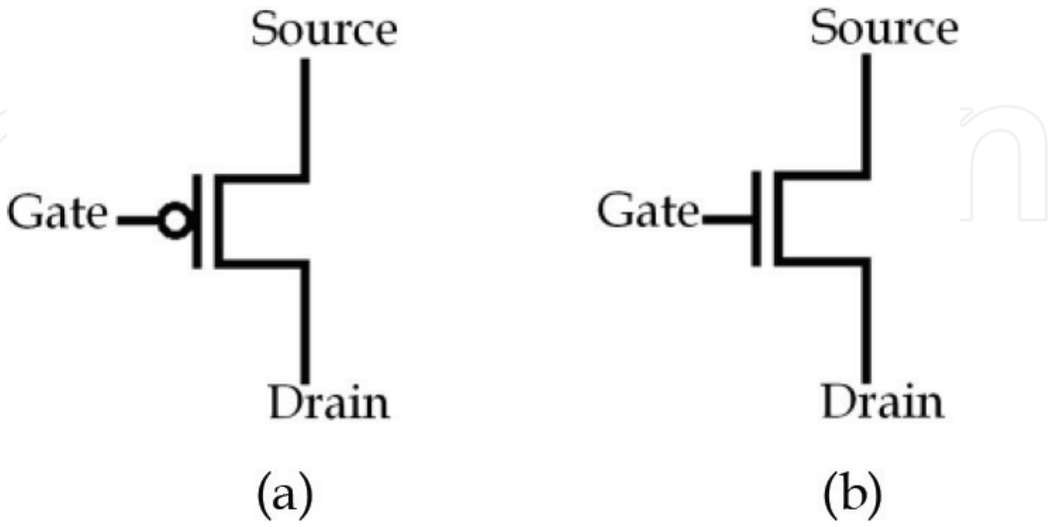

Figure 3. The symbol of (a) a PMOS transistor and (b) an NMOS transistor.

Physical gate length	Year						
	2015	2017	2019	2021	2024	2027	2030
High-performance logic (nm)	24	18	14	10	10	10	10
Low-performance logic (nm)	24	20	16	12	12	12	12

Table 2. Forecast of gate length by ITRS.

distribution. Some of the examples of these short-channel effects are the threshold voltage roll-off in the linear region, drain-induced barrier lowering (DIBL) and bulk punch-through [10]. To suppress these effects, additional steps, such as the introduction of retrograde well, lightly doped drain, halo implantation, and so on, have been introduced to the IC fabrication process [11]. As the device continues to shrink, however, curbing the short-channel effects turns out to be a strenuous task. When the feature size approaches the sub-nanometre range (i.e. 90 nm and below), static leakage current due to the short-channel effects has become a serious problem.

When the technology node reached 22 nm in 2011, Intel Corporation announced the fabrication of the tri-gate transistor, replacing the conventional planar MOSFET. More commonly known as the FinFET, this device has a three-dimensional transistor structure, as shown in **Figure 4**. From the figure, it is clear that a FinFET is named so because of the protruding source/drain terminals from its substrate surface, which closely resemble the fins of a fish. Since the gate wraps around the inversion layer, FinFETs provide higher current flow from source to drain. This feature also allows better control of the current flow—it reduces current leakage considerably when the device is at its 'off-state' and minimizes short-channel effects at its 'on-state'. Since the device has lower threshold voltage than the planar MOSFET, a FinFET can also operate at a lower voltage. In other words, the new device shows less leakage, faster switching and lower power consumption. However, certainly, the efficiency improvement

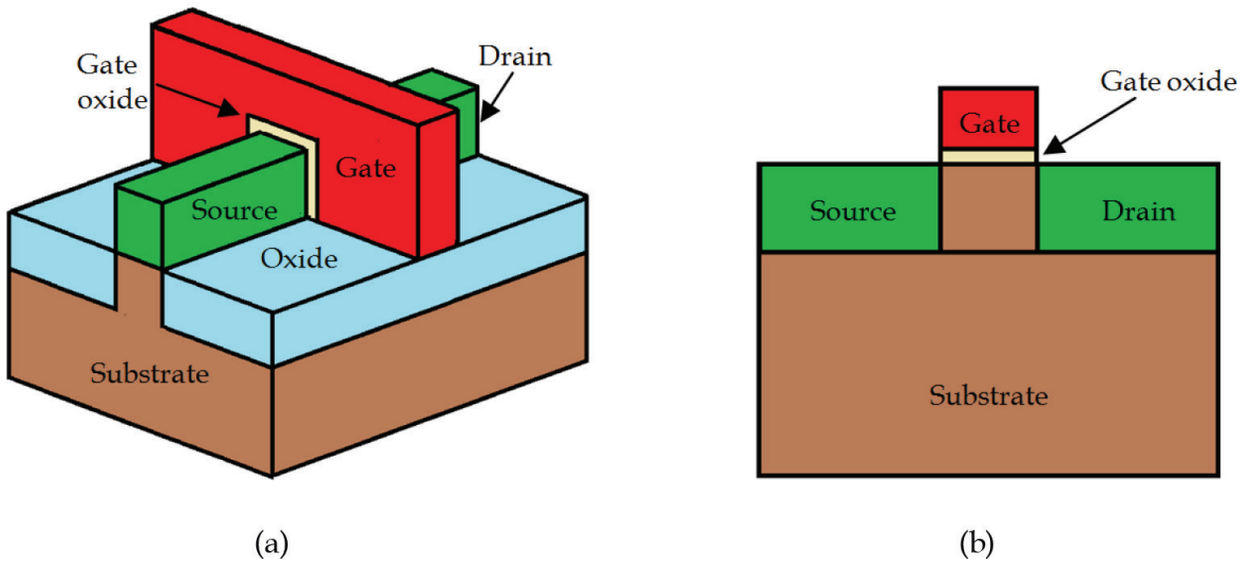

Figure 4. The (a) basic structure and (b) cross section of a FinFET.

found in the FinFET comes at the expense of increased fabrication complexity. The introduction of additional fabrication steps is inevitable in order to form the fin-like structure.

5. VLSI design flow

Generally, the design process of a VLSI chip involves three stages namely the (i) behavioural, (ii) logic circuit and (iii) layout representations. At each of this stage, verification is to be performed at the end before proceeding to the next. Hence, it is common to have repetitions and iterations in the processes [12].

5.1. Behavioural representation

Behavioural representation is the first step of the entire VLSI design flow. At this stage, it is important to specify the functionalities of the device and how it is going to communicate with the exterior. The design architecture is to be drawn panned out. A hardware description language (HDL) such as Verilog HDL or VHDL is used to define the behaviour of the device.

5.2. Logic circuit representation

After the HDL codes are successfully simulated, functional blocks from standard cell libraries are used to synthesize the behavioural representation of the design into logic circuit representation. Once the design is verified, the gate level netlist is generated. The netlist is necessary in order to develop the layout of the design.

5.3. Layout representation

At the final stage, the physical layout of the design is created. The process starts with floor planning which defines the core and routing areas of the chip. In order to optimize the design, the building blocks are arranged and orientated at their best locations. This process is known as placement. Once this is completed, a routing process is performed to interconnect the building blocks.

6. IC fabrication

To fabricate the chip, the layout is sent to a fab or a foundry. In a fab, a single-crystal semiconductor ingot is first grown. Wafers are then sliced from the ingot. The layout is printed onto the dice in each wafer. In the initial step of chip fabrication, the active regions or wells for the NMOS and PMOS transistors are first formed at the substrate. In order to separate the transistors, an oxide layer is subsequently deposited in between each neighbouring well. Transistors are then built at each active region. The primary processes to form a transistor include the growth of the gate oxide layer, the deposition of the poly-gate, and the doping of the source and drain regions. In the final fabrication step, the transistors are interconnected in accordance to the layout of the design. In a nutshell, the process of chip fabrication can be

broadly separated into four stages: (i) well formation, (ii) device isolation, (iii) transistor making and (iv) interconnection [13]. Although the walkthrough may appear straight forward, it is, in practical, complicated and laborious. To fabricate a VLSI chip, the die has to undergo repetitive thermal processes (such as oxidation, diffusion, annealing, etc.), lithography, ion implantation, etch, dielectric film deposition (such as chemical vapour deposition or CVD), chemical mechanical polishing (CMP) and metallization [13].

7. IC packaging

To protect the chip from harsh external environment (e.g. being exposed to UV light or moisture or being scratched), it is essential to encapsulate the chip in a package. The three most commonly used techniques for packaging are (i) wirebonding, (ii) flip-chip and (iii) tape-automated bonding (TAB) [4]. Once the chip is carefully packaged, it is then ready to be released to the market.

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References

[1] Arsov GL. Celebrating 65th anniversary of the transistor. Electronics. 2013;**17**:63-70. DOI: 10.7251/ELS1317063A

[2] Lukasiak L, Jakubowski A. History of semiconductors. Journal of Telecommunications and Information Technology. 2010;**1**:3-9. DOI: 10.1088/0031-9120/40/5/002

[3] Moore GE. Cramming more components onto integrated circuits. Electronics. 1965;**38**:14-117. DOI: 10.1109/N-SSC.2006.4785860

[4] Yeap KH. Fundamentals of Digital Integrated Circuit Design. 1st ed. Central Milton Keynes: Authorhouse; 2011

[5] Lilienfeld JA. Method and apparatus for controlling electric currents. U. S. Patent No. 1745175A (Filed October 8, 1926, issued January 28, 1930)

[6] Kahng D. Electric field controlled semiconductor device. U. S. Patent No. 3, 102, 230 (Filed 31 May 31, 1960, issued August 27, 1963)

[7] Hofstein S R, Heiman, FP. Silicon insulated-gate field-effect-transistor. Proceedings of IEEE. 1963;**51**:1190-1202

[8] Wanlass SM, Sah CT. Nanowatt logic using field-effect metal-oxide semiconductor triodes. In: Proceedings of the IEEE Conference on Solid-state Circuits Conference. Digest of Technical Papers; 1963; Philadelphia, PA, US. p. 32-33

[9] International Technology Roadmap for Semiconductors 2.0 [Internet]. 2015. Available from: https://www.semiconductors.org [Accessed: 3 April 2017]

[10] Sze SM. Semiconductor Devices: Physics and Technology. 2nd ed. New York, NY: John Wiley and Sons; 2002

[11] Ahmad I, Ho YK, Majlis BY. Fabrication and characterization of a 0.14 μm CMOS device using ATHENA and ATLAS simulators. International Scientific Journal of Semiconductor, Physics, Quantum Electronics, and Optoelectronics. 2006;**9**: 40-44. DOI: https://doi.org/10.15407/spqeo

[12] Kang S–M, Leblebici Y. CMOS Digital Integrated Circuits: Analysis and Design. Singapore: McGraw-Hill; 2005

[13] Xiao H. Introduction to Semiconductor Manufacturing Technology. Upper Saddle River, New Jersey: Prentice Hall; 2001

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