Chapter 6

Metal-Semiconductor Interfaces in Thin-Film Transistors

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Abstract

The metal-semiconductor interface in thin-film transistors (TFTs) is one of the bottlenecks on the development of these devices. Although this interface does not play an active role in the transistor operation, a low-quality interface can be responsible for a low performance operation. In a-Si TFTs, a doped film can be used to improve this interface, however, in other TFT technologies, there is no doped film to be used. In this chapter, some alternatives to improve this interface are analysed. Also, the influence of this interface on the electrical stability of these devices is presented.

Keywords: thin-film transistors, metal-semiconductor, contact resistance, short channel effects

1. Introduction

In all electronic devices, an electrical connection to the real world is necessary. In the case of thin-film transistors (TFTs), the quality of this electrical connection may be the difference in having high or low performance devices. The connection is made by source/drain electrodes in contact with the active layer. These metal-semiconductor interfaces have not played an active role in the transistor operation. However, a low-quality interface can be responsible for a low performance operation. Indeed, this research topic is one of the bottlenecks on the development of thin-film transistor technologies.

It is desirable to have the closest to an ideal metal-semiconductor interface or an ohmic contact with very low contact resistance; in other words, source/drain contacts with no barriers for the carrier flow in either positive or negative voltage polarization. Ideally, this occurs when metal and semiconductor work functions are of similar value and there are no interface states. However, having metal-semiconductor contacts without interface states is difficult and matching the semiconductor and metal work functions is nearly impossible. For these reasons, it is important to find alternatives to improve the metal-semiconductor interface in TFTs.

In metal-semiconductor interfaces, one may have several cases: ohmic contacts with low or high contact resistance and non-ohmic contacts with low or high contact resistance. Being this last, the most commonly obtained. The contact resistance can be extracted experimentally by the extrapolation of the width-normalized resistance (RW), obtained from the linear regime of the output characteristics I_{ds} vs. V_{ds}, for different channel lengths and gate voltages V_{gs}, as indicate in **Figure 1** [1, 2].

The problem associated with a high contact resistance is that it induces a potential drop at the drain/source contacts, affecting the electrical performance of the device [1–4]. On short channel TFTs, as the channel length is reduced, the source/drain contact resistance may be higher

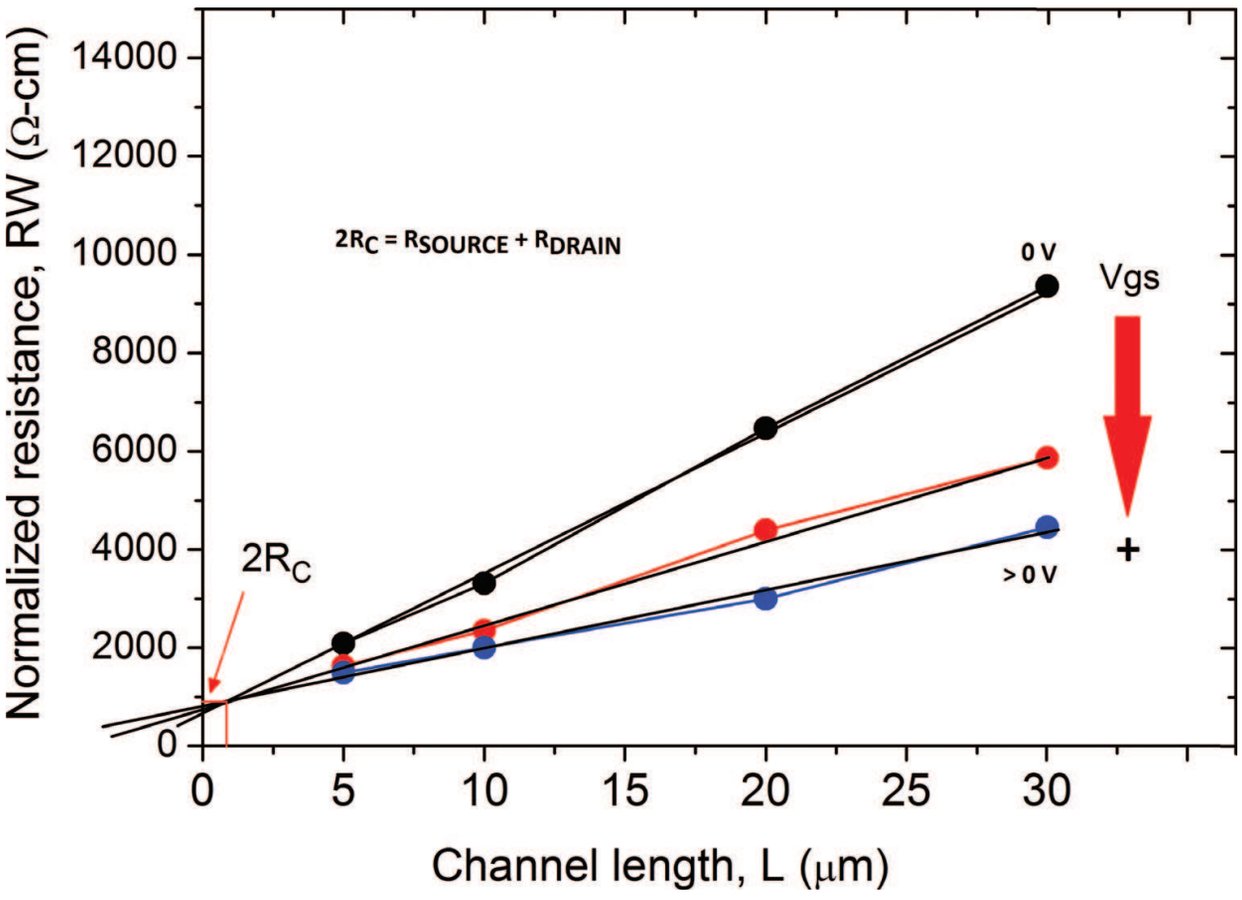

Figure 1. Width-normalized resistance (RW) (obtained from the linear regime of the output characteristics) for different channel lengths and gate voltages V_{gs}.

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than the channel resistance, as result the electrical behaviour may be governed by the contact resistance. This may induce several mechanisms: some of them reported the degradation of the transconductance, drop of carrier mobility, impact ionization, among others. Indeed, there is not a value of channel length to determine if short channel effects will be exhibited on the electrical characteristics of the TFT. Reported TFTs exhibited short channel effects at channel lengths *L* lower than 20 μm, meanwhile other TFTs (some with high contact resistance) did not exhibited short channel effects at *L* of 10 μm [1, 3–10]. Moreover, a TFT may exhibit high contact resistance effects at considered long channel values. These effects can be presented as superlinear behaviour or current crowding in output characteristics [1, 11, 12]. It is always desirable to have a low contact resistance; however, the channel resistance must be dominant.

2. Experimental section

The high quality SiO_2 film was obtained by spin-coating of SOG (SOG700B Filmtronics) diluted with deionized water and cured at 200°C. The a-SiGe:H active layer was deposited using low frequency (110 kHz) plasma-enhanced chemical vapor deposition (PECVD) at 200°C, pressure of 0.6 Torr and an RF power of 300 W. The a-SiGe:H films were deposited from SiH_4 and GeH_4 feed gases with H_2 dilution. The flow rate of SiH_4 (10% H_2) and H_2 was 45 sccm and 1000 sccm, respectively, and the GeH_4 (90% H_2) flow rate was 105 sccm. The n+ a-Ge:H film was deposited using low frequency PECVD at 200°C with a pressure of 0.6 Torr and RF power of 300 W, with a GeH_4 (90% H_2) flow of 250 sccm, H_2 flow of 3500 sccm and PH_3 (99% H_2) flow of 20 sccm. The aluminium was e-gun evaporated.

3. Alternatives for metal-semiconductor interface improvement

The requirements for getting a high-quality metal-semiconductor interface are complex. Typically, in field-effect transistors, a heavily doped interlayer or contact region film is used between the semiconductor and source/drain electrodes in order to improve the metal-semiconductor interface. However, in amorphous semiconductors, the doping efficiency drops at high doping levels. Moreover, in some TFT technologies, there are no doped interlayer films to improve the metal-semiconductor interface. These make even more complex to obtain a high-quality interface.

3.1. Doped regions for source/drain contacts

In the case of hydrogenated amorphous silicon (a-Si:H), Le Comber and Spear [13] reported that amorphous silicon prepared by plasma-enhanced chemical vapor deposition (PECVD) can effectively be doped by adding small amounts of phosphine (PH_3) or diborane (B_2H_6) to the silane (SiH_4) in the discharge gas. As expected, the conductivity increases at low doping levels. However, at higher doping levels, the conductivity decreases presumably due to the generation of defect states.

Figure 2 shows the contact resistance of a-Ge:H films at 200°C as function of the PH_3 flow. At low flow of PH_3 the contact resistance decreases, but at higher flow it increases. This behaviour agrees with the reported by Le Comber and Spear. Similarly, **Figure 3** shows the contact resistance of the p-type a-Ge:H film as a function of the B_2H_6 flow. At low flow of B_2H_6, the contact resistance increases but at higher flow it decreases and finally increases again. This behaviour also agrees with the reported by Le Comber and Spear. These interlayer films enhance the tunnelling of carriers through the metal-semiconductor interface, reducing the contact resistance and improving the interface. The n-type a-Ge:H film was successfully used as a contact region film in ambipolar a-SiGe:H TFTs [14].

3.2. Plasma processes to improve the contact resistance

In this section, the improvement of carrier mobility, on/off-current ratio and threshold voltage using hydrogen plasma at the active layer prior to define the source/drain contacts is presented. Firstly, an over-etching in the active layer before forming the source/drain contacts is performed. This over-etching closes the source/drain contacts to the induced channel layer, as indicate in **Figure 4**.

Figure 4a shows the structure of the TFT after the deposition of the gate electrode, gate insulator, active layer and passivation layer. Typically, after this step, the passivation layer is etched to form the source/drain contacts (**Figure 4b**). In this case, added to the etching of the passivation layer, an over-etching in the active layer is performed, as indicate in **Figure 4c**. Moreover,

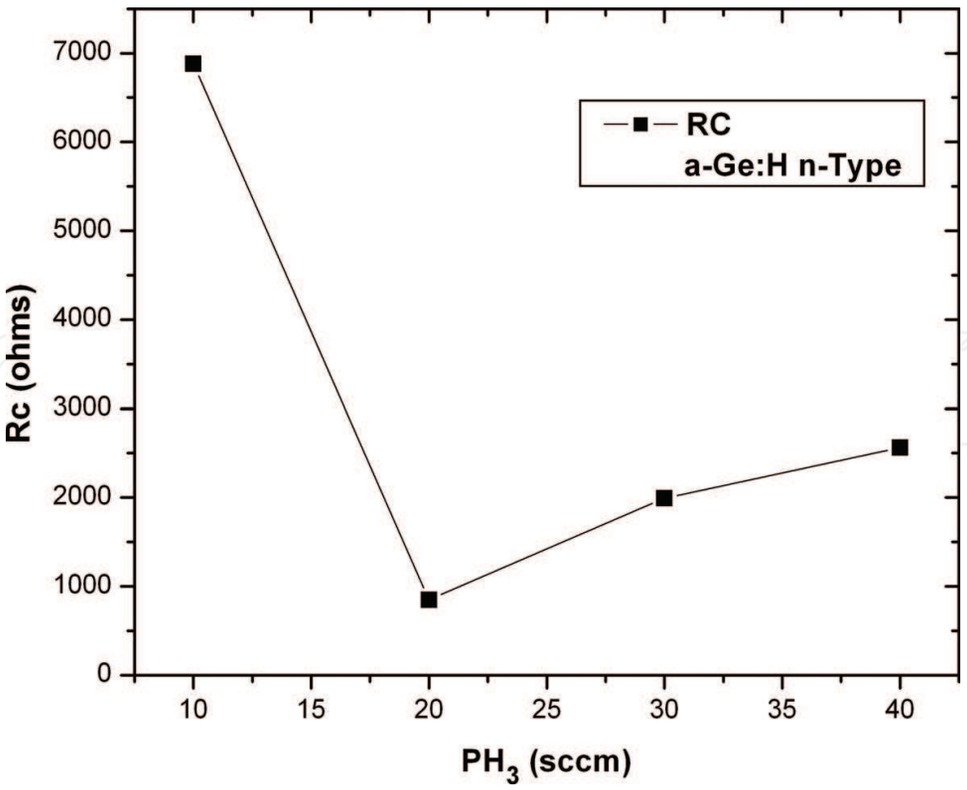

Figure 2. Contact resistance of the n-type a-Ge:H films as a function of the PH_3 flow.

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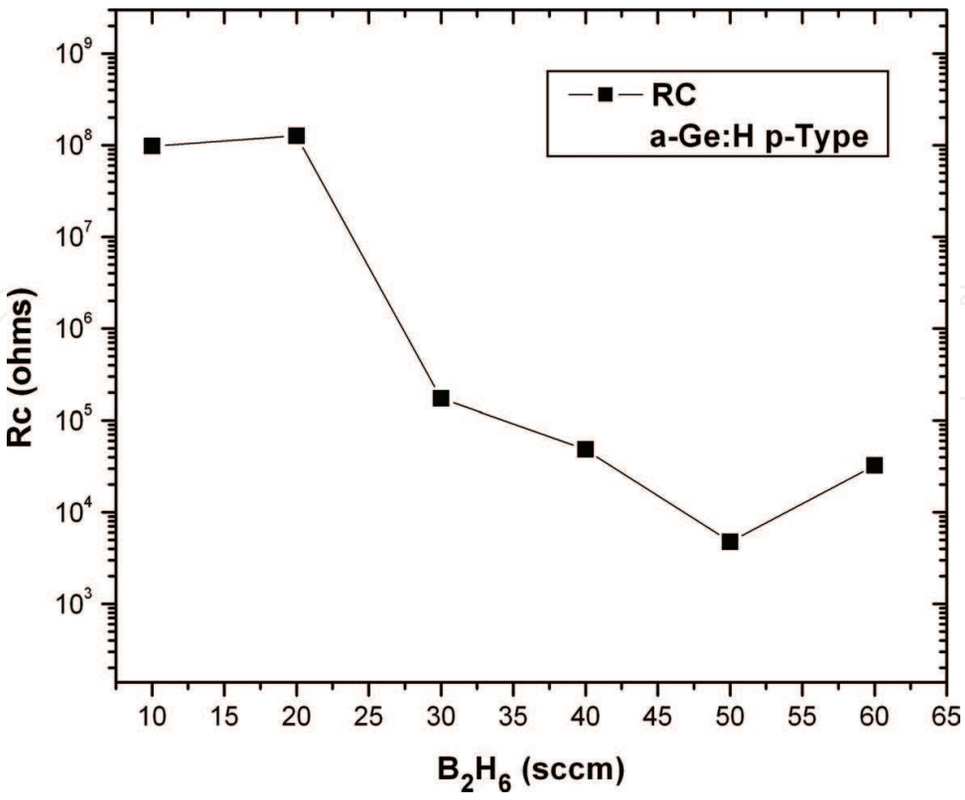

Figure 3. Contact resistance of the p-type a-Ge:H films as a function of the B_2H_6 flow.

a hydrogen plasma is applied [15]. For comparison, a set of devices without hydrogen plasma was fabricated. Finally, the source/drain contacts are formed (**Figure 4d**).

Figure 5 shows the transfer characteristics of the TFTs with and without hydrogen plasma. The TFTs with applied hydrogen plasma exhibit an on/off-current ratio approximately of 10^6 and an off-current approximately of 300 fA at 0 V_{gs}. While the TFTs without hydrogen plasma exhibit an on/off-current ratio of 10^3 and off-current of 20 pA. The subthreshold slopes values for both TFTs with and without hydrogen plasma were 0.56 and 0.61 V/DEC, respectively. The slopes are very similar. Typically, in TFTs, the subthreshold slope is largely decided by the quality of gate insulator-active layer interface. The subthreshold slope is dependent on the trap density in the active layer (N_T) and at the interface (D_{it}). The subthreshold slope can be approximated as the following equation [15]:

$$S = qK_B T\left(N_T ts + D_{it}\right)/C_{ox} \log(e) \quad (1)$$

where q is the electron charge, K_B is the Boltzmann constant, T is the absolute temperature, ts is the active layer thickness and C_{ox} is the gate insulator capacitance per unit area. If N_T or D_{it} is separately set to zero, the respective maximum values of N_T and D_{it} are obtained. The N_T and D_{it} values were of 2.65×10^{17} cm^{-3}/eV and 2.65×10^{12} cm^{-2}/eV, respectively, for TFTs with applied hydrogen plasma. For TFTs without hydrogen plasma, the values were of 2.88×10^{17} cm^{-3}/eV and 2.88×10^{12} cm^{-2}/eV, respectively. Since both TFTs have identical insulator-semiconductor interface and the over-etching process only affects the source/drain regions, we do not expect any difference in the quality of the insulator-semiconductor interface of the devices.

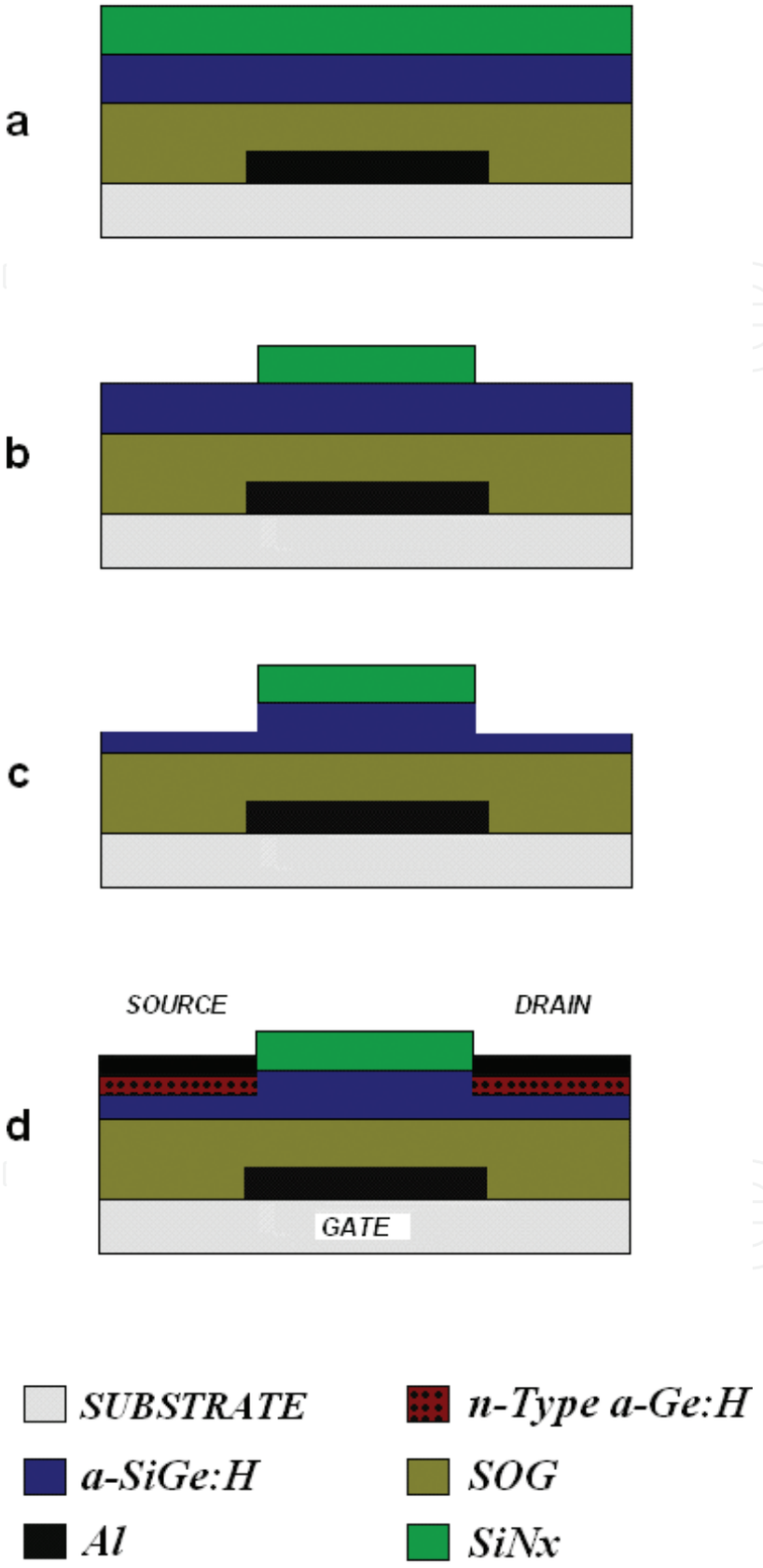

Figure 4. Process flow and cross-section of the TFT with over-etching at source/drain regions. (See text for description).

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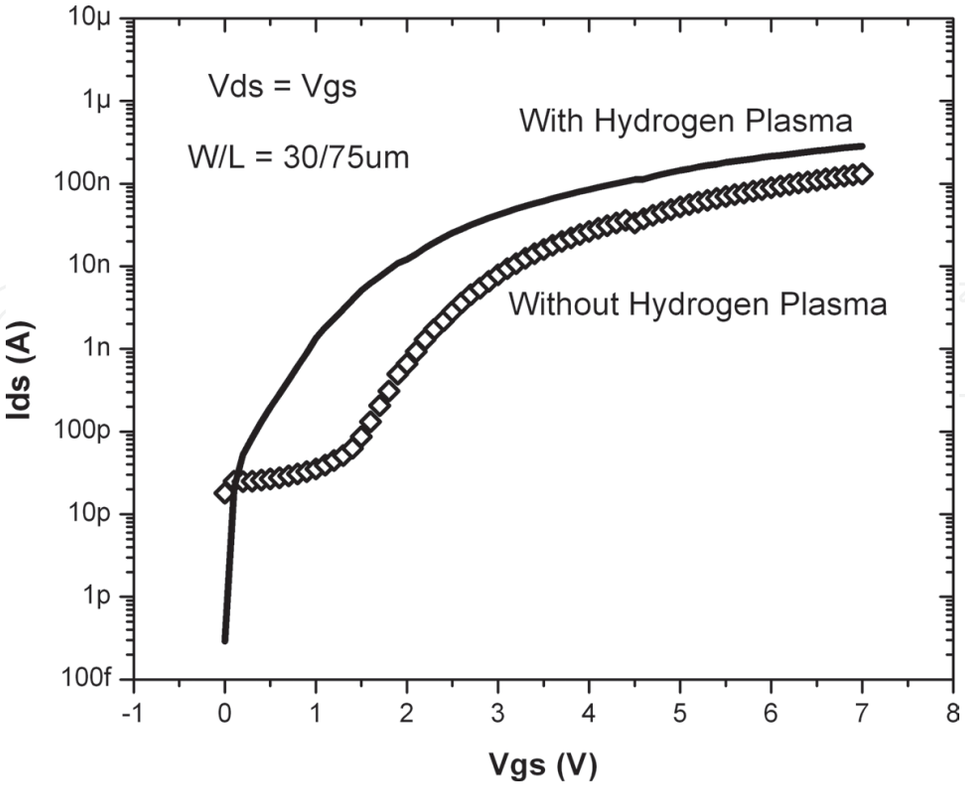

Figure 5. Transfer characteristics of the TFTs with and without hydrogen plasma.

On the other hand, **Figure 6** shows the square root of I_{ds} vs. V_{gs} of the TFT at a saturation regime. The threshold voltage and field-effect mobility can be extracted from the intercept with V_{gs} axis and slope, using Eq. (2).

$$I_{ds} = \mu_{FE} C_{ox}(W/2L)(V_{gs} - V_T)^2 \quad (2)$$

where μ_{FE} is the field-effect mobility, C_{ox} is the capacitance per unit area of the gate insulator, W and L are the channel width and the length, respectively, and V_T is the threshold voltage. The extracted threshold voltage and field-effect mobility were of 0.8 and 0.85 cm^2/Vs, respectively, for TFTs with hydrogen plasma. While 1.86 and 0.52 cm^2/Vs were extracted for TFTs without hydrogen plasma.

It is well known that hydrogen saturates dangling bonds in amorphous films [16]. Thus, the hydrogen plasma reduces the plasma-induced damage in the source/drain regions of the active layer, and as result the contact resistance of the TFT is improved. This can be corroborated with the higher values of carrier mobility and on-current.

Figures 7 and **8** show the output characteristics of the TFTs with and without hydrogen plasma. The output characteristics of TFTs without hydrogen plasma exhibit a high contact resistance that appears in the form of current crowding, in the bias range of 0–1V of V_{ds}. Also, the driving current capability is higher for TFTs with hydrogen plasma, as indicated by their values of I_{ds}. These results confirm the hydrogen plasma reduces the plasma-induced damage and improve the metal-semiconductor interface. These processes in the source/drain regions lead to form good ohmic contacts.

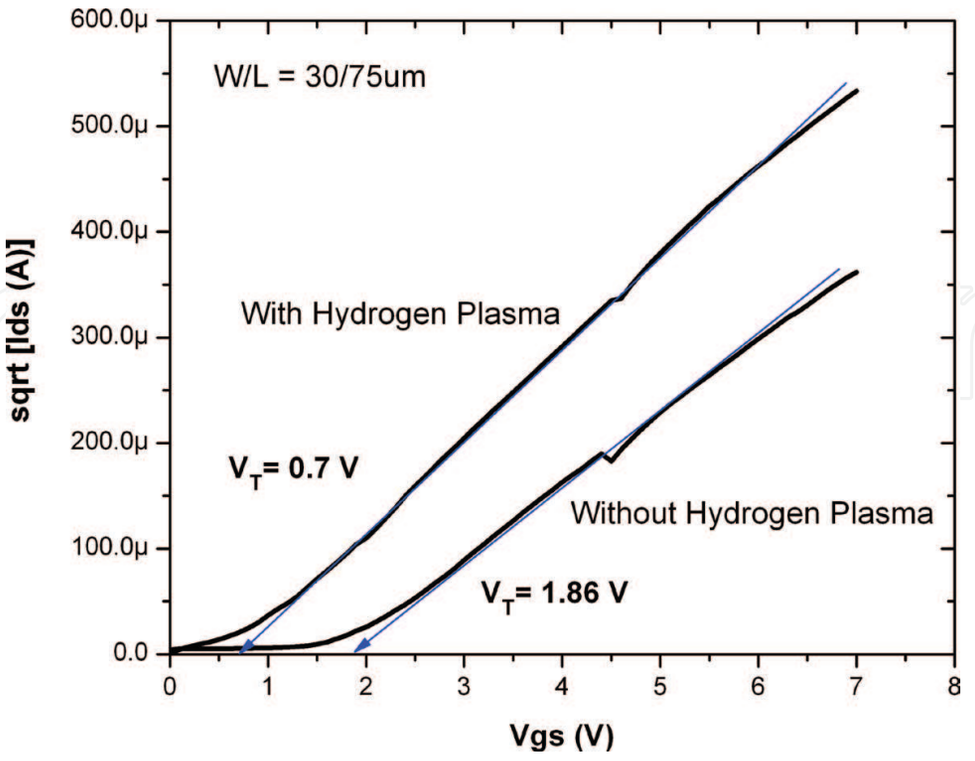

Figure 6. Square root of I_{ds} vs. V_{gs} of the TFT at saturation regime.

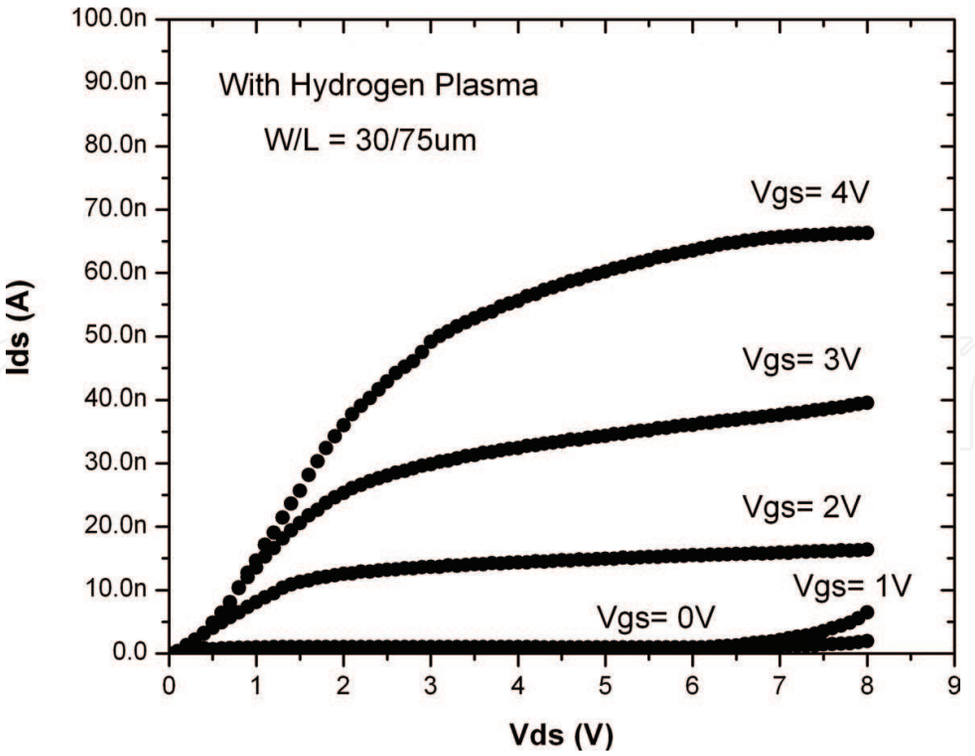

Figure 7. Output characteristics of TFTs with over-etching and hydrogen plasma.

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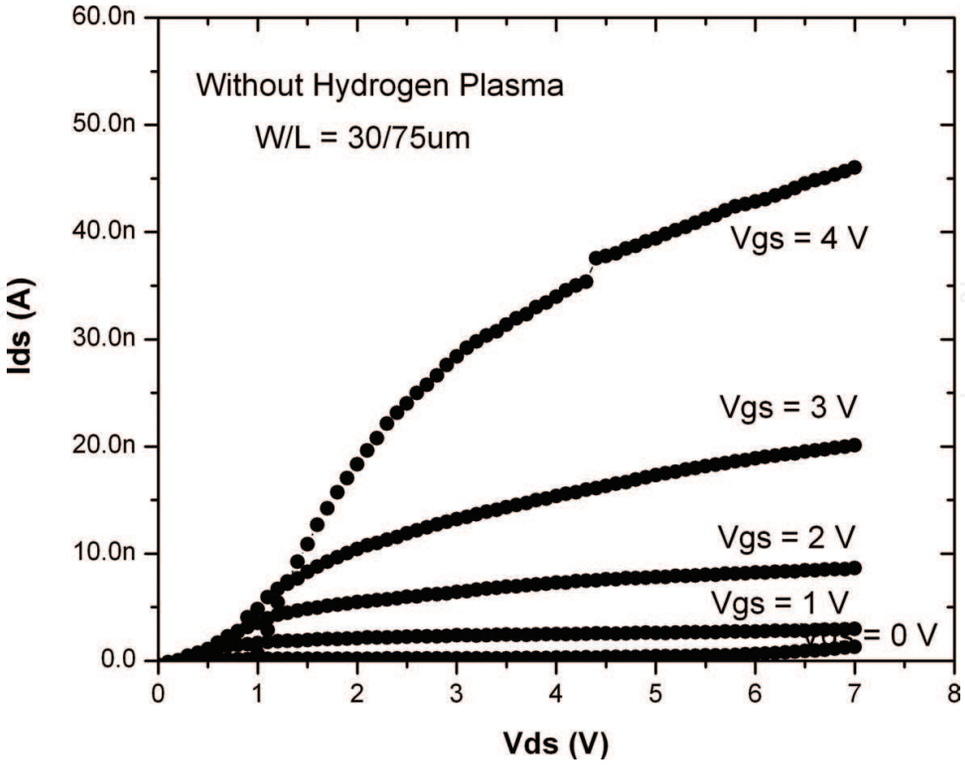

Figure 8. Output characteristics of TFTs with over-etching but without hydrogen plasma.

3.3. Planarization of the gate electrode in bottom-gate TFTs

Thin-film transistors are successfully employed in active-matrix displays [17]. In this application, the inverted staggered structure is the most used [17]. In an inverted structure, the gate electrode is placed at the bottom of the structure (bottom-gate structure). The advantage of using this inverted structure is that the gate electrode protects the active layer from backplane light. The problem is when the active-matrix displays become larger, the number of address lines must increase and the gate lines must be narrower and longer. To avoid an increase in the resistance of the gate line, which results in delay on the display performance, the gate line must be thicker. Then, the problem with this thicker gate is that the gate insulator tends to be thinner around the corners of the gate, increasing the leakage current and electric stress due to the high electric field at the corner [18]. In order to reduce these effects, the planarization of the gate electrode was proposed by other groups [19, 20].

As far as we know, the only work related to the study of the planarization of the gate electrode is conducted by Chen et al. [18]. They reported a reduction in the contact resistance attributed to the planarization process. However, this improvement in the contact resistance is difficult to understand, since the planarization of the gate electrode improves the insulator-semiconductor interface but not the metal-semiconductor interface. Firstly, the experimental characteristics of planarized and unplanarized TFTs are presented. After that using a physically based simulator (SILVACO), the main interfaces are analysed to understand the origin of this improvement.

The experimental transfer characteristics of unplanarized and planarized TFTs are shown in **Figure 9**. The planarized TFT shows a subthreshold slope ~0.45 V/DEC and ~0.49 V/DEC, for n-type and p-type regions, respectively, while on/off-current ratios around 10^5 were obtained for n-type and p-type regions. On the other hand, the unplanarized TFT shows a subthreshold slope ~1 V/DEC for an n-type region and 1.3 V/DEC for a p-type region, on/off-current ratios ~10^4 and 10^3 for n-type and p-type regions, respectively.

The threshold voltage and field-effect mobility were extracted from the transfer characteristics operating in the saturation regime ($V_{ds} = V_{gs}$), using Eq. (2). For planarized TFTs, the threshold voltage was 1.11 and −2.18 V for n-type and p-type regions, respectively. The extracted field-effect mobilities were 0.68 and 0.15 cm^2/Vs for n-type and p-type regions, respectively. For unplanarized TFTs, the threshold voltage was 2.4 and −3.35 V for n-type and p-type regions, respectively. The extracted field-effect mobilities were 0.11 cm^2/Vs for an n-type region and 0.02 cm^2/Vs for a p-type region.

Figure 10 shows the output characteristics for planarized and unplanarized TFTs. It is important to mention that the output characteristics show an ambipolar behaviour. A detailed discussion and modelling can be found in Ref. [14]. In the output characteristics of unplanarized TFTs, current crowding appears in the bias range from 0 to 1 V of V_{ds}. This high contact resistance effect slightly appears in planarized TFTs. To corroborate this effect, the contact resistance was extracted from the n-type region of both planarized and unplanarized TFTs. The contact resistance was extracted by the extrapolation of the width-normalized contact resistance as indicated in **Figure 1**. The contact resistance was approximately 1413 Ωcm for

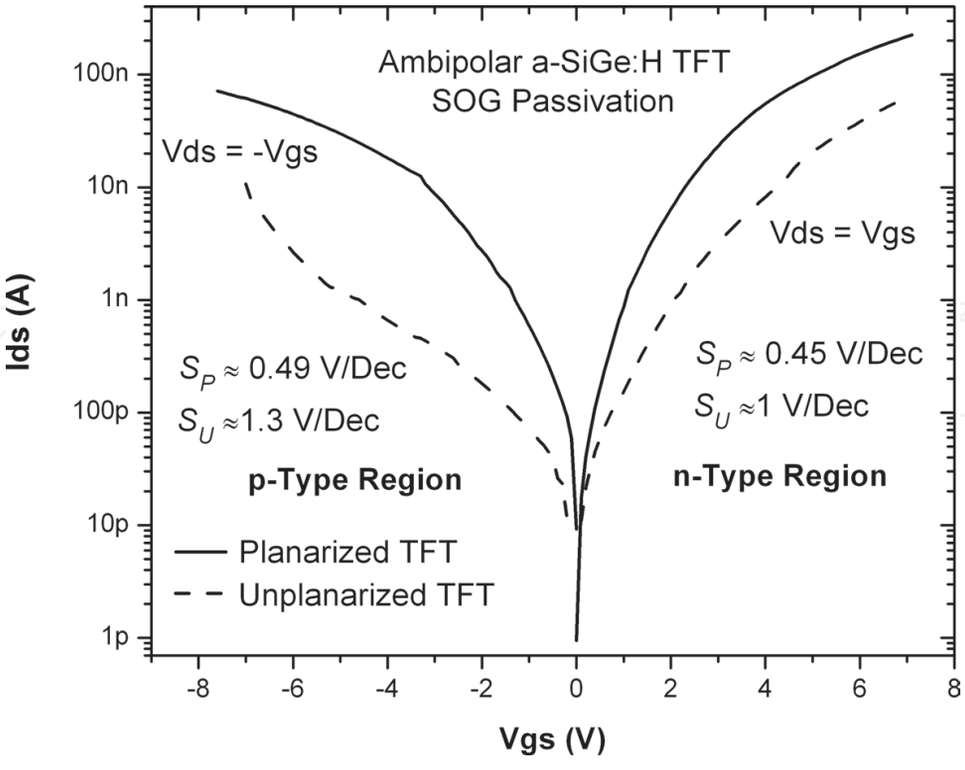

Figure 9. Transfer characteristics of unplanarized and planarized TFTs.

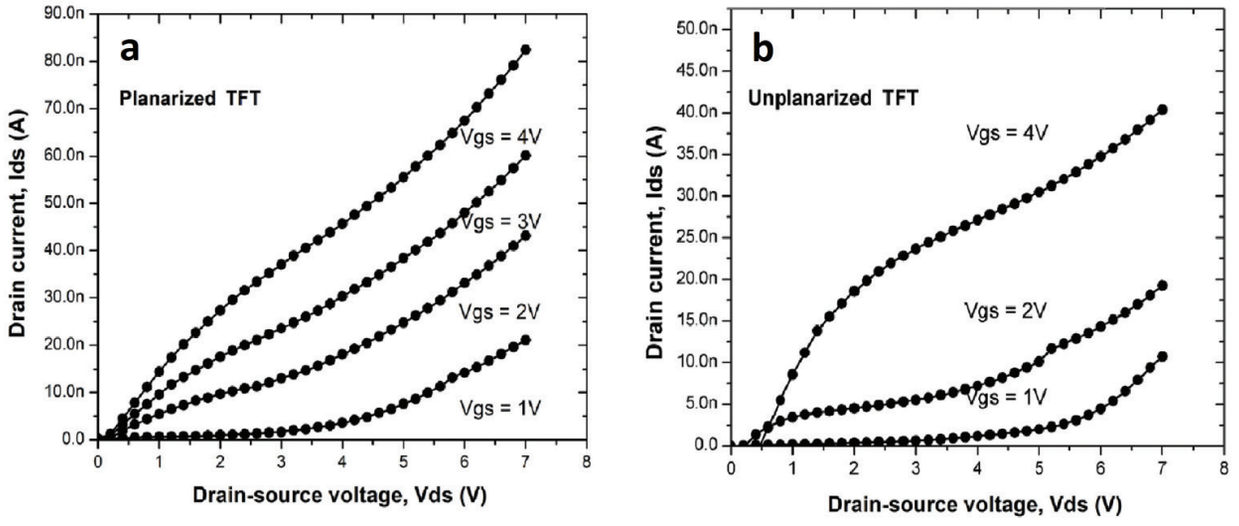

Figure 10. Output characteristics for planarized and unplanarized TFTs. a) Planarized and b) Unplanarized.

unplanarized TFTs and 589 Ωcm for planarized TFTs. This agrees with the higher values of drain current in planarized TFTs. It is important to note that subthreshold slope is improved in planarized TFTs. Some authors suggest a better injection of carriers from the source electrode into the active layer [21]. Also, other authors have reported a better subthreshold slope after improving the contact resistance [22, 23].

The experimental results agree with the reported previously by Chen et al. However, the improvement in contact resistance by the planarization process is unexplained. Using ATHENA, both planarized and unplanarized structures were simulated. Then, using ATLAS, electrical measurements were simulated. The cutline tool within the ATLAS simulator generates one-dimensional profiles from the insulator-semiconductor and metal-semiconductor interfaces. Ideal contacts were considered for source/drain contacts in both unplanarized and planarized simulated TFTs (ohmic contacts without contact resistance).

Figure 11 shows a comparison of the cross-section of planarized and unplanarized TFTs simulated by ATHENA. Applying a positive gate bias of 5 V, the electric field of the planarized and unplanarized gate electrodes was extracted by ATLAS (**Figure 12**). As expected, for the planarized TFT, the electric field is uniform through the insulator-semiconductor interface. However, for the unplanarized TFT, the electric field is not uniform through the insulator-semiconductor interface. There is an increase of the electric field due to the thinner gate insulator. This increase in the electric field causes an accumulation of electrons in the channel close to the corners of the gate, as shows **Figure 13**.

The difference of the electron concentration in the channel works as a scattering mechanism, limiting the mobility of the carriers. This can explain the lower extracted field-effect mobility in the unplanarized TFTs. Also, the variations of the electron concentration reflect an increase in the conduction band energy of the active layer close to the source/drain contacts, as show in **Figure 14**. This increase in energy acts as a barrier for the electrons, where only electrons with higher energy can pass the barrier. As result, the device contact resistance apparently

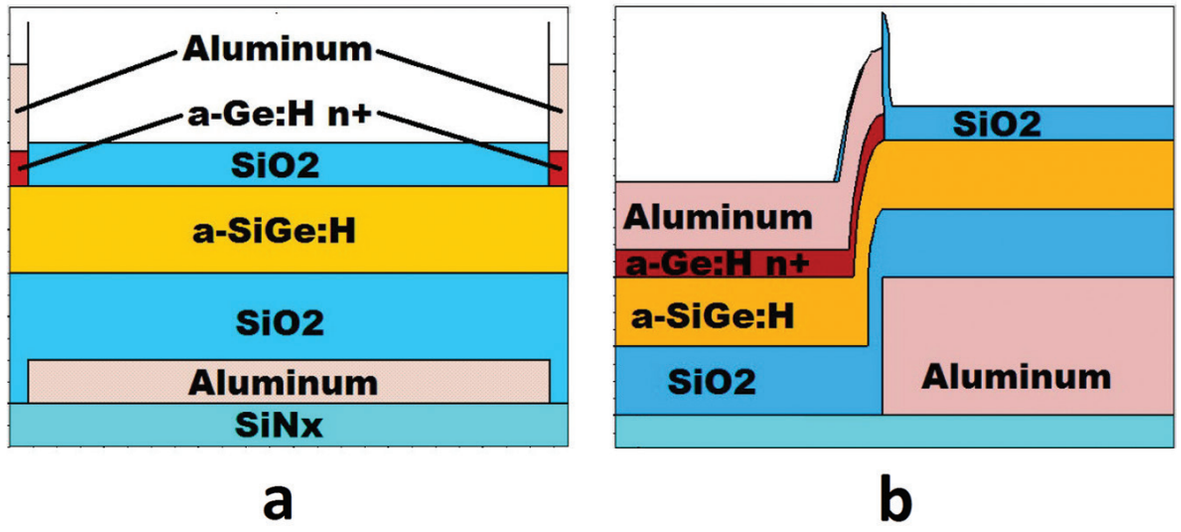

Figure 11. Cross-section of planarized and unplanarized TFTs simulated by ATHENA. a) Planarized and b) Unplanarized.

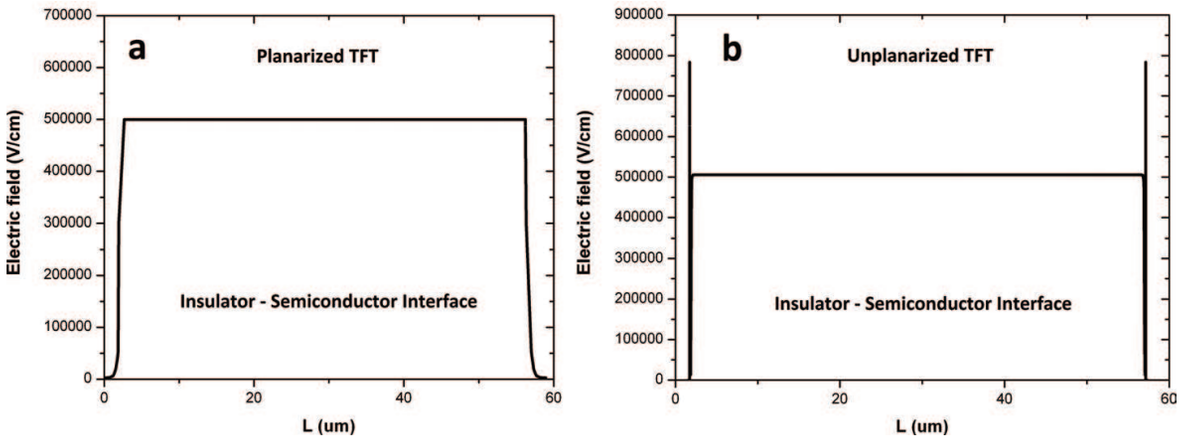

Figure 12. Electric field of the planarized and unplanarized TFTs simulated by ATLAS. a) Planarized and b) Unplanarized.

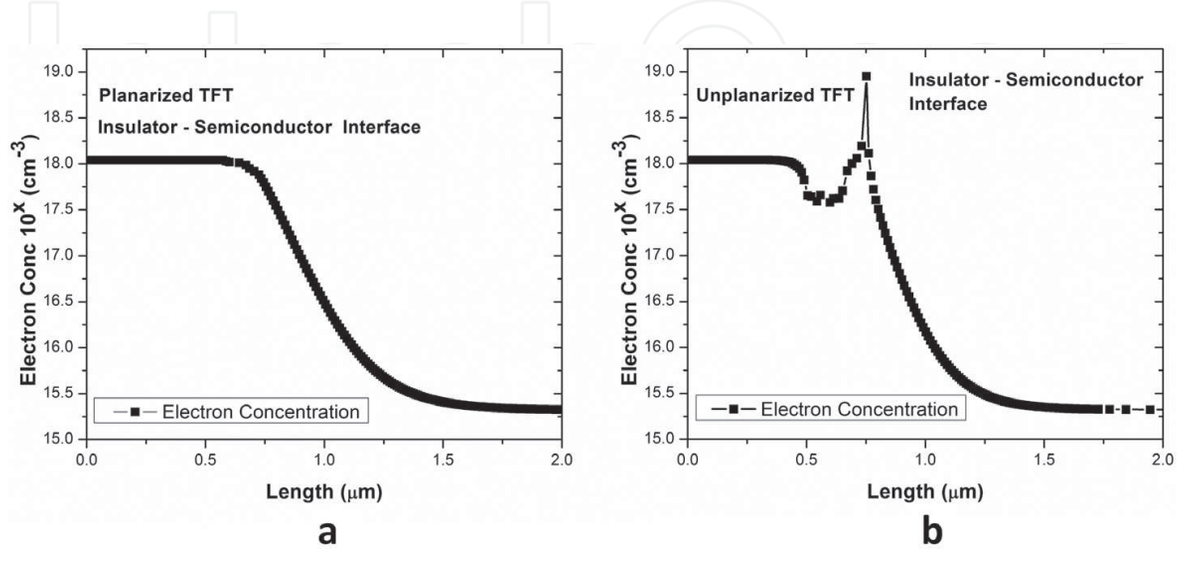

Figure 13. Accumulation of electrons in the channel close to the corners of the gate simulated by ATLAS. a) Planarized and b) Unplanarized.

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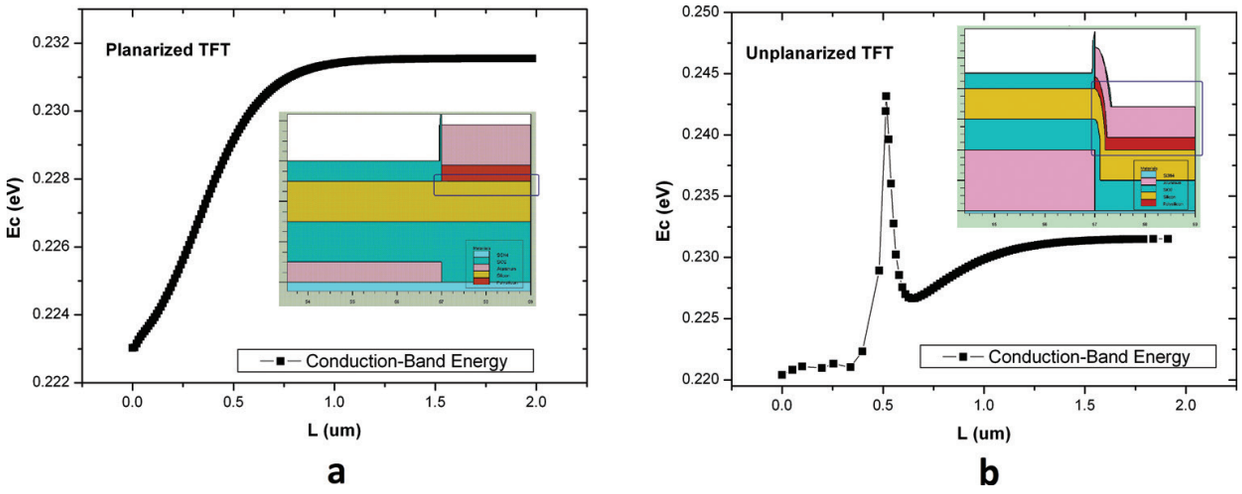

Figure 14. Conduction band energy of the active layer close to the source/drain contacts. a) Planarized and b) Unplanarized.

increases. To corroborate these assumptions, **Figure 15** shows the simulated output characteristics of both planarized and unplanarized TFTs. The simulation agrees with the behaviour exhibited in the experimental and simulated results.

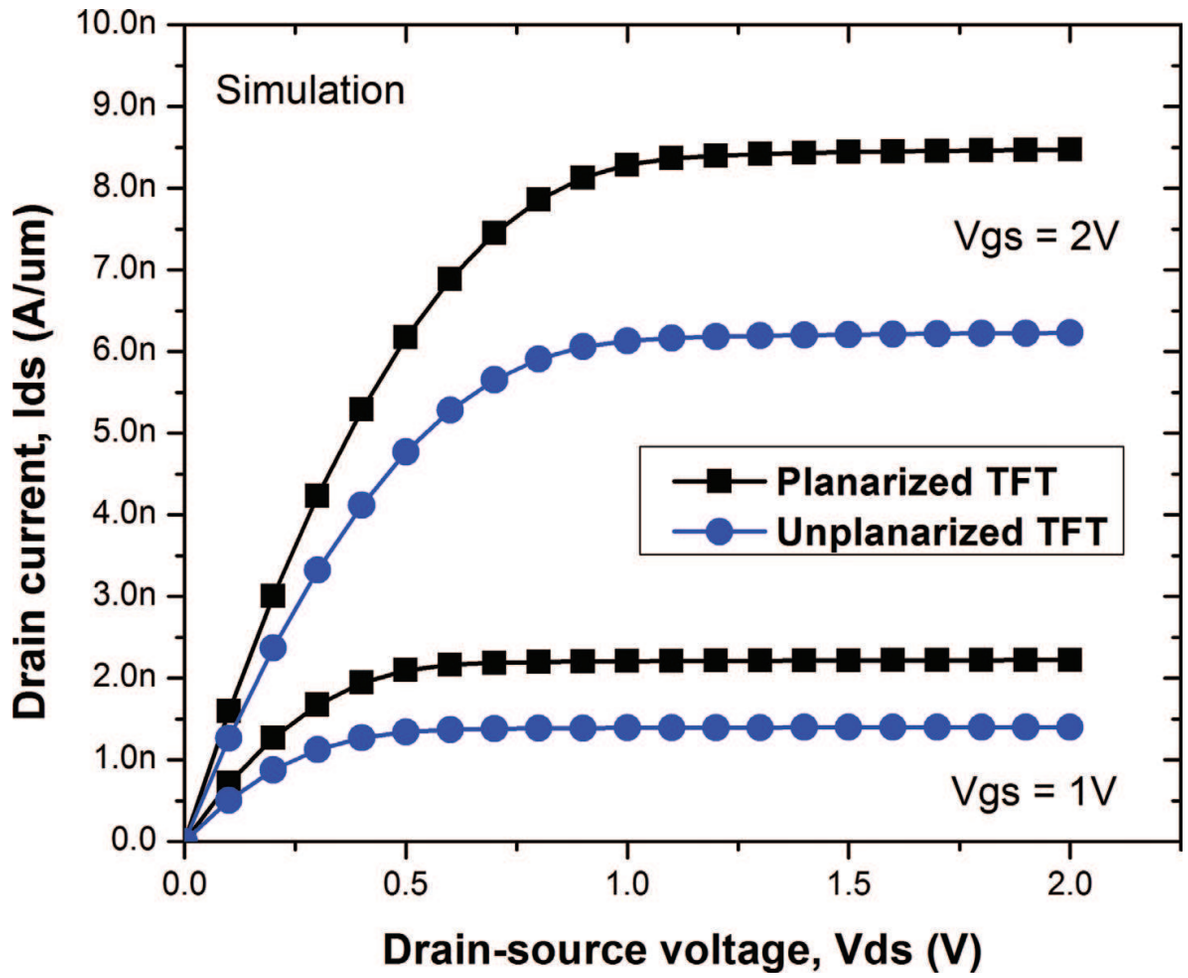

Figure 15. Simulated output characteristics of planarized and unplanarized TFTs.

4. Influence of metal-semiconductor interface on electrical stability of TFTs

Despite the high potential of TFTs to enable low-cost electronics, these devices have the disadvantage of threshold voltage shift after a prolonged application of gate bias stress. In a-Si TFTs, the threshold voltage shift mechanisms have been studied to estimate the long-term behaviour of TFT circuits. Because of the continuous growing application of novel material-based TFTs in electronics, an updated research for threshold voltage shift mechanisms is needed. The defect state creation in active layer and charge trapping in the gate dielectric is presumably the mechanisms responsible for the threshold voltage shift in TFTs. During the application of gate bias stress (or during normal operation), the charge trapping and defect state creation mechanisms occur simultaneously; therefore, the experimental results of threshold voltage shift do not provide any information about the quantitative effect of each of these mechanisms on the threshold voltage shift of the TFT. In addition, it has been proposed the relaxation of the threshold voltage after the annealing of the defect states in the active layer and the charge back tunnelling of trapped electrons inside the gate insulator [24–26]. However, the experimental published results for the relaxation of threshold voltage do not support the defect state annealing mechanism. While the estimations of charge trapping and de-trapping from gate insulator traps show a good agreement with the experimental threshold voltage relaxation. Therefore, from the threshold voltage shift mechanisms, charge trapping in the gate insulator is reversible [26–30].

On the other hand, the proposed mechanisms responsible for threshold voltage shift are directly related to the insulator-semiconductor interface. However, it has been also reported that quality of the metal-semiconductor interface strongly influences the kinetics of threshold voltage shift and relaxation of TFTs [31]. Based on the results reported for the charge trapping and defect state creation mechanisms of threshold voltage shift, a general conclusion cannot be drawn. The kinetics of the mechanisms strongly depends on the fabrication process of the TFTs. It is important to consider that deposition conditions of the active layer also affect the rate of the creation of the extra defect states in the active layer.

In this section, a comparison of the threshold voltage shift in TFTs with the same insulator-semiconductor interface but different metal-semiconductor interface is presented. The threshold voltage shift is calculated as a function of the stress time at gate bias stress of 20 V and V_{ds} = 0 V. These are the typical conditions for electrical stress in TFTs [32–36]. The complete fabrication procedure of the TFTs can be found elsewhere [14]. The gate insulator was deposited in two sets of devices using the same deposition conditions. After that the fabrication of the metal-semiconductor interface was different. In one set of devices, it was employed the over-etching and plasma processes described in Section 2.2. As passivation layer a silicon nitride film was used. On the other set of devices, the active layer and n+ contact region films were continuously deposited with no vacuum break in the chamber. As passivation layer a silicon oxide film was used. The schematic cross-section of the fabricated devices is shown in **Figure 16**.

Table 1 summarises the parameters extracted in both TFTs. Since both TFTs have identical insulator-semiconductor interface, the slight difference in values of subthreshold slope is

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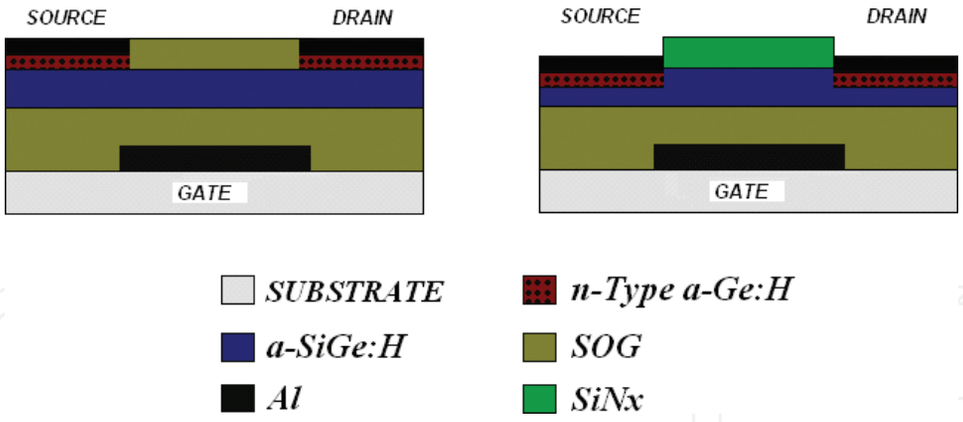

Figure 16. Schematic cross-section of the fabricated devices.

Parameter	TFT SiNx passivation (hydrogen plasma)	TFT SiO_2 passivation
SS	0.56 V/DEC	0.45 V/DEC
On/off-current ratio	10^6	$>10^5$
ΔV_T (6000 sec)	2.25 V	1.14 V
Field-effect mobility	0.85 cm^2/Vs	0.68 cm^2/Vs
Off-current	~0.3 pA	~0.95 pA

Table 1. Comparison of the parameters of the TFTs.

considered just statistical fluctuation. The values of off-current are of the same order of magnitude. The on/off-current ratio is very similar for both TFTs. However, an important difference in field-effect mobility is found. The mobility for TFTs using SiNx as a passivation layer (hydrogen plasma) was 0.85 cm^2/Vs, higher than the 0.68 cm^2/Vs for TFTs using SiO_2 passivation. This result is related to the metal-semiconductor interface, the higher value of mobility may indicate a lower contact resistance.

Figure 17 shows the threshold voltage shift ΔV_T as a function of the stress time. The figure shows a higher shift for TFTs using SiN*x* passivation. It is important to mention that the observed threshold voltage shift for both TFTs could not be recovered after a rest period of 48 hours and under the application of negative gate bias, suggesting that the shift is irreversible. Since the charge trapping in the gate insulator is reversible, therefore, under the applied gate bias conditions, the shift in the threshold voltage seems to be due to creation of defect states in the active layer.

The higher value of mobility results of a lower contact resistance, however, the higher instability of this TFT related to defect state creation suggests a dependency with the fabrication of the metal-semiconductor interface. Probably due to defects induced by the over-etching process. Also, the SiN*x* passivation layer may has influence on the electrical instability of the TFT. Further research is necessary to address these assumptions. Although both TFTs

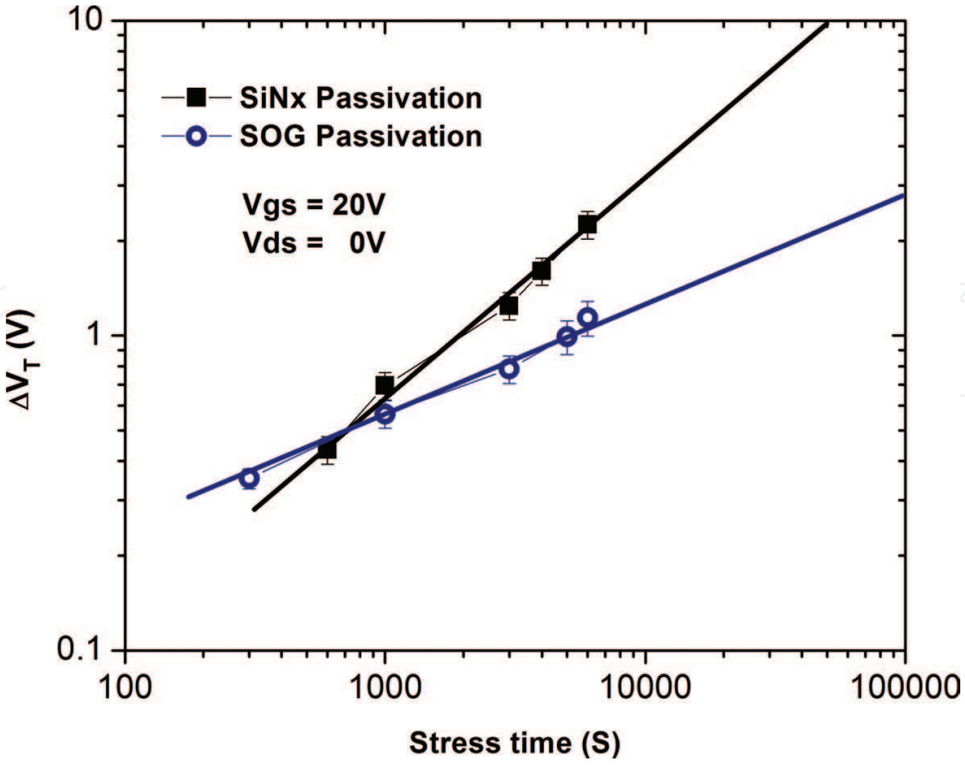

Figure 17. Threshold voltage shift ΔV_T as function of the stress time.

have the same insulator-semiconductor interface, the metal-semiconductor interface plays an important role in the electrical stability of these devices. The research of the kinetics of the mechanisms responsible for the instability on TFTs needs to be extensively explored for emergent TFT technologies.

5. Conclusions

In summary, some alternatives to improve the metal-semiconductor interface are analysed. An over-etching at the source/drain regions of the active layer can improve the TFT electrical performance, since this process gets close the n+ contact layer and the electron induced-channel. Moreover, the plasma-induced damage by the over-etching process is reduced after the application of a hydrogen plasma. On the other hand, the planarized TFTs exhibit better performance due mainly to the improved contact resistance. The simulations show an increase in the conduction band energy in the a-SiGe:H film at the metal-semiconductor interface. This increase acts as a barrier for the electrons, which results in an apparent increase of contact resistance. Finally, the influence of the metal-semiconductor interface in the electrical stability of TFTs is presented. Although the compared TFTs present the same insulator-semiconductor interface, the fabrication of the metal-semiconductor interface plays an important role in the electrical stability of these devices.

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