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Advanced SiC/Oxide Interface Passivation

Yogesh Kumar Sharma

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Abstract

To save energy on an electric power grid, the idea of redesigned 'micro-grids' has been proposed. Implementation of this concept needs power devices that can operate at higher switching speeds and block voltages of up to 20 kV. Out of SiC and GaN wide band gap semiconductors, the former is more suitable for low- as well as high-voltage ranges. SiC exists in different polytypes 3C-, 4H- and 6H-. 4H-SiC due to its wider band gap, 3.26 eV has higher critical electric field of breakdown (E_c) and electron bulk mobility compared to 6H-SiC. Even with all these benefits 4H-SiC full potential has not yet been realized. This is due to high trap densities (D_{it}) at the interface. In addition to 4H-polytype, in recent years, there is a reignited interest on cubic silicon carbide (3C-SiC), which can be potentially grown heteroepitaxially on 12″ Si substrates, as it would result in a drastic cost reduction of semiconductor devices compared to the successful but exorbitantly expensive SiC hexagonal polytype technology (4H-SiC). In this chapter, we discuss and summarize all different interface passivation techniques or processes that have led to a vast improvement of these (4H- or 3C-SiC/SiO_2) interfaces electrically.

Keywords: silicon carbide, MOSFET, interface trap density, mobility, PSG, nitrogen plasma, NO passivation, BTS

1. Introduction

1.1. Progress in semiconductor devices

The first solid-state amplifier was manufactured by using germanium (Ge) which was seen as the semiconductor material of the future. With time, silicon (Si) turned out to be more appropriate for a plethora of reasons [1–4]. Silica, the source of Si, is commonly available

and is easier to get high-purity Si from it. Silicon can easily be doped to produce n-type, p-type and semi-insulating material [5]. In addition to all these, a native oxide SiO_2 can be grown on Si using thermal oxidations at relatively low temperatures of around 900°C [6–8]. These properties make Si semiconductor industry favourite. At present, semiconductor industry worth is more than $300 billion [9]. Around 10% of this total is in smart integrated circuits and electronic power devices [10, 11]. In excess to more than 50% of our electricity is conditioned by electronic power devices [12, 13]. These devices are important because they determine the cost and efficiency of an electronic system. Hence, they have a greater influence on the economy of a country. The arrival of devices like the bipolar transistors in the 1950s led to the replacement of vacuum tubes [13, 14], and these improvements made possible the Second Electronic Revolution with Si as the material of choice. Power devices had a vital place in this revolution. In the 1970s, there were bipolar devices with a blocking voltage capacity of 500 V and high current capabilities. Also in 1970, International Rectifier Inc. launched the first metal-oxide-field-effect transistor (MOSFET) [15]. The idea was to switch bipolar devices with MOSFETs for high power use. The MOSFET is a unipolar device and thus can switch at a higher speed. Also, the MOSFET is a voltage-controlled device where the junction transistor is a current-controlled device. Higher switching speed means operation at higher frequencies where other system components such as inductors can be made smaller in size, and voltage control instead of current control means saving of internal energy in the device.

1.2. Need of a wide band-gap semiconductor device

To save energy on an electric power grid, the idea of redesigned 'micro-grids' has been proposed [16, 17]. Implementation of this concept needs power devices which can operate at higher switching speeds and block voltages of up to 20 kV [18]. A potential solution for this problem is to use wide band-gap semiconductor (e.g. SiC) power devices [19]. For a power device, the Baliga figure of merit (BFOM) [20] is given by

$$BFOM = \mu_N \varepsilon_S E_C^3 \tag{1}$$

μ_N = bulk mobility of SiC, ε_S = permittivity of SiC, E_C = critical electric field of breakdown for SiC. Higher the BFOM, more suitable the semiconductor is for high power operation.

1.3. Unipolar devices

Power devices can be divided into two categories—bipolar and unipolar. Schottky diodes and MOSFETs are examples of unipolar devices. In a unipolar device, only one type of carrier (either a majority electron or a majority hole) is responsible for current flow. The device can operate at higher frequencies which results in lower switching losses [20]. There is a flow of both majority and minority carriers in bipolar devices. The slower minority carriers have to be injected and removed to get the device to turn on and off, so

in bipolar devices there is power loss due to switching and leakage current. The n-channel Si-MOSFET is a better choice for low voltages (~100 V), and it can operate at high switching speed, 100 kHz. But as the blocking voltage increases, the on-state resistance increases drastically. The SiC-MOSFET enables us to go to higher operating voltages (order of kilo volts) with higher switching speed. This is possible because SiC has a high critical breakdown field, almost seven times that of Si. The specific on resistance (R_{ON}) of a MOSFET is given by [2]

$$R_{ON} = 4 V_B^2 / \mu_N \varepsilon_S E_C^3 \tag{2}$$

V_B is the desired blocking voltage, μ_N is the bulk electron mobility and ε_S is the semiconductor permittivity.

Bulk electron mobilities are similar for lightly doped Si and SiC (900–1200 cm^2/V s). However, $E_C^{SiC} \sim 7 E_C^{Si}$, so that for a given blocking voltage, R_{ON} can be a factor of 343 (7^3) times lower for SiC. Another way to think of this advantage is that lower critical field of Si means a much thicker drift layer is needed to support the source-drain voltage in blocking state. A thicker drift layer means higher drift resistance and thus higher R_{ON} for Si but lower R_{ON} for SiC. Furthermore, due to unipolar nature of the device we do not have to deal with stored charge and hence a FET will have higher switching speed.

1.4. Oxidation

Oxidation of 4H-SiC is a very important processing step during the manufacturing of a device. The performance of a metal-oxide semiconductor (MOS) device is dependent on the quality of the gate oxide layer. Out of many oxidation processes, thermal oxidation is the process most commonly used to form the interface (4H-SiC/SiO$_2$). Thermal oxidation is typically carried out in an oxygen (O$_2$) atmosphere (500 sccm) at 1150°C. The thermal oxidation process has been investigated both experimentally and theoretically by researchers. First-principle calculations done by Di Ventra et al. have shown that during thermal oxidation, atomic oxygen diffused onto the surface of SiC and formed an advancing interface (4H-SiC/SiO$_2$) [21]. Tan et al. confirmed experimentally that the excess carbon atoms diffused out as carbon monoxide (CO) [22]. For thicker oxide layers, their simulations showed that CO may break up either in SiO$_2$ bulk or at the interface (4H-SiC/SiO$_2$). The released oxygen participates in another round of oxidation, and the carbon atoms may lead to the formation of carbon clusters. Di Ventra et al. also proposed the formation of carbon dioxide (CO$_2$) while CO was emitted out through a thick oxide layer. Kanup et al. developed theoretical predictions of the formation of stable carbon pairs and carbon interstitials [23]. These defects combined with silicon interstitials form near-interface traps (N_{IT}). Near-interface traps are more critical compared to bulk traps for the mobility of SiC MOSFETs. The oxidation process can also cause the injection of carbon into SiC substrate. This injected carbon can exist in different forms such as carbon interstitials (C_i) and carbon di-interstitials ($C_i)_2$ to further degrade the FET channel

mobility [4–6, 24]. The oxidation rate of 4H-SiC depends upon the orientation of 4H-SiC wafers. This has been determined experimentally by Shenoy et al. [25]. The oxidation rate for C-face is three to five times faster than for the Si-face. Alumina-enhanced oxidation (AEO) is very fast due to the Na that is released from the alumina at the oxidation temperature. AEO on Si-face at 1050°C gives growth rate which is 10 times faster than normal thermal oxidation at 1150°C [26].

1.5. 4H-SiC/SiO$_2$ interface passivation

Silicon carbide exists in different polytypes 6H-, 4H- and 3C-. A MOSFET fabricated using 6H- polytype has field-effect inversion channel mobility which is much higher than that of 4H- polytype MOSFET (due to higher band gap of 4H-, Eg ~ 3.26 eV, most of the interface traps for 4H-SiC falls in the forbidden band, Eg ~ 3.0 eV for 6H- polytype). 6H-SiC due to its lower band gap, 3.0 eV, has lower critical electric field of breakdown (E_c) and bulk mobility compared to 4H-SiC. Also, in 4H- the field-effect mobility is more isotropic [5, 27] as compared to 6H-SiC. All these benefits make 4H- polytype a preferred choice among other polytypes of SiC for power devices. Although 4H- polytype has all these advantages, its full potential has not yet been exploited. This is due to high interface trap densities (D_{it}) at the interface (4H-SiC/SiO$_2$) 10^{13} eV^{-1}cm^{-2}. This value is much higher than the D_{it} of Si/SiO$_2$ interface (10^{10} eV^{-1}cm^{-2}). The cause of higher D_{it} is the formation of Si-dangling bonds, C-dangling bonds, O vacancies and C clusters. All this occurs during the oxidation of 4H-SiC [6–8]. Different post-oxidation annealing (called as passivation) techniques had been tried in the past to reduce the interface traps, for example, post-oxidation annealing in nitric oxide (NO), nitrous oxide (N$_2$O), ammonia (NH$_3$) and hydrogen (H$_2$) ambient [13, 29, 30]. NO/N$_2$O led to the incorporation of nitrogen (N) at the interface and forms different chemical species C-N, Si-N, Si-N-O and reduces the near D_{it} [6, 7]. The combined NO + H$_2$ passivation (NO passivation followed by H$_2$ passivation) gives improved interface which results in slightly better mobility ~40 cm^2/V s. Allerstan et al. have shown that the presence of sodium (Na$^+$) ion at the interface increases inversion channel mobility drastically up to 150 cm^2/V s, on the Si face of 4H-SiC MOSFET [11]. However, Na$^+$ moves under applied bias and hence destabilizes the device due to changing threshold voltage (V_T).The a-face (1120) of 4H- polytype with Al$_2$O$_3$/SiO$_2$ composite gate oxides leads to devices with channel mobilities of 100 cm^2/V s or more, but these MOSFETs showed higher leakage currents and lower breakdown voltages [13, 28]. Some groups have reported that the thermal oxidation at higher temperatures can lead to a better interface with a low-interface trap density value ~2 × 10^{11} eV^{-1}cm^{-2} at 0.2 eV from the conduction band (CB) edge [15, 29]. In the following sections, different interface passivation processes will be discussed.

1.5.1. Phosphorous interface passivation

In phosphorous (P) passivation, the interface is treated with P source to get a gate oxide with P at the interface. This can be done by using either a gas mixture of POCl$_3$, N$_2$ and O$_2$ or SiP$_2$O$_7$ as a planar solid source to form phosphosilicate glass (PSG), P$_2$O$_5$, under high-temperature

(1000°C) annealing in nitrogen environment. With P passivation, we can have different process variations in order to obtain different results, which are discussed in the following sections.

1.5.1.1. Thick PSG process

In thick PSG device, a 70-nm thermal oxide is grown and then passivated by a 3-h P passivation process. During interface passivation, the following reaction takes place, which leads to the formation of phosphosilicate glass. The formation of this PSG layer leads to a high concentration of P at the interface. The P concentration near interface is ~2 × 10²¹ cm⁻³ using Secondary Ion Mass Spectroscopy (SIMS), data are not shown.

$$SiP_2O_7 \xrightarrow{\quad N_2 \text{ gas 1L/min, 1000°C} \quad} SiO_2 + P_2O_5 \tag{3}$$
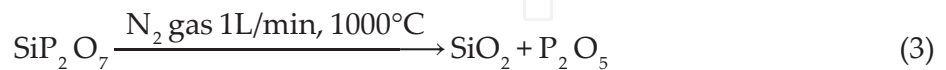
The D_{it} is significantly lower as compared to NO-passivated device and is 2×10^{-11} eV⁻¹cm⁻² at 0.2 eV from the conduction band edge, $E_c - E = 0.2$ eV, **Figure 1**. In all the D_{it} measurements, high-low C-V technique is used to extract the values. MOS capacitor results show that P passivation is more effective than NO passivation. The field-effect mobility of an n-channel MOSFET after P passivation is two times higher compared to standard NO passivation (**Figure 2**).

Bias temperature stress (BTS) test was performed on metal-oxide semiconductor capacitors for a positive/negative bias and results are shown in **Figure 3(a)** [30]. For a positive BTS test, the electric field is ~+1.5 MV/cm. The value of 0 V for flatband voltage (V_{FB}) before BTS in the case of phosphorous passivation confirms fewer interface traps after this process. The V_{FB} is significantly higher (~2 V) after NO annealing. After the positive BTS test, V_{FB} increases drastically from 0 to −18 V. The reason behind this shift in V_{FB} is induced positive polarization charge at the interface due to the formation of PSG layer. Results of a negative BTS test are also shown in **Figure 3(a)**. Due to induced negative polarize charge at the interface, the V_{FB} shifts in positive direction. Thus, the PSG layer makes devices highly unreliable by shifting V_{FB} in opposite directions. Results of a positive BTS test for a thick PSG MOSFETs are shown in **Figure 3(b)**. A negative shift of −2 V in threshold voltage after a positive BTS test confirms
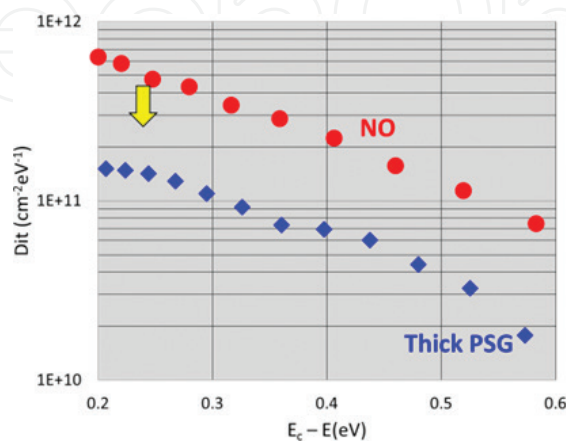

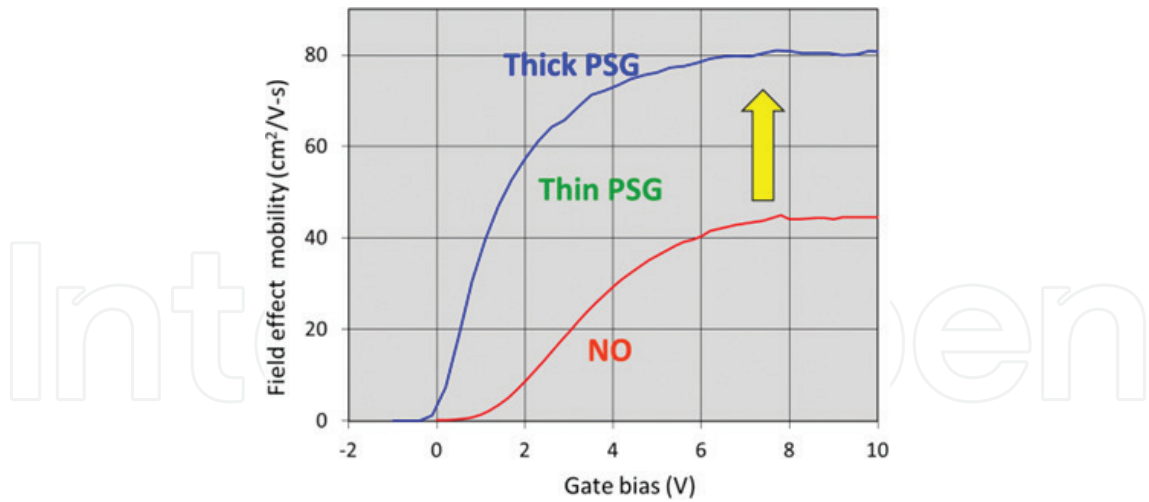**Figure 1.** D_{it} after 3-h P passivation and comparison with NO passivation.

Figure 2. Field-effect mobility of a MOSFET after P passivation and comparison with NO passivation.

that all these devices are highly unstable and of no practical use. Again, the near zero values for V_T confirm the effectiveness of P passivation compared to NO passivation.

Phosphorous process leads to improved interface by making traps electrically inactive and hence leads to higher field-effect mobility in 4H-SiC MOSFETs [6, 30]. Although the values of diffusion coefficients of impurities in SiC are very low, the possibility of P diffusion into SiC cannot be neglected. Phosphorous in the SiC substrate could have two effects: (i) phosphorous in the SiC can passivate carbon di-interstitial clusters and the correlated dangling bonds and (ii) the presence of phosphorous in the substrate can increase the concentration of n-type dopants (P) in the 4H-SiC/SiO$_2$ interface region to produce a counter-doping effect. This phenomenon has been observed in nitrogen-implanted 4H-SiC MOSFET. Both these effects (reduction in interface trap and counter-doping) lead to a lower V_T and a higher channel mobility [31, 32].
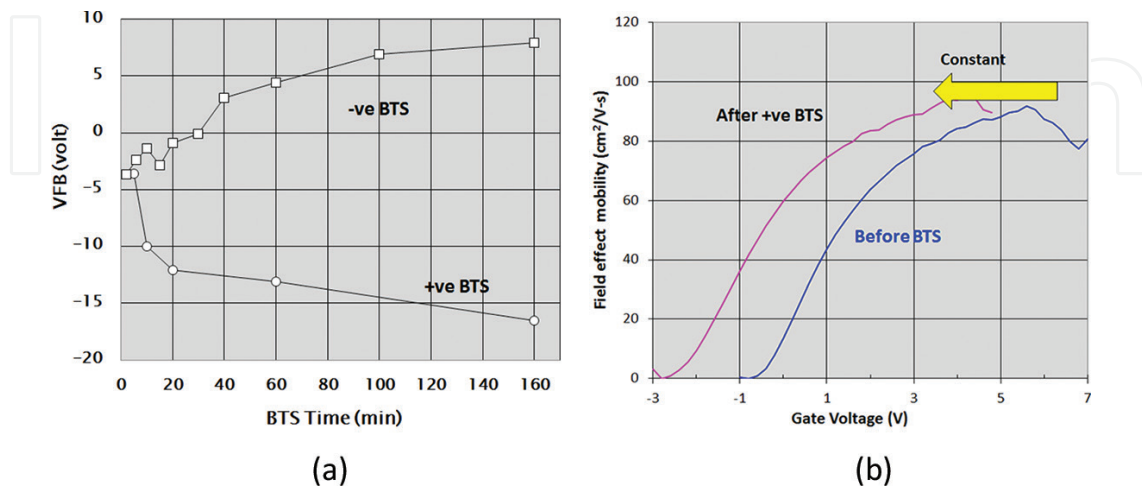

Figure 3. (a) V_{FB} after positive and negative BTS of a MOS capacitor. (b) Mobility data before and after positive BTS on a thick PSG MOSFET.

1.5.1.2. Etched PSG process

Annealing of an SiO_2 layer in a P_2O_5 ambient converts it into a phosphosilicate glass layer. PSG is a polar material [33], and if a positive/negative bias is applied at the gate terminal of MOSFET a positive/negative polarization sheet charge is induced at the $4H$-SiC/SiO_2 interface. The effect of this induced charge is similar to the effect of Na^+ ions at the interface. The presence of either charge leads to an unsTable 4H-SiC MOSFET. For example, this polarize charge can change a "normally-off" device to a "normally-on" device. X-ray photoelectron spectroscopy (XPS) results [34, 35] reveal that PSG layers cannot be removed completely by etching in BOE if is grown on 4H-SiC while opposite is true for the layer grown on Si. After BOE etching in the case of SiC, a 2–3-nm Si-C-O-P interfacial layer can still be seen which is equivalent to a phosphorous areal density of 2×10^{14} atoms/cm² (approximately one-tenth of a monolayer). Before etching, the areal density of phosphorus is 10^{15} cm^{-2}. We lose P after etching which is reflected in higher trap density for the etched PSG sample, **Figure 4**. In order to understand this phenomenon, we need to address the following two questions: (i) Is the un-etched PSG layer responsible for the better interface trap and hence high field-effect mobility? and (ii) Is there any difference between the bulk PSG layer and the un-etched layer in terms of induced polarization charge? These two questions are very important in order to understand the field-effect mobility and threshold voltage stability of the devices. An etching experiment on P-passivated MOS capacitors was performed to answer these questions. On etched devices, a thick layer of deposited oxide is used to fabricate MOS capacitors by using a low-pressure chemical vapour deposition (LPCVD) system at a temperature of 650°C. The D_{it} and V_{FB} results of PSG-etched devices are shown in **Figures 4** and **5** and are also compared with etched NO-passivated devices.

The D_{it} for an etched NO device is like as-oxidized MOS capacitors. The values are significantly higher and similar to the D_{it} profile for an unpassivated MOS device. These results show that, after etching, there is a decrease in the areal densities of both P and N from the $4H$-SiC/SiO_2 interface. As a result, we observed worst electrical properties of the interface
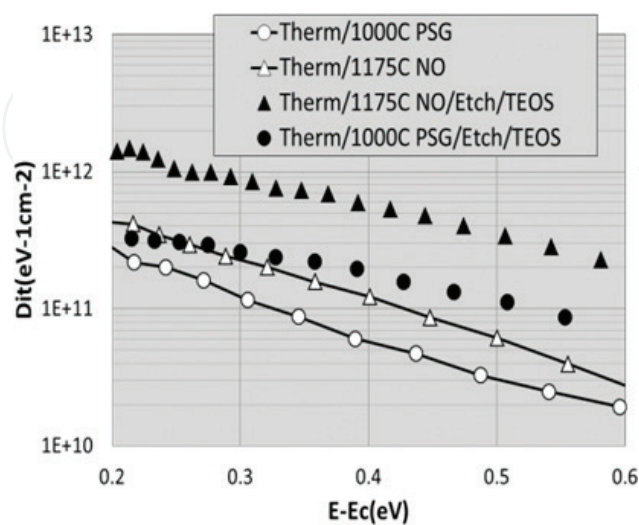

Figure 4. D_{it} before and after etching for NO and PSG MOS capacitors trap density increases after etching.
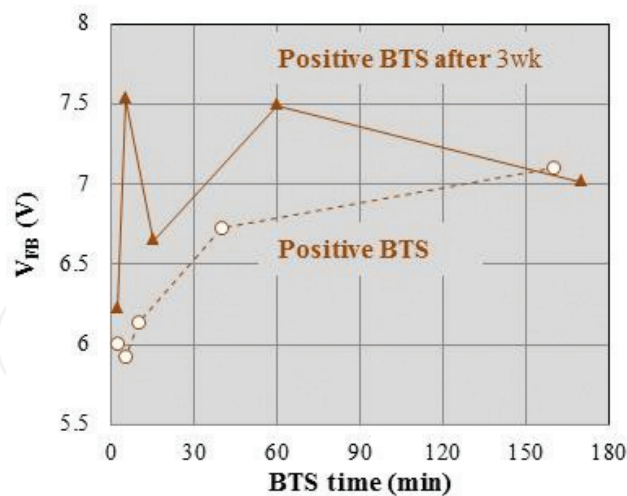
Figure 5. Positive BTS data of an etched PSG MOS capacitor device stability after etching.

caused by increased interface trap densities. The results of BTS tests for etched P-passivated samples are shown in **Figure 5**. The etched devices have flatband voltages, which remain constant at around 6 V and are caused by the electron injection phenomenon from the SiC into the polar (PSG) layer. For the etched PSG MOS capacitors, the values are reduced significantly showing the absence of high induced polarization charge at the interface. In the case of thick PSG samples, polarization charge induces a negative shift in V_{FB} which keeps on increasing with increasing BTS test time. The results of BTS tests for the etched PSG MOS capacitors show that, after etching, stability improves at the cost of higher interface trap density.

1.5.1.3. Thin PSG devices BTS

P passivation of the 4H-SiC/SiO$_2$ interface reduces the D_{it} but increases the threshold voltage instability due to the formation of a PSG layer during the process (**Figure 6**) [18]. In order to make the devices more reliable after P passivation, a different approach is used which involves a thin PSG layer (~10 nm). The D_{it} of a thin MOS capacitor is shown in **Figure 7**. D_{it} value for thin PSG MOS device is 3×10^{11} eV^{-1}cm^{-2} at $E_c - E = 0.2$ eV which is two times lower than NO-passivated device. The corresponding lateral 4H-SiC MOSFET has a peak channel
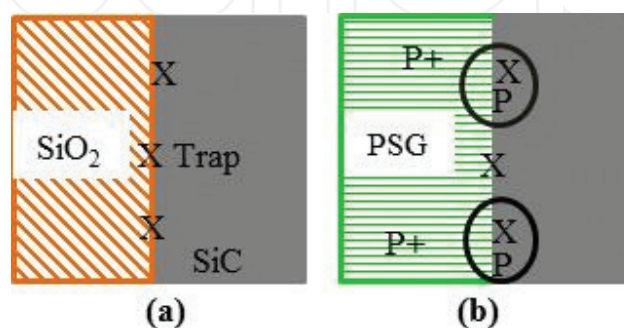

Figure 6. Gate oxide before (a) and after (b) P passivation. The P which passivates the traps at the interface also leads to instability by transforming SiO$_2$ into PSG.
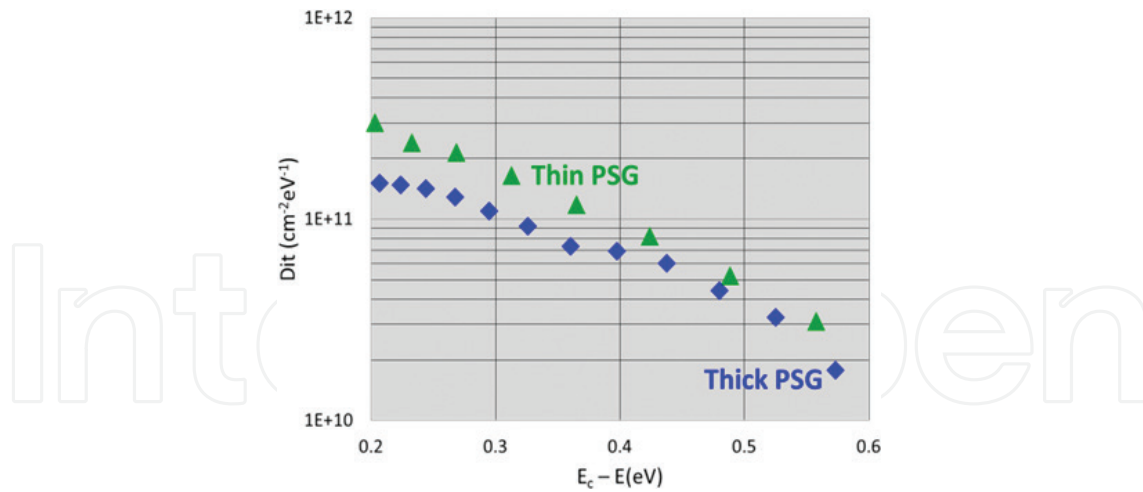
Figure 7. D_{it} for thin PSG MOS capacitor. D_{it} is lower than NO device, but higher than thick PSG device.

mobility of ~75 cm^2/V s, **Figure 7**. This number is approximately two times higher compared to an NO device. Although the mobility of a thick PSG is higher (**Figure 2**), the device is plagued with threshold voltage instability. The breakdown field for thin PSG device is NO-like, but its leakage current is significantly higher (not shown). Results for positive BTS tests for thin PSG MOS capacitors and MOSFETs are shown in **Figure 8(a)** and **(b)**, respectively. An oxide field of ~+1.5 MV/cm was applied at 150°C during positive BTS tests for all the samples. The thin PSG MOS capacitors show an improved electrical interface which translates into stable flat-band voltage values of the MOS capacitors. **Figure 8(b)** shows the electric field-effect mobilities of the MOSFETs before and after positive BTS tests performed for 8 h. We can observe that there is a small right shift caused by electron injection, in the field-effect mobility curve. This once again proves that using the thin PSG process, the device stability can be improved. The instability of thick PSG devices is due to polarization charge which is negligible in the case of
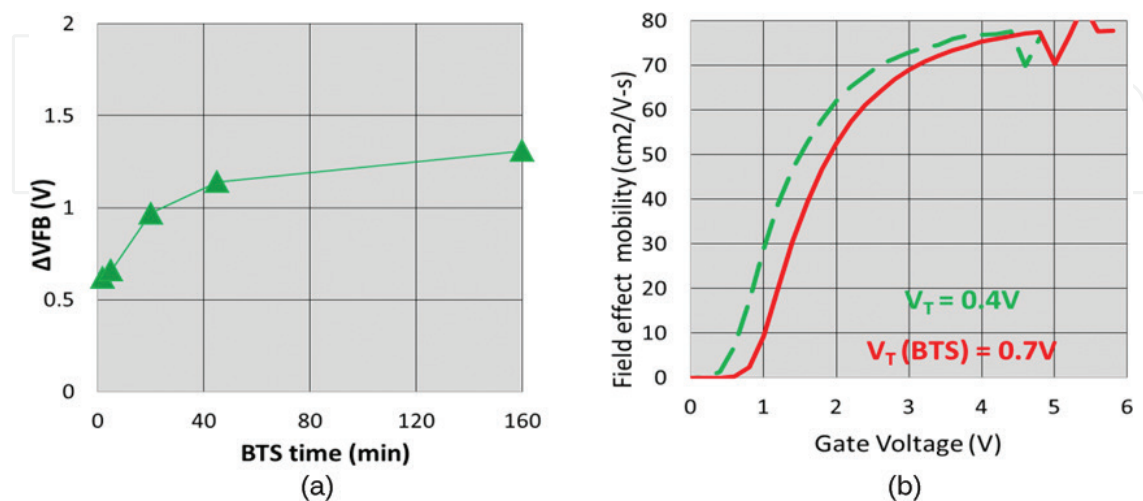

Figure 8. (a) Positive BTS data of a thin PSG MOS capacitor. Data show improved device stability. $\Delta V_{FB} = V_{FB}^{final} - V_{FB}^{initial}$ (b) Mobility data of a MOSFET with (dashed curve) and without 8-h positive BTS.

thin PSG devices. There is one-to-one relationship between the thickness of the PSG layer and shift in flatband voltage (ΔV_{FB}) for a given BTS voltage. As we increase the thickness of the gate oxide layer from 10 nm (thin PSG devices) to 70 nm, we get less stable device.

1.5.2. Nitrogen plasma (N-plasma) passivation of the 4H-SiC/SiO$_2$ interface

NO passivation is the process that has been used in the production of commercial SiC MOSFET. This process reduces the D_{it} of the interface, it has some limitations. This process is performed at high temperature between 1150 and 1200°C. The mechanism is that at such a high temperature, NO dissociates into atomic N and O. The N produced during the reaction reduces the number of the traps by passivating them, while the O reacts with the SiC layer forming an additional SiO$_2$ layer and hence a new set of interface traps [16]. Thus, there are two mechanisms going on simultaneously in competition. With N-plasma passivation where there is no atomic O, it is possible to eliminate additional oxidation and hence limiting the total number of traps caused during post-oxidation annealing. As a result during N-plasma passivation, the D_{it} decreases drastically. Also, we get some extra benefit from this process. It has been seen that after this process, the D_{it} continues to decrease with the increase of N plasma exposure time, which is not true in the case of NO passivation. In that process, the N concentration saturates at the interface after the annealing time of 2 h [17]. The D_{it} for 4-h N-plasma passivation is NO-like and results in NO-like mobility (~40 cm^2/V s). Eight-hour N-plasma-passivated MOS devices give D_{it} ~3 × 10^{11} eV^{-1}cm^{-2}. If mobility scales with D_{it}, MOSFETs that have undergone an 8-h N-plasma passivation should have a peak field-effect mobility of ~100 cm^2/V s.

For N-plasma passivation, ground-state atomic N is created in microwave plasma and a portion of these atoms recombine to emit at visible wavelengths. The set-up used to create N-plasma is shown in **Figure 9**. The snapshot of the spectrum formed during the N-plasma passivation is shown in **Figure 10**. In the spectrum, a peak is obtained at the wavelength of

Figure 9. High-temperature microwave plasma furnace used for nitrogen plasma passivation (N-plasma passivation).
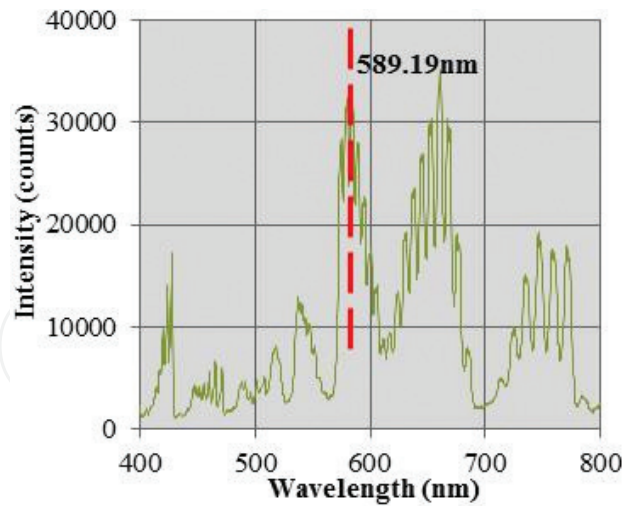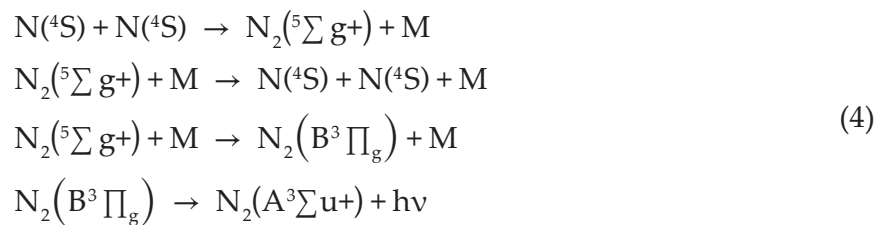
Figure 10. Typical spectrum of nitrogen during N-plasma passivation.

589.19 nm. This peak is obtained due to the recombination of active ground-state (^{4}S) N atoms. This recombination is followed by the decay of an excited state in the N_2 molecule and gives rise to yellow afterglow [19]. The mechanism, which causes the afterglow, takes place due to the following reaction.

$$
\begin{aligned}
N(^4S) + N(^4S) &\rightarrow N_2\left(^5\textstyle\sum g+\right) + M \\
N_2\left(^5\textstyle\sum g+\right) + M &\rightarrow N(^4S) + N(^4S) + M \\
N_2\left(^5\textstyle\sum g+\right) + M &\rightarrow N_2\left(B^3\textstyle\prod_g\right) + M \\
N_2\left(B^3\textstyle\prod_g\right) &\rightarrow N_2(A^3\textstyle\sum u+) + h\nu
\end{aligned}
\tag{4}
$$

Also, the intensity of yellow afterglow of emission is proportional to the square of concentration of active ground-state atoms. The amount of radiation detected at 589.19 nm is therefore a measure of the atomic nitrogen concentration in the plasma [36, 37]. After N-plasma passivation for the desired time, the recovery step was performed at 1160°C in N_2 flow. This step is used to heal the damage caused during the nitrogen plasma exposure of oxide and helps to improve the breakdown characteristics of the devices.

1.5.2.1. Four-hour N-plasma passivation on thermal oxide

Initially, the N-plasma process was used on the interface grown using a standard thermal oxidation. Nitrogen plasma also causes damage to the interface so N-plasma process is followed by a recovery process. Results obtained for a 4-h N-plasma process followed by a 2-h recovery process (from plasma damage) are shown in **Figure 11(a)** and **(b)** [38]. The D_{it} and electric field-effect mobility obtained under these conditions are both "NO-like." The thickness of the oxide layer used is 70 nm. The peak value of field-effect mobility of MOSFET is ~45 cm^2/V s (which is like NO-passivated MOSFET). The V_T determined by using the linear portion of the drain current versus gate voltage curve is around 4 V (**Figure 12**). After N-plasma passivation, the oxide breakdown field of the MOS capacitor is ~4 MV/cm. This lower breakdown field is
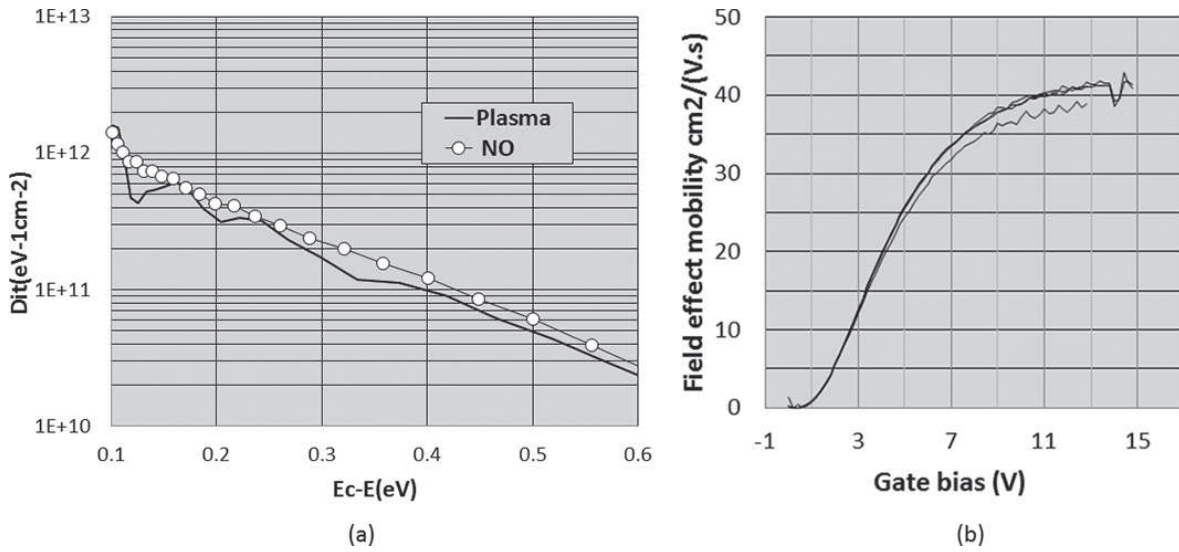
Figure 11. (a) Interface trap density (both NO and plasma) and (b) mobility for 4-h N-plasma passivation.

due to the damage caused during N-plasma passivation. This is the result of the gate leakage current and needs further optimization of the recovery process done after the passivation step. Also, we can conclude that the recovery anneal of 2 h is not enough.

1.5.2.2. Four-hour N-plasma passivation on deposited oxide

To limit carbon liberation (by minimizing the number of processing steps which causes oxidation) of the SiC, thermal oxide layers can be replaced by deposited oxides. The peak value of field-effect mobility for a companion MOSFET is ~50 cm²/V s (**Figure 12**), which is significantly higher than "NO-like" device, with threshold voltage again ~4 V (**Figure 13**). Note that this value is 25% higher than the one obtained with thermally grown oxide [38, 39].
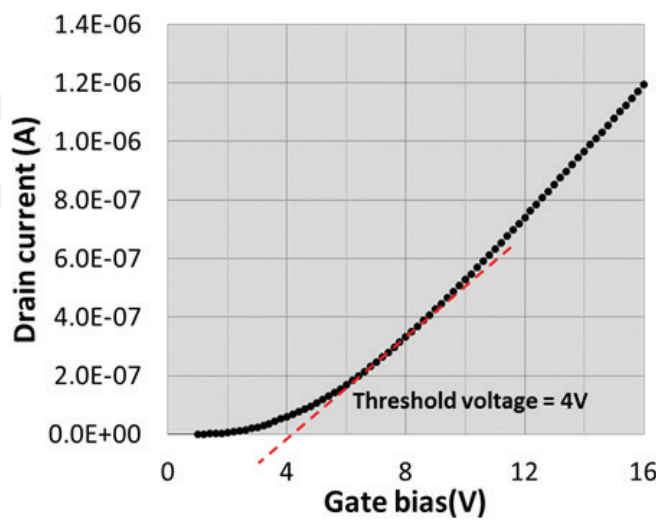

Figure 12. Threshold voltage (V_T) for a 4-h N-plasma passivation. The extrapolation in linear region method is used to extract the threshold voltage.
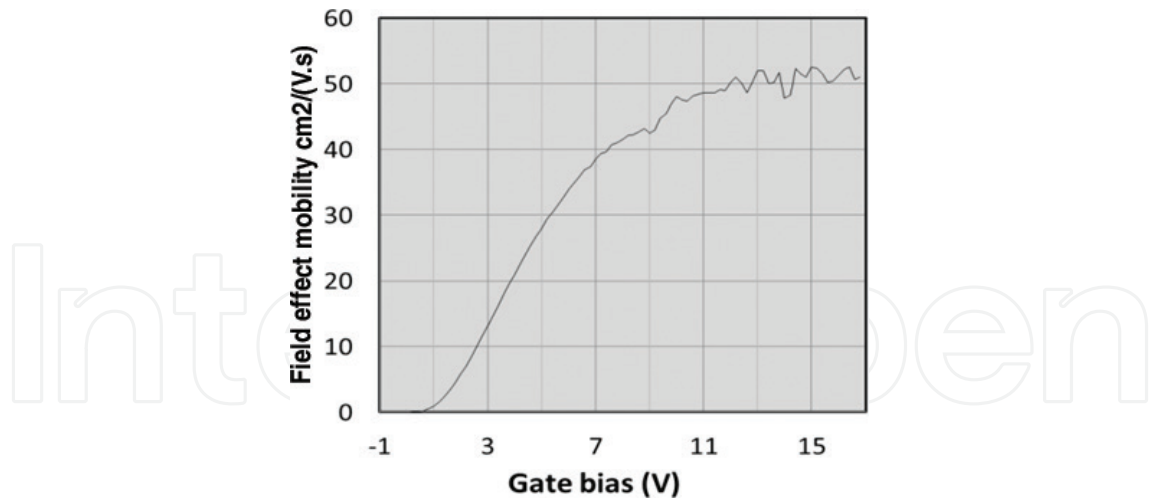

Figure 13. Mobility for a deposited oxide + 4-h N-plasma-passivated MOSFET.

1.5.2.3. Eight-hour N-plasma passivation

The interface trap density after 8-h N-plasma passivation with 6-h recovery is shown in **Figure 14(a)** for 62-nm thermal oxides [3, 39, 40]. The D_{it} at 0.2 eV is 2×10^{11} cm^{-2}eV^{-1}, which is like the MOS capacitors having a thick PSG layer. But as we discussed, these types of devices are highly unstable and of no practical use. With N-plasma passivation, we do not have this problem because the oxide layer is still SiO$_2$ and still non-polar in nature. The areal densities of N obtained after Secondary Ion Mass Spectroscopy measurements done on the MOS capacitors, which underwent 4-h and 8-h N-plasma passivation, are 6×10^{14} and 1.5×10^{15} cm^{-2}, respectively. The areal density for standard NO-passivated MOS capacitor is also 6×10^{-14} cm^{-2} and has been used as a reference sample. Also, XPS data for N-plasma-passivated devices have shown (not presented here) that the D_{it} for devices that have undergone this process is
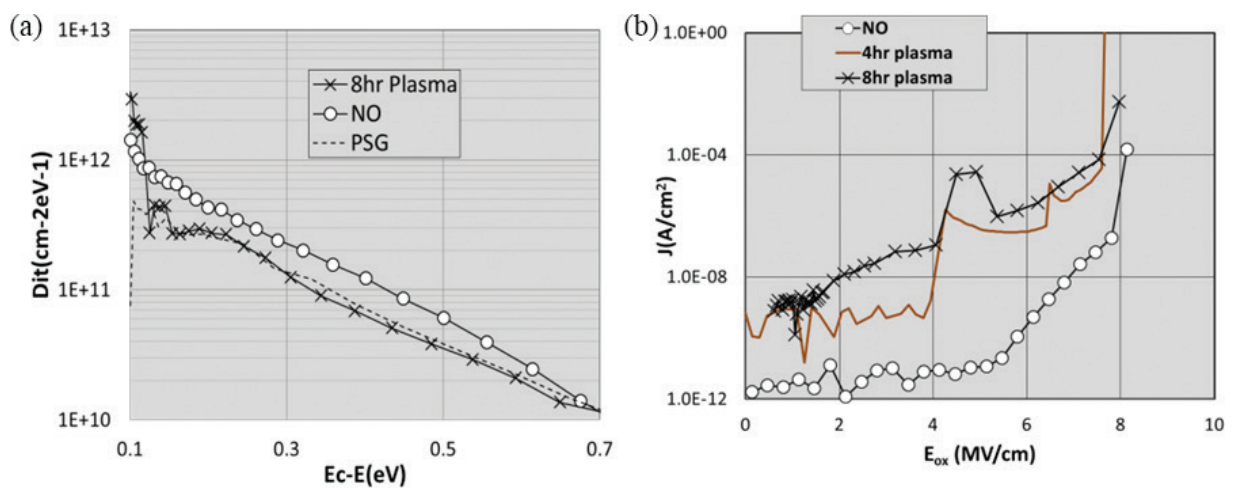
Figure 14. (a) Interface trap density for 8-h N-plasma passivation, and compared with thick and NO-passivated devices. The D_{it} is at $E_c - E = 0.2$ eV is 2×10^{11} cm^{-2}eV^{-1}, which is like thick PSG MOS capacitors. (b) Breakdown characteristics of MOS capacitors after 8-h N-plasma passivation. The dashed curve is for a standard NO device.

almost 2.5 lower than that for NO-passivated devices. **Figure 14(b)** shows breakdown characteristics after an 8-h N-plasma passivation. The oxide is leaky compared to NO, and the breakdown field is lower (~2 MV/cm for some devices). If mobility scales with D_{it}, MOSFETs that have undergone an 8-h N-plasma passivation should have a peak field-effect mobility of ~100 cm²/V s. Further optimization of the process is desirable to achieve higher N concentration at the interface and to improve the yield of the process.

1.5.3. High-temperature oxidation

Lately, there has been a growing interest in high-temperature oxidation of 4H-SiC. Studies have shown that if the oxidation conditions are optimized, then the 4H-SiC/SiO₂ interface grown after the process has much better electrical properties to the ones grown under standard conditions (1100–1200°C). In the following sections, we see the progress made in this area. Also, we discuss the effect of performing P and N_2O post-oxidation annealing on the oxides grown at high temperatures. It has been observed that high-temperature oxidation performed at 1500°C can lead to a better interface with D_{it}. **Figure 15(a)** shows the effect of temperature on the D_{it}. We can see with the increase of temperature from 1200 to 1500°C that D_{it} reduces from 2×10^{12} to 5×10^{11} cm⁻²eV⁻¹ at $E_c - E = 0.2$ eV. **Figure 15(b)** shows the linear transfer characteristics and field-effect mobilities of the devices measured at room temperature [36]. The V_T values for the devices without any passivation are typically around 5 [3, 49] which is due to the large number of traps at the interface. The net charge of these traps is negative in nature. This high-temperature process is effective in reducing in number of trapped and resulted in low threshold voltages observed in the MOSFETs. The reduction in trapped charge is reflected by the field-effect mobility of ~40 cm²/V s. This value is much lower than the previously reported results, even the one obtained at 1400°C. All this is a direct reduction
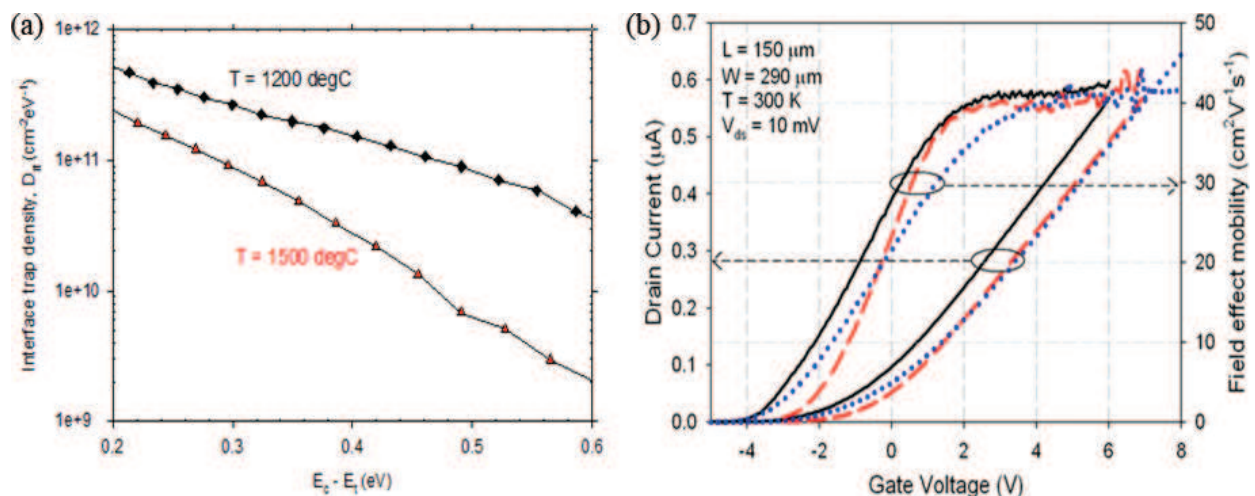

Figure 15. (a). D_{it} of thermal oxides grown at 1200 and 1500°C in a pure oxygen flow rate of 0.05 l/min. The increase in temperature resulted in approximately a twofold reduction in D_{it} from 5.3×10^{11} to 2.5×10^{11} cm⁻²eV⁻¹, a $E_c - E = 0.2$ eV. (b). Linear transfer characteristic and field effect mobility of 3 lateral 4H-SiC MOSFETs. Whilst there is a variation in threshold voltage, the novel high temperature gate oxidation process yields a consistent maximum mobility of ~40 cm²V⁻¹s⁻¹.

in Coulomb scattering. In this approach (high-temperature oxidation), there is no need of performing the post-oxidation annealing of the 4H-SiC/SiO$_2$ interfaces.

1.5.3.1. Combined N$_2$O and phosphorous passivations of the 4H-SiC/SiO$_2$ interface with oxide grown at 1400°C

Phosphorous (P) passivation is more effective than N$_2$O passivation in improving the 4H-SiC/SiO$_2$ interface by reducing the number of traps at the 4H-SiC/SiO$_2$ interface. There are some studies performed by Rong Hua et al. [41] to see the combined effect of high-temperature oxidation with either P or N$_2$O passivation. The MOS capacitor with 1400°C dry oxidation and without any post-oxidation passivation process has the highest D_{it} as shown in **Figure 16(a)**. The D_{it} results from the MOS capacitors have one-to-one relation with the field-effect mobility of the MOSFETs shown in **Figure 16(b)**, where the lowest D_{it} corresponds to the highest field-effect mobility. From **Figure 16(b)**, it can be seen that the P passivation can increase the peak field-effect mobility of a 4H-SiC MOSFET to about 66 cm^2/V s, which is five times higher than the value obtained after high-temperature N$_2$O-annealing process. Compared to low field-effect mobility, ~2 cm^2/V s, of the MOSFETs with gate oxide grown at 1400°C for 1 h without post-oxidation annealing process, the P-post-oxidation annealing (POA) process can dramatically increase the field-effect mobility.

However, the combined N$_2$O- and P-passivation processes have shown a slight decrease in the peak field-effect mobility value (60 cm^2/V s) compared to the P-only passivation. This value is still much higher than obtained using N$_2$O passivation (12 cm^2/V s). The only drawback for the combined N$_2$O- and P-passivation processes is that the MOSFET still has a negative threshold voltage (V_T) value (~−5 V) but better than the P-only passivation. The net positive charge at/or near the interface 4H-SiC/SiO$_2$ resulted in a negative V_T of the device. This value can be improved with further optimization of the process. The negative threshold voltage means that the device is normally on which is not an ideal choice from the application point
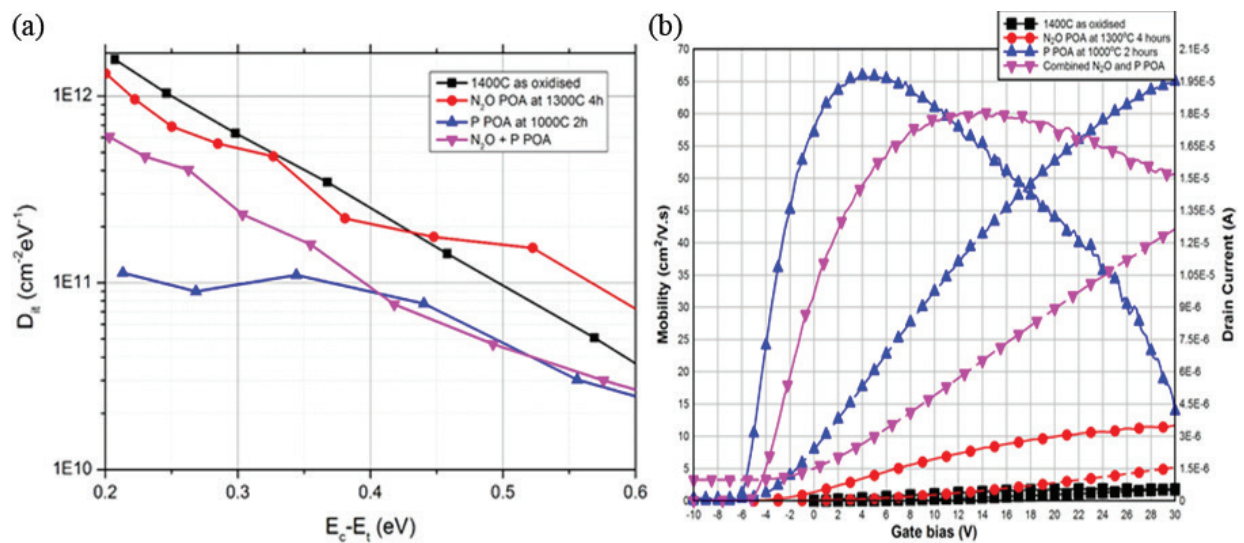

Figure 16. (a). Interface trap density extracted using high-low frequency capacitance method for MOS capacitors fabricated with different passivation conditions. (b). Field-effect mobility and the drain current against the gate bias for lateral MOSFETs with different passivation conditions.

of view. Potentially, this problem could be solved by using a thin layer (a few nm thick) of SiO$_2$ which afterward undergoes the suggested combined N$_2$O and P POA and then finally topped up by a thick(40-nm) deposited SiO$_2$ layer. There is no extra benefit of performing P passivation on the devices which have already had N$_2$O POA.

1.5.3.2. Impact of N$_2$O passivation on 4H-SiC/SiO$_2$ interfaces grown at high temperature

The results on high-temperature oxidation (1500°C) have shown a reduction in the interface trap density (D_{it}) without performing any kind of interface passivation. It would be interesting to see the impact of N$_2$O passivation on the oxides grown via high-temperature oxidation process. The interface is grown with high-temperature oxidation, and the results are shown in **Figure 1**. There is a decrease in the D_{it} for the high-temperature as-oxidized MOS capacitors as compared with the MOS capacitors grown using standard oxidation process. But there is no further improvement in the D_{it} with N$_2$O passivation performed at 1350°C, **Figure 17**. The electric field of breakdown for MOS capacitors with high-temperature oxidation with and without N$_2$O passivation is lower than 8 MV/cm. The reason for an early breakdown in the case of high-temperature as-oxidized MOS capacitors is not clear and further study is needed.
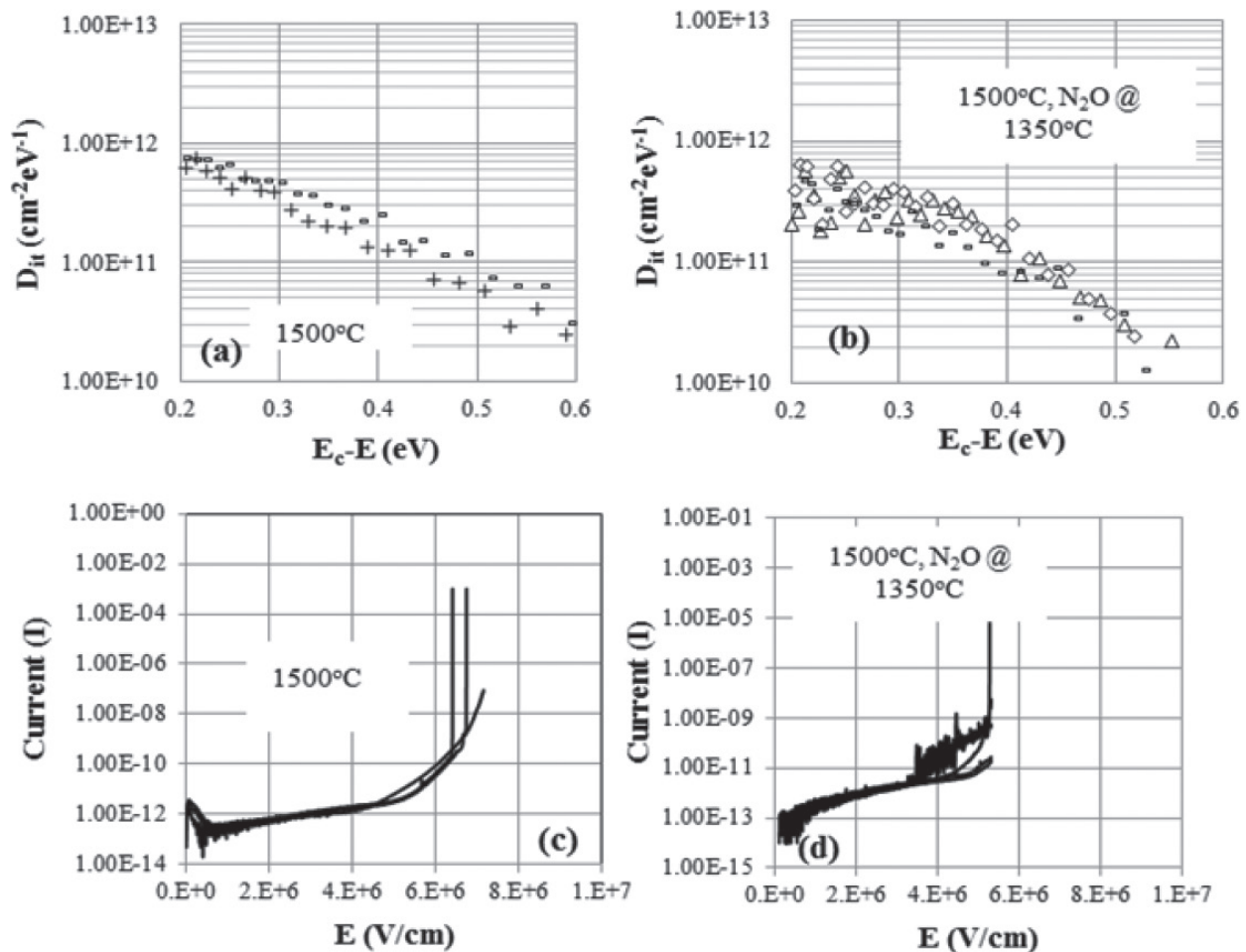

Figure 17. The electrical properties of the 4H-SiC MOS capacitors with a high-temperature (1500°C) thermal oxidation, interface trap density (a–b) and oxide breakdown (c–d).

In the case of passivated devices, this could be due to the incorporation of nitrogen throughout the bulk of the oxide, as previously reported on 4H-SiC MOS capacitors after ammonia passivation. We also performed N_2O passivation on the MOS capacitors grown via the standard oxidation process, and the results are shown in **Figure 18**. Again, the electric field of breakdown is lower for these devices. Also, there is no improvement in the D_{it} with the increase of temperature for N_2O passivation. The breakdown data for N_2O passivation at 1450°C could not be obtained due to a high increase in the oxide thickness after the passivation.

1.5.4. Other interface passivation processes

In addition to all these interface passivation processes, there are some studies done using boron (B) and Sb. Modic et al. have shown that Sb-doped surface channel in combination with nitric oxide post-oxidation annealing can increase the channel field-effect mobility to 100 cm^2/V s [42]. Also, Okamoto et al. were able to increase the channel field-effect mobility to 102 cm^2/V s by introducing boron atoms to the interface [43].

1.6. 3C-SiC/SiO$_2$ interface

There is a reignited interest on cubic silicon carbide (3C-SiC), which can be potentially grown heteroepitaxially on 12″ Si substrates, as it would result in a drastic cost reduction of semiconductor devices compared to the successful but prohibitively expensive SiC hexagonal
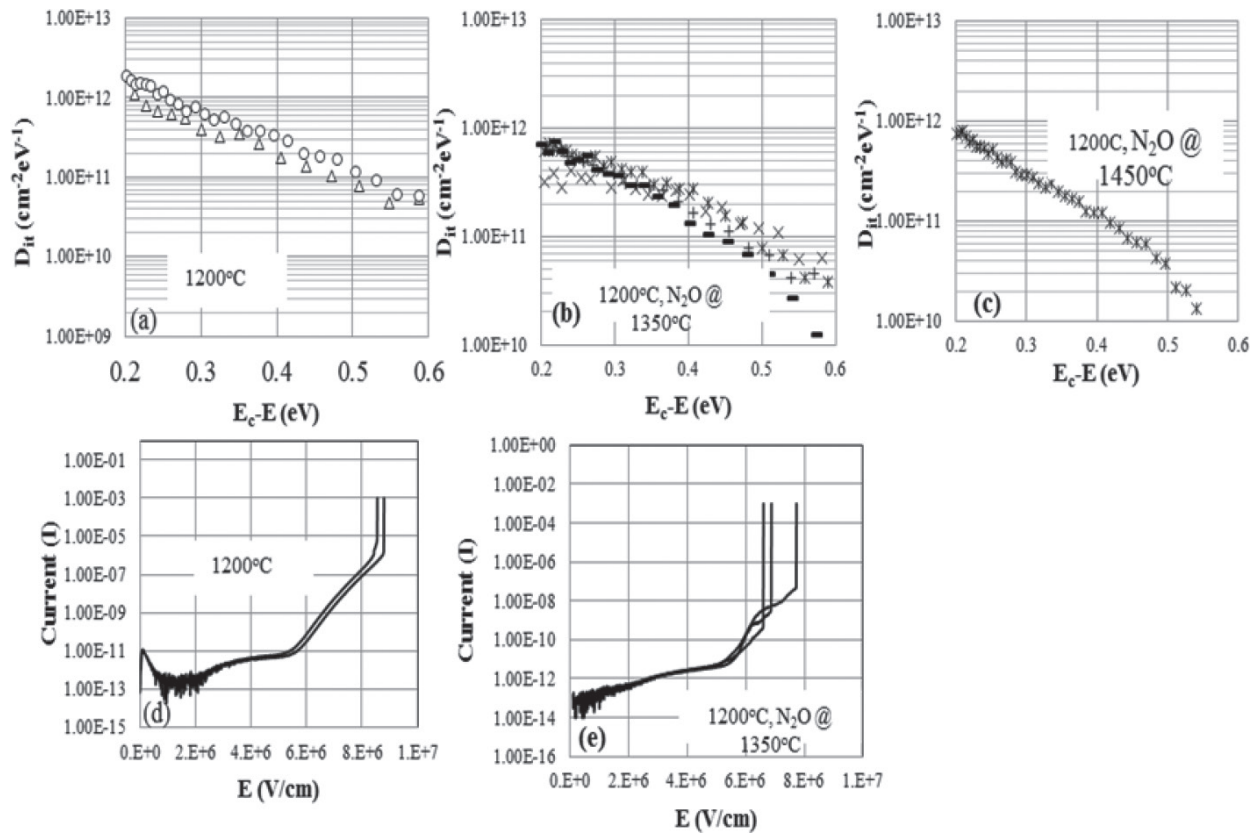

Figure 18. The electrical properties of the 4H-SiC MOS capacitors with a standard oxidation process (1200°C thermal oxidation) followed by N2O passivation at 1350 and 1450°C. From (a)–(c) D$_{it}$ versus E$_C$-E and (d)–(e) show breakdown characteristics of various MOS capacitors with different oxidation/passivation processes.

polytype technology (4H-SiC). It has been demonstrated that lateral power transistors in 3C-SiC outperform Si and 4H-SiC devices up to 1200 V, and represent an alternative to gallium nitride (GaN) technology. Also, GaN transistors are normally on, and as a result, it is challenging to control them eclectically. The voltage ratings for which these 3C-SiC devices are targeted for make them useful in automotive and other domestic appliances. Thus, this 3C-SiC technology has a huge potential for reducing the global carbon footprint.

1.6.1. High-temperature dry/thermal oxidation (1200–1400°C) and N_2O passivation of the 3C-SiC/SiO$_2$ interface

Due to the smaller band gap of 3C- (2.2 eV) compared to 4H- (3.2 eV), a fewer number of traps lie within the energy band gap of 3C-SiC in a metal-oxide-semiconductor structure resulting in better field-effect mobility [44]. It is found that 3C-SiC has different oxidation chemistry compared with 4H-SiC; 70–80-nm oxide can be grown at 1100°C in 1 h, which is 10 times faster than the oxidation rate of 4H-SiC on the Si face [45]. Also for the Si face in 4H-SiC, it has been observed that mobility increases with decreasing D_{it}. For example, as we go from thermally grown gate oxide to post-oxidation-annealed (passivated) oxide using hydrogen (H$_2$) passivation, NO/N$_2$O passivation, nitrogen plasma (N-plasma) passivation or phosphorous (P) passivation, D_{it} decreases significantly [37, 46–48]. Thomas et al. have shown that as-grown oxidized at 1500°C resulted in a 4H-SiC MOSFET with maximum field-effect mobility of 40 cm^2/V s. Sharma et al. have studied high-temperature oxidation of 3C-SiC [49]. In that work, the highest temperature used for the oxidation of 3C-SiC is 1400°C, because of the limit dictated by the melting point of Si (1414°C). The oxidation is done in 100% oxygen ambient. In addition, a standard nitrous oxide post-oxidation annealing of the interface is performed to see its effect.

A 3C-SiC/Si wafer with heterostructure grown on on-axis p-type Si (001) substrate was used in the work. The 3C-SiC epilayer is n-type with a doping concentration of N_D ~ 1 × 10^{16} cm^{-3}. The thickness of epilayer was around 10 μm. Lateral MOS-C structure had been used to study the electrical properties of the interface (inset of **Figure 19(a)**). The oxidation was performed at high temperatures followed by 30-min argon (Ar) annealing at temperatures used for oxidation. Standard high-low C-V and conductance techniques were used to analyse the 3C-SiC/SiO$_2$ interface. In addition, lateral *n*-channel MOSFETs were fabricated to extract the field-effect mobilities (μ). Planar MOSFETs were fabricated on the same substrate which was used to fabricate the MOS capacitors. **Figure 19** shows the normalized C-V curves at 1 MHz for different MOS-Cs. There are three distinct features of these curves. The first is a large flatband voltage shift ($\Delta V_{FB} = V_{FB,i} - V_{FB,ideal}$) towards negative gate bias, the second is increased capacitance in depletion and the third is to observe the large stretch-out in C-V characteristics. The subscript '*i*' stands for different processing conditions used to grow the gate oxide, *i* = 1 for 1200°C oxidation, *i* = 2 for 1300°C oxidation, *i* = 3 for 1300°C oxidation and *i* = 4 for 1300°C oxidation followed by N$_2$O annealing. **Figure 19(b)** shows a comparison between the ideal and experimental C-V curves for each temperature. The ideal C-V curve is obtained (solving the electrostatic and Poisson equation) by assuming that the 3C-SiC/SiO$_2$ interface is perfect, having no defects near the interface and also in the bulk of the oxide and 3C-SiC. The doping value used in the computations for the high-temperature-oxidized samples was N_D = 0.63 × 10^{16} cm^{-3} for all the oxidation temperature range, that is, the 3C-SiC doping concentration
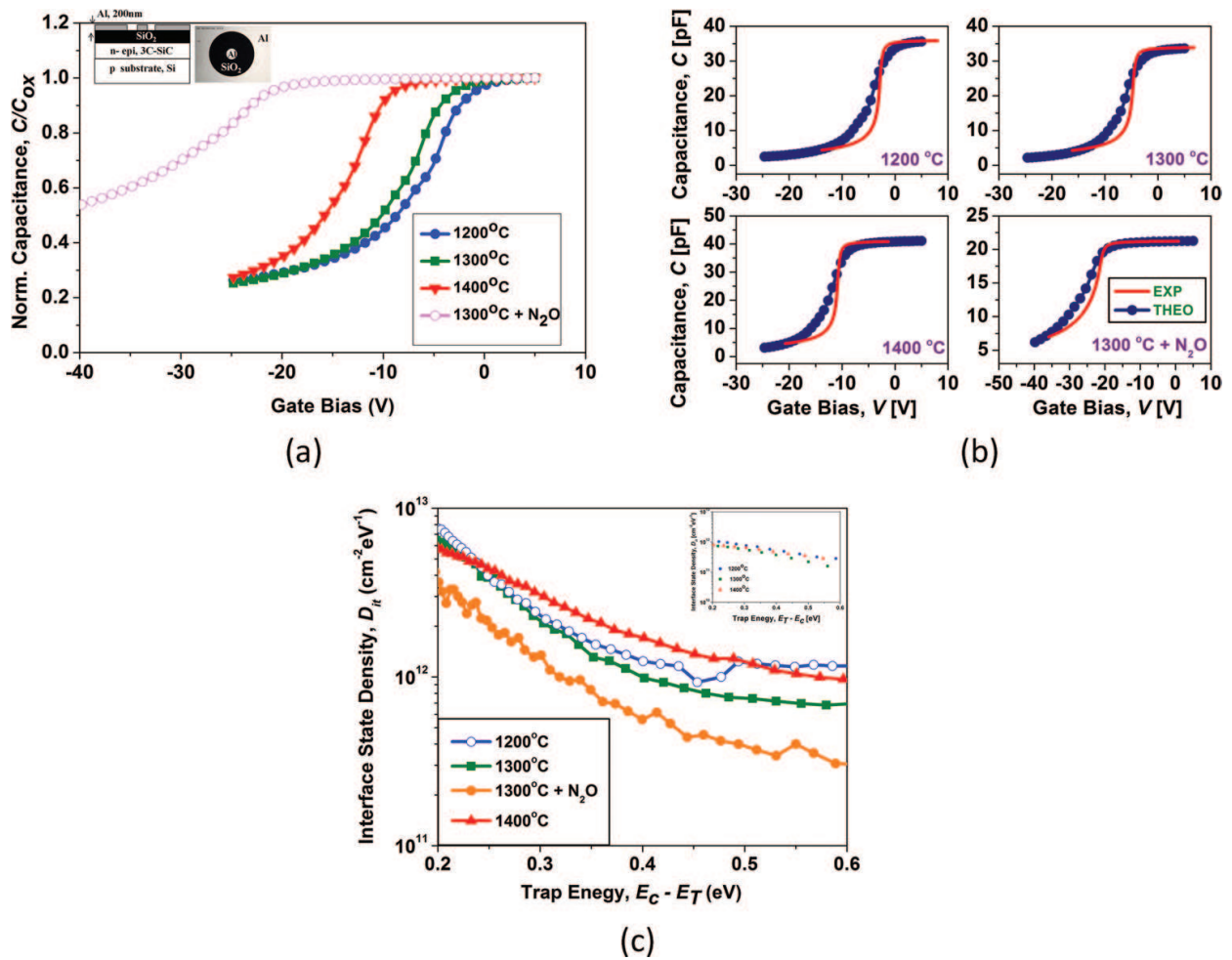
Figure 19. (a) Typical 1-MHz C-V curves for 3C-SiC MOS structures with oxides grown at 1200, 1300, 1400 and 1300°C+N_2O. (b) A comparison between the ideal and experimental C-V curves for each temperature. (c) Interface state densities (D_{it}) for 3C-SiC MOS structures with and without post-oxidation anneal (N_2O) process, calculated using Terman C-V and conductance (inset) methods. Due to a very wide Gaussian dispersion, it is not possible to extract D_{it} for the N_2O-annealed device using the conductance method.

seems to be stable even for 1400°C. Interestingly, a significant increase in the 3C-SiC doping was observed for the sample further annealed in N_2O. In this case, a value of N_D = 2.45 × 10^{16} cm^{-3} was used to fit the experimental capacitance. The flatband voltage shift shows the existence of net positive fixed charge at the interface and its origin is believed to be the presence of carbon clusters and dangling bonds formed after thermal oxidation [6] Carbon clusters and dangling bonds act as donor-like states and are positively charged when they are empty and as a result give rise to a negative shift in V_{FB}. The calculations for effective oxide charge (Q_{EFF}) has been done (not shown) for all the MOS-Cs. It was found that Q_{EFF} increases with temperature, which is different from the results reported previously on 3C-SiC MOS-Cs and further research is required to explain this behaviour [50]. In addition to carbon clusters, the nitrogen-related complex in the case of 1300°C (oxidation + N_2O annealing) MOS-C causes a large shift in V_{FB}, likely due to its incorporation in the 3C-SiC surface and resulting in an increased doping concentration [51]. Also, as mentioned above, all the curves are significantly stretched out compared to the ideal curve, representing the presence of high interface traps. These traps

could be near the conduction band edge and/or the presence of oxide near interface traps (also known as slow traps) [52]. Hysteresis (not shown) in the C-V curves indicates the slow nature of some of the traps [52]. In addition, less band banding is caused by increased net positive fixed charge at the interface resulting in increased capacitance in depletion region [53]. **Figure 19(c)** shows the density of interface traps (D_{it}) extracted from the Terman C-V method and compared with conductance methods (shown as inner graphic of **Figure 1**). Both these methods give consistent results with 1300°C (oxidation + N_2O) leading to the lowest D_{it} = 1.8 × 10^{12} cm^{-2}eV^{-1} at $E_c - E_T$ = 0.25 eV. This value is two times smaller than the one obtained with the 1300°C oxidation process (D_{it} = 3.7 × 10^{12} cm^{-2}eV^{-1}). It is believed that these D_{it} values are rather high, primarily because of the contribution of slow states. As it can be seen in **Figure 19(b)** for the 1300°C (oxidation + N_2O) device, the plateau is quite ideal for voltages larger than the flatband (accumulation) but in depletion there is a relevant dispersion (ideal versus experimental), typical signature of the oxide near interface traps. The superiority of annealed device is also confirmed by the G-V plot as shown in **Figure 20(a)**, performed at 100 kHz. The area under the conductance peak is a measure for D_{it}. The position of the peak corresponds to the energy position in the band gap and as all these peaks occur at gate bias close to V_{FB}, it can be inferred that these peaks are a measure of D_{it} close to the CB edge of 3C-SiC [49]. Devices without the N_2O post-oxidation annealing have larger area under G-V curves when compared with the annealed device, implying higher D_{it} for non-annealed devices. The peak value of 1300°C (oxidation + N_2O) is much smaller than other devices and hence this device has the lowest D_{it} being consistent with Terman and conductance methods. Also, all of the admittance-voltage (G-V) curves have finite full width at half maximum (FWHM) signifying that these traps are dispersed over an energy range within the band gap and are not localized at a fixed energy value. Similar results have been reported on the MOS capacitors implanted with N [54]. As the 1300°C oxidation process with N_2O post-oxidation annealing gives the lowest D_{it}, this process was used to fabricate a lateral 3C-SiC MOSFET. Also, a lateral MOSFET was fabricated with the 1300°C oxidation process, as for a reference sample. The results of mobility
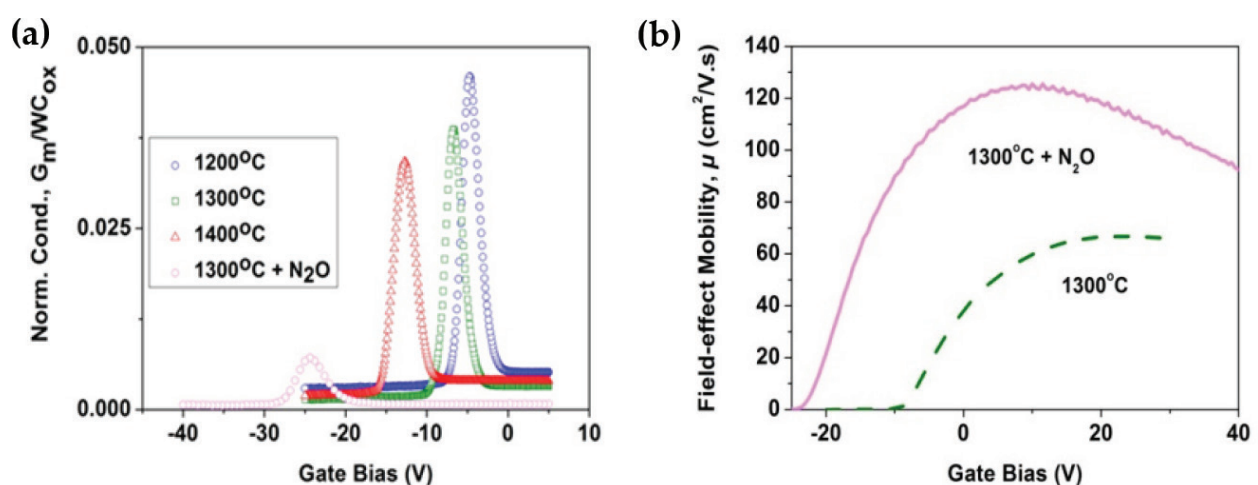

Figure 20. (a) Normalized conductance curves of 3C-SiC MOS structures taken for different gate voltages at probe frequency (ω) = 100 kHz. (b) Field-effect channel mobilities (μ) for N_2O-annealed and non-annealed 3C-SiC MOSFETs. Both the N_2O post-oxidation annealing and thermal oxidation were done at 1300°C.

measurements for lateral MOSFETs are shown in **Figure 20(b)**. The device with N_2O annealing has a peak channel mobility of approximately 120 cm²/V s, and shows a ×2 improvement in peak mobility as compared with a 1300°C as-oxidized MOSFET which has a mobility of 60 cm²/V s. This is consistent with the fact that the N_2O-annealed MOS-C has better D_{it} as compared with the as-oxidized 1300°C MOS-C. The MOSFET annealed in N_2O has a relatively sharp turn-on and a peak channel mobility of 125 cm²/V s. At greater gate biases, the field-effect mobility decreases because of the increasing surface field, which may be an indication of the surface roughness to be a dominant scattering mechanism [40]. **Figure 21** shows atomic force microscopy (AFM) analysis that has been performed on all of the devices in order to see the effect of temperature on the surface morphology. The root-mean-square (RMS) values of roughness for all these MOSCs lie in the range of 0.54–0.60 nm, showing that high temperatures (≥1300°C) do not have effect of temperature on the surface morphology. The RMS values of roughness for all these MOSCs lie in the range of 0.54–60 nm, showing that high temperatures ($T ≥ 1200°C$) do not have any significant detrimental effect on the oxide surface. The Secondary Ion Mass Spectrometry profiles are shown in **Figure 22**. The N_2O-annealed device shows the accumulation of nitrogen at the interface which is responsible for the improved D_{it} and field-effect mobility (μ) in this process. There is virtually no appreciable difference between the Si, O and C profiles for all the devices, and it could be due to no out-diffusion or diffusion of species from the interface. There is a possibility that the Si, O and C concentration
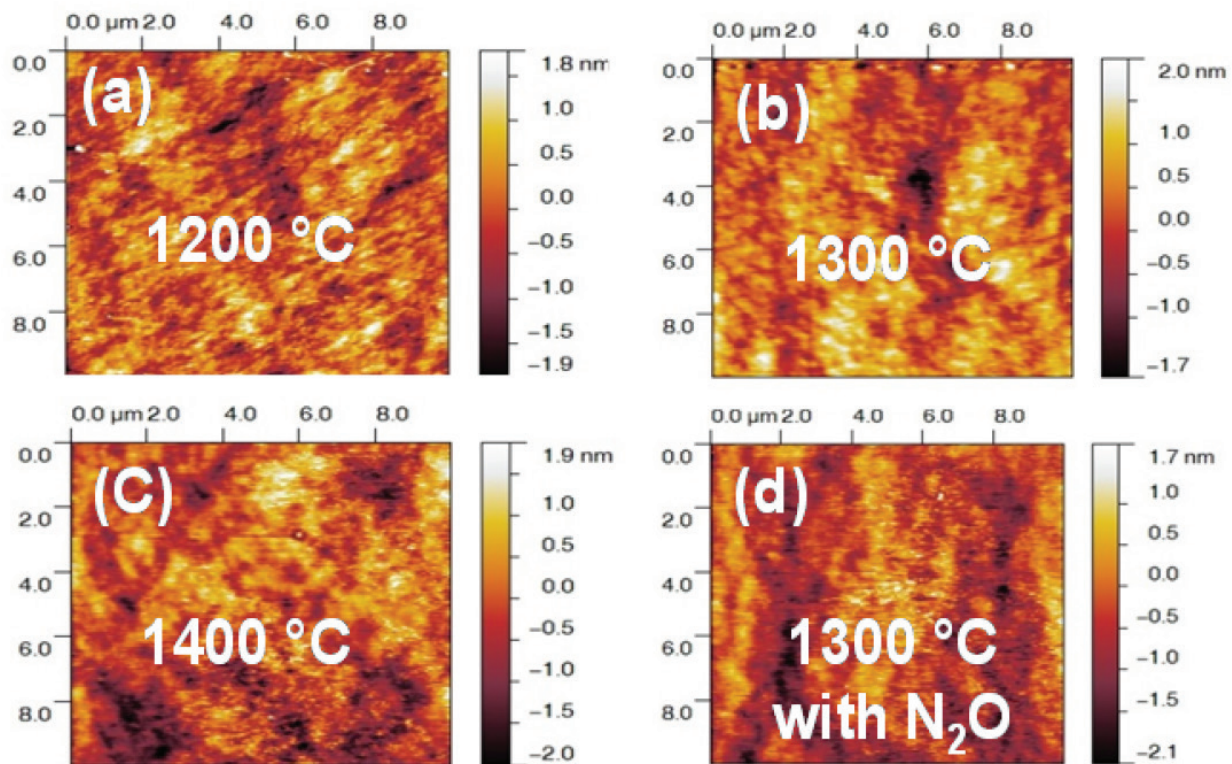

Figure 21. Atomic force microscopy (AFM) for results different processed MOS capacitors with as-grown thermal oxide (a) at $T = 1200°C$ (b) $T = 1300°C$, (c) $T = 1400°C$ and (d) $T = 1300°C$ with N_2O post-oxidation annealing. The RMS values of roughness within a range of 0.54–0.60 nm, implying that high temperature does not have deteriorating effect on the surface morphology of devices.
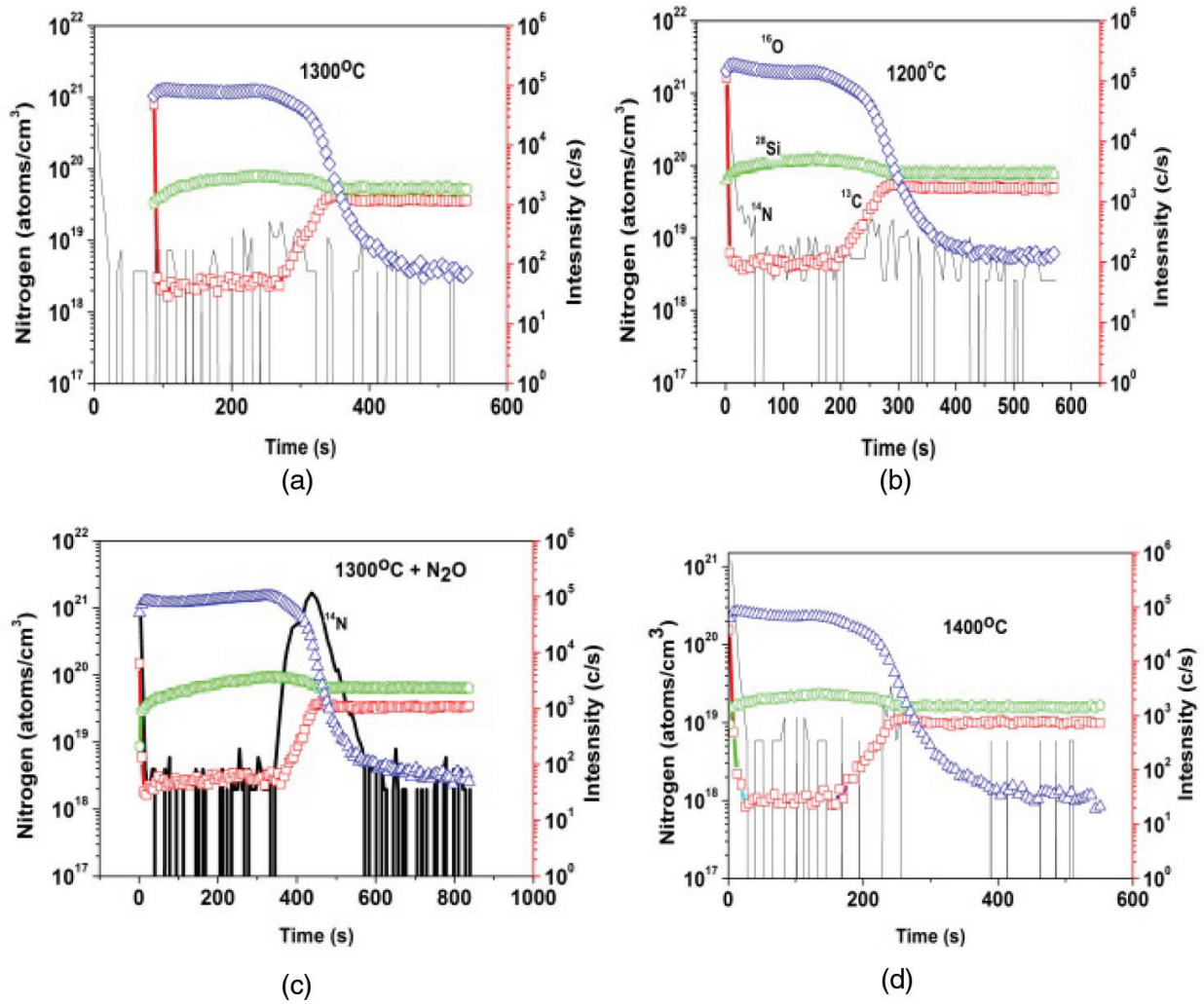
Figure 22. SIMS profiles for 3C-SiC MOS capacitors fabricated under different conditions with (a)–(c) for as-oxidized MOS capacitors. From plot (d), it is evident that most of the nitrogen has accumulated at the 3C-SiO$_2$/SiC interface in the case of 1300°C N$_2$O-annealed device. It is obvious that most of the nitrogen has accumulated at the SiO$_2$/SiC interface after an NO anneal.

decreases monotonically very slightly with temperature, which is not within the tolerances of SIMS measurement. The parallel equivalent conductance spectroscopy is used to further anal-yse the characteristics of the high-temperature oxidation. **Figure 23** shows G_P/ω versus probe frequency (f) curves for non-annealed and 1300°C (oxidation + N$_2$O) devices. By fitting the curves to a Gaussian fit, the interface state density, trap time extracted. As shown in **Figure 5**, the 1300°C (oxidation + N$_2$O) device could have no Gaussian dispersion or a very wide Gaussian dispersion, and as a result it, is not possible to fit the experimental data and it is not possible to extract D_{it}, trap time constant (t_p) and surface-potential fluctuations (σ_s) for the Gaussian dispersion, for the annealed device. The D_{it} extracted using this technique for all the devices is shown as the inset of **Figure 1**. Naik and Chow have reported a wide Gaussian dispersion for conductance curves on NO-treated 4H-SiC MOS-C [54], which potentially explains the results presented here. **Figure 24(a)** plots the trap time constant as a function of energy. As we can see from the figure that across the different energy levels in the band gap, t_p increases with increasing temperature. At a constant temperature, t_p increases as we go
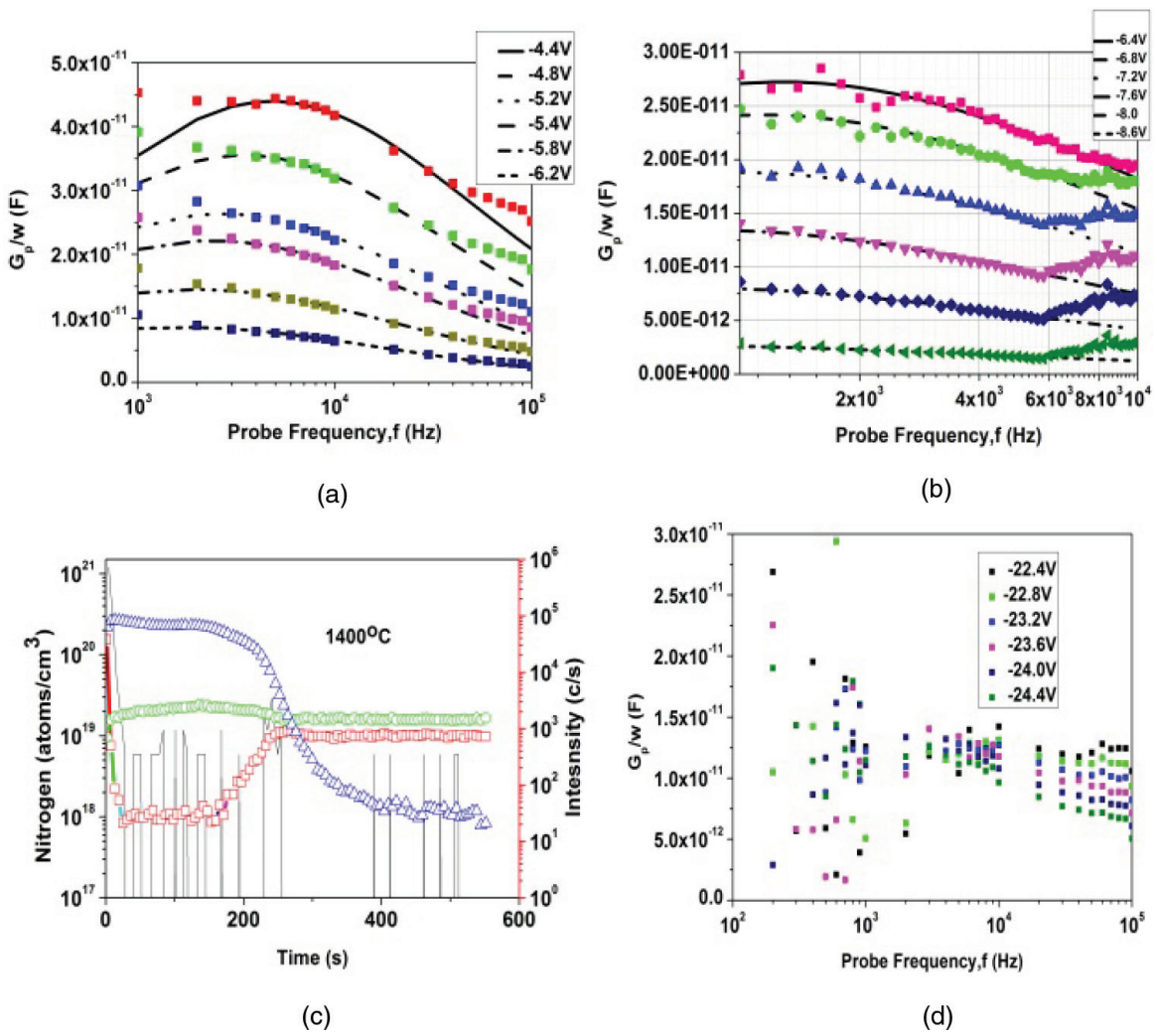
(a)

(b)

(c)

(d)

Figure 23. G_p/ω versus probe frequency (ω) at different biases in depletion region for MOS capacitors with as-grown thermal oxide (a) at $T = 1200°C$, (b) $T = 1300°C$, (c) $T = 1400°C$ and (d) $T = 1300°C$ with N$_2$O post-oxidation annealing.

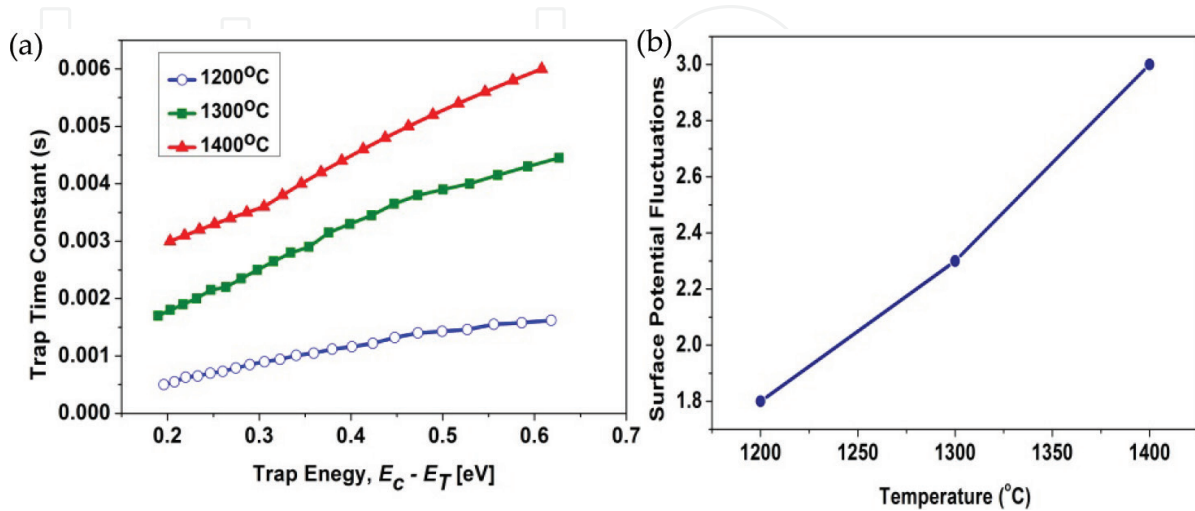**Figure 24.** (a) The trap time constant as a function of energy and (b) the temperature dependence of standard deviation of the surface potential (σ_s).

deeper into the band gap. The surface-potential fluctuations can be extracted by performing the curve fitting to the *G-V* curves. In **Figure 24(b)**, we can see the temperature variation of the standard deviation of the surface potential (σ_s) which is caused by fluctuations of interface states for different MOS capacitors. The values lie between 2 and 3, which indicates that the 3C-SiC/SiO$_2$ interface is electrically better than 4H- polytype (σ_s = 4 for 4H- and around 2 for Si). This fairly low value of σ_s, coupled with the low value of D_{it} and the MOSFET field-decreasing large field-effect mobility, suggests that Coulombic interface-scattering-related effects should not limit transistor performance.

In conclusion, high-temperature oxidation (1200–1400°C) has been used to grow the 3C-SiC/SiO$_2$. Out of all the oxidation temperatures investigated, 1300°C was found to be the optimum temperature for oxidation. The interface can be improved further by performing the N$_2$O post-oxidation annealing again at 1300°C for 2 h, though this leads to high accumulation of N at the interface. The lateral MOSFET with N$_2$O-annealed oxide yielded a field-effect mobility of 125 cm^2/V s, which is twice the value of non-annealed MOSFET, with the gate oxide grown at 1300°C (60 cm^2/V s). The low values of σ_s and larger μ for as-oxidized MOS-Cs show that the 3C-SiC/SiO$_2$ interface is better than its 4H-SiC counterpart (at least in terms of interfacial fast traps). These findings have important implications for SiC-MOS technology as 3C-SiC/Si can provide a low-cost alternative even in the case of high temperature of processing.

Acknowledgement

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