Chapter 9

Modeling of Silicon Photonic Devices for Optical Interconnect Transceiver Circuit Design

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Additional information is available at the end of the chapter

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Abstract

Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating co-simulation environments with compact optical device simulation models. This chapter presents compact Verilog-A silicon carrier-injection and carrier-depletion ring modulator models which accurately capture both nonlinear electrical and optical dynamics. Experimental verification of the carrier-injection ring modulator model is performed both at 8 Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9 Gb/s with a 65-nm CMOS driver capable of asymmetric pre-emphasis pulse duration. Experimental verification of the carrier-depletion ring modulator model is performed at 25 Gb/s with a 65-nm CMOS driver capable of asymmetric equalization.

Keywords: microring modulator, carrier-injection, carrier-depletion, optical interconnects, silicon photonics, co-simulation, Verilog-A

1. Introduction

Due to low channel loss and the potential for wavelength division multiplexing (WDM), optical interconnects are well suited to address the dramatic requirements in high-speed interconnect capacity and transmission distance demanded by mega data centers and supercomputers [1, 2]. For these applications, silicon photonic platforms are attractive due to their large-scale photonic device integration capabilities and potential manufacturing advantages. As shown in **Figure 1**, compact and energy-efficient WDM interconnect architectures are possible with silicon photonic microring resonator modulators and drop filters [3], as these high-Q devices occupy smaller footprints than large-area Mach-Zehnder modulators [4] and offer inherent wavelength multiplexing without extra device structures, such as array waveguide gratings.

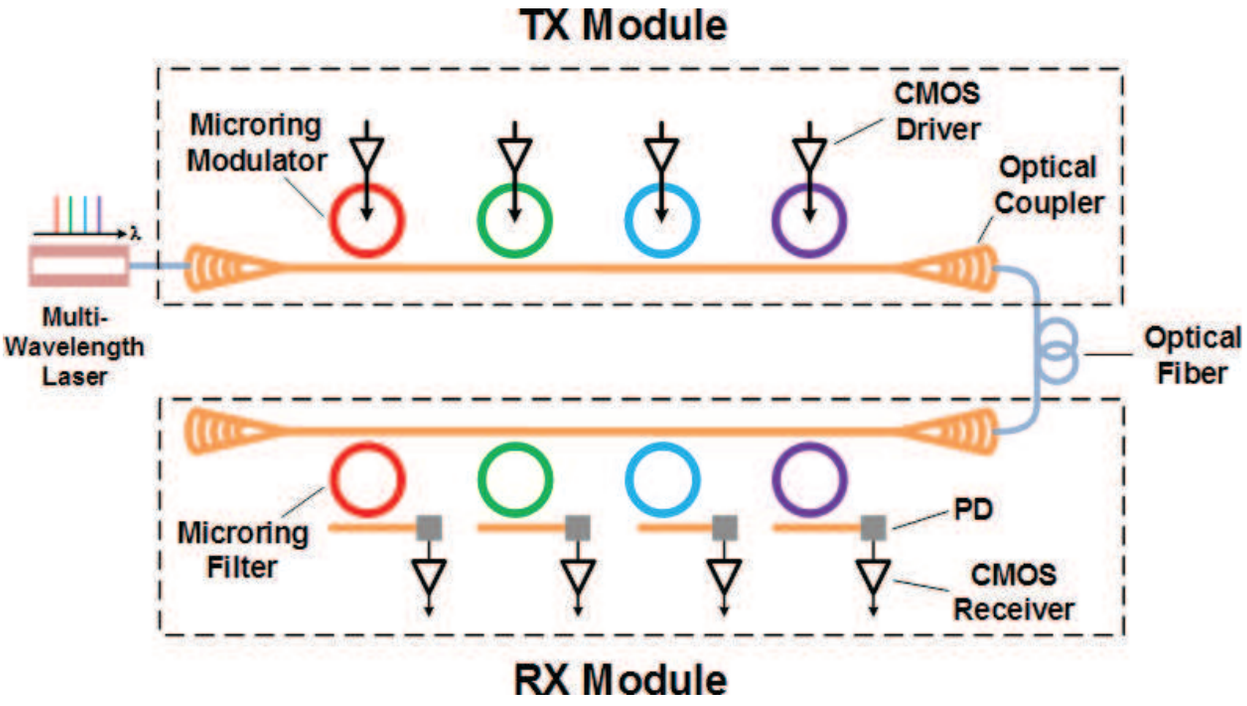

Figure 1. Silicon photonic ring resonator-based wavelength-division-multiplexing (WDM) interconnect system.

The most common high-speed silicon ring modulators operate based on the plasma dispersion effect, with devices based on carrier accumulation, depletion, and injection which display various trade-offs. Accumulation-mode modulators based on metal-oxide-semiconductor (MOS) capacitors can achieve high extinction ratios, but their modulation bandwidth is limited by the relatively high device capacitance [5]. At data rates near 10 Gb/s, injection-mode modulators based on forward-biased p-i-n junctions are an attractive device due to their high modulation depths and rapid bias-based resonance wavelength tuning capabilities [6, 7], but their speed with simple non-return-to-zero (NRZ) modulation is limited by both long minority carrier lifetimes and series resistance effects [8]. Depletion-mode modulators based on reverse-biased p-n junctions can achieve high speed (~40 Gb/s) [9], but require large drive voltages [10]. Injection-mode modulators provide higher energy efficiency and depletion-mode modulators offer higher bandwidth density. Sections 2 and 3 present two compact Verilog-A models for carrier-injection and carrier-depletion ring modulators including both nonlinear electrical and optical dynamics, respectively. Finally, Section 4 concludes the chapter.

2. Silicon carrier-injection ring modulator model

Pre-emphasis signaling, which improves optical transition times, is necessary in order to achieve data rates near 10 Gb/s with carrier-injection ring modulators [7, 8, 11, 12]. As the effective device time constant is different during a rising transition (limited by long minority carrier lifetimes) versus a falling transition (limited by series resistance), nonlinear pre-emphasis waveforms are often used [11, 12]. In addition, the device's optical dynamics must be considered in optimizing the pre-emphasis waveforms [13, 14]. The optical bandwidth is limited by the photon lifetime,

which is related to the ring resonator's Q factor, and the ring's phase delay during modulation should be considered to capture the nonlinear optical dynamics. In order to compensate these electrical and optical dynamics, the transmitter circuit must be carefully designed to supply a high-speed pre-emphasis signal with the proper pulse depth, pulse duration, and dc bias. This motivates co-simulation environments with compact optical device simulation models that accurately capture optical and electrical dynamics.

Although previous models have been developed for accumulation-mode [15] and depletion-mode [16] ring modulators, previous models for injection-mode ring devices [8, 17] have lacked accurate modeling of the large-signal p-i-n forward-bias behavior [18] and nonlinear optical dynamics in a format suitable for efficient co-simulation. This section presents a compact Verilog-A model for carrier-injection ring modulators which includes both nonlinear electrical and optical dynamics [19]. The model, which combines an accurate p-i-n electrical [18] and a dynamic ring resonator model [13], will be described and experimentally verified both at 8 Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9 Gb/s with a 65-nm CMOS driver capable of asymmetric pre-emphasis pulse duration.

2.1. Model description

As shown in **Figure 2**, the modeled carrier-injection ring modulator consists of a ring waveguide coupled to a straight waveguide, with p+ and n+ doping in the inner and outer ring regions, respectively. Accurate high-speed modeling requires inclusion of both electrical and optical dynamics, with **Figure 3** showing a flow chart of the model implementation. When a driving voltage is applied, the dynamic current response is determined by a p-i-n diode SPICE model based on a moment-matching approximation of the ambipolar diffusion equation [18]. After obtaining the current dynamics, the total carriers are calculated by integrating this diode current. However, as some of the carriers recombine and remain inside the waveguide during signal transients, only a portion act as free carriers and impact the effective ring index [20]. Utilizing a subsequent high-pass filter with a time constant equal to the carrier lifetime allows extraction of the free carriers used to calculate the ring index and loss changes due to the plasma dispersion effect [21]. Finally, the optical output power is related to the changes in refractive index and absorption coefficient by a dynamic ring resonator model which accurately considers the ring's cumulative phase shift [13].

The electrical SPICE model is described in **Figure 4**. Electrically, the carrier injection ring modulator is treated as a p-i-n diode (**Figure 4(a)**). As shown in **Figure 4(b)**, the total voltage across the device is distributed across the diode's intrinsic region, $V_{epi}(V(10, 12))$, two junctions, $V_j(V(12, 20))$, and the two terminal contact resistances, V_c. The charge, q_0, required for the total current response, is given by modeling the junction characteristics with the applied voltage, V_j, shown in **Figure 4(c)**. In order to accurately model both the dc and dynamic I-V characteristics, the total current I consists of the current injected into the intrinsic region, $I_{epi,}$ and the current due to the anode recombination effect, I_r. As shown in **Figure 4(d)**, I_r is calculated via q_0 and I_{epi} is modeled by a tenth-order network, modified from Ref. [18] for enhanced accuracy. The tenth-order network is designed according to an approximation of the transfer function (the

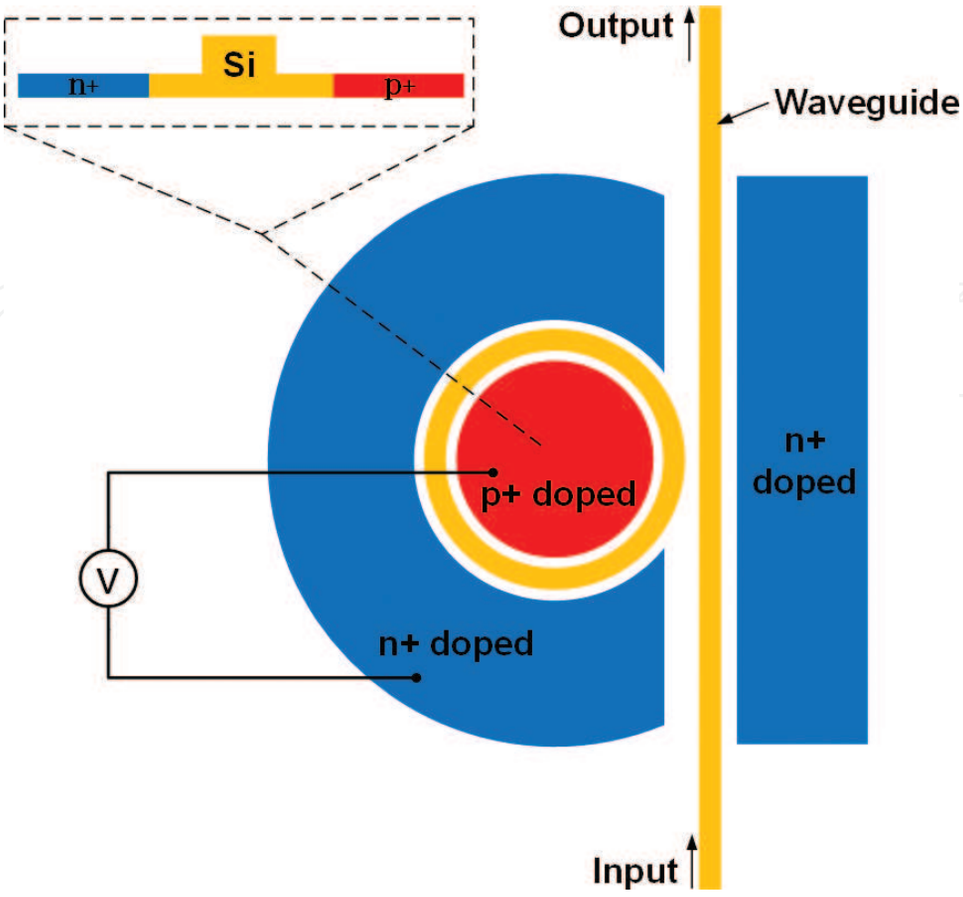

Figure 2. Top and cross-section views of a carrier-injection ring resonator modulator.

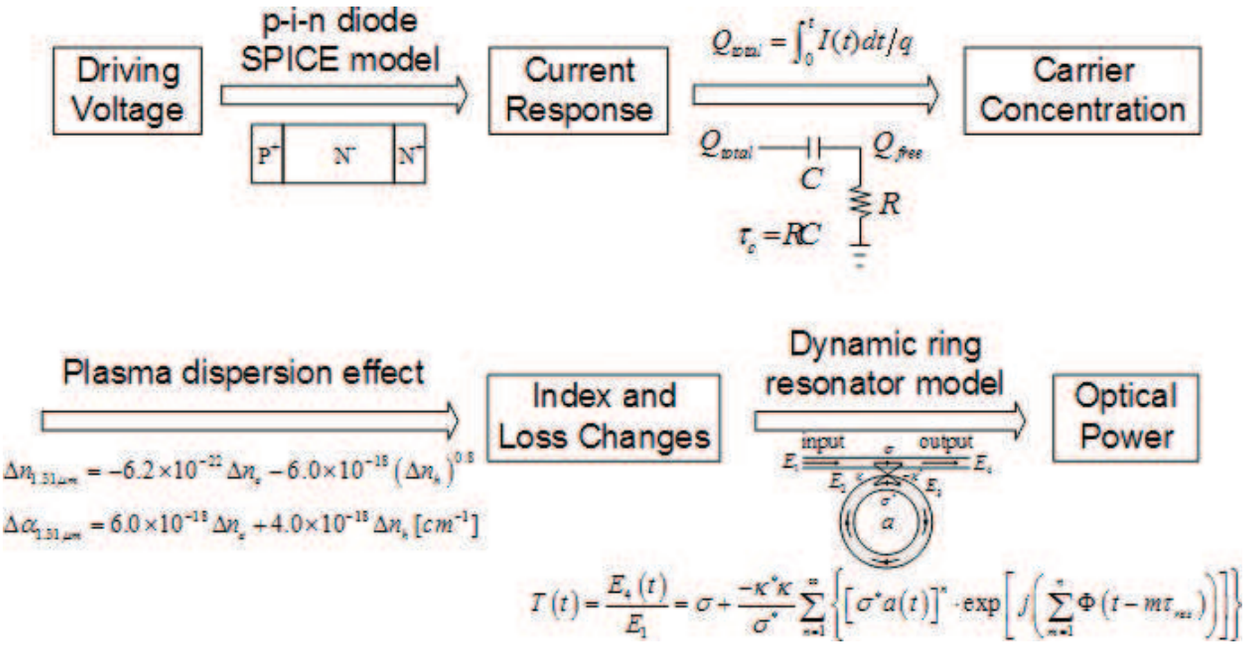

Figure 3. Model flow chart.

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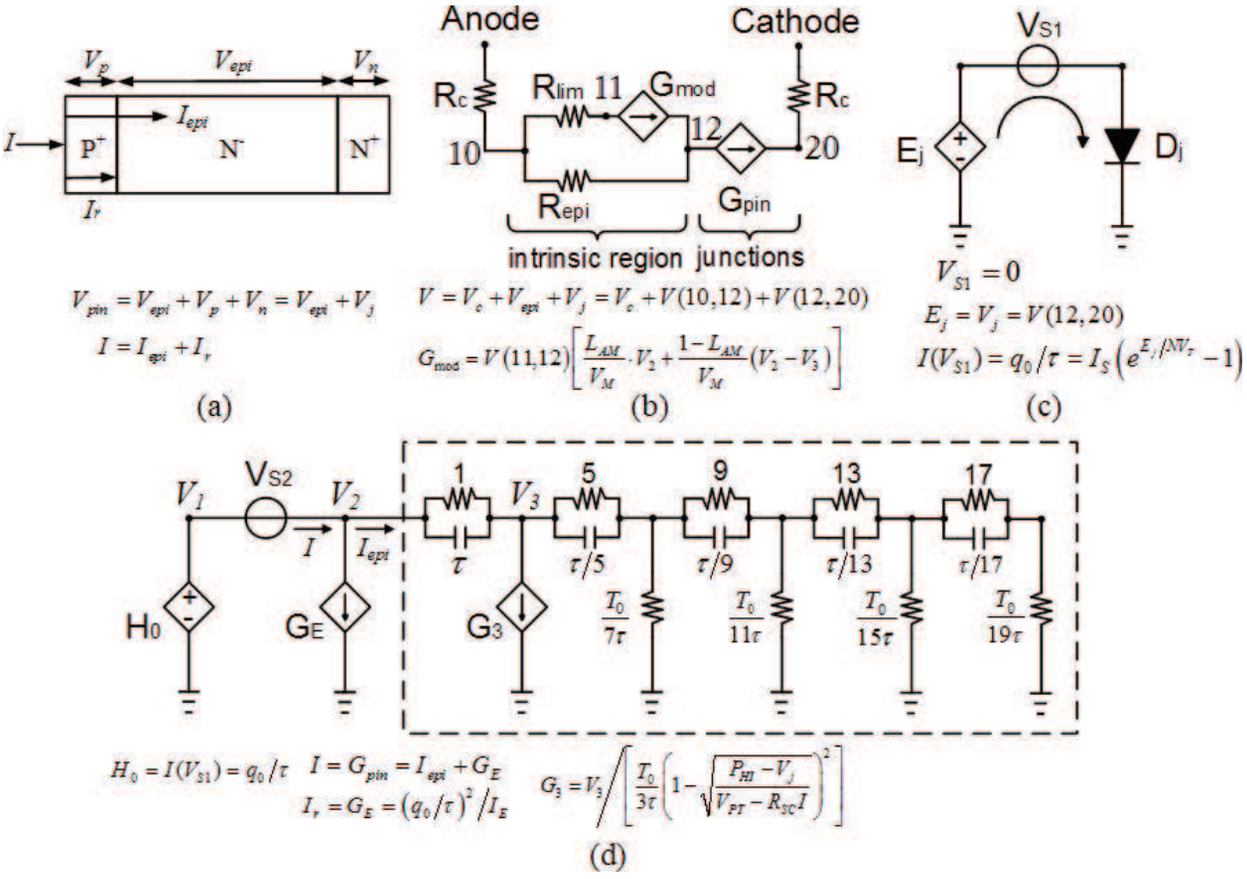

$$V_{pin} = V_{epi} + V_p + V_n = V_{epi} + V_j \qquad I = I_{epi} + I_r$$

$$V = V_o + V_{epi} + V_j = V_o + V(10,12) + V(12,20)$$

$$G_{mod} = V(11,12)\left[\frac{L_{AM}}{V_M}\cdot V_2 + \frac{1-L_{AM}}{V_M}(V_2 - V_3)\right]$$

$$V_{S1} = 0 \qquad E_j = V_j = V(12,20)$$

$$I(V_{S1}) = q_0/\tau = I_S\left(e^{E_j/NV_T} - 1\right)$$

$$H_0 = I(V_{S1}) = q_0/\tau \qquad I = G_{pin} = I_{epi} + G_E$$

$$I_r = G_E = (q_0/\tau)^2/I_E \qquad G_3 = V_3\Big/\left[\frac{T_0}{3\tau}\left(1 - \sqrt{\frac{P_{HI} - V_j}{V_{PT} - R_{SC}I}}\right)^2\right]$$

Figure 4. p-i-n Diode and SPICE model schematic: (a) p-i-n diode cross-section, (b) p-i-n voltage distribution model, (c) junction *I-V* characteristic model, and (d) p-i-n current distribution model. The above model is modified from Ref. [18] with the inclusion of contact resistors and by increasing the current distribution model to tenth-order for increased accuracy.

ratio of the intrinsic region current, I_{epi}, and charge, q_0) via asymptotic waveform evaluation (AWE), which is deducted from the ambipolar diffusion equation [22]. The current through the diode D_j, is equal to q_0/τ, is converted to a voltage via the current-controlled voltage source H_0 to drive a network which models the current dynamics in the intrinsic region. Three important nonlinear effects, described by current sources G_{mod}, G_E, and G_3, are included. G_{mod}, which is a function of $V(11,12)$, represents the conductivity modulation in the intrinsic region, G_E expresses the anode recombination effect, and G_3 implements the moving boundary effect during reverse recovery.

Table 1 summarizes the electrical model parameters and shows values for a 5 μm radius device. The extraction procedure for these parameters is described in **Figure 5**. After initializing the parameters with reasonable empirical values, their values are obtained via curve fitting to dc and high-frequency measurements. Eight of the parameters are extracted from the dc characteristic of **Figure 6(a)**. An iterative process is used to curve fit this data, with high sensitivity parameters R_C, I_S, and N first estimated, followed by the low-sensitivity parameters P_{HI}, I_E, V_M, R_{lim}, and R_{epi} related to the previously mentioned nonlinear effects. In the parameter extraction procedure, current levels above 100 μA are given higher weight in the curve fitting since the model is targeted for optical interconnect applications with NRZ modulation.

Parameter	Unit	Description	Empirical range	Value
R_C	Ω	Contact resistance	10–100	50
I_S	A	Saturation current	$1 \times 10^{-14} - 1 \times 10^{-12}$	5.78×10^{-14}
N	–	Emission coefficient	1–2	1.46
P_{HI}	V	Build-in voltage	0.5–1	0.7
T_0	s	Transit time	1×10^{-10}–1×10^{-9}	1.046×10^{-10}
I_E	A	Emitter recombination knee current	1.0×10^{-4}–1.0×10^{-2}	1.0×10^{-3}
V_M	V	High-injection voltage drop on the base	0–0.5	0.12
R_{lim}	Ω	Carrier-scattering series resistance	1×10^{-3}–3×10^{-3}	1.8×10^{-3}
L_{AM}	–	Forward-recovery coefficient	0–0.1	0.03
τ	s	Carrier lifetime in the base	1.0×10^{-10}–1.0×10^{-8}	1.0×10^{-9}
R_{epi}	Ω	Base region resistance	1.0×10^{2}–1.0×10^{3}	300
V_{PT}	V	Reverse-recovery coefficient	5–20	10
R_{SC}	Ω	Reverse-recovery coefficient	1–100	18

Table 1. Model parameters of the p-i-n diode, with values for a 5 μM device.

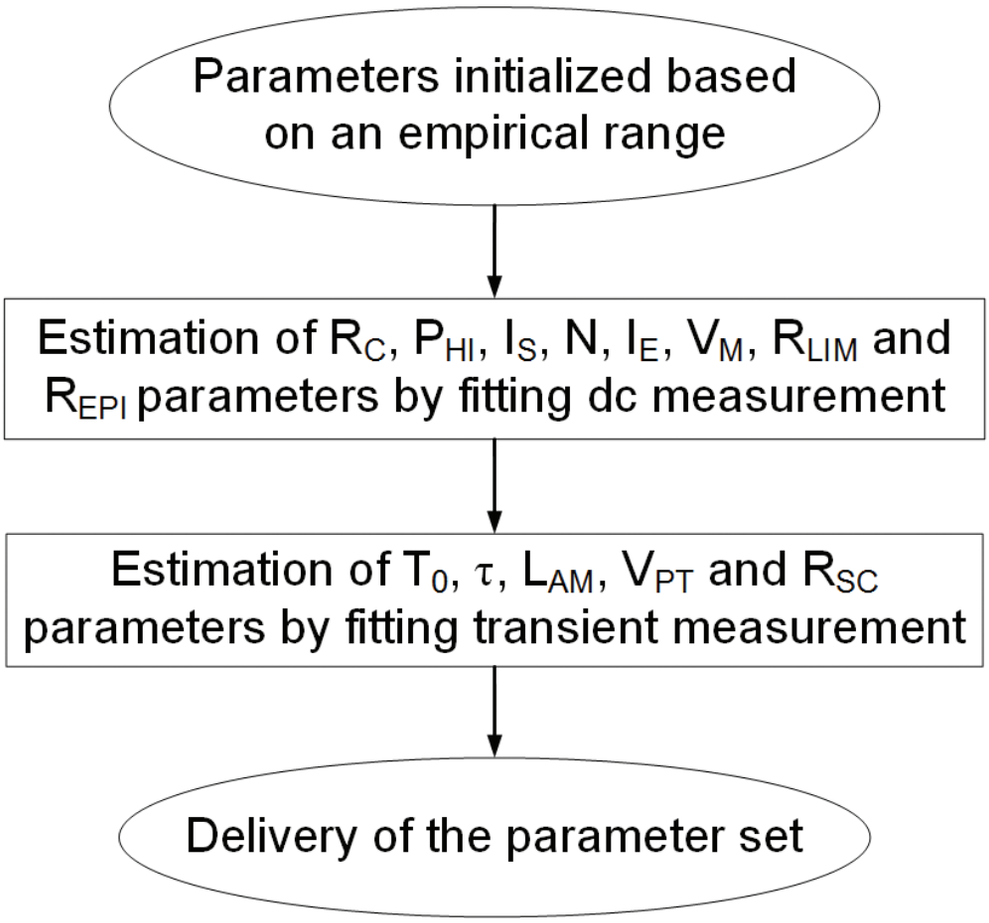

Figure 5. Electrical p-i-n diode parameter extraction procedure.

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As shown in **Figure 6(a)**, excellent matching is achieved at these current levels at the cost of some minor error at low current conditions. The remaining five parameters are extracted from **Figure 6(b)** dynamic current response to a 10 Gb/s clock pattern with a voltage swing between −0.5 and 1.5 V. In a similar manner, high sensitivity parameters T_0 and τ are first estimated, followed by the low-sensitivity parameters L_{AM}, V_{PT}, and R_{SC}. Excellent amplitude matching is achieved between the transient simulation and measured results, implying that the current dynamics are captured well. While there is slightly more harmonic content in the measured results, this small error is not deemed critical for NRZ modulation applications. Overall, utilizing the measured dc *I-V* characteristic and transient response for parameter extraction allows for parameters R_C, I_S, N, P_{HI}, T_0, τ, R_{lim}, and R_{epi} to be well defined, while low-sensitivity parameters I_E, V_M, L_{AM}, V_{PT}, and R_{SC} are more softly defined.

After obtaining the dynamic current response, the total carriers are calculated by integrating the diode current with $Q = \int_0^t I(t)dt/q$. The total carriers consist of the following components [20]:

$$Q_{total}(t) = Q_{remain}(t) + Q_{recombine}(t) + Q_{free}(t), \tag{1}$$

which correspond to carriers remaining in the waveguide during signal transients, Q_{remain}, carriers recombining inside the p-i-n diode, $Q_{recombine}$, and the free carriers, Q_{free}, which impact the effective ring index and loss [21]. As shown in **Figure 7**, the remaining and recombining carriers increase with time, while the free carriers can be extracted utilizing a high-pass filter with a time constant equal to the carrier lifetime. These free carriers are then used to calculate the ring index and loss changes due to the plasma dispersion effect. At a wavelength of 1.31 μm, which is near the resonance wavelength of the devices characterized in this work,

$$\Delta n_{1.31\ \mu m} = -6.2\times10^{-22}\Delta n_e - 6.0\times10^{-18}(\Delta n_h)^{0.8} \tag{2}$$

$$\Delta \alpha_{1.31\ \mu m} = 6.0\times10^{-18}\Delta n_e + 4.0\times10^{-18}\Delta n_h\ [\mathrm{cm}^{-1}], \tag{3}$$

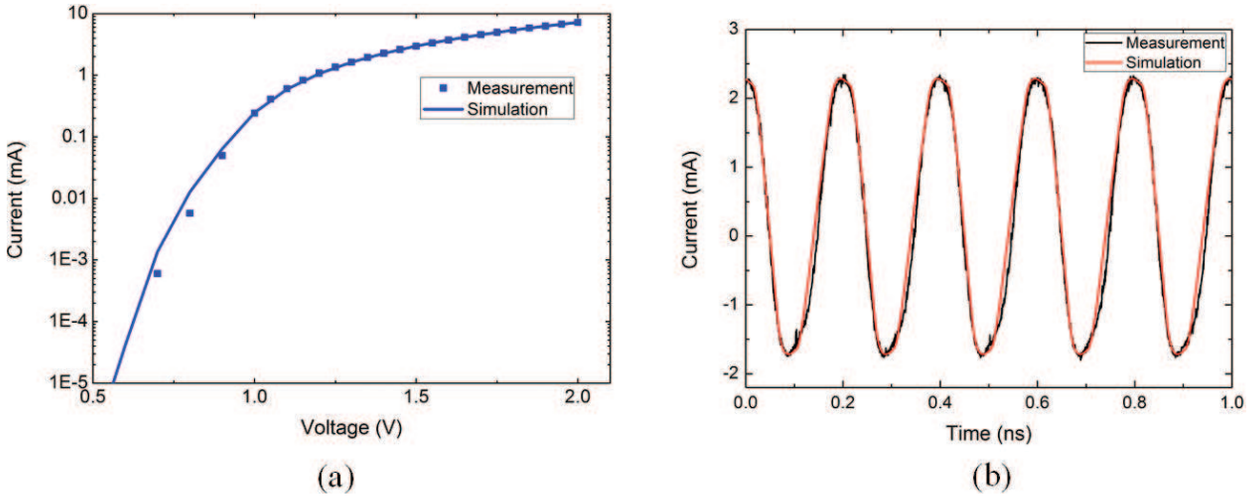

Figure 6. Measured and simulated (a) dc *I-V* characteristic and (b) transient response with a 10 Gb/s clock pattern with voltage swing between −0.5 and 1.5 V.

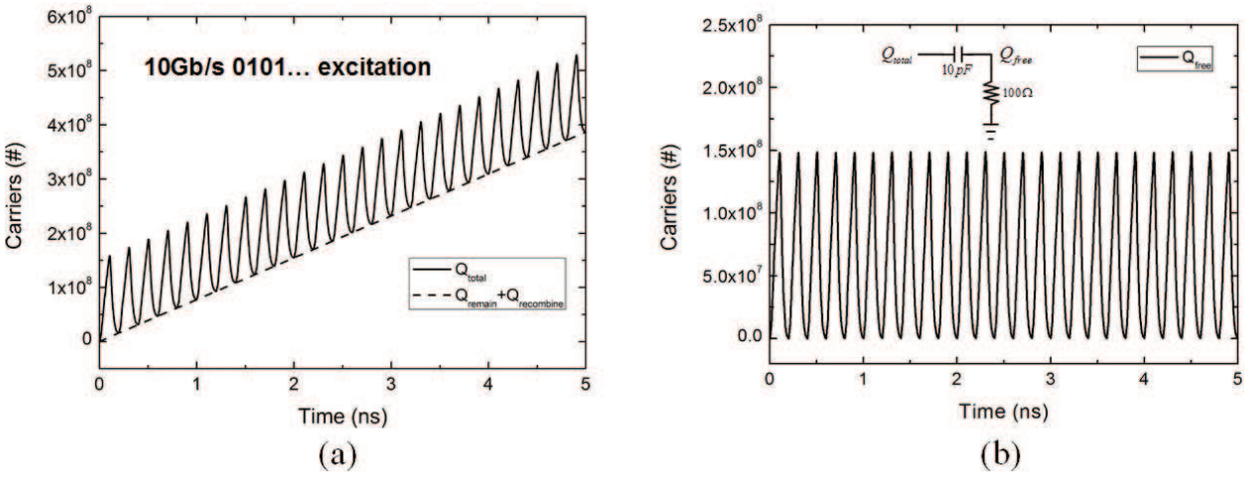

Figure 7. Carriers obtained from the electrical model with a 10 Gb/s clock pattern with voltage swing between −0.5 and 1.5 V: (a) total carriers and (b) free carriers extracted utilizing a high-pass filter with a time constant equal to the carrier lifetime.

where Δn_e and Δn_h are the electron and hole carrier densities [cm^{-3}], respectively. This model assumes $\Delta n_e = \Delta n_h$.

The optical output power is related to the change in refractive index and absorption coefficient by a dynamic ring resonator model which assumes lossless coupling and a single polarization (**Figure 8**). Considering the ring resonator's index dynamics, its time-dependent transmission is described by

$$T(t) = \frac{E_4(t)}{E_1} = \sigma + \frac{-\kappa^* \kappa}{\sigma^*} \sum_{n=1}^{\infty} \left\{ [\sigma^* a(t)]^n \cdot \exp\left[j\left(\sum_{m=1}^{n} \Phi(t - m\tau_{res}) \right) \right] \right\}, \tag{4}$$

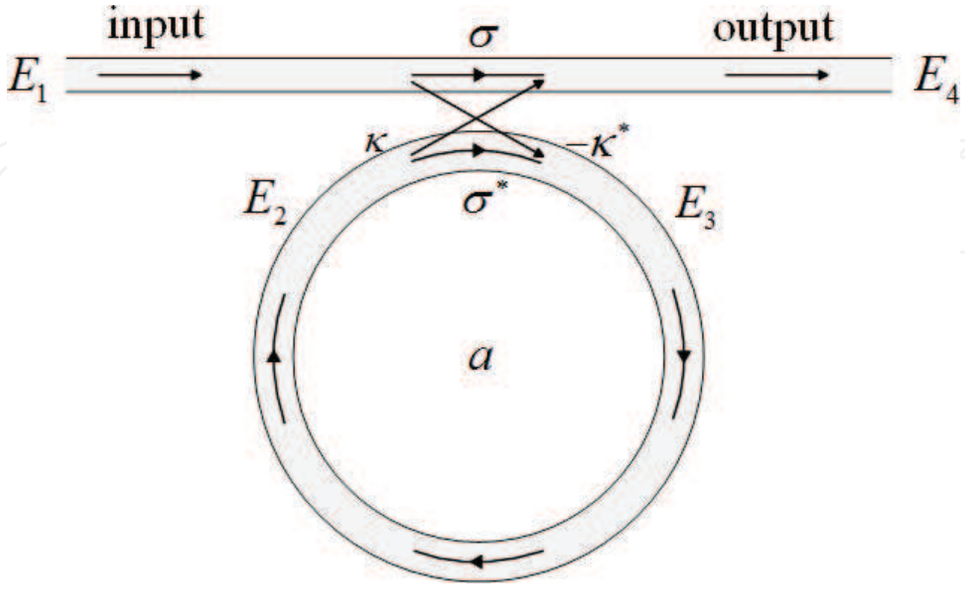

Figure 8. Microring resonator optical model.

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where σ and κ are coupling coefficients, $|\kappa^2| + |\sigma^2| = 1$, a is the ring loss coefficient with zero loss corresponding to $a = 1$ and which relates to the absorption coefficient α as $a^2 = \exp(-\alpha L)$, L is the ring circumference, Φ is phase shift, τ_{res} is the resonator round-trip time, and $|T(t)|^2$ is the optical transmission power [13]. The three critical model parameters such as σ, a, and n_{eff} are extracted by curve fitting the steady-state transmission

$$T(t) = \sigma + \frac{-\kappa^* \kappa}{\sigma^*} \sum_{n=1}^{\infty} \left\{ [\sigma^* a(t)]^n \cdot \exp[jn\Phi(t)] \right\} = \frac{\sigma - a(t) \cdot \exp[j\left(\Phi(t)\right)]}{1 - \sigma^* a(t) \cdot \exp[j\left(\Phi(t)\right)]} \tag{5}$$

where

$$\Phi(t) = \frac{2\pi}{\lambda} n_{eff}(t) L, \tag{6}$$

λ is the optical wavelength and n_{eff} is the effective index. As shown in **Figure 9**, by fitting the measured through port optical spectrum from a 5-μm ring resonator with applied bias

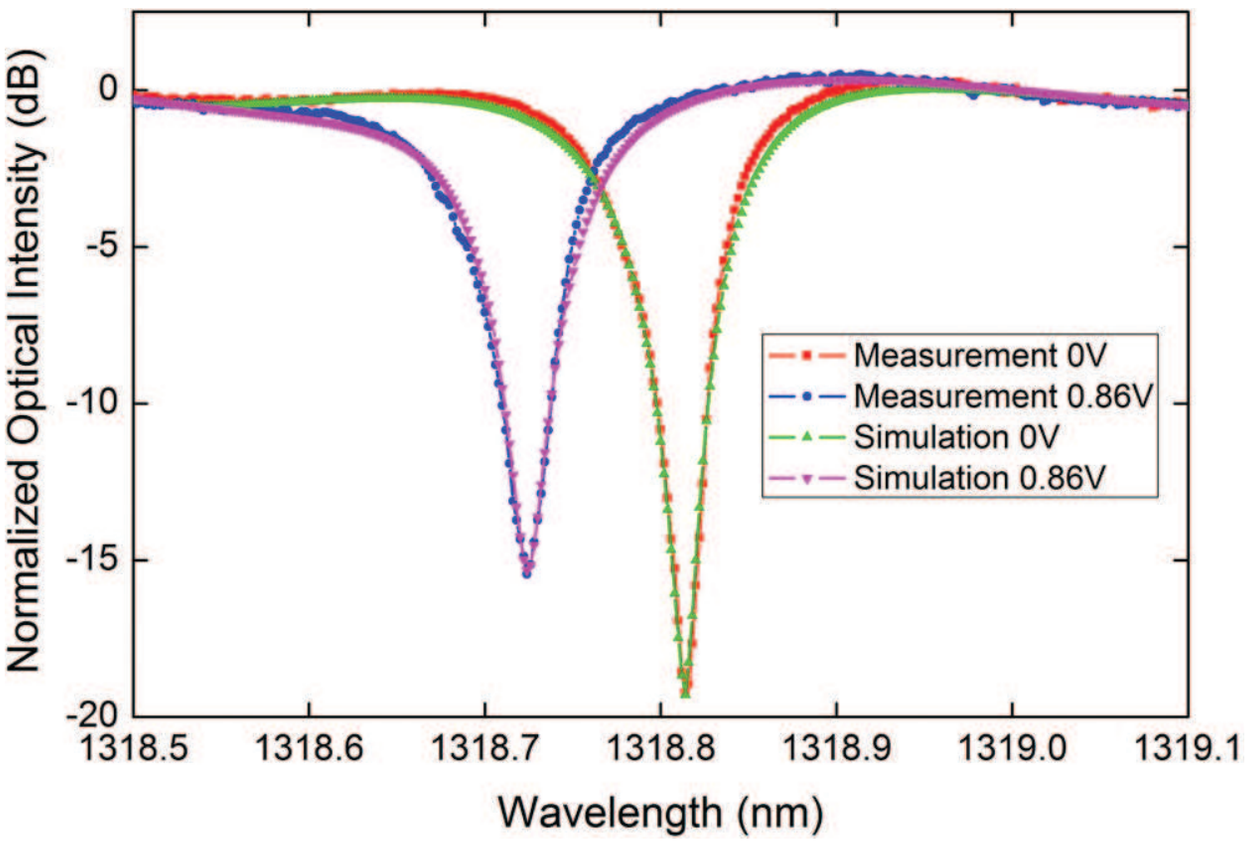

Figure 9. Measured and simulated ring resonator through port optical spectrums. These curves are normalized to the input laser power, accounting for ~10 dB of grating coupler loss.

voltages of 0 and 0.86 V, σ = 0.9944, a = 0.9931, and n_{eff} = 2.5188, are obtained. Utilizing these values in the model described by Eq. (4) allows for excellent matching with measured optical responses with large-signal high-speed modulation.

2.2. Comparison of simulated and measured results

This section presents a comparison of the presented model simulation results with high-speed large-signal measurements. Experimental verification of the model is performed both at 8 Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9 Gb/s with a 65-nm CMOS driver capable of asymmetric pre-emphasis pulse duration.

2.2.1. Symmetric pre-emphasis modulation with external driver

In order to demonstrate the ring modulator model accuracy, comparisons are made with the measured responses of a 5 μm radius carrier-injection ring modulator operating at 8 Gb/s with pre-emphasis modulation. As shown in the experimental setup of **Figure 10**, differential outputs of a high-speed pattern generator are combined to generate a pre-emphasis NRZ drive signal. The impact of pre-emphasis pulse duration, pulse depth, and dc bias is investigated, with a constant 2 Vpp swing maintained as these parameters are varied. Vertical couplers are used to provide light from a CW laser to the ring modulator input port and direct the modulated light out to a fiber connected to an optical oscilloscope for eye diagram generation.

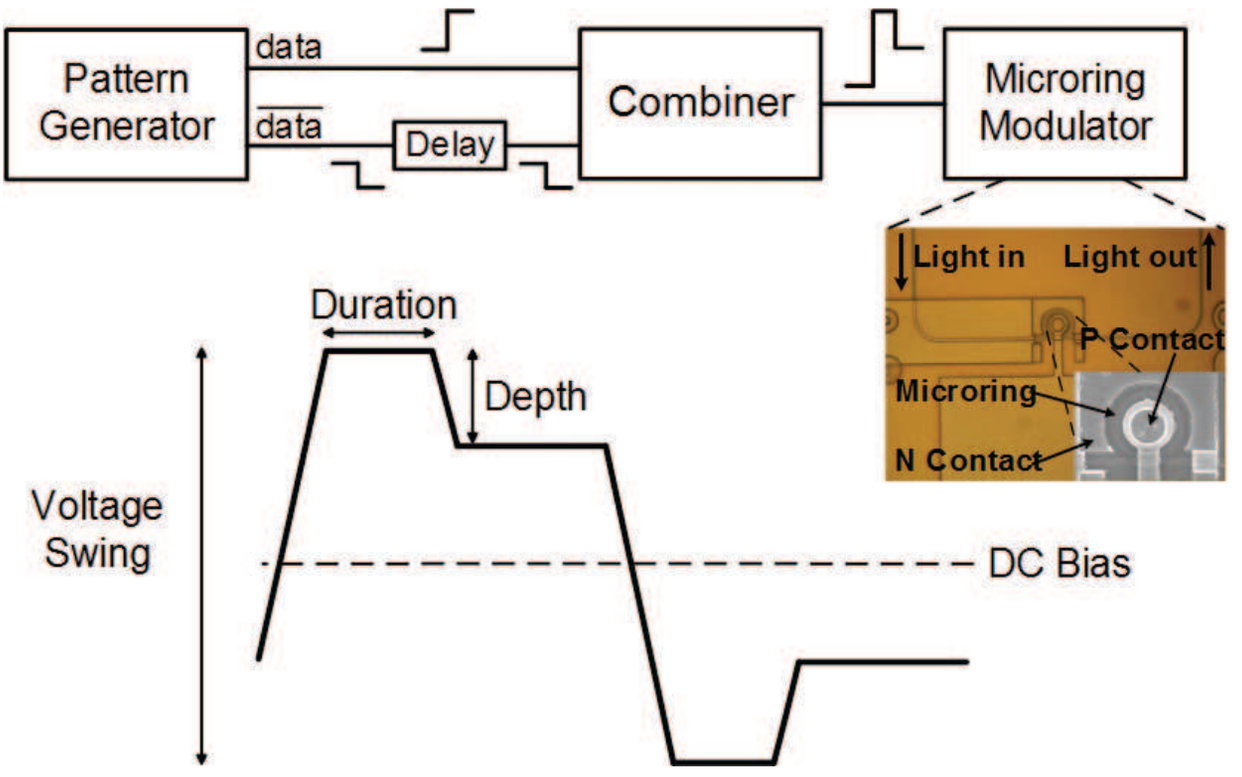

Figure 10. Pre-emphasis NRZ signal generation and waveform.

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In all the measured eye diagrams, the CW laser wavelength is tuned to align with the 0 V ring modulator resonance wavelength. Transition times of 40 ps are used in all the external modeling results, which match the equipment used in the measurements.

As predicted by the proposed ring model, utilizing a simple drive signal that is centered at a 0.7 V bias without pre-emphasis results in a very poor eye diagram with a 2^7–1 PRBS data pattern (**Figure 11**). Here the measured eye is completely closed by the system's random jitter, which is not included in the modeling results. Utilizing an optimal 0.8 V pre-emphasis pulse depth, the impact of pulse duration is shown in **Figure 12**. While a 40 ps duration allows the eye to partially open, the height and width are still degraded due to the long rise time caused by the minority carrier lifetime. Increasing the pulse duration to 80 ps provides optimal eye opening, with excellent matching between the simulated and measured eyes observed.

Relative to the optimal eye diagram of **Figure 12(b)**, **Figure 13** shows how the modeling results correlate with measurements as the pre-emphasis pulse depth is varied. An increase in pulse depth to 0.9 V results in excessive overshoot during a rising transition and slow settling to the steady-stage high level due to the relatively low amount of injected carriers after the pre-emphasis pulse. The model's transfer function does introduce some error in these low-carrier recombination dynamics, which results in some offset in the precise positioning of the falling-edge transitions, both **Figure 13** simulated and measured results show similar significant falling-edge deterministic jitter. A decrease in pulse depth to 0.7 V produces excessive charge for the steady-state high level, which results in slow fall times due to the modulator's series resistance limiting carrier extraction (**Figure 13(b)**).

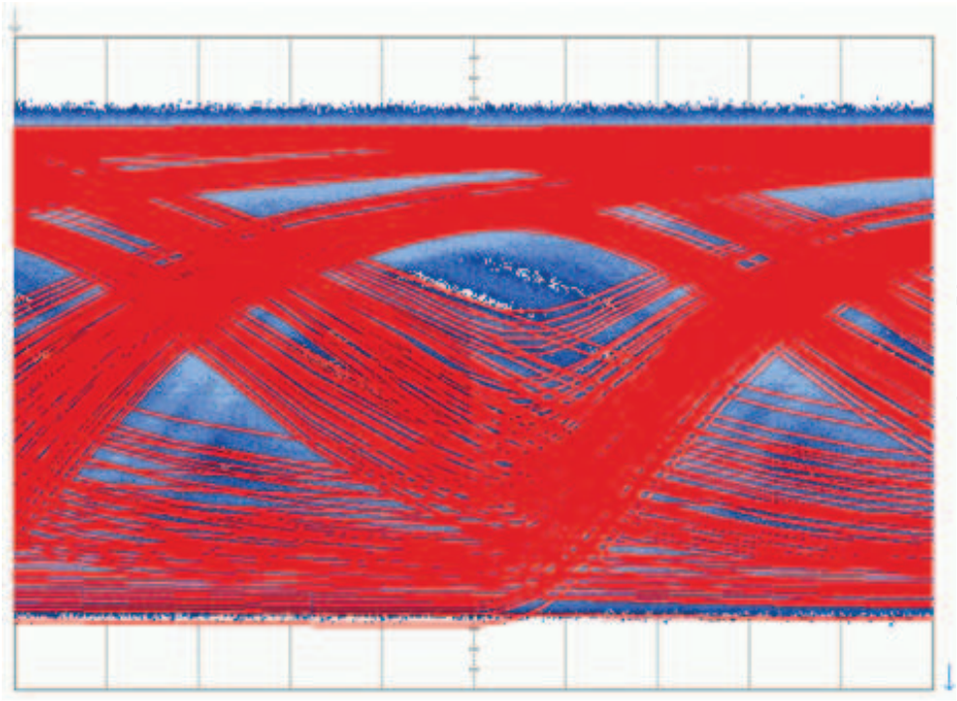

Figure 11. 8 Gb/s measured (blue) and simulated (red) optical eye diagrams with simple NRZ modulation without pre-emphasis [19].

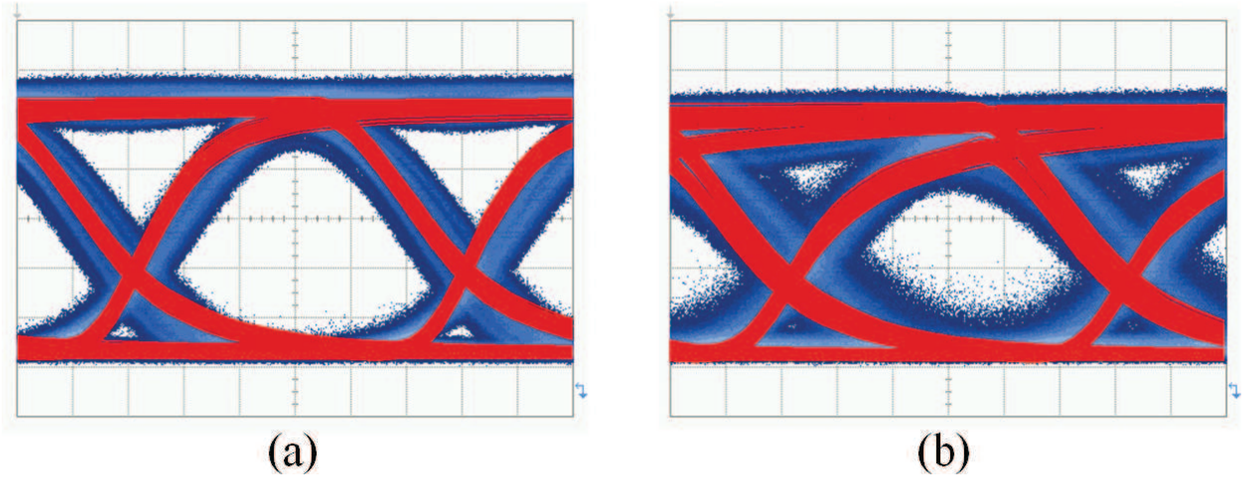

Figure 12. Impact of pre-emphasis pulse duration on 8 Gb/s measured and simulated optical eye diagrams with 0.8 V pulse depth, 0.7 V dc bias, and pulse duration of (a) 40 ps and (b) optimal 80 ps.

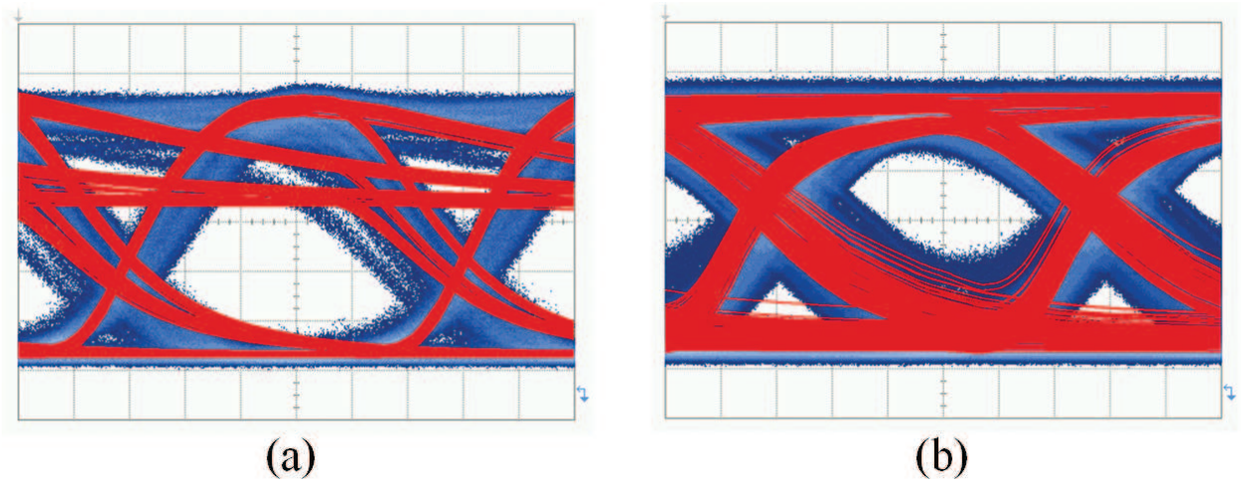

Figure 13. Impact of pre-emphasis pulse depth on 8 Gb/s measured and simulated optical eye diagrams with 80 ps pulse duration, 0.7 V dc bias, and pulse depth of (a) 0.9 V and (b) 0.7 V.

Figure 14 shows the impact of dc bias. As shown in **Figure 14(a)**, an increase in dc bias to 0.75 V produces excessive charge for the steady-state high level which is similar to a decrease in pulse depth to 0.7 V. A decrease in dc bias to 0.65 V results in slower carrier injection and degraded rising transitions (**Figure 14(b)**). Overall, results of **Figures 12–14** show excellent correlation between the proposed ring modulator model and measurements over varying pre-emphasis pulse duration, pulse depth, and dc bias.

2.2.2. Asymmetric pre-emphasis modulation with CMOS driver

A key objective of the model is to enable an opto-electronic co-simulation environment which allows for both the optimization of transceiver circuitry and the ability to study the impact of optical device parameters. The co-simulation capabilities are demonstrated by comparing simulated modeling results with the measured responses of the 5 μm radius carrier-injection

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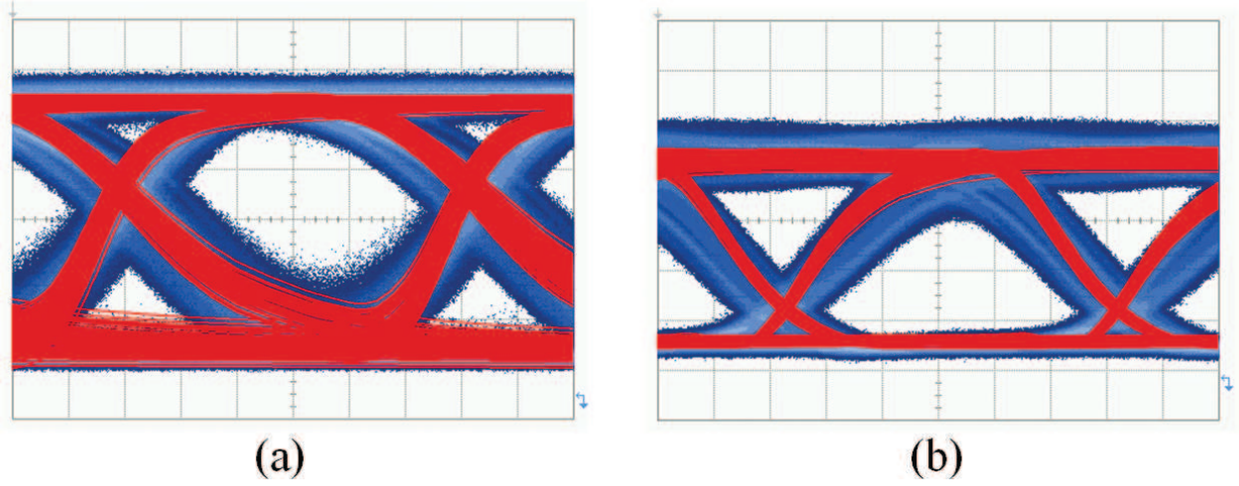

Figure 14. Impact of pre-emphasis dc bias on 8 Gb/s measured and simulated optical eye diagrams with 80 ps pulse duration, 0.8 V pulse depth, and dc bias of (a) 0.75 V and (b) 0.65 V.

ring modulator driven with a custom-designed CMOS driver. As shown in hybrid-integrated prototype in **Figure 15**, the pre-emphasis NRZ driver implemented in a 65-nm CMOS technology [12] is wire-bonded both to the PCB and the silicon ring modulator for testing. While the pre-emphasis pulse depth is fixed in this CMOS driver implementation, the prototype does have the ability to adjust the dc bias and the pre-emphasis pulse duration in an asymmetric manner for independent optimization of the rising and falling responses.

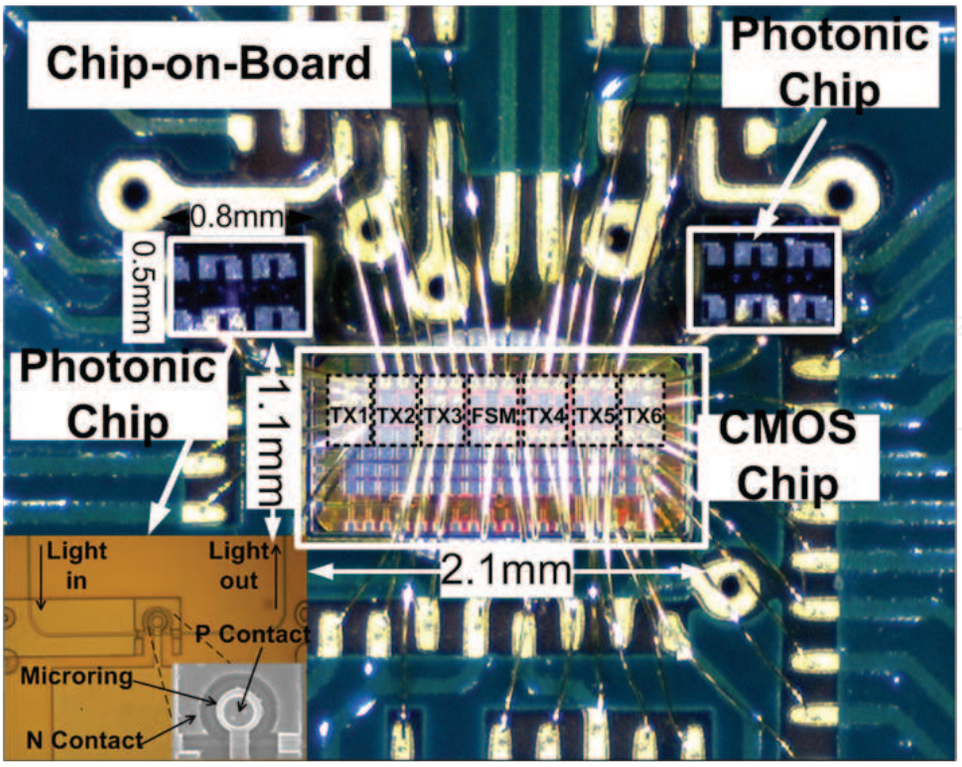

Figure 15. Hybrid-integrated optical transmitter prototype bonded for optical testing.

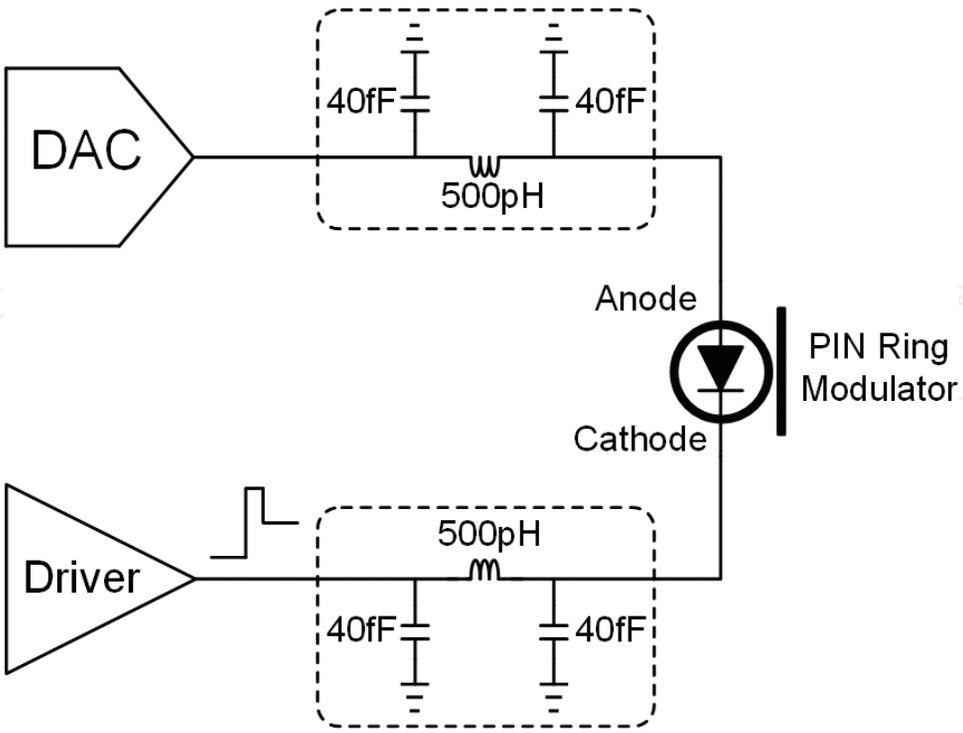

Figure 16. Co-simulation schematic with 65-nm CMOS high-speed CMOS driver, bias DAC, and Verilog-A carrier-injection ring resonator modulator model.

Figure 16 shows the co-simulation schematic in a CADENCE environment, with transistor-level schematics for the high-speed driver and bias digital-to-analog converter (DAC), lumped elements for the wirebond interconnect, and the Verilog-A carrier-injection ring resonator

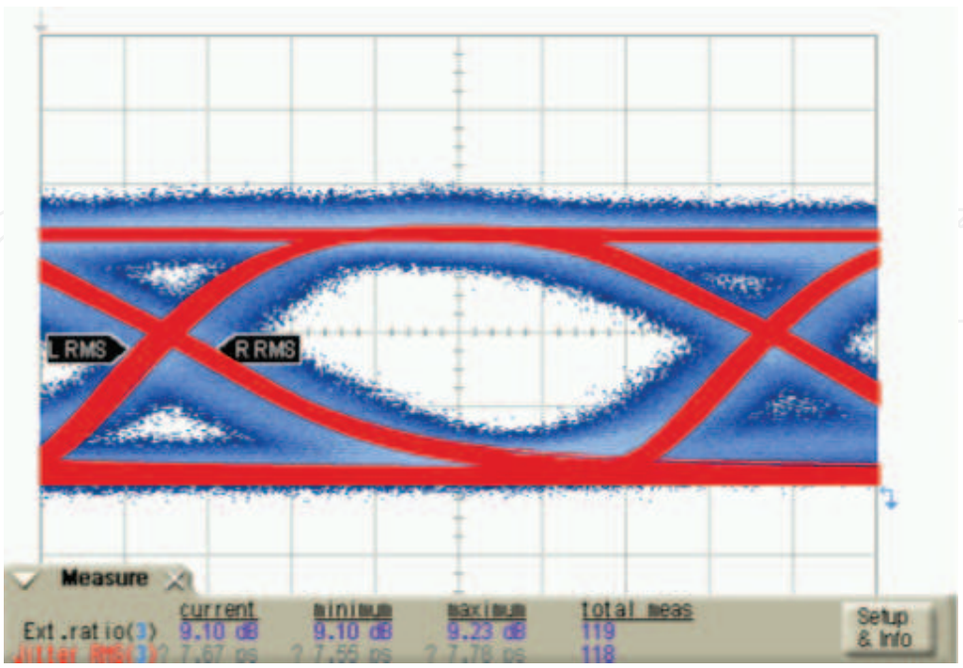

Figure 17. 9 Gb/s measured and co-simulated optical eye diagrams with the ring resonator modulator driven by the 65-nm CMOS driver.

modulator model. The single-ended driver provides a high-speed 2 Vpp output swing with independent dual-edge pre-emphasis duration tuning on the cathode of the ring modulator, while the 9-bit bias tuning DAC is connected to the anode for dc bias adjustment [12]. 500 pH inductors are used to model the ~0.5 mm bondwires that connect the high-speed driver and DAC to the modulator, while 40 fF capacitors model the chips' bondpads. **Figure 17** shows that the optimal 9 Gb/s measured and co-simulated eye diagrams, balancing extinction ratio and eye opening, are achieved when the anode bias is 1.45 V and asymmetric pulse durations for rising and falling transitions are 70 and 50 ps, respectively.

3. Silicon carrier-depletion ring modulator model

For carrier-injection ring modulators, large modulation depth and efficiency are achieved at the cost of relative low modulation bandwidth [12]. It limits application in ultra-high speed data communication. In contrast, carrier-depletion modulators have higher modulation speed ~40 Gb/s. A 320 Gb/s eight-channel WDM transmitter based on carrier-depletion ring modulators was demonstrated in Ref. [9]. The modulation speed of carrier-depletion ring modulators is limited by electrical bandwidth and optical bandwidth. The electrical bandwidth is determined by the RC bandwidth of the ring modulator where the voltage-controlled capacitance results in a nonlinear frequency response with a large voltage swing. The optical bandwidth is limited by photon lifetime related to the Q factor of ring resonators where the time rate of change in ring energy during modulation indicates nonlinear optical dynamics [23]. Therefore, an accurate carrier-depletion ring modulator model is essential to optimize transmitter circuitry while ring modulator models in Refs. [15, 16, 24, 25] did not demonstrate both nonlinear electrical dynamics and optical dynamics.

To design and optimize an optical interconnect transceiver circuitry, an accurate co-simulation environment is required for low-power and high-bandwidth operation. Photonic device models developed in Verilog-A provide the advantage of model compatibility with commercial SPICE circuit simulators. This section presents a Verilog-A carrier-depletion ring modulator model including nonlinear electrical and optical dynamics which provides a co-simulation environment for optical interconnect systems design. The model will be described and verified at 25 Gb/s with a 65-nm CMOS driver capable of asymmetric equalization.

3.1. Model description

The structure of the carrier-depletion ring modulator is shown in **Figure 18**. It consists of a rib waveguide of 500 nm width, 220 nm height, and 90 nm slab height coupled to a ring waveguide with radius of 7.5 μm, p-n junctions formed with outer p+ and inner n+-type doping with doping level near 2×10^{18} cm^{-3} on approximately 75% of the ring waveguide, p++ and n++-type doping utilized for ohmic contact formation, and an integrated heater with 550 Ω resistance formed by doping 15% of the ring with n+-type doping [26]. The ring modulator was fabricated at the IME A*STAR Singapore through OpSIS.

The proposed carrier-depletion ring modulator model is shown in **Figure 19**. The left side is the circuit model in which the electrical bandwidth is dominantly limited by resistances from

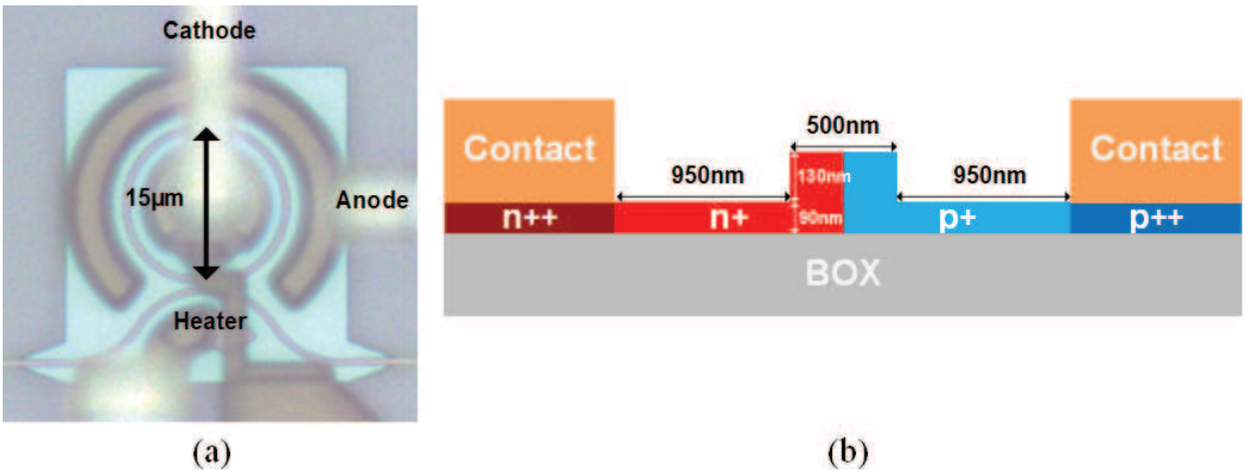

Figure 18. (a) Die photo and (b) cross-section view of carrier-depletion ring modulators.

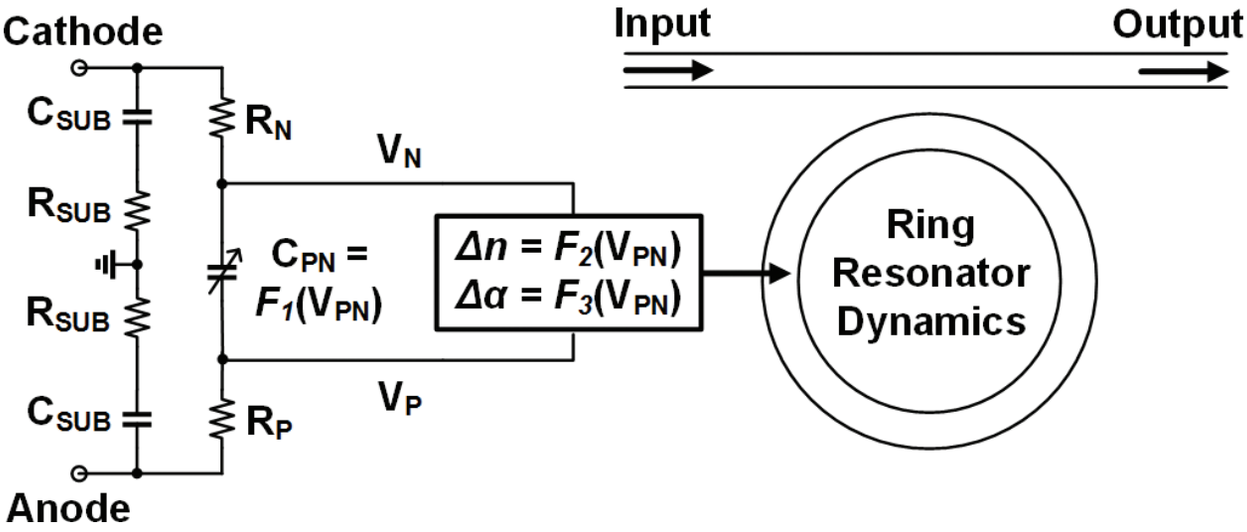

Figure 19. Carrier-depletion ring modulator model.

the electrodes to the junction and capacitance. The right side is the dynamic ring resonator model, and it is related to circuit model by functions of refractive index and absorption coefficient changes versus voltage drop on the junction. By fitting S11 parameter of the device, C_{sub} is 2.5 fF, R_{sub} is 750 Ω-cm, C_{pn} with no bias voltage is 25 fF, and R_p and R_n are 30 Ω [9]. Extracting the devices' carrier densities versus applied voltage with Lumerical allows calculation of the refractive index, n, and absorption coefficient, α, changes by the plasma dispersion effect [21], which for a $\lambda = 1.55$ μm input wavelength are formulated as

$$\Delta n_{1.55\ \mu m} = -8.8\times10^{-22}\Delta n_e - 8.5\times10^{-18}(\Delta n_h)^{0.8} \tag{7}$$

$$\Delta\alpha_{1.55\ \mu m} = 8.5\times10^{-18}\Delta n_e + 6.0\times10^{-18}\Delta n_h\ [\mathrm{cm}^{-1}], \tag{8}$$

Figure 20 shows how the single phase shifter ring modulator's effective index, absorption coefficient changes, and junction capacitance change versus applied reverse-bias voltage

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where $C = \Delta Q/\Delta V$. By curve fitting **Figure 20**, the three parameters Δn, $\Delta\alpha$, and C are then extracted as a polynomial function of voltage.

$$f(V) = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + a_4 V^4 \tag{9}$$

Table 2 gives the a_0-a_4 coefficients, where the valid voltage range is 0–5 V.

The dynamic optical output power is related to the changes in refractive index and absorption coefficient by a ring resonator modeling [23]:

$$\frac{\partial A}{\partial t} = \left(2\pi cj\left(\frac{1}{\lambda} - \frac{1}{\lambda_0}\right) - \frac{1}{\tau}\right)A + j\mu S_i \tag{10}$$

$$S_o = S_i + j\mu A, \tag{11}$$

where $1/\tau = 1/\tau_c + 1/\tau_l$ is an amplitude decay time constant associated with power coupling to bus waveguide τ_c and power lost due to absorption and scattering τ_l, c is light velocity, λ is laser wavelength, λ_0 is the ring resonant wavelength, A is the energy stored in the ring, μ is the mutual coupling between the ring and the bus waveguide, and S_i and S_o are incident and transmitted waves. The coupling factor μ satisfies $\mu^2 = \kappa^2 v_g/2\pi R = 2/\tau_c$, where κ is the coupling ratio, v_g is the ring group velocity, and R is the radius of the ring. The circuit model and ring resonator model are related by $2\pi(n_0 + \Delta n)R = m\lambda_0$ and $\tau_l = 1/\left(v_g exp\left((\alpha_0 + 0.75\Delta\alpha)2\pi R\right)\right)$, where ring effective index with no bias is ~2.57 and ring group index is ~3.89 extracted from Lumerical simulation, and the mode number m = 28 when R = 7.5 μm and λ = 1552.3 nm. By fitting the measured optical spectrum through port applied with reverse bias 0 and 4 V shown in **Figure 21**, three

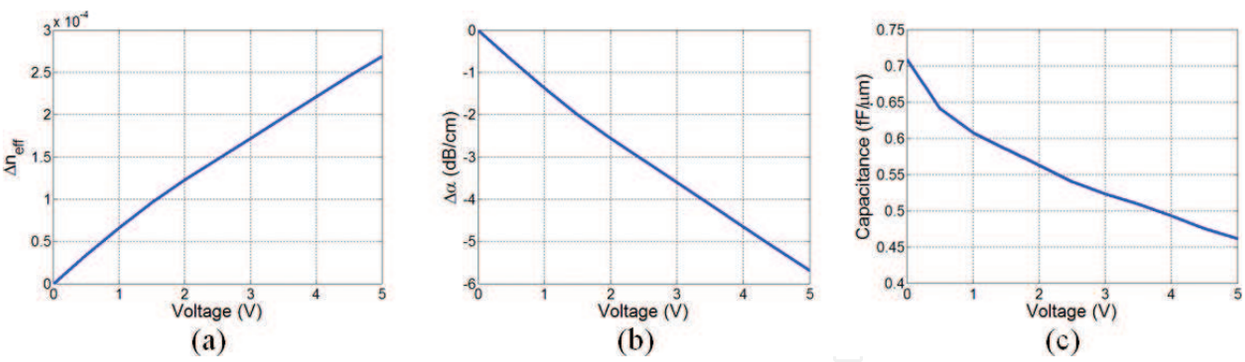

Figure 20. (a) The change of refractive index, (b) the change of absorption coefficient, and (c) the junction capacitance versus applied reverse-bias voltage.

Parameter	Unit	a_0	a_1	a_2	a_3	a_4
Δn_{eff}	–	-4.3×10^{-7}	7.3×10^{-5}	8.0×10^{-6}	1.1×10^{-6}	5.2×10^{-8}
$\Delta\alpha$	dB/cm	0.01	1.5	0.17	-2.3×10^{-2}	1.0×10^{-3}
C	fF/μm	0.71	−0.14	5.5×10^{-2}	-1.2×10^{-2}	1.0×10^{-3}

Table 2. Polynomial coefficients of Δn_{eff}, $\Delta\alpha$, and C.

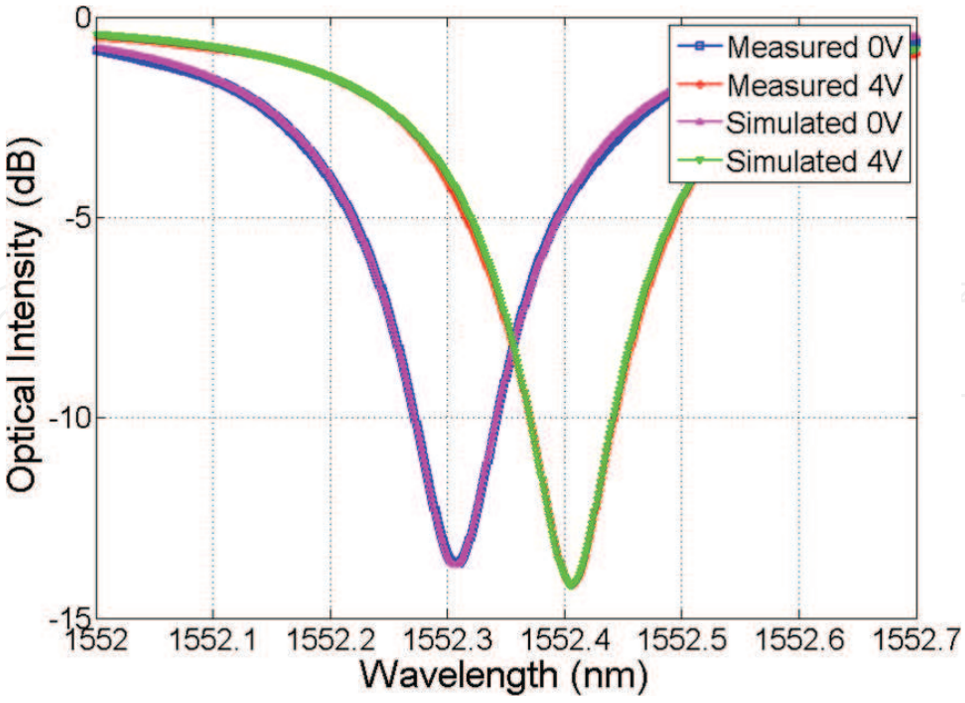

Figure 21. Measured and simulated optical spectrum at through port.

parameters of the model, τ = 9.07 ps, κ^2 = 0.0354, and n_0 = 2.5694, are obtained. The laser wavelength is set to be the resonant wavelength of the ring resonator at 1552.31 nm to maximize the extinction ratio (ER) for NRZ modulation.

3.2. Comparison of simulated and measured results

A key objective of the model is to enable an opto-electronic co-simulation environment which allows for both the optimization of transceiver circuitry and the ability to study the impact of optical device parameters. The co-simulation capabilities are demonstrated by comparing simulated modeling results with the measured responses of the 7.5 μm radius carrier-depletion ring modulator driven with a custom-designed CMOS driver. As shown in hybrid-integrated prototype in **Figure 22**, the AC-coupled differential driver implemented in a 65-nm CMOS technology [27] is wire-bonded both to the PCB and the silicon ring modulator for testing. The prototype has the ability to adjust the equalization to optimize high data rate performance.

Figure 23 shows the co-simulation schematic in a CADENCE environment, with transistor-level schematics for the high-speed differential driver, lumped elements for the wirebond interconnect, and the Verilog-A carrier-depletion ring resonator modulator model. The differential driver provides a high-speed 4.4 Vpp output swing with an asymmetrical feed-forward equalizer (FFE) to compensate the device nonlinearity [27]. 500 pH inductors are used to model the ~0.5 mm bondwires that connect the high-speed differential driver to the modulator, while 40 fF capacitors model the chips' bondpads.

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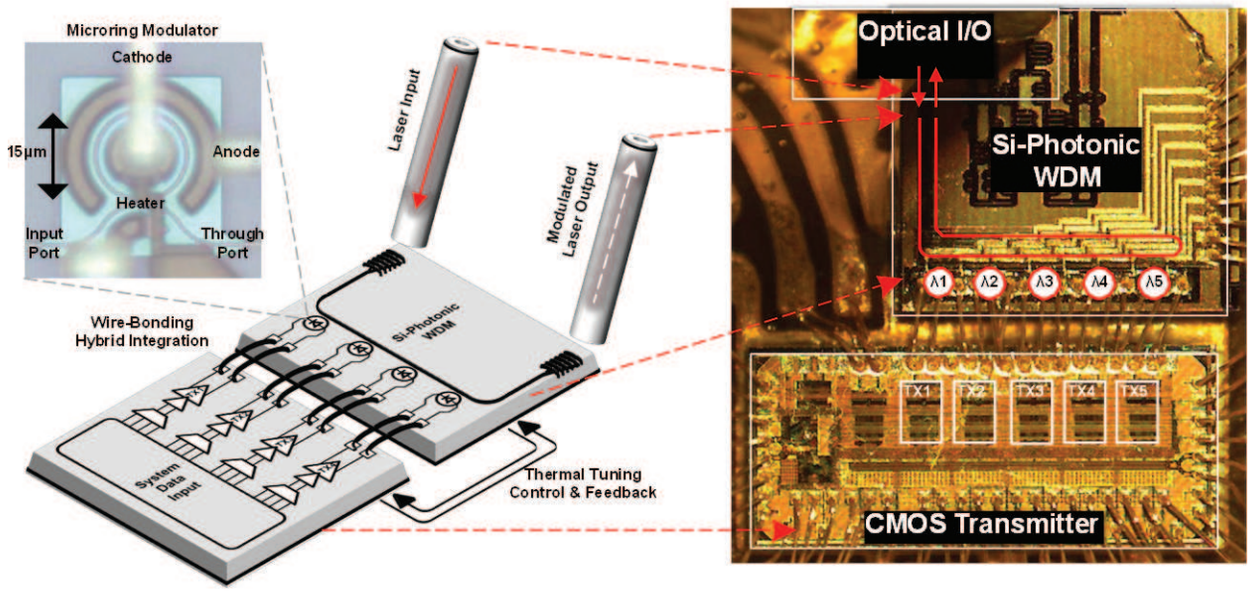

Figure 22. Optical transmitter prototype assembly.

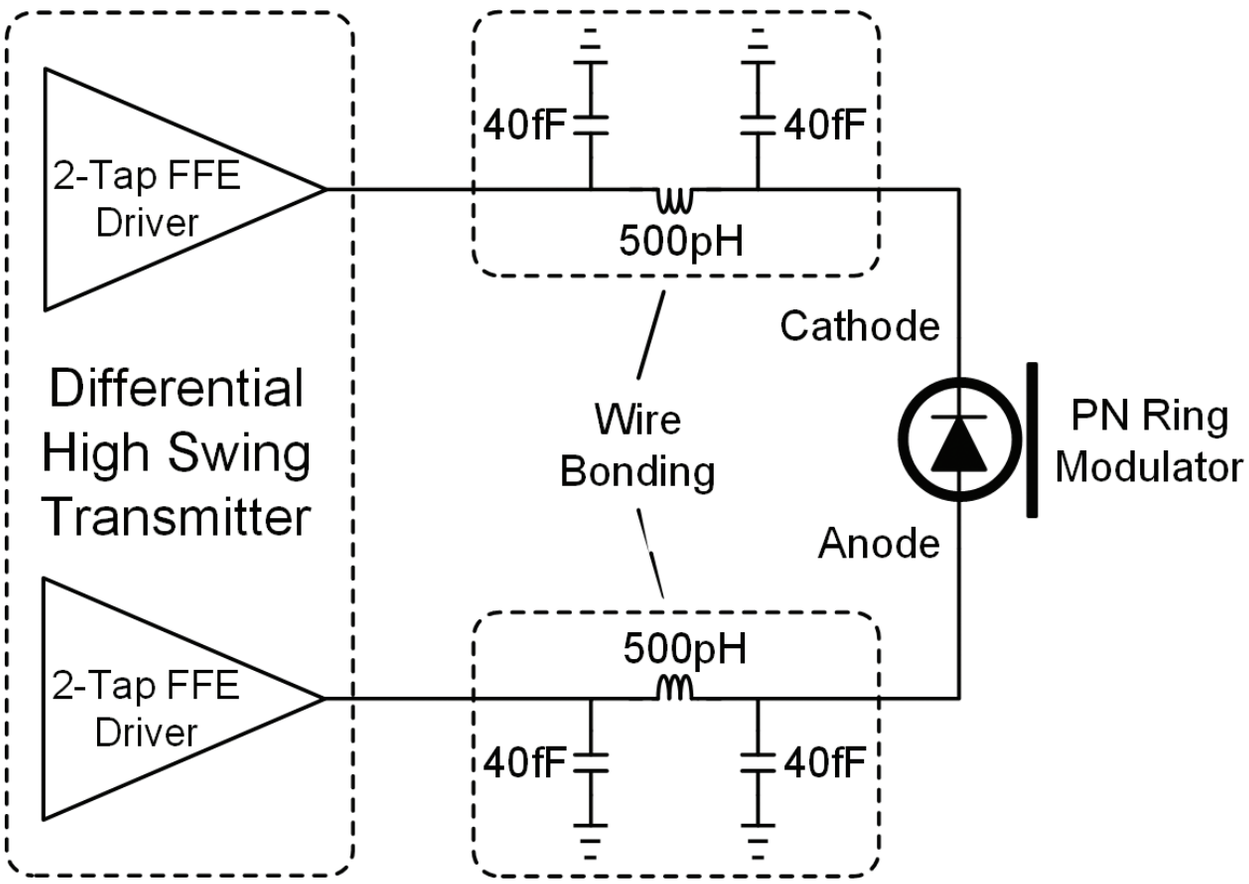

Figure 23. Co-simulation schematic with 65-nm high-speed differential CMOS driver and carrier-depletion ring resonator modulator model.

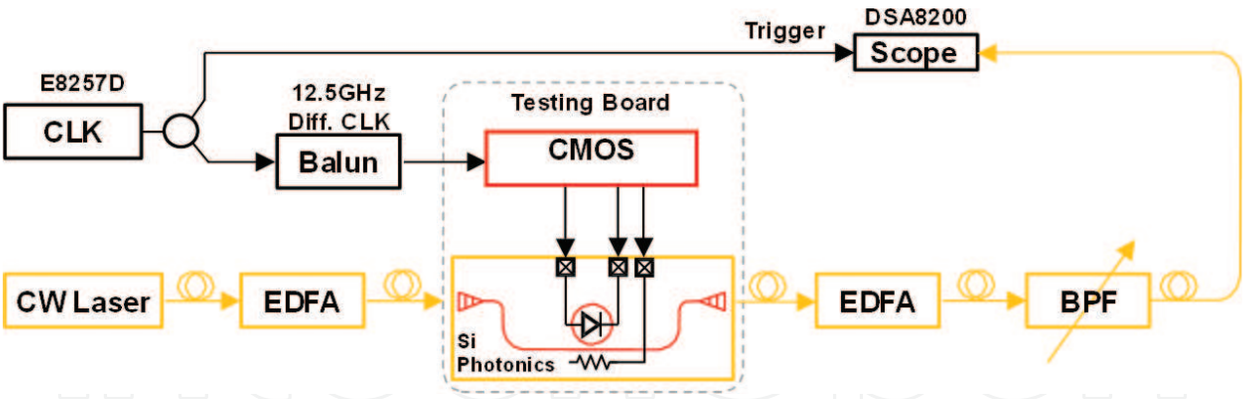

Figure 24. Experimental setup for optical testing.

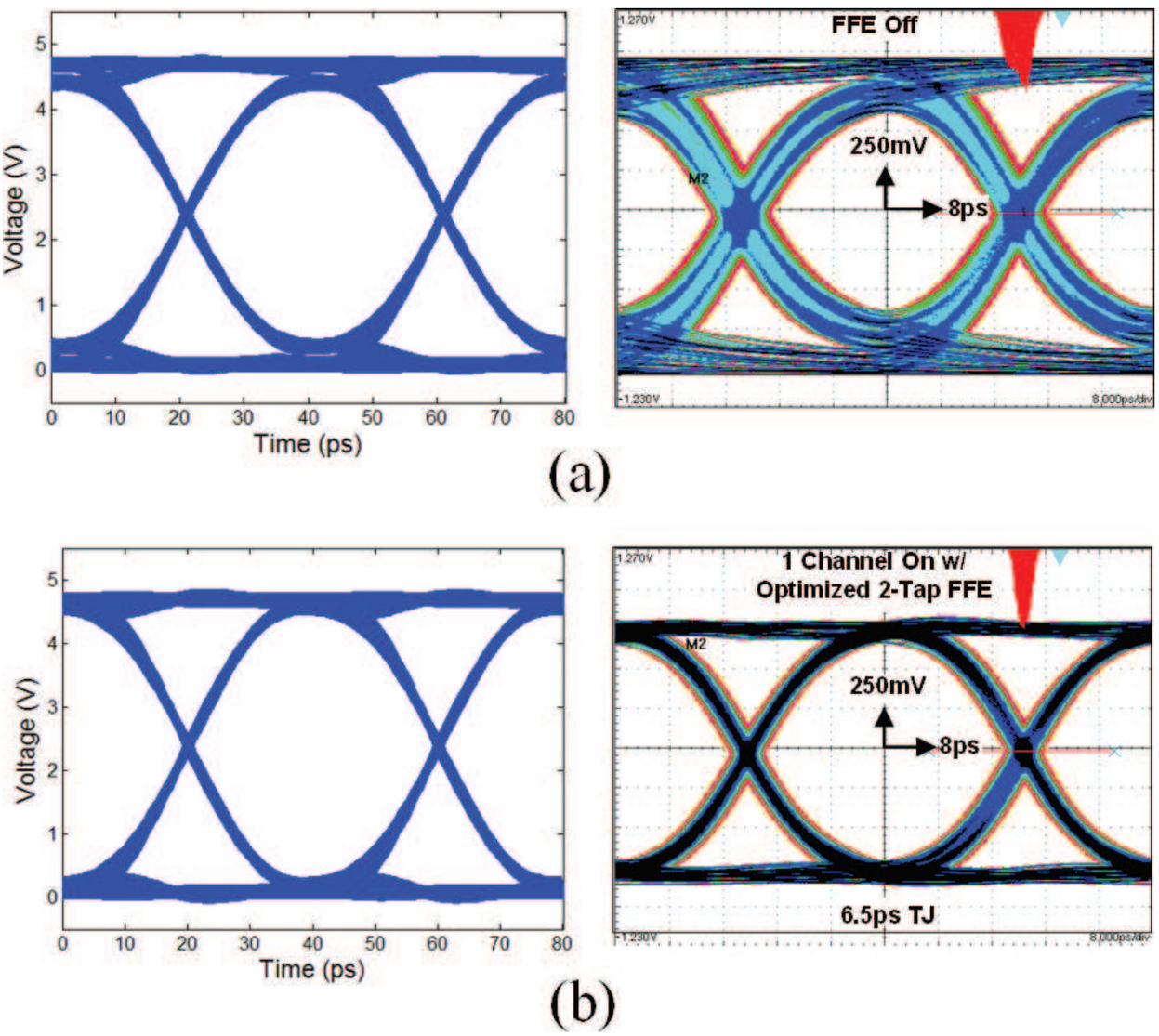

Figure 25. Measured and simulated 25 Gb/s electrical input eye diagrams (a) without equalization and (a) with optimized symmetric equalization.

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For model verification, 25 Gb/s measured and simulated eye diagrams are compared. The experimental setup is shown in **Figure 24**. The optical output from the CW laser is amplified by two erbium-doped fiber amplifiers (EDFAs) before and after the photonic chip to compensate input and output insertion losses due to the fiber-to-grating coupler coupling. A bandpass filter is utilized after EDFAs to suppress the amplified noise to increase the signal-to-noise ratio. A clock is utilized for a trigger of an oscilloscope and the input of the CMOS driver. The optical output is received by the oscilloscope.

Figure 25 shows the 25 Gb/s 2^7–1 PRBS CMOS driver signal for model simulation, which matches excellent with the measured eye diagrams including without equalization (**Figure 25(a)**) and with optimized symmetric equalization (**Figure 25(b)**). As shown in the 25 Gb/s eye diagrams of **Figure 26**, excellent matching is achieved between the measured and co-simulated results with and without equalizations. Due to the device bandwidth limitation and nonlinearity, the optical output power is distorted with an unequal amount of inter-symbol-interference (ISI) (**Figure 26 (a)**), which degrades the effective extinction ratio (ER). As shown in **Figure 26(b)**, this asymmetrical ISI is compensated by an optimized nonlinear equalizer.

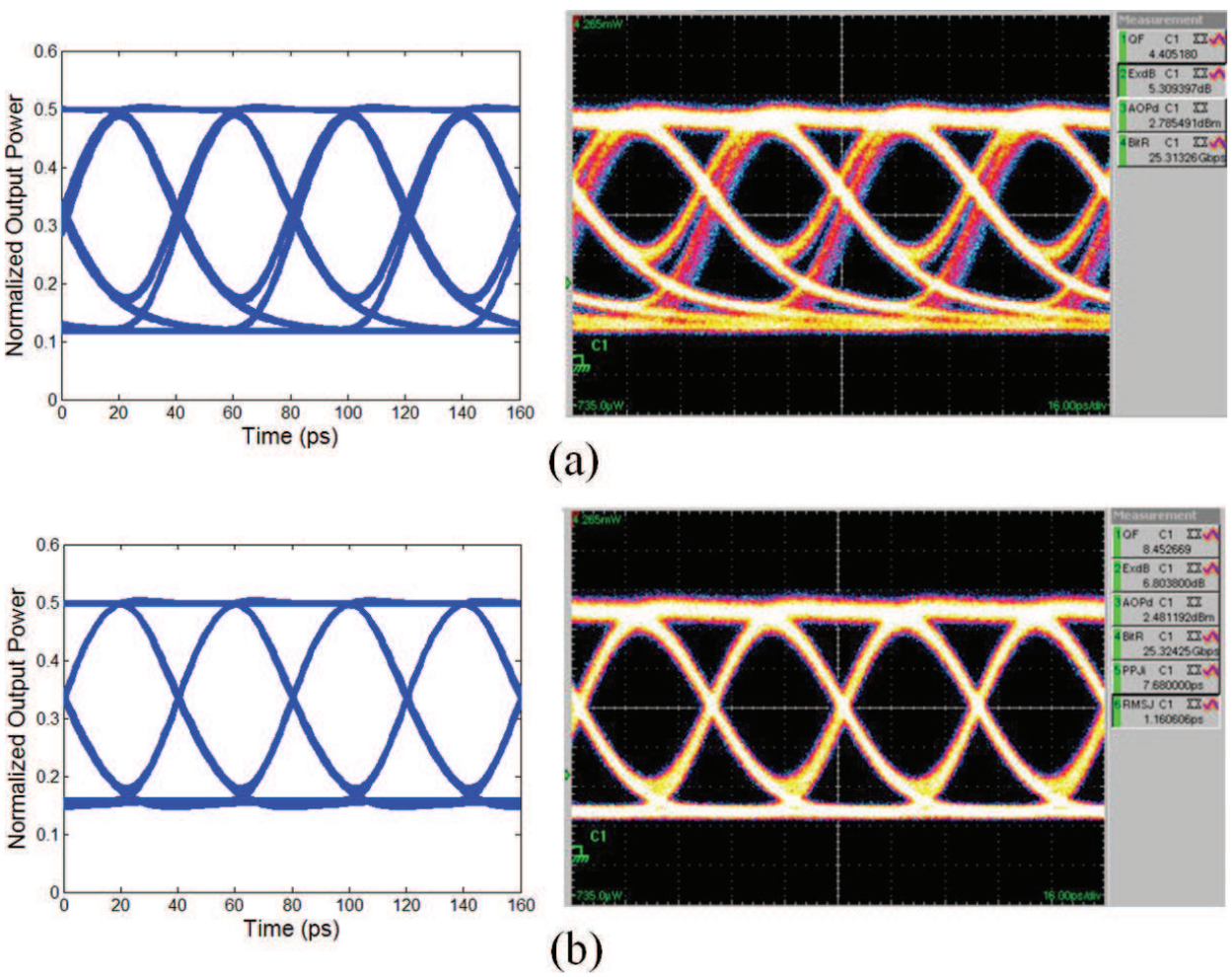

Figure 26. Measured and co-simulated 25 Gb/s optical output eye diagrams (a) without equalization and (b) with the same optimized asymmetric equalization.

4. Conclusions

Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating accurate co-simulation environments. The presented compact Verilog-A models for carrier-injection and carrier-depletion ring modulators include both nonlinear electrical and optical dynamics, allowing for efficient optimization of transmitter signal levels and equalization settings. For the model of carrier-injection microring modulators, excellent matching between simulated and measured optical eye diagrams is achieved both at 8 Gb/s with symmetric drive signals with varying amounts of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9 Gb/s with a 65-nm CMOS driver capable of asymmetric pre-emphasis pulse duration. For the model of carrier-depletion ring modulators, excellent matching between simulated and measured optical eye diagrams is achieved at 25 Gb/s with a 65-nm CMOS driver capable of asymmetric equalization.

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Parts of this chapter are reproduced from authors' recent journal publication, work, and so on [28].

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