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Research on the Characteristics of Silicon MOS-Like Light-Emitting Structure by Utilizing the Technology of Field-Induced Optical Radiation Mechanisms

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Additional information is available at the end of the chapter

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Abstract

As a well-known core material, silicon is becoming one of the most promising materials of photonic integration field. The chapter provides the research of integrated silicon MOS-like light-emitting structure utilizing the technology of field-induced optical radiation mechanisms. The silicon light-emitting device (Si-LED) plays an important role in realizing the on-chip optical interconnects, but Si-LED integrating on bulk silicon is facing many challenges due to the hybrid integration. In addition to be fully compatible with the standard complementary-metal-oxide-semiconductor (CMOS) process technology, the Si-LED also avoids the challenges that are mentioned above through integrating with bulk silicon substrate monolithically.

Keywords: light emitting device, optical radiation mechanism

1. Introduction

Silicon is the material par excellence. It is the most widely studied material in the history of civilization. In fact, the present-day information age has dawned with an electronics revolution brought about by the maturity of silicon-based microelectronics. The growth of the silicon industry follows the no-famous Moore's law, which states that the number of transistors in an integrated circuit chip doubles every 18 months. However, during the last decade there has been an indication of the decline of Moore's law. There are doubts whether in future silicon-based integrated circuits (ICs) will deliver the same advantages and increased functionalities over time as in the past.

The p-n junction is the vital component of most semiconductor devices. In this chapter, the concept of a light-emitting p-n junction is developed and characterized. Many studies in the past have correlated breakdown occurring in silicon p-n junctions with impact ionization and with material and structure parameters, especially some radiative recombination occurs while electron-hole pairs are produced during avalanche breakdown. Both the electrons and the holes can be heated by the electric field. The radiative transition between hot carriers emits photons larger than the energy gap. Hence, the luminescence during avalanche breakdown is characterized by a broad emission spectrum that extends to the energy of ~ 3.36 eV (i.e., with the shortest wavelength of ~ 369.05 nm), which represents the energy separating the hottest electron from the hottest hole. It is noted that ~ 3.36 eV is equal to $3E_g$ and the energy for impact ionization by a hot carrier is about $1.5E_g$. Substantial progress has been made in the field of silicon p-n junctions emitting visible light when operating in reverse-avalanche mode. The silicon-based light-emitting device (Si-LED), which is actually a simple p-n junction that is fully compatible with standard complementary-metal-oxide-semiconductor (CMOS) technology, is a potential light source that can monolithically be integrated with the silicon dioxide waveguide, photo-detector, and receiver circuit on a single silicon chip. The widespread use of SOI for PMIC and RF applications has added to the potential applications of Si-LEDs.

The weakest point of silicon is that proper light emitters and modulators cannot be realized due to its indirect bandgap. On the other hand, there is a steady advance in the field of photonics. Although discrete devices using the compound semiconductor materials and their alloys show very good performance, the levels of integration and performance are far below what has already been achieved in electronic integration on the same substrate. It is natural to expect that OEIC will provide the same advantages, that is, low cost due to batch fabrication, high functionality, scaling for denser integration, and so on, as provided by silicon ICs. Instead, if OEIC could grow on silicon and integrate with electronic ICs by using the same production facilities, the benefits to be accrued need no further elaboration. Si-based systems will then be used in all fields of electronics, computers, and communication. Therefore, Si-based photonics remains an active area of research and over the last 10–15 years some significant milestones have been achieved [1].

Another important area of application of silicon photonics is in very large-scale integrated (VLSI) circuits. The complexity of present-day ICs has reached a high level on different levels shown in **Figure 1**. The metallic interconnects, mainly Cu, produce delay due to resistor-capacitor (RC) time constants, which far exceed the transit time delay associated with the individual transistors. If the increase in speed is to be maintained at the same rate for the next-generation ICs, the interconnect bottleneck must be properly addressed. Optics is believed to be the right solution for the problem [2].

In the present chapter, the authors give an overview of the recent developments and the present status in silicon optoelectronics. A short history of the development of silicon-based light sources is given in Section 2. Next, Section 3 is devoted to point out why the Bremsstrahlung model is definitely not adequate to describe the radiative relaxation of hot carriers in reverse-biased silicon p-n junctions; other radiative processes, such as spontaneous radiative relaxation of electrons between states in two conduction bands, is suggested to be most likely

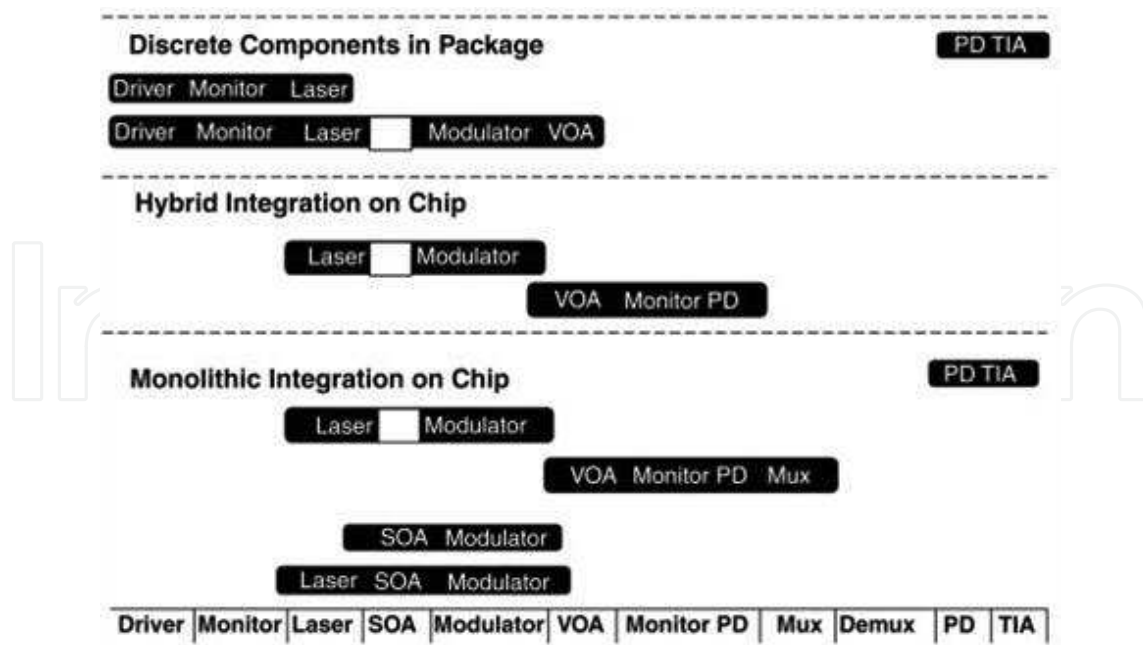


Figure 1. Level of device integration in commercially available product (After Ref. [3]).

responsible for the hot-carrier-induced luminescence. For the purpose of high-speed performance in electro-optic modulation, the high-frequency modulator optical response and data transmission are reviewed in Section 4. Finally, Section 5 concludes that the silicon light-emitting device with high-speed data transmission capability will be one of the key building blocks for the integrated silicon photonic chip for next-generation communication networks as well as future high-performance computing applications for optical interconnections.

2. Two- and multi-terminal CMOS/BiCMOS silicon LEDs

Silicon photonics has become one of the most promising photonics integration platforms in the last decade. This is mainly due to the combination of a very high index contrast and the availability of silicon CMOS fabrication technology, which allows the use of electronics fabrication facilities to make photonic circuitry. Unfortunately, the indirect bandgap of silicon leads to low efficiency. The rate of electron-hole recombination in silicon material is too low to produce emitted photons in forward-biased silicon p-n junctions, but light emission observed from reverse-biased silicon p-n junctions under avalanche breakdown was reported in 1955 by Newman [4]. The photograph of a silicon p-n junction being biased in the reverse direction at breakdown emits a yellowish light in the junction region as shown in **Figure 2**.

Next, Kramer et al. demonstrates that light-emitting devices can be integrated using industrial CMOS technology and operated at CMOS voltage level [5]. The reverse-biased p-n junction is capable of broad-band visible-light emission between 450 and 800 nm in the avalanche breakdown region under reverse bias with efficiency of the order of 10^{-8} . The spectral output of a p^+n^- junction operated in avalanche breakdown is given in **Figure 3**.

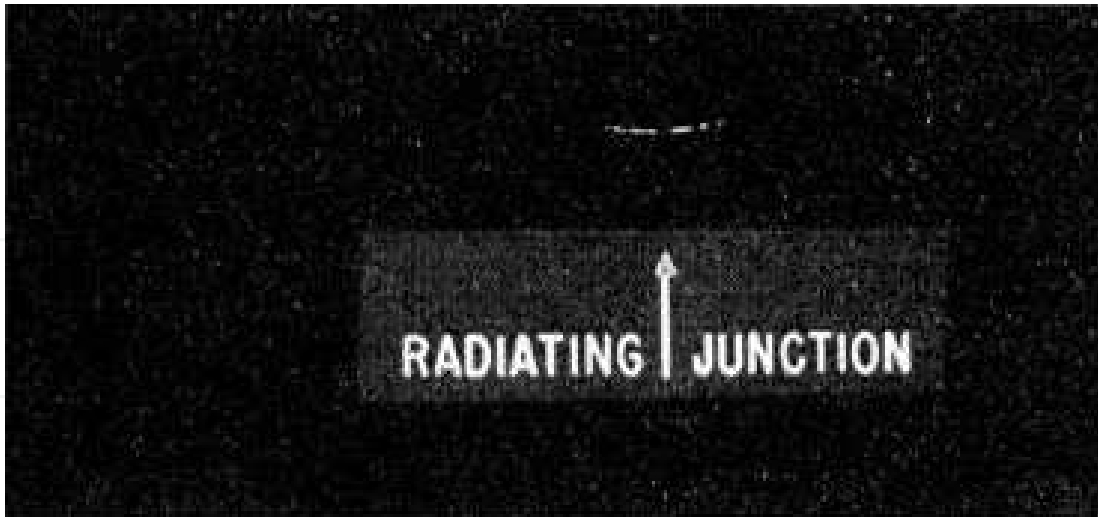


Figure 2. A photograph of the light emitted from a worked silicon p-n junction unit operating in the breakdown region. The junction is the horizontal bow-shaped curve. Current flows vertically across it (After Ref. [4]).

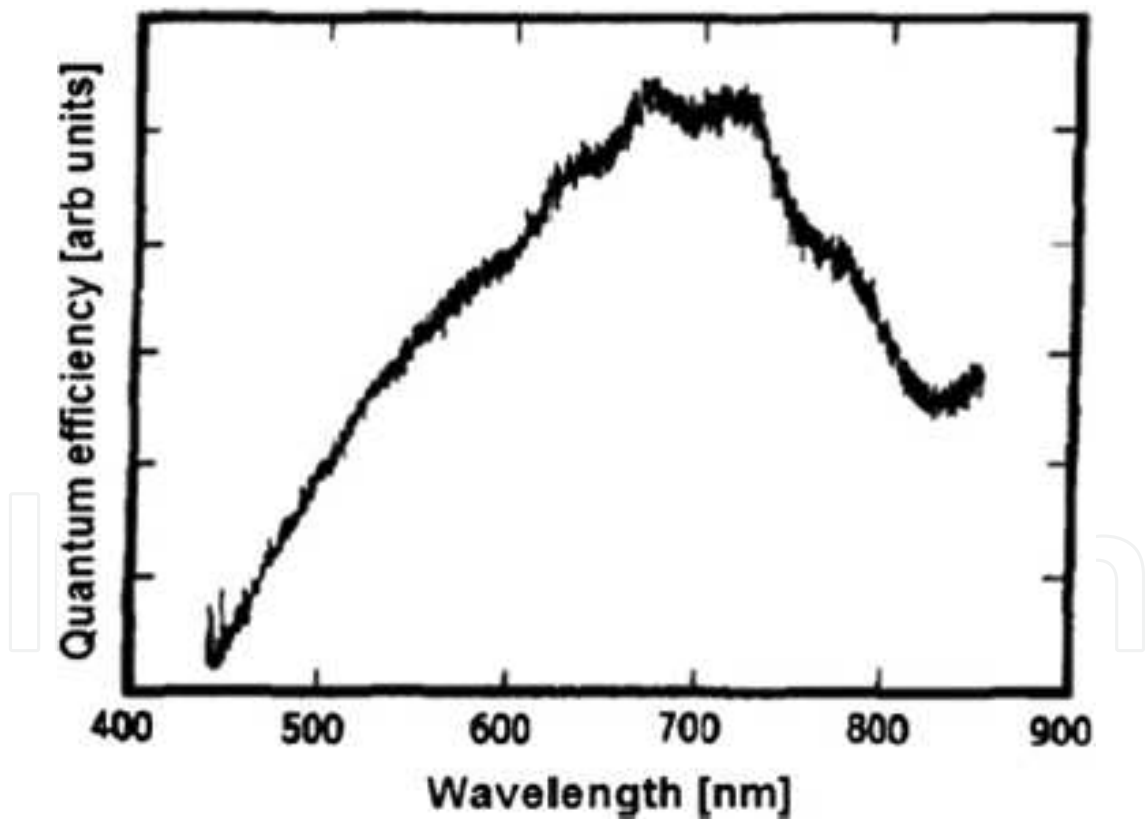


Figure 3. Emission spectrum of the silicon p^+n^- junction in the avalanche breakdown regime; typical reverse voltage is 33.2 V at reverse current of 25 mA, peak wavelength occurs at 700 nm, electric-to-optical power conversion efficiency is 1.1×10^{-9} , and quantum efficiency is 2.0×10^{-8} (After Ref. [5]).

Reference [6] shows a planar n^+p shallow-junction structure that is fabricated using a standard 1.2- μm CMOS process with no adaptations of the process at all. Excellent uniformity has been

obtained for large area devices. Furthermore, it is demonstrated that the light levels and intensity levels generated from the devices are indeed useful for on-chip electro-optical coupling and for chip-to-environment electro-optical coupling.

In addition to the study of silicon diode LED in which the light emission is due to the avalanche breakdown of the silicon p-n junction, a novel gate-controlled diode MOS-like multi-terminal device is described where both the light intensity and spatial light pattern of the device are controlled by an insulated MOS gate voltage.

Indeed, a metal-oxide-semiconductor field-effect transistor (MOSFET) consists of two identical gate-controlled diodes (i.e., “p⁺ Source/Drain to n-Substrate,” in a PMOSFET device) [7]. Since source and drain are grounded (i.e., $V_d = V_s = 0$ V), the reverse bias of the two p-n junctions is defined by the substrate voltage V_{sub} which is a fixed value. By changing the gate voltage V_g , the channel layer in the PMOSFET device can be categorized by the following three types:

a. *Inversion layer*

The gate voltage V_g varies while the substrate voltage V_{sub} is fixed. As shown in **Figure 4(a)**, the channel layer is a p-type inversion layer if $V_g < V_{sub}$. In addition, the concentration of the surface channel layer decreases with the increase in V_g .

b. *Depletion layer*

If the gate voltage V_g is high enough to be approximately equal to the substrate voltage V_{sub} , the p-type inversion layer will disappear in the channel and be replaced by the n-type substrate. As shown in **Figure 4(b)**, the depletion width of channel surface should be comparable to the depletion width of the “p⁺ Source/Drain to n-Substrate” junction diode.

c. *Accumulation layer*

If $V_g > V_{sub} > 0$, electrons will move toward the channel surface. The greater V_{gsub} (i.e., $V_g - V_{sub}$) is, the stronger an n⁺ accumulation layer will be generated near the surface channel. It is well known that the concentration of the layer is exponentially monotonic with a maximum at the channel’s surface and a minimum that is equal to the substrate concentration at the bottom of the channel layer. The depletion width has the minimum at point B in **Figure 4(c)** and the maximal depletion width equals the depletion width of the “p⁺ Source/Drain to n-Substrate” junction, which is point A in **Figure 4(c)**. **Figure 4(d)** provides more characterizations referring to point B, which actually is the transition between the p⁺ Source/Drain region and the channel layer underneath the gate. If $V_g = V_{sub}$, depletion width is unchanged as to be X_d (i.e., the depletion width of “p⁺ Source/Drain to n-Substrate” junction in thermal equilibrium). If $V_g > V_{sub}$, the depletion width at the transition will decrease from X_d to x_2 because of the accumulation layer (n-type) with a thickness 2. If $V_g \gg V_{sub}$, the depletion width at the joint will continue to decrease from x_2 to x_1 and the thickness of accumulation layer will increase to thickness 1. Furthermore, $x_1 < x_2$ means that gate voltage V_g is proportional to the concentration of the surface channel.

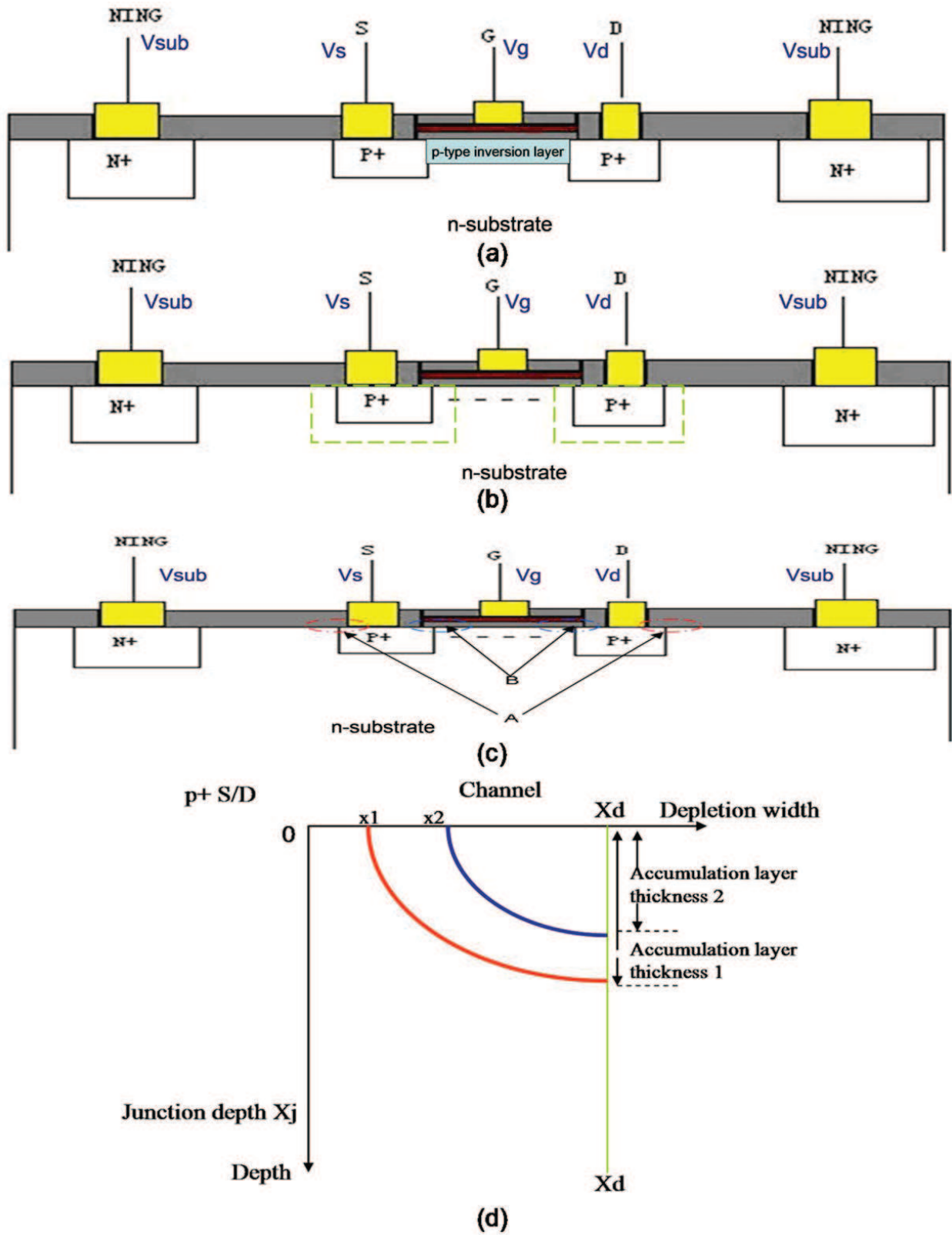


Figure 4. The characterization of the channel layer: (a) inversion, (b) depletion, (c) accumulation, and (d) depletion region width near the channel surface.

Indeed, in the accumulation layer, the thickness is just a few tens of nanometers. For the MOS structure in the accumulation mode, the relationship between the gate voltage and the accumulation layer's concentration and thickness is analyzed in the subsequent text. A derivation of the accumulation layer thickness as a function of substrate-doping concentration will show that the layer is very small and hence can be considered as a surface charge. The distribution of the charge as a function of depth, x , can be found using Poisson's equation [8]

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{\rho}{\epsilon_{si}} = -\frac{q}{\epsilon_{si}}(p - n + N_d - N_a) \quad (1)$$

with

$$p(x) = p_{p0} \exp\left(-\frac{q\Phi(x)}{kT}\right) = N_a \exp\left(-\frac{q\Phi(x)}{kT}\right) \quad (2)$$

and

$$n(x) = n_{p0} \exp\left(\frac{q\Phi(x)}{kT}\right) = \frac{n_i^2}{N_a} \exp\left(\frac{q\Phi(x)}{kT}\right) \quad (3)$$

where p_{p0} is the equilibrium hole concentration in the p-type material, n_{p0} is the equilibrium electron concentration in the same material, and $\Phi(x)$ is the potential in the silicon as a function of depth. Far from the surface of the silicon, the potential is equal to zero: $\Phi(x \rightarrow \infty) = 0$, which will be used as a boundary condition for Eq. (1).

In the hole accumulation layer formed in p-type substrate shown in **Figure 4(c)**, one can assume that $n \ll p$ and $N_d \ll N_a$, thus Eq. (1) can be rewritten as

$$\frac{d^2\Phi(x)}{dx^2} = -\frac{\rho}{\epsilon_{si}} = -\frac{q}{\epsilon_{si}}N_a \left[\exp\left(-\frac{q\Phi(x)}{kT}\right) - 1 \right] \quad (4)$$

where ϵ_{si} is the permittivity of silicon. From a numerical calculation, it is finally found that the thickness of the accumulation layer, x_{acc} , can be found using the condition that $\Phi(x = x_{acc}) = 0$:

$$x_{acc} = \sqrt{2}L_D \cos^{-1}\left(\exp\left(\frac{q\Phi_s}{2kT}\right)\right) \quad (5)$$

The thickness of the accumulation layer, x_{acc} , can thus vary between 0 and $\frac{\sqrt{2}}{2}\pi L_D$, depending on the accumulation charge.

The result is also drawn in **Figure 5**. Since the carrier (*hole*) concentration is an exponential function of the potential, the charge density increases very rapidly close to the surface and most of the accumulation charge is concentrated within a depth much smaller than x_{acc} as shown in **Figure 6**. Hence, the charge in the accumulation layer can be considered as a surface charge.

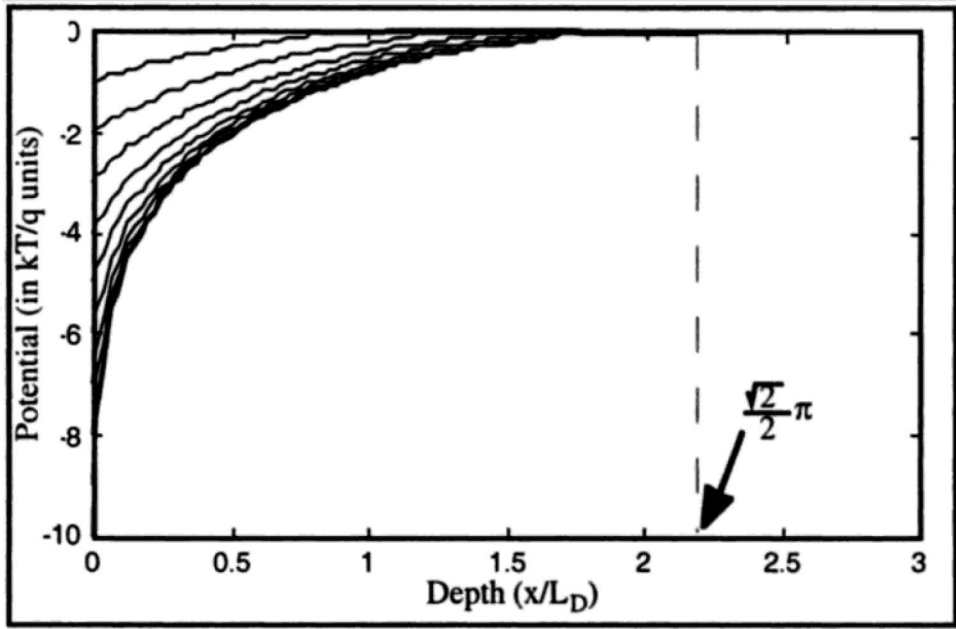


Figure 5. Potential (normalized to kT/q) in an accumulation layer (holes in p-type silicon) as a function of depth (normalized to L_D) for different values of surface potential (After Ref. [8]).

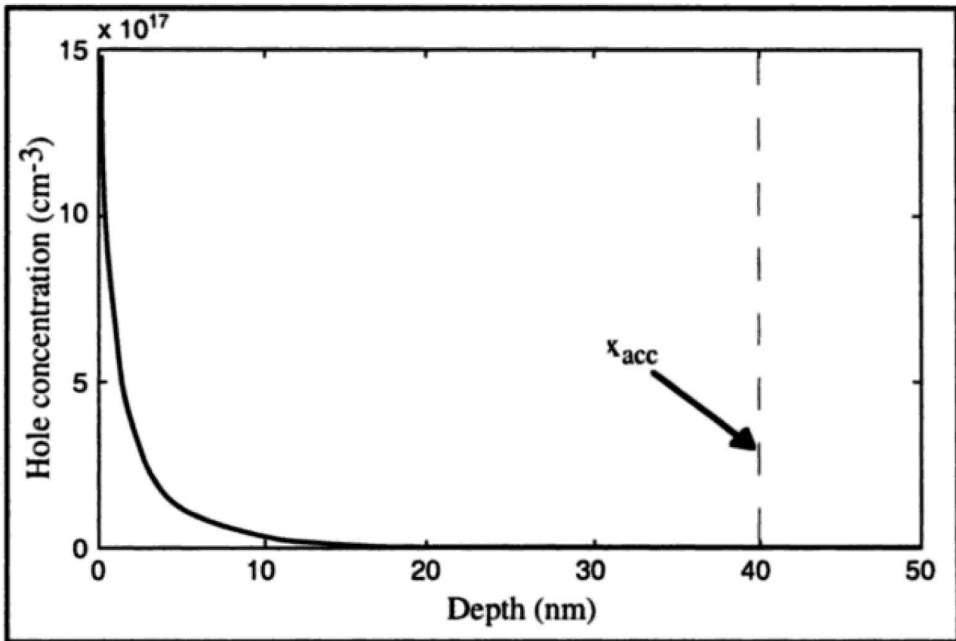


Figure 6. Hole concentration profile in an accumulation layer. The substrate-doping concentration, N_a , is equal to 10^{16} cm^{-3} and the surface potential, Φ_s , is equal to $-5kT/q$ (After Ref. [8]).

Due to the increase in the concentration of accumulation layer and the decrease in the depletion width near the surface channel, the breakdown voltage BV of the “p⁺ Source/Drain to n-Substrate” junction decreases with the increase in gate voltage V_g . Moreover, if the accumulation layer is approximately treated to consist of numerous n-type thin layers that are individually with their own concentrations, the PMOSFET being in the operating condition mentioned above is a combination of Zener breakdown p-n junctions and avalanche breakdown p-n junctions.

As shown in **Figure 7**, it is shown that the breakdown voltage BV of a p^+n junction (i.e., the “ p^+ Source/Drain to n-Substrate” junction in a PMOSFET device) decreases with the increasing gate voltage V_g .

On the other hand, the mixture of Zener breakdown and avalanche breakdown (i.e., a transition from avalanche to tunneling) could be the major reason for the reduction in BV of the two parallel-connected p-n junctions (i.e., the “ p^+ Source/Drain to n-Substrate” junction shown in **Figure 4**) because it is known that the Zener breakdown voltage is usually much lower than the avalanche breakdown voltage. More specifically, at large positive gate voltages, a strong accumulation layer occurs and the surface electron concentration shields the electric field within the peripheral junction depletion region from the gate, reducing the effect of the gate voltage on avalanche breakdown in the “ p^+ Source/Drain to n-Substrate” junction of the PMOSFET device [10].

As discussed previously, a higher gate voltage V_g can induce the lower breakdown voltage BV of the two p-n junctions (i.e., the “ p^+ Source/Drain to n-Substrate” junction in the PMOSFET device). Next, the reverse current I_{sub} flowing through the p-n junctions with breakdown mechanisms will increase with gate voltage V_g while the substrate voltage V_{sub} (i.e., the reverse bias of the two p-n junctions) is a fixed value [11]. Since the optical emission power is linear with the reverse current I_{sub} [12], increasing the gate voltage V_g is a significant method to realize electro-optic modulation in the three-terminal gate-controlled diode Si-PMOSFET device [13–15].

It is noted that the Si-diode LED (i.e., the p-n junction is reverse-biased to avalanche breakdown) is a two-terminal device and the Si gate-controlled-diode LED (i.e., the reverse-biased p-n junction with varying the gate voltage) is a three-terminal device. In particular, a silicon light-emitting device with the structure of a Si-PMOSFET device that is fully compatible with the standard Si-CMOS process technology experimentally demonstrates that the reverse current I_{sub}

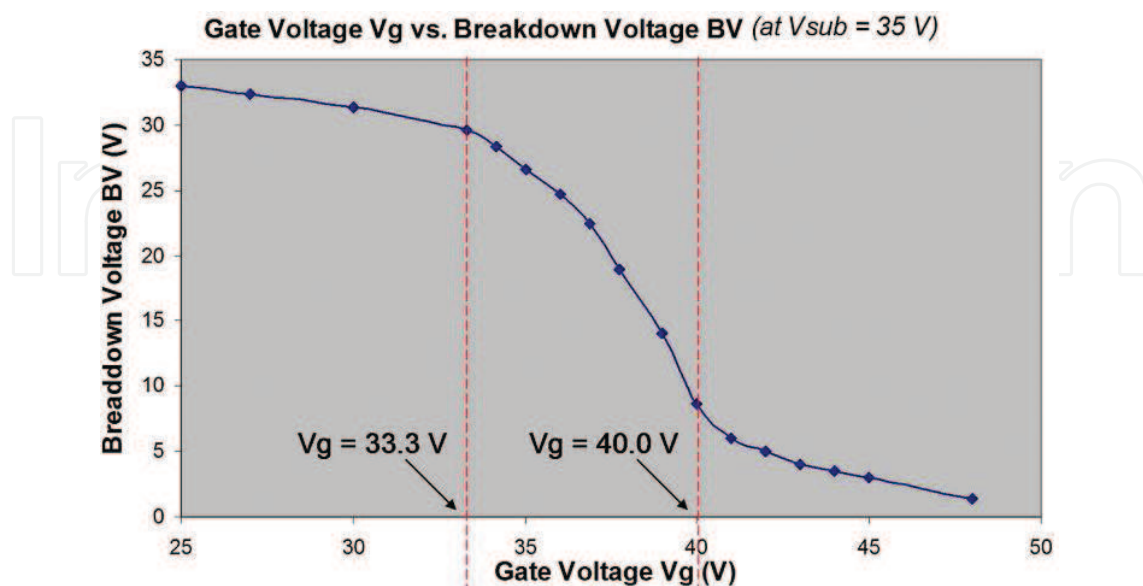


Figure 7. The high-voltage extreme for BV saturation occurs if V_g is being lower than ~ 33.3 V (i.e., the turn-on voltage), the low-voltage extreme for BV saturation occurs if V_g is being higher than ~ 40 V, V_g is almost linear (with a symbol of -) with BV in the intermediate range 33.3 V $< V_g < 40$ V, and BV tends toward 38 V if V_g is approaching 0 V (After Ref. [9]).

is always linearly proportional to optical emission power whether the Si-PMOSFET device acts as a two-terminal device (i.e., p-n junction diode, the “p⁺ Source/Drain to n-Substrate” junction with floating the gate, Si-diode LED) or acts as a three-terminal device (i.e., gate-controlled diode, the “p⁺ Source/Drain to n-Substrate” junction in the course of varying the gate voltage, Si gate-controlled diode LED). The optical power measured from the device is divided by the photon energy to obtain the number of collected photons, and then the external quantum efficiency is defined as the ratio of the number of collected photons to the number of injected electrons. Such linearity implies that the control of the increasing current is a significant way to enhance the quantum efficiency of this light source device no matter what the physical structure (i.e., two or three terminals) of the device is.

For the first time, it has been discovered that, at the same reverse current, the optical output power in the gated diode structure is higher than the optical output power in diode structure. In other words, for this PMOSFET-like device, the three-terminal operating mode (i.e., Si gate-controlled-diode LED) is more efficient than the two-terminal operating mode [12].

Furthermore, the Si gate-controlled-diode LED can be treated as an efficient low-voltage optical source. It is observed that both the quantum efficiency and electrical-optical power conversion efficiency increase obviously though the reverse current I_{sub} is much lower because of the reduction in reverse-bias voltage V_{sub} . Such a phenomenon may be explained by the absorption coefficient of silicon at different wavelengths and is suggested to be a practical approach to realizing emission efficiency enhancement in near future [11].

3. Characterization of the optical properties

Assuming that the classic Bremsstrahlung model is approximately applicable, the origin of optical radiation observed in the reverse-biased silicon p-n junction could be explained by the Coulomb interaction between impact ionized carriers and charged centers in the depletion region. The charged center, also known as quantum dot, is an artificial atom in fact even if it has a mass that is approximately equal to one atom. Besides the properties of atoms such as having discrete energy levels and shell structure, the artificial atom, quantum dot, including tenability and comparability of level spacing, Coulomb scattering, and thermal energy are more advanced than the natural atom by allowing transport measurement [16].

Since the number of carriers is proportional to the number of emitted photons, the number of light spots increases with the reverse current rather than individual spots growing brighter. It is concluded that the avalanching current is carried through the junction by these localized emitting spots (i.e., quantum dots). Despite a great deal of theoretical and experimental work to clarify the mechanism of the strong visible luminescence from reverse-biased silicon p-n junctions, it still remains unclear because of this complication. Overall, the major mechanism is drawn in **Figure 8** and can be interpreted by the three different transitional processes below:

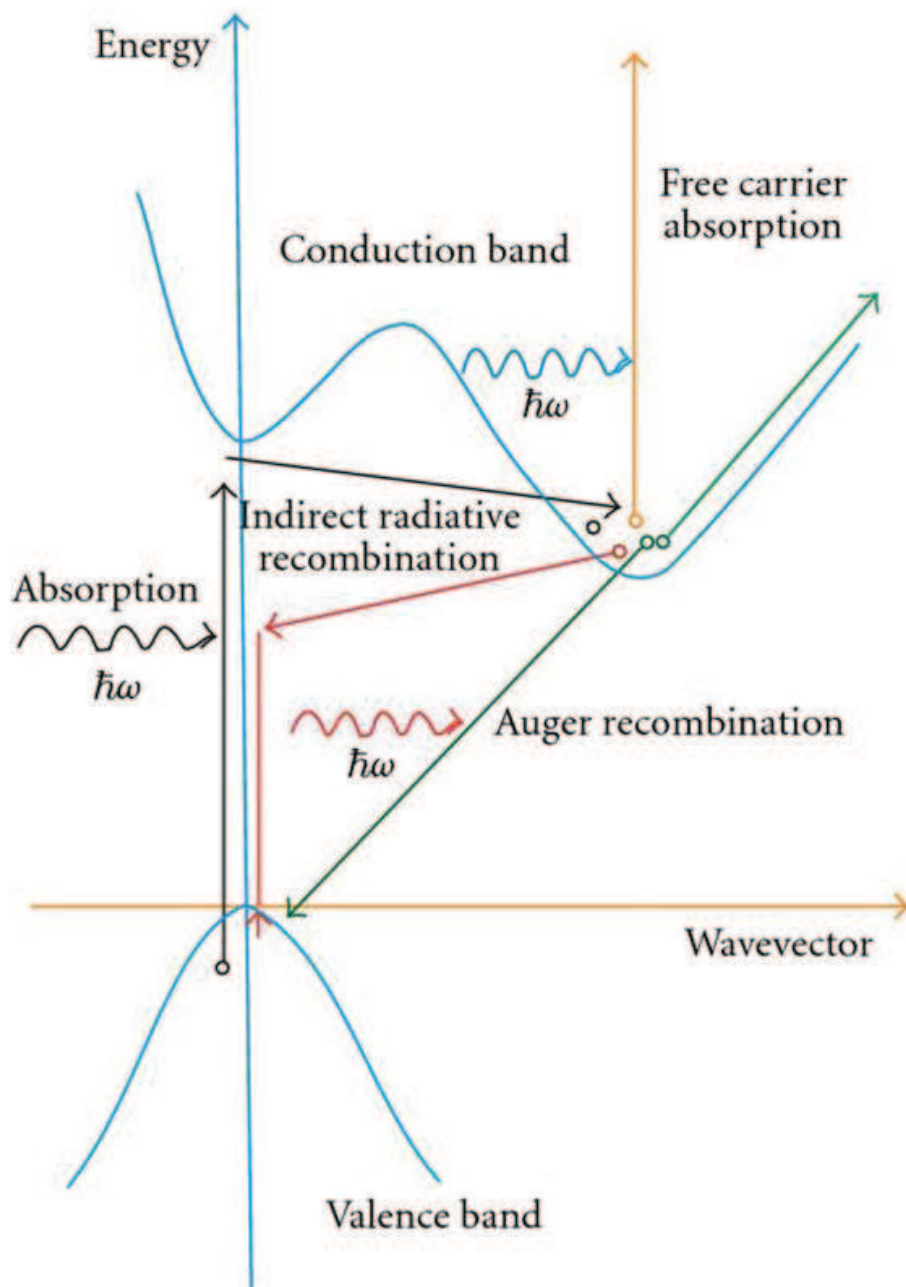


Figure 8. Band structure of bulk Si with the various possible transitions for an electron-hole pair: radiative recombination, Auger recombination, and free-carrier absorption (After Ref. [17]).

a. *Intra-band direct transition*

Most hot carriers do not find suitable transition partners with the same vector in k -space for photon radiation transition. As a substitute, phonon radiation is the most possible result for getting back to a low-energy state. The output light power per unit optical frequency is expressed as

$$I(\nu)_{Intraband} = C_1(h\nu)^{3.5\frac{1-3/\alpha}{2+3/\alpha}} \exp[-b(1.41h\nu - E_0)] \quad (6)$$

where C_1 is a constant, b is the function of mean-free path, E_0 is the threshold energy for ionization, and α is a positive value that is related to the electric field and mean-free paths of ionized electrons and emitted photons [18].

b. Intra-band indirect transition

This transition only occurs by the intervention of phonon assistance, in which phonons are radiated mostly by intra-band direct transition. Since the transition is the well-known Bremsstrahlung radiation (i.e., the scattering of an electron by an external field, accompanied by the emission of a photon), the output light power per unit optical frequency can be written as

$$I(\nu)_{\text{Bremsstrahlung}} = C_2 \exp\left(\frac{h\nu}{kT_e}\right) \quad (7)$$

where C_2 is a constant, k is the Boltzmann's constant, and T_e is the effective temperature [19]. The optical radiation is induced by the inelastic collision (i.e., inelastic X-ray scattering) between carriers (e.g., electron and hole) and charged centers (e.g., artificial atom). The probability of finding a carrier in state E_B is

$$P(E_B) = \frac{\exp(-\beta E_n)}{\sum_n \exp(-\beta E_n)} \quad (8)$$

which is known as canonical or Maxwell-Boltzmann distribution. Assuming the electric and magnetic fields each represents one degree of freedom, the average energy β will be equal to kT_e .

c. Inter-band transition

Under most situations, inter-band composition is the most effective process of photon emission. It must satisfy many conditions, such as same vector in k -space and direct transition of hot carriers. Commonly, the transverse momentum of a wave vector is written as

$$k(\zeta) = \sqrt{\frac{2m_e}{\hbar} (PE - E_e)} \quad (9)$$

where ζ is the distance from the electron energy to the center of the band, m_e is the effective mass of electron, PE is the potential energy of the Si-SiO₂ barrier, and E_e is the energy of incoming electron. Further, the detailed form of $PE - E_e$ is given by

$$PE - E_e = \frac{(0.5E_g)^2 - (qE_y\zeta)^2}{E_g} \quad (10)$$

where E_g is the bandgap energy of silicon and E_y is a vertical field induced by the gate-to-source/drain voltage drop.

It should be mentioned that silicon is a material with indirect bandgap. For indirect gap materials, the wave vector dependence is essential in order to get a sharp peak in the emission spectrum of exciton molecules [20]. Accordingly, the output light power per unit optical frequency can be written as [21]

$$I(\nu)_{Interband} = I(\nu)_{Emission} - I(\nu)_{Absorption} \quad (11)$$

Correspondingly, the electroluminescence spectra captured from the Si-PMOSFET device operating as Si gate-controlled-diode LED by the optical spectrometer is given in **Figure 9**. There is a distinct emission peak at 625 nm in the emitting wavelength range of 400–900 nm, and the light intensity increases with the gate voltage V_g . No obvious phenomenon of spectral shifting is observed with different operating voltages and currents.

Figielsky and Torun [22] proposed the intra-band transition, specifically Bremsstrahlung of hot carriers at charge centers. Chynoweth and McKay [23] explains emission with wavelength longer than 539 nm using intra-band transitions. Wolff [24] proposed intra-band hole transition near $k = 0$ to explain low-energy spectra, but cannot fit the emitting wavelength longer than 620 nm. It is concluded that

- Photons with emitting wavelength longer than 620 nm are attributed to indirect inter-band process in high-field carrier populations.
- Bremsstrahlung radiation appears to dominate at intermediate range of 539–620 nm.
- The mechanism can be treated as near-direct inter-band transition for emitting wavelength shorter than 539 nm.

The phenomenon of and the physical mechanisms for the generation of minority carriers in the Si-MOSFET are also studied, since carrier transport in submicron silicon CMOS MOSFET

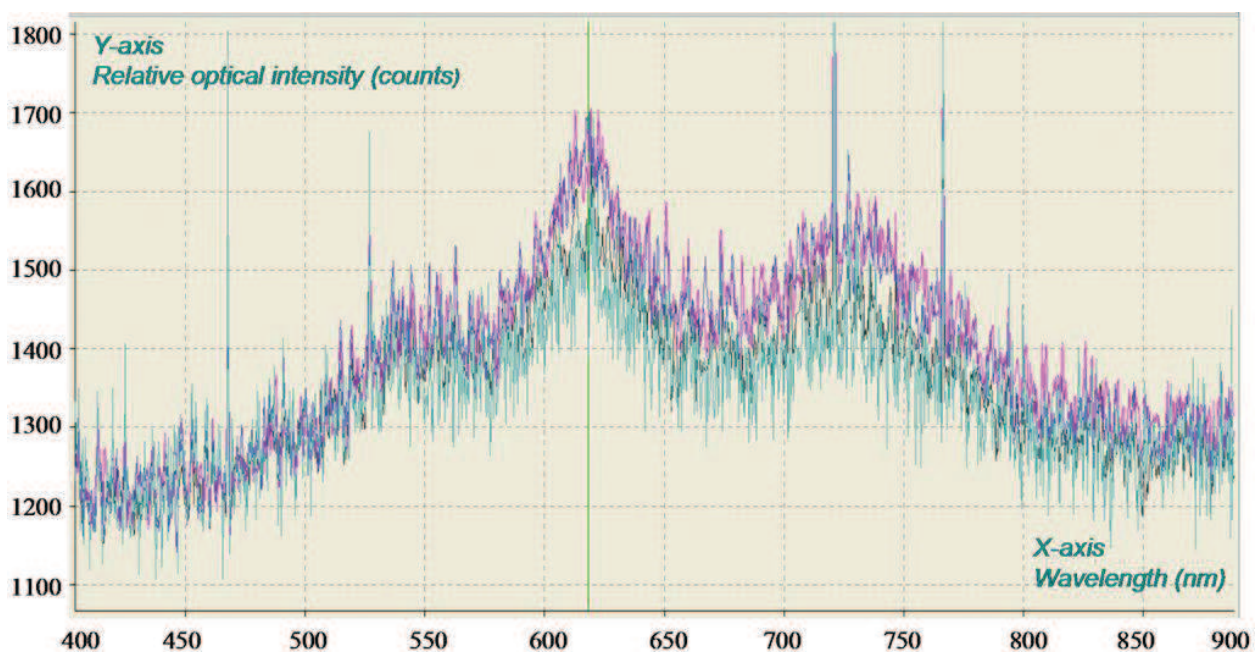


Figure 9. Output electroluminescence spectra.

demonstrates strong hot-carrier effects. A reverse-biased p-n junction is shown at a fixed separation for a MOSFET biased in the saturation region; because this p-n junction is reverse-biased, it acts as a collector of minority carriers in the substrate [25]. In Ref. [26], the spectral characteristics of the emitted photons from n-channel MOSFETs biased into saturation were investigated directly using photon emission spectroscopy; the correlation between the substrate current of the bias voltages, channel current, and channel length were presented; theoretical calculation of the photon emission intensity based on the Bremsstrahlung radiation mechanism does not agree well with the experimental measurements when the variation of the channel electric field with bias was accounted for; this suggests that Bremsstrahlung radiation of hot electrons in the Coulomb-scattering field of the dopant atoms is unlikely to be the dominant mechanism of photon emission in n-channel MOSFETs; other mechanisms such as direct and phonon-assisted conduction-to-conduction band transitions have to be considered to explain the hot-carrier-induced photon emission mechanism.

4. Analysis of modulation speed in the reverse-biased silicon p-n junction-based LED

As a centrosymmetric material, silicon has no electro-optic effect. The only way to achieve a modulator is to use the free-carrier effect where the free-carrier concentration is controlled in a p-n junction by injection, accumulation, or depletion. Demonstrations of high-speed modulation in free-carrier-depleted silicon-based modulators have been made theoretically [27] and experimentally [28, 29]. A four-terminal p^+pnn^+ vertical modulator integrated into a SOI rib waveguide, based on carrier depletion in a p - n junction formed in one arm of a Mach-Zehnder interferometer, was proposed in 2005. Based on a similar design, Intel in 2007 developed a high-speed and high-scalable optical modulator based on depletion of carrier in a vertical p-n junction diode showing data transmission up to 30 Gbit/s at 1550 nm [28]. Pinguet et al. [30] realized a lateral modulator either with pn or with $pipin$ structure both achieving about 10-GHz roll-off frequency and insertion losses of 3 and 5 dB, respectively. Due to the low refractive effects, these modulators have to be mm-long. In order to reduce the device dimensions of optical resonators, a compact device using a ring resonator with a diameter of 10 μm was reported in Ref. [31].

The modulation speed of the silicon p-n junction can be categorized by the following two types: (a) the forward-biased operation of p-n junctions for light emission is a slow, inefficient, and unreliable process because of the indirect band structure of silicon; (b) the reverse-biased operation of p-n junctions for light emission is a fast process in which the limiting speed of light modulation is determined by the transit time of the minority carriers across the junction during the filament of breakdown currents.

In particular, light modulation at 20 GHz is reported for the first time for a reverse-biased p-n junction operating in avalanche breakdown mode [32]. The light modulation at such a high speed rules out any possibility of phonon-assisted indirect transitions, but implies the existence of intra-band transitions of hot carriers. Furthermore, gigahertz range modulation can be

explained through intra-band transition of avalanche-generated hot carriers, which have broad energy distribution explaining the broadband light emission of 430–800 nm [33].

In contrast to reverse-biased p-n junction-based Si-diode LED in which the modulation speed is limited by the minority carrier's lifetime, the modulation speed of Si gate-controlled-diode LED is limited by the discharge time of the metal-oxide-semiconductor (MOS) capacitor instead of the natural carrier lifetime. Carrier confinement occurs in the band-bending region near the silicon surface, and the MOS capacitor discharge time can presumably be controlled via the RC time constant or other effects in the circuit. The Si gate-controlled-diode LED operates on the principle of the MOS capacitor and not on the abovementioned standard p-n junction diode [34].

It is important to note that a Si-PMOSFET device is able to work as two identical gate-controlled diodes (i.e., the "p⁺ Source/Drain to n-Substrate" junctions with varying gate voltage V_g) [15] or as two p-n junction diodes (i.e., the "p⁺ Source/Drain to n-Substrate" junctions with floating gate terminal) [35]. Accordingly, the electro-optic modulation schematics for both the two-terminal Si-diode LED and the three-terminal Si gate-controlled-diode LED are presented in Ref. [36].

Snyman et al. [37] further discusses the speed of Si-diode LED. With the dynamic on-resistance of the p-n junction in avalanche in the tens of kilo-ohms range and the reverse-biased junction capacitance in the range of fF, the RC time constant will be in the range of tens of psec. This will be sufficient to produce modulation in excess of 10 GHz. For the speed of Si gate-controlled-diode LED, the intrinsic modulation speed could be as high as a few hundred GHz [36, 37]. Furthermore, it shows the expected Si gate-controlled-diode LED modulation frequency range as a result of parasitic capacitances in the MOSFET device for a given biasing condition; these derivations verify that the modulation speed is about a few hundred GHz, and a new model is proposed to further predict the modulation speed at a chosen DC-biasing condition [38].

Gardes et al. [39] proposed a ring-resonator modulator which is based on the carrier depletion in a reverse-biased p-n junction and is formed on a 300 nm wide, 150 nm etch depth, and 200 nm high-rib waveguide. A linearly polarized light beam emitted from a tunable laser with emitting wavelength range of 1520–1620 nm was coupled into the waveguide using a polarization-maintaining lensed fiber, and then the output light was collected by an objective and focused on an IR detector. Regarding the transient analysis, the frequency response of the MOS-structure-based electro-optical modulator was measured using an AC signal generated by an opto-RF vector network analyzer. As presented in **Figure 10**, the RF signal was coupled to the ring resonator using ground-signal-ground electrodes, and the modulated optical signal was then coupled back to the opto-RF vector network analyzer. As a candidate for highly compact, wide bandwidth modulator, the device could exhibit an electrical small signal bandwidth of 19 GHz shown in **Figure 11**.

In addition, a comparison between the Si-diode LED and Si gate-controlled-diode LED in the field of phase modulation can be obtained from the modulation curves shown in **Figures 12** and **13**. For the case of two-terminal Si-diode LED, the depletion width of the reverse-biased p-n junction depends on the bias voltage and doping concentration: the charge density change

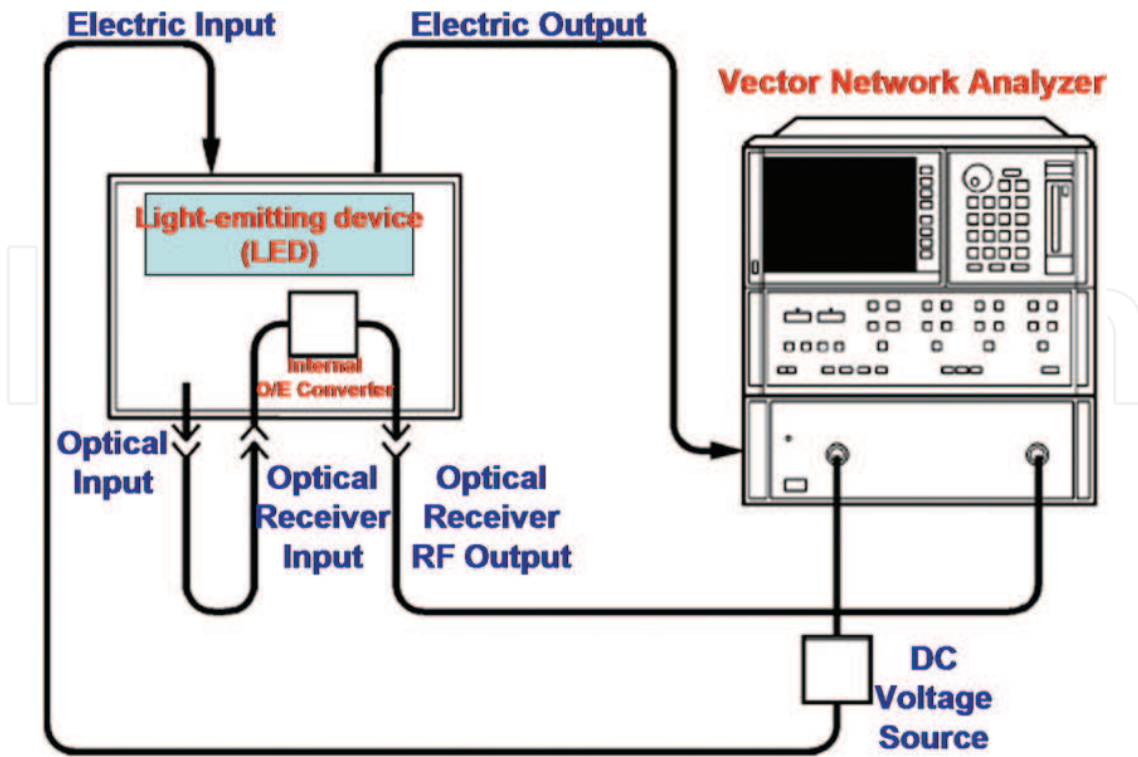


Figure 10. Schematics for the transient measurement.

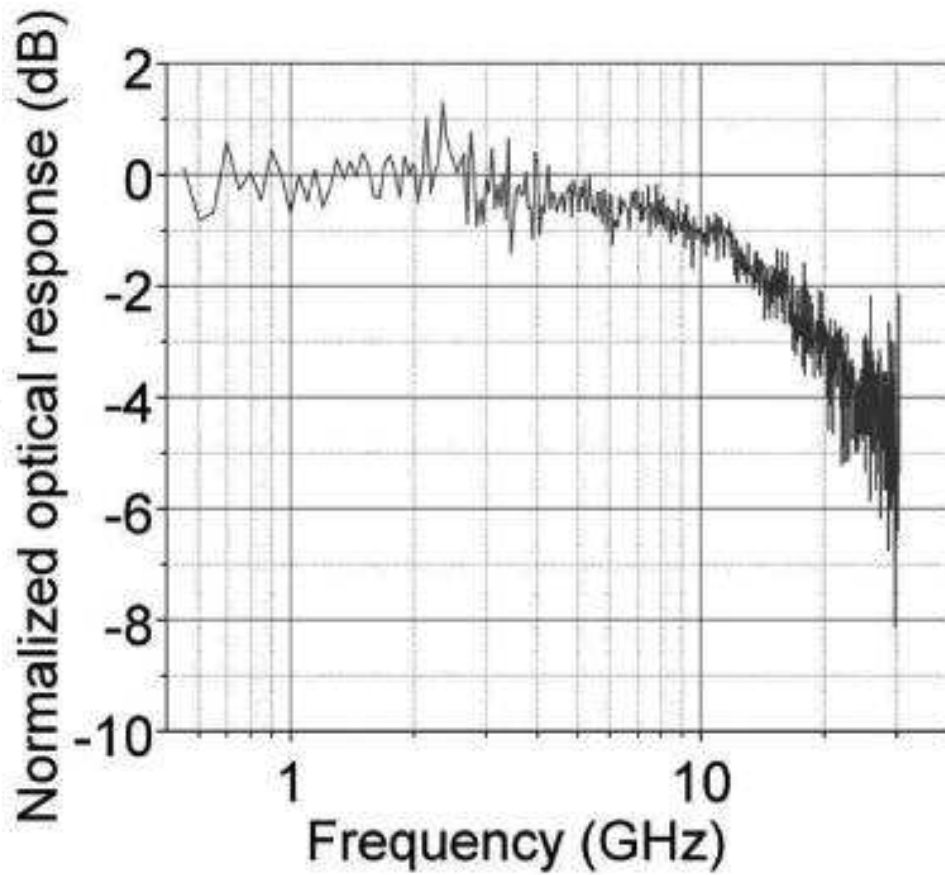


Figure 11. Normalized optical response as a function of frequency (After Ref. [40]).

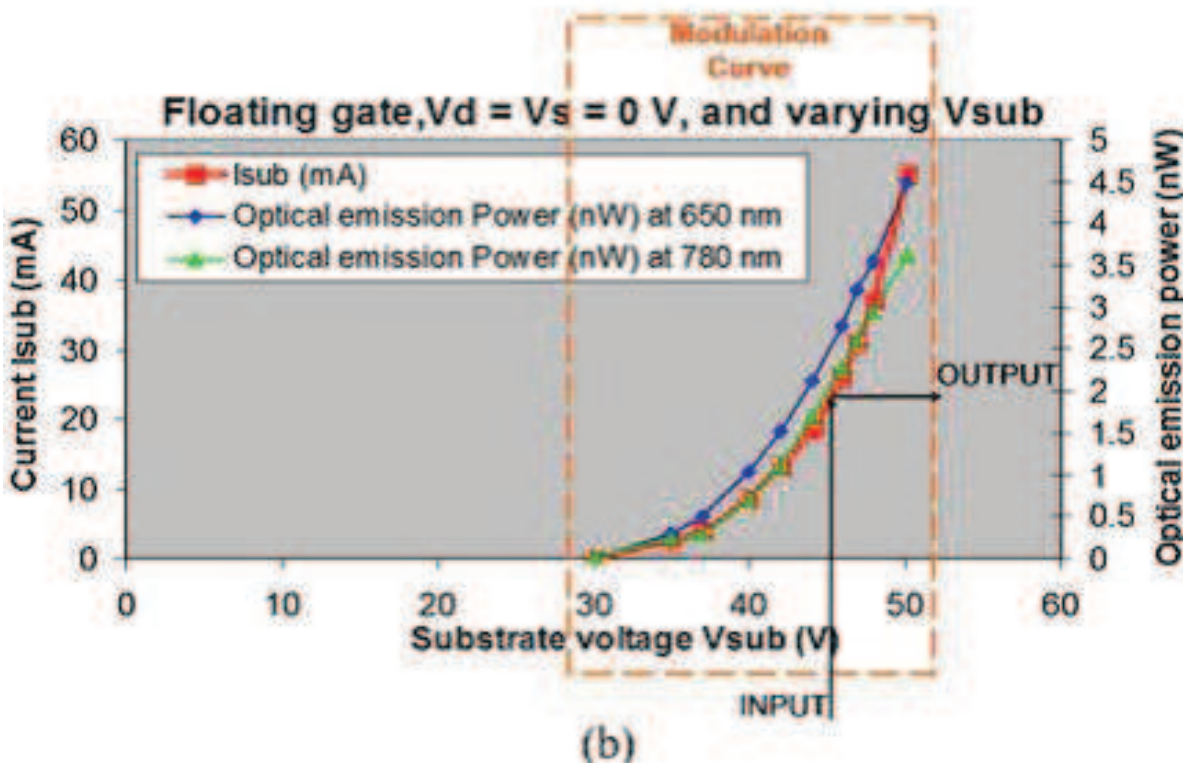
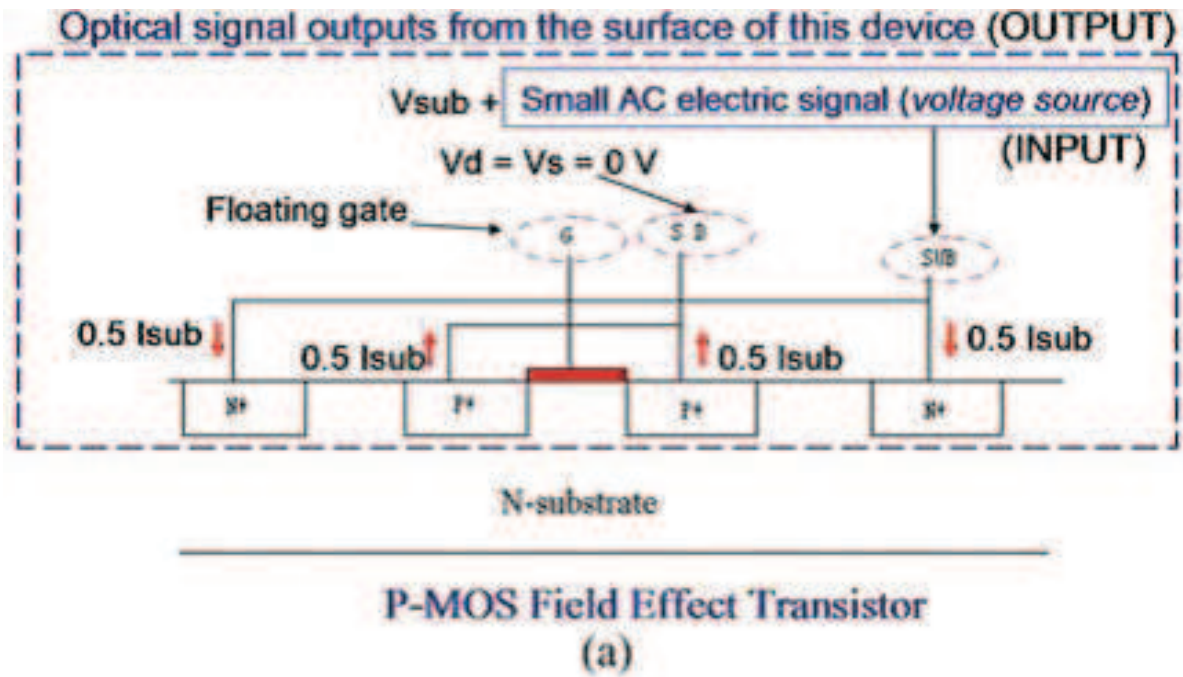


Figure 12. (a) V_{sub} , a DC source, is the reverse bias across the “p⁺ S/D to n-sub” junction. (b) V_{sub} is varied to realize optical modulation in the two-terminal device. The transfer function between the electric input and the optical output is determined by the slope of the modulation curve.

associated with the depletion width change due to the bias voltage V_{sub} . Because the depletion width is not linearly dependent on the drive voltage V_{sub} , it is similarly expected that the phase shift is not to be linearly dependent on the voltage. Accordingly, the modulation curve shown in **Figure 12** is nonlinear. This is quite different from the MOS-capacitor modulator, which

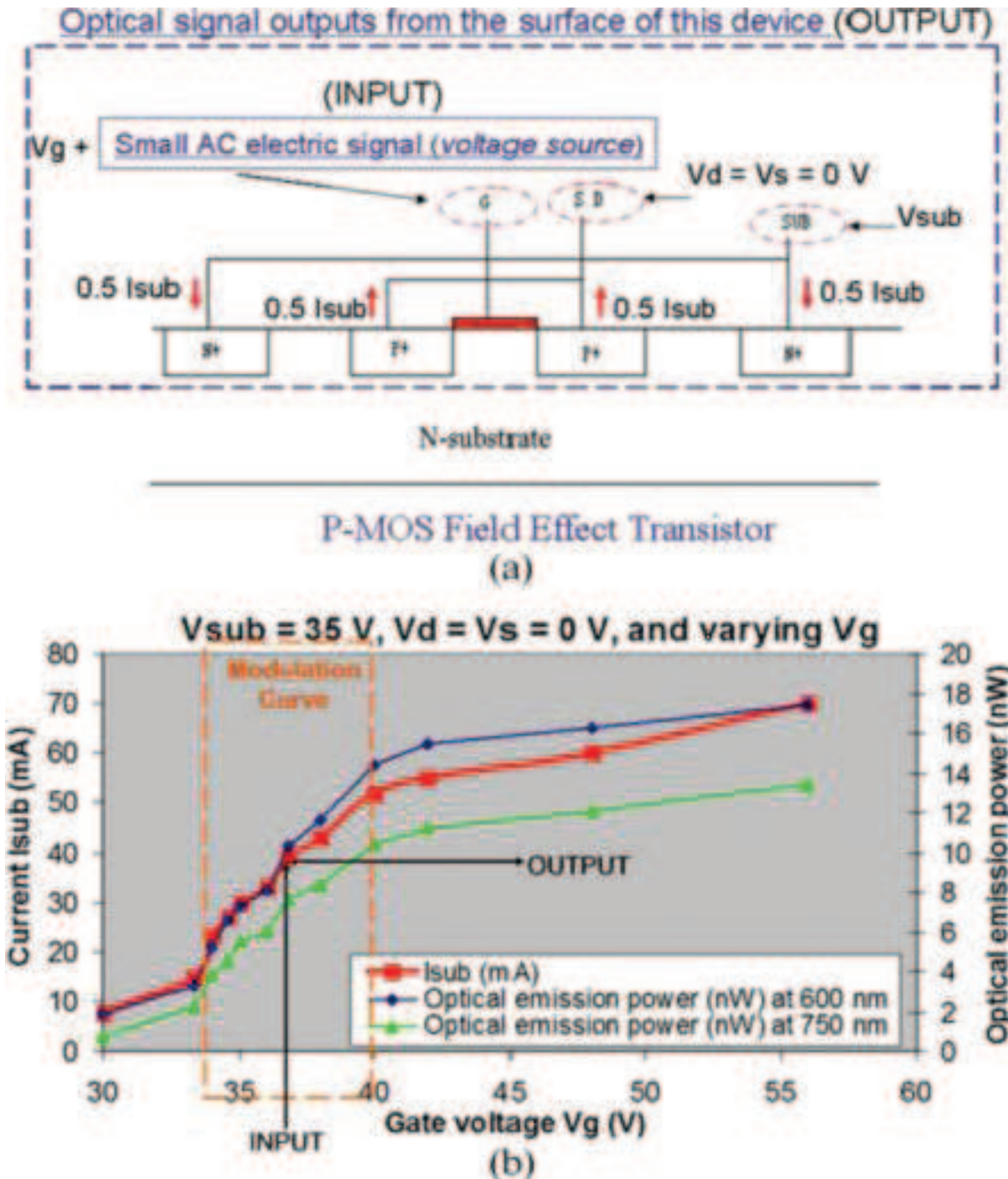


Figure 13. (a) V_g , a DC source, is the gate voltage. V_{sub} , a DC source, is the reverse bias across the “p⁺ S/D to n-sub” junction. (b) V_g is varied to realize optical modulation in the three-terminal device. The transfer function between the electric input and the optical output is determined by the slope of the modulation curve (After Ref. [36]).

shows linear dependence of the phase shift versus the drive voltage V_g . Accordingly, the modulation curve shown in **Figure 13** is almost linear.

The potential application of the Si-LED is for monolithic integration in silicon CMOS-integrated circuits (Si CMOS ICs). The importance of the realization of chip-scale optical interconnection by

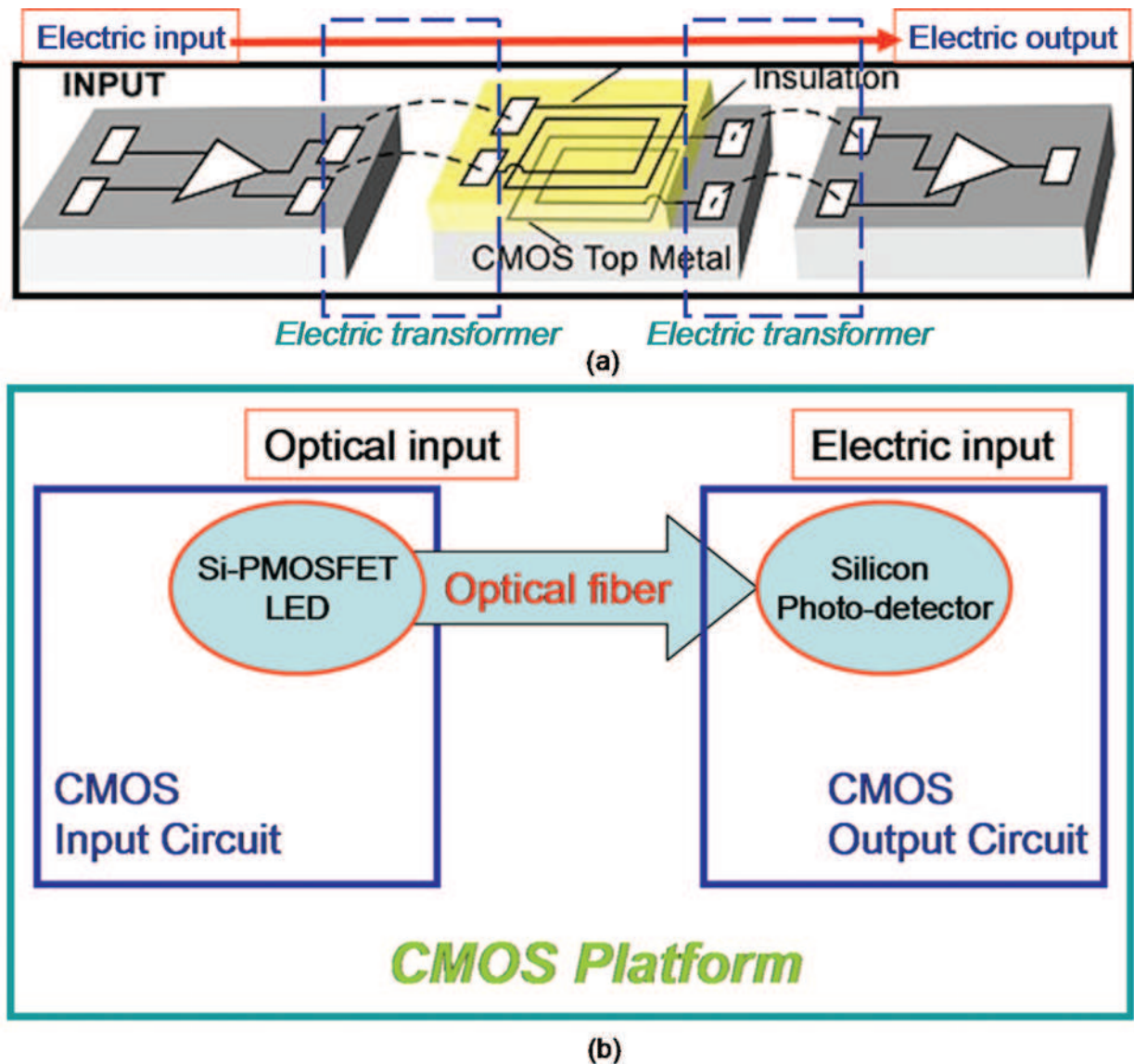


Figure 14. Interconnect: (a) electric interconnection and (b) optical interconnection.

silicon light source should be mentioned. Conventional electric interconnection in today's computers has a bottleneck for high-speed and large-capacity data transmission.

As shown in **Figure 14(a)**, *iCouple* uses the electric transformer as the isolator and the metal as the interconnect [40]. To break through the bottleneck, a replacement of electric interconnection by optical interconnection is the only possible way with great potential. More specifically, the concept of on-chip optical interconnect with silicon light emitter, waveguide, input, and output circuits integrated on the standard CMOS fabricating platform is simply illustrated in **Figure 14(b)**. The silicon light source with a PMOSFET device structure, Si-PMOSFET LED, has been analyzed in detail in Refs. [11–15], and the PMOSFET device is fully compatible with the Si-CMOS process technology that is schematically shown in **Figure 15**.

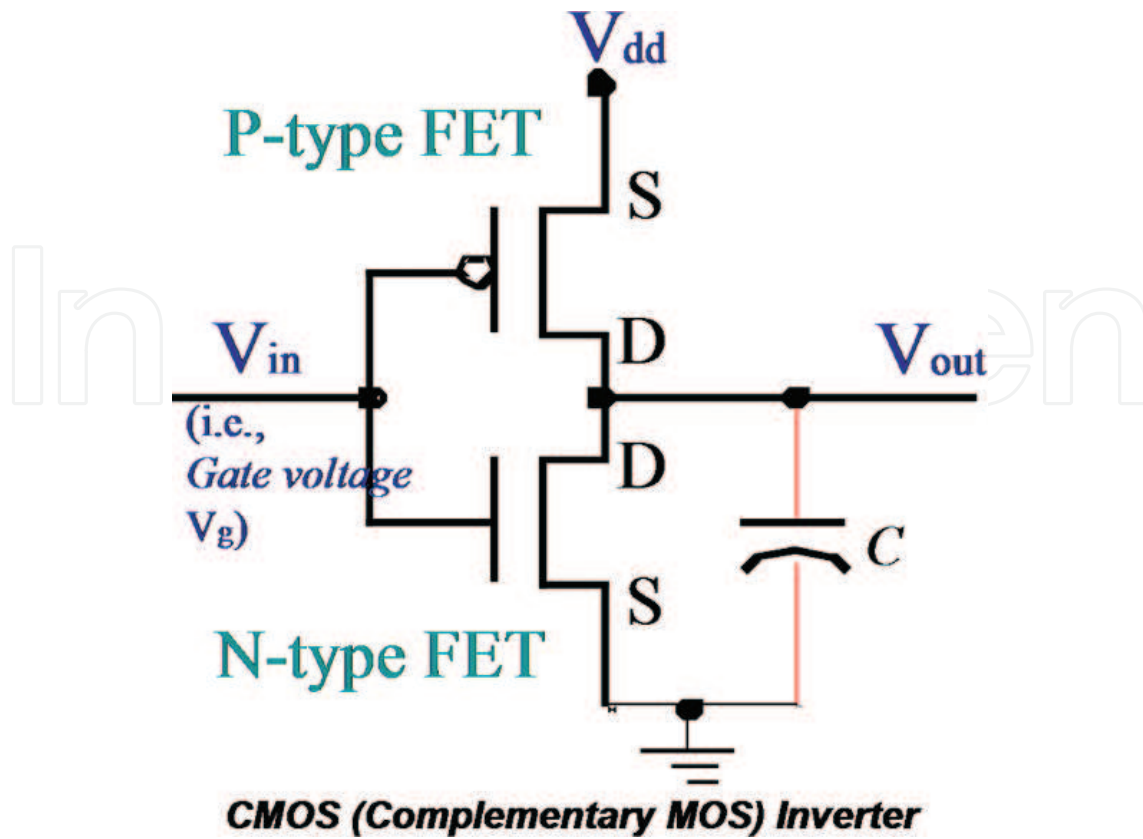


Figure 15. Schematic diagram of CMOS (complementary MOS) inverter: modern MOSFET technology has advanced continually since its beginning in the 1950s. The complementary nature of p-type FETs and n-type FETs makes it possible to design low-power circuits called CMOS or complementary MOS circuits. Because of the advantages of low-power dissipation, short propagation delay, controlled rise and fall times, and noise immunity equal to 50% of the logic swing, the CMOS process is defined as the standard fabricating technology for semiconductor devices and electronic circuits in industry [41].

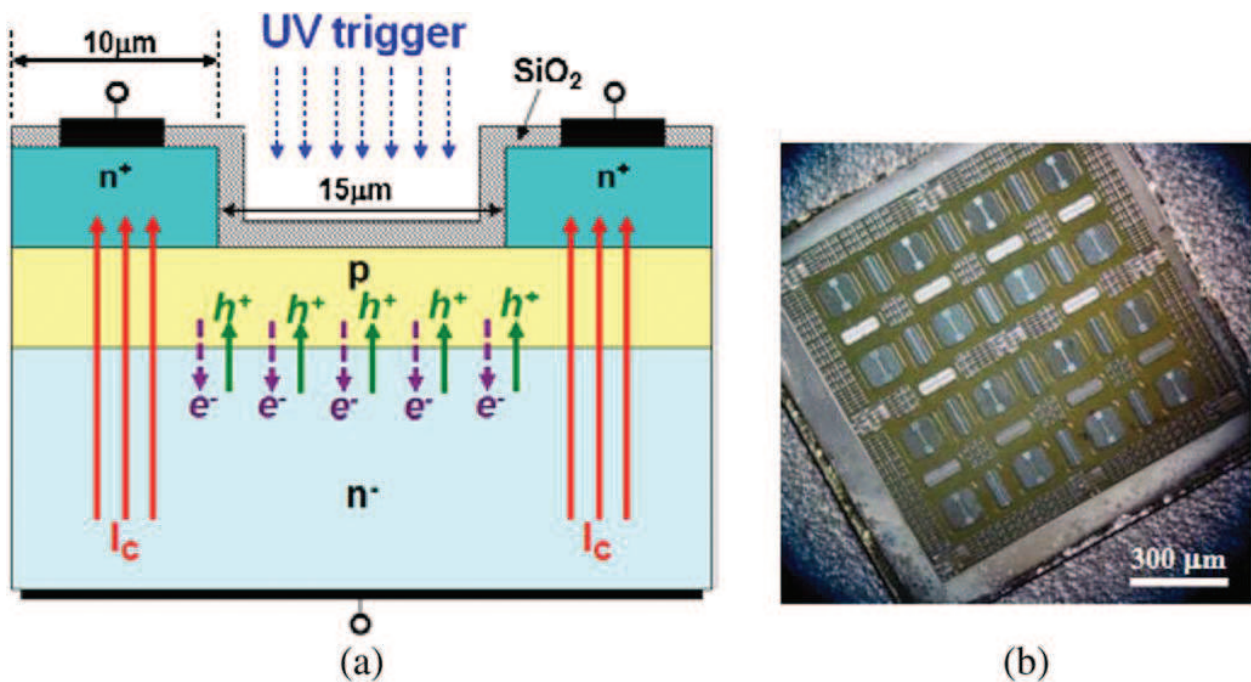


Figure 16. (a) Schematic and (b) micro for optically activated power transistors on an n-type SiC substrate (After Ref. [42]).

Moreover, the Si-LED is also a satisfactory substitution for the ultra-violet (UV) light source given in **Figures 16** and **17** to optically activate the SiC power photo-transistor. Although the optical power emitted from Si-LED is very low, the bipolar-transistor-structured photo-transistor with internal current gain can amplify the photo-induced current. The power devices such as the lateral insulator gate bipolar transistor (L-IGBT) and the lateral extended drain MOS (LEDMOS) can be seen. **Figure 18** shows the schematic cross-sectional view of the investigated n-type L-IGBT, n-type LEDMOS, and p-type LEDMOS devices in the plasma display panel (PDP) scan driver ICs.

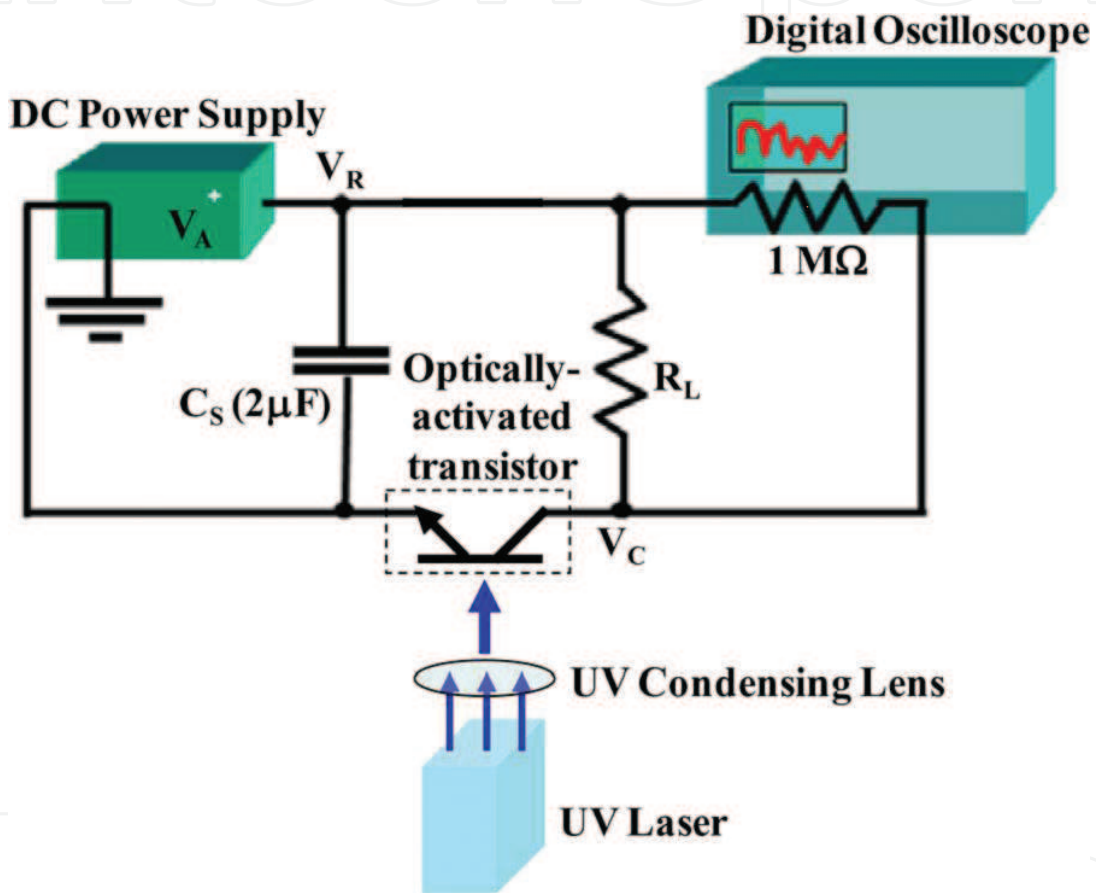


Figure 17. Test circuit for optical switching evaluation (After Ref. [42]).

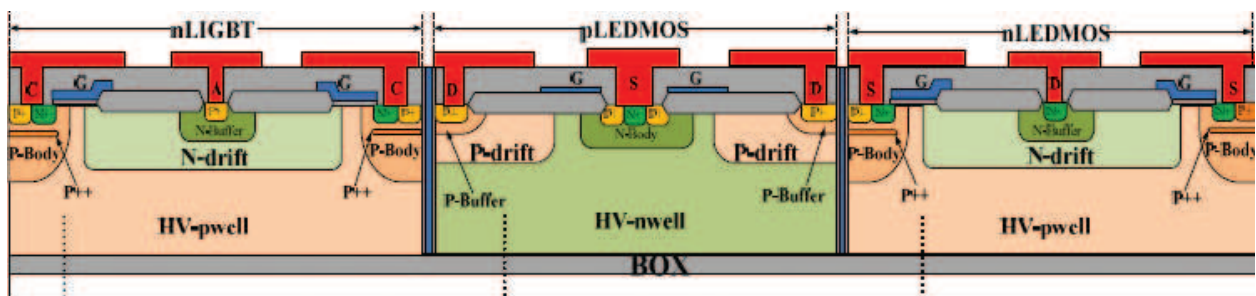


Figure 18. The schematic cross sections of the nLIGBT, nLEDMOS, and pLEDMOS devices (After Ref. [43]).

5. Optocoupler applications

Optical coupling is increasingly used in systems where complex communications must occur across a galvanic isolated boundary. Specially, in factory automation there exists a need for various pieces of equipment to communicate with each other and with a central computer via a bus. Because many of these pieces of equipment involve power devices, disruptive transient electrical signals are generated. To prevent these signals from corrupting the communication bus, optical isolation is used.

Industrial control applications also require optocoupler. An example is the motor controller which includes sophisticated DSP-based functions. Optical isolation is used by the motor controller to control the electrical power to the motor and to monitor the motor's response both electrically and mechanically. In addition, the so-called Internet of Thing (IoT) requires the control of many actuators using Internet communication. There are cases where the internet controller will need to be isolated from the actuator because of severe noise generated in the actuator such as inductive spikes.

Typically, today's optocoupler manufactures place only a single GaAs LED chip on the sending side of the optocoupler. It is left up to the user to provide an interface to the electrical requirements of the LED. This typically entails using discrete components to convert logic level signals or other types of signals to a signal suitable for driving the LED. With a silicon-based LED, however, interface circuits can be built on the same chip as the LED, thus eliminating the need for external, discrete components. Thus, the ability to place circuits on the LED side reduces component count.

Integration of the light-emitting function with silicon allows two distinct advantages over existing technology. One is the integration of a complex circuit function on the LED side of an optocoupler. GaAs LED technology does not support circuit functions. The other is the potential to make multiple bi-directional transmit and receive channels using only two pieces of silicon in a single package. Using SOI offers the potential to integrate both the receive and the transmit functions onto a single chip. The resulting higher level of integration not only lowers cost but simplifies manufacturing for both optocoupler manufacturer and the customer. An added caveat is that many optocouplers do not require high bandwidths with 1 MHz being adequate.

6. Conclusion

The article reviews a Si-LED with the structure being similar to the PMOSFET device. The electroluminescence of reverse-biased silicon p-n junctions could be explained by the direct inter-band, Bremsstrahlung, and indirect band with phonon assistance. Even if the optical emission efficiency of the reverse-biased silicon p-n junctions is very low [6, 44], extremely fast modulation speed can still make them a good choice for light emitters for many applications requiring low-intensity light, such as inter-chip optical interconnects [45–47].

Worley [48] described the methods of laying out avalanche light-emitting diodes in which a heavily doped region of one type of polarity, a second, lighter-doped region of like polarity,

and a heavy-doped region of opposite type polarity are disposed in a silicon substrate. Electrodes are laid out such that light emitted by the avalanching p-n junction is not blocked. Such a structure provides shallow implants to improve efficiency by avoiding the silicon-oxide interface for stability and by avoiding concentrating injections around junction corners to avoid concentrating injections. Combining with the structures like vertical and side-emitting junctions and side-emitting system-on-insulator (SOI) junctions, the reverse-biased silicon p-n junction diode LED is useful in SOI-based optocouplers for the IGBTs [49].

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