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# Heteroepitaxy of III–V Zinc Blende Semiconductors on Nanopatterned Substrates

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Additional information is available at the end of the chapter

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## Abstract

In the last decade, zinc blende structure III–V semiconductors have been increasingly utilized for the realization of high-performance optoelectronic applications because of their tunable bandgaps, high carrier mobility and the absence of piezoelectric fields. However, the integration of III–V devices on the Si platform commonly used for CMOS electronic circuits still poses a challenge, due to the large densities of mismatch-related defects in heteroepitaxial III–V layers grown on planar Si substrates. A promising method to obtain thin III–V layers of high crystalline quality is the growth on nanopatterned substrates. In this approach, defects can be effectively eliminated by elastic lattice relaxation in three dimensions or confined close to the substrate interface by using aspect-ratio trapping masks. As a result, an etch pit density as low as  $3.3 \times 10^5 \text{ cm}^{-2}$  and a flat surface of submicron GaAs layers have been accomplished by growth onto a  $\text{SiO}_2$  nanohole film patterned Si(001) substrate, where the threading defects are trapped at the  $\text{SiO}_2$  mask sidewalls. An open issue that remains to be resolved is to gain a better understanding of the interplay between mask shape, growth conditions and formation of coalescence defects during mask overgrowth in order to achieve thin device quality III–V layers.

**Keywords:** heteroepitaxy, nanopatterning, crystal defects, defect trapping, compound semiconductors, strain relaxation

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## 1. Introduction

III–V compound semiconductors are the materials of choice for making state-of-the-art power electronic and optoelectronic devices, which is due to the outstanding properties of this class of semiconductors. First, they have mostly direct bandgaps covering a broad range between 0.2 eV for InSb [1] and 5.3 eV for zinc blende AlN [2] (at room temperature, respectively).

Also, bandgaps and lattice parameters can be continuously tailored by forming ternary and quaternary alloys. This allows for continuous tuning of the wavelength of light-emitting or absorbing devices and of the lattice parameter in order to reduce lattice misfit to the substrate or between different layers in the device. By decreasing the size of the semiconductor close to the size of the electron wavelength quantum confinement effects come into play, providing an additional degree of freedom for tailoring the emission or absorption wavelength. Another benefit of the carrier confinement arises from the change in the density of states distribution leading to sub-band formation and increased exciton-binding energies in quantum wells, which enables the realization of high-performance LEDs, laser devices and solar cells. Moreover, GaAs, InAs and InSb have very high electron mobilities in the range between 9400 cm<sup>2</sup>/Vs for GaAs [3] and 78,000 cm<sup>2</sup>/Vs for InSb [4], which make them ideal for applications in high-speed power electronics. A particular advantage of zinc blende semiconductors as opposed to their wurtzite-structure counterparts is that piezoelectric fields occur to a much lesser extent in the former because of their high symmetry. In zinc blende layers grown along the [001] direction piezoelectric effects are completely absent [5].

In view of the compelling properties and the great potential for applications but also the high production cost of III–V semiconductor wafers there is a rising demand for integrating III–V structures into the less expensive and well established Si technology [6]. This is important e.g. for developing high-performance light sources on the Si platform. However, growth of high-quality III–V layers on planar Si substrates is hampered by the considerable mismatch of lattice parameters and thermal expansion coefficients as well as by the polar/non-polar surface incompatibility leading to the formation of defects, i.e. threading dislocations (TDs), stacking faults (SFs), twins and anti-phase boundaries (APBs). Threading defects, which cross the active layers of devices, are known to degrade their performance and lifetime by formation of electronic levels in the bandgap inducing non-radiative carrier recombination [7]. In addition, charge carriers are scattered at the defects, the diffusion of impurities is intensified, and defects reaching the layer surface increase its roughness.

In order to reduce the defect density in heteroepitaxial-mismatched layers on planar substrates different strategies have been pursued, like utilization of graded buffer layers [8], thermal cycle annealing and strained layer superlattices [9, 10]. Unfortunately, these approaches are time-consuming, yield limited defect density reductions or require thick buffer layers to be grown. For example, by application of complex thermal cycle annealing and strained layer superlattice processes in the case of GaAs growth on Si(001) an etch pit density lower than  $\sim 1.2 \times 10^6$  cm<sup>-2</sup> could not be achieved [9–11]. An alternative route of eliminating defects consists of using *nanopatterned* instead of planar substrates for the heteroepitaxial growth. In this way, III–V layers of remarkably high structural and morphological quality with respect to their low thickness have been achieved in the last ten years. Heteroepitaxial growth of c-GaN on nanopatterned 3C-SiC/Si(001) has also extensively been studied [12, 13] but in the following emphasis will be placed on arsenides, phosphides and anti-monides.

The book chapter is organized as follows. Section 2 reviews the different heteroepitaxial approaches for growing zinc blende structure III–V layers on nanopatterned mismatched

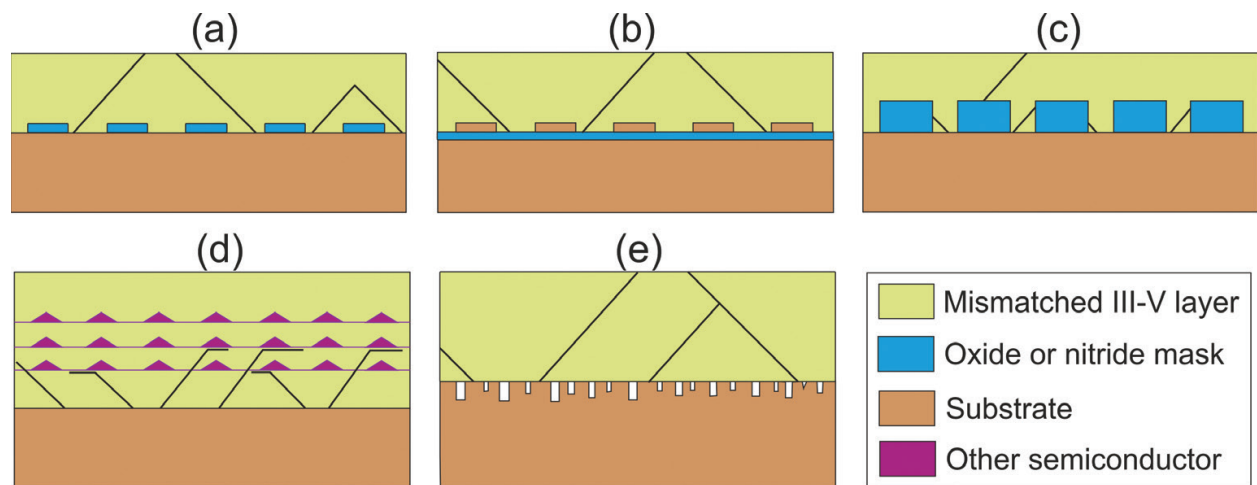
substrates. Focus is put on approaches that aim at a reduction of defect densities by applying different defect elimination mechanisms. Also, the resulting structural, morphological and optical quality of the layers is assessed. After that, Section 3 highlights the relevance of such high-quality III–V layers for advanced applications.

## 2. Heteroepitaxial layer growth and quality on nanopatterned surfaces

In the following semiconductor, heteroepitaxy strategies are reviewed, which use nanopatterned substrates in order to minimize the density of misfit-related defects in III–V layers. **Figure 1** provides an overview. Most of these heteroepitaxy approaches rely on nanoscale selective growth (Section 2.1.1) on a mask-patterned surface, i.e. selective growth on nanoscale crystalline areas, which are laterally surrounded by an oxide or nitride mask layer (**Figure 1(a–c)**). This growth mode, which also enables selective area growth of nanowires and quantum dots (QDs), can be exploited for the epitaxial lateral overgrowth (Section 2.1.2) and aspect ratio trapping (ART) techniques (Section 2.1.3). Moreover, multiple QD layers on planar, buffer layer coated substrates can be exploited as dislocation filters (**Figure 1(d)**, Section 2.2). Yet another approach uses nanoporous substrate surfaces without any mask, where the local three-dimensional elastic lattice relaxation enhances the layer quality (**Figure 1(e)**, Section 2.3).

### 2.1. Growth on mask-patterned surfaces

The use of nanopatterned oxide or nitride masks offers a great potential for the heteroepitaxial growth of mismatched semiconductor layers. Low-defect III–V layers have been dem-



**Figure 1.** Overview of heteroepitaxial growth methods on nanopatterned substrates. The graphs show schematic cross-sections of the layer systems, respectively. (a–c) Three variants of mask-controlled growth with nucleation on nanoscale substrate areas: (a) thin mask film with nanoopenings, (b) continuous mask film with substrate nanoislands on top, (c) mask nanoopenings with aspect ratio  $>1$  (aspect ratio trapping technique), (d) growth using multiple QD layers as dislocation filters and (e) growth on a mask-free nanoporous substrate. In (a–e) the inclined black lines indicate the propagation of threading crystal defects.

onstrated on substrates covered with (i) a mask layer having nanoscale line or round shaped openings, or with (ii) semiconductor islands or mesas on top of a continuous mask layer. In both variants the nanoscale semiconductor areas on the surface serve as nucleation sites for the III–V growth. Due to lateral growth the overgrown islands eventually coalesce to form continuous III–V layers, bridging the mask areas in between them.

### 2.1.1. Nanoscale selective growth

Nanoscale selective growth (NSG) describes selective homoepitaxial or heteroepitaxial growth on the unmasked areas of a partially masked substrate surface. It represents a key mechanism in the growth of mismatched layers on mask patterned substrates, first proposed by Luryi and Suhir [14]. In the following two subsections, the conditions required for NSG are analysed theoretically and corresponding experimental observations are described [15].

#### 2.1.1.1. Theoretical description

On an ideal surface, i.e. in absence of nucleation centres such as impurities, defects or surface steps, selective growth can be achieved (i) by surface out-diffusion of the adatoms from the masked to the unmasked areas and/or (ii) by adatom desorption before the cluster formation starts. The surface out-diffusion mechanism works if the lateral dimensions of the masked areas are chosen smaller than the surface migration length of the adatoms, i.e. the average diffusion length before desorption or agglomeration with other atoms. This allows the adatoms to diffuse to the unmasked areas and to suppress crystal nucleation on the masked areas resulting in selective growth in the mask openings [15]. In the case (ii) the surface diffusion length of the adatoms without coming across other adatoms has to be less than a characteristic length describing the average distance between adjacent adatoms [16]. NSG can be described by an equation analogous to that for step-flow growth with a critical cluster size of 1, where arriving atoms diffuse to a step edge:

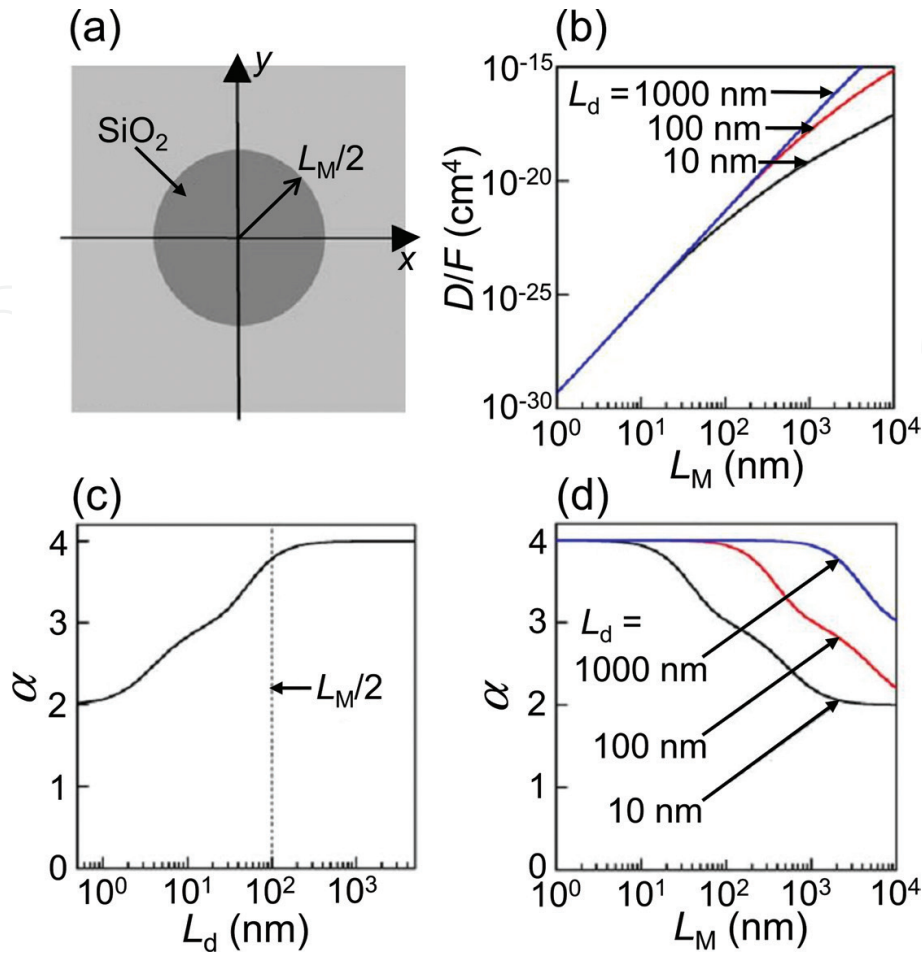
$$\frac{\partial n}{\partial t} = F - \frac{n}{\tau_{\text{des}}} + D \nabla^2 n \quad (1)$$

Here,  $n$  denotes the areal density of adatoms on the mask at time  $t$ ,  $F$  is the flux of atoms arriving on a unit mask area per unit time  $t$ .  $\tau_{\text{des}}$  designates the desorption-limited adatom residence time on the surface, and  $D$  the surface diffusion constant.

In the vicinity of the substrate-mask boundary a gradient of the surface potential occurs, which provides the driving force for diffusion of adatoms from the mask to the substrate [16, 17]. The potential gradient also prevents the adatoms to diffuse in reverse direction, i.e. from the GaAs surface onto the mask. For a circular  $\text{SiO}_2$  mask with diameter  $L_M$  as displayed in **Figure 2** and the boundary condition  $n(L_M/2, t) = 0$ , the steady state is given for [15]:

$$\frac{D}{F} = \frac{\pi L_M^4}{4N} \sum_{m=1}^{\infty} \left[ z_m^2 + \left( \frac{L_M}{2L_d} \right)^2 \right]^{-1} \sim L_M^\alpha \quad (2)$$

For selective growth the total number of Ga adatoms on the  $\text{SiO}_2$  mask  $N$  is small and can be set to 1 without affecting the results for  $\alpha$ .  $z_m$  is the  $m$ th zero of the zero-order Bessel function,  $L_d$  is the diffusion length of a Ga atom on a planar  $\text{SiO}_2$  surface and  $\alpha$  is a



**Figure 2.** (a) Schematic of a SiO<sub>2</sub> disc of diameter  $L_M$  deposited on a GaAs surface, (b) calculated ratio  $D/F$  versus  $L_M$  for different  $L_d$  according to Eq. (2). (c, d) Diagrams showing the exponent  $\alpha$  as a function of (c)  $L_d$  and (d)  $L_M$ , obtained from (b), respectively. In (c)  $L_M = 200$  nm ( $\alpha = 3.8$ ), where the dashed line marks  $L_d = L_M/2$ . (Reproduced from [15], with the permission of AIP Publishing.)

dimensionless exponent [15]. **Figure 2(b)** plots  $D/F$  as a function of  $L_M$  for different  $L_d$ , and **Figure 2(c)** and **(d)** display the resulting exponent  $\alpha$  versus  $L_d$  and  $L_M$ , respectively. With increasing  $L_M$  and decreasing  $L_d$   $\alpha$  decreases from 4 to 2, owing to desorption. In the limit  $\alpha = 4$  ( $L_M \ll L_d$ ) suppression of growth on the mask is achieved only by surface out-diffusion, whereas for  $\alpha = 2$  ( $L_M \gg L_d$ ) selective growth is accomplished solely by desorption. In the latter case the critical flux below which selective growth occurs obeys an exponential scaling law:

$$F_c \sim \frac{v_0^2}{C} \exp\left[-\frac{2E_{\text{des}} - E_{\text{diff}}}{kT}\right], \quad (3)$$

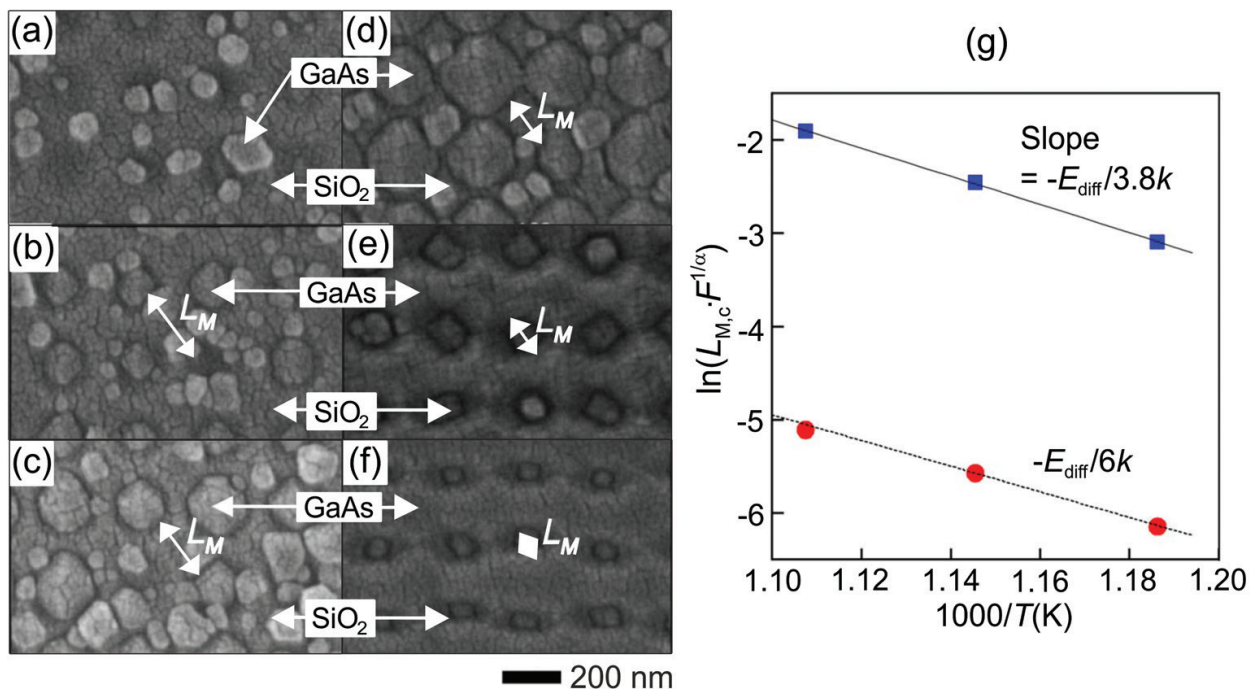
where  $E_{\text{des}}$  denotes the activation energy for adatom desorption,  $E_{\text{diff}}$  is the activation energy for adatom surface diffusion,  $T$  is the absolute temperature,  $k$  is the Boltzmann constant and  $v_0$  is a desorption rate constant. Commonly,  $2E_{\text{des}} > E_{\text{diff}}$  meaning that the critical flux below which nucleation on the SiO<sub>2</sub> mask can be suppressed increases with rising temperature.

### 2.1.1.2. Experimental observations

Experimentally, two main types of nanopatterned substrates have been utilized for oxide mask-based NSG/nanoheteroepitaxial growth: (i) substrates covered with a mask film having round or line shaped openings and (ii) substrates capped with a continuous mask layer with nanoscale semiconductor islands or horizontal wires on top. On the one hand, the fabrication of type (i) substrates is more facile. On the other hand, type (ii) offers the advantage of compliant nanoscale substrate islands, which can accommodate a portion of the misfit strain.

Approach (i) has been extensively studied by Lee et al. [16, 17] and Lee and Brueck [15]. They used  $\text{SiO}_2$  films deposited on GaAs(001) substrate by electron beam evaporation. For the patterning of the  $\text{SiO}_2$  films interference lithography followed by dry etching [15] was deployed, resulting in arrays of approximately circular mask openings with pattern periods between 260 and 350 nm. By varying the dry etching time different opening sizes were realized. For the longer etching times the openings coalesced leaving isolated  $\text{SiO}_2$  islands on the GaAs substrate. Scanning electron microscopy (SEM) images of the surface after molecular beam epitaxy (MBE) growth at  $570^\circ\text{C}$  using a Ga flux of  $F = 0.33 \times 10^{14}$  atoms/( $\text{cm}^2\text{s}$ ) show that the growth becomes increasingly selective [15], when reducing the mask dimension  $L_M$  from infinity to 70 nm (**Figure 3(a–f)**). For these conditions the critical mask dimension  $L_{M,c}$  below which growth on the mask is completely inhibited amounts to  $\sim 120$  nm. The experimental  $L_{M,c}$  results for different growth temperatures and Ga fluxes confirm that the temperature has the strongest influence on  $L_{M,c}$ . **Figure 3(g)** depicts a plot of  $\ln(L_{M,c} \cdot F^{1/\alpha})$  over  $1/T$  for  $\alpha = 3.8$  and  $\alpha = 6$ , where  $\alpha = 3.8$  is the exponent, which the calculations (Eq. (2), **Figure 2**) predict for the experimental mask dimensions, and  $\alpha \approx 6$  has been found by means of growth kinetic MBE simulations [18] for a critical cluster size of 1 by using different boundary conditions than in the study of Lee et al. [15]. From the slope the activation energy  $E_{\text{diff}}$  for surface diffusion of a Ga adatom on a  $\text{SiO}_2$  surface was determined in the range between  $\sim 4.9$  eV for  $\alpha = 3.8$  and  $\sim 6.8$  eV for  $\alpha = 6$ , which significantly exceeds the activation energy for surface diffusion of a Ga adatom on a GaAs surface of  $\sim 1$  eV [19]. The short diffusion lengths of Ga adatoms on  $\text{SiO}_2$  related to the large  $E_{\text{diff}}$  comply with the small critical mask dimensions observed in the experiments.

Regarding the morphology of the GaAs islands selectively grown in circular mask openings it has been found that the height as well as the shape of the islands varies with the diameter of the openings [17]. With decreasing opening diameter the island height increases, because of the larger mask area and related increased number of Ga atoms diffusing from the mask to the GaAs surface (**Figure 4(a)**). Side-view SEM images show that the cross-sections of the GaAs islands change from a round profile for small opening diameters to trapezoidal shapes for larger diameters (**Figure 4(b)**). In all cases, the total GaAs volume deposited in the mask openings is considerably smaller than the estimated volume of a continuous GaAs layer on a mask-free GaAs surface using the same deposition time, indicating that not all Ga adatoms impinging on the  $\text{SiO}_2$  areas migrate to the mask openings. According to the estimated volume of GaAs islands deposited at  $630^\circ\text{C}$  on a continuous  $\text{SiO}_2$  film a sticking coefficient of Ga atoms on  $\text{SiO}_2$  of  $\sim 0.13$  was estimated [17]. A more recent study found a value of  $\sim 0.007$  at  $632^\circ\text{C}$  and confirmed the expected exponential dependence on the inverse absolute temperature [20].

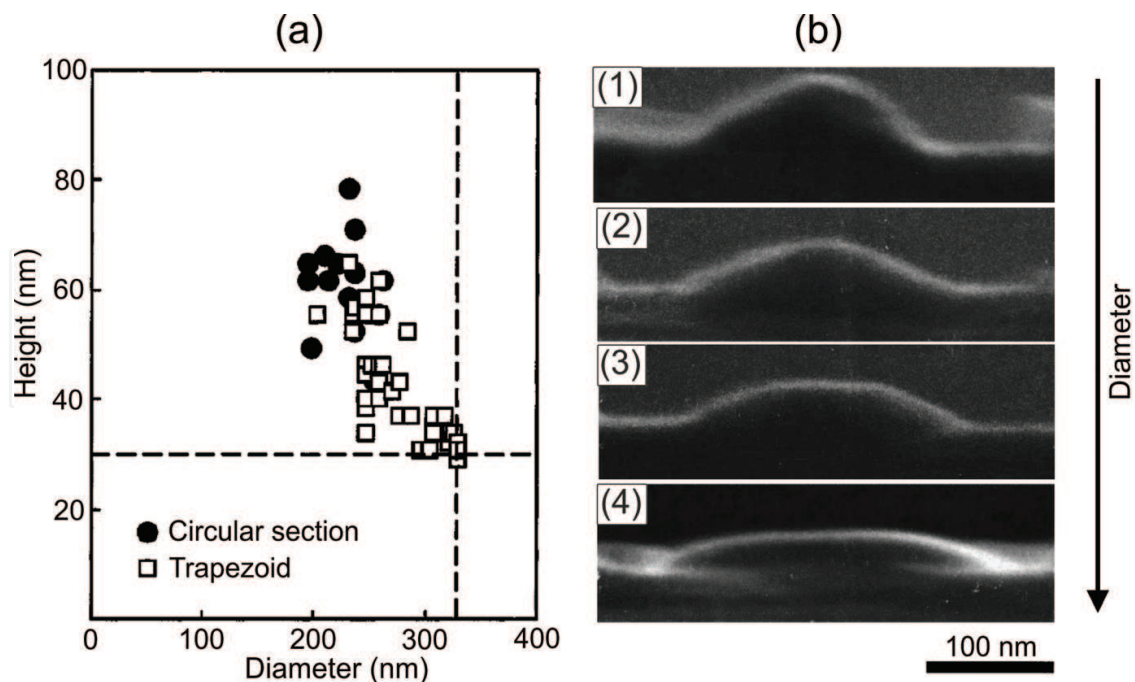


**Figure 3.** Top-view SEM images showing GaAs grown by MBE at 570°C on GaAs(001) covered with SiO<sub>2</sub> masks having different lateral dimensions  $L_M$ . (a) Continuous SiO<sub>2</sub> film, i.e. infinite  $L_M$ , (b)  $L_M \approx 270$  nm, (c)  $L_M \approx 220$  nm, (d)  $L_M \approx 180$  nm, (e)  $L_M \approx 120$  nm, and (f)  $L_M \approx 70$  nm. The periodic features in (b) through (d) are SiO<sub>2</sub> mask openings, while those in (e) and (f) are SiO<sub>2</sub> islands. (g) A plot of  $\ln(L_{M,c} \cdot F^{1/\alpha})$  over  $1/T$  for NSG of GaAs on SiO<sub>2</sub>-nanopatterned GaAs(001) and two different exponent values  $\alpha = 3.8$  and  $\alpha = 6$ . The values of the critical mask dimension  $L_{M,c}$ , the flux  $F$  and the growth temperature  $T$  are deduced from MBE growth experiments conducted at three different temperatures. Straight lines are Arrhenius fits. (Reproduced from [15], with the permission of AIP Publishing.)

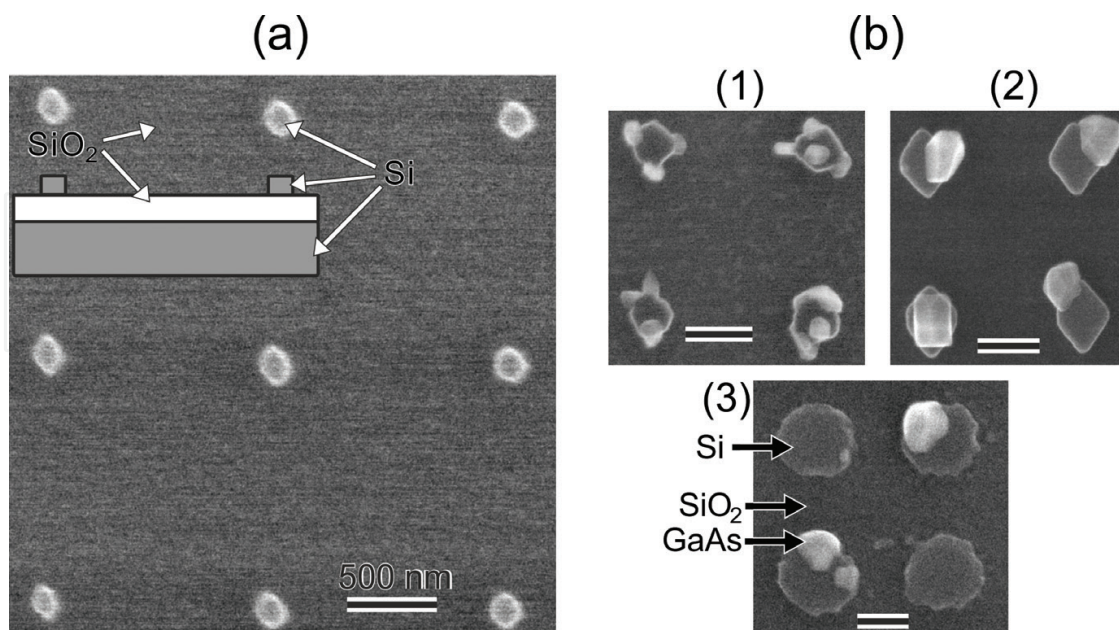
In the second approach, nanoscale Si islands on a continuous SiO<sub>2</sub> film mask serve as nucleation sites for the heteroepitaxial growth. Such patterned surfaces can be obtained by patterning of silicon-on-insulator (SOI) wafers, i.e. by removing parts of the Si top layer. Zubia et al. studied the metalorganic vapour phase epitaxy (MOVPE) growth of GaAs on square arrays of SOI islands with diameters between 100 and 280 nm, and a pitch of 500 nm (**Figure 5(a)**) [21, 22].

During the initial growth stage crystalline GaAs nuclei form on the Si islands, where the number and size of the nuclei strongly depend on the temperature-controlled surface diffusion (**Figure 5(b)**) [21]. For low temperatures multiple GaAs crystals were observed on each Si island, while only a fraction of the Si islands was covered with GaAs for high temperatures. At an optimum temperature of 605°C each Si island has one GaAs crystal on top. The size, shape and structural quality of these GaAs nuclei play an important role for the subsequent lateral growth (performed at optimum temperature). For an initial growth temperature below 605°C various types of defects such as twins appear in the overgrown GaAs, while for 605°C (**Figure 6**) only stacking faults on the {111} planes have been found by transmission electron microscopy (TEM) diffraction [21]. In contrast, threading dislocations represent the dominant defect in GaAs growth on planar Si. The spacings of the Moirée fringes visible in TEM images as well as the diffraction spot spacings consistently indicate a residual lattice strain of 0.4–0.7% in the GaAs [21], i.e. given the GaAs-Si lattice misfit of ~4% the nanoheteroepitaxial GaAs is predominantly relaxed. However, it has not been clarified whether the relaxation originates from misfit dislocations (MDs) at the Si/GaAs heterointerface, from elastic relaxation or from both.





**Figure 4.** (a) Diagram plotting the height of GaAs islands grown by MBE selectively in  $\text{SiO}_2$  mask openings as a function of opening diameter. The vertical and horizontal dotted lines represent the pattern period and the thickness of a GaAs layer on a mask-free GaAs substrate using the same growth parameters, respectively. (b) Side-view SEM images showing the diameter-dependent transition from round to trapezoidal cross-section profiles of the GaAs islands selectively grown in the mask openings. (Reproduced from [17], with the permission of AIP Publishing.)

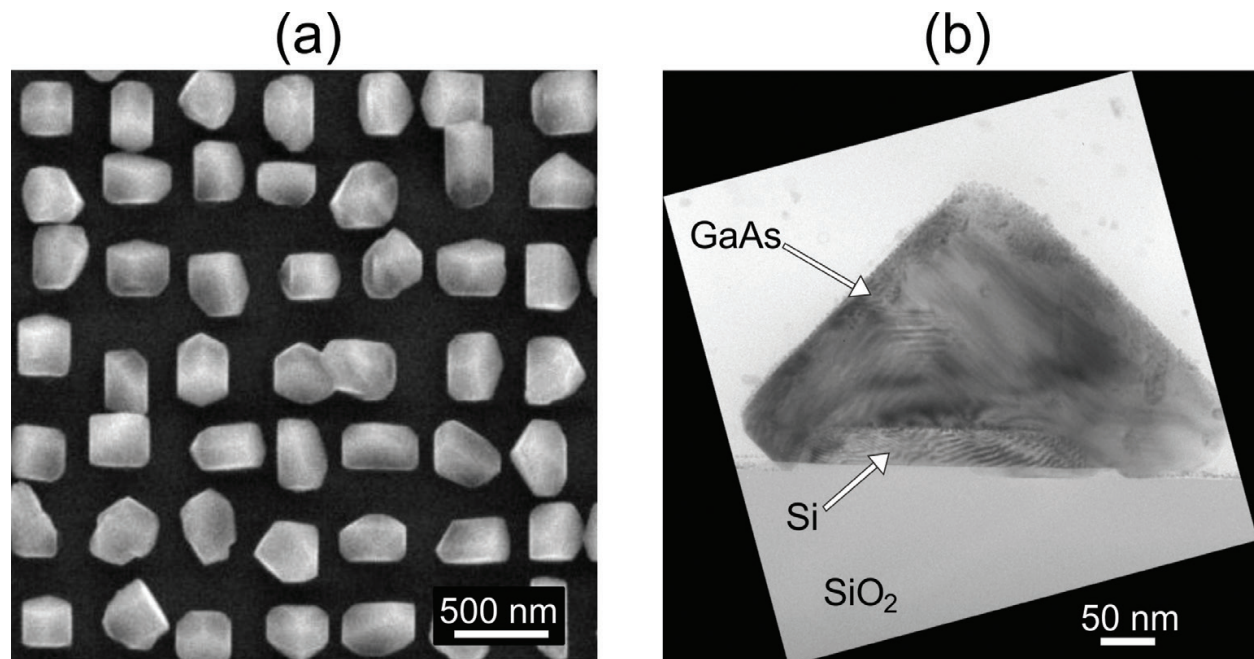


**Figure 5.** (a) Plan view SEM image of the patterned silicon-on-insulator (001) substrate with Si nanoislands on top. The inset shows a schematic cross-section of the structure. (b) Plan view SEM images of GaAs crystallites on silicon islands for different growth temperatures: (1) 519°C, (2) 605°C and (3) 734°C. The scale bars in (b) are 200 nm [22].)

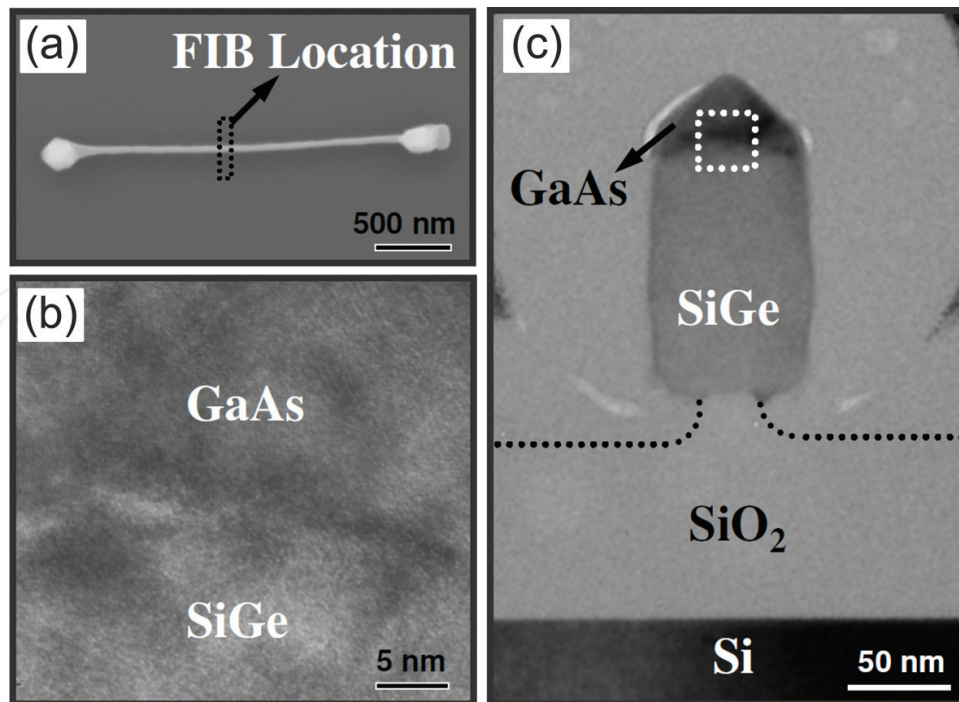
Apart from nanoscale semiconductor islands also lateral nanowires on a continuous mask film can be used for selective three-dimensional growth of III–V semiconductors. On Si(001) substrate Chin et al. fabricated  $\text{Si}_{0.35}\text{Ge}_{0.65}$ -on- $\text{SiO}_2$  structures by deposition of a  $\text{Si}_{0.85}\text{Ge}_{0.15}$  layer onto a SOI substrate and subsequent two-step Ge condensation process [23]. After photolithography and dry etching lateral  $\text{Si}_{0.35}\text{Ge}_{0.65}$  nanowires on  $\text{SiO}_2$  were obtained, which served for the study of selective migration enhanced epitaxy (MEE) growth of GaAs onto the nanowires (**Figure 7**). Owing to the pulsed Ga and As fluxes and intermittent annealing phases in MEE, selective growth is achieved even in the case of masks patterned on the micrometre scale. Cross-sectional TEM images reveal that GaAs grows pseudomorphically and defect-free in the form of faceted planar nanowires on top of  $\sim 75$  nm wide  $\text{Si}_{0.35}\text{Ge}_{0.65}$  nanowires (**Figure 7(c)**). Defects that relieve the strains due to the  $\sim 1.5\%$  lattice misfit are absent because both  $\text{Si}_{0.35}\text{Ge}_{0.65}$  and GaAs lattice regions relax elastically in the lateral and vertical directions.

### 2.1.2. Lateral overgrowth of oxide mask and layer coalescence

By means of continued deposition on a mask nanopatterned substrate the selectively formed heteroepitaxial crystals grow and finally coalesce to form a continuous layer. In 1991 Ismail et al. were probably the first who—unintentionally—performed heteroepitaxial overgrowth of a nanometre thin holey  $\text{SiO}_x$  film [24]. GaAs was deposited by two-step MOVPE growth onto a sawtooth-patterned vicinal Si(001) substrate defined by  $\{111\}$  surface facets. The two-step growth was followed by either an ex situ rapid thermal annealing at  $900^\circ\text{C}$  or a thermal cycle growth. In TEM analyses, it was found that a  $\sim 1$  nm thin  $\text{SiO}_x$  film covered the Si/GaAs interface. The GaAs layer exhibited an exceptionally low etch pit density of  $<10^4$   $\text{cm}^{-2}$  at  $0.8$   $\mu\text{m}$  distance from the heterointerface, and a dislocation density evaluated from plan-view TEM of



**Figure 6.** Plan view SEM (a) and cross-sectional TEM image (b) of 100 nm GaAs MOVPE growth on nanopatterned silicon-on-insulator (001) substrate. The GaAs nucleation was performed at  $605^\circ\text{C}$  [22].)



**Figure 7.** (a) Top-view SEM image depicting a  $\text{Si}_{0.35}\text{Ge}_{0.65}$  nanowire with a GaAs layer grown on top, (b, c) cross-sectional TEM images confirming pseudomorphic, defect-free GaAs on the  $\text{Si}_{0.35}\text{Ge}_{0.65}$ . Image (b) covers the region defined by the white dotted rectangle in (c). The TEM specimen was prepared by focussed ion beam at the position marked by an arrow in (a). (Reproduced from [23], with the permission of AIP Publishing.)

$<10^5 \text{ cm}^{-2}$  for  $1 \mu\text{m}$  layer thickness. Based on the limited TEM data, two different mechanisms were considered to account for the occurrence of such a low-defect density: firstly, the orientation of the Si substrate could be transferred to the GaAs layer via Si-GaAs contacts in small pinholes in the interfacial oxide, where MDs formed. Because of the small area fraction of the pinholes, the overall MD density was strongly reduced. The also observed twins and SFs are likely to originate from the roughness of the oxide layer [25]. Secondly, the obtained GaAs layer could have resulted from a type of graphoepitaxy, where the GaAs ‘perceives’ only the symmetry and the inclination of the  $\{111\}$  facets and not the exact positions of the Si atoms. As the  $\text{SiO}_x$  film separated the GaAs and Si crystals, relaxed dislocation-free GaAs formed directly above the  $\text{SiO}_x$  during the final annealing step.

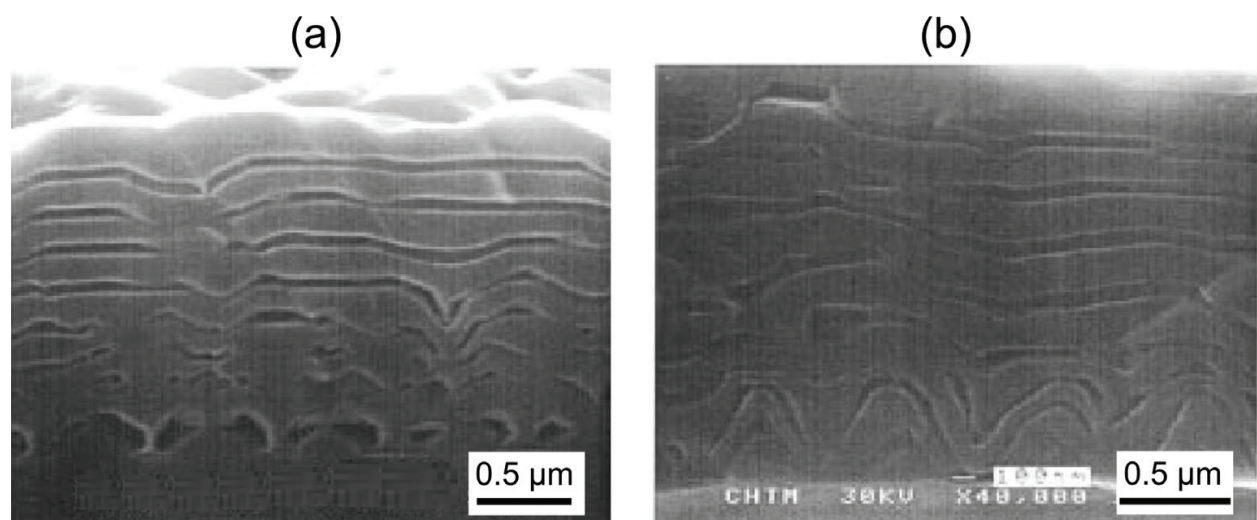
Following a theoretical study on the concept of nanoheteroepitaxy by Zubia and Hersee [26], Hersee et al. reported that the faceting of the forming heteroepitaxial NSG crystals plays a decisive role for the island coalescence and thus for the surface morphology of the coalesced layer [27]. Like in the earlier work of Zubia et al. [21] heterogeneous faceting was observed, which leads to locally different growth rates. To analyse explicitly the layer coalescence behaviour, GaAs and  $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$  marker layers were grown by MOVPE onto a GaAs(001) substrate nanopatterned with a holey  $\text{SiO}_2$  film [27]. After coalescence different growth habits of the layer surface were observed along two orthogonal cleaving directions by using cross-section SEM [27] (**Figure 8**): in one direction a rapid surface planarization occurred, while the growth remained conformal to the substrate geometry in the orthogonal

direction. This can provoke again surface roughening in the former direction, which slowly decays with increasing layer thickness. However, still significant large-scale variations of the layer thickness in the order of 100 nm were present even for layer thicknesses in excess of 1  $\mu\text{m}$ .

More recently, the growth of coalesced heteroepitaxial III–V layers on highly mismatched substrates patterned with nanoporous or nanohole oxide masks was investigated in the cases of GaSb on GaAs(001) (misfit  $\sim 7.8\%$ ) and GaSb on Si(001) (misfit  $\sim 12\%$ ).

Jha et al. deployed a  $\text{SiO}_2$  nanohole mask (hole diameter  $\sim 20$  nm) fabricated by blockcopolymer lithography and reactive ion etching for MOVPE heteroepitaxy of GaSb on GaAs(001) and reported an improved quality of the GaSb layers [28]. For a layer thickness of 200 nm the width of the (004) X-ray rocking curve decreased to  $\sim 40\%$  of that of GaSb grown on non-patterned GaAs. Moreover, the GaSb layer on the nanopatterned GaAs exhibited a strongly reduced surface roughness as measured by atomic force microscopy (AFM), and the absence of threading dislocations as indicated by cross-sectional TEM. However, twins on the  $\{111\}$  planes were observed, which seem to nucleate on the  $\text{SiO}_2$  mask.

Nanoheteroepitaxial growth with reduced surface roughness and defect density was demonstrated by Nakamura et al. for even larger misfits, i.e. for the GaSb/Si system [29]. They used ultrathin  $\text{SiO}_2$  films (thickness  $\sim 0.3$  nm) with openings of a high areal density of  $10^9$  to  $10^{12}$   $\text{cm}^{-2}$  as masks on the Si(001) substrate. The growth was performed in three stages by means of MBE (**Figure 9(a)**): In the first stage elastically strain-relaxed GaSb nanodots formed in the  $\text{SiO}_2$  openings, followed by nanodot coalescence in the second stage. During the third stage, which was conducted at a higher temperature than stages 1 and 2, the final layer with a flattened surface was obtained. For optimum growth temperatures a root mean square surface roughness of  $\sim 7$  nm was achieved for a total layer thickness of  $\sim 90$  nm. Cross-sectional HRTEM images indicated a reduced threading dislocation density of  $\sim 10^8$ – $10^9$   $\text{cm}^{-2}$

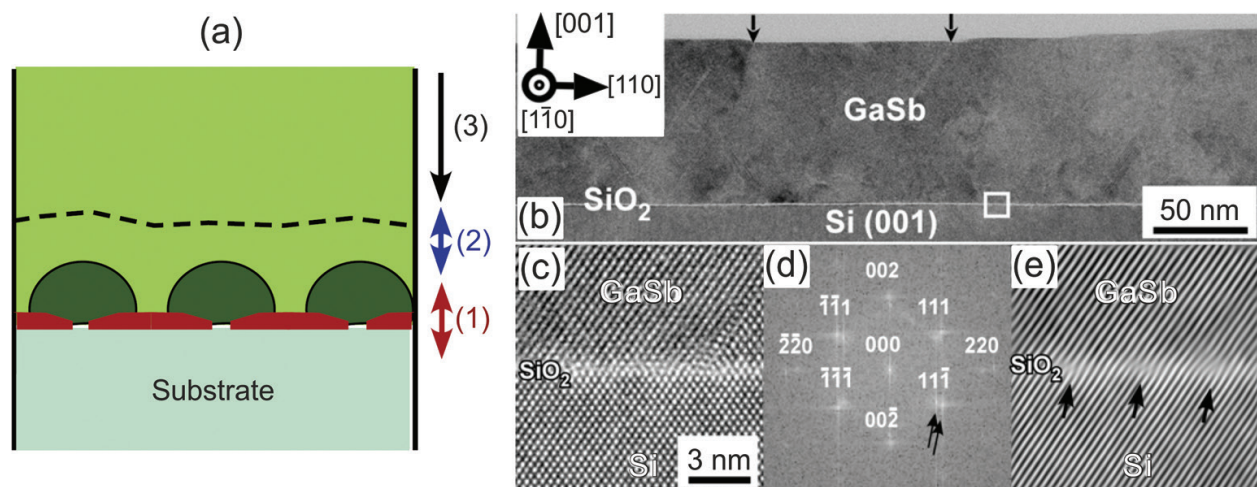


**Figure 8.** Cross-section SEM images of a coalesced GaAs layer grown on oxide nanopatterned GaAs(001) substrate along two orthogonal cleaving directions (a, b). The darker layers are intentionally grown  $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$  layers serving as thickness markers. (Copyright 2002 IEEE. Reprinted, with permission, from [27].)

as compared to  $10^9 \text{ cm}^{-2}$  for a  $\sim 1 \mu\text{m}$  thick GaSb layer grown by using an AlSb initiation layer (**Figure 9(b)**). According to Fourier transformation analysis of HRTEM images the GaSb lattice was almost completely relaxed (**Figure 9(c)** and **(d)**). As, except for the openings, GaSb and Si were separated by the ultrathin  $\text{SiO}_2$  layer, the misfit was not accommodated by MDs. Rather, the GaSb lattice planes above the  $\text{SiO}_2$  exhibited close-to-equilibrium spacings, i.e.  $\sim 12\%$  wider spacings than the corresponding Si planes beneath the oxide (**Figure 9(e)**), which can be attributed to the elastic relaxation in the nanodots during the growth. The direct Si/GaSb contacts in the openings, but also the very thin oxide layer enable a transfer of the epitaxial relationship.

Heteroepitaxial growth and continuous layer formation has also been studied by using grating-shape nanopatterned oxide masks. He et al. [30] applied a three-stage MOVPE growth scheme to obtain a smooth GaAs layer surface on a Si(001) substrate: the first stage served for selective deposition of GaAs in the trenches, while in the second and third stages coalescence and planarization of the GaAs layer were achieved. Repetition of the experiment for different trench orientations showed that this has a strong impact on the coalescence and consequently on the surface roughness of the layer. Minimum surface roughness was observed for a trench orientation parallel to [410], i.e.  $\sim 31^\circ$  inclined to the [110] direction, due to maximum and uniform lateral growth rate. **Figure 10** compares the GaAs layer morphology for different trench orientations on the basis of AFM and cross-sectional SEM images.

Another approach compassing nanoscale selective growth and filtering of defects relies on MBE growth through the openings of a silica colloidal monolayer [31]. First, a GaAs buffer layer is grown on a planar Si(001) substrate, partially relieving the misfit by formation of extended defects. The subsequently deposited silica sphere monolayer enables selective growth of GaAs in the monolayer openings on the GaAs buffer surface (**Figure 11**). Due to the conical shape of the openings, propagating defects are largely stopped at the silica surfaces.



**Figure 9.** (a) Schematic of the three-step MBE growth procedure, (b) cross-sectional HRTEM image of a GaSb layer on Si(001) substrate obtained by the procedure of (a), (c) Detail of (b) showing the marked square area in (b), (d) Fourier transform of (c), (e) inverse Fourier transform using the  $(11\bar{1})$  and  $(\bar{1}\bar{1}1)$  lattice planes. (Copyright IOP Publishing. Reproduced with permission from [29]. All rights reserved.)

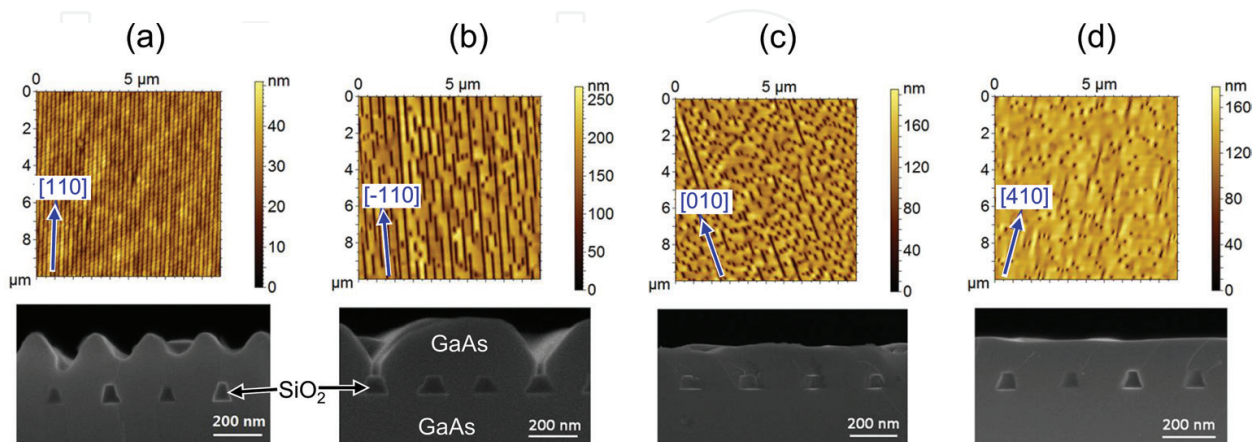
When the growing GaAs surface has passed half the height of the spheres elastic relaxation in the lateral directions contributes to reduce the misfit strains.

### 2.1.3. Aspect ratio-trapping techniques

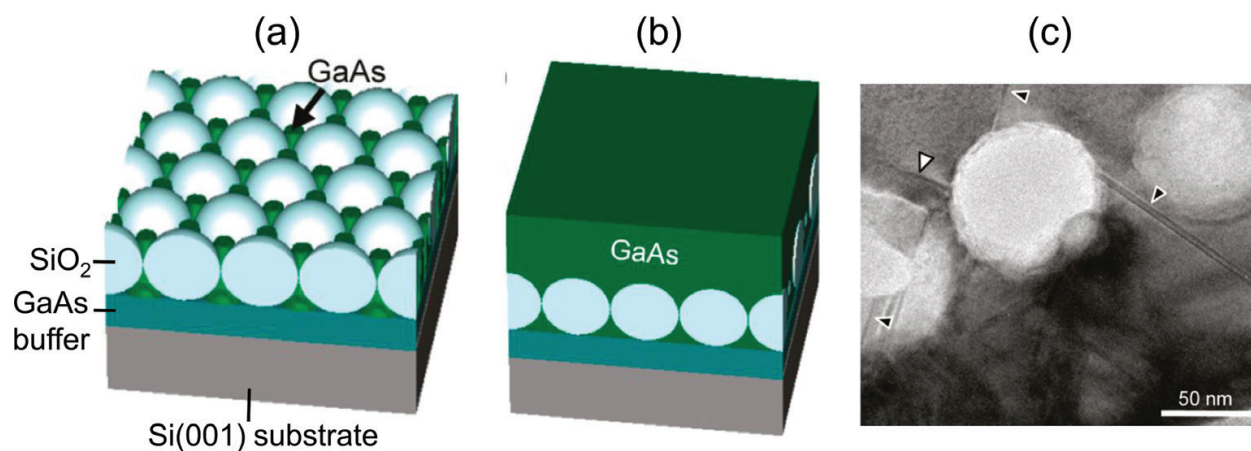
Although three-dimensional elastic relaxation of the lattice relieves the misfit strains during lateral overgrowth of thin masks, defects at the heterointerface may still form threading segments, which extend far into the layer. In order to stop the propagation of such defects ART techniques have been developed, where the growth areas are situated at the bottom of cylindrical or trench shaped mask openings whose height exceeds their lateral width. Therefore, defects that propagate in the layer on planes inclined to the substrate surface, such as {111} slip planes in the case of a {001} substrate, get trapped at the intersections of the slip planes with the mask walls and are hence hindered to further spread into the layer. Essentially, the lattice undergoes a plastic relaxation where the defects are confined to a region close to the heterointerface and mask sidewall regions. Owing to the efficient plastic relaxation and considerable mask height the layer is nearly completely relaxed when reaching the mask top so that elastic relaxation during mask overgrowth can be neglected.

#### 2.1.3.1. Growth on surfaces patterned with a trench mask

Among the ART techniques those deploying  $\text{SiO}_2$  or  $\text{SiN}_x$  masks with trench shaped openings along  $[110]$  or  $[\bar{1}\bar{1}0]$  have been most extensively studied. The trench masks can be fabricated (i) by oxidation of the Si substrate surface, lithography and reactive ion etching, or alternatively (ii) by using processes based on the established shallow trench isolation technology [32]. In particular, selective-area MOVPE growth of InP and GaAs on trench mask patterned Si(001) substrate has attracted great interest [25, 33–43]. Although the detailed defect reduction mechanism depends on the trench dimensions, on the shape of the trench bottom as well as on the heteroepitaxial growth sequence and conditions, the common characteristic



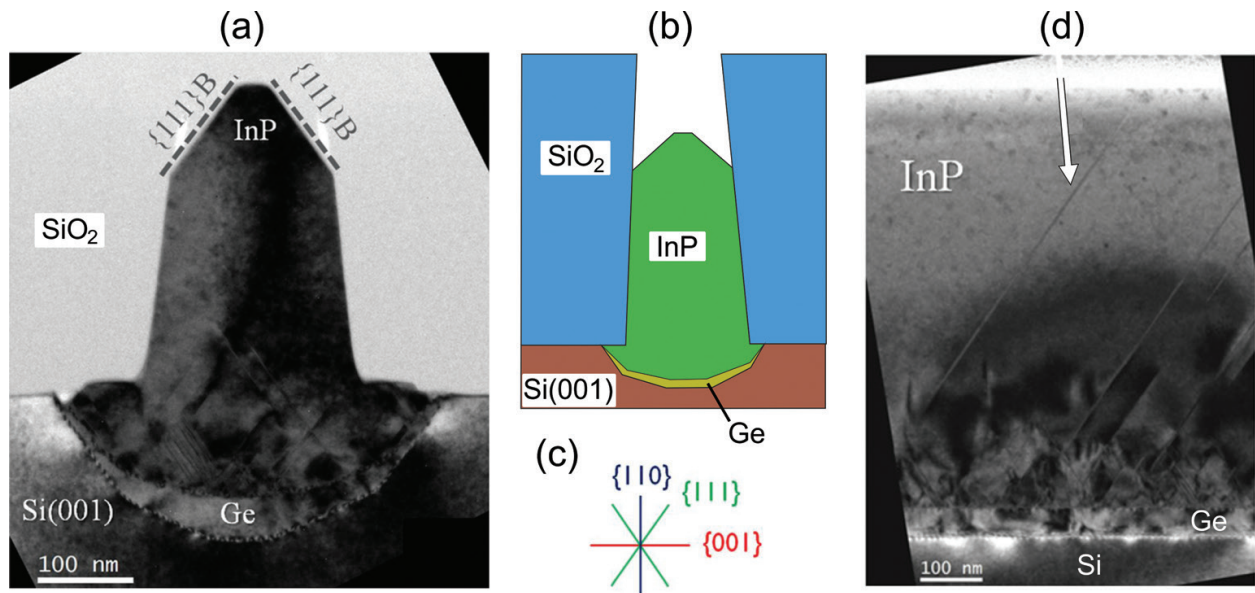
**Figure 10.** AFM images (top row) and cross-sectional SEM images (bottom row) of GaAs layers after the second MOVPE growth stage on  $\text{SiO}_2$  stripe patterned Si(001), with stripe orientations: (a)  $[110]$ , (b)  $[\bar{1}\bar{1}0]$ , (c)  $[010]$  and (d)  $[410]$ . (Reproduced from [30], with the permission of AIP Publishing.)



**Figure 11.** (a, b) Schematics illustrating the growth of a GaAs layer onto a  $\text{SiO}_2$  nanosphere layer covered  $\text{Si}(001)/\text{GaAs}$  buffer template, (c) cross-section TEM image corresponding to (b). The black arrowheads and the white arrowhead point to  $\{111\}$  stacking faults and to a defect off from  $\{111\}$ , respectively. (Reprinted (adapted) with permission from [31]. Copyright 2011 American Chemical Society.)

of trench-based ART techniques consists in the stopping of propagating misfit defects, i.e. dislocations, stacking faults and twins, at the trench sidewalls. This applies to defects on  $\{111\}$  planes parallel to the trench direction. However, threading defects running on  $\{111\}$  planes inclined to the trenches are not trapped and can cross the layer (**Figure 12**). XRD  $\omega$ - $2\theta$  scans of the (004) reflection demonstrated that the selectively grown InP and GaAs regions are almost fully relaxed [36, 40]. Obviously, the aspect ratio of the trenches (height divided by the width) determines the fraction of threading defects that are trapped by the sidewalls. For aspect ratios larger than 2 misfit defects are confined to the lower part of the trenches, whereas the upper part has a high crystal quality with an etch pit density close to zero [43].

One of the key factors for the formation and trapping efficiency of defects is the shape of the trench bottom. Orzali et al. found that in the case of a recess in the Si substrate defined by a  $\text{Si}(001)$  bottom surface and  $\text{Si}\{111\}$  facets in the vicinity of the sidewalls MOVPE GaAs nucleated preferentially on the  $\{111\}$  facets, thus forming a central void after growth front coalescence [25]. SFs and TDs originating from the trench bottom annihilated at the oxide sidewalls, while only few twin lamellae crossed the layer and reached the surface. Merckling et al., who used a Ge buffer layer in a 'round' Si recess defined by  $\{111\}$ ,  $\{112\}$  and (001) facets, evidenced a MD network at the Si/Ge interface (**Figure 12(a)**). Threading defects on the trench parallel  $\{111\}$  planes are stopped by the  $\text{SiO}_2$  sidewalls (**Figure 12(a)**), whereas some defects on the inclined  $\{111\}$  planes reach the layer surface (**Figure 12(d)**). A  $\{111\}$  V grooved trench bottom, which can be conveniently fabricated by anisotropic wet etching of the Si substrate, permits a further reduction of the defect density in the III-V layer, for several reasons: firstly, the  $\{111\}$  surface, especially when covered with an As monolayer, energetically facilitates the nucleation of III-V layers [25]. Secondly, single steps on  $\text{Si}\{111\}$  surfaces do not induce APB formation [44]. Thirdly, the incorporation and arrangement of MDs in the  $\{111\}$  heterointerface is alleviated, because dislocations can glide on the  $\{111\}$  planes. In the case of MOVPE GaAs deposited in such trenches propagating SFs and TDs are confined to the lower part of the trench, leaving the upper part defect-free with very few twins [25].



**Figure 12.** (a, d) Cross-section TEM images of InP/Ge/Si(001) heterostructures (Ge: buffer layer) in 150 nm wide in SiO<sub>2</sub> trenches with viewing direction (a) parallel and (d) perpendicular to the trenches, (b) schematic of the structure, dashed lines indicate threading defects, (c) orientation of lattice planes in (a–c). In (a) the vertical surfaces of the SiO<sub>2</sub> mask are invisible. In (d) the white arrow marks a twin lamella crossing the entire layer. (Reproduced from [36], with the permission of AIP Publishing.)

As shown by XRD pole figure analysis for the InP/Si(001) system the defects are distributed anisotropically on the {111} planes, i.e. more defects populate the  $(\bar{1}11)$  and  $(1\bar{1}1)$  planes parallel to the trench bottom faces (for trenches along [110]) than the inclined  $(11\bar{1})$  and  $(111)$  planes [37]. This finding agrees with TEM analyses, which prove the presence of a dense nanotwin network within 10 nm distance from the trench-parallel Si/InP{111} interfaces, effecting the lattice relaxation. On the other inclined {111} planes stacking faults and twins propagate, which extend from the Si/InP interface towards the layer top surface, where they could limit the performance of devices. Regarding the determination of defect densities of heteroepitaxial nanostructures the width of XRD rocking curves provides qualitative data useful for the comparison of samples having the same layer thickness, as the X-ray penetration depth is in the  $\mu\text{m}$  range. For the quantification of defect densities plan-view TEM of larger areas represents the most reliable technique, which yields a density of layer-crossing twin lamellae in the  $10^8$ – $10^9$  cm<sup>-2</sup> range for GaAs fins grown in {111} V grooved trenches on Si(001) [25].

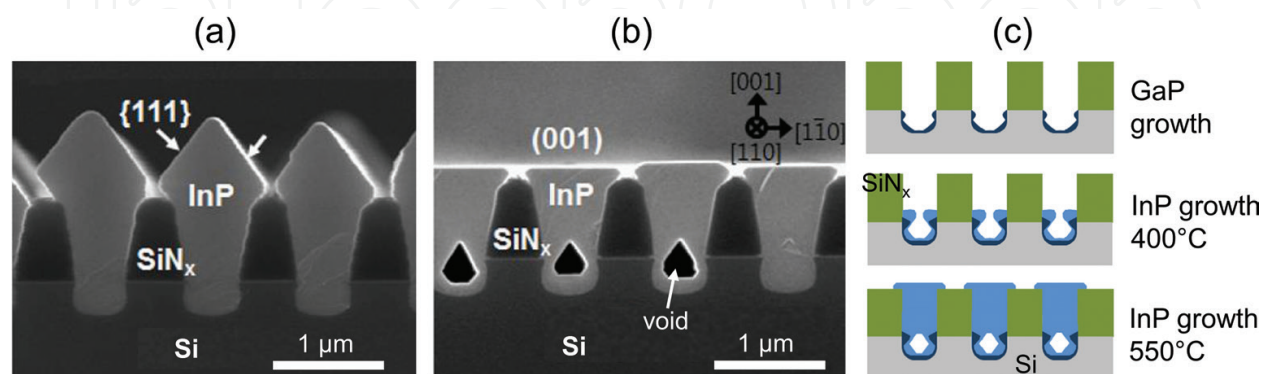
Furthermore, it has been found that the surface morphology of InP layers deposited selectively in trenches critically depends on the MOVPE growth conditions, especially on temperature and pressure [36, 38]. These parameters determine the precursor/adatom diffusivity and the heat transfer from the substrate to its surroundings, thus the growth rates of different facets. Before starting layer growth, a high temperature annealing step in the H<sub>2</sub> carrier gas is helpful to remove surface oxide layers and to promote the formation of double steps in the case of a Si(001) surface, which prevents the development of APBs [45]. Concerning the main growth step similar, but slightly different layer morphologies have been reported by different groups, depending on the structure of the patterned samples and the growth



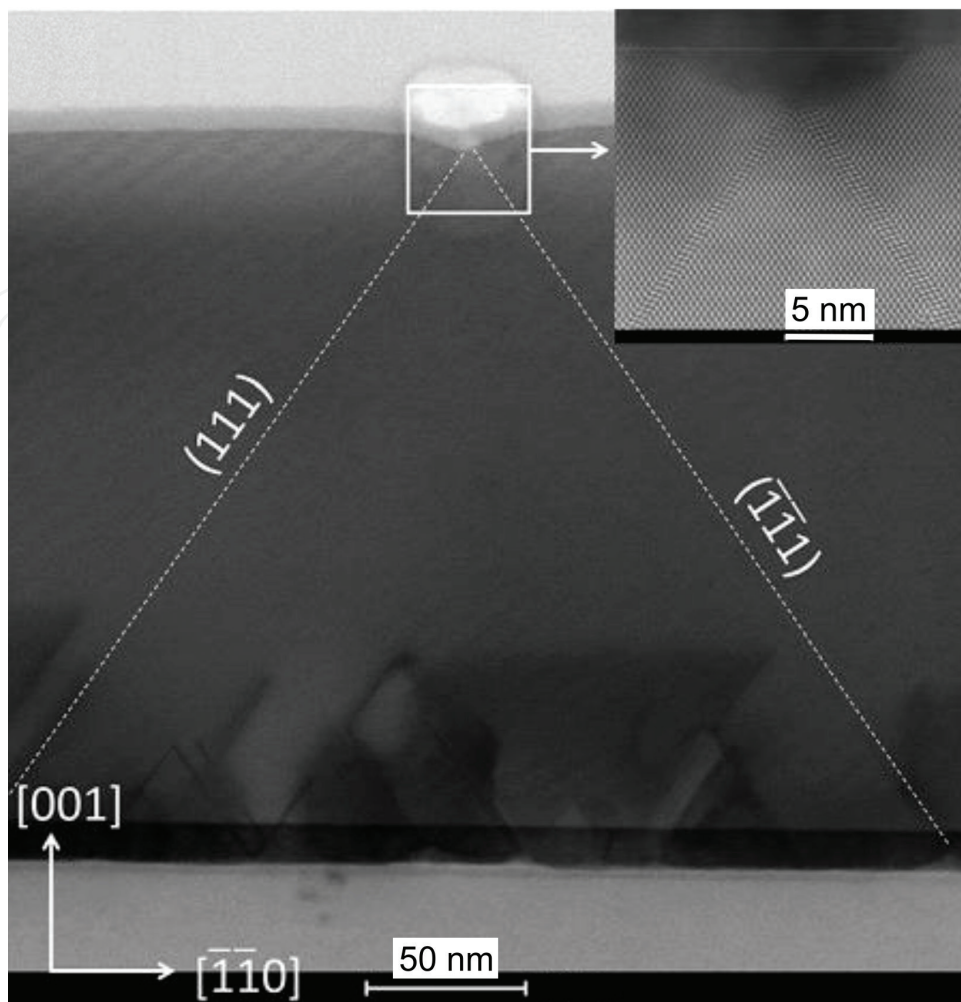
setup. By using phosphine as group-V precursor, a  $\text{SiN}_x$  trench mask with rounded rectangular recess in the  $\text{Si}(001)$  substrate and GaP and InP low-temperature buffer layers Lee et al. obtained wedge-shaped InP ridges bounded by  $\{111\}$  facets for a high growth temperature of  $650^\circ\text{C}$  (**Figure 13(a)**), whereas an atomically smooth InP(001) top surface resulted for  $550^\circ\text{C}$  (**Figure 13(b)**) [38]. In the latter case, GaP islands appeared on the Si sidewalls and in the course of continued InP deposition the lateral growth led to coalescence of opposing sidewall deposits before the recess was fully filled (**Figure 13(c)**). Consequently, a void together with a (001) growth surface was formed. Merckling et al. in contrast deployed a  $\text{SiO}_2$  trench mask with shallow curved recess in the  $\text{Si}(001)$  substrate, a Ge buffer layer with As termination for improved InP wetting, and used a two-stage InP deposition and tert-butylarsine and tert-butylphosphine as group-V precursors [36]. These authors reported highest uniformity of the ridge-shaped crystals bounded by  $\{111\}$  planes for a growth temperature of  $550^\circ\text{C}$ . At higher temperatures large three-dimensional islands protruding from the trenches were observed while at lower temperatures non-uniform faceting occurred due to a large density of defects.

Clear evidence for the correlation between crystal defects and surface morphology has been established Orzali et al. for GaAs grown by MOVPE on  $\text{SiO}_2$  trench-patterned  $\text{Si}(001)$  [25]. Analysis of high-resolution STEM images reveals that single twins intersecting the surface give rise to steps, whereas twins that intersect beneath the surface produce surface pits (**Figure 14**).

In order to keep the defect density low, two distinct types of buffer layers are frequently used in combination with the trenches. On the one hand, buffer layers of a different material with a lattice parameter between those of the substrate and of the layer deposited on the trench bottom reduce the effective misfit. For the InP/Si system (i) Ge with a Ge/InP misfit of  $\sim 4\%$  [33, 36] (**Figure 12**) and (ii) GaP avoiding the polarity mismatch at the InP/GaP interface [38] (**Figure 13**) have been used as buffer materials. On the other hand, buffer layers of the layer material grown at low temperature help to achieve a relatively smooth layer surface, since at low temperature the reduced Ga adatom diffusivity promotes the formation of a large density of small nucleation islands, which rapidly coalesce. Low temperature buffer layers contain a lot of defects leading to a relief of misfit strains and to an improved crystal quality in the following homoepitaxial layer grown at higher temperatures.



**Figure 13.** Cross-sectional SEM images of InP layer on  $\text{SiN}_x$  trench patterned  $\text{Si}(001)$  for a growth temperature of (a)  $650^\circ\text{C}$  and (b)  $550^\circ\text{C}$ . (c) Schematic growth evolution for (b). (Reprinted from [38], Copyright 2015, with permission from Elsevier.)



**Figure 14.** Bright-field STEM image of a GaAs layer in a SiO<sub>2</sub> trench on Si(001) depicting a shallow surface pit with twin lamellae intersecting underneath. The viewing direction is perpendicular to the trench direction. Inset: High magnification high-angle annular dark field STEM image of the pit. (Reproduced from [25], with the permission of AIP Publishing.)

After prolonged growth on trench mask patterned substrates the III–V layer grows above the mask and coalesces to form a continuous layer, where the coalescence often induces the development of further defects. In the case of GaAs MOVPE growth over a SiO<sub>2</sub> trench mask Li et al. observed {111} twins and stacking faults initiating at the SiO<sub>2</sub> top surface [46]. By using optimized MOVPE growth parameters for the coalescence stage, i.e. a slightly lower temperature and a higher V/III ratio as compared to the growth in the trenches the density of these defects was reduced. In this way, Li et al. obtained a high-quality GaAs layer on patterned Si(001), however with considerable large-scale thickness variations.

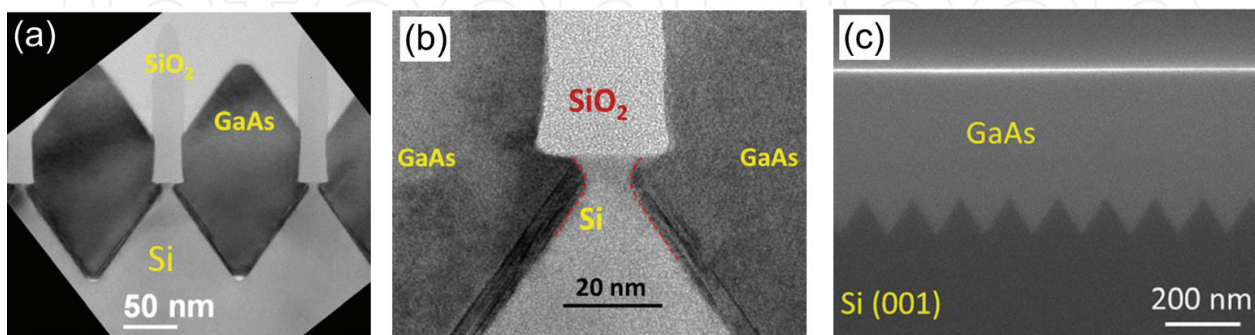
Very recently, it has been demonstrated that GaAs nanoridge arrays grown by the ART technique on exactly oriented Si(001) substrate can be used after removal of the SiO<sub>2</sub> mask as a GaAs-on-Si compliant substrate for a coalescence growth step in order to obtain APB-free, low-defect GaAs layers with flat (001) surfaces [47]. In the SiO<sub>2</sub> mask trenches V-grooved {111}

bottom faces were generated by KOH etching (**Figure 15**). The  $\text{SiO}_2$  walls were underetched, and beneath the  $\text{SiO}_2$  walls a curved Si surface formed, which undertakes the task of defect trapping instead of the  $\text{SiO}_2$  walls. Remarkably, during the coalescence growth step no defects originated from the top of the Si ridges in between neighbouring V grooves, as seen in TEM images (**Figure 15**). Furthermore, the TEM analysis shows that the misfit was accommodated by a large density of SFs within the first few nanometres from the Si/GaAs interface. This method has the advantages that no new defects appear in the coalesced layer in the course of oxide overgrowth and that the resulting layer surface has a low root-mean-square roughness of 1.9 nm measured in a  $5 \times 5 \mu\text{m}^2$  scan area for a layer thickness of only  $\sim 300$  nm.

### 2.1.3.2. Growth on surfaces patterned with a cylinder hole mask

In contrast to trench masks cylindrical mask openings allow to trap misfit defects running on all lattice planes that are inclined against the substrate normal. Despite this benefit, ART with cylinder hole masks has been investigated only by few research groups [48–50]. Hsu et al. [48] reported the MOVPE growth of smooth continuous 900 nm thick GaAs layers of low defect density on Si(001) substrate patterned with a round nanohole  $\text{SiO}_2$  mask having a hole diameter of 55 nm and aspect ratio of 4.7. Like in the case of ART trenches, threading misfit defects were confined to the lower part of the holes, giving monocrystalline, relaxed GaAs in the upper part and a very low etch pit density of  $3.3 \times 10^5 \text{ cm}^{-2}$  of the coalesced continuous GaAs layer. Application of a two-stage growth scheme (nucleation layer at low temperature, main growth at higher temperature) allowed to avoid thermal tensile strains in GaAs arising from the thermal expansion mismatch between Si and GaAs, as observed in GaAs layers on planar Si substrates by a redshift of the photoluminescence bandgap emission energy. However, the surface morphology of the coalesced GaAs layer and its defect structure above the  $\text{SiO}_2$  holes has not been addressed in the work of Hsu et al. [48].

Chang et al., who studied the selective MBE growth of GaAs on  $\text{SiO}_2$  nanohole patterned Si(001) found that the top surface of the GaAs nanostubs was not planar but bounded by inclined facets [50]. These authors stated that SFs starting near the Si/GaAs interface originated from disorders in the stacking sequence during merging of GaAs nuclei, owing to



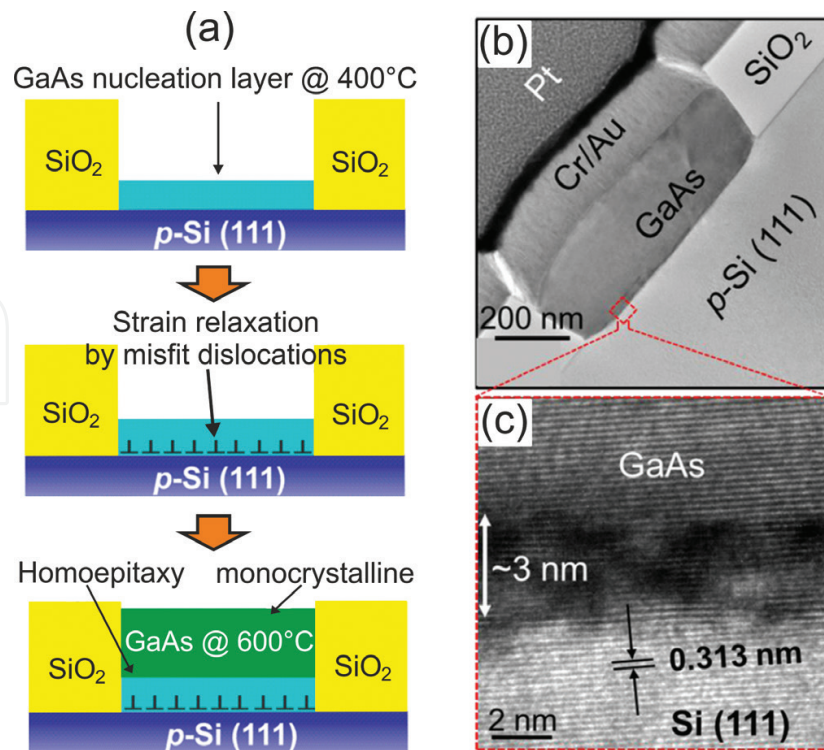
**Figure 15.** (a, b) Cross-section TEM images of GaAs nanoridges grown by the ART technique on Si(001). The zoomed-in TEM image (b) reveals SF trapping by the curved Si undercuts. (c) Cross-section SEM image of a coalesced GaAs layer obtained from the nanoridges shown in (a, b) by overgrowth after  $\text{SiO}_2$  mask removal. (Reproduced from [47], with the permission of AIP Publishing.)

different Si surface planes generated by the reactive ion etching of the holes. In contrast, SFs originating at the SiO<sub>2</sub> sidewalls formed due to local stresses in the GaAs induced by SiO<sub>2</sub> surface roughness.

Although Si(111) does not constitute the main substrate in complementary metal oxide semiconductor technology, a method for the growth of small GaAs layer volumes on Si(111) having structural and morphological characteristics highly attractive for applications has been developed: Chu et al. [49] deployed a two-stage MBE growth to obtain monocrystalline GaAs with atomically smooth surface and low defect density in the openings of a SiO<sub>2</sub> hole mask on Si(111). The growth mechanism and thus the properties of the resulting layer can be understood as follows (**Figure 16(a)**): During the first low-temperature growth stage numerous small GaAs islands form by homogeneous nucleation, which then coalesce. During the temperature ramping from the lower to the higher temperature used in the second growth stage the nucleation layer regrows epitaxially and, as a consequence of the thermal expansion coefficient mismatch between Si and GaAs, MDs are introduced at the GaAs/Si interface. As revealed by cross-section TEM analyses, these dislocations are confined to within ~3 nm from the GaAs/Si interface (**Figure 16(c)**). In the second stage growth proceeded in a layer-by-layer fashion, which yielded monocrystalline GaAs of high quality and low roughness (**Figure 16(b)**).

## 2.2. Defect filtering by multiple quantum dot layers

Another approach to enhance the quality of III–V semiconductor layers grown on mismatched substrates, exploits multiple layers of QDs, which act as a filter for threading defects [51]. QDs form by self-organized Stranski-Krastanov growth of a semiconductor material which shows (i) good wettability and (ii) considerable lattice misfit to the host crystal on which it is deposited. Typically, the QD layers are not grown directly on the substrate, but on a low-temperature buffer of the III–V layer material to be deposited (**Figure 17(a)**). In this way, the QD layers hinder the threading defects coming from the plastically relaxed buffer in extending to the subsequently grown III–V layer. Moreover, misfit strain in the vicinity of the QD layer originates only from the misfit between the QD and the III–V layer material, and not additionally from misfit between different lower and upper layer materials. The defect blocking effect has been explained by a deflection of the defect propagation induced by the strain fields of the QDs [52, 53]. In these strain fields dislocations experience shear Peach-Koehler forces, which lead to a sideward deflection so that the dislocation is redirected towards the material edges or subjected to annihilation before reaching the surface (**Figure 17(a)**). Calculations based on continuum elasticity predict increasing effectiveness of a single QD layer to bend TDs with increasing QD base area, but only a weak increase with QD height [52]. Besides the QD base area, the dislocation bending effectiveness is enhanced by using a larger number of QD layers. However, in the case of too large QDs or too large number of QD layers strain accumulates and gives rise to MD formation. Therefore, an optimum layer quality is expected for a QD size and number of QD layers just below the critical values for dislocation formation. For the Si/GaAs system, Yang et al. reported that a defect filter layer consisting of ten InAs QD layers with a QD width of 20–30 nm separated by 50 nm spacer layers on 2 μm GaAs buffer layer

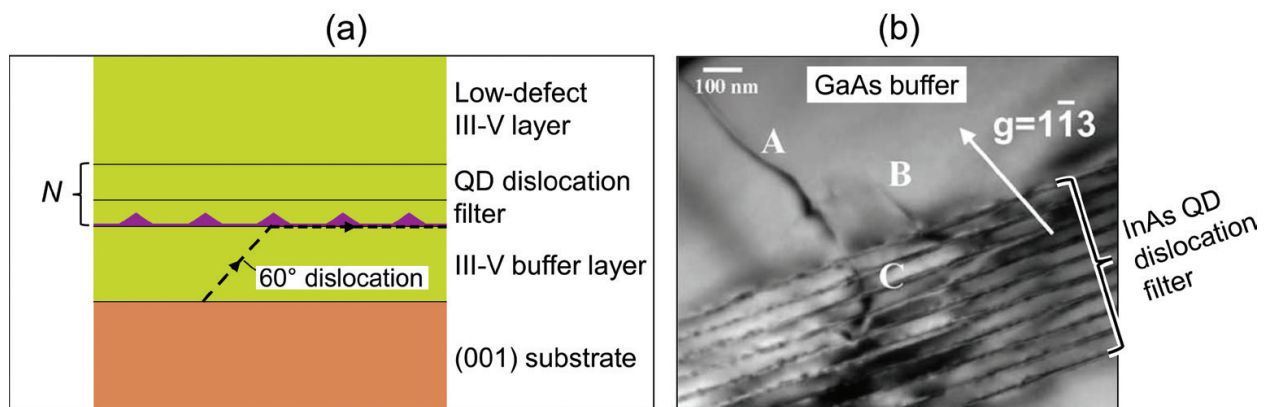


**Figure 16.** (a) Schematic of the two-stage MBE growth on  $\text{SiO}_2$  hole mask patterned Si(111), (b) cross-section TEM image of the Si/GaAs heterostructure fabricated by the procedure of (a), (c) HRTEM image from the marked area in (b). (Reprinted (adapted) with permission from [49]. Copyright 2014 American Chemical Society.)

was most effective [52]. Their TEM analysis demonstrated that  $60^\circ$  dislocations were bent to the side (i.e. the dislocation labelled 'B' in **Figure 17(b)**), and moreover, that pure edge dislocations were stopped at the interface between the GaAs spacer layer and the QD (the dislocation labelled 'C' in **Figure 17(b)**). The detailed mechanism of this blocking of edge dislocations is not well understood. Apart from dislocation filtering, QD layers also contribute to reduce the density of point defects in the layer, because the QD strain field imposes a driving force for point defects with compressive (dilatative) strain to migrate to elastically dilated (compressed) lattice regions. Further reduction of the defect density, measured as the etch pit density on the GaAs layer surface, was enabled by a combined application of QD dislocation filter layers and a buffer layer grown in three stages, starting with low temperature, followed by intermediate and eventually high-temperature growth [54]. However, the etch pit density of  $9 \times 10^5 \text{ cm}^{-2}$  resulting for a GaAs top layer thickness of  $1 \mu\text{m}$  [54] still exceeds the value achieved with ART growth of GaAs using a  $\text{SiO}_2$  cylinder hole mask [48] (Section 2.1.3.2).

### 2.3. Growth on mask-free nanopatterned surfaces

Although the growth on mask-free nanopatterned surfaces has been frequently used for site controlled fabrication of semiconductor QDs or nanoislands [55], it is also beneficial for improving the quality of continuous III–V layers [56–59]. Here, 'nanopatterned' means that the substrate surface exhibits ordered or random topographical features with



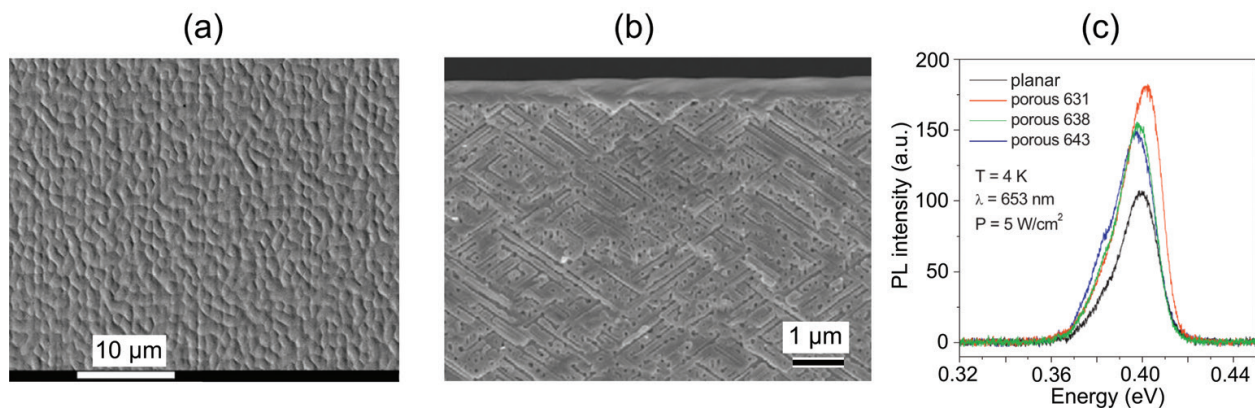
**Figure 17.** (a) Schematic cross-section of a heterostructure, in which multiple QD layers are deployed as dislocation filter, (b) cross-section TEM image using  $(1\bar{1}3)$  diffracting planes, showing the bending or blocking effect of a ten-fold InAs QD layer stack on threading dislocations (A, B, C) in GaAs grown on Si(001) substrate. ((b) (Copyright 2007 IEEE. Reprinted, with permission, from [52].)

dimensions well below  $1\ \mu\text{m}$ . In general, the insufficient blocking of threading defect propagation in the growth on mask-free nanopatterned surfaces leads to a lower increase of the layer quality as compared to the heteroepitaxy approaches based on: (i) selective growth on mask-patterned substrates (Section 2.1) and (ii) on growth using QD dislocation filter layers (Section 2.2). Nevertheless, growth on mask-free nanopatterned surfaces is interesting for reducing defect densities in III–V layers because of the simplicity and low cost of the processes needed for the substrate nanopatterning. Essentially, the active defect elimination mechanisms originating from the reduced growth area size and the geometry of the substrate surface rely on three-dimensional elastic lattice relaxation of the substrate and/or the layer as well as on defect trapping at steep or concave topographic features.

So far, morphologically different surfaces fabricated by different methods have been deployed in studies of the quality of III–V layers grown on mask-free nanopatterned surfaces. One possibility to create nanoroughened surfaces is *in-situ* annealing of Si(001) in  $\text{H}_2/\text{O}_2$  ambient in the MOVPE reactor, which effects the formation of volatile Si compounds such as SiO and thus a nanoscale roughening (pitting) of the Si surface. By using spectroscopic polarimetry Liu et al. [56] showed that polar GaP deposited by MOVPE on non-polar nanoroughened vicinal Si(001) (misfit  $\sim 0.4\%$ ) formed continuous layers, and attributed the continuous layer growth to a large number of nucleation sites owing to the higher reactivity between nanoroughened Si and the TMGa precursor, whose mobility was seen to decrease.

Nohavica et al. [57] performed liquid phase epitaxy growth of InAs on electrochemically etched micro- to nanoporous InP substrates (misfit  $\sim 3.2\%$ ). Due to the enhanced elastic relaxation of misfit strains an improved InAs layer morphology and a 20–35% reduction of the dislocation density of etched surfaces were obtained as compared to an InAs layer grown on a planar InP substrate. Similarly, the same group reported MOVPE growth and characterization of  $\text{In}_x\text{Ga}_{1-x}\text{As}$  layers ( $0.2 \leq x \leq 1$ ) on electrochemically etched nanoporous GaAs(001) substrates [58]. Such nanoporous GaAs surfaces showed low roughness areas

between the pore openings and are therefore suitable for nucleation of a layer on these small smooth areas. SEM images revealed a relatively smooth surface of a deposited  $0.4\ \mu\text{m}$  thick  $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$  layer (**Figure 18(b)**). However, the mosaic-shaped pattern visible in top-view SEM images indicated the presence of grains (**Figure 18(a)**). InAs layers grown on nanoporous GaAs exhibited enhanced low-temperature photoluminescence emission as compared to an InAs layer of same thickness grown on planar substrate (**Figure 18(c)**). As crystal defects boost non-radiative electronic transitions, the photoluminescence intensity represents an indicator of the crystal quality. The observed improved crystal quality can be assigned to elastic relaxation of misfit strains both in the layer and in the substrate during lateral pore overgrowth leading to a reduction of the defect density. Due to the high porosity of the GaAs substrate of  $\sim 50\%$  compliancy of the substrate lattice is expected.



**Figure 18.** Plan view (a) and cross-section (b) SEM images of a  $0.4\ \mu\text{m}$  thick  $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$  layer on nanoporous GaAs(001) substrate (misfit  $\sim 1.4\%$ ), (c) photoluminescence spectra of  $1.2\ \mu\text{m}$  thick InAs layers grown on planar and on porous GaAs(001) substrates with different pore layer thicknesses (610–631, 635–638, 641–643  $\mu\text{m}$ ). (Reprinted from [58], Copyright 2013, with permission from Elsevier.)

### 3. Relevance of nanoheteroepitaxial layers for advanced optoelectronic applications

It has been recognized long ago that excellent crystalline quality is essential for a high performance of semiconductor power and optoelectronic devices. In particular, minority carrier devices such as insulated-gate bipolar transistors, as well as light-emitting and absorbing devices require dislocation densities below  $10^5\ \text{cm}^{-2}$  [24, 60], which has not been achieved by traditional methods of defect reduction in planar III–V heteroepitaxy on the common Si platform. However, in the last 10 years, substantial progress has been made in the heteroepitaxial growth of low-defect, mismatched semiconductors by using nanopatterned substrates, which allowed to accomplish a good crystalline quality of III–V layers close to that needed for long-lifetime devices. Recently, these nanoheteroepitaxy methods have been exploited for the

realization of several III–V devices integrated on a Si platform. Examples include laser diodes [59, 61], GaAs solar cells [49], and GaAs/ $\text{In}_x\text{Ga}_{1-x}\text{As}$  tunnel diodes for digital circuits applied e.g. in inverters or random-access memory cells [62, 63]. Further applications have been proposed such as In-rich  $\text{In}_x\text{Ga}_{1-x}\text{As}$  channels for n-type metal oxide semiconductor field effect transistors with enhanced electrical characteristics [64] or GaAs waveguides for lasers [42]. Exemplarily, we will briefly describe the fabrication and performance of two such unique devices, one using oxide-separated, disc-shaped III–V volumes as the active region of a solar cell, and one exploiting the V-groove defect reduction technique as the basis for a QD microdisc laser structure.

### 3.1. GaAs nanodisc *p-i-n* solar cell on Si(111) nanopatterned with a $\text{SiO}_2$ hole mask

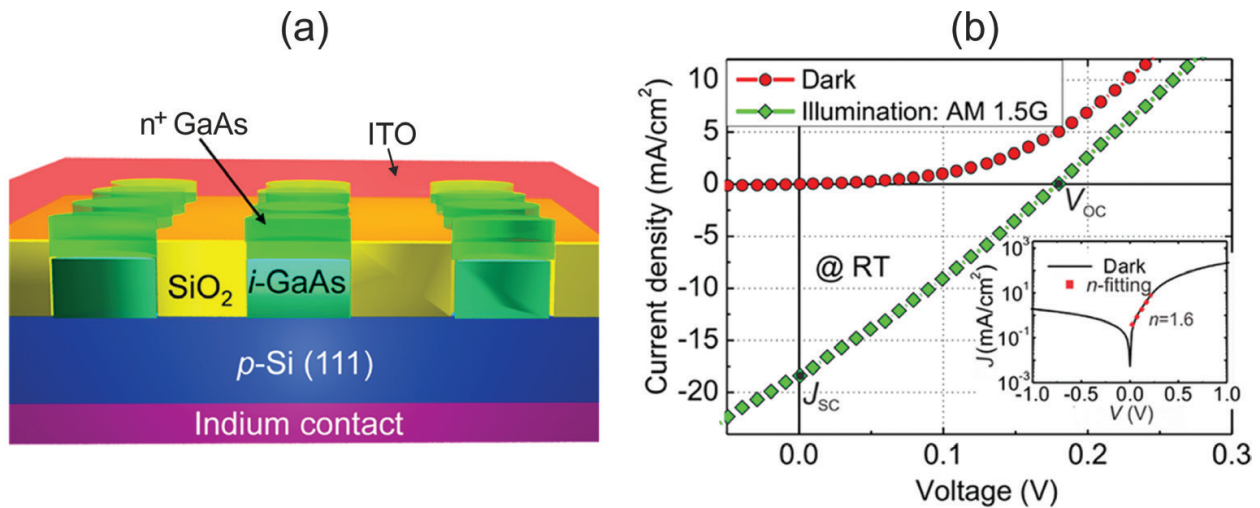
A prototype GaAs nanodisc *p-i-n* solar cell was fabricated on p-doped Si(111) substrate by using two-stage MBE growth for selective deposition of an intrinsic GaAs buffer layer (nucleation layer: 25 nm, main layer: 150 nm) in the circular openings of a  $\text{SiO}_2$  hole mask, as described in Section 2.1.3.2 [50]. On the (111) surface of the buffer layer 50 nm of strongly n-doped (n+) GaAs was grown. To complete the device, indium tin oxide (ITO) and indium contacts were deposited on the top GaAs and bottom Si, respectively (**Figure 19(a)**). In the dark, the current density-voltage characteristic of the solar cell showed a good rectification behaviour with a current ratio  $> 10^2$  for  $\pm 1$  V bias (**Figure 19(b)**). Under illumination of one sun AM 1.5G a short circuit current of 18.4 mA/cm<sup>2</sup>, an open circuit voltage of 0.18 V, an ideality factor  $n = 1.6$  and a fill factor of 28% were obtained. The resulting energy conversion efficiency of 0.9% is similar to the values reported for nanostructured solar cells, but much lower than those for conventional Si solar cells. The poor conversion efficiency and fill factor can be explained by surface states at the GaAs/ $\text{SiO}_2$  interface and carrier-trapping dislocations at the Si/GaAs interface. It is expected that these characteristic values can be enhanced by suitable  $\text{SiO}_2$  surface passivation and improved contacts.

### 3.2. QD microdisc laser using nanoheteroepitaxial buffer on Si(001)

GaAs buffer layers on V-grooved exact-oriented Si(001) templates have been used to fabricate  $\text{InAs}/\text{In}_x\text{Ga}_{1-x}\text{As}$  dot-in-a-well microdisc laser structures emitting at  $\sim 1.2$   $\mu\text{m}$  wavelength with almost similar characteristics as devices fabricated on native GaAs substrate [59]. For the growth of the low-defect GaAs buffer layer a two-step deposition was used starting with selective growth in  $\text{SiO}_2$  trenches followed by  $\text{SiO}_2$  removal and the mask-free GaAs coalescence growth step by MOVPE, as described in Section 2.1.3.1. The active region comprised five InAs QD layers embedded in  $\text{In}_x\text{Ga}_{1-x}\text{As}$  quantum wells separated by GaAs spacer layers, respectively, grown by MBE (**Figure 20(b)**). **Figure 20(a)** depicts a cross-section TEM image of the as-deposited layer structure. In order to obtain the micro-discs (**Figure 20(c)**) colloidal lithography and reactive ion etching were deployed.

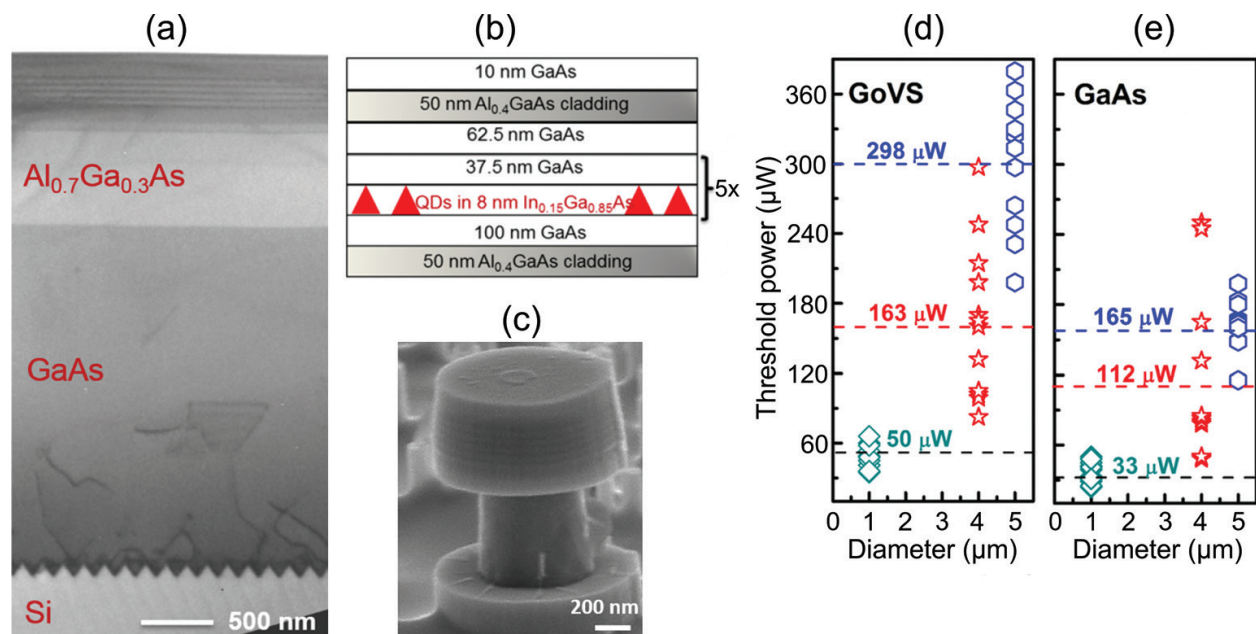
Optical emission spectra were measured with a micro-photoluminescence setup in surface-normal pump/collection configuration under continuous wave excitation at 10 K. A low average threshold power of 50  $\mu\text{W}$  has been achieved for 1  $\mu\text{m}$  disc diameter, as compared to 33  $\mu\text{W}$  for





**Figure 19.** (a) Schematic cross-section of the p-i-n solar cell grown on Si(111), (b) current density-voltage characteristics of the device in the dark and under illumination of one sun AM 1.5G. The inset shows a semilogarithmic current density-voltage curve for the non-illuminated state. (Reprinted (adapted) with permission from [49]. Copyright 2014 American Chemical Society.)

lasers on GaAs substrate (**Figure 20(d, e)**). With increasing disc diameter the threshold power rose due to smaller mode separation, occurrence of multimode lasing and absorption in the microdisc centre. The larger lasing thresholds on the Si substrate can be explained by the presence of crystal defects (i) inside the active region, reducing the modal gain and (ii) outside the active region promoting carrier recombination, thus lowering the injection efficiency of the carriers.



**Figure 20.** (a) Cross-section TEM image of the as deposited laser structure on V-grooved Si(001), (b) Schematic cross-section of layers in the disc region, (c) oblique-view SEM image of the microdisc, (d, e) threshold power for different disc diameters on GaAs-on-V-groove-Si (GoVS) template (d) and on GaAs substrate (e). The dashed lines denote the average thresholds. (Reproduced from [59], with the permission of AIP Publishing.)

## 4. Summary

In summary, heteroepitaxial approaches deploying nanopatterned substrates for the growth of mismatched III–V zinc blende semiconductor layers of low defect density are reviewed. As an important growth mode occurring in some of these approaches, nanoscale selective growth is explained with focus on its scaling with adatom surface migration and desorption. Efficient trapping and elimination of misfit-related defects has been demonstrated by ART techniques using nanopatterned oxide or nitride masks as well as by utilization of multiple QD defect filter layers. The active mechanisms of defect elimination in these growth methods are described. Besides, heteroepitaxial growth on mask-free nanoporous substrates also reduces the defect density, albeit in a less pronounced fashion. Finally, selected applications of low-defect III–V layers integrated on the common Si platform are presented. Remarkably, laser structures on the Si substrate have been realized exhibiting characteristics not far from those of structures grown on native GaAs substrates.

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