Chapter 1

Carrier Mobility in Field-Effect Transistors

Philippe Gaubert and Akinobu Teramoto

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/67885

Abstract

Authors investigate the carrier mobility in field-effect transistors mainly when fabricated on Si(110) wafers. They showed that the methods developed to extract the conduction parameters cannot be implemented for Si(110) p-MOSFETs. Authors then developed a more accurate mobility model able to simulate not only the drivability but also the transconductance for these same devices. The study of the relation between the mobility, channel direction and wafer orientation revealed that the channel direction had a significant impact on the mobility for transistors fabricated on Si(110) wafers, the highest electron and hole mobilites being obtained for a channel along the <100> and <110> directions, respectively. No relations were found for Si(100) wafers. The study of the dependence of the scattering mechanism limiting the mobility in Si(110) n-MOSFETs showed that the Coulomb and surface roughness scattering mechanisms were responsible for the degradation of the mobility when compared to the one on Si(100) wafers. Finally, the measurement of the mobility in an accumulation-mode MOSFETs is not straightforward since a bulk contribution, owing to the SOI layer, is adding to channel current. A methodology has been successfully implemented that led to the experimental verification of the universal behaviour of the mobility in an accumulation layer.

Keywords: mobility, electron, hole, silicon, temperature, crystallographic orientation, channel direction, scattering mechanism, modeling, accumulation, extraction, (100), (110)

1. Introduction

The concept of employing an electric field to modulate the conductivity of a channel has been proposed first by Lilienfeld during the 1930s [1], long before its practical fabrication by Shockley et al. in 1947 [2]. Since, the field-effect transistor has taken several directions and is at the root of various devices such as the metal-oxide-semiconductor FET (MOSFET) [3], dual gate MOSFET [4], junction FET [5], high electron mobility transistor [6], four-gate transistor [7] and so on. Nevertheless, the most important parameter for all these devices is the mobility of

the carrier flowing inside the channel. Their mobility, also known as their ability to move through the crystal, will define the electrical performances of the device. The mobility is consequently a paramount parameter, and its good knowledge is of prime importance to first understand the physics underlying the conduction mechanisms inside semiconductor devices and second to be able to model and simulate a single transistor and in turn more complex circuits. The mobility in field-effect transistors hinges on various physical and environmental parameters that we propose to investigate for MOSFETs fabricated on (100) and (110) silicon-oriented wafers.

In Section 2, the method to measure the mobility is briefly reviewed for different structures, while Section 3 investigates several methods to extract the conduction parameters such as the low field mobility in Si(100) and Si(110) p-MOSFETs. Thus, its modeling is presented in Section 4 for the same devices. Results regarding the impact of the channel direction and wafer orientation on the mobility are investigated in Section 5 while the impact of the temperature is reported in Section 6 for Si(110) n-MOSFETs. Recently, devices based on the majority carriers rather than the minority ones to generate the current showed promising results. A methodology to extract their mobility is presented in Section 7 and is applied to accumulation-mode Si (100) p-MOSFETs. Finally, Section 8 concludes the chapter.

2. Experimental measurement of the mobility

The knowledge of the experimental mobility of carriers that are flowing inside the channel of a FET is essential for the development of semiconductor devices and in turn electronic circuits. The direct measurement of the effective mobility μ_{eff} is not possible, but its calculation is enabled through the measurement of the drain current I_d—gate voltage V_g characteristic and of the gate-channel capacitance C as a function of the gate voltage. Both characteristics can be measured at V_d = 100 mV on a large gate transistor with at least a gate length L and gate width W above 50 μm in order to allow an accurate measurement of the capacitance. The substrate, source and drain electrodes are grounded, and the measurement of the capacitance is carried out on the gate electrode side at relatively low frequencies f between 1 and 100 kHz to neglect the serie resistances. Thus, the inversion charge Q_{inv} per unit area is calculated from the C – V_g characteristic

$$Q_{inv}(V_g) = \int_{-\infty}^{V_g} C(Vg)dV_g. \quad (1)$$

The effective mobility μ_{eff} is finally calculated from

$$\mu_{eff}(V_g) = \frac{L}{W}\frac{I_d(V_g)}{V_d Q_{inv}(V_g)}. \quad (2)$$

At this stage, the effective mobility can be plotted as a function of the carrier sheet density by dividing the inversion charge Q_{inv} by the elementary charge q. It can also be plotted as a function of the transverse effective electric field E_{eff} that is calculated as follows:

$$E_{eff}(V_g) = \frac{1}{\varepsilon_{Si}\varepsilon_0}[Q_{dep} + \eta Q_{inv}(V_g)], \tag{3}$$

where Q_{dep} is the depletion charge per unit area, ε_{Si} is the dielectric constant of the silicon, ε_0 is the permittivity of the vacuum, and η is a term referring to the averaging of the transverse electric field over the carrier distribution inside the conduction channel. In Eq. (3), the depletion charge Q_{dep} is theoretically calculated from the doping concentration N_{sub} of the channel. It is expressed as follows:

$$Q_{dep} = \sqrt{\frac{4\varepsilon_{Si}\varepsilon_0\phi_B N_{sub}}{q}}, \tag{4}$$

with

$$\phi_B = \frac{k_B T}{q}\ln\left(\frac{N_{sub}}{n_i}\right), \tag{5}$$

being the bulk Fermi energy. In Eq. (5), k_B is the Boltzmann constant, T is the temperature in Kelvin, and n_i is the intrinsic carrier concentration. Takagi et al. [8] confirmed experimentally that in Eq. (3), η is equal to 1/3 for hole and to 1/2 for electron on Si(100) wafers [9]. Regarding Si (110) wafers, η is generally taken equal to 1/3 for both hole [3, 10] and electron [11].

Contrary to bulk transistors for which the methodology has been described previously, the substrate of transistors fabricated on silicon-on-insulator (SOI) wafers sometimes cannot be accessed and then cannot be grounded. The back-gate cannot be biased and can be floating as long as the applied gate voltage is large enough to neglect the impact of the back-gate [12]. The expression of the depletion charge Q_{dep} given by Eq. (4) must be rearranged in Eq. (3) since the buried oxide is preventing the expansion of the depletion. If the depletion is expending deeper than the buried oxide, Q_{dep} is given by $qN_{sub}t_{SOI}$ where t_{SOI} is the thickness of the SOI layer.

In the case of devices involving the majority carriers rather than the minority ones such as accumulation-mode transistors that will be studied in Section 7, the entire SOI layer is neutral when the accumulation layer is formed. The depletion charge Q_{dep} in Eq. (3) must be removed, and the calculation is involving the sole accumulation charge Q_{acc} [13, 14]. Eqs. (3) and (4) are rewritten as follows:

$$\mu_{eff}(V_g) = \frac{L}{W}\frac{I_d(V_g)}{V_d Q_{acc}(V_g)} \tag{6}$$

and

$$E_{eff}(V_g) = \frac{\eta Q_{acc}(V_g)}{\varepsilon_{Si}\varepsilon_0}. \tag{7}$$

3. Mobility extraction methods

The knowledge of the conduction parameters is useful to model the drivability of a MOSFET and in turn simulate complex circuits. All extraction methods rely on the knowledge of the $I_d - V_g$ drain current-gate voltage characteristic measured for various gate lengths L and gate widths W.

The calculation procedures are based on the expression of the drain current in the linear region for a gate overdrive voltage $V_g - V_{th}$ (V_{th} being the threshold voltage) greater than the drain voltage V_d ($V_g - V_{th} >> V_d$). In this range, the drain current I_d is expressed as follows:

$$I_d = \mu_{eff} C_{ox} \frac{W - \Delta W}{L - \Delta L} (V_g - V_{th})(V_d - I_d R_{acc}). \quad (8)$$

where R_{acc} is the parasitic access resistances located at the source and drain contacts and C_{ox} is the oxide capacitance. ΔW and ΔL are, respectively, the width and length gate channel reduction. In Eq. (8), the effective mobility μ_{eff} is generally replaced by the well known [15]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_g - V_{th})}, \quad (9)$$

where μ_0 is the low field mobility and θ is the mobility attenuation factor.

Depending on the extraction method, it is possible to obtain the low field mobility μ_0, the mobility attenuation factor θ, the parasitic access resistance R_{acc} in series with the intrinsic resistance of the channel of the transistor, the channel width reduction ΔW and the channel length reduction ΔL.

3.1. Silicon wafers with a (100) crystallographic orientation

Four different extraction methods have been used to extract the conduction parameters in p-MOSFETs fabricated on (100) silicon-oriented wafers. These methods are the Schreutelkamp method [16, 17], the interpolation method explained in Tsividis book [18], the Ghibaudo method [19] and finally the Ciofi method [20].

The Schreutelkamp method is based on Eqs. (8) and (9) and requires the calculation of intermediate parameters around a given gate overdrive voltage $V_g - V_{th}$ that has been measured on several transistors featuring various gate length L for a given gate width W. A representation of this method is shown in **Figure 1** for $V_g - V_{th} = 1$ V. I_d^{-1} is plotted as a function of the gate length L, and the intersection with the vertical and horizontal axis is collected as shown in the inset of **Figure 1**. The low field mobility μ_0 is extracted from the slope of the linear plot $(1/I_d)_{int}/L_{int}$ versus $(V_g - V_{th})^{-1}$, while the mobility attenuation factor θ is obtained from the intersection with the vertical axis. On the other hand, the intersection of the plot L_{int} versus $L_{int}/(1/I_d)_{int}$ with the vertical axis gives the channel length reduction ΔL, and the intersection with the horizontal axis gives the parasitic access resistance R_{acc}. The extracted data according to the Schreutelkamp method on Si(100) p-MOSFETs are reported in **Table 1**. Note that the Schreutelkamp method does not allow the obtaining of the gate width reduction ΔW. The

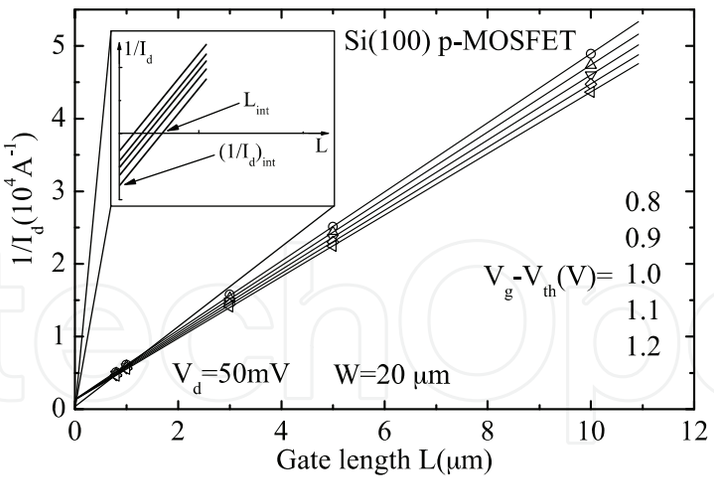

Figure 1. Example of the procedure to obtain L_{int} and $(1/I_d)_{int}$ for the centered V_g–V_{th} = 1 V in the frame of the Schreutlkamp method.

	Schreutelkamp	Interpolation	Ciofi	Ghibaudo
μ_0 (cm^2/Vs)	115	/	114	118
θ (V^{-1})	0.31	/	0.348	0.359
Racc (Ω)	98	106	68.9	67.41
ΔL (μm)	−0.1	−0.128	−0.121	−0.13
ΔW (μm)	/	−0.352	−0.322	−0.331

Table 1. Conduction parameters extracted using several methods for Si(100) p-MOSFETs at V_d = 50 mV [21].

impact of the centered gate overdrive voltage $V_g - V_{th}$ on the conduction parameters has been conducted. The results on the low field mobility μ_0 and channel length reduction ΔL are shown in **Figure 2**. Both values are strongly decreasing when the gate overdrive voltage is increased until $V_g - V_{th}$ = 0.8 V and are reaching a more stable behavior afterwards. For $V_g - V_{th}$ < 0.8 V, the transistor is not working in the linear regime, and Eq. (8) is inaccurate, thus the fast drop. Additionally, the mobility model does not fit accurately the effective mobility, making the calculation even more inaccurate. For $V_g - V_{th}$ > 0.8 V, the low field mobility μ_0 is slightly increasing, while the channel length reduction ΔL is slightly decreasing. The reason is that even if Eq. (8) can be applied, Eq. (9) does not perfectly model the effective mobility. For each centered $V_g - V_{th}$, the parameters that are modeling the mobility are slightly changing in order to accurately fit the effective mobility according to the centered $V_g - V_{th}$. In turns, the channel length reduction ΔL and the low field mobility μ_0 are not constant. An equivalent behavior has been also acknowledged when the mobility attenuation factor θ and the parasitic access resistance R_{acc} have been plotted as a function of the centered gate overdrive voltage $V_g - V_{th}$.

Like the previous method, the one developed by Ghibaudo is also based on the same equations; however, the calculation requires the derivative of the $I_d - V_g$ curves for different gate

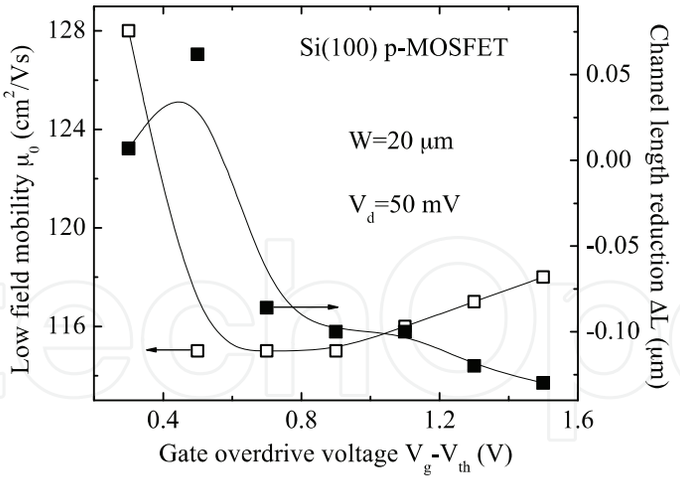

Figure 2. Evolution of the extracted low field mobility μ_0 and channel length reduction ΔL as a function of the centered gate overdrive voltage V_g–V_{th} in the frame of the Schreutlkamp method.

length L and gate width W, that is the transconductance g_m. Data measured around the threshold voltage are used. The plots $I_d/g_m^{0.5}$ and $g_m^{-0.5}$ as a function of $V_g - V_{th}$ allow the extraction of the intermediate parameters G_m and θ^*, respectively, since $I_d/g_m^{0.5} = (G_m V_d)^{0.5}(V_g - V_{th})$ and $g_m^{-0.5}=(G_m V_d)^{-0.5}[1 + \theta^*(V_g - V_{th})]$. Note that, the linear fittings are realized in the range $V_g>V_{th}$. The slope of the former fitting gives G_m, while the latter one allows the extraction of θ^*. Thus, the intersection of the plot G_m versus W with the horizontal axis gives the gate width reduction ΔW, and the intersection of the plot G_m^{-1} versus L gives the gate length reduction ΔL. Finally, the mobility attenuation factor θ and the parasitic access resistances R_{acc} are obtained from the plot θ^* versus G_m since $\theta^*=\theta + G_m R_{acc}$. θ^* is the extrinsic mobility attenuation factor. The extracted parameters for Si(100) p-MOSFETs using the Ghibaudo method are reported in **Table 1**.

While the Ghibaudo method is making use of the derivative, the extraction method developed by Ciofi is based on the numerical analysis of the discretization of the $I_d - V_g$ characteristics and requires here as well the calculation of two intermediate parameters, K and H. They are extracted from the plot V_d/I_d versus $V_g - V_{th}$ for several gate lengths L and gate widths W since $V_d/I_d=K^{-1}((V_g - V_{th})^{-1} + H)$. H and K are related together by $H=\theta + KR_{acc}$, and the plot H versus K allows the obtaining of the mobility attenuation factor θ and the parasitic access resistances R_{acc}. Plotting K^{-1} versus L and K versus W, respectively, gives the gate length reduction ΔL and the gate width reduction ΔW at the intersection with the horizontal axis. Data measured at relatively high gate overdrive voltage for Si(100) p-MOSFETs have been used, and the results of the Ciofi method are reported in **Table 1**. θ^* versus G_m for the Ghibaudo method and H versus K for the Ciofi method have been plotted on the same **Figure 3**. The results in **Figure 3** are almost identical for both methods, so are the units. In fact, K and G_m are the transconductance parameter and equals to $\mu_0 C_{ox} W/L$. Moreover, the similarity between both methods is obvious since $\theta + KR_{acc}=H=\theta^*=\theta + G_m R_{acc}$. Note that, for both the Ghibaudo and the Ciofi methods, the knowledge of the threshold voltage V_{th} prior their implementation is not mandatory since the threshold voltage V_{th} can be extracted during the procedures described above.

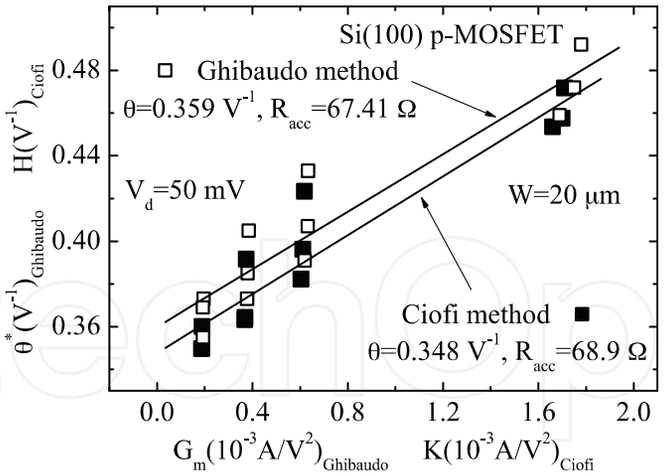

Figure 3. Fitting of $\theta^* = f_g(G_m)$ for the Ghibaudo method and $H = f_c(K)$ for the Ciofi method to obtain the access the parasitic access resistance R_{acc} and the mobility attenuation factor θ [21].

Even if the method is quite limited since the low field mobility μ_0 and the mobility attenuation factor θ cannot be evaluated, the interpolation method proposed in the book by Tsividis has been still implemented for Si(100) p-MOSFETs and the results are reported in **Table 1**.

The four methods have been successfully employed to extract the conduction parameters although a disagreement is visible in regards to the parasitic access resistances R_{acc}. The similarity between the Ciofi method and the Ghibaudo method leads to very similar data and in turn an undervaluation of the parasitic access resistances R_{acc} when compared with the values obtained using the two other methods.

3.2. Silicon wafers with a (110) crystallographic orientation

The extraction methods previously described have been implemented for p-MOSFETs fabricated on (110) silicon-oriented wafers in order to extract the conduction parameters. The results are reported in **Table 2**, and the extraction methods are consistent. Compared to Si (100) p-MOSFETs, the low field mobility μ_0 for Si(110) p-MOSFETs is almost three times higher, confirming the superiority of the hole mobility on (110) silicon surface [22].

At the same time, the mobility attenuation factor θ is 10 times weaker for Si(110) p-MOSFETs, indicating that the degradation of the effective mobility might be much more pronounced for Si

	Schreutelkamp	Interpolation	Ciofi	Ghibaudo
μ_0 (cm^2/Vs)	303	/	285	281
θ (V^{-1})	0.042	/	0.038	X
R_{acc} (Ω)	48	57.76	63	X
ΔL (μm)	−0.67	−0.44	−0.43	−0.38
ΔW (μm)	/	−0.39	−0.42	−0.39

Table 2. Conduction parameters extracted using several methods for Si(110) p-MOSFETs at V_d = 100 mV [21].

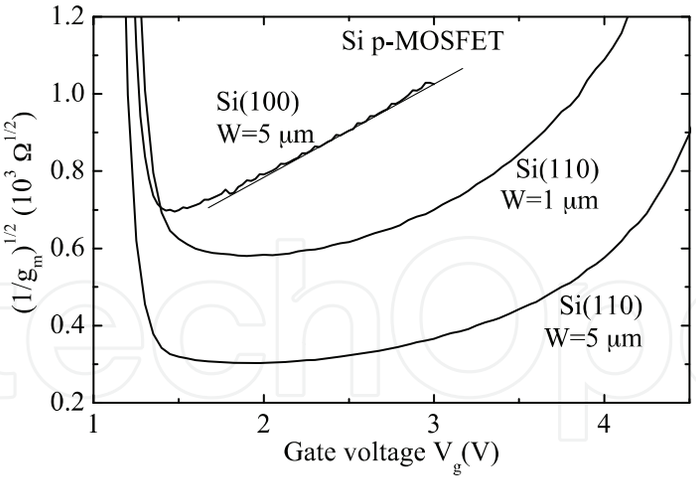

Figure 4. Plot of $g_m^{-0.5}$ as a function of the gate overdrive voltage V_g–V_{th} for transistors fabricated on Si(100) and Si(110) wafers. The linear fitting of the curve allows the extraction of the intermediate parameter G_m in the frame of the Ghibaudo method. L = 10 μm, V_d = 50 mV for Si(100) and V_d = 100 mV for Si(110) transistors.

(100) p-MOSFETs. However, the main result is the impossibility to extract the parasitic access resistances R_{acc} and the mobility attenuation factor θ with the Ghibaudo method, whereas the method has been successfully employed for Si(100) p-MOSFETs [23]. Indeed, as shown in **Figure 4**, whereas the extraction of G_m from $I_d/g_m^{0.5}$ has been possible, and in turn the extraction of the low field mobility μ_0, the gate length reduction ΔL and the gate width reduction ΔW, the linear fitting of $g_m^{-0.5}$ versus the gate voltage could not be done. Concerning the Schreutelkamp method, the same procedure as previously described has been carried out and a behavior similar to the one noticed for Si(100) p-MOSFETs has been acknowledged.

4. Modeling of the mobility

4.1. Silicon wafers with a (100) crystallographic orientation

The modeling of the hole mobility using Eq. (9) with the data reported in **Table 1** (μ_0 = 115 cm^2/Vs and θ = 0.35 V^{-1}) has been carried out and compared with the experimental data of the effective mobility for Si(100) p-MOSFETs. The result is reported with the dashed line in **Figure 5** and demonstrates the great accuracy of the extraction method and of the model provided by Eq. (9) when the effective electric field E_{eff} is above 0.3 MV/cm. Below this value, the model is inaccurate since the effective mobility is limited by the Coulomb scatterings, scatterings that are not taken into account in Eq. (9). The conduction parameters (μ_0 = 115 cm^2/Vs, θ = 0.35 V^{-1}, R_{acc} = 70 Ω, ΔL = −0.33 μm, ΔW = −0.13 μm, V_d = 50 mV and W = 20 μm) have been implemented in Eqs. (8) and (9) to model the drain current I_d in p-MOSFETs with different gate length L and the transconductance g_m has been calculated afterwards. The results are shown in **Figure 6** with the thick full lines. At the exception of V_g<V_{th}, the modeling is greatly fitting the experimental data for either I_d or g_m. The maximum of the transconductance g_m cannot be estimated because Eq. (9) does not model the Coulomb scatterings

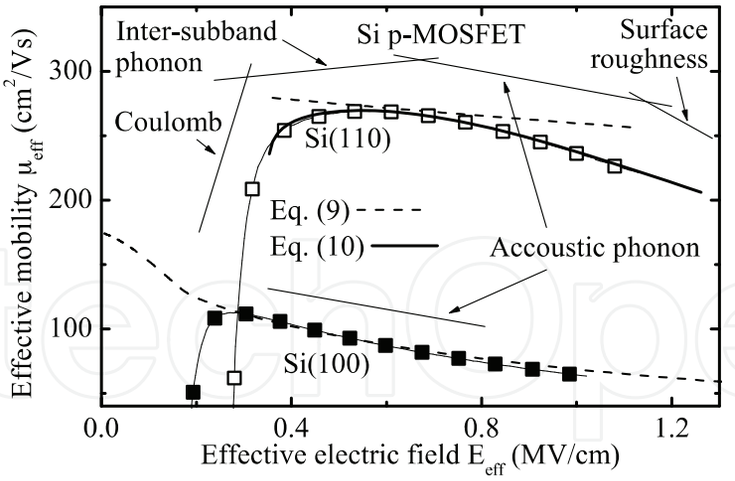

Figure 5. Effective mobility μ_{eff} as a function of the effective electric field E_{eff} for Si(100) and Si(110) p-MOSFETs. The dashed lines report the modeling carried out with Eq. (9), $\mu_0 = 115$ cm^2/Vs and $\theta = 0.35$ V^{-1} for the Si(100) wafers and $\mu_0 = 285$ cm^2/Vs, $\theta = 0.038$ V^{-1} for the Si(110) ones. The full line reports the modeling with Eq. (10) and $\mu_0 = 280$ cm^2/Vs, $\theta_1 = 0$ V^{-1}, $\theta_2 = 0.05$ V^{-2}, and $\alpha = 0.04$ for Si(110) wafers.

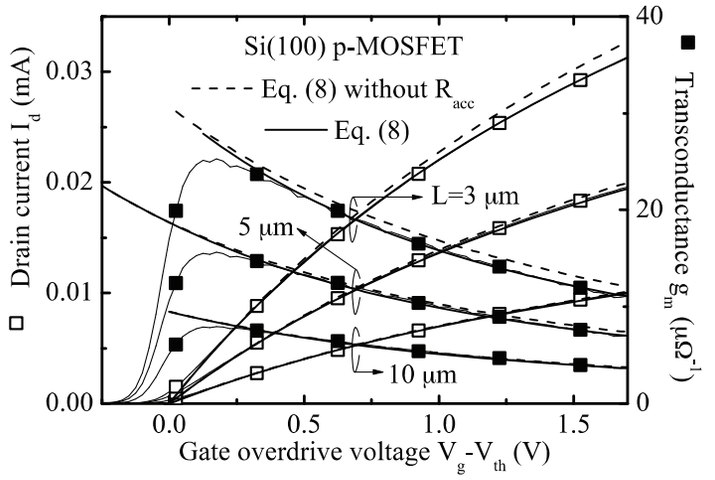

Figure 6. Drain current I_d (left) and transconductance g_m (right) as a function of the gate overdrive voltage V_g–V_{th} for Si (100) p-MOSFETs featuring different gate length. The lines are the modeling carried out with $\mu_0 = 115$ cm^2/Vs, $\theta = 0.35$ V^{-1}, Eqs. (9) and (8) with (full thick lines) and without (dashed lines) taking into account the parasitic access resistances $R_{acc} = 70$ Ω. $\Delta L = -0.33$ μm, $\Delta W = -0.13$ μm, $V_d = 50$ mV, $W = 20$ μm.

mechanisms. A second simulation has been calculated without taking into account the parasitic access resistances R_{acc} in Eq. (8), and the results are shown with the dashed line in **Figure 6**. The fact to neglect the parasitic access resistances R_{acc} leads to a discrepancy between the model and the experimental data that is enhanced when the size of the device is shrinked.

4.2. Silicon wafers with a (110) crystallographic orientation

The modeling of the mobility has been carried out for the Si(110) wafers with the parameters obtained in **Table 2**. $\mu_0 = 285$ cm^2/Vs and $\theta = 0.038$ V^{-1} have been implemented in Eq. (9), and

the result is shown with the dashed line in **Figure 5** and does not provide a great accuracy like it was the case for Si(100) wafers. Nevertheless, the procedure has been moved forward, and the simulation of the drain current I_d and the transconductance g_m has been calculated with Eq. (8) and the following parameters: $\mu_0 = 285$ cm^2/Vs and $\theta = 0.038$ V^{-1}, $\Delta L = -0.4$ μm, $\Delta W = -0.4$ μm and $R_{acc} = 60$ Ω. The results for the drain current I_d are shown with the dashed lines in **Figure 7**, while the results for the transconductance g_m are shown in **Figure 8** with the dashed lines. The modeling is accurate at first but strongly divert from the experimental data when the gate overdrive voltage is increased. The use of Eq. (9) does not give at all satisfactory

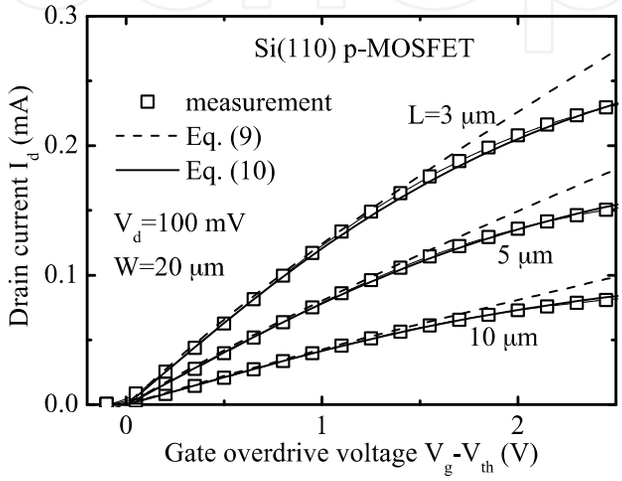

Figure 7. Drain current I_d as a function of the gate overdrive voltage V_g–V_{th} for Si(110) p-MOSFETs featuring different gate length. The dashed lines are the modeling carried out with Eqs. (8), and (9), $\mu_0 = 285$ cm^2/Vs and $\theta = 0.038$ V^{-1}. The full lines are the modeling carried out with Eqs. (1), and (10), $\mu_0 = 280$ cm^2/Vs, $\theta_1 = 0$ V^{-1}, $\theta_2 = 0.05$ V^{-2}, and $\alpha = 0.04$. $\Delta L = -0.4$ μm, $\Delta W = -0.4$ μm and $R_{acc} = 60$ Ω.

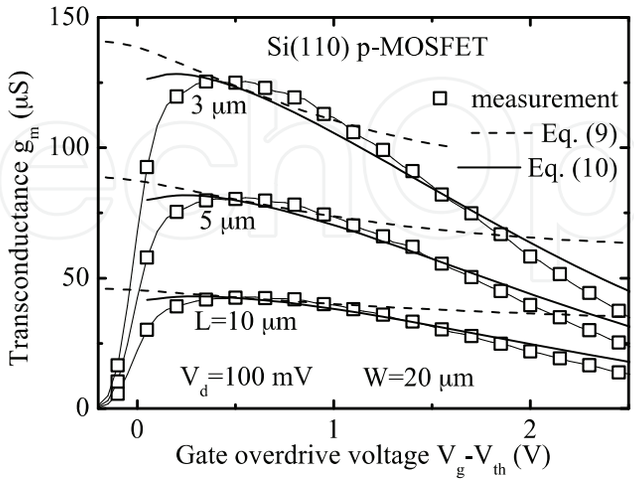

Figure 8. Transconductance g_m as a function of the gate overdrive voltage V_g–V_{th} for Si(110) p-MOSFETs featuring different gate length. The dashed lines are the modeling carried out with Eqs. (8), and (9), $\mu_0 = 285$ cm^2/Vs and $\theta = 0.038$ V^{-1}. The full lines are the modeling carried out with Eq. (8), and (10), $\mu_0 = 280$ cm^2/Vs, $\theta_1 = 0$ V^{-1}, $\theta_2 = 0.05$ V^{-2}, and $\alpha = 0.04$. $\Delta L = -0.4$ μm, $\Delta W = -0.4$ μm and $R_{acc} = 60$ Ω.

agreement with the experiment, especially concerning the transconductance g_m. The well-established model that is Eq. (9) cannot be used to simulate the mobility and thus the drivability of Si(110) p-MOSFETs. Other models [24, 25] have been implemented but did not give enough satisfactory results. Contrary to the (100) orientation for which the single phonon scattering mechanism is limiting the hole mobility over the working range, the hole mobility for the (110) orientation is limited by the Coulomb, phonon and surface roughness scatterings mechanism over the whole measurement range. Thus, a model able to take into account these three mechanisms is required. While Eq. (9), which models only the phonon scattering, is sufficient to simulate the Si(100) p-MOS transistors, a new model including all three scattering mechanisms is needed for the Si(110) wafers.

$\mu_{Coul} = A_{Coul}T^{-1}E_{eff}^{\beta_{Coul}}$ [26] with $\beta_{Coul} \geq 0$ and $\mu_{sr}=A_{sr}E_{eff}^{-2}$ [27] are simple ways to model the Coulomb scatterings and surface roughness scatterings, respectively. A_{Coul} and β_{Coul} are constants associated with the Coulomb scattering mechanism, while A_{sr} is a constant associated with the surface roughness scattering mechanism. T is the temperature. Assuming that the effective electric field E_{eff} is proportional to the gate overdrive voltage $V_g - V_{th}$, the dependence of the several scattering mechanisms can be introduced into Eq. (9), which is already modeling the Coulomb scatterings mechanisms to finally give [21]

$$\mu_{eff} = \mu_0 \frac{A_\alpha (V_g - V_{th})^\alpha}{1 + \theta_1 (V_g - V_{th}) + \theta_2 (V_g - V_{th})^2}. \tag{10}$$

μ_0 is the low field mobility. θ_1 corresponds to the conventional mobility attenuation factor seen in Eq. (9) and is related to the contribution coming from the phonon scatterings. θ_2 is a quadratic mobility attenuation factor related to the surface roughness scatterings. α is a parameter related to the Coulomb scatterings, while A_α equals to 1 and is introduced to maintain the uniformity of the unit system. As shown in **Figure 6** with the full line, Eq. (10) greatly matches the experimental data. The fitting parameters are as follows $\mu_0 = 280$ cm^2/Vs, $\theta_1 = 0$ V^{-1}, $\theta_2 = 0.05$ V^{-2}, and $\alpha = 0.04$. The simulation of the drain current I_d and the tranconductance g_m has been carried out for Si(110) p-MOSFETs featuring different gate length by implementing Eq. (10) into Eq. (8). $\mu_0 = 280$ cm^2/Vs, $\theta_2 = 0.05$ V^{-2}, $\alpha = 0.04$, $\Delta L = -0.4$ μm, $\Delta W = -0.4$ μm, $R_{acc} = 60$ Ω, $V_d = 100$ mV and $W = 20$ μm. The results are reported with the full lines in **Figures 7** and **8**. The modeling of the drain current I_d is greatly accurate even for short gate length. The modeling of the transconductance g_m in **Figure 8** is also fairly accurate. Both, the results regarding the drain current I_d and the transconductance g_m testify of the good agreement of Eq. (10). In **Figure 8**, it seems that the maximum of the transconductance g_m, result of α the parameter related to the Coulomb scatterings, can be also calculated. This statement must be taken with care since the maximum of the transconductance is obtained for biases that do not correspond to the linear region, making Eq. (8) obsolete. Actually, the parameter α does not solely reflect the Coulomb scatterings. Indeed, the hole mobility in Si (110) wafers has a peculiar behavior in the form of the inter-subband phonon scatterings. Contrary to the acoustic phonon scatterings that are more and more limiting the mobility with an increase of the effective electric field, the inter-subband phonon scatterings have the specificity to decrease when the effective electric field is increased [21, 28] as sketched in **Figure 5**.

5. Relation between the mobility, the channel direction and the wafer orientation

Inversion-mode fully depleted p- and n-channel silicon-on insulator (SOI) MOSFETs have been fabricated on bonded SOI (100) and (110) crystallographic silicon-oriented wafers. For each wafer, transistors with different channel directions were manufactured. The process flow has been entirely conducted in the clean room of the Fluctuation Free Facility at Tohoku University. 33-mm-diameter wafers have been used after cutting them from 8 inches wafers. The doping concentration has been adjusted to 10^{16} cm^{-3} by ion implantation. The thickness of the SOI layer was 50 nm, and the thickness of the buried oxide was 100 nm. Prior the formation of the 7.5-nm-thick gate oxide by radical oxidation [29] an alkali-free process [22, 30] able to keep the silicon surface flat was used. The roughness of the Si/SiO_2 interface was further reduced by repeating several times the procedure radical oxidation–etching [31]. The procedure has been repeated two times for the Si(100) wafers and four times for the Si(110) ones and led to the same microroughness measured to 0.08 nm. The effective mobility has been measured according to the methodology presented in Section 2 at V_d = 50 mV. Measurements have been carried out on MOSFETs with a gate dimension of W = 100 μm and L = 100 μm.

5.1. Silicon wafers with a (100) crystallographic orientation

The low field mobility μ_0, the mobility attenuation factor θ, the gate length reduction ΔL, the gate width reduction ΔW and the parasitic access resistances R_{acc} have been extracted for Si (100) n- and p-MOSFETs and are available in a previous paper by Gaubert et al. [32]. The Ghibaudo and Ciofi methods have been used. **Figure 9** shows the effective mobility for hole and electron on Si(100) wafers. It is clear that n-MOSFETs own greater performances than p-MOSFETs since the mobility of the former ones is five times higher than the mobility of the latter ones. It is also clear that the channel direction has no impact on the mobility of the n-MOSFETs. However, a slight difference can be noticed for the hole, the highest mobility being measured for a channel along the <100> direction. The direction of choice for the

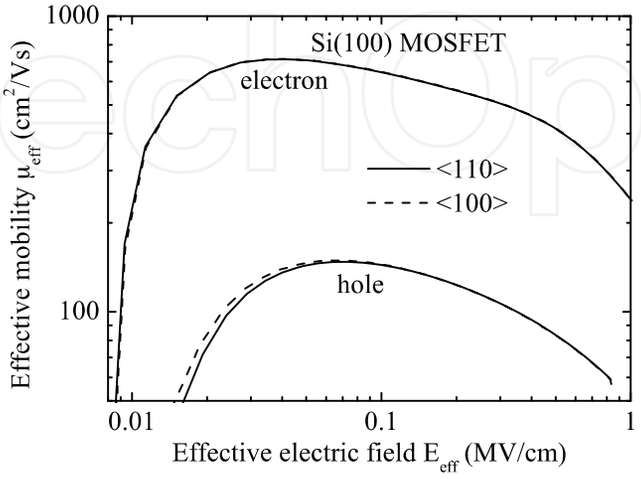

Figure 9. Electron and hole effective mobility μ_{eff} as a function of the effective electric field E_{eff} for Si(100) MOSFETs featuring a channel along the <110> (full lines) and <100> (dashed lines) directions.

electronic manufacturers is the <110> direction and an easy and costless way to slightly enhance performances of electronic devices would be to manufacture p-MOSFETs on Si(100) wafers with a channel following the <100> direction. The shift from the <110> direction for the <100> direction can give rise to a maximum enhancement of 10% of the drivability [12].

5.2. Silicon wafers with a (110) crystallographic orientation

It has been demonstrated in Section 3 that the extraction methods are difficult to set up for p-MOSFETs on Si(110) wafers. Nevertheless, the method proposed by Tsividis has been used for the Si(110) p-MOSFETs while the Ciofi and Ghibaudo method helped extract the conduction parameters for the Si(110) n-MOSFETs. The results are reported in a previous paper by Gaubert et al. [32]. The mobility in Si(110) p-MOSFETs is shown in **Figure 10**. The dependence with the channel is clearly visible. The highest mobility is obtained for a channel following the <110> direction, while the lowest one is obtained for a channel along the <100> direction. Furthermore, an increase in the mobility with the effective electric field can be noticed, especially for the <110> direction, where an increasing limitation by the phonon scatterings was expected. This behavior is caused by the inter-subband phonon scatterings as noticed in Section 4.2. The clear role played by the inter-subband phonon scatterings on limiting the mobility spans on a more visible way in **Figure 10** than in **Figure 5**. The reason is the lower doping concentration of the devices studied in this section that consequently shifts the Coulomb scattering limited mobility to lower effective electric fields. The inter-subband phonon scatterings are explained by the small energetic separation between the two lowest heavy-hole-like subbands, which is favoring the inter-subband transitions assisted by the absorption of optical phonon. This behavior reaches its maximum for a channel along the <110> direction since the holes in this direction have the lowest mass [12].

The $I_d - V_g$ curves for Si(110) n-MOSFETs have been measured, and the results are presented in **Figure 11** along with the corresponding tranconductances g_m. The larger drivability is ascribed to the <100> direction. From Ref. [32], the value of the attenuation factor θ for the Si(100)

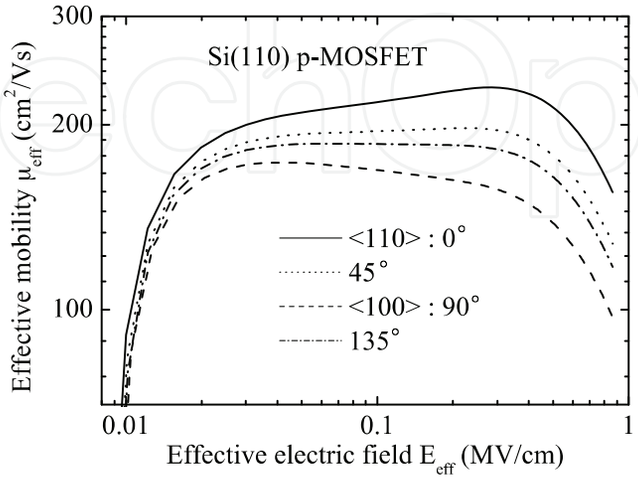

Figure 10. Effective mobility μ_{eff} as a function of the effective electric field E_{eff} for Si(110) p-MOSFETs featuring a channel along several directions.

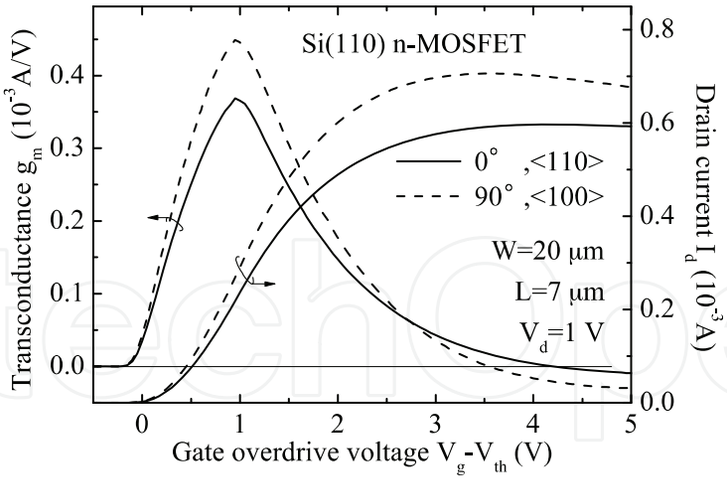

Figure 11. Drain current I_d (right) and transconductance g_m (left) as a function of the gate overdrive voltage V_g–V_{th} for Si (110) n-MOSFETs featuring a channel along the <110> (full lines) and <100> (dashed lines) directions.

n-MOSFETs is 0.175 V^{-1}, while the one obtained for the Si(110) n-MOSFETs is 0.6 V^{-1}. The larger value for Si(110) wafers reflects an unusual degradation of the mobility that makes the drain current I_d saturate and drop at high gate overdrive voltage $V_g - V_{th}$, as shown in **Figure 11**. The saturation and decrease in the drain current I_d are more pronounced for the <100> direction and find its origin in the balance of the linear product (current is proportional to nμ) between the increase in the number of carriers n and the decrease in the mobility μ. As shown in **Figure 11**, the unusual consequence is a negative transconductance g_m at high voltage. The mobility is shown in **Figure 12**. Like for the Si(110) p-MOSFETs and contrary to the Si(100) n-MOSFETs, there is a dependence between the mobility and the channel direction. The highest mobility is obtained for the <100> direction, and the lowest is obtained for the <110> direction, the opposite trend revealed for Si(110) p-MOSFETs. The surface roughness is limiting in more proportion the mobility of the transistors along the <100> direction and explains the more pronounced drop of the drain current I_d shown in **Figure 11**.

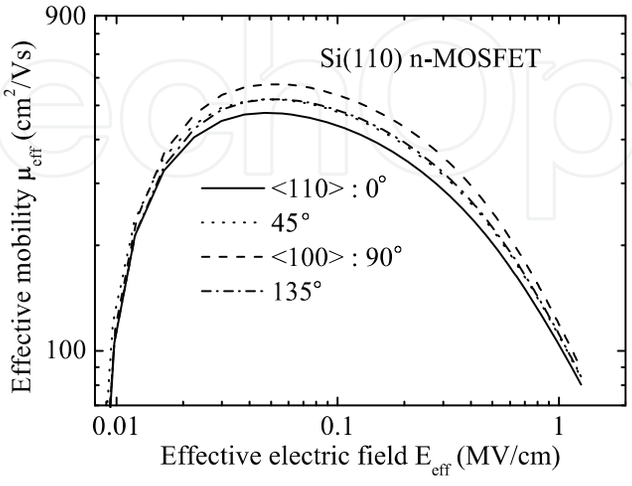

Figure 12. Effective mobility μ_{eff} as a function of the effective electric field E_{eff} for Si(110) n-MOSFETs featuring a channel along several directions.

http://dx.doi.org/10.5772/67885

6. Relation between the mobility and the temperature

It is well known that temperature has a major impact on the performances of MOSFETs. Every scattering mechanisms that are limiting the mobility have a specific response toward the change in temperature as Gaubert et al. demonstrated for Si(110) n-MOSFETs [33]. Contrary to p-MOSFETs fabricated on Si(110) wafers, the mobility of n-MOSFETs on this orientation is limited by the Coulomb scattering in the low range effective electric field, the phonon scattering in the middle range and finally the surface roughness scattering at high effective electric field. With the intention to understand the response of each scattering mechanisms taken individually to the temperature, a study has been conducted on Si(110) n-MOSFETs investigated in the precedent section. Transistors with a channel along the <100> direction have been studied for different temperatures from 213 to 473°K. **Figure 13** reports the drain current I_d and the associated transconductance g_m for three different temperatures. Increasing the temperature degrades the drivability and the transconductance even though a slight improvement in the latter quantity can be acknowledged at high gate voltage. In addition, the peculiar behavior acknowledged in the previous section for Si(110) n-MOSFETs, that is a saturation followed by a drop of the drivability with an increase of the gate voltage, is amplified with a decrease of the temperature and leads to even more negative transconductance in the high bias range. This suggests that the drop of temperature increases the degradation ratio generated by the surface roughness scattering mechanisms. The mobility for different temperatures is shown in **Figure 14**. As expected, the mobility is enhanced when the temperature is reduced. The scattering mechanisms have been studied separately by the means of the modeling. The mobilities shown in **Figure 14** have been modeled according the Matthiessen rule with the three main scattering mechanisms:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{Coul}} + \frac{1}{\mu_{Ph}} + \frac{1}{\mu_{SR}} = \frac{1}{A_{Coul}E_{eff}^{\beta}} + \frac{1}{A_{Ph}E_{eff}^{-0.3}} + \frac{1}{A_{SR}E_{eff}^{\gamma}}. \tag{11}$$

μ_{Coul} is the Coulomb-limited mobility, proportional to E_{eff}^{β} where β is a fitting parameter [34]. μ_{Ph} is the phonon-limited mobility, generally proportional to $E_{eff}^{-0.3}$ [11]. Finally, μ_{SR} is the surface

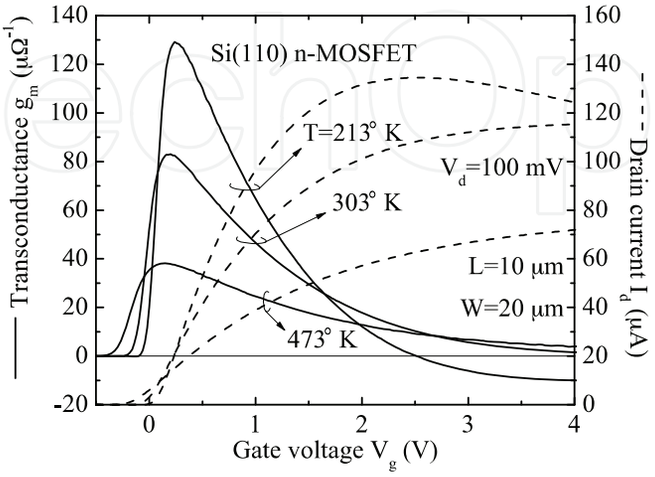

Figure 13. Drain current I_d (right) and transconductance g_m (left) as a function of the gate voltage V_g for Si(110) n-MOSFETs measured at three different temperatures.

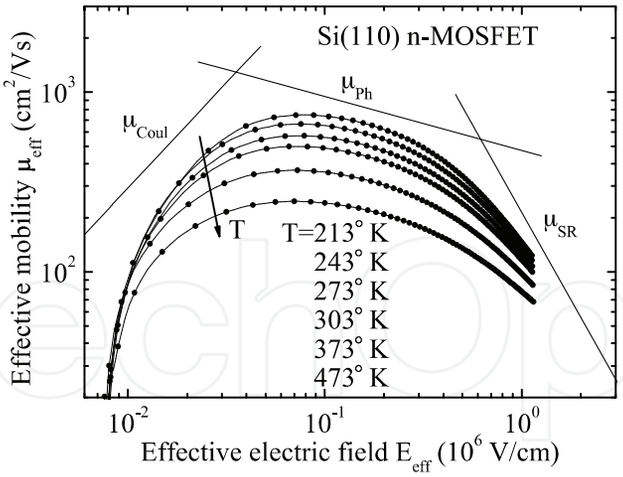

Figure 14. Effective mobility μ_{eff} as a function of the effective electric field E_{eff} for Si(110) n-MOSFETs measured at different temperatures. The several scattering mechanisms limiting the mobility have been also reported.

roughness-limited mobility. It is proportional to E_{eff}^{γ} [35] where γ is a fitting parameter generally found between −1 and −3. Quantities A_{Coul}, A_{Ph} and A_{SR} are fitting parameters associated, respectively, with the Coulomb, Phonon and Surface roughness scattering mechanisms.

The results for the Coulomb scattering mechanisms μ_{Coul} are shown in **Figure 15**. The Coulomb-limited mobility μ_{Coul} is temperature dependant, and β is varying between 0.8 and 1.2. A point independent of the temperature is visible for an effective electric field around 3×10^3 V/cm. It corresponds to the crossing point visible on the $I_d - V_g$ curves of **Figure 13** for V_g around 100 mV. Below that, point the temperature increases the energy of electron that are scattering less since the Coulomb interaction is weakening. Finally, results shown in **Figure 15** and those reported by Gaubert et al. [33] showing an attenuation of the variation of A_{Coul} with a decrease in the temperature suggests that the Coulomb-limited mobility μ_{Coul} might become independent of the temperature at low temperature. The results regarding the phonon-limited mobility μ_{Ph} are shown in **Figure 16**. The phonon-limited mobility μ_{Ph} is temperature

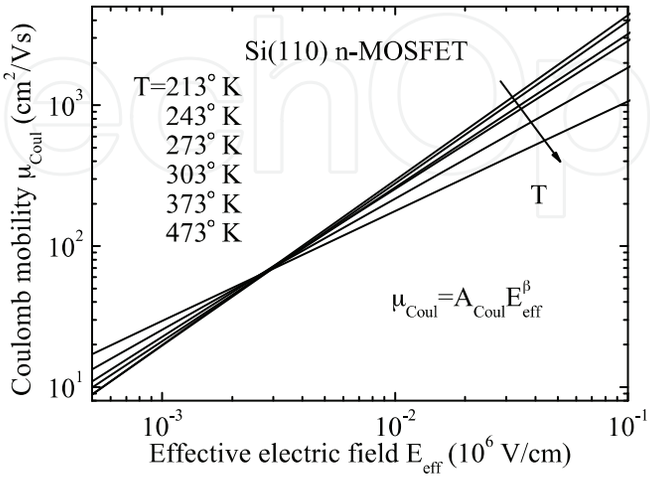

Figure 15. Extracted Coulomb mobility μ_{Coul} as a function of the effective electric field E_{eff} for Si(110) n-MOSFETs measured at different temperatures.

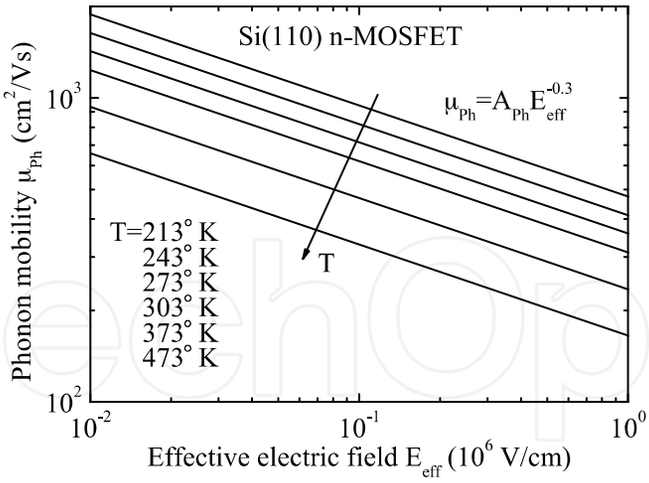

Figure 16. Extracted phonon mobility μ_{Ph} as a function of the effective electric field E_{eff} for Si(110) n-MOSFETs measured at different temperatures.

dependant according to a $T^{-1.3}$ law. Nevertheless, their ratio with the effective electric field remains unchanged with a change in temperature. The results regarding the surface-roughness-limited mobility μ_{SR} are shown in **Figure 17**. The surface-roughness-limited mobility μ_{SR} is temperature dependant. However, like for the Coulomb-limited mobility μ_{Coul}, the results at low temperature strongly suggest that the surface-roughness-limited mobility μ_{SR} becomes independent when the temperature is lowered down. Gaubert et al. [33] showed that A_{SR} is converging towards a constant value for temperature lower than 200°K, with γ reaching a value of −2. The surface-roughness-limited mobility μ_{SR} features a crossing point for effective electric field around 2 MV/cm, roughly corresponding to the breakdown of the gate oxide. Above this point, the increase in temperature is reducing the collision with the interface. The study of this peculiar behavior is made extremely difficult owing the impossibility to carry measurements on.

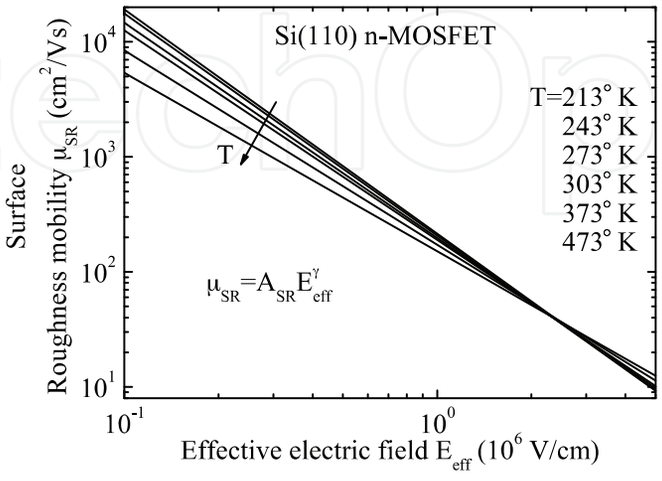

Figure 17. Extracted surface roughness mobility μ_{SR} as a function of the effective electric field E_{eff} for Si(110) n-MOSFETs measured at different temperatures.

To finish, the shift from the Si(100) wafers to the Si(110) wafers degrades the electron mobility as testified by results shown in **Figures 9** and **12**. The study of the mobility in Si(100) n-MOSFETs has been conducted in a similar way for 303° K exclusively, and the calculation of each scattering mechanisms showed that this degradation is actually the result of a strong limitation arising from the Coulomb and surface roughness scattering rather than the phonon mechanisms, results that has been demonstrated by Gaubert et al. [33].

7. Mobility in an accumulation layer

Even though making use of the majority carriers to generate the current [36, 37] is already known and has been investigated more than 40 years ago, this approach has recently gained interest, and recent studies have positioned the accumulation-mode MOSFETs as serious competitors [13, 14, 38–41] to take over the conventional transistors for future CMOS technologies. Scarce data have been published so far regarding the carrier mobility flowing inside an accumulation layer [14, 36], and a method to extract it from the conventional mobility measurement is proposed here since in accumulation-mode MOSFETs the conduction, and thus, the measured mobility involves the conduction inside the accumulation layer and the conduction occurring inside the SOI layer. Planar mode fully depleted silicon-on-insulator p-type MOSFETs on three different unibond p-type SOI (100) silicon oriented wafers have been fabricated in order to assess the mobility in an accumulation layer. The doping concentration of the SOI layer has been adjusted to 10^{15}, 10^{16} and 2×10^{17} cm^{-3}. A 7.5-nm-thick gate oxide has been formed by plasma oxidation after etching the SOI layer until reaching 50 nm. The mobility measurement method proposed in Section 2 has been followed with $Q_{dep} = 0$. The results are shown in **Figure 18**. The mobility for the conventional inversion-mode p-MOSFETs has been reported for comparison and accurately follows the universal curve by Takagi et al. [8] at high effective electric field E_{eff}. While the results suggest that the mobility for the accumulation-mode devices possessing a doping concentration of 10^{15} and 10^{16} cm^{-3} is following the universal curve, it is clear that the one with a doping concentration of 2×10^{17} cm^{-3}

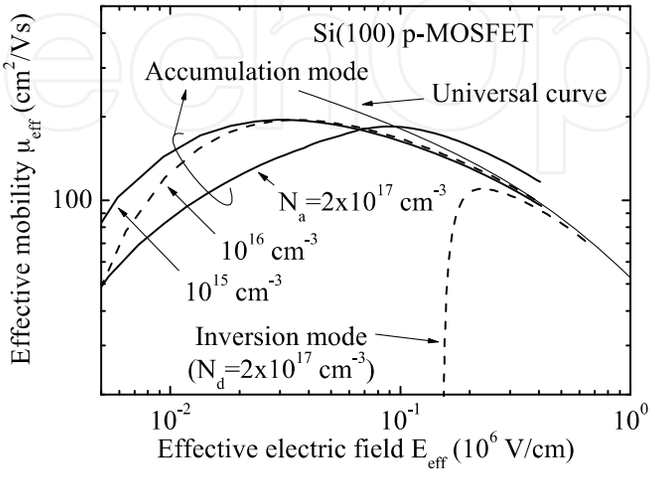

Figure 18. Experimental effective mobility μ_{eff} as a function of the effective electric field E_{eff} for accumulation- and inversion-mode Si(100) p-MOSFETs featuring different doping concentrations.

does not. As expressed previously, the SOI layer is contributing to the total measured current, and in turn, it is included in the calculation of the mobility as presented in Eq. (2). It is also clear from **Figure 19** that the calculation of Q_{acc} is false in the case of accumulation-mode MOSFETs. Indeed, the impact of the SOI layer is clearly visible and must be removed to obtain $C - V_g$ characteristics such as the one reported for an inversion-mode MOSFETs in **Figure 19**.

The appropriate evaluation of the mobility must be conducted from the relevant data, the accumulation charge and the current generated exclusively by the accumulation layer. At the flat-band voltage $V_{fb,}$ the SOI current reaches its maximum value and its subtraction from the $I_d - V_g$ curves give the current generated by the accumulation layer. V_{bf} is evaluated from the knowledge of the flat-band capacitance C_{fb} obtained from

$$\frac{1}{C_{fb}} = \frac{1}{C_{ox}} + \frac{1}{C_{deb}}, \tag{12}$$

where C_{deb} is the Debye capacitance and can be easily calculated like C_{ox}. V_{fb} is obtained with the help of the $C - V_g$ curves shown in **Figure 19**. By turn, the maximum SOI current and SOI charge are evaluated, respectively, from the $I_d - V_g$ and $Q_{acc} - V_g$ curves and subtracted afterwards. The calculation of the effective mobility μ_{eff} and of the effective electric field E_{eff} has been conducted again for the three doping concentration, and the results are shown in **Figure 20**. All curves are now reaching the universal curve indicating that an accumulation layer has a universal behavior identical to the one seen for an inversion layer. The universal curve by Takagi et al. [8] is appropriate for both the inversion and accumulation layers. It is also confirming the rightfulness of $\eta = 1/3$ for the calculation of the effective electric field E_{eff} in Eq. (7) indicating again that the carriers in an accumulation layer are behaving in a similar way than the ones in an inversion layer with regard to the phonon and surface roughness scattering mechanisms as previously described by Chindalore et al. [42]. To finish contrary to the inversion layer, an early screening of the Coulomb scattering is occurring in the case of an accumulation layer, allowing the mobility in an accumulation layer to reach at first the bulk mobility

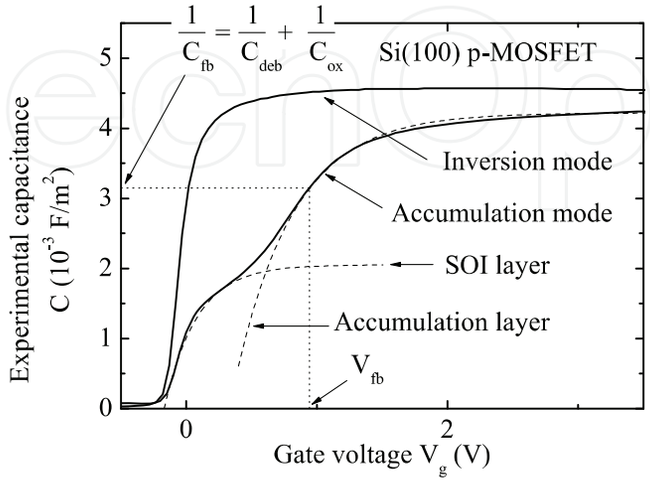

Figure 19. Experimental capacitance C as a function of the gate voltage V_g for accumulation- and inversion-mode Si(100) p-MOSFETs with a doping concentration $N_{d(a)} = 2 \times 10^{17}$ cm^{-3}. The capacitance has been measured at $V_d = 100$ mV and a frequency f = 100 kHz.

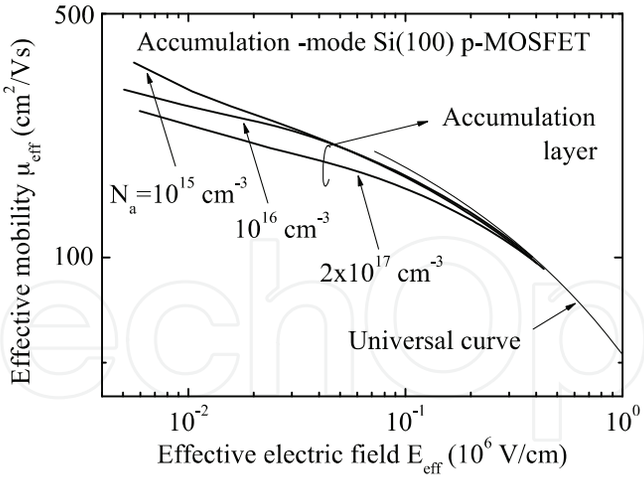

Figure 20. Calculated effective mobility μ_{eff} inside the accumulation layer of accumulation-mode Si(100) p-MOSFETs featuring different doping concentrations as a function of the effective electric field E_{eff}.

before the phonon scatterings dominate [14, 43], thus the monotonically decrease in the mobility seen at low effective electric field E_{eff} in **Figure 20**.

These last results indicate that even if the mobility shown in **Figure 18** for accumulation-mode MOSFETs with a doping concentration 10^{15} and 10^{16} cm^{-3} could have been interpreted as correct, are actually false owing to the contribution of the SOI layer.

8. Conclusion

In this chapter, we reviewed some of the main aspects of the mobility in field-effect transistors and especially for the (110) crystallographic silicon-oriented wafers. The mobility in p-MOSFETs on Si(110) wafers is limited by inter-subband scattering mechanism making its extraction by the means of the Ghibaudo method inappropriate and in turn its modeling inaccurate. A more adapted model relying on a physical approach has been developed. This new expression is incorporating the Coulomb, phonon and surface roughness scattering mechanism and is allowing a precise modeling of the drivability and transconductance in Si(110) p-MOSFETs. In addition, the study showed a clear dependency between the mobility and the channel direction for transistors fabricated on Si(110) wafers, while no impact has been noticed for conventional Si(100) wafers. The highest mobility has been revealed for a channel along the <100> direction for electron and along the <110> direction for hole. The study in temperature in Si(110) n-MOSFETs showed that the Coulomb and surface roughness scattering mechanisms are actually temperature dependent. More, the degradation of the electron mobility in Si(110) wafers has been explained by a substantial increase in the Coulomb and surface roughness scatterings than the phonon ones when compared with the Si(100) wafers. To finish, a methodology has been proposed and successfully employed to calculate the carrier mobility in the accumulation layer of newly developed accumulation-mode MOSFETs. The result showed afterwards that accumulation and inversion layers are behaving in a similar way in regard to the phonon and surface roughness scattering mechanism. Nevertheless, the mobility in an accumulation layer

is monotonically decreasing from the bulk mobility when the electric field is increased, owing to an earlier screening of the carrier by the Coulomb scatterings.

Author details

Philippe Gaubert[1]* and Akinobu Teramoto[2]

*Address all correspondence to: gaubert@m.tohoku.ac.jp

1 Graduate School of Engineering, Tohoku University, Sendai, Japan

2 New Industry Creation Hatchery Center, Tohoku University, Sendai, Japan

References

[1] Lilienfeld, JE. Method and apparatus for controlling electric currents. U. S. Patent No. 1,745,175 (Filed October 8, 1926. Issued January 18, 1930).

[2] Brattain, Walter. Bell Labs Logbook (December 1947). pp. 7–8, 24. https://www.pbs.org/transistor/science/labpages/labpg5.html

[3] Teramoto A, Hamada T, Yamamoto M, Gaubert P, Akahori H, Nii K, et al. Very high carrier mobility for high-performance CMOS on a Si(110) surface. IEEE Trans Electron Dev. 2007;54(6):1438–1445.

[4] Barsan RM. Analysis and modeling of dual-gate MOSFET's. IEEE Trans Electron Dev. 1981;28:523–534.

[5] Chang D, Lee M, Chen D, Liva V. Power junction FETs (JFETs) for very low-voltage applications. Proc. IEEE APEC; Austin, USA, 2005, 1419–1423.

[6] Gill DM, Kane BC, Svensson SP, Tu DW, Uppal PN, Byer NE. High-performance, 0.1 μm InAlAs/InGaAs high electron mobility transistors on GaAs. IEEE Electron Dev Lett. 1996;17(7):328–330.

[7] Akarvardar K, Cristoloveanu S, Gentil P. Analytical modeling of the two-dimensional potential distribution and threshold voltage of the SOI four-gate transistor. IEEE Trans Electron Dev. 2006;53(10):2569–2577.

[8] Takagi S, Toriumi A, Iwase M, Tango H. On the universality of inversion layer mobility in Si MOSFET's: part I—effects of Substrate Impurity Concentration. IEEE Trans Electron Dev 1994;41(12):2357–2362.

[9] Sabnis AG, Clemens JT. Characterization of the electron mobility in the inverted <100> Si surface. Int Electron Dev Meet. 1979:18–21.

[10] Saitoh M, Kobayashi S, Uchida K. Physical understanding of fundamental properties of Si (110) pMOSFETs inversion-layer capacitance, mobility universality, and uniaxial stress effects. Int Electron Dev Meet. 2007:711–714.

[11] Takagi S, Toriumi A, Iwase M, Tango H. On the universality of inversion layer mobility in Si MOSFET's: part II—effects of surface orientation. IEEE Trans Electron Dev. 1994;41 (12):2363–2368.

[12] Gaubert P, Teramoto A, Cheng W, Ohmi T. Relation between the mobility, 1/f Noise, and channel direction in MOSFETs fabricated on (100) and (110) silicon-oriented wafers. IEEE Trans Electron Dev. 2010;57(7):1597–1607.

[13] Cheng W, Teramoto A, Hirayama M, Sugawa S, Ohmi T. Impact of improved high-performance Si(110)-oriented metal–oxide–semiconductor field-effect transistors using accumulation-mode fully depleted silicon-on-insulator devices. Jpn JAppl Phys. 2006;45 (4B):3110–3116.

[14] Gaubert P, Teramoto A, Sugawa S, Ohmi T. Hole Mobility in accumulation mode metal-oxide-semiconductor field-effect-transistors. Jpn J Appl Phys. 2012;51:04DC07-1~6.

[15] Merckel G, Borel J, Cupcea NZ. An accurate large-signal MOS transistor model for use in computer-aided design. IEEE Trans Electron Dev. 1972;19(5):681–690.

[16] Schreutelkamp RJ, Deferm L. Internal report IMEC, n° P30005-IM-FP-001. 1993.

[17] Schreutelkamp RJ, Deferm L. A new method for measuring the saturation velocity of submicron CMOS transistors. Solid-State Electron. 1995;38(4):791–793.

[18] Tsividis Y. Operation and Modeling of The MOS Transistor. s.l.: McGraw-Hill, 1999. p. 521.

[19] Ghibaudo G. New method for the extraction of MOSFET parameters. Electron Lett. 1988;24(9):543–545.

[20] Ciofi C, Macucci M, Pellegrini B. A new measurement method of MOS transistor parameters. Solid-State Electron. 1990;33(8):1065–1069.

[21] Gaubert P, Teramoto A, Ohmi T. Modelling of the hole mobility in p-channel MOS transistors fabricated on (110) oriented silicon wafers. Solid-State Electron. 2010;(54):420–426.

[22] Gaubert P, Teramoto A, Hamada T, Yamamoto M, Kotani K, Ohmi T. 1/f Noise Suppression of pMOSFETs Fabricated on Si(100) and Si(110) Using an Alkali-Free Cleaning Process. IEEE Trans Electron Devices. 2006;53(4):851–856.

[23] Gaubert P, Teramoto A, Suwa T, Ohmi T. Accurate extraction of conduction parameter in MOSFETs on Si(110) surface. Proc. 28th International Conference on the physics of semiconductors; Hawaii, USA 2006:1393–1394.

[24] Ong TC, Ko PK, Hu C. 50-Å Gate-oxide MOSFET's at 77 K. IEEE Trans Electron Devices. 1987;34(10):2129–2135.

[25] Ghibaudo G, Balestra F. A method for MOSFET parameter extraction at very low temperature. Solid State Electron. 1989;32(3):221–223.

[26] Stern F. Two-subband screening and transport in (001) Si inversion layers. Surf Sci 1976;73:197–206.

[27] Hartstein A, Ning TH, Fowler AB. Electron scattering in silicon inversion layers by oxide and surface roughness. Surf Sci 1976;58:178–181.

[28] Fischetti MV, Ren Z, Solomon PM, Yang M, Rim K. Six-band k.p calculation of the hole mobility in silicon inversion layers: dependence on surface orientation, strain, and silicon thickness. J ApplPhys 2003;94(2):1079–1095.

[29] Sekine K, Saito Y, Hirayama M, Ohmi T. Highly reliable ultrathin silicon oxide film formation at low temperature by oxygen radical generated in high-density krypton plasma. IEEE Trans Electron Devices. 2001;48(8):1550–1555.

[30] Ohmi T. Total room temperature wet cleaning for Si substrate surface. JElectrochem Soc. 1996; 143(9): 2957–2964.

[31] Morita Y and H. Tokumoto. Atomic scale flattening and hydrogen termination of the Si(001) surface by wet-chemical treatment. JVacSciTechnol A Vac Surf Films. 1996;14(3):854–858.

[32] Gaubert P, Teramoto A, Cheng W, Hamada T, Ohmi T. Different mechanism to explain the 1/f noise in n- and p-SOI-MOS transistors fabricated on (110) and (100) silicon-oriented wafers. JVacSci Technol. BMicroelectron ProcessPhenom. 2009;27(1):394–401.

[33] Gaubert P, Teramoto, Sugawa S, Ohmi T. The role of the temperature on the scattering mechanisms limiting the electron mobility in metal-oxide-semicoductor field-effect-transistors fabricated on (110) silicon-oriented wafers. Proc. 42th European Solid-State Device Research Conference; Bordeaux, France 2012:213–216.

[34] Stern F, Howard WH. Properties of semiconductor surface inversion layers in the electric quantum limit. Phys Rev. 1967;(163):816–835.

[35] Mazzoni G, Lacaita AL, Perron LM, Pirovano A. On surface roughness-limited mobility in highly doped n-MOSFETs. IEEE Trans Electron Dev. 1999;(46):1423–1428.

[36] Sun SC, Plummer JD. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. IEEE Trans Electron Dev. 1980;27(8):1497–1508.

[37] Ando T, Fowler AB, Stern F. Electronic properties of two-dimensional systems. Rev Mod Phys. 1982;54:437–672.

[38] Colinge JP, Lederer D, Afzalian A, Yan R, Lee CW, Akhavan ND, Xiong W. Properties of accumulation-mode multi-gate field-effect transistors. Jpn J Appl Phys. 2009;48(3):034502-1∼7.

[39] Cheng W, Teramoto A, Ohmi T. Experimental demonstration and analysis of high performance and low 1/f noise Tri-gate MOSFETs by optimizing device structure. Microelectron Eng. 2009;86(7/9):1786–1788.

[40] Gaubert P, Teramoto A, Sugawa S. Impact of doping concentration on 1/f noise performances of accumulation-mode Si(100) n-MOSFETs. Jpn J Appl Phys. 2016;55:04ED08-1~6.

[41] Gaubert P, Teramoto A, Sugawa S. Performances of accumulation-mode n- and p-MOSFETs on Si(110) wafers. Jpn J Appl Phys. 2017;56:04CD15-1∼7.

[42] Chindalore GL, McKeon JB, Mudanai S, Hareland SA, Shih WK, Wang C, Tasch AF, Maziar CM. An improved technique and experimental results for the extraction of electron and hole mobilities in MOS accumulation layers. IEEE Trans Electron Dev. 1998;45:502–511.

[43] Mudanai S, Chindalore GL, Shih WK, Wang H, Ouyang Q, Tasch AF, Maziar CM, Banerjee SK. Models for electron and hole mobilities in MOS accumulation layers. IEEE Trans Electron Dev. 1999;46:1749–1759.