Chapter 7

Macroporous Silicon: Technology and Applications

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Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/67698

Abstract

Macroporous silicon (MPS) is a versatile material that since its origin in the early 1990s has seen intense research and has found applications in many fields. MPS is a key technology in photonic crystals research, and optic and photonic applications are its main applications. However, this chapter is devoted to several of the non-photonic uses of MPS. In particular, new electronic and MEMS devices and applications will be described. Furthermore, in this chapter, the technology of MPS fabrication will be presented.

Keywords: macroporous silicon, electrochemical etching, field effect transistors, supercapacitors, microneedles, MEMS

1. Introduction

Macroporous silicon (MPS) is a novel material, which was described as such in the early 1990s by Lehmann in his pioneering works [1–3] and by other researchers [4, 5]. Since its first description, MPS has attracted great interest, and it has been suggested for many applications in several fields such as electronics [6], optics [7], photonics [8], solar cells [9], and even energy storage [10], fuel cells [11] or catalysis [12].

One particular form of MPS consists on an ordered arrangement of the pores that are etched on the silicon bulk. In such form, the primary interest of MPS is as photonic crystals (PCs). However, as it will be revealed throughout the chapter, many other applications have been proposed for MPS, which does not make use of that interesting optical properties. For such cases, the use of an ordered array of pores may not be necessary, but in many cases, this can give certain advantages.

In the present chapter, a brief review on the technology of macroprorous silicon, its fabrication techniques and its applications will be presented. In this chapter, special emphasis is made regarding the *non-photonic* applications of MPS.

2. Brief history of macroporous silicon

Electrochemical etching (EE) of silicon (and germanium) was known from the late 1950s. The works of Uhlir [13], Turner [14] and others [15] were the first to study the semiconductor dissolution in an electrolyte under anodic conditions. These initial works dealt with electropolishing of the semiconductor in order to obtain flat, defect-free surfaces or for bulk thinning. However, it was noticed that under certain conditions, pits were formed instead of a uniform etching over the treated surface [13, 14]. In particular, low voltages and currents, or the pre-existence of surface defects, were found to promote surface pitting, preferentially at surface irregularities or defects. Therefore, this allows removing material locally in a more or less controlled manner. The processing of surfaces done by this technique in the described way gives rise to *porous materials*, in which a portion or the whole of it is *porosified*, resulting in a sponge-like structure. An example of this process is schematically shown in **Figure 1**.

Hydrofluoric acid (HF) is one of the electrolytes used for EE. Its interest is that, in ambient conditions, it reacts very slowly with silicon[1] but readily etches the semiconductor when an electric current flows through the electrochemical cell. The anodic oxidation of silicon in hydrofluoric acid with the correct potential and current produces *porous silicon*[2] (PS). The first specimens of PS were found to be *microporous* with a random distribution of the etched voids. However, this first form of PS was not initially distinguished as microporous, and, nowadays, the term PS is still used to refer to its microporous form.

After the discovery, the interest of this new material in fields such as electronics and photonics became clear. Later on, the macroporous form of PS was developed, and it has also shown its potential in fields as different as catalysis [16], drug delivery [17], energy storage [18] or optical

Figure 1. Electrochemical set-up for semiconductor etching and electropolishing. Details of the surface during several steps of the etching process are shown in panels (A), (B) and (C). Initially, the surface has a low content of defects such as pits, dislocations or protrusions. After the anodic treatment is started with the right conditions, the surface (B) shows a certain degree of electropolishing but existing pits start growing, and new pits evolve. After a prolonged treatment, the surface and bulk (C) show noticeable change, and pores grow deep into the sample creating a sponge-like material.

[1]Silicon dissolution in HF is a thermodynamically favourable process; however, the dissolution rate is very small: $R_{Si} = 2.5 \times 10^{23}\ cm^{-2}\ s^{-1}$ (about 0.3 Å/min) at room temperature [33].

[2]It must be noted that electrochemical etching is one possible method to obtain porous silicon. A different technique is stain etching. This is a purely chemical method based on the chemistry of silicon in HF – HNO_3 mixtures, which also produces PS. See for example [24].

sensors [7]. The first instances of MPS can be found in the early 1990s in Lehmann's pioneering works on fabrication [1, 2] and application of macroporous silicon [19]. In his works, he focused primarily on the formation of ordered MPS in a controlled manner. The fabrication technique used in his works was the *photo electrochemical etching* (PECE) of silicon in HF and was thoroughly characterized [3]. Nevertheless, PECE is not the only method available for MPS fabrication, the other main one being (*deep*) *reactive ion etching* ([D]RIE). MPS will be covered in more detail in the next section. In this chapter, particular emphasis will be made on the photo electrochemical fabrication process as described by Lehmann.

2.1. What is macroporous silicon?

Macroporous silicon is a particular form of porous silicon. One way of classifying porous silicon is looking at the 'pore size'. According to the IUPAC [20], the material can be designated as *microporous* for pore sizes below 2 nm, then *mesoporous* for sizes under 50 nm, and *macroporous* for pore diameters larger that 50 nm. However, this simple classification does not give enough information about the material, as the pore morphology can vary greatly, and therefore, the 'pore size' cannot be precisely defined. In spite of these limitations, the average pore diameter d_{pore} is often regarded as the 'pore size'. MPS has an average pore diameter greater than 50 nm, and in practical realizations of the material, typical pores are larger than 100 nm.

Besides pore size, MPS can also be described either as ordered or random regarding the surface pore growth site distribution; this is shown in **Figure 2**. Nevertheless, the individual pore diameter distribution is not generally accounted in the classification of the material. Other morphological characteristics of macroporous silicon such as pore shape, branching, depth or depth profile are not normally considered when classifying MPS.

MPS is a versatile material that has some very interesting properties. To begin with, silicon is the material of choice in the semiconductor and MEMS industry. This opens the possibility to use many of the existing production methods, techniques, experience and equipment available in VLSI foundries and research labs. As a result, important costs savings can be achieved for the development and fabrication of devices based on MPS. Furthermore, it has been shown that by employing standard CMOS fabrication methods, it is possible to integrate MPS (and PS in general) into VLSI devices [21]. The possibility of monolithic integration is a clear advantage

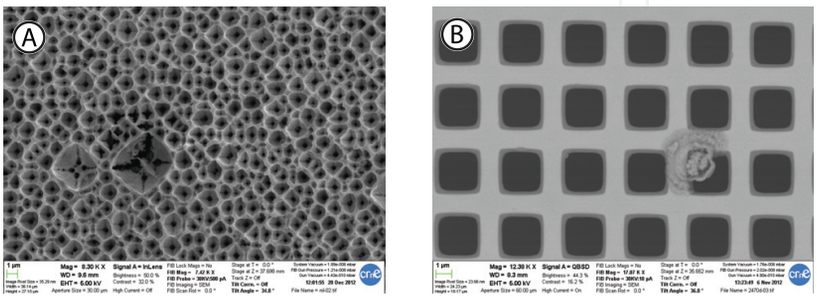

Figure 2. Top view of random (A) and ordered (B) macroporous silicon. Pore radius may not be uniform, as shown in the random sample (A).

of MPS for next-generation device fabrication. Furthermore, MPS can be processed to create complex structures, as those of **Figure 3** from Ref. [22]. The as-etched structures can be further processed to alter some morphological properties [23], to passivate the surface or to functionalize the MPS device with coatings such as catalysts [12], nanoparticles and others.

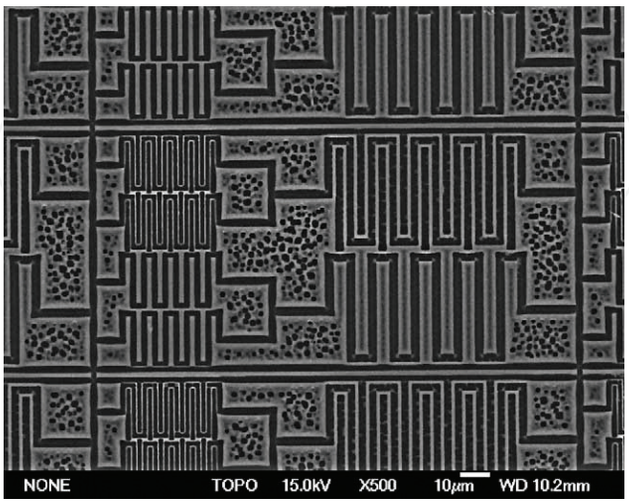

Figure 3. Complex MPS structure fabricated with the PECE of silicon in HF. Reprinted from [22], Copyright 2002, with permission from Elsevier.

3. Fabrication of macroporous silicon

There exist several microfabrication and micromachining techniques that allow the production of MPS devices. Due to its historical importance, and because it allows micromachining in three dimensions, the *electrochemical etching* of silicon remains one of the most important and versatile fabrication methods, as will be shown later. The next method in importance is *reactive ion etching*. Other remarkable methods[3] include electroless etching of silicon[4] (stain etching [24], metal-assisted etching [25], etc.), direct laser writing (DLW) [26], lithographic methods (layer-by-layer [27], interference lithography [28], block copolymer [29] …) and glancing angle deposition [30].

3.1. Reactive ion etching

RIE is a well-known method for shaping silicon in microelectronics and MEMS device fabrication [31]. A succinct description is as follows: this is a dry etching process where a plasma of a specific mixture of gases is used to selectively remove material from the stock. This process is done in a low-pressure chamber. A mask is necessary to define the affected regions, and the etch proceeds anisotropically in the unmasked areas. The material is eroded at a speed that depends on the gas mixture, temperature, chamber pressure and power of the plasma. As described, RIE is simply a necessary step in the fabrication of MPS, as the mask can be defined

[3]An exposition of the different methods for PC fabrication and their possibilities can be seen in Ref. [89].

[4]For a general treatment on the subject, see Ref. [33].

by several means. For instance, layer by layer or DLW may or may not require the use of RIE for the fabrication of MPS and PCs.

The most interesting aspects of RIE for the processing of MPS are that it allows defining very small features, and that it is completely integrated into the VLSI fabrication process flow. Using RIE to create the pores gives great freedom in the mask layout as both processes are independent. This allows adding point defects, linear defects or other lattice disordering elements. This ability is of great interest for light processing and optical devices, such as waveguides, interferometers or resonators. It is, however, not limited to the photonics field, as it has also been demonstrated for electronic applications such as capacitors.

In spite of these advantages, the fabrication of MPS with RIE has some limitations. Firstly, etching high aspect ratio[5] (AR) pores into silicon using plain RIE can be tricky. Effects such as masking, microloading, footing or redeposition must be taken into account, otherwise the resulting pores will not have a uniform profile in depth. These effects are particularly serious when trying to develop high AR trenches, as pores may close after a certain depth and grow no further. For deeper pores, a DRIE process must be adopted. Nevertheless, DRIE leaves 'large' scallops on the sidewalls that are generally undesired. Besides this, MPS fabricated by RIE is limited to 2-d structures, as the etched features depend on a planar mask[6] and material etching is essentially in the direction of the plasma electric field.

3.2. Electrochemical etching

Electrochemical etching of silicon is a very versatile method for the fabrication of MPS. As was found from the initial works on silicon etching, silicon can be selectively dissolved when immersed in an HF bath, and an electric current flows through. Therefore, this in an *electrochemical* method as a current is needed to activate the chemical reactions that dissolve silicon. In the absence of such current, the silicon substrate remains practically unaltered. Furthermore, to perform the etching, the silicon must be the *anode* in the electrochemical system. Otherwise, there will be no reaction at the surface, as for the reactions to occur holes must be exchanged. Both n- and p-type silicon can be dissolved by this technique.

The pore evolution and morphology using the EE method depends on several factors. On one hand, the current density and electrode potential determine de amount of etched silicon but have little influence in the advance of the 'pore front', that is the etch velocity. On the other hand, the electrolyte concentration, temperature, and optional additives affect the etch velocity and pore shape, and limit the practical operation area of the electrical parameters [1, 32]. Furthermore, the Si bulk characteristics such as doping type and density, crystal orientation, and carrier lifetime strongly determine the morphology of the pores, and the obtainable pore dimensions [32].

In the porous layer formation regime, it has been found that currents through the electrochemical cell have a similar shape to that shown in **Figure 4** (for n-type silicon). In particular, PS formation

[5]'Aspect ratio' is defined as the ratio between the pore width over the pore length.

[6]Some attempts have been made into creation of 3-d PCs exploiting the scalloping effect of RIE; however, progress has been slow [90].

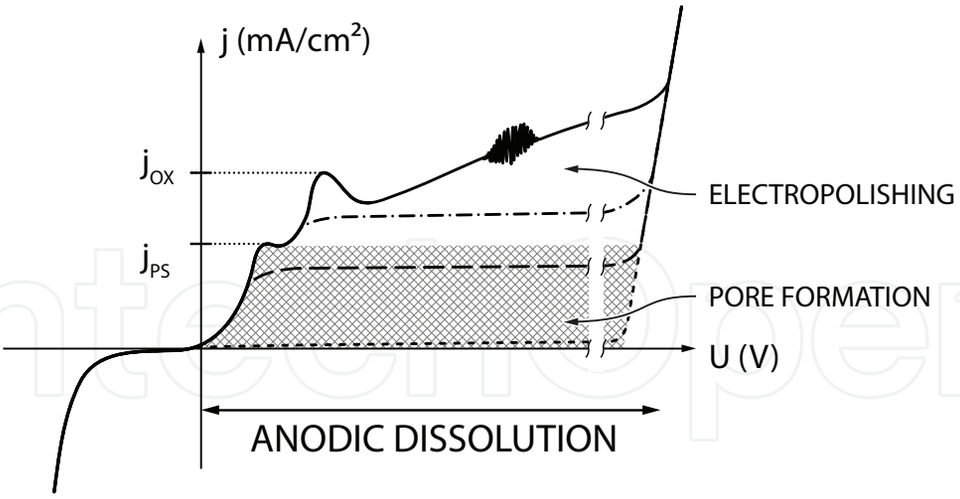

Figure 4. Currents through an H/Si electrochemical system for different applied potential and illumination. The shown $j(v, \Phi_e)$ is for an n-type silicon bulk. Solid line (—) is for 'infinite' illumination, dash-dot (— •) is for high illumination intensity, dash (—□—) is for medium IR intensity, and short dash (–□–) is for no illumination condition.

occurs if the current density is kept below J_{PS}. Larger currents will start to electropolish the surface of the semiconductor. For very large currents, $j > J_{ox}$, only electropolishing will take place. The chemical processes involved in the dissolution of silicon are quite complex and depend on the local current intensity and fluoride ion concentration. Two competing mechanisms act on the silicon surface: formation of SiO_2 and subsequent dissolution by HF, and direct dissolution of silicon [4, 33]. Oxide formation and dissolution consume four holes, and thus have valence 4 ($\lambda = 4$). On the other hand, direct dissolution of silicon requires two to three holes depending on light intensity: low intensity favours $\lambda = 3$, while high intensity favours $\lambda = 2$. More insight on the chemicophysical aspects of silicon dissolution can be found in the works of Lehmann [2, 3], Zhang [4, 32] and Kolasinski [33].

The electrical characteristics of the silicon wafer substrate are determinant for the morphology of the etched pores. The size of the resulting pores is strongly dependent on the wafer resistivity (as seen in **Figure 5**) and the use of a mask to define the nucleation centres. From Lehmann's [3] and Zhang's [4] work, in the MPS etching regime, the pore morphology and growth are basically dependent on the space charge region (SCR) formed in the pore region in contact with the electrolyte. It was proposed that etching occurs at localized sites with a current density of J_{PS} whose value is just a function of the weight concentration of hydrofluoric acid: $J_{PS} = Kc^{3/2} \exp(-E_a/kT)$. The pore growth speed depends only on the current passing through the etched areas; thus, it can be calculated by the removed charge and valence of the reaction: $v = J_{PS}/nq_eN_{Si}$. Here, $K = 3300$ mA cm^{-2} is an empirically determined constant, c (wt. % HF) is the electrolyte concentration, $E_a = 343$ meV is the empirically found activation energy, k is the Boltzmann constant, T is the temperature in Kelvin, n is the reaction valence, q_e is the electron charge (1.602×10^{-19} C), and N_{Si} is the atomic density of silicon (5×10^{22} cm^{-3}) [2]. Typical concentration of HF used for MPS etching is around 2.4–10%.

In the case of ordered MPS, where a mask is used to define the pore growth sites (nucleation centres), etching current at the tips will be such that $j_{tip} = J_{PS}$; thus, the pore will advance at the

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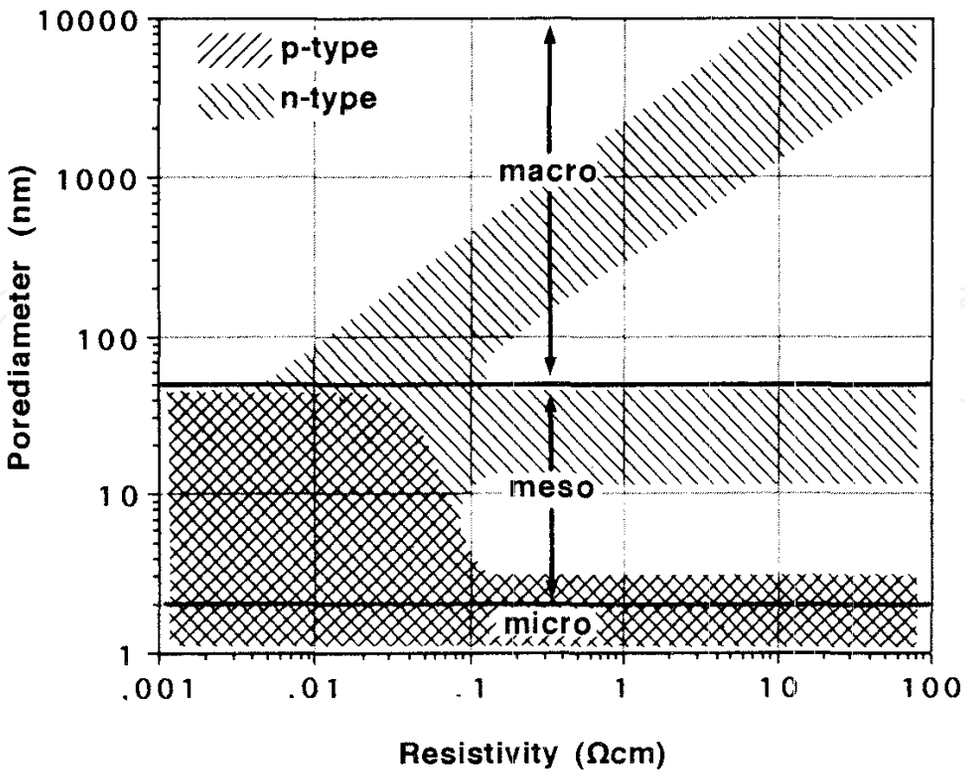

Figure 5. Etched pore diameter for different silicon doping type and concentration. © 1996 IEEE. Reprinted, with permission, from [19].

same speed irrespective of pore size. However, by adjusting the total current through the Si substrate, it is possible to change the actual etched area (and thus pore diameter) since porosity $p = A_{\text{total}}/A_{\text{etched}} = j/J_{\text{PS}}$. The pattern for the pore distribution can be fabricated using any lithographic means like UV or NIL. The mask can be a corrosion-resistant material such as silicon nitride, but, given that MPS etching is highly anisotropic and selective under the correct parameters, it is possible to transfer the pattern directly to the silicon and create *etch pits* at the desired sites that will act as nucleation points. This will promote the pore formation at *only* these sites. The unreacted silicon 'left behind' the pore tip is further passivated by hydrogen adsorption reducing the already low Si etch rate in HF.

As holes are needed for the porosification, for n-type silicon, these need to be generated somehow. One of the most extended methods is PECE, after the work by Lehmann [2]. This method requires illuminating the work silicon with suitable IR light; thus, the etching cell and controlling system must be similar to the one depicted in **Figure 6**. In such system, the cell current is proportional to the illumination intensity. Knowing the current limits from **Figure 4**, the computer control can be programmed to adjust the photogenerated current and cell potential to keep the pore growth stable. Electrolyte temperature is also controlled, as variations of it will change the J_{PS} and thus the etching speed. HF is pumped through the cell to remove any gas bubbles that may form from the release of hydrogen during etching and to provide fresh electrolyte. The electrical contact on the Si substrate may be done by coating with a thin transparent conductor or by physical contact with a different electrolyte on the backside. The simple configuration shown in **Figure 6** uses a high-doped layer on the backside with a probe to contact the backside. Oxygen

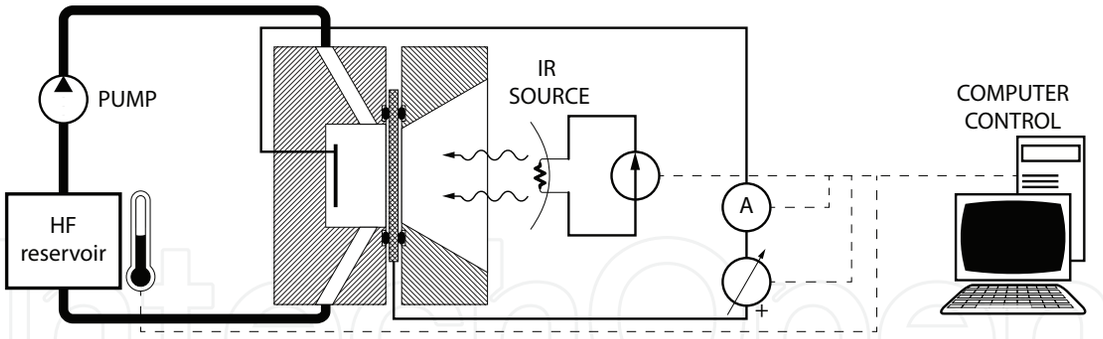

Figure 6. Etching system used in the MNT group for the fabrication of MPS.

dissolved in the electrolyte can also affect the pore shape, particularly if these are very deep. To reduce the unwanted oxidation, purging the electrolyte with bubbling N_2 is recommended.

It was seen that pore diameter (porosity) can be controlled in MPS by adjusting the photogenerated etching current. This is exploited to create 3-d structure by freely changing the IR illumination intensity as the pores progress. In spite of the limits to the achievable shapes imposed by the electrochemical system, it is possible to create very complex structures like chirped modulations [34], embedded defects [35], etc. MPS with pores with diameters down to 100 nm has been reported [36]; however, only straight pores have been shown, and surface quality is still low. Better pores are obtained for $d_{\text{pore}} = 275\ \mu\text{m}$ [37]; however, those are still straight. The smallest reported 3-d MPS is about 500 nm pitch [38].

3.3. Surface treatment and functionalization

After the MPS layer is etched, several post-processing steps can be applied to the device. This may be of particular importance for MPS fabricated using EE. This is because the electrochemical process leaves a thin microporous silicon layer on the pores' walls. The thickness and roughness of this microporous layer will depend on the electrolyte composition and concentration, as well as on the substrate resistivity and applied potential [32] (see **Figure 7a**). A simple way to remove this layer is to perform a short thermal oxidation of the MPS structure. The microporous layer will readily oxidize [39]. After the oxidation step, the oxidized PS layer can be removed by dipping the MPS structure in an HF solution, leaving a very smooth and defect free surface on the walls of the pores. The so-prepared surface can be further processed, for instance to create high-quality oxide layers, as seen in **Figure 7b**.

This oxidation-oxide removal cycle can be repeated several times in order to create enlarged, cylindrical pores.[7] This is useful when creating 3-d MPS structures and strong modulation is desired, such as pores interconnecting with each other at specific points and resulting in an opal-like structure (see **Figure 8**). The pore shape can be further altered by etching the freshly fabricated MPS structure in diluted wet chemical etchants such as KOH or TMAH. This allows obtaining flat faces that are not possible from PECE alone [40].

[7]The actual pore cross-sectional shape obtained with EE is not perfectly cylindrical and depends on potential applied and other factors [19].

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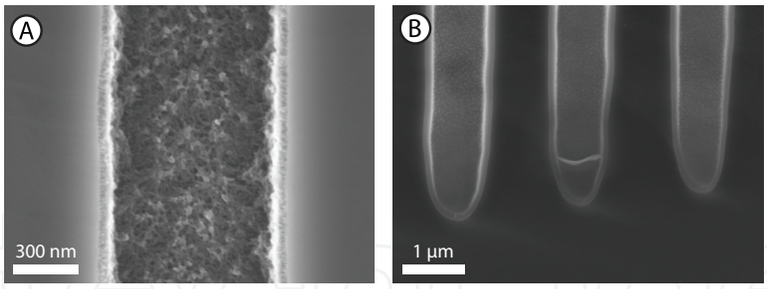

Figure 7. Detail of the pore surface of a MPS structure fabricated by EE. (A) shows a freshly etched pore revealing a layer of microporous silicon in the walls. After oxidizing, stripping and further oxidizing, a much smoother, microporous-free surface is seen in (B).

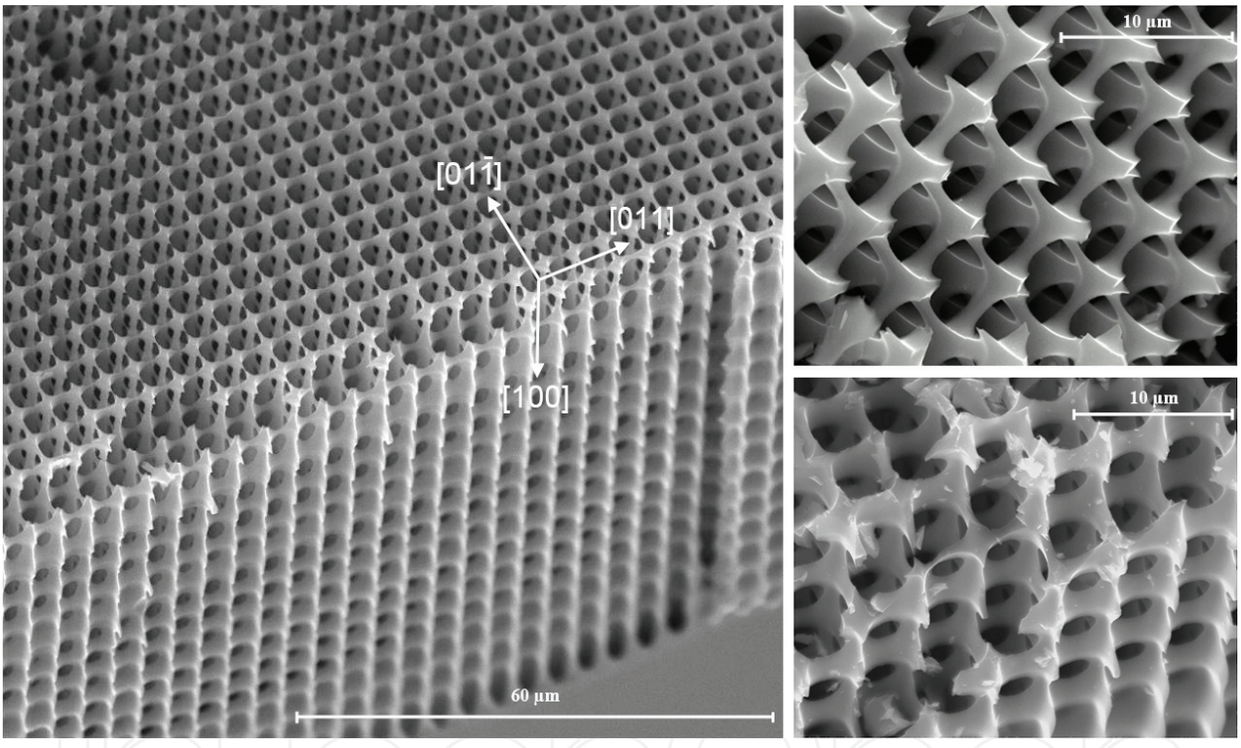

Figure 8. Bird's-eye views of the 3-d MPS modulated pores and subsequent widening of the pores. Reprinted from [23], Copyright 2008, with permission from Elsevier.

3.3.1. Functionalization

The increased available surface in MPS has been of interest for sensors. To improve the adsorption of species on the surface or the sensitivity of the device, several surface functionalization approaches have been proposed. For instance, carbonization of the PS structure helps in passivating and stabilizing the porous layer better than oxidation [41] or to avoid oxidation altogether. This is of particular interest for photoluminescence applications [41] and humidity sensors [42]. Other surface treatments have been proposed depending on the application. For example, using the atomic-layer deposition (ALD) method, it is possible to cover the walls of a MPS structure conformally with materials such as alumina (Al_2O_3),

titania (TiO_2) or tantalum oxide (Ta_2O_5), which have applications in sensing devices [43] and electronic devices [44]. Other surface treatments of great interest for energy applications or chemical reactors are the deposition of nanoporous materials like zeolites [45] and catalysts like cobalt, platinum or palladium [12, 16].

3.4. Porous membranes

Certain applications require the passage or filtering of a fluid. Other applications seek that the passing fluids undergo certain chemical reactions. In either case, having a very large surface is beneficial. The main advantages are the fast mass and heat transfer, the short diffusion length and pressure drop, and the precise control of the process, resulting in higher product yields (for chemical reactors) and increased efficiency [16]. For this application, MPS has been proposed as a better alternative to common monoliths used in catalysis [12]. MPS membranes have also been suggested as ratchets [46] for physically selecting particles. Membranes have also been found useful for microfluidics [17] and for electrodeposition inside the pores.

The fabrication of the MPS membranes can be done by dissolving the remaining silicon bulk on the backside after the electrochemical etching of the pores. A common technique is to use alkaline anisotropic etchants typical in MEMS processing [47]: potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH). The membrane is formed when the removed silicon reaches the pore tips. When performing such process, it is necessary to protect the porous volume, as it will etch much faster than the silicon bulk. Furthermore, it may be interesting to selectively etch the MPS structure to reveal only part of the pores. For this reason, first a protective layer must be prepared on the structure surface. This can be accomplished by oxidation of the MPS sample. This protective layer must have a minimum thickness: the dissolution process is not perfectly uniform, leaving a roughened surface [48]. Therefore, in some places, the pore tips will be uncovered earlier. The protective layer must be thick enough to withstand until the full membrane is finished, otherwise the etchant will leak and rapidly dissolve the porous volume.

This process has to be carefully monitored to avoid overetching and the destruction of the protective layer. In this regard, TMAH has a greater Si-SiO_2 selectivity [47], therefore making this process more robust. The actual method employed for the membrane fabrication will ultimately depend on any further processing and application of the MPS device. In particular, KOH may not be suitable if there are posterior high-temperature steps or the process flow has to be CMOS compatible.

3.4.1. In situ

As an alternative to alkaline etching of silicon, there is the possibility to create the membrane during the electrochemical pore growth phase. Two approaches are possible: entering the electropolishing regime during EE [49], and creating a sacrificial PS layer at the bottom [50]. The latter approach has been successfully applied for MEMS devices where the sacrificial micro-PS is formed underneath the actual device, such as cantilevers [51],

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thermal actuators [52] or sensing devices [53]. After the micro-PS is formed, the devices are released by dissolving this porous volume [50]. This can be done with a sufficiently diluted etchant or with plasma. Alternatively, one can oxidize the PS and then remove the oxide by an HF dip [50, 54]. This method can be also applied to MPS structures by a double-layer technique: first etching the macroporous volume and afterwards evolving the micro-PS beneath the macropores [54]. This may require changing the HF solution between etching phases.

The fabrication of an in situ membrane using the electropolishing regime is very similar to the sacrificial method. As in the previous method, it can be applied for both micro-PS and MPS. In this case, only the current density (and potential if necessary) is increased above the j_{PS} threshold [55]. This will promote the electropolishing of silicon at the pore tip depth and can be performed for an extended period of time to completely detach the MPS membrane from the Si substrate [49] (see **Figure 9**). For very high AR structures, it is important to take into account the acid concentration and the diffusion of reactants at the pore ends [2].

3.5. Pore filling

Conformal coating of the high AR structures present in MPS is often straightforward. Several techniques common in microfabrication are available for the task (e.g. ALD) [56]. However, the complete filling of such structures can be more difficult. Such methods can be very slow to fully fill the pore volume or have conformality issues for very thick depositions. An alternative method to fill the pores is to use either *electroless deposition* or *electrodeposition* (also *electroplating*). These methods are also common in MEMS [56] and CMOS microfabrication for the metallization layers of VLSI circuits [57].

Electroless deposition and electrodeposition are commonly used to deposit metals, though these processes are not limited to those materials. Copper is typically used in VLSI

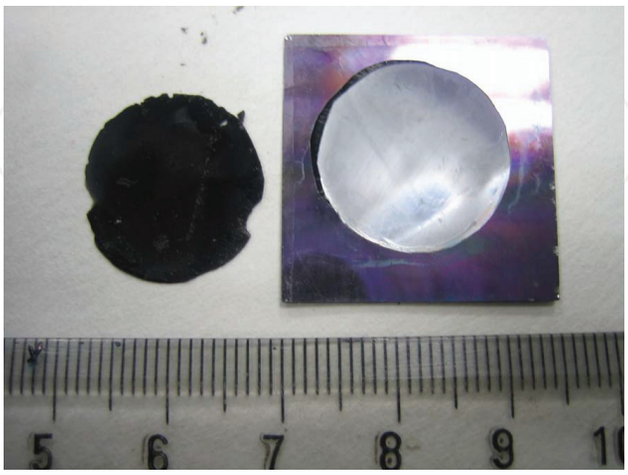

Figure 9. MPS membrane fabricated with in situ electropolishing. The black surface corresponds to the backside of the detached membrane; at the right is the supporting silicon substrate where the MPS was etched. © 2008 IEEE. Reprinted, with permission, from [49].

microfabrication. However, Cu easily diffuses through SiO_2 and Si [58], and it has poor adhesion to dielectrics like SiO_2. Noble metals can also be deposited by these means, for example gold; however, this would result in exceptionally expensive devices as the total volume of a MPS structure is large. Some good candidates for pore filling are nickel and aluminium. Aluminium plating would be the preferred material for an industrial process; however, Al plating is more complex (non-aqueous solution [59]) and has higher safety risks (inflammable or explosive products). On the other hand, nickel plating is simple and well known in industry, both electroless and electrodeposition. A MPS structure can be directly plated without further processing: Ni will deposit along the walls of the pores and exposed surface. However, for high AR pores, the deposition can be non-uniform, resulting in early pore closing and leaving voids inside the filling [57]. A way to avoid such issues is to use MPS membranes. Open membranes allow the passage of the electrolyte, thus reducing concentration gradients. Electrode size and electrolyte are also important for uniformity of the deposition.

Focusing in Ni electroplating, a typical plating bath is a dissolution of nickel sulphamate, nickel chloride and boric acid for pH correction. This plating solution is used at about 55°C. The resulting surface is a smooth, matte finish deposit. In particular, in the work of Vega et al. [18], this technique was used to fill MPS membranes as seen in **Figure 10**. The membranes were initially oxidized, and a metal evaporation was performed on one of the sides (the front face was used due to the better, smooth, surface). The so-prepared membrane was contacted on the metal face and afterwards insulated to avoid deposition on this face. The sample was submerged in the plating solution with the free face looking the counterelectrode, and the plating was performed at a mean current of 30 mA/cm^2. Deposition speed varied linearly with current, but the open surface (total pore area) determined the actual speed and had to be calibrated for each different MPS structure. The electrodeposits can be performed both with DC current and with pulsed current. As the silicon structure is protected by an insulating layer of silicon dioxide, Ni only deposits on the advancing Ni front inside the pores. This results in a smooth and void-free pore filling as seen in **Figure 10**.

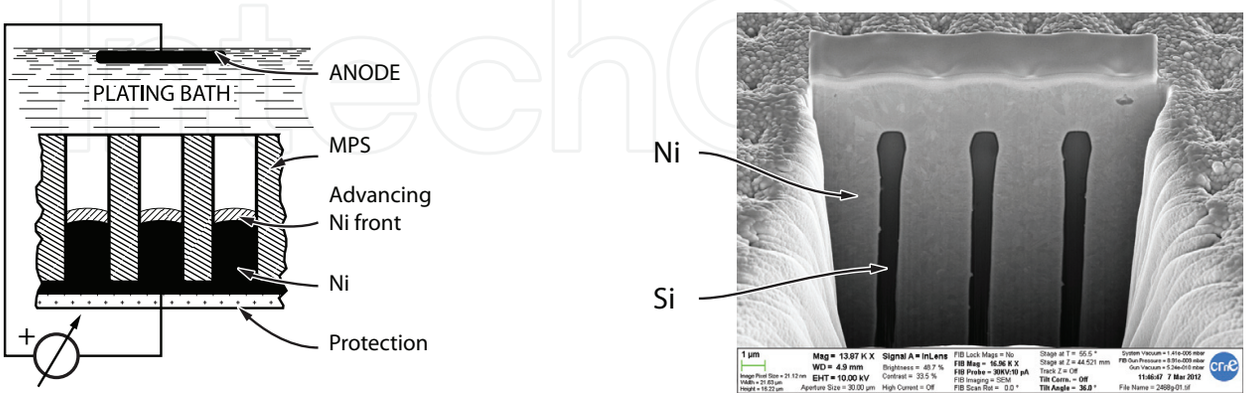

Figure 10. SEM micrograph of a macroporous silicon membrane filled with nickel. The left panel shows schematically the deposition on Ni inside the pores. To the right, a SEM image of a filled MPS structure is cut using FIB milling to expose the interior of the membrane; a platinum layer is used to aid the milling procedure. It can be seen that nickel fully covers the pore interior as well as the surface of the sample.

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4. Applications of macroporous silicon

In this section, a brief description of a selection of the non-photonic applications of MPS will be presented. In particular, applications in the electronic devices and MEMS fields will be examined. However, bear in mind that MPS can be applied to a very broad range of fields, only some applications can be introduced here.

4.1. Field effect transistors

Power applications either demand operating at high voltages, high currents or both. In power MOS-FET devices, the gate oxide thickness determines the maximum potential the transistor can withstand (in the absence of a drift region). However, thick oxides will increase the threshold voltage, V_{th}. Furthermore, MOS transistors have a negative thermal coefficient, therefore for high currents, on-resistance, R_{ON}, will increase and thus limit the maximum current. In this situation, a large number of devices connected in parallel may be necessary to handle the demanded current density.

In these circumstances, power MOS structures evolved to *trench transistors* in the early 1990s and to the *superjunction* (SJ) *devices* [60] in mid-1990s. The outcome is a device with a much reduced R_{ON}. A summary of the vertical trench device structures is shown in **Figure 11**. Having millions of 'micro transistors', each one will handle a tiny amount of the requested current. As seen from **Figure 11**, the construction of these devices is fairly complex, requiring many steps and masks.

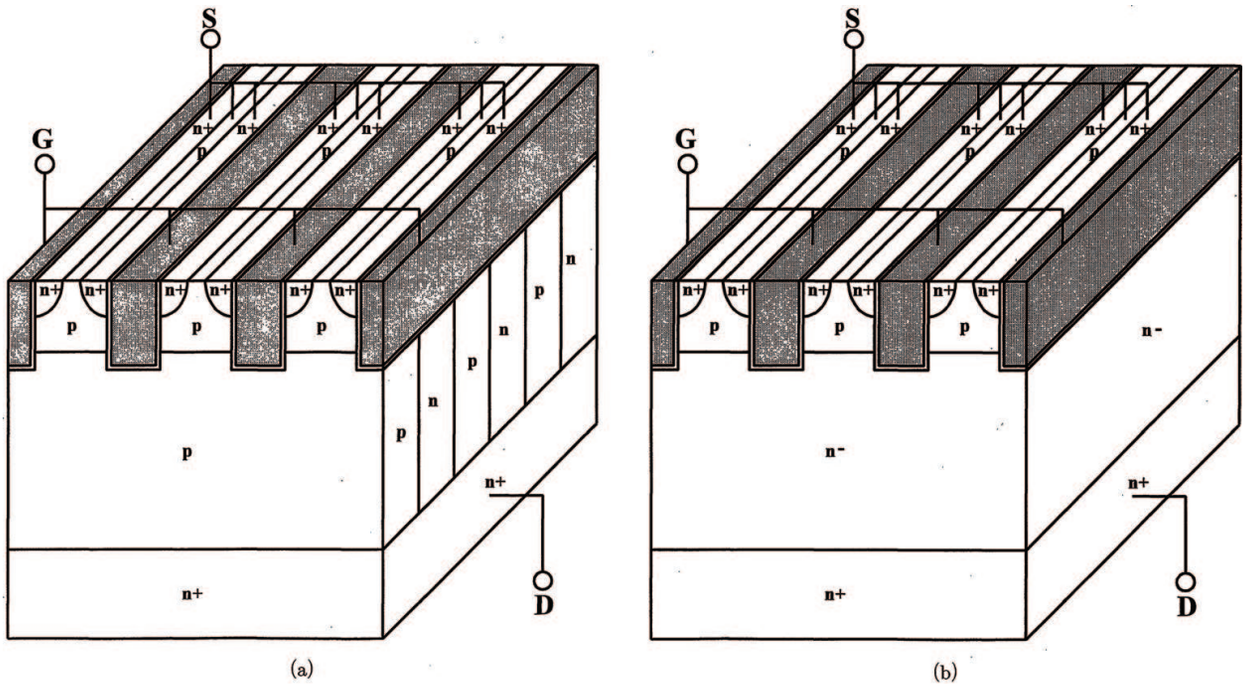

Figure 11. Structure of vertical MOS-FETs, (a) n-channel, trench gate and (b) conventional. Copyright 1997 The Japan Society of Applied Physics, from [60].

MPS provides an alternative to simplify the fabrication of trench FET transistors. Basically, the aim is to take advantage of the ease to obtain a large number of pores or trenches. EE of silicon provides a material with a controllable density of pores, which can be arranged freely (under certain constraints), and with a profile, which can be further adjusted to meet the device performance goals. The pores can subsequently be coated or filled by appropriate means (e.g. chemical vapor deposition (CVD) or thermal oxidation) to make either the gate or the channel of the device. Overall, the obtained structure is simpler and easier to fabricate, thanks to the reduced number of processing steps required. In Ref. [6], the suitability of such MPS structures was studied theoretically.

According to the definition of the channel region, two kinds of devices can be distinguished: vertical structures are those whose channel corresponds to the pore volume, while the gate is formed by the MPS surrounding material; and horizontal devices are those with the roles reversed, that is the channel is the MPS bulk material, while the pore volume constitutes the gate. Thus, carrier flow takes place in the pores for the vertical devices and through the MPS substrate for the horizontal devices.

Using ordered MPS, some of the proposed FET have the configurations shown in **Figure 12**: vertical J-FET and MOS-FET, and horizontal J-FET and insulated gate (IG) J-FET.[8] Using a square lattice with a pitch of 4 μm, a density of over 10 million unit devices per cm^2 is achieved. MPS of the given feature size fabricated using the PECE technique employs low-doped silicon substrates. In particular, n-type, phosphorous doped, $\rho = 3\ \Omega$ cm, ⟨100⟩ oriented wafers are suitable for the above case. For the vertical devices, where the MPS substrate acts as the gate, this is not a limiting factor. However, for the horizontal operating devices, this is indeed an issue. To overcome this drawback, a doping of the as-etched MPS must be performed. Furthermore, removing the microporous layer after EE to get a smooth, defect-free, surface will slightly widen the pores. This must be taken into account when designing the

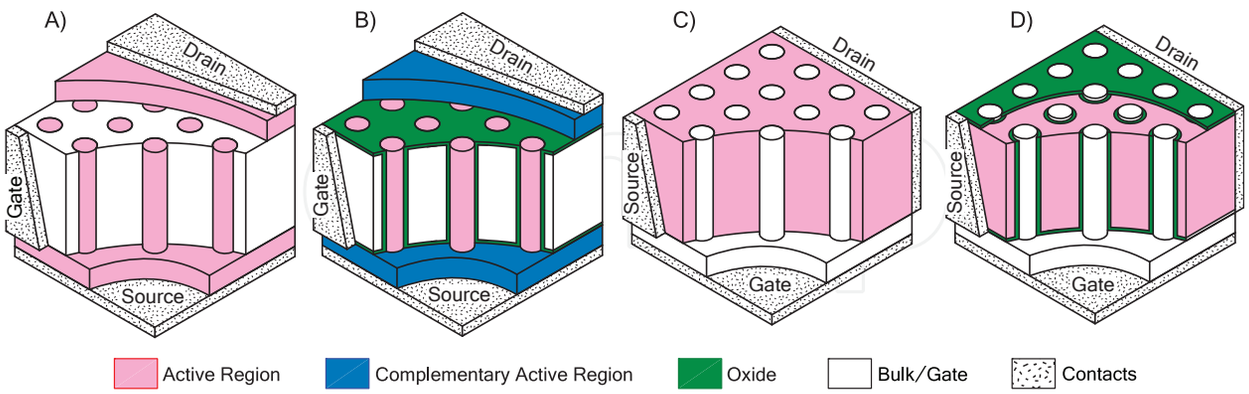

Figure 12. Breakout view of the proposed devices. For vertical structures (J-FET [a] and MOS-FET [b]), the channel corresponds to the pores, while for horizontal structures (J-FET [C] and IG J-FET [D]), the channel is the bulk porous silicon. © 2011 IEEE. Reprinted, with permission, from [6].

[8] As will be shown, it can operate with both positive and negative V_{GS}, and thus is also referred as *enhanced J-FET*.

devices. For the MOS or IG devices, a thin layer of insulating material, such as silicon oxide, can be deposited or thermally grown on the pores' walls.

After preparing the MPS supporting structure, the pores are filled. For the vertical structures, a CVD process may be performed to fill the pores with a semiconductor, such as silicon, of the desired doping. In contrast, for the horizontal ones, this step is not as critical. To form the gate, one can either choose a CVD process to coat with a relatively thin film of conducting or semiconducting material, or, alternatively, use an electrodeposition method, such as the one described in section *pore filling* to fill the pores with a metal.

From the work in Ref. [6], it can be seen that the overall specific on-resistance, R_{ON}, is comparable to that of more complex trench and SJ devices. It can be noticed that J-FET devices have larger $R_{ON,}$ but this is to be expected as it solely depends on the channel resistivity, whereas MOS devices operate in strong inversion. Reducing the drift region (particularly for J-FET devices) and exploring alternative pore profiles may help in reducing R_{ON}. Regarding the breakdown voltage V_{br} of the devices, it was found that for all of them it was around 40 V. The electric field distribution revealed that this was caused mainly by the sharp edges found near the gate-drain region. The obtained V_{br} results are similar to those other found in literature (with no drift region for high-voltage operation). Nevertheless, a higher breakdown voltage can be obtained by adding a drift region and physically separating the gate from the drain, at the cost of a more complex fabrication process.

A summary of the device characteristics from Ref. [6] is given in **Table 1**. One of the most notable characteristics is the large current densities that these devices can handle. For instance,[9] the vertical J-FET from Ref. [6] is able to handle near 600 A/cm^2. In general, the performance of the proposed devices is comparable to that of more complex trench FETs. Finally, for the IG device, two things stand out: when operating in *enhancement mode* ($V_{GS} > 0\ V$), the transfer function is surprisingly linear, and that achieving complete turn-off of the device may require large potentials.

Regarding the small signal behaviour of the devices, the obtained results show that individual cell devices have moderate capacitance. Though these devices may be unsuitable for their use in signal applications, they are satisfactory for fast switching of loads in power applications.

4.2. Supercapacitors

MPS has also been shown to be applicable for energy storage since the beginnings of its research, see, for example, the work by Lehmann [61] or IBM [62]. The purpose of using MPS for capacitors is twofold: on one hand, there is the need of large capacitance devices for energy storage [10]; on the other hand, there is a drive towards higher integration, be it for cost and space savings or for efficiency reasons [63].

To fabricate high-capacity devices using MPS, one takes advantage of the greatly enlarged available surface area. Basically, there are few ways to increase capacity: electrochemical means (Helmholtz double layer or chemical energy storage[10]), decrease plate separation,

[9]The current density is calculated over the cross section of the channel.

[10]The former case would apply to capacitors, while the latter case would be for batteries.

		Vertical		Horizontal		
		J-FET	**MOS-FET**	**J-FET**	**IG J-FET**	
Specific on-resistance	R_{ON}	5.1	0.67	0.74	0.074	mΩ cm^2
Gate bias*	V_{GS}	0	10	0	10	V
Transconductance gain	g_m	16.6	70.6	616.7	875.0	μS
Pinch-off/threshold Voltage	V_{po} or V_{th}	−3.21	0.45	−3.8	−3.5	V
Input gate capacitance	C_G	11.6	40.0	17.4†	70.0†	fF
Gate oxide thickness	t_{ox}	–	100	–	100	nm
Pore diameter	d_{pore}	2	2	3	3.6	μm

These results correspond to: channel doping is 10^{-18} cm^{-3}.
Gate doping is 10^{-16} cm^{-3}.
Pore length $l_{pore} = 20$ μm.
Drain-source potential was set to $V_{DS} = 8$ V for parameter determination.
*Value used for parameter determination.
†The given values are for a single cell and may not scale linearly.

Table 1. Transistor characteristics summary for a single pore device, from Ref. [6].

increase the plate surface, increase the dielectric constant or a combination of the former. E*lectrolytic capacitors* (ELCs) and EDLCs are based on the double layer effect,[11] while *electrostatic capacitors* (ESCs) rely only on charge accumulation. In particular, ELCs are capable of offering moderate-to-large capacity densities. ESCs, on the other hand, are capable of larger power densities and have a lower ESR (thus a higher operating frequency) [64]. To improve capacity, ESCs rely on choosing materials with high dielectric constant, reducing the dielectric thickness and extending the surface of the capacitor. Two types of dielectrics can be distinguished: class 1 or direct/paraelectric, and class 2 or ferroelectric [65]. Ferroelectric materials have very large dielectric constants but are sensitive to electric field and to ambient conditions (humidity and temperature) [66]. On the other hand, paraelectric materials have lower dielectric constant but are more stable. Some class 1 dielectrics are silicon dioxide and other materials frequently used in semiconductor industry for gate insulator such as alumina (Al_2O_3), silicon nitride (Si_3N_4) or high-*k* materials [67]. Though using high-*k* materials seems the most obvious solution, it has to be considered that they also have lower breakdown electric field (E_{bd}) and larger leakage; thus, complex insulator layer stacks [68] may be needed to achieve the desired performance.

Having a thinner insulating layer between the capacitor plates will help increase the capacitance of the device. However, care must be exercised as leakage currents will increase substantially due to direct tunnelling for thin insulators [68]. Furthermore, a thinner insulating layer will also affect the maximum operating voltage. Finally, to maximize capacitance, the effective

[11]Modern implementations of such capacitors having *activated carbon* as electrodes offer large gains in capacity density and are referred as *electric double-layer capacitors* (EDLCs), *ultracapacitors* and commercially as *supercapacitors*.

plate area can be extended without increasing the footprint of the device. To achieve such goal, advanced devices have intricate surface shapes that extend into the volume of the capacitor plates [18, 61, 62, 69].

The use of PS in its various forms for high-value capacitor devices can be traced back to the early development of PS. MPS was first suggested for its use as capacitors with the work from Lehmann [61], and since then, the industry has shown interest in the research and development of high-value capacitors based on this material [61, 70]. The techniques used to build the MPS structures of the capacitors have been both PECE [61, 71] and RIE [70, 71]. The pores of MPS give an enlarged surface to create the plates of the capacitor device. Pores may be arranged randomly or in a pattern. Random MPS is simpler to fabricate, and capacitor devices with $C_{sp} = 4$ nF/mm^2 have been reported in Ref. [69]. However, using random MPS will result in uneven current distribution, and sharp edges where the electric field will concentrate and possibly break the dielectric. Furthermore, if the devices are to be defined in specific zones, a mask is needed nonetheless, so not using a patterned pore array is less justified. The use of ordered MPS requires a more complex fabrication flow; however, it has the advantage of being well defined, so final capacitance can be accurately calculated and obtained, plus giving control over the actual shape of the pores.

MPS-based capacitors use the porous substrate as one of the plates, so the other electrode must be deposited over the substrate. Plates can be arranged in several ways. For instance, it is possible to deposit a single layer to create a two-plate capacitor [18, 69], or to use a multiple layer approach, stacking several dielectric-conductor coatings to create a MIM-like capacitor. In the work by Klootwijk [70], the MIMIMIM stack depicted in **Figure 13** results in a very large capacitance density device, with a specific capacitance $C_{sp} = 440$ nF/mm^2 [70]. However, its performance is lower than expected, see **Table 2**. Using multilayer stacking greatly complicates the fabrication process, so the simpler approach of a two-plate capacitor may be desirable. In **Table 2**, a summary of the state-of-the-art supercapacitors based on MPS is given.

4.2.1. Fabrication

Once the MPS is etched, it may be necessary to perform a doping of the porous substrate. This is especially necessary in case of EE MPS as the Si substrate used has 'low' doping concentrations as seen in section *Electrochemical Etching*. In particular, for a 4 μm pitch MPS structure, an n-type phosphorous doping of 1.5×10^{16} cm^{-3} is used in Ref. [18]. To improve ESR, a degenerate n^{++} layer deep enough is diffused surrounding all of the porous area. Additionally, a porous membrane can be formed as described in section *Porous Membranes*. This step can be done after the doping step, though it is preferably done before it to better control the doping of the MPS structure.

A common issue found in such large surface capacitors is the elevated leakage currents,[12] as seen in **Table 2**. To keep them at reasonable levels is mandatory to have a very high quality insulating layer. The predominantly used insulating materials have been those common in CMOS: SiO_2, Si_3N_4, and Al_2O_3. Thicknesses used have been around 10 nm to 50 nm. However, most works noted a larger than expected leakage, and this has been primarily attributed to the

[12]Leakage current density is calculated considering the footprint area of the device.

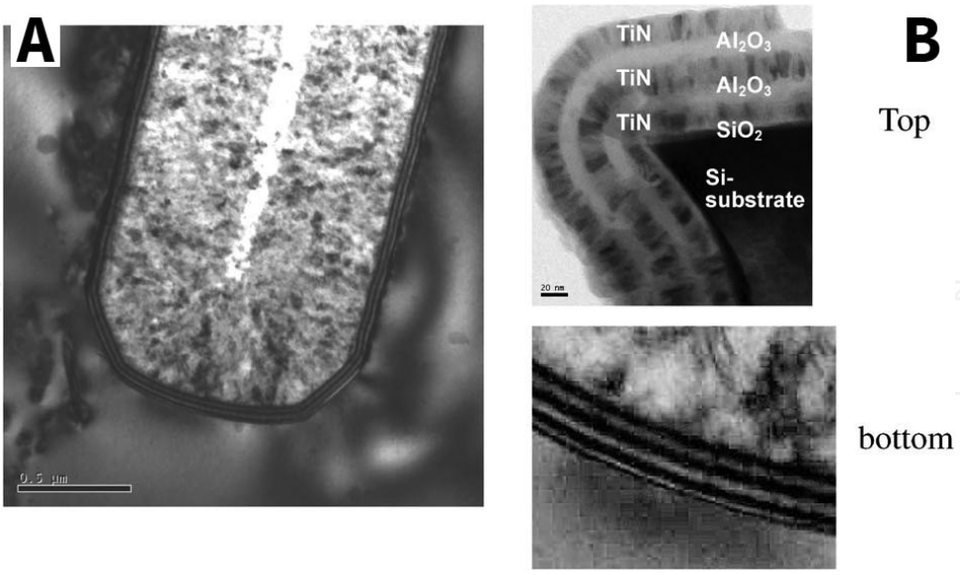

Figure 13. Cross-sectional TEM view for MIM-type MPS supercapacitors. (a) shows an overview of the capacitor MIM stack at the bottom of the pore. In (b), a detail view of the top and bottom of the pore is shown. © 2008 IEEE. Reprinted, with permission, from [70].

Refs.	Method	Configuration	Depth (μm)	Density (pore/μm^2)	Specific capacitance C_{sp} (nF/mm^2)	Breakdown voltage V_{br} (V)	ESR (Ω)	Leakage I_{leak} (mA/cm^2)
[71]	EE	ONO/polySi	100	0.094	100	–	0.1	–
[72]	RIE	SiO_2/TaN	0.1	721.69	31.3	–[†]	–	1 @ 1V
[44]	EE	Al_2O_3/ZnO : Al	50	0.16	25	~8[*]	–	1.5 @ 2.5V
[70]	DRIE	$SiO_2/[TiN/Al_2O_3]_3$	30	–	440	6	10	1 @ 3V
[73]	EE	ON/polySi	72	1	700	8	20	1 @ 3V
[18]	EE	SiO_2/Ni	130	0.0625	110	20	1.1	$\ll$0.001@ 1V

[*]Not reported but inferred from **Figure 4**.
[†]From **Figure 3**, the reported device should be able to operate in the ±3 V range.

Table 2. MPS supercapacitors state of the art. Best figures reported.

increased E field strength in the curved regions (tip and edges) of the pores. To achieve the remarkably low leakage current in [18], the authors note that especial care of surface cleanliness was needed; also after the membrane opening and substrate doping, it was found best no to completely fill the pores.

After the dielectric layer is placed, the pores are filled to define the other plate. This can be done with nickel following the procedures described in section *pore filling*. The use of a metal electrode helps in achieving a very low ESR for the final device. The fabrication process flow is schematically depicted in **Figure 14**.

Electrical characterization of the devices can be approximated by a simple RC model. As the main contributor to capacitance is due to the cylindrical pores, the capacitance value can be predicted by the formula of the cylindrical capacitor $C_{\text{unit}} = 2\pi\varepsilon_0\varepsilon_r l_{fill}/\ln(1 + t_{ox}/r_{pore})$. As seen from **Figure 15**, the simple RC model is reasonable at low frequencies; however, the capacity is shown to be not ideal and is presumed to be due to relaxation in the dielectric interfaces [74].

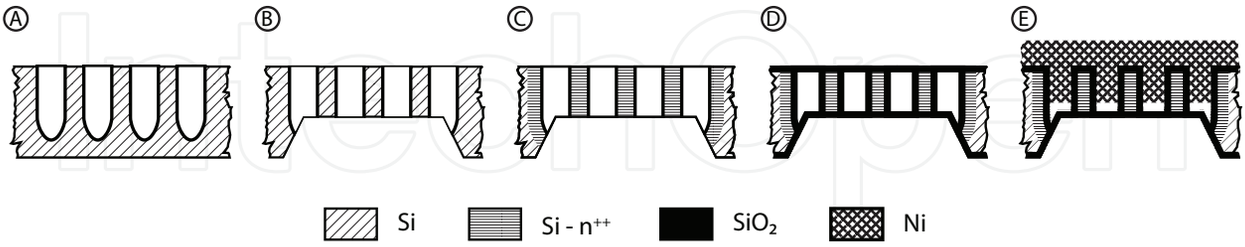

Figure 14. Fabrication flow for the capacitor described in Ref. [18]. (a) Etching of the pores, (b) membrane opening, (c) substrate doping, (d) thermal SiO_2 layer growth and (e) pore filling and electrode connection.

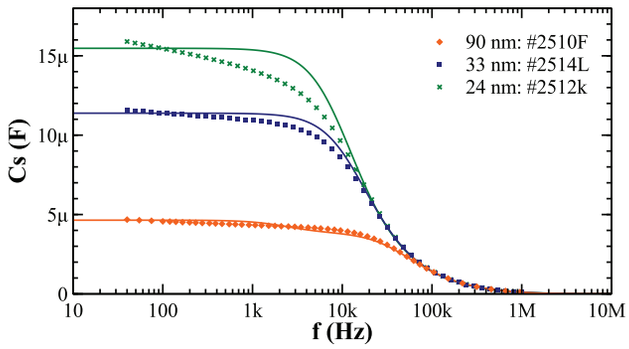

Figure 15. Series capacitance (symbols) and the fitted RC model (solid line) for the MPS capacitors of [18]. © 2014 IEEE. Reprinted, with permission, from [18].

4.3. Through silicon vias

Nowadays, the microelectronics industry is highly interested in 3-d (monolithic) integration looking for improvements in package integration, the reduction of interconnect delays, cost savings and system scaling [75]. Among the different technological options, through silicon vias (TSVs) and silicon interposers have been shown to be an enabling technology that has recently reached the consumer market in the form of ultra-high-density memory modules [76]. The most common method for TSV fabrication found in the literature is RIE etching of the silicon to create the vias, then pore filling with copper by a dual damascene process, surface planarization, and pad definition (and repeat the process for the other side) [75]. Pore surface roughness may impose certain complications when filling the pores [77], as well as pore shape has an impact on reliability by thermal cycling [77].

EE MPS may offer a simplified approach to TSV fabrication. The pore shape is easily controlled by the current waveform, and deep pores are effortlessly etched. The obtained surfaces can be made smooth by a short oxidation and oxide stripping (see *Surface treatment and functionalization*),

and pores can be easily filled. An example of MPS for TSVs can be found in the work by Defforge [78].

4.4. Microneedles

For biomedical applications, microfabrication of miniaturized complete analysis platforms (lab-on-a-chip) is being vigorously researched [79]. In particular, the extraction and injection of fluids to tissues are of great interest. Microneedles provide a way to simplify this procedure while minimizing some nuisances like pain [80] or risk of infection, being minimally invasive[13] [80]. Microneedles have been reported of several materials and features, as well as fabrication methods [80]. MPS has also been shown to be suitable to be used in such applications. Furthermore, MPS-based microneedles have shown distinct advantages over 'conventional' ones, like smaller diameter and higher density, and foremost a simpler fabrication process.

The first reference to MPS fabricated by EE applied for microneedles is found in the work by Rodríguez et al. [17] and Rajaraman [81]. In Rodriguez et al. work, MPS is used to create arrays of SiO_2 microneedles with diameters ranging from 2 to 5 μm, up to 140 μm in length, and wall thickness about 100 nm. The process and results obtained are shown in **Figure 16**. The fabrication process consists of creating a MPS membrane, and once the pore tips are exposed, remove them by a rapid dip in HF (see **Figure 16c**). To create the needles, the membrane is further processed in TMAH to remove silicon from the backside (see **Figure 16d**). At this stage, the microneedles are prepared and just remain attaching the fluid handling fixtures. Rajaraman's work is essentially identical, though a slightly more complex process is described, as needles are formed in the front face.

A similar approach is followed by Barillaro and his group [82]. In this case, instead of forming the needles by removing silicon from the backside, they use the back-face

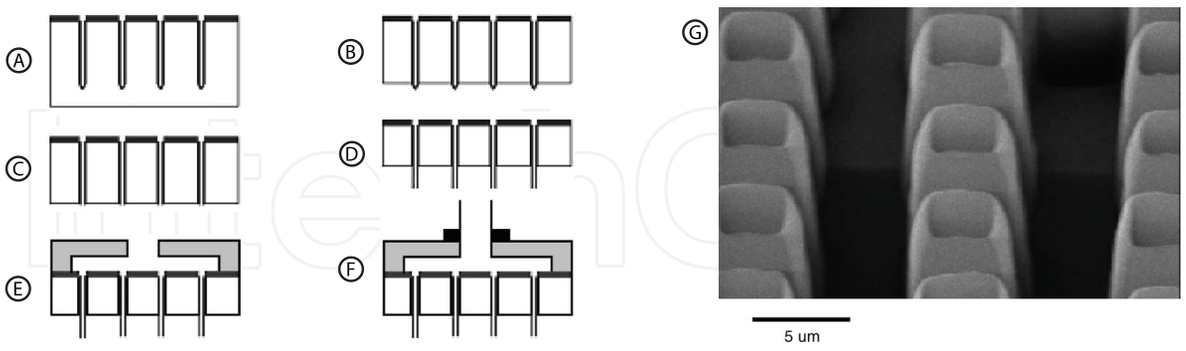

Figure 16. Silicon dioxide microneedles fabricated from MPS. From the starting MPS in (A), a membrane is done (B) and the oxidized pore tips are etched in HF to open the membrane (C). The membrane is further processed by removing silicon from the backside with TMAH (D) and revealing the SiO_2 microneedles. A reservoir is glued to the prepared device (E) and a tube for fluid delivery can be attached (F). In (G), a close-up of the needles tip is shown. Adapted from [17], Copyright 2005, with permission from Elsevier.

[13]Microneedles are short and only penetrate the epidermis [91], avoiding the dermis where nerve terminations are located.

membrane cavity to create a reservoir and subsequently etch the frontside to create the needles. Furthermore, Barillaro et al. conducted skin penetration tests showing that 1 μm wall thick can withstand repeated skin insertion without breaking. Other studies confirm these findings and show that SiO_2 microneedles require less force for effective penetration [83].

Besides hollow microneedles as the ones previously described, MPS has also been used to create high AR SiO_2 pillars [84]. Basically, the fabrication process is the same as for the microneedles, described earlier (see **Figure 16**), but stops after the membrane creation. The released pillars can be further used for sensing applications, drug delivery by coating the pillars [80], skin pre-perforation [80] or microreactors [45].

Microneedles can also be applied to other uses in addition to biomedicine. For example, for inkjet printing [85], micronozzles have been shown to be able to print extremely fine detail lines.

4.5. Other MEMS devices

MPS technology can be adapted for the fabrication of complex shapes and structures with uses in other MEMS applications. For example, EE micromachining has been proposed as way for fabrication of embedded heat sinks [86]. The idea is to create a free-standing MPS structure by in situ membrane etching and later filling the porosified volume with copper by electrodeposition. Thanks to the higher thermal conductivity of Cu, higher efficiency in thermal dissipation can be achieved for dense VLSI circuits.

However, it is in microfluidics and lab-on-chip applications that MPS is most interesting. Pore diameter can be modulated and adjusted for filtering applications [46, 54], such that using the appropriate pore size one can selectively allow the passage of particles or biological species. Furthermore, the device can easily be protected against harsh environments by oxidation or other surface treatment. Particular mention must be made to the work of Barillaro's group [22]. Some outstanding examples are a capillarity-driven (self-powered) microfluidic system based on MPS [87] and a MPS microstructures for label-free optical detection of cells [88].

6. Conclusion

This review has shown several applications of macroporous silicon to a wide range of fields, besides the optical and photonic, that are also of utmost relevance. In particular, it has been shown that MPS has many uses the fabrication of electronic devices, such as in energy storage (supercapacitors). Other important areas of application of MPS are microfluidics and lab-on-a-chip, where the freedom in structure micromachining allows creating complex structures capable of being integrated in a complete sensing platform. The use of MPS has helped to improve existing devices and has allowed to develop new ones. Also, MPS has been applied in MEMS device fabrication. The applications of MPS represent a vast field that is still in active development.

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