Sérgio Carlos da Conceição Pires

Arquitecturas de Transmissores Sem Fios Reconfiguráveis e Multi-Protocolo

Multi-Standard Reconfigurable Wireless Transmitter Architectures

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Tese apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Doutor em Engenharia Electrotécnica, realizada sob a orientação científica do Professor Doutor José Carlos Pedro, Professor Catedrático do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro e sob a coorientação científica do Professor Doutor Pedro Miguel Cabral, Professor Auxiliar do Departamento de Electrónica, Telecomunicações e Informática da Universidade de Aveiro.

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Para a Sandra, Matilde e Gustavo.

"If we knew what it was we were doing,
it would not be called research, would it?"
Albert Einstein

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palavras-chave

Modulação em amplitude, transmissor de portada pulsada, filtros de cavidade, modulação em fase, amplificador de potência, modulador de largura de pulsos, modulador sigma-delta, amplificador de potência comutado.

resumo

A constante exigência por sistemas de transmissão sem fios altamente eficientes, tem fomentado o interesse em técnicas comutadas aplicadas à necessária amplificação em potência. O transmissor de RF com a portadora pulsada em amplitude, ou seja, um transmissor sem fios em que a portadora modulada em fase é comutada em amplitude em modo activo e inactivo, de acordo com uma determinada conversão amplitude-tempo, tal como as modulações de largura de pulsos ou sigma-delta, constitui uma arquitectura promissora capaz de transmitir eficientemente sinais com modulações complexas altamente exigentes. No entanto, os testes das implementações práticas apresentam resultados que ficam muito aquém das promessas teóricas (linearidade e eficiência perfeitas).

Esta tese apresenta, como contributo original para o conhecimento, o primeiro estudo aprofundado e respectivo modelo das características de eficiência e linearidade que podem ser conseguidas com esta arquitectura. A análise começa com uma breve descrição do comportamento teórico idealizado destes sistemas de amplificação comutados, seguido do estudo das muitas fontes de imperfeições que surgem na implementação real. Em particular, é dada uma especial atenção à modulação de carga causada pela interacção, frequentemente ignorada, entre o filtro de banda estreita de reconstrução e o amplificador comutado, que, de entre os vários problemas adicionais que afectam o seu desempenho, força uma implementação com dois transístores. O desempenho desta arquitectura é perfeitamente explicado como base na teoria apresentada, suportada por simulações e respectivos resultados das medidas efectuadas com uma implementação prática plenamente funcional. A partir das conclusões retiradas é formulado um conjunto de recomendações que permitem melhorar desenhos futuros, um dos quais proposto e verificado nesta tese. É sugerida uma importante modificação à arquitectura tradicional, onde a portadora modulada em fase está sempre activa - permitindo uma implementação com um transístor único - e a amplitude é impressa na fase da portadora de acordo com um código bi-fásico.

keywords

Amplitude modulation, carrier-burst transmitter, cavity filters phase modulation, power amplifier, pulse-width modulator, sigma delta modulator, switched-mode power amplifier.

abstract

The continuous demand for highly efficient wireless transmitter systems has triggered an increased interest in switching mode techniques to handle the required power amplification. The RF carrier amplitude-burst transmitter, i.e. a wireless transmitter chain where a phase-modulated carrier is modulated in amplitude in an on-off mode, according to some prescribed envelope-to-time conversion, such as pulse-width or sigma-delta modulation, constitutes a promising architecture capable of efficiently transmitting signals of highly demanding complex modulation schemes. However, the tested practical implementations present results that are way behind the theoretically advanced promises (perfect linearity and efficiency).

My original contribution to knowledge presented in this thesis is the first thorough study and model of the power efficiency and linearity characteristics that can be actually achieved with this architecture. The analysis starts with a brief revision of the theoretical idealized behavior of these switched-mode amplifier systems, followed by the study of the many sources of impairments that appear when the real system is implemented. In particular, a special attention is paid to the dynamic load modulation caused by the often ignored interaction between the narrowband signal reconstruction filter and the usual single-ended switched-mode power amplifier, which, among many other performance impairments, forces a two transistor implementation. The performance of this architecture is clearly explained based on the presented theory, which is supported by simulations and corresponding measured results of a fully working implementation. The drawn conclusions allow the development of a set of design rules for future improvements, one of which is proposed and verified in this thesis. It suggests a significant modification to this traditional architecture, where now the phase modulated carrier is always on – and thus allowing a single transistor implementation – and the amplitude is impressed into the carrier phase according to a bi-phase code.

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List of Acronyms

AC	Alternate Current
ACPR	Adjacent Channel Power Ratio
ADC	Analog to Digital Converter
ADS	Advanced Design System
ASIC	Application Specific Integrated Circuit
ASK	Amplitude Shift Keying
ATC	Amplitude to Time Converter
AWG	Arbitrary Waveform Generator
AWGN	Additive White Gaussian Noise
BAW	Bulk Acoustic Wave
BPF	Band Pass Filter
BPPWM	Band Pass Pulse Width Modulator
BW	Bandwidth
CDF	Cumulative Distributive Function
CDMA	Code Division Multiple Access
CLK	Clock
CMOS	Complementary Metal Oxide Silicon
CRFB	Cascade Resonator and Feedback
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
DCO	Digital Control Oscillator
DDRC	Differential-like Digital-to-RF Converter
DPA	Digital controlled Power Amplifier
DQM	Digital Quadrature Modulator
DRFC	Direct Radio Frequency Converter
DRP	Digital RF Processor
DVB	Digital Video Broadcast

EDGE	Enhanced Data Rates for GSM/DCS Evolution
EDSM	Envelope Delta Sigma Modulator
EM	Electro-Magnetic
ENOB	Effective Number of Bits
FET	Field Effect Transistor
FIRST	Flexible Integrated Radio System and Technology
FPGA	Field Programmable Gate Array
FR	Fixed Rod
FRAMES	Future RAdio wideband MultiplE access system
GEN	Generator
GND	Ground
GSM	Global System for Mobile Communications
GWT	Guided Wave Technology
HSPA	High Speed Packet Access
ICNIA	Integrated Communication Navigation Identification Avionics
IEEE	Institute of Electrical and Electronic Engineering
IMN	Input Matching Network
JTRS	Joint Tactical Radio System
LPF	Lowpass Filter
LSB	Least Significant Bit
LTE	Long Term Evolution
MEMS	Micro-Electromechanical Systems
MSB	Most Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCO	Numerically Controlled Oscillator
NMSE	Normalized Mean Squared Error
OFDM	Orthogonal Frequency Division Multiplex
OMN	Output Matching Network
OSR	Oversampling Ratio
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board

PDF	Probability Distribution Function
PDM	Pulse Density Modulator
PLL	Phase Locked Loop
PPM	Pulse Position Modulator
PSK	Phase Shift Keying
PVT	Process Voltage and Temperature
PWM	Pulse Width Modulator
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RF-CAB	Radio Frequency Carrier Amplitude-Burst
RF-CPB	Radio Frequency Carrier Phase-Burst
RFIC	Radio Frequency Integrated Circuit
RFPA	Radio Frequency Power Amplifier
SAW	Surface Acoustic Wave
SDR	Software Defined Radio
SMPA	Switched-Mode Power Amplifier
SNR	Signal to Noise Ratio
SRR	Software Reconfigurable Radio
TR	Tuning Rod
V_{AC}	Alternate Current Voltage Source
V_{DC}	Direct Current Voltage Source
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

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Chapter 1 – Introduction

1.1 Motivation

The way people communicate and exchange information suffered several changes throughout the ages. However, as depicted in Fig. 1, it is possible to define a simple common system communications model composed by a source, a transmission channel and a receiver that collects the information that has been sent.

Fig. 1 – Example of a simple communications model.

In order to transfer the information (input data) from one location to the other, it is necessary to transfer energy by forcing a change of a physical quantity (pressure, voltage, current, electric field, magnetic field, among others). Depending on the type of channel used, only specific forms of physical support are possible, and the information must be pre-processed so that it is possible to achieve a reliable communication. Therefore, considering one of the most important transmission channels, the free space or the air interface, the electromagnetic energy (radio wave generated by an antenna), is one of the most common physical supports for exchange information. These radio waves have characteristics, such as amplitude and phase, which can be used to introduce the required changes in the physical quantity so that the information can be transferred.

A single frequency wave, with constant amplitude and phase cannot carry any information, because it is not possible to map the input data if nothing changes in the radio wave. However, this difficulty can be surpassed if the amplitude or the phase changes according to the desired data. Since the frequency spectrum is an expensive resource, the researchers are always trying to find a better way to transmit more input information per spectrum unity, Hz, by changing the radio wave characteristics (amplitude and phase). This is the concept of radio wave modulation.

Initially, the modulation was implemented continuously (analog), but since we are in the time of digital computers, the information (pictures, voice, files, etc) is converted into binary data. So, currently, the modulation is also digital (discrete in time and coded in amplitude). Additionally, the digital modulation is also more efficient than the analog one. Hence, it is adopted a modulation strategy, in which orthogonal vectors describe a two dimensional space, where the axes are typically referred to as the in-phase (I) and quadrature (Q) data.

Each of the dots shown in Fig. 2 is called a symbol and represents a pre-defined number of input data bits, depending on the total symbol number in the plane. The symbols can be represented in rectangular (Cartesian) coordinates by (1)

$$s(t) = I(t)\sin(\omega t) + Q(t)\cos(\omega t) \tag{1}$$

where ω is the carrier angular frequency, $I(t)$ is the in-phase vector data and $Q(t)$ is the quadrature vector data.

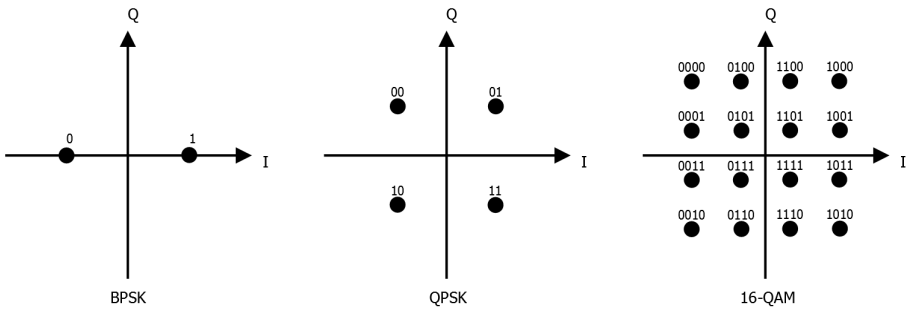

Fig. 2 – Typical examples of digital amplitude and phase modulation formats.

The combination of the vector amplitudes $I(t)$ and $Q(t)$ allows the representation of any symbol in the 2 dimensional plane.

It is also possible to represent the exact same symbols in a polar format, using the amplitude ($A(t)$ measured from the origin to the symbol position) and phase ($\theta(t)$) of the carrier, (2)

$$s(t) = A(t)\cos[\omega t + \theta(t)] \tag{2}$$

With these representations, it is possible to change the amplitude and the phase of the radio wave in use, so that the spectrum efficiency is optimized.

Taking advantage of this digital modulation and due to the different end user needs, business opportunities and technology evolution, a large number of protocols (translated into standards) for digital wireless communications have been developed and implemented. These standards are different in protocol structure, but share similar modulation formats.

As previously mentioned, a communications system is composed of a source, a channel and a receiver. Focusing on the source, in the electric context, it can be implemented by using an electronic transmitter, which is used to implement (1) and (2).

The Cartesian transmitter (Fig. 3) is widely used in wireless systems due to its simplicity, since it is a direct representation of (1).

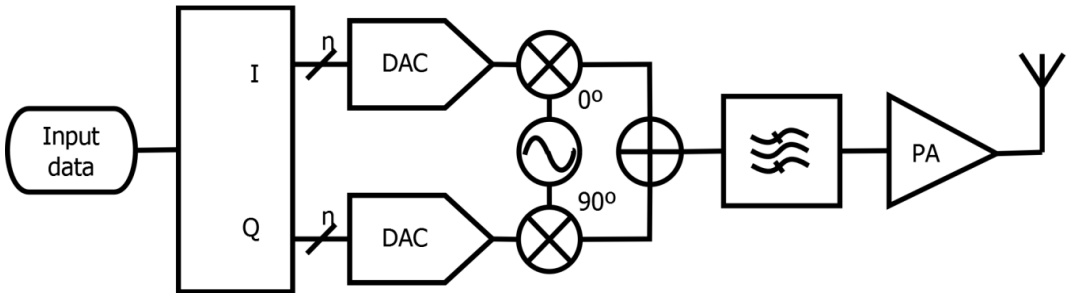

Fig. 3 – Generic direct-conversion Cartesian transmitter schematic.

Moreover, the circuit handles band limited signals, leading to simpler implementation. However, several issues arise from this architecture, [1], being the power amplifier (PA) an identified handicap, because as it needs to be linear, it is inherently inefficient.

A solution for the PA efficiency problem comes from the polar representation, (2), whose circuit implementation is depicted in Fig. 4. As the PA input signal has constant envelope, the PA can operate at its highest performance operating condition, increasing the overall transmitter efficiency. However, despite these advantages, there are some drawbacks, namely the need for the PA power supply modulation. The high current values associated with the wide bandwidth of the envelope (which may be several times the input signal bandwidth) bring in additional problems, namely at circuit implementation level.

In addition to this power and spectrum efficiency optimization goals, nowadays, digital wireless Tx should also provide reconfigurability. In fact, the actual wireless communication systems work with a large number of standards (802.11a/b/g/n, Bluetooth,

CDMA2000, WiMAX, HSPA+, LTE, DVB-T/H), being a desired goal that all, or most of them, are available in the same device. Although the majority of these standards are not simultaneously in operation, their presence, along with the need to reduce the product size and power consumption, poses important and difficult challenges for those who develop these devices.

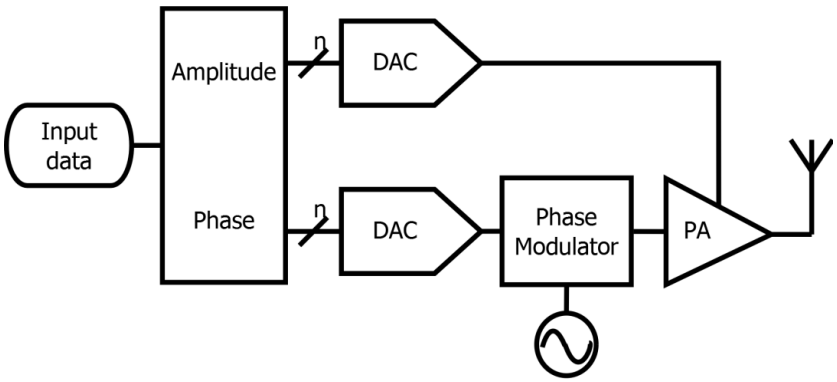

Fig. 4 – Generic Polar transmitter schematic.

Besides the standards multiplicity, due to the countries' internal regulations, the spectrum is used differently worldwide, leading to a wide number of non-contiguous frequency bands available for wireless communications. Therefore, the handsets need to support several of these bands to enable users' mobility (roaming).

Nowadays, the technical differences between each standard requires the use of different transmission blocks, leading to an inefficient architecture and with an increased final cost. The impact of this limitation is visible either in handsets, with more area necessary for integrated circuits and in base stations, where the components need to be replicated.

It is also known that analog architectures tend to become costly relatively to their digitally intensive counterparts. Analog systems are not only difficult to integrate (do not fully benefit from the integrated technology scalability), but also require complex techniques to compensate, for example, gain and phase imbalances (due to process voltage and temperature (PVT) variations), to meet performance and production yield targets.

Therefore, the transmission chain optimization, so that it can be used by more than one standard, without jeopardizing the highly demanding performance specifications of power and spectral efficiency (system linearity), is crucial to achieve the desired gains in both financial and technological aspects. So, the development of a highly efficient,

reconfigurable, digital intensive and multi-band architecture for wireless transmitters is an identified need. This thesis is a contribution towards the answer to these requirements.

1.2 Previous Work

With the increase of digital systems processing speed, the architectures evolution took an important step forward, with the introduction of Software Defined Radio (SDR). The SDR concept started in the late 1970s by the United States (US) Air Force, [2], with the program Integrated Communication, Navigation, Identification and Avionics (ICNIA). The purpose of this project was to develop an architecture to support multifunctional, multiband airborne radios in the 30 MHz - 1600 MHz band. Some of the several hardware functions were dedicated to convert the analog signal into digital in the fewer steps possible. These functionalities were implemented by applying specific integrated circuits (ASICs), whose objective was to provide a generic digital interface that could be used as much as possible by several communication entities. This project evolved in the early 1990s, into a program called SpeakEasy, [3], with the purpose of developing an architecture and technology capable of meeting the future military requirements for multimedia networking operations. During the first developments, the ASICs provided the signal digital processing, but did not allow the system reconfiguration. However, after the field programmable gate arrays (FPGAs) invention by Xilinx in the mid 1980s, the FPGA replaced the ASIC allowing the hardware configuration at the design stage but also the hardware reconfiguration during the field operation. This was one of the major technology evolution steps that made the SDR attractive for the future.

Being aware of this evolution, J. Mitola started to explore the SDR concept in [4], and proposed later its vision for the future SDR, [5], a complete software configurable radio, allowing maximum flexibility and adaptability to different communication scenarios. Unfortunately, due to technological limitations, this solution suffers from several problems that prevent it, in practice, from benefiting from all its theoretical potential. At the receiver level, the analog to digital converter (ADC) is limited in operating band, resolution, dynamic range and sampling frequency. At the transmitter level, in the final stage, the radio frequency (RF) power amplifier (PA) is limited in linearity, power efficiency, operating band and integration ability. Therefore, the increasingly fast FPGA allows the

implementation of Software Reconfigurable Radio (SRR), which are continuously being improved.

Simultaneously, the US military projects continued to evolve into the joint tactical radio system (JTRS), [6], envisioned to be the next generation tactical radio for future advanced military operations. The civil communications also started to use this technology like, as an example, the European flexible integrated radio system and technology (FIRST), [7], and future radio wideband multiple access system (FRAMES), [8].

Following the previous developments and having as major aim the re-configurability, several architecture proposals were further published (more details will be given in Chapter 2), with either Cartesian or Polar topologies.

Nokia and ST Microelectronics [9–11] presented an I&Q architecture, where each baseband branch is digitally processed and prepared for direct RF up-conversion and transmission. It uses two modified low power current steering digital-to-analog converters (DAC), to transform the digital signal into an analog one. The DAC clock is similar to an RF local oscillator allowing the up-conversion in the same operation. The analog output signal of each branch is filtered to remove the unwanted replicas. Both are then combined to form the composite signal. One major problem of this architecture is the presence of I&Q impairments, which was solved by University of Texas and Texas Instruments [12], [13], who used just one similar low power DAC. In this case, all the signals upstream of the DAC are digitally generated, granting a high level of re-configurability.

Other researchers, based on the Envelope Tracking polar topology, Texas Instruments [14–16], developed an architecture, where the envelope path is digitally modulated by a combination of a binary encoder (coarse values) and an one bit sigma-delta modulator ($\Sigma\Delta M$). The phase path was implemented by an all digital phase locked loop (PLL), whose numerically controlled oscillator (NCO) frequency is determined by an array of varicaps. At the output, both paths are combined by a digital low power amplifier with a current based structure, which works also as a digital to analog converter. It is formed by an array of transistors connected in parallel, being possible to control the output current by turning ON the appropriate number of transistors.

A different approach was adopted by Jayaraman [17] where, based on his previous work [18], he used a bandpass sigma-delta modulator ($BP\Sigma\Delta M$), to transform the baseband modulated input signal in a switching signal of one bit (only two levels, ON and OFF) and

with a higher central output frequency. With this signal (a pulsed constant envelope) it is possible to use switching power amplifiers, such as Class D, E or F. After the signal is amplified and before it is delivered to the load, the switching noise is removed by a narrow bandpass filter (BPF), converting the varying pulse density time information into smooth amplitude variations. With a similar structure, Arizona State University and Texas Instruments [19] presented an alternative, where the output signal of the BPΣΔM will feed a modified low power current steering DAC composed by a tap delay line (due to the BPΣΔM one bit stream), where each delay output controls a current source. The sum of all the individual currents forms the amplitude varying output signal.

The presented last two architectures, based on BPΣΔM, need to support high speed switching signals, which can cause additional problems (for instance, switching losses), hence, Wang [20] started to work on an alternative architecture based on polar topology, which was initially proposed by Posner [21], the Radio Frequency Carrier Amplitude-Burst (RF-CAB) transmitter. The common analog phase-modulated carrier is modulated in amplitude in an ON-OFF mode, according to some prescribed envelope-to-time conversion, such as a pulse width modulator (PWM) or a sigma-delta modulator (ΣΔM). There are two variants, one where the envelope and phase paths are combined prior to the amplifier and the other, where the envelope path directly controls the power supply of the amplifier in a more traditional polar configuration. In both options, it is possible to use a high efficiency switched-mode power amplifier (SMPA), such as Class D, E or F, because the input signal has a constant envelope.

It is noticeable in these proposals that re-configurability is the common point where progress is most evident, due to the emphasis and importance given to it. In the architectures' demonstration and testing, besides the re-configurability, the linearity is the parameter most often used, through the use of commercial standards, evidencing compliance with the noise masks. However, the efficiency is often overlooked and it is normal not to consider either the output amplifier or the reconstruction bandpass filter in the analysis, so that the validation is usually performed at low output power. One reason for this omission is the limitation of some architectures, namely the ones based on the Cartesian topology, which prevents the usage of high efficiency power amplifiers. Nevertheless, the proposals suggested by Jayaraman [17] (BPΣΔM) and Posner [21] (RF Carrier Amplitude-Burst Transmitter) can use those amplifiers, but the former one requires

very high speed switching signals, as previously referred, and also a dynamic external load modulation for SMPA proper operation, [22].

Unfortunately, this RF-CAB architecture revealed itself as an example of the long way that can separate a good system-level idea from a fully functional circuit level implementation. Indeed, its new challenging concepts (different from the traditional architectures), along with its theoretically promised performance, turned it into a topic of active research.

In [23–25] several envelope modulators were studied, either by simulation or in a practical implementation, but, in these studies the impact of the adopted choices in the RF-CAB transmitter was only superficially addressed.

The RF-CAB performance using different combinations of the amplitude modulator and SMPA was studied in more detail in [26–31], but the reconstruction BPF was neither included in simulations or measurements. The researchers assumed the "posteriori filtering" of the out-of-band noise and discarded any influence of the filter dynamics in the system performance. Additionally, the impact of the filter on the SMPA performance was identified in [32], [33], with the observation that, with the used implementation, the out-of-band energy was reflected back to the amplifier. So, in order to separate the SMPA from the BPF, the researchers inserted an isolator in between these two circuits, at the expense of a substantial degradation of the system power efficiency. In fact, the interaction between the SMPA and the BPF was identified in [34], where the researchers observed that by changing the length of the connection between these two blocks, the performance changed. However, the proposed zero length connection is restrictive and not feasible in many implementations. Staying with the initial configuration, the complete system was tested and measured in [35], but the obtained 43% drain efficiency (and further dropping at lower input power values) for a 3 tone input signal is quite far from the theoretical expectations. Then, Jeong, Liao and Wang took profit of its inherent dynamic load modulation to propose an implementation intended to mimic the Doherty architecture, [36], [37]. However, this attempt only works as a RF-CAB in the upper half duty-cycles (50% to 100%) of the envelope modulator output, while, in the lower half, it works as a Class-B amplifier. Hence, it is not able to take full profit of the 100% efficiency theoretically expected from the RF-CAB.

1.3 Objectives

The transceivers digitization path that have been followed and developed in the last decade, allowed, not only a higher system integration, but also the implementation of architectures different from the traditional ones. As previously presented, in the quest for a transmitter architecture that is able to simultaneously achieve reconfigurability, linearity and efficiency, among the described options, the RF-CAB transmitter is, in theory, one of the options that has more potential.

Although the effort placed by other researchers in exploring this architecture has been significant, there is still much to be done, since the RF-CAB behavior is not completely clear. In the previous research, the focus was given to the digital part to achieve the reconfigurability, but the last stage amplification and filtering was, in the majority of the situations, left aside. So, we will focus exactly on this last stage, in particular in the interaction between the power amplifier and the reconstruction filter.

Therefore, the main objective of this thesis is to study, model and access the performance limits of the RF Carrier Amplitude-Burst transmitter architecture shown in Fig. 5.

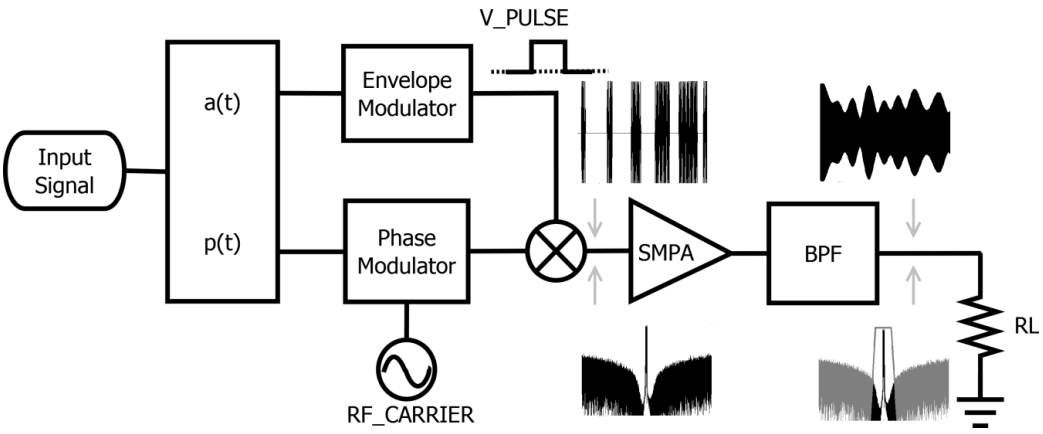

Fig. 5 – RF carrier burst transmitter architecture.

In order to fulfill this goal, the following tasks were defined,

- Develop a theoretical model able to describe the RF-CAB transmitter. A special focus was given to the blocks' interaction, specially between the power amplifier and the bandpass filter, but also to the influence of the envelope modulator characteristics in the system performance.

- Design a physical prototype, to test and verify the theoretical predictions, using discrete components.
- Identify the limitations of this architecture and test the proposed recommendations and optimizations with a practical prototype.

1.4 Thesis' Outline

In Chapter 1 the wireless transmitter architecture topic is introduced, where the main characteristics are described as well as the performance impact of the new standards in the current implementations. This acts also as the motivation for this work. A brief description of the previous work in this field is included, accessing the usefulness of the presented objectives for this thesis. This chapter also contains how the objectives were achieved and the state of the art contributions of this thesis.

In Chapter 2 the state of the art in reconfigurable digital intensive architectures is presented, including a more detailed description of the architecture under study (RF-CAB).

Chapter 3 describes the RF-CAB design at system level, in which the main characteristics of the blocks that compose the architecture are described.

In Chapter 4 the analysis of the RF-CAB at circuit level is performed. It starts with a brief revision of the theoretical idealized behavior of these switched-mode amplifier systems, where the ideal circuit is described. A special attention is paid to the dynamic load modulation caused by the interaction between the narrowband signal reconstruction filter and the SMPA. Additionally, both the efficiency and linearity will be addressed through a theoretical analysis and simulations, providing several recommendations prior to the physical implementation. An illustrative prototype is then presented and the experimental validation also treated.

In order to overcome some of the limitations observed in the RF-CAB, Chapter 5 describes a different approach to the envelope modulation (phase instead of amplitude), but keeping the majority of the RF-CAB characteristics. This new architecture is described at system and circuit level, where the efficiency and linearity are analyzed in theory and via simulations, which are corroborated by the corresponding prototype measurements.

Chapter 6 ends this thesis, where the most important conclusions of the research hereby done are summarized, and possible venues for future research are presented.

Additionally, in Annex A includes a thorough description about how to design combline cavity filters.

1.5 Thesis' Contributions

The optimization of wireless transmitter architectures is a subject of active research, where the ultimate goal is to simultaneously achieve reconfigurability, high integration, efficiency and linearity. The RF-CAB transmitter has been considered a strong candidate to achieve these objectives, but the several issues that have been reported by other researchers prevented its full applicability. It is believed that the majority of the doubts regarding this architecture are clarified with this thesis' contribution, where important and novel information about the RF-CAB functional behavior is reported. These contributions have been published in international conferences and journals, whose papers P1 to P5 are listed at the end of this Sub-Chapter.

In the scientific literature it is usual to find published work where the results do not include the RF-CAB output reconstruction filter. The reason for this omission might rely in the lack of answers for the strange behavior that is sometimes observed when the PA is connected to the BPF. This thesis proves that there is a one to one combination between the types of these two blocks. In fact, a more general solution is also reported, where, by only changing the PA-BPF connection length, any filter topology can be used with the same PA type [P1]-[P2], [P4].

In addition, among the possible RF-CAB implementations, the use of single-ended SMPAs in these transmitters is one of the most common ones, due to their standalone PA efficiency. However, in order to be effective, it is proved in this thesis that an additional element must be added, the flywheel, so that the system works as designed [P4]. With such a design, it is also proved that the transmitter drain efficiency is not dependent on the envelope modulator coding efficiency [P4]. In fact, it was proved that the RF-CAB is, ideally, perfectly linear and efficient. However, the real prototype impairments add extra efficiency and linearity losses, whose sources are thoroughly analyzed and verified [P4].

In order to overcome some of the performance limitations inherent to the analyzed RF-CAB implementation, it is proposed in this thesis the RF Carrier Phase Burst (RF-CPB), which does not need any flywheel transistor [P3], [P5].

[P1] - Sergio C. Pires, Pedro M. Cabral and José C. Pedro, "A carrier-burst transmitter implementation: Design of bandpass filter and amplifier-BPF connection", *Proc. Workshop Integrated Nonlinear Microwave and Millimeter-Wave Circuits (INMMIC)*, Dublin, Ireland, pp. 1-3, Jun. 2012

[P2] - Sergio C. Pires, Pedro M. Cabral and José C. Pedro, "Impact of the Amplifier-Bandpass Reconstruction Filter Interaction on the Linearity of Carrier Amplitude-Burst Transmitters", *IEEE 14th Annual Wireless and Microwave Technology Conference (WAMICON)*, Orlando, Florida, United States, pp. 1-4, Apr. 2013

[P3] - Sergio C. Pires, Pedro M. Cabral and José C. Pedro, "RF Carrier Phase-Burst Transmitter", *IEEE MTT-S International Microwave Symposium Digest (MTT)*, Seattle, Washington, United States, Jun. 2013

[P4] - Sergio C. Pires, Pedro M. Cabral and José C. Pedro, "Carrier Amplitude-Burst Transmitters - From Architecture to Circuit", Submitted to *IET Microwaves, Antennas & Propagation,* 2013

[P5] - Sergio C. Pires, Pedro M. Cabral and José C. Pedro, "Envelope Modulator Selection for RF Carrier Phase-Burst Transmitters", Submitted to *IEEE Microwave and Wireless Component Letters.,* 2013

Chapter 2 – State of the Art of Digital Intensive Multi-standard Wireless Transmitter Architectures

In the near future, it will not be possible to achieve the SDR requirements in terms of dynamic range and noise, so Software Reconfigurable Radio (SRR) has been a consistent approach. With this, it is desired that the radios can re-configure their transmission standard, without the underlying hardware changes, by changing only its internal characteristic connections. It will also be possible to better control the system at both the design and manufacture, because digital circuits are less sensible to tolerance oscillations, very common in analog components (integrated or discrete). This is an adopted direction by some industrial and academic authors.

Although the SDR theme has already almost two decades, the research activity in this topic has intensified recently, taking into account the main initial objective (re-configurability) and given the evolution of digital technology that enabled faster processing power. In the integrated circuit field, for radio frequency (RF) applications, Silicon Germanium (SiGe) and Gallium Arsenide (GaAs) are the most common technologies used in the analog part, due to their speed and power capabilities. In the digital part of the transceivers, CMOS has been the most widely used technology, because it is reliable, scalable and less expensive. Recent CMOS processes started to be more competitive in terms of technical performance, leading to the appearance of analog CMOS. The technology processes evolved in a way that the analog transistors started to have RF capabilities. However, not only the analog part evolved, as the transistors become faster, but the digital parts also started to operate at higher clock frequencies, allowing higher digital processing power. This progress also reinforced the transceiver "digitization", becoming appellative to have a full CMOS transceiver, with evident gains in terms of design, manufacture and testing.

As referred before, this investigation topic has been subject to work by industry and academic players, either standalone or in joint cooperation. Starting with the architectures in which the industry is involved, some examples will be presented and analyzed according with the three initial objectives, re-configurability, linearity and efficiency. It is important

to notice that some of these architectures were actually implemented in commercial products.

2.1 DRFC - Direct Radio Frequency Converter

Elaborated jointly between Nokia and ST Microelectronics, [9–11], Fig. 6, it is proposed an I&Q based architecture, at which each branch is digitally processed at baseband through interpolators and filters to prepare the signal for RF transmission. It uses a direct up-conversion, as the baseband signal feeds the Digital to RF Converter (DRFC), a special mixed mode up-converter. The DRFC is a modified current steering Digital to Analog Converter (DAC), with similar function as a mixer, whose clock has the same frequency as a local oscillator (LO). Current steering DAC's are usually composed by a large number of individual cells (2Bit Number), contributing each one to the final current sum, allowing the output signal amplitude and phase to be changed as the input data changes. In this case, a 10bit DAC was used, so it will be necessary 1024 of these cells. Each one of these cells needs to be connected to the global clock, causing additional difficulties on the distribution, due to its large number.

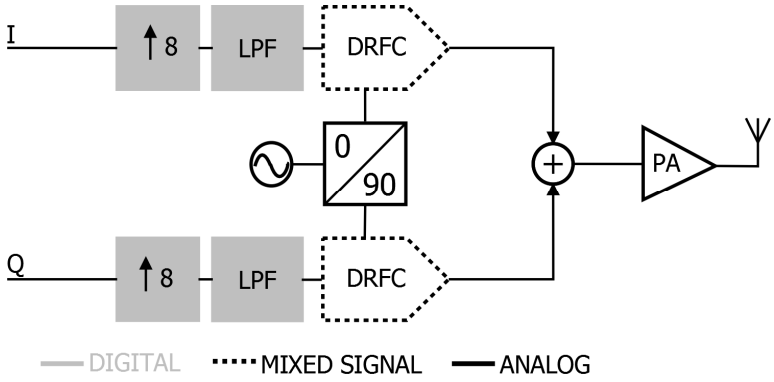

Fig. 6 – Direct radio frequency converter architecture.

Additionally, the precision required for the Least Significant Bit (LSB) is enormous, causing large difficulties in the implementation, due to the tolerances in integrated circuits. To overcome them, this DAC was segmented in two parts, one binary coded with 6 coarse bits and the other thermometer coded with 4 bits, leading to less stringent implementation, as is usually done with these types of DAC.

The DRFC individual cells, Fig. 7, have a topology similar to a Gilbert-cell mixer. Both Baseband Data and clock (Local Oscillator) are differential and switching signals. In the case of the LO, as it is analog generated, latches are introduced at DRFC input, to convert it to digital domain. The output of this cell will be a current signal, which will have the same phase as the input data (ON or OFF). At the global output, the final current will be the sum of all cells, being filtered (filter included inside DRFC block) in order to remove the unwanted signal replicas.

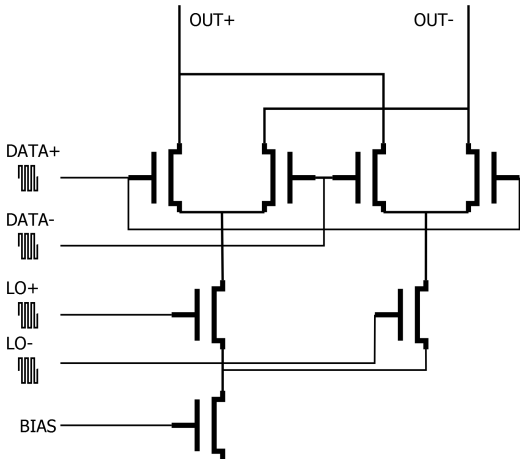

Fig. 7 – Cell implementation of the direct radio frequency converter.

Nevertheless being a step forward to digital integration and besides all difficulties inherent to current steering DAC's, this architecture suffers from the same old problems of I&Q architectures, such as I&Q imbalance (I and Q branches are summed at DAC's output as analog signals). To overcome these impairments, complex digital compensation techniques are required. The tests performed by the authors with WCDMA, WLAN and GSM standards indicate that it is possible to change the standard by updating the digital part of the chip and still fulfilling the spectrum masks for each one. Therefore, not only the re-configurability is good, but also the linearity is accomplished. Regarding the efficiency, which was never mentioned by the authors, it is expected to be low. Since the output power from the DRFC output is low, an external RFPA is needed to increase it and when a complex digital modulation is used, the RFPA needs to be linear and dimensioned in power back-off, leading to efficiency issues. The analog nature and characteristics of the DRFC output signal prevents the usage of a more efficient power amplifier. Due to these

characteristics, regarding the last stage of amplification, this architecture is very similar to the conventional analog one and all the associated and well known problems.

2.2 DQM - Digital Quadrature Modulator

In a cooperation between University of Texas and Texas Instruments, [12], [13], the authors proposed another architecture, Fig. 8. Based on the system described in Chapter 2.1 (Direct Radio Frequency Converter), the objective was to solve two main issues:

- Use and generation of Digital clock
- I&Q impairments

Starting with the first one, the clock generation is based on the work of Staszewski [15], which will be described in Chapter 2.4. Considering that the clock is available and in digital format, it is possible to generate several phases and frequencies needed for the proper operation of the system.

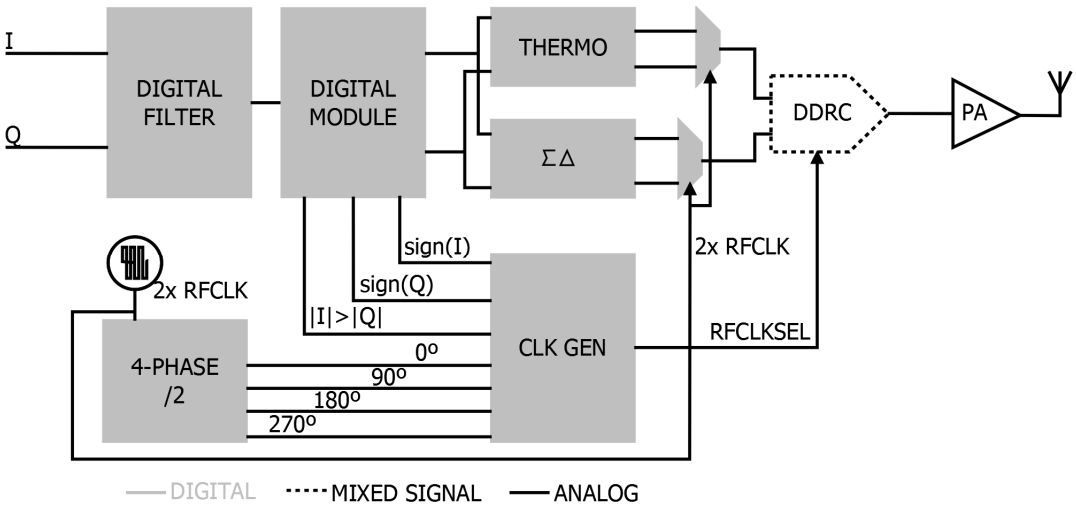

Fig. 8 – Digital quadrature modulator architecture.

The I&Q impairments were solved by using just one Digital to Analog Converter (DAC), so no recombination is needed at analog side, where the I&Q composite signal will come directly from DAC's output. At the same time, as the DAC is a current steering one, the precision requirements were also relaxed by the use of segmentation. However, in this case, for the coarse part, the binary codification was abandoned and replaced by

thermometer encoding. For the precision part, a sigma-delta modulator (ΣΔM) was used to take advantage of its oversampling and noise shaping characteristics.

Considering again Fig. 8, after the signals I&Q were processed by DIGITAL FILTER block (filtering and up-sampling), the DIGITAL MODULE block generates two major bus signals |I-Q| and |I+Q| which will feed the THERMO encoder for the integer Most Significant Bits (MSB) and ΣΔM encoder for the fractional Least Significant Bits (LSB). In fact, two equal pairs of these encoders exist to handle both |I-Q| and |I+Q| signals. The output of the THERMO encoders (bus with 2MSB bits), as well as the outputs of the ΣΔM (one bit) will feed the Differential-like Digital-to-RF Converter block (DDRC), which is a current steering DAC. This processing will be done at 2x the clock frequency, so both |I-Q| and |I+Q| in series will appear at the input of the DDRC, in one clock period. With just these two signals, the information of phase and amplitude is lost, so the proper selection and phase of |I-Q| and |I+Q| is done through the choice of the appropriate clock phase from CLK GEN block. This block selects the clock signal phase accordingly with the signs of I and Q in a four quadrant operation. As the clock phase changes accordingly, the DAC's output will have a four-quadrant codification, allowing the implementation of complex digital modulations. At DDRC, the MSB bits will provide the major part of the output current and the one bit Sigma-Delta output will provide the fine tuning.

As it can be seen in the block diagram, almost all the blocks are digitally implemented, which it is very good in terms of integration and the absence of analog impairments in this architecture it is a strong added value.

This system was tested by the authors with WiMAX standard, fulfilling the spectrum mask requirements, but as the output is digitally driven, with large spurious and replicas, before the external power amplifier (PA), analog filtering is necessary. Once again, in this case, the PA needs to be dimensioned with back-off if complex modulations are used, leading to inefficiency. No options to minimize this issue were suggested by the authors.

2.3 DIF2RF - Digital Intermediate Frequency to Radio Frequency

Arizona State University and Texas Instruments [19] developed an architecture based on the usage of a bandpass Sigma Delta modulator (BPΣΔM) and a current steering digital

to analog converter (DAC), Fig. 9. Contrarily to the two previous architectures, this one uses a super-heterodyne non-conventional structure.

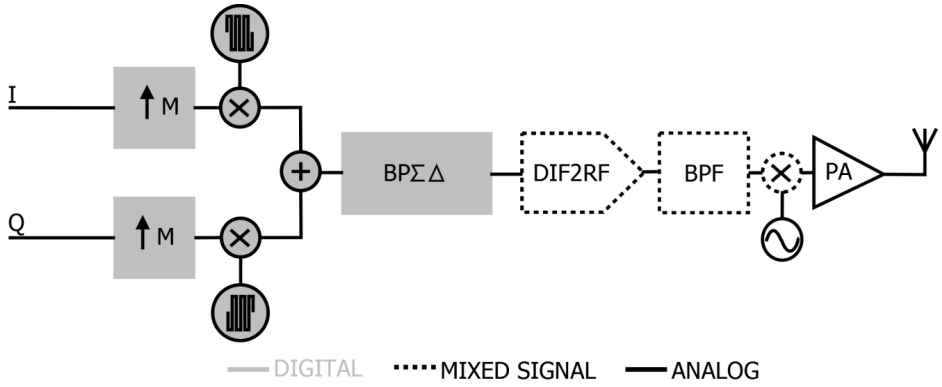

Fig. 9 – Digital intermediate frequency to RF architecture.

A Cartesian topology is used, where the data from I and Q branches is up-sampled and digitally modulated into an intermediate frequency (IF), which is low enough to be implemented by simple logic. After that, the data is coded by the BPΣΔM with one output bit, centered at IF frequency. The resulting signal will feed the current steering DAC (has a different structure from the ones described before in the two previous architectures), Fig. 10.

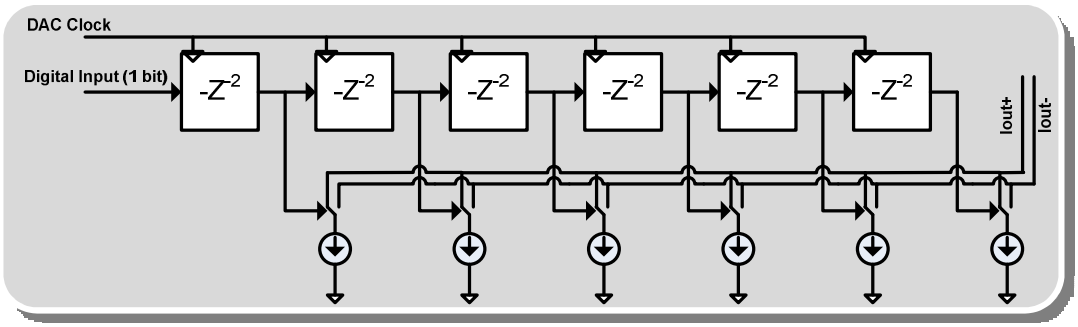

Fig. 10 – Digital Intermediate Frequency to RF tap filter and current cells.

The DAC is composed by a tap delay line, in which each output will control a current source. This is necessary, because the BPΣΔM output is composed by one bit stream. This block also performs up-conversion, with the current sources being switched ON and OFF by a higher frequency LO. At the output of the DAC, the unwanted quantization noise

from the BPΣΔM is removed by a bandpass filter. Additionally, as the output signal is analog and continuous, a linear PA is necessary to increase the output power.

This architecture is less suitable for integration than for example the DQM one (Chapter 2.2) but, it introduces a new block, the BPΣΔM. Although, the re-configurability is not higher than the previous proposals. The tests performed just used two tones for linearity assessment. The efficiency was not addressed, not even a proposal of what amplifier could be used in this architecture.

2.4 DRP - Digital RF Processor

Texas Instruments formed a special group dedicated to this subject based on the work of Staszewski [14–16], having even produced successfully the following system, Fig. 11. Based on the Envelope Tracking Polar topology, the Digital RF Processor (DRP) amplitude path is modulated by a binary encoder for coarse values and by a ΣΔM (one bit) for fine adjustments. Both buses are then combined and formed in a single bus which will control the amplitude of the Digital controlled Power Amplifier (DPA).

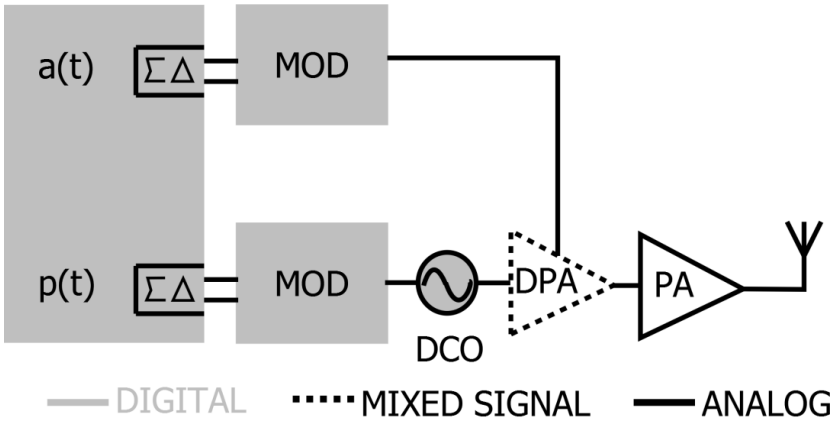

Fig. 11 – Digital RF processor architecture.

The phase path has also two main buses, a binary for coarse values and a ΣΔM (one bit) for fine adjustments. After the combination result of these two buses will control the Digital Controlled Oscillator (DCO), which is the core of this architecture, Fig. 12, formed by an all digital phase-locked loop (PLL).

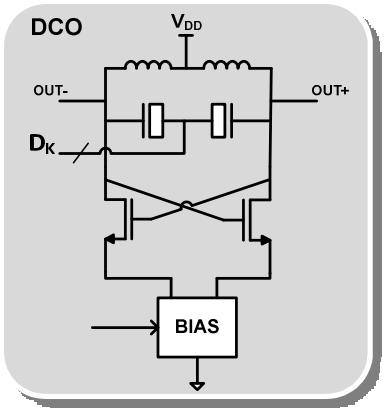

Fig. 12 – Core of the digital controlled oscillator.

In this case, the phase has several sub-buses forming a phase tuning word with data for acquisition and tracking (integer and fractional), and also fine adjustments for process voltage and temperature (PVT) variations.

In the DCO, an oscillator containing a few inductors and an array of varicaps constitutes the only analog part of its core. The oscillation frequency is controlled by the selection of the varicaps, controlled by the phase tuning word previously described. With this procedure all phase modulations are possible, within the inherent limits of the varicaps array values, but with enough resolution and precision required for example by GSM and EDGE (tested standards by the researchers).

At the end, the DPA, Fig. 13, will assemble the amplitude and phase paths. The structure is current based, formed by transistors connected in parallel so that the output current would be the sum of all the ON transistors. The buses that come from amplitude and phase paths will control bit by bit, individually, each of these transistors. Like this, it is possible, not only to control the output signal amplitude, but also, the frequency and phase in an operation similar to a current steering DAC. At the output of the DPA, the signal is filtered and then an external PA is used for power boosting.

This architecture is almost all digitally implemented, being highly reconfigurable. In fact, the DCO is a major development in this area, which is highly referred and used in other authors work. However, the tests performed and presented, only included GSM and EDGE standards, which are less demanding than for instance CDMA2000. The efficiency was not referred by the authors and it is also necessary to add an external PA to increase the output power, because the DPA is power limited.

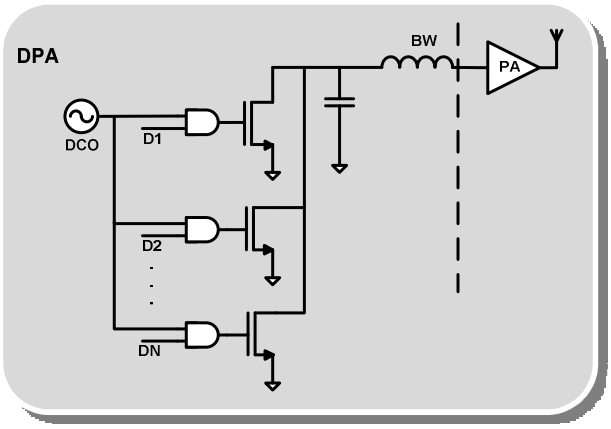

Fig. 13 – Structure of the digital power amplifier.

2.5 BP-(ΣΔM;PWM) - Bandpass-(Sigma Delta Modulator ; Pulse Width Modulator)

Another researcher, Jayaraman [17] based on his previous work on bandpass Sigma Delta modulator (BPΣΔM) [18], theoretically proposed the following architecture, Fig. 14, for a RF transmitter.

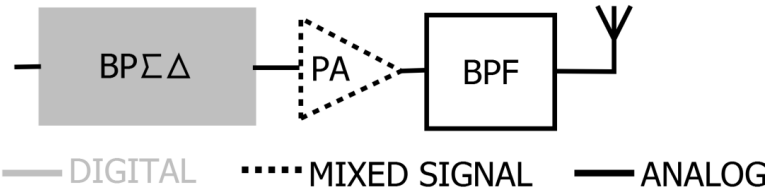

Fig. 14 – Bandpass sigma delta modulator transmitter architecture.

This type of architecture is also referred as Class-S amplifier, which was firstly proposed by Bedford patent [38], but only on the late 90's become interesting with the speed increase of integrated circuits.

A BPΣΔM performs two operations. First, it transforms the amplitude and phase information of a baseband modulated input signal in the time information of a one bit switching signal (only two levels, ON and OFF). Second, it up-converts the input signal to a higher central frequency. The spectrum of this signal will have a similar shape to the one of a lowpass sigma-delta modulator (LPΣΔM), in which a designed (small) bandwidth is noise free from the high-pass quantization noise, but centered at the RF carrier frequency

instead of DC. The proposed modulator has a switching frequency four times higher than the RF carrier frequency. Since the output signal has a pulsed constant envelope, it allows the use of switch-mode power amplifiers (SMPA), such as Class D, E or F, with significant good perspectives regarding the efficiency. After the signal is amplified, the quantization noise is removed by a narrow bandpass filter (BPF), before it is delivered to the load.

The researchers soon realized that for relatively high RF carrier frequencies, the switching speed of the BPΣΔM reached a value where it was very complicated to design the modulator with the current transistor technology and the power consumption dramatically increased due to the switching losses.

Having these difficulties in mind, Iwamoto [39] constructed a demonstrator with a 10MHz carrier, Fig. 15. The BPF had a 10MHz central frequency, 700 KHz of 3dB BW and 0.7 dB of insertion loss.

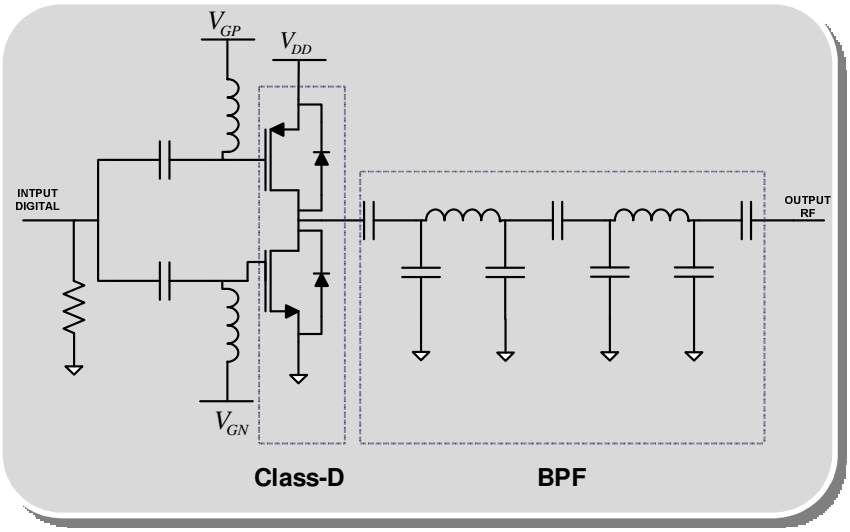

Fig. 15 – Class-D amplifier and bandpass filter.

Although the system has a theoretical high potential, the results for two tone tests did not fulfill the expectations. The measured output power for each tone was 23dBm, for 40dBc of 3rd order inter-modulation distortion (IM3) and 33% of output efficiency. Several causes were appointed for this large decay in efficiency, namely, the losses in the transistor (high R_{on} and switching losses) and the BPF attenuation. Additionally, another potential problem was pointed, regarding the amplifier input driver, which needs to have a

large bandwidth (the switching signal from the BPΣΔM must not be affected by the driver) as well as an enough output power to properly drive the power amplifier (PA).

This same team continued this investigation line [40], [41], but their major focus was to develop a digital BPΣΔM capable to achieve a higher RF carrier, for a switching frequency of 3.2 GHz.

Other researchers also followed the same path,[25], [42–44], and developed other types of BPΣΔM or BPPWM [45], for this type of architectures. All of them presented results for the linearity at the output of the digital modulator with several standards, but decided not to analyze the PA and BPF. The lack of this analysis do not allow in practice to assess how the efficiency of whole transmitter behaves in the presence of such high frequencies.

The ON and OFF periods of these time variant high frequency digital switching signals, might have different time durations leading to variable instantaneous duty-cycle, which degrades the SMPA performance for a fixed output matching network (OMN), [46], [47].

Knowing this handicap, Ozen et al [22] proposed a solution to efficiently amplify these signals, which involved the dynamic configuration of the OMN according with the input signal characteristics. However, not only the method involved the usage of special high power varicaps, which limit their practical use, but also the output reconstruction BPF and its interaction with the SMPA was not included in the analysis.

This type of architecture has a great re-configurability potential but, the high switching speeds of the bandpass modulator increases the digital power consumption, which may penalize the overall efficiency of the transmitter, and the fact that it is necessary to introduce an external load modulation, are two major drawbacks regarding the full usage of this type of architecture.

2.6 RF Polar and RF Carrier Amplitude-Burst Transmitter

In order to overcome the difficulties imposed by the high switching frequency of the band pass Sigma-Delta Modulator (BPΣΔM), Wang [20] started to work in an alternative architecture (initially proposed by Posner [21]) based on Polar topology, with two options, where the Sigma-Delta modulator (ΣΔM) does not need to have such high speed. In this architecture it is only necessary to modulate the envelope at baseband, therefore the ΣΔM is low pass, reducing considerably the switching speed. The amplitude path is now

composed by a bit stream where the amplitude information has been converted in time, where the information lies in the pulses density. In the phase path, a RF carrier will be modulated in phase by the input signal phase information, turning it into a constant envelope signal.

The recombination of the two paths can be done in two ways. In the first, Polar Transmitter, Fig. 16, the modulated RF carrier will be the input signal of the PA, while the modulated envelope will control the power supply of the PA. In the second, RF-CAB transmitter, Fig. 17, both paths are combined prior to the PA, which has constant power supply. The PA input signal will now be an ON-OFF RF carrier. As in the previous architectures (using BPΣΔM), the large quantization noise introduced by the ΣΔM will be removed by the BPF, which needs to have a narrow bandwidth (BW).

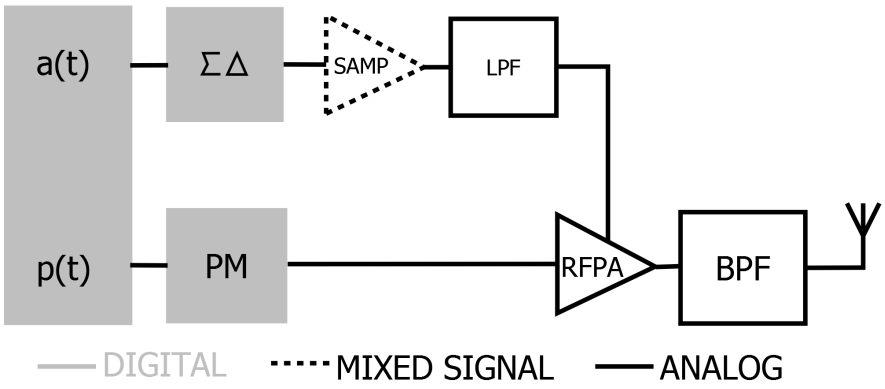

Fig. 16 – Generic polar transmitter architecture.

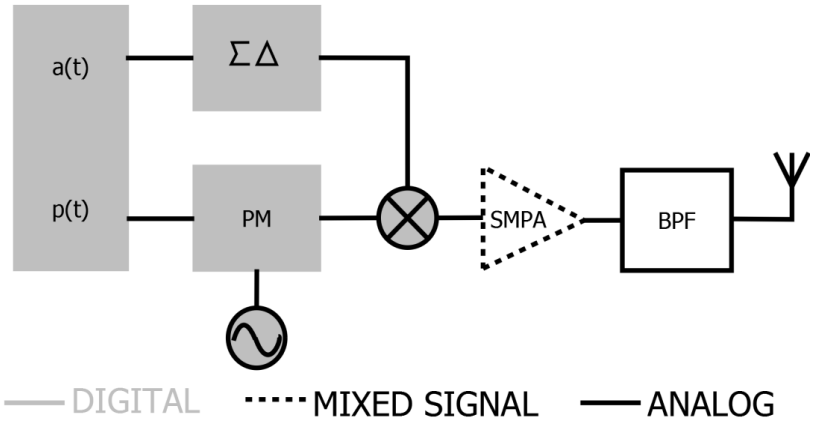

Fig. 17 – RF carrier amplitude-burst transmitter architecture with envelope codification by a ΣΔM.

The Polar Transmitter was adopted by Choi [27], where it was used a ΣΔM to code the envelope and also Class-D and Class-F amplifiers for the output stage. Choi tested the system with a CDMA IS-95A signal, resulting in 31% of overall efficiency and 45dBc of ACPR for 22.1 dBm of output power. The authors also used a three bit ΣΔM, with which achieved better results. The drawback of this architecture is the switching of the PA power supply high current, which can be quite difficult for high values.

The RF-CAB transmitter is also popular, with further developments from Wang team [35], where Dupuy implemented a system composed by a ΣΔM for the envelope, a Class-E PA at 2.47GHz and a bandpass filter of 26MHz pass-band with 2dB of insertion loss. The signal used for testing was composed by 3 tones at 2.47GHz and 2.47GHz +-1MHz. The overall efficiency obtained was around 30% for an output power of 18dBm.

Although the efficiency practical results are not those expected, the potential of this architecture is evident. The re-configurability can be achieved by the lowpass ΣΔM for the envelope modulation and the phase modulation could be achieved by a DCO similar to the one used in Digital RF Processor architecture, Chapter 2.4, allowing a complete standard modification, by just reconfiguring the hardware. The switching speed of the lowpass ΣΔM is slower than the one of a bandpass ΣΔM and therefore the system efficiency is less restricted by this block. The fact that the combined signal is composed by a pulsed modulated carrier, allows the usage of a high efficiency SMPA, such as a Class-E or F. Theoretically, the system is linear, but the proposed implementations had not yet been proved it in practice.

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Chapter 3 – RF Carrier Amplitude-Burst Transmitter Architecture

The RF-CAB (presented in Fig. 18) system operation of is strongly influenced by the amplitude to time converter (ATC) and the output bandpass reconstruction filter. The ATC converts the varying input envelope signal into a two-level one and the BPF removes the large amount of switching noise introduced by the ATC coding.

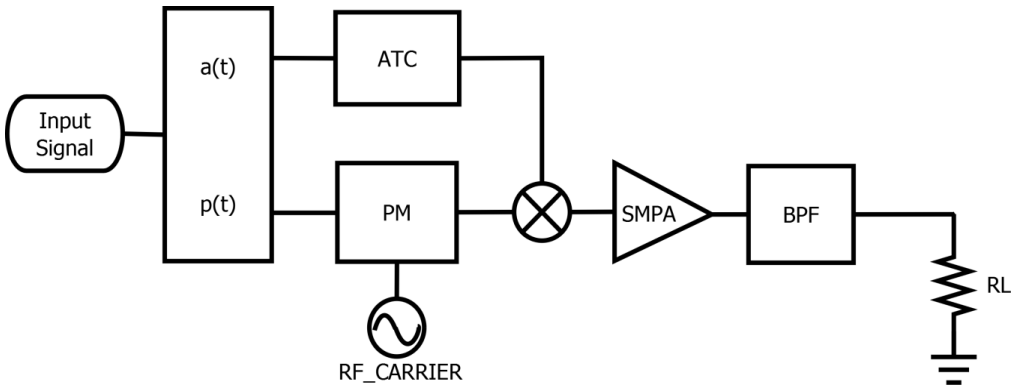


Fig. 18 – RF Carrier amplitude-burst transmitter.

In general the ATC can be divided into two subcategories, the Pulse Density Modulation (PDM) and the Pulse Position and/or Width Modulation (PPM/PWM). In the PDM, the output signal has pulses with unity duration whose density variation encodes the input signal. In the PPM or PWM, the input signal is encoded by the pulses position and width respectively.

The frequency proximity of the switching noise (introduced by the ATC) to the band of interest (centered at the carrier after the multiplication with the phase modulated carrier) is dependent on these modulator's characteristics and will define the BPF characteristics. The filter must be narrower (more difficult to design) or wider, depending on how close the noise is to the pass-band. Considering the ΣΔM, it is possible to move away the noise from the passband by either changing the modulator characteristics [48] (increasing the order and sampling frequency), or by using feed-forward techniques [49], which relaxes the BPF design specs. Similar behavior is achieved with the PWM by increasing the triangular

wave comparison frequency. The drawback is that the amplitude modulator complexity increases. So, there is a trade-off, where the design complexity can be iteratively balanced between these two blocks.

From the system perspective, the design of the remaining blocks is more independent. The phase modulator design is completely stand-alone and the SMPA can be ideally selected among one of the available switched-mode PA types (Class-D, E, F), since it is assumed that it does not interact with the other blocks.

In the following Sub-Chapters, possible options for the required subsystems will be presented, as well as their major functional and implementation characteristics. A strong emphasis will be given to the ATC, SMPA and BPF, while the remaining blocks (phase modulator, oscillator and baseband block) will be left for a future analysis. At the end of this chapter, the system will be designed, taking into account the previous descriptions.

3.1 Envelope Modulator - Amplitude to Time Converter

It is possible to implement the ATC in multiple forms and optimize it in even more ways, but it is not the purpose of this thesis to explore all of these options. As previously referred, one of the objectives is to verify the impact of the characteristics of the two types, PDM and PWM (since the PPM is similar to PWM we will focus on PWM), on the RF-CAB performance. So, in this Sub-Chapter, we will focus on describing the generic architecture of these modulators and their principal characteristics in both time and frequency domains. Several simulation (using Matlab) results that help understanding some of their functionalities will also be presented.

Therefore, starting with the PWM, in the left side of Fig. 19 is depicted the modulator input signals, in the center a possible implementation and in the right side the output signal of the modulator.

It is a very simple system, composed by a comparator with two inputs and an output. The input signal is connected to the positive input and a triangular wave is connected to the negative input. If the input signal is higher than the comparison triangular wave, the output of the comparator is high, or low if the opposite is verified. The output signal is described by its amplitude levels (HI and LOW) and also by its timing.

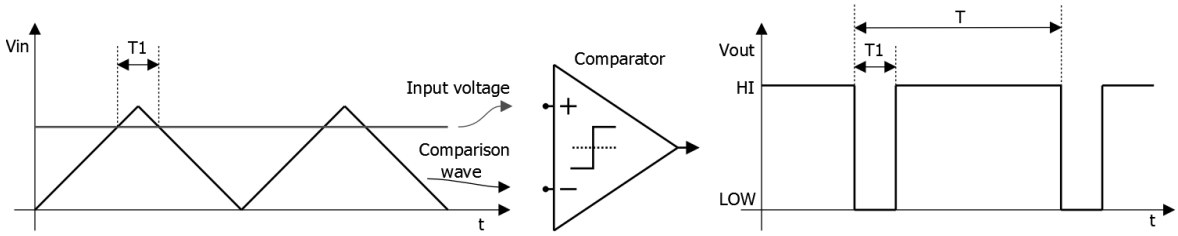


Fig. 19 – Pulse-width modulator device with input and output waveforms.

Since the width changes accordingly with the input signal level, the timing (duty-cycle, δ) is the relation between the HI time and the wave period,

$$\delta = \frac{T - T1}{T} \tag{3}$$

As an example, the signal with variable amplitude presented in Fig. 20 was modulated by a PWM with a triangular comparison wave with a frequency of 10 MHz.

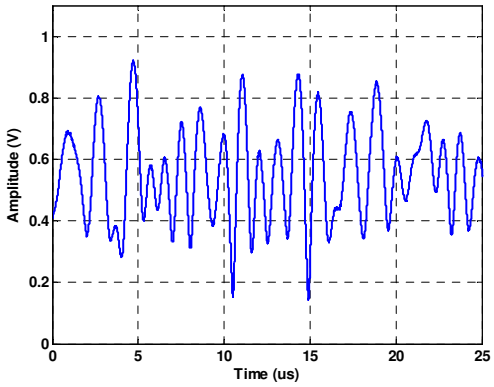


Fig. 20 – Signal with variable amplitude in time domain.

The output of the modulator is depicted in Fig. 21, where it is possible to see that, as expected, when the input signal increases, the HI periods are larger than the LOW ones.

Another very important characteristic is the frequency of the comparison wave. Since it must be possible to recover the input signal by filtering the switching noise introduced by the codification, the triangular wave frequency must be at least two times higher than the input signal bandwidth. In Fig. 22 it is shown the normalized power spectrum of both the input signal and the PWM output signal, where the input spectrum is replicated around

each of the comparison wave harmonics. There are some cases, like this one, where the input signal bandwidth is not limited, leading to an inevitable overlap between the input and output spectrum. However, as it will be shown later in this chapter, depending on the required linearity of the recovered signal (after removing the switching noise), this overlap might not be too important.

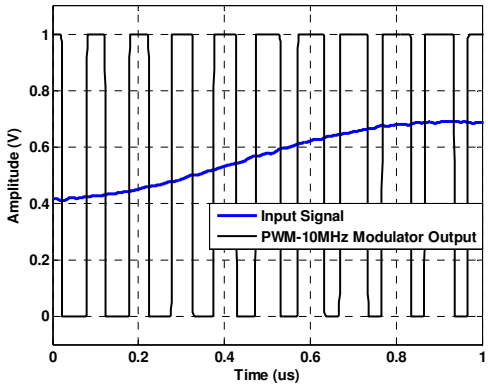


Fig. 21 – Variable amplitude input signal and PWM-10MHz amplitude to time converter output signal in time domain.

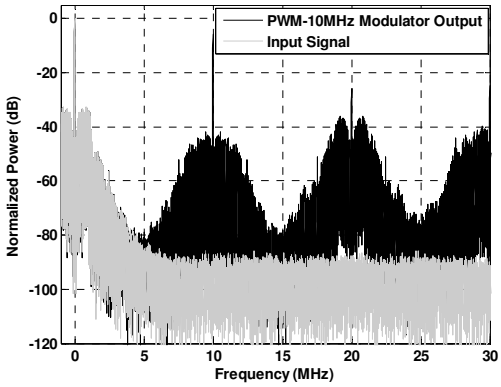


Fig. 22 – Variable amplitude input signal and PWM-10MHz amplitude to time converter output signal in frequency domain.

Still on PWM, ideally, it does not have quantization error, because the if both the input signal and comparison wave are analog, the timing resolution would be infinite. However, the baseband signal will be replicated around the PWM comparison frequency harmonics and as previously referred, if its bandwidth is not limited, then the harmonics will overlap

with the baseband signal causing distortion [50]. Additionally, in a digital implementation, the sampling frequency will impose the noise floor that the PWM is capable to achieve.

Continuing with the PDM, the most popular architecture is the ΣΔM, which has a total different structure relatively to the PWM. There is an immense amount of work that innumerous researchers have produced in this topic, which led to vast range of configurations, topologies and their variations [51], but we will concentrate in the digital architectures. An example of a ΣΔM is depicted in Fig. 23 and is composed by a feedback structure with a digital integrator and a one bit comparator. In this case, it is a first order modulator, where the order is defined by the integrator number.

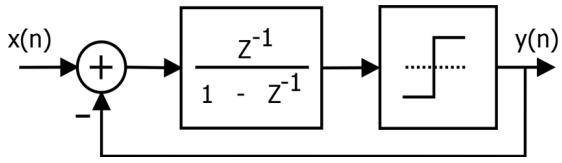


Fig. 23 – 1st Order general sigma-delta modulator.

The initial signal, if analog, is first sampled, producing $x(n)$, which is the ΣΔM input signal. This sampling frequency must be several times higher than the input signal bandwidth, leading to an oversampling modulator. At the output, $y(n)$ is an one bit signal with just two levels, HI and LOW, produced by the one bit comparator or analog to digital converter (ADC). In spite of the large quantization noise introduced by the one bit ADC, this modulator has the ability to shape this noise with a highpass frequency characteristic, leaving a lowpass noise free region. The input signal spectrum must lie in this lowpass frequency band, to allow a recovery after the codification.

Another advantage of this structure is that it has an inherent input signal dithering (necessary to achieve an effective codification, in a oversampling modulator, [52]) introduced by the quantization error of the one bit ADC. However, this dithering is not optimum (truly random) and follows a repetitive pattern, which introduces some additional unwanted signals in the output spectrum, known as idle tones. However, it is possible to minimize this issue by increasing the modulator order (introducing more integrators). In fact, the ΣΔM order increase not only attenuates the idle tones effect, but also improves the quantization noise shaping, increasing the noise free bandwidth.

An example of a third order ΣΔM is presented in Fig. 24. The gain blocks *gx* (acting in fact as digital attenuators) are introduced to prevent the integrators' saturation and are optimization parameters of this architecture.

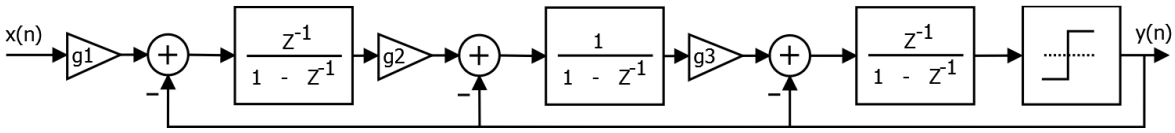


Fig. 24 – 3rd Order general sigma-delta modulator.

This 3rd order ΣΔM was tested using an input signal composed by a DC value plus some random additive white Gaussian noise (AWGN), to evaluate its performance. The normalized spectrum of the output signal is presented in Fig. 25 for a sampling frequency of the modulator equal to 90 MHz.

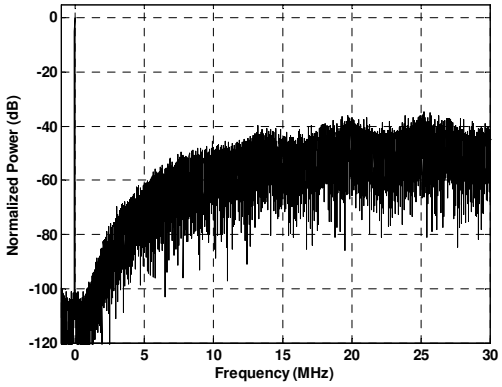


Fig. 25 – ΣΔM SD3-90 MHz amplitude to time converter output signal normalized spectrum for a DC (plus noise) input signal.

It is visible the highpass characteristic of the noise and the noise free region at the low frequencies, where it is possible to calculate the signal to noise ratio (SNR) [53],

$$SNR = 10\log\left[\frac{3\left(2^N-1\right)^2(2L+1)OSR^{2L+1}}{2\pi^{2L}}\right] \tag{4}$$

where, N is the number of bits, L is the modulator order and OSR the oversampling ratio, which is defined as the ratio of the sampling frequency over twice the lowpass bandwidth.

Depending on the lowpass reconstruction filter, the SNR might be lower or higher. In fact, for this type of modulator and for a very low bandwidths, the noise should be very low, increasing the SNR. This behavior is not visible in Fig. 25, where a noise floor slightly higher than -100 dB close to DC is presented. The problem is that when the input signal frequency is very low, the oversampling increases and at every instant, the input signal resembles a continuous signal for the modulator, causing instabilities. For testing purposes, we added some noise, which limit the observable noise floor.

As was previously referred, as close the noise is to the input signal band, the BPF design specs need to be more restrictive, increasing the implementation difficulty. So, among the countless ΣΔM available improvements, it is possible to modify the ΣΔM structure, inserting feedback signals in order to increase the noise free region. An example of such an improvement is depicted in Fig. 26,[51].

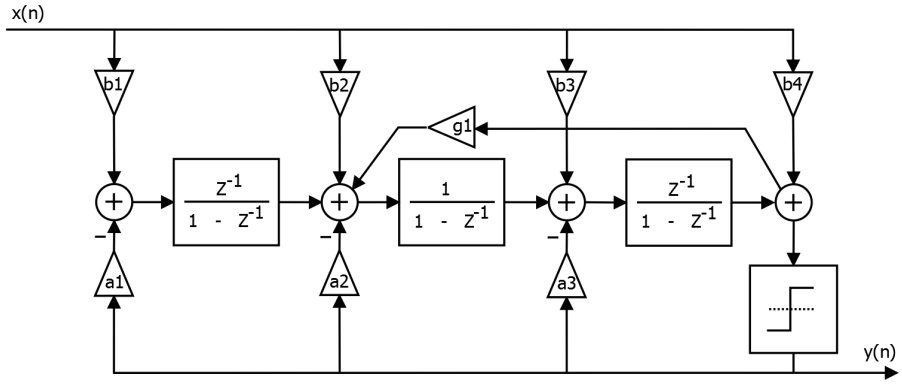


Fig. 26 – 3rd Order sigma-delta modulator with cascade resonators and feedback.

This 3rd order ΣΔM with cascade resonators and feedback (CRFB3) architecture has the same number of resonators, but several paths of feedback and feed-forward were added. The *ax* and *bx* gain blocks are optimized so that the output signal normalized spectrum of Fig. 27 is obtained. To better compare this ΣΔM architecture with the regular one, the same test conditions (input signal and sampling frequency) were used. The noise free region widened, but at the expense of the noise floor increase, a tradeoff that depend on each application.

It is possible to increase the noise free region by increasing the order and/or the sampling frequency, but in both cases the complexity of the modulators also increases. An

order of 3 is relatively easy to develop and a sampling frequency of a couple hundred MHz do not substantially increase the switching power consumption.

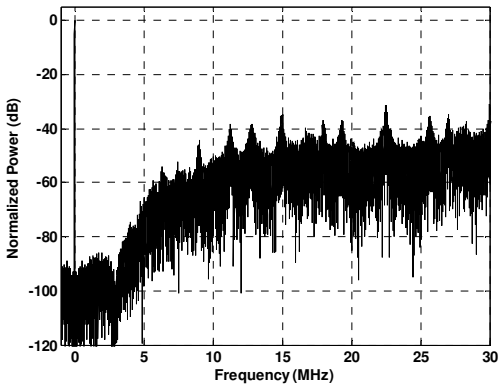


Fig. 27 – ΣΔM CRFB3-90 MHz amplitude to time converter output signal normalized spectrum for a DC (plus noise) input signal.

The same signal with variable amplitude presented in Fig. 20 was used to test the described ΣΔM. An excerpt of both input and modulated output signals are shown in Fig. 28 and Fig. 29 for the normal and CRFB ΣΔM respectively, in time domain.

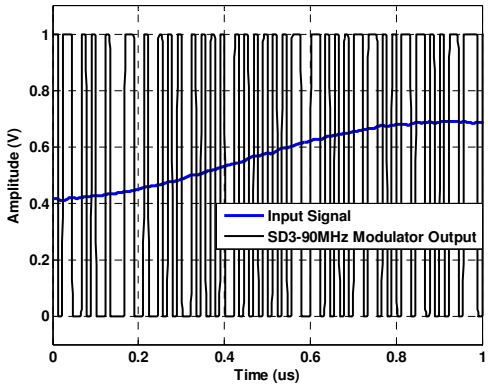


Fig. 28 – Variable amplitude input signal and - ΣΔM SD3-90 MHz amplitude to time converter output signal in time domain.

In this case, it is visible in the periods of faster switching that the pulses have a minimum duration, which is equal to half the period of the sampling frequency. Since both ΣΔM structures use the same sampling frequency, the pulses minimum duration is equal.

The differences rely in the density of these pulses for the same time frame, which is more evident in the frequency domain.

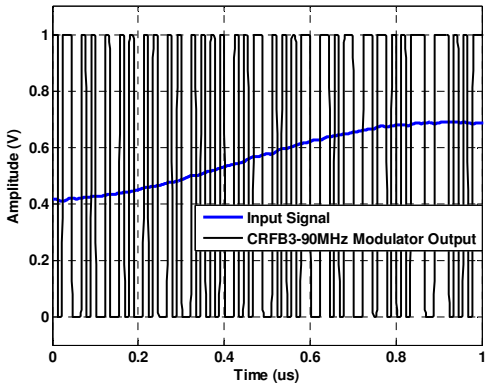


Fig. 29 – Variable amplitude input signal and - ΣΔM CRFB3-90 MHz amplitude to time converter output signal in time domain.

The normalized spectrum is depicted in Fig. 30 and Fig. 31 for the normal and CRFB ΣΔM respectively, showing a wider noise free region of the CRFB structure, corroborating the prior description.

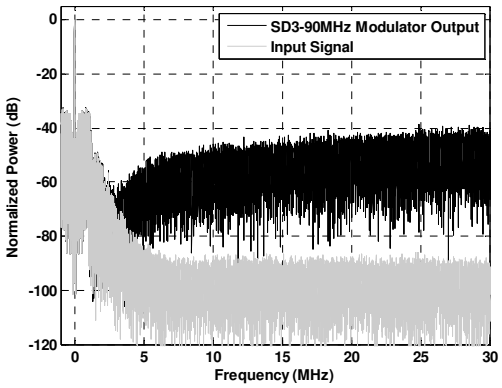


Fig. 30 – Variable amplitude input signal and output signal of the ΣΔM SD3-90 MHz amplitude to time converter in frequency domain

Now, following this brief introduction of some types of PWM and PDM, we will now compare their spectrum noise performance. For that, we measured the approximated bandwidth at which the switching noise was lower than -80dBc, which is equivalent to

roughly 13 effective number of bits (ENOB) of a regular Nyquist ADC. The bandwidth values obtained for several PWM and ΣΔM are presented in Table 1.

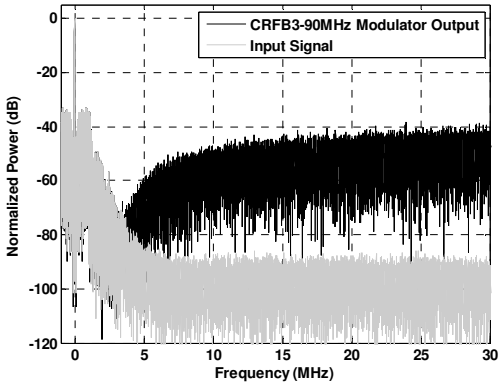


Fig. 31 – Variable amplitude input signal and output signal of the ΣΔM CRFB3-90 MHz amplitude to time converter in frequency domain

Table 1 – Envelope modulator bandwidth @ -80 dBc of switching noise.

Modulator	BW @-80 dBc (MHz)
PWM 10MHz	5.0
PWM 15MHz	7.5
PWM 30MHz	15.0
SD3 90MHz	2.5
SD3 150MHz	3.5
CRFB3 90MHz	3.5
CRFB3 150MHz	5.0

These figures indicate that (not considering the implementation differences and difficulties) the PWM is capable of having a wider noise free region. Regarding the ΣΔM, as expected, both the sampling frequency increase and the structure modification improved the noise free region.

Using these bandwidth values, the output modulated signal was recovered by two ideal rectangular lowpass filters (bandwidth of 2.5 MHz and 4 MHz) and compared with the input signal. This comparison was made with the calculation of the normalized mean squared error (NMSE), between both signals, whose results for the selected modulators are presented in Table 2.

Table 2 – Normalized mean squared error of the modulated signal after being recovered by a 2.5 MHz and 4 MHz BW square lowpass filter.

Modulator	NMSE (dB) 2.5 MHz	NMSE (dB) 4 MHz
PWM 10MHz	-53	-54
PWM 15MHz	-54	-54
PWM 30MHz	-54	-54
SD3 90MHz	-51	-39
SD3 150MHz	-55	-53
CRFB3 90MHz	-51	-48
CRFB3 150MHz	-53	-53

The filter bandwidth of 2.5MHz was selected so that the NMSE was lower than -50 dBc for all the modulator types. The best performance was obtained for the PWM and higher sampling frequency ΣΔM. When the filter bandwidth increase, the performance of the ΣΔM with 90 MHz sampling frequency degraded, because the switching noise was allowed to enter in the recovered signal, degrading it.

As an example, in Fig. 32, Fig. 34 and Fig. 33 it is depicted a few examples of the comparison between the input and recovered signals for selected modulators (the delay between the signals was not compensated in the ΣΔM).

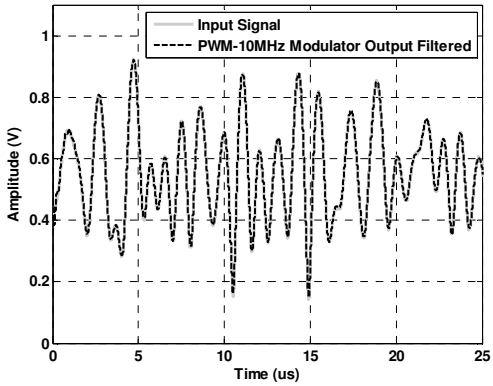


Fig. 32 – Variable amplitude input signal and the modulated version (by a PWM-10MHz amplitude to time converter) after being recovered by a 2.5 MHz rectangular lowpass filter.

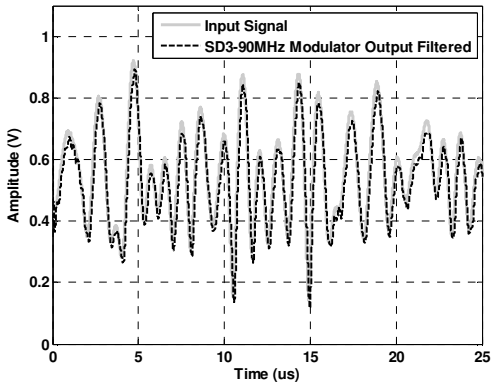


Fig. 33 – Variable amplitude input signal and the modulated version (by a ΣΔM SD3-90MHz amplitude to time converter) after being recovered by a 2.5 MHz rectangular lowpass filter.

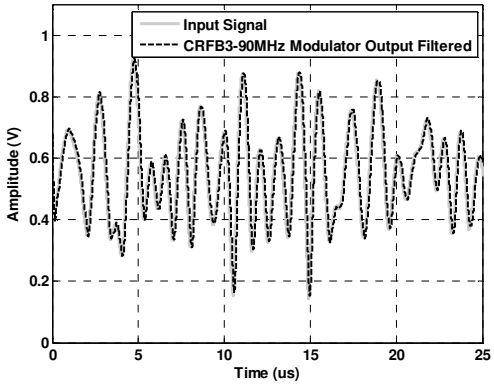


Fig. 34 – Variable amplitude input signal and the modulated version (by a ΣΔM CRFB3-90MHz amplitude to time converter) after being recovered by a 2.5 MHz rectangular lowpass filter.

3.2 Single-ended Switched-mode Power Amplifier

The power amplifier (PA) is the last active amplification stage in the RF-CAB transmitter, Fig. 18. As its denomination indicate, this amplifier deals with a considerable amount of power, so it is important to optimize its efficiency, in order to minimize the overall power consumption. Therefore, among the several PA classes, the ones that provide the best efficiency are the switched-mode ones (D,E and F) and their variants [50]. The operation of these amplifiers is strongly non-linear, not being very useful to amplify RF signals with slow varying envelope. However, as we have previously described, in the RF-CAB, the signal envelope coding combined with the constant envelope phase modulated RF carrier provides a burst signal at the amplifier input. This signal is ideal for the SMPA operation, because it is either OFF, where the SMPA is shutdown, or ON forcing the SMPA to operate at its most efficient condition.

In Fig. 35 is depicted a general simplified schematic of a FET based SMPA.

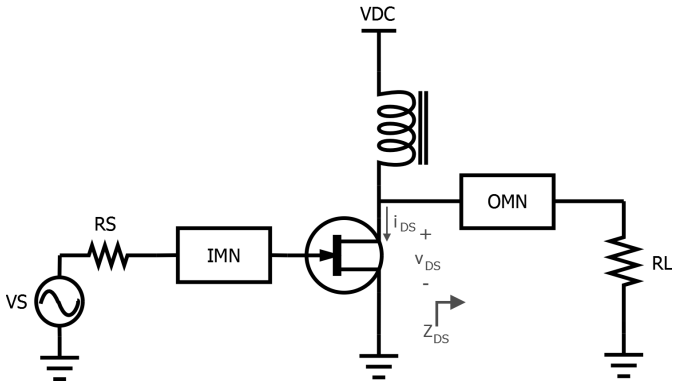


Fig. 35 – General Single-ended Power Amplifier simplified schematic.

The signal source is connected to the gate of the FET through an input matching network (IMN), which matches the source output and gate impedances. At the drain of the FET, a RF choke provides the DC output bias, preventing as well the RF signal to flow into the DC source (AC short-circuit). The FET drain is also connected an output matching network (OMN) that has double function. It matches the drain and load impedances at the designed fundamental frequency and also provides the necessary impedances at the fundamental and harmonics required to implement the desired SMPA class, as indicated in Fig. 36. The purpose of the harmonic load matching is to shape both the FETs current and

voltage, so that they do not overlap at any time instant, ideally guaranteeing that the FET has no power dissipation.

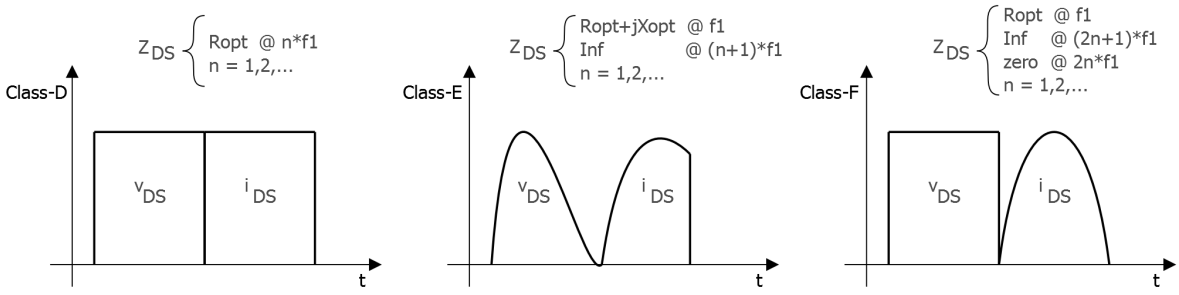


Fig. 36 – Switched-mode power amplifiers transistor waveforms and output impedance requirements.

The resistive Class-D in our case is of no use, because the SMPA output will be connected to the BPF, which will act as a reactive load to the fundamental and harmonics and any resistive element place in the OMN will degrade the efficiency. Therefore, since the Class-E and F are ideally 100% efficient, either one would a good choice from the system architecture perspective.

3.3 Bandpass Filter

The bandpass filter connected at the SMPA output is the responsible for the recovery of the smooth envelope lost during the amplitude to time conversion. However, before deciding the characteristics, it is important to describe some of the options available to implement this block [54].

Starting with the BPF transfer function, Fig. 37 depicts the amplitude frequency response of a normalized filter and associated major parameters. These can be divided in the ones related with the passband (BW_p) and the stopband (BW_s). Regarding the passband, it should be centered around the BPF central frequency f_0, the maximum attenuation (insertion loss, *IL*) must be defined, as well as the maximum ripple, *Ar*. Depending on the filter topology the passband might be defined as the bandwidth where the attenuation is smaller than the ripple in band or at 3dB below the insertion loss if the ripple do not exist. In the stopband, this bandwidth is defined as the one where the minimum attenuation (*As*)

is achieved. The ratio between the stopband and passband defines the transition band and is a very important parameter for the RF-CAB architecture.

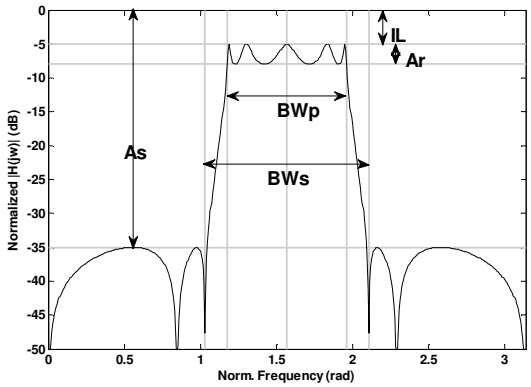


Fig. 37 – Bandpass filter amplitude frequency response associated parameters.

Depending on the filter type some of the parameters might not be necessary or might have different definitions. Nevertheless, it is mandatory to verify the most important characteristics in order to select the most suitable filter type for a specific application. The normalized amplitude frequency response of some of the most common filter approximations is presented in Fig. 38. As an example, the Butterworth has a flat passband response, but has a longer transition band. On the other hand, the elliptic has shorter transition band, but has ripple in both passband and stopband. Therefore, some trade-offs in the design must be assumed when the filter type is selected.

3.4 Architecture System Design

3.4.1 Amplitude to Time Converter and Input Signal Selection

The foremost objective of this work is to test and model the RF-CAB transmitter. Therefore, in order to use the ATC options presented in Chapter 3.1 we must select a dynamic signal with a variable envelope that the ATC can efficiently code. In Table 3, it is presented the channel bandwidth and the peak to average power ratio of several commercial standards.

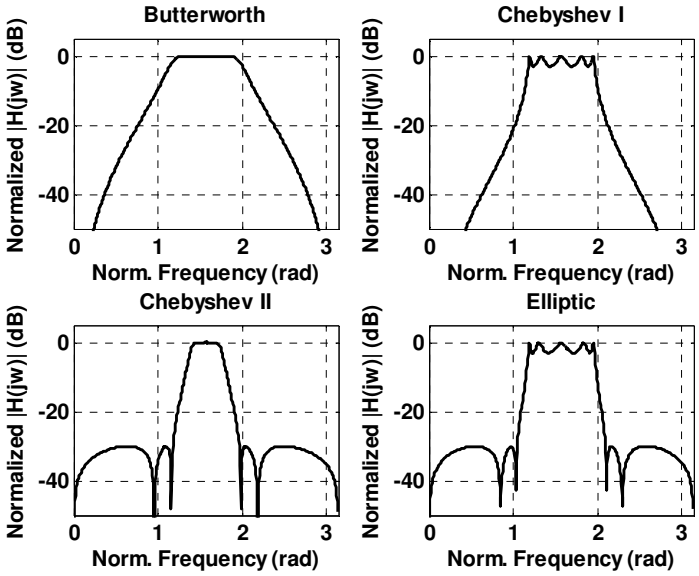


Fig. 38 – Amplitude frequency response of several bandpass filter approximations.

Table 3 – Peak to Average Power Ratio and Channel Bandwidth of several standards.

Standard	PAPR (dB)	BW (MHz)
GSM	0.0	0.2
EDGE	3.5	0.2
WCDMA	4	5
CDMA2000RV	6	1.2288
WiMAX	[8 - 12.5]	[1.25 - 20]
LTE DL	[7 - 10]	[1.4 - 20]
LTE UL	[5.5 - 8]	[1.4 - 20]

The ATC will code only the envelope signal, whose bandwidth, depending on the standard characteristics (PAPR), might be several times the channel bandwidth. So, in order to use all the modulators presented in Table 1, we selected a signal with a relatively

low channel and envelope bandwidth. Therefore, the CDMA2000RV fulfills the requisites and was the selected one. The baseband normalized power spectrum is depicted in Fig. 39.

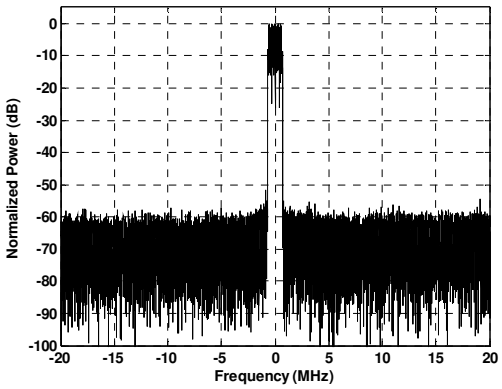


Fig. 39 – CDMA2000RV baseband signal power spectrum.

Using the RF-CAB system described by Fig. 18, we used the CDMA2000RV as input signal. The signal processing, including the splitting up in amplitude and phase, the amplitude codification, the RF carrier phase modulation and the multiplication of the two branches, was all done by software (Matlab). With this procedure, I plan to have the full control on the SMPA input signal generation. As an example, the normalized power spectrum of the carrier burst signal using some ATC's is presented in Fig. 40,Fig. 41 and Fig. 42, for a central frequency of 450 MHz.

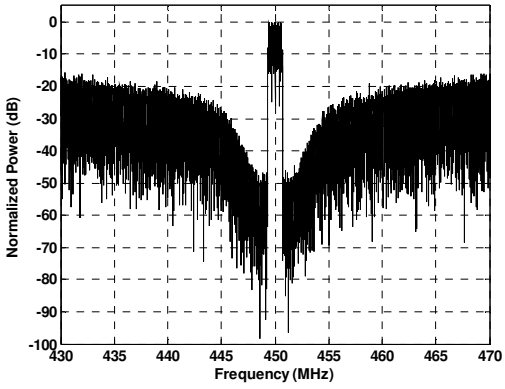


Fig. 40 – CDMA2000RV RF carrier amplitude-burst signal power spectrum with the envelope modulated by a 3rd order simple lowpass ΣΔM with 90MHz sampling frequency.

In order to complete the analysis, the SMPA input signal was generated, using all the modulators presented in Table 1. In a brief summary, the linearity (ACPR) and noise free

bandwidth achieved with all the ATCs is presented in Table 4. These figures not only indicate that the signal codification has been correctly implemented, but also corroborate the previous analysis were the best results were also obtained with the PWM.

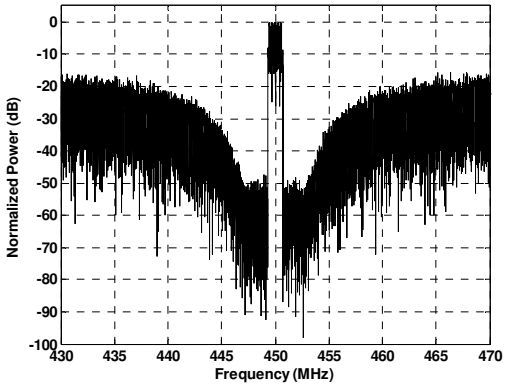


Fig. 41 – CDMA2000RV RF carrier amplitude-burst signal power spectrum with the envelope modulated by a 3rd order lowpass CRFB ΣΔM with 90MHz sampling frequency.

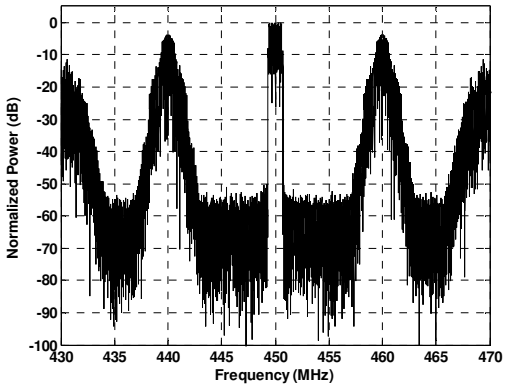


Fig. 42 – CDMA2000RV RF carrier amplitude-burst signal power spectrum with the envelope modulated by a lowpass PWM with 10MHz comparison frequency.

In the time domain, an excerpt of the RF Carrier amplitude-burst signal is depicted in Fig. 43, where it is visible the envelope modulator effect.

3.4.2 Switched-mode Power Amplifier Selection

As was previously indicated, since the Class-E and F are ideally 100% efficient, either of these two options is a good choice from the system architecture perspective. However, due to its OMN simplicity, the Class-F PA will be used.

Table 4 – Adjacent channel power ratio of the RF carrier amplitude-burst signal and switching noise free bandwidth.

Modulator	ACPR (dBc)	BW (MHz)
No modulator	61	-
PWM 10MHz	56	10
PWM 15MHz	57	15
PWM 30MHz	57	30
SD3 90MHz	51	5
SD3 150MHz	57	7
CRFB3 90MHz	54	7
CRFB3 150MHz	56	12

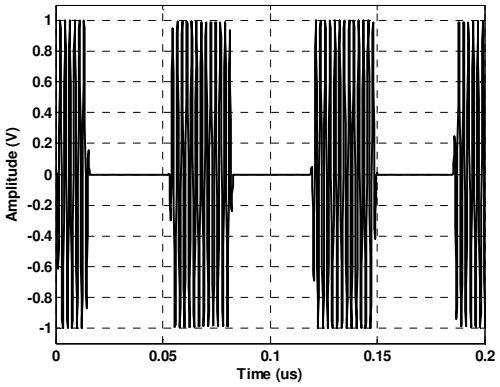


Fig. 43 – CDMA2000RV RF carrier amplitude-burst signal in time domain with the envelope modulated by a lowpass PWM with 10MHz comparison frequency.

3.4.3 BPF Design Requirements

Some of the BPF characteristics will be directly influenced by type of ATC used in the system. Two of the most important ones are the noise free bandwidth imposed by the envelope modulation, Table 4, and the relative power of the switching noise that must be removed, as illustrated in Fig. 42. All the design requirements are presented in Table 5.

The required passband (BW_P) is directly influenced by the minimum noise free bandwidth imposed by the ATC, Table 4. The stopband (BW_S) should be twice the passband, to relax the filter requirements . The stopband attenuation (A_S) must be higher than the highest noise relative power, Fig. 42, and the passband attenuation (Ar) as well as the insertion loss (IL) should be (reasonable) as low as possible. Regarding the central frequency, at system level, there is no limitations for its value, so once again any reasonable one is possible.

Table 5 – RF carrier amplitude-burst bandpass filter design requirements.

BPF Design Requirements	
f_0	Any
BW_P	5 MHz
BW_S	10 MHz
Ar	<0.1 dB
As	-60 dB
IL	<-0.1 dB

3.5 Conclusions

This system is 100% efficient and perfectly linear if the SMPA is perfect and also the BPF has an infinite attenuation in the rejection band. If that does not happen, the SMPA FET will dissipate some power and a certain amount of switching noise power will be dissipated in the load. Therefore, besides these constraints, it will be shown in Chapter 4 that some of the presented system level assumptions are too optimistic, as there are some circuit level interaction effects between the blocks, associated to their practical implementation, which are not possible to predict during the system design.

Chapter 4 – RF Carrier Amplitude-Burst

Following the system level design of the RF-CAB transmitter, in this chapter it is described how the described blocks and recommendations can be implemented in a practical circuit. The design and development are mostly centered in the amplification and filtering stages, where, a special attention is paid to the interaction between the SMPA and the BPF.

In the circuit development field, the theoretic analysis is essential to fully understand the circuit behavior dynamics. Since the practical implementation involves the use of real devices, whose impairments usually place strong limits to the forecasted theoretical performance, the circuit theory knowledge is crucial to develop circuit improvements or alternatives able to attenuate or even overcome the observed limits.

4.1 Ideal Circuit Level Design

4.1.1 Lowpass and Bandpass Buck Converter

It is widely known that the common DC-DC Buck converter, shown in Fig. 44, is a system that is ideally 100% efficient and linear.

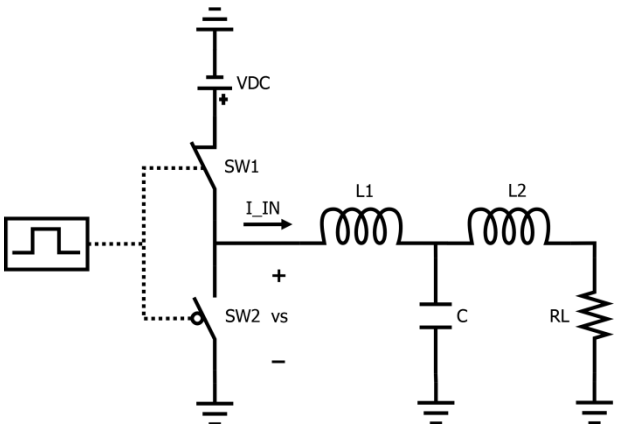


Fig. 44 – Ideal lowpass buck converter.

A direct current voltage (VDC) is applied to the lowpass filter (LPF) when the input control signal is ON. Having a voltage source, the LPF must have as first element a series

inductor, so that the LPF input voltage is integrated by the inductor. During the OFF period, the LPF is connected to ground, to keep the continuity of the inductor current. From this circuit it is possible to conceive its bandpass counterpart version, as depicted in Fig. 45.

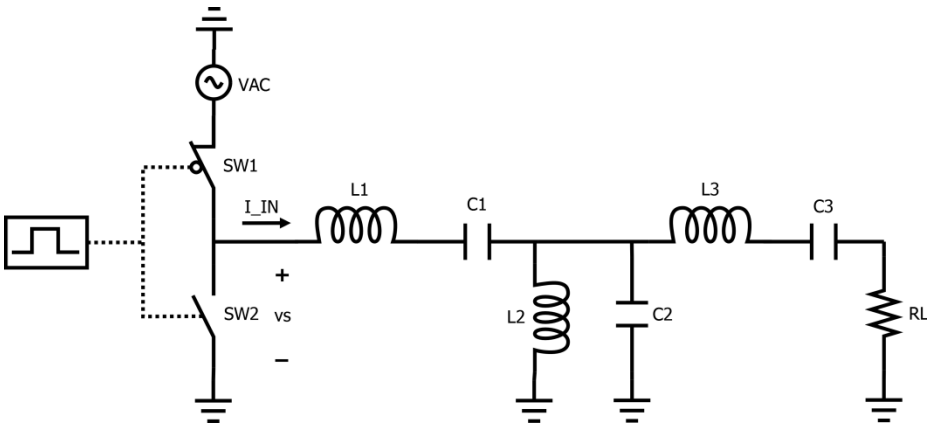


Fig. 45 – Ideal bandpass buck converter.

The VDC source and LPF are replaced by an alternate current voltage source (V_{AC}) and a BPF, respectively.

So, now, the voltage applied to the BPF is described by (5) during the ON periods and (6) during the OFF period of the input control signal.

$$v_S(t) = V_S \cdot \sin(\omega_C t) \tag{5}$$

$$v_S(t) = 0 \tag{6}$$

Similarly to its lowpass version, and due to similar reasons, since the AC source is a voltage one, the BPF must have an input series LC resonator, as for instance a T type filter. To distinguish the filters with series input resonator from the ones with parallel input resonator, the T type nomenclature will be used for the former.

At the BPF input, a burst sine wave is applied, which results in a BPF output whose amplitude is dependent on the pulse-width of the square wave that controls the switches. When this signal is ON, it will close SW1 (SW2 is open), connecting V_{AC} to the BPF.

When the control signal is OFF, SW2 closes (SW1 is now open) allowing the current continuity of the T type BPF.

The output linearity of this circuit (verified using a transient simulator) revealed to be excellent, where the output envelope is linearly proportional to the coded input signal envelope pulse-width and regardless of the pulse-width and only dependant on the out-of-band switching noise attenuation by the BPF. Similarly, the output power efficiency (defined as the ratio of the output channel power over the total DC power) is as high as the BPF attenuation in the rejection band. An example, for 40 dBc of attenuation, even if the input signal has a very low coding efficiency of 10% (ratio between the signal power and the switching noise power),[55], the RF-CAB efficiency is 99.91%, because the only dissipative element is the load. This proves that (i) there should be no fundamental reason why a RF-CAB transmitter should not reach the promised power efficiency values, and (ii) that when properly designed, the performance of such a transmitter architecture is not significantly affected by the input signal coding efficiency.

4.1.2 RF-CAB Transmitter and Bandpass Filter Duality

According to the canonical filter realization theory, a bandpass filter can have two dual topologies, the T and Π, depending on whether the out-of-band input impedance tends to a short or an open circuit.

The differences between these two topologies are very important in the RF-CAB transmitter architecture context , but since they may have the same prescribed frequency transmission response function, it would not be possible to discriminate each topology from only the measured S21(ω). Therefore, the S11(ω) is usually used for this purpose, where we can see that at ω→DC and ω→∞, while the T topology shows an open-circuit input impedance (series capacitor and inductor), the Π topology presents a short-circuit (parallel inductor and capacitor). Hence, they both have a S11(ω) reflection coefficient with amplitude equal to one, but with opposite sign.

As a consequence, due to the input series resonator of the T topology, the RF voltage can be abruptly changed in the input, while the current cannot. In the Π topology the opposite happens, due to the parallel resonator.

So, if the filter of Fig. 45 was replaced by the one of Fig. 46, this circuit - when implemented with real transistors - would provide extremely poor efficiency results.

Indeed, when each of the transistors turns ON, the Π filter faces a sudden input RF voltage change generating a huge current spike in the input resonator, something that cannot be accommodated without associated power dissipation in the transistor switches.

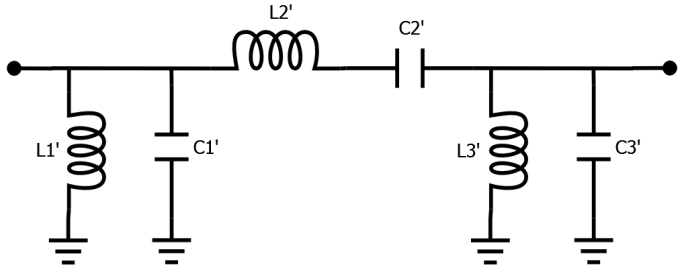


Fig. 46 – Bandpass filter Π topology.

The explanation for this malfunctioning is as follows. When the filter of Fig. 45 was changed by its dual, the RF-CAB transmitter with only the filter change corresponds to an incomplete dual transformation. It is necessary to proceed with the remaining components' transformation. From a theoretical point of view, the required steps are:

1st - Change the BPF to its dual (T to Π)

2nd - Change the voltage source to its dual (current)

3rd - Change the series switches to parallel ones

4th - Change the parallel switches to series ones

After these changes, the final dual circuit is presented in Fig. 47. The operation of the switches is similar to the previous dual system but, behaving now as an ideal current source. The filter is charged with a constant current and the voltage at its input will gradually adapt. This ideal system, in the same conditions as its dual, described in Chapter 4.1.1, guarantees the same efficiency and linearity performance.

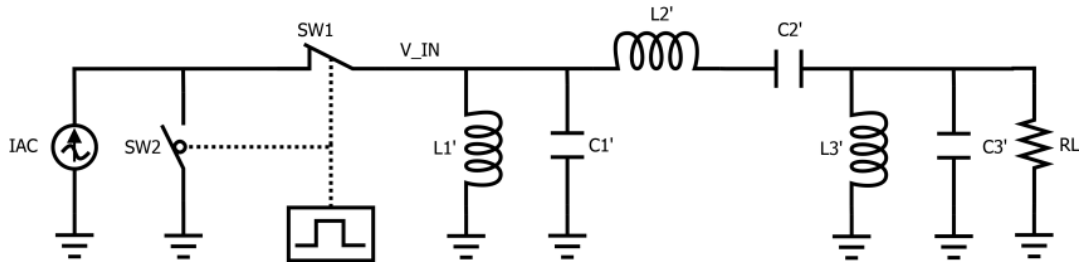


Fig. 47 – RF-CAB transmitter with AC current source.

4.1.3 Ideal Load Modulation

In this Sub-Chapter the impact that burst signals cause on the impedance presented to the switches by an ideal BPF or, in a practical implementation, to the SMPA will be object of study. It will also be described the design requirements that guarantee the RF-CAB maximum efficiency and linearity.

We started by assuming that the signal described in (5) carries a continuous-time envelope $V_m(t)$, that is completely reconstructed by the filter (which presents a 1:1 impedance transformation ratio) so that,

$$V_m(t) = V_S \cdot \delta(t) \tag{7}$$

where $\delta(t)$ is the time-varying pulse-width of the pulsed-wave modulated envelope or the duty-cycle of a fixed frequency square wave. If the filter is terminated by a resistor R_L, the output power will be,

$$P_{out} = \frac{1}{2}\frac{\left\langle V_m(t)^2 \right\rangle}{R_L} = \frac{1}{2}V_S{}^2\frac{\left\langle \delta(t)^2 \right\rangle}{R_L} \tag{8}$$

in which $<V_m(t)^2>$ stands for the averaged square value of $V_m(t)$.

In a succession of periods of the pulsed-wave, for which the envelope is approximately constant, so that $\delta(t) = \delta$, this output power equals,

$$P_{out} = \frac{1}{2}\frac{\left\langle V_m(t)^2 \right\rangle}{R_L} = \frac{1}{2}V_S{}^2\frac{\delta^2}{R_L} \tag{9}$$

If the filter is assumed passive and lossless, then energy conservation determines that its input power, or the energy it receives per period,

$$P_{in} = \frac{1}{2}\frac{V_S{}^2}{R_{in}}\delta \tag{10}$$

must equal P_{out}. But, this can only be possible if the filter input resistance, R_{in}, varies with the duty-cycle according to,

$$R_{in} = \frac{R_L}{\delta} \tag{11}$$

which is consistent with the result derived by Kim [56] for a particular RLC series resonator, but extends this result by proving that the filter input resistance variation is independent of the particular amplifier or filter realizations, but inherent to the system architecture itself.

Rigorously speaking, what this shows is that the real part of the net input impedance presented by the filter during the ON-state, i.e., when it is driven by the active amplifier, must equal R_L/δ. It does not provide any guarantee that the filter input impedance is purely resistive, that such a R_{in} is constant during the ON-state nor does it say anything about the input resistance at the OFF-state. As a matter of fact, in the OFF-state, the filter input impedance loses its natural significance – such R_{in} would be negative as the filter no longer behaves as a load but as a source because of the BPF stored energy – reason why we will assume in this chapter that R_{in} is only the filter input resistance at the ON-state, unless otherwise stated.

4.1.4 Real BPF Load Modulation

In the previous Sub-Chapter, the BPF impedance variation was analyzed considering a BPF with infinitesimal bandwidth. However, it is important to verify the impact of real component models in the impedance variation, even if they have ideal behavior.

The previous analysis is now extended assuming that the filter is a series LC resonator followed by a parallel LC resonator or, in general, any bandpass filter of bandwidth BW (given in Hertz) whose first element is a series LC resonator. Therefore, its equivalent dominant pair of conjugate poles, p_1 and p_1^*, $[(s- p_1)\,(s- p_1^*) = s^2+(\omega_0/Q)s+ \omega_0^2]$, is given by,

$$p_1 = -\lambda \pm j\sqrt{\omega_0^{\,2} - \lambda^2} \tag{12}$$

in which ω_0 stands for the LC resonance frequency – the BPF central frequency – and λ – the resonator damping factor – is related to the BPF loaded quality factor,

$$\lambda = \frac{\omega_0}{2Q_L} = \pi \cdot BW \tag{13}$$

The poles p_1 and p_1^* are complex when $\lambda<\omega_0$, which is the case when the filter is under-damped, with a high Q (small bandwidth compared with the central frequency). Accordingly, and assuming the filter transient response is determined by its single pair of dominant conjugate poles, the transient response of the input current of our BPF, when excited by a step sinusoidal voltage given by (5), located at its central frequency –so that its input current can be considered in phase with the applied voltage and so the impedance can be approximately resistive – will be,

$$i(t,\tau) = \left(I_i \sin(\omega_0 t) - I_f \sin(\omega_0 t)\right)e^{-\lambda\tau} + I_f \sin(\omega_0 t) \tag{14}$$

where I_i and I_f are the initial and final envelope current values, respectively, and t and τ represent the RF signal short time-scale and the pulsed waveform long time-scale, respectively.

So, when this filter is excited by a sine wave multiplied by a pulse train of constant duty-cycle, δ, and repetition frequency $f = 1/T$ much higher than its bandwidth, BW, i.e.,

$$f \rangle\rangle \frac{1}{2\pi}\frac{\omega_0}{2Q_L} = \frac{1}{2} \cdot BW \tag{15}$$

$v_L(t,\tau)$ will be approximately equal to $V_L * sin(\omega_0 t)$ and its input current envelope will be approximately equal to an asymmetric triangular wave, evolving from I_{min} to I_{MAX}.

Therefore, after some manipulation of (14), we have,

$$i_{on}(\tau) = \frac{V_S}{R_L}\left(\frac{e^{-\lambda(1-\delta)T} - 1}{1 - e^{-\lambda\delta T}e^{-\lambda(1-\delta)T}}\right)e^{-\lambda\tau} + \frac{V_S}{R_L} \qquad for\ 0 < \tau < \delta T \tag{16}$$

So, the general BPF input impedance (only defined during the input signal ON period) can be calculated by dividing *Vs* (constant value) by (16),

$$R_{in}(\tau) = \frac{V_S}{i_{on}(\tau)} = R_L \frac{1 - e^{-\lambda T}}{(e^{-\lambda(1-\delta)T} - 1)e^{-\lambda\tau} + 1 - e^{-\lambda T}} \tag{17}$$

This input resistance varies between,

$$R_{in\,\min} = R_L \frac{1 - e^{-\lambda T}}{1 - e^{-\lambda\delta T}} = R_L \frac{1 - e^{-\pi \cdot BW \cdot T}}{1 - e^{-\pi \cdot BW \cdot \delta \cdot T}} \tag{18}$$

and

$$R_{in\,MAX} = R_L \frac{1 - e^{-\lambda T}}{e^{-\lambda(1-\delta)T} - e^{-\lambda T}} = R_L \frac{1 - e^{-\pi \cdot BW \cdot T}}{e^{-\pi \cdot BW\,(1-\delta)T} - e^{-\pi \cdot BW \cdot T}} \tag{19}$$

A simple simulation example using ADS® with an elliptic filter of 3MHz bandwidth, terminated with a 50Ω resistor and driven with a 33.(3)MHz pulsed wave was conducted and its results compared in the Table 6, with the estimates of (18), (19). These results prove that these estimates are very good in the whole duty-cycle range. As can be easily seen by inspection, not only the estimates for δ=0 and δ=1 are exact, but also the values of R_{inmin} and R_{inMAX} tend to R_L/δ - (11) - when the filter bandwidth tends to zero.

In fact, the ADS® simulation example evidences another important aspect of (15). As previously mentioned, when a burst sine wave is applied to a series LC resonator, its input current will only be a triangular wave if the pulse train envelope frequency is strongly attenuated by the LC resonator. However, in the presented example, the 33.(3) MHz pulsed wave is not that much higher than half the BPF BW (approximately 20x) and still, the obtained impedance corroborates the presented theory. Since the elliptic filter imposes at the pulse train envelope frequency more than 60 dB of attenuation, it guarantees that the BPF input current has a triangular wave shape. So, (15) should be interpreted as the attenuation that the BPF must apply to the pulse train envelope frequency and its harmonics. Similar results can be achieved with lower coded envelope frequencies, as long as the filter attenuation is high at those frequencies.

This procedure is also in line with the conclusions presented by Zverev in [57], where it is shown that, for narrow band filters, the envelope analysis provides a very good approximation to the filter analysis.

Additionally, the previous analysis was presented for a static input signal with fixed coded envelope frequency and variable duty-cycle. However, if a dynamic signal is used, the coded envelope consists of pulses with variable density. In spite of these differences, and as long as its lowest instantaneous frequency fulfills (15) or is strongly attenuated by the BPF, the filter input current is an increasing ramp during the ON periods and an decreasing ramp during the OFF periods. This behavior is independent of the envelope codification method (PWM, ΣΔM,...) or of its coding efficiency.

Table 6 – Filter input resistance simulated vs calculated.

Duty-Cycle	Method	R_{inMAX} (Ω)	R_{inmin} (Ω)
δ = 10 %	Simulation	581	385
	Theory	569	441
δ = 25 %	Simulation	233	166
	Theory	223	180
δ = 50 %	Simulation	110	87
	Theory	107	93
δ = 75 %	Simulation	68	61
	Theory	69	64

4.2 Circuit Implementation

Although the circuit of Fig. 45 implements the RF-CAB (Fig. 18), where the envelope modulator and the modulated RF Carrier can be connected to the input control signal and

the V_{AC} source, respectively, a direct practical implementation is not easy to develop. In order to overcome these difficulties, it is possible to slightly change its configuration, as depicted in Fig. 48. The AC voltage source is replaced by a DC one and its phase information incorporated in the input control signal. The burst signal is now obtained by multiplying a priori the RF_CARRIER (output of the phase modulator), by V_PULSE (output of the envelope modulator) and applied to the switches. When this burst signal is ON and above zero, it will close SW1 (SW2 is open), connecting V_{DC} to the BPF for half of the cycle of the RF carrier. In the other half, the signal is below zero, so SW2 closes (SW1 is now open), providing a zero voltage to the BPF input. When the burst signal is OFF, (SW1 is open) SW2 closes, and stays closed for the whole time of the OFF period, providing the required current continuity of the T type BPF. If the composite input signal is a complex dynamic signal having both phase and amplitude modulation, the V_PULSE will be the coded version of the envelope amplitude (by a ΣΔM or PWM) and the RF_CARRIER will be a constant-envelope phase-modulated RF carrier.

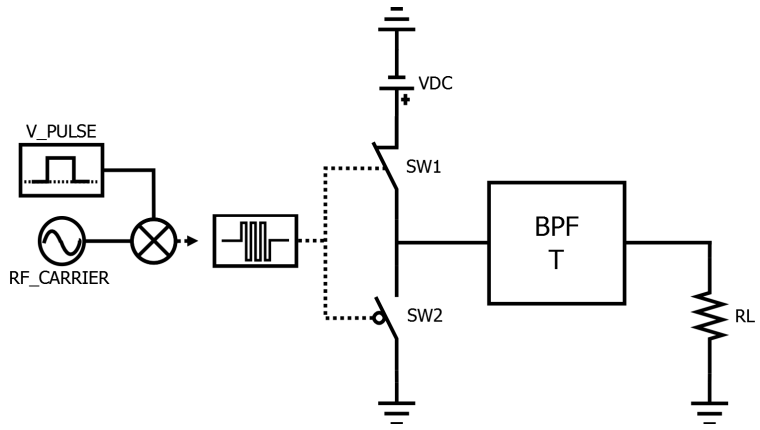


Fig. 48 – Bandpass buck converter with DC power source.

Despite their differences, these two circuits, Fig. 45 and Fig. 48, are perfectly equivalent and so produce an equal final outcome (in both linearity and efficiency).

4.2.1 Switched-mode Power Amplifier Selection

The next step is to select an appropriate PA that could efficiently implement in practice the functions provided by the switches of Fig. 48. As stated in Chapter 3.2, the PA should be selected among one of the switched-mode classes (E, F). Being this circuit very similar

to a pure Class-D in a totem-pole configuration, this amplifier would be the natural choice for the SMPA. However, it is hard to achieve high efficiency values at RF and microwave frequencies - due to the switching losses in both transistors (induced by their drain-source capacitance) [58] –, which has impeded the direct application of this architecture to high power amplification. Therefore, the solution is to use the single-ended Class-E or F in the implementation. But, as it will be shown, these options are not perfect. Nevertheless, due to their analysis simplicity, the Class-F will be selected.

The basic equivalent circuit of these unipolar amplifiers is depicted in Fig. 49, where a MOSFET is replaced by an ideal switch, SW. For simplicity, the output matching network required to implement a Class-E or Class-F is not included. During the ON period, when the input signal is a continuous wave (CW), the BPF input impedance R_{in} (load impedance for the transistor), achieves its lowest value equal to R_L (11), since $\delta = 1$. When the input signal is in burst-mode, $\delta < 1$, R_{in} increases. As a consequence, the transistor load will always be higher than R_L. So, amplifying the input signal to a level that guarantees that the SMPA is kept in voltage saturation for R_L, assures that, for the other values of R_{in}, the SMPA is always kept the voltage saturation mode. Therefore, the SMPA provides the desired AC voltage source as it was required by the usage of a T-type BPF.

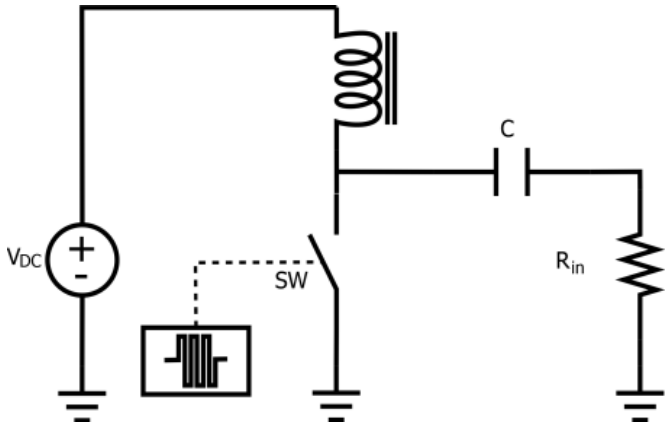


Fig. 49 – Switched-mode power amplifier basic equivalent circuit.

During the OFF period, the transistor (switch) stops switching and stays open. The RF bias Choke, which during the ON period was providing DC current, will still act as a current source (as the inductor current cannot change abruptly) that will disappear shortly after the transition from ON to OFF. The BPF will now seek for a low RF impedance path to ground (so that the current continuity is preserved), but it only finds a low value DC

current source with a high impedance at RF. So, the equivalent circuit model for the RF signal components is presented in Fig. 50 (the DC current source is not included for simplicity). It is thus evident that the unipolar switched-mode amplifier cannot fulfill the BPF OFF period condition (low impedance to ground) by itself, being necessary to introduce a new element in the circuit. This element is a flywheel switch that will short-circuit the BPF input to ground during the OFF periods of the input signal. Fig. 51 depicts the RF-CAB circuit with this new element (SW2), where the SMPA is represented by its RF equivalent circuit model, depicted in Fig. 50. Also the major component and design impairments (addressed in detail in the next sub-Chapter) are included.

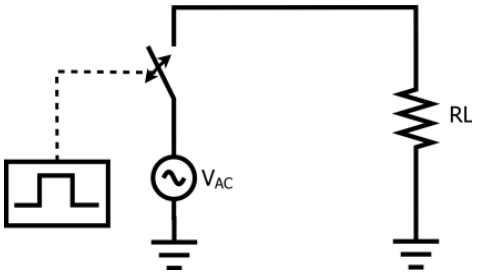


Fig. 50 – Switched-mode power amplifier simplified equivalent circuit model with an AC voltage source.

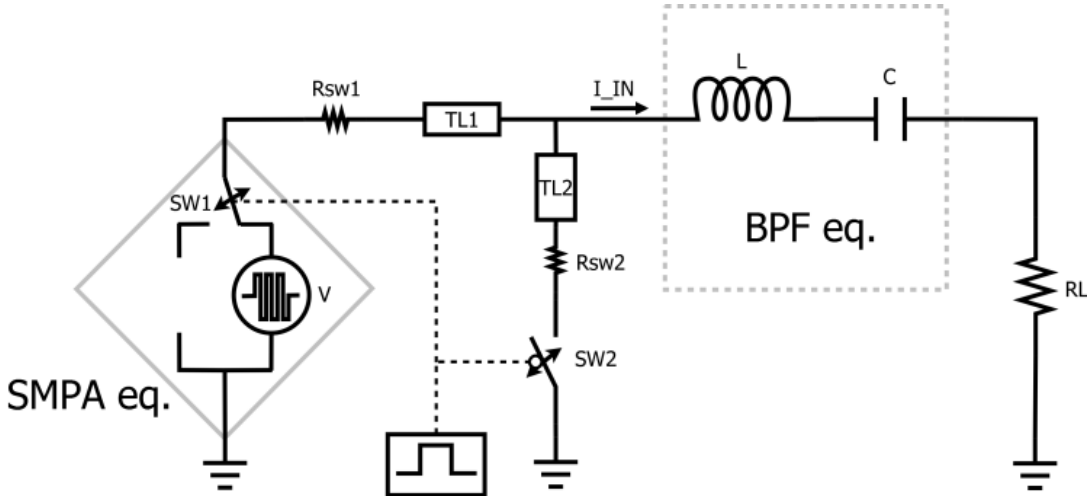


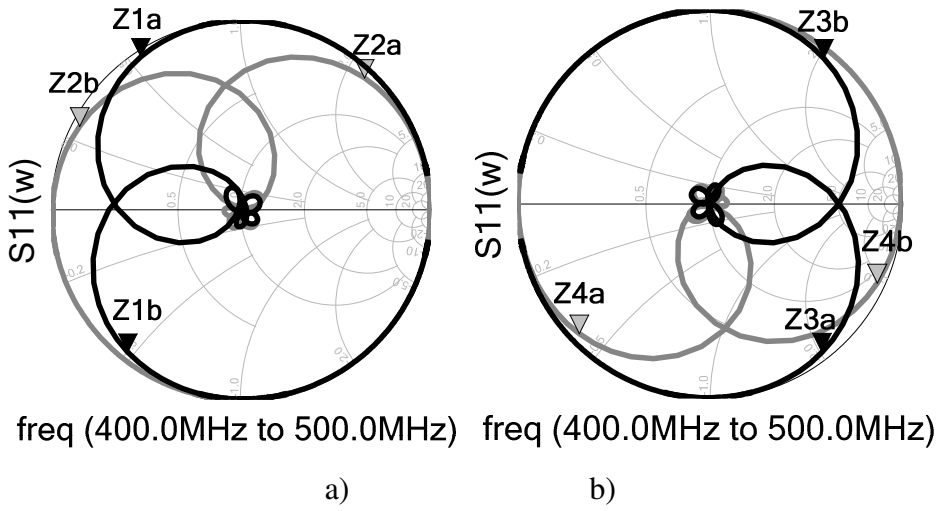
Fig. 51 – RF carrier amplitude-burst transmitter equivalent circuit with block impairments.

4.2.2 Power amplifier interaction with BPF

In the previous sub-Chapter, it was shown that the filter selection must be carefully carried out to guarantee the system performance. However, in practice, sometimes it is

hard to fulfill all these requirements. For instance, although the examples presented previously, were based on LC lumped filters (useful to exemplify the differences between them), these are seldom used at microwave frequencies. Indeed, cavity, surface acoustic wave (SAW), bulk acoustic wave (BAW), among others are alternatively used in wireless systems making it harder to identify the corresponding basic T or Π topology. So, it is important to have an indirect measurement that can help in this process. As presented in sub-Chapter 4.1.2, the filter input reflection, S11(ω), has the required information.

As an example, the simulation of a 5th order elliptical LC T filter with a central frequency of 450MHz, 5MHz of pass-band and 10MHz of stop-band is shown in Fig. 52 (a), while, in Fig. 52 (b), the same simulation is presented for the Π type version of the same filter. The graphs present the evolution of the S11(ω) from 400MHz up to 500MHz.



a) b)

Fig. 52 – Simulated BPF input reflection, $S_{11}(\omega)$. (a) T-Type filter [Z1] and T-Type filter+40º TL [Z2]. (b) Π-Type filter [Z3] and Π -Type filter+40º TL [Z4].

When the curves trajectory of Fig. 52 (a) Z1 are close to the Smith chart centre (as expected with a small variation), this corresponds to the pass-band frequencies of the filter. However, it is obvious the large variations seen in the transition and cut-off high and low bands. In these two frequency ranges, the S11(ω) follows opposite trajectories in the Smith chart. This simulation was performed with an ideal zero length connection between the source and the filter, using a T type filter. However, in practice, the presence of a transmission line (TL) with a certain length in between is mostly certain. So, if we insert it, we will observe a clockwise rotation in the S11(ω), with the increase of the TL length, as

shown in Fig. 52 (a) Z2 for an additional TL of 40º. It can be shown that if the TL has a quarter wavelength at central frequency, the S11(ω) characteristic of a Π filter (Fig. 52 (b) Z3) will be similar to the respective dual T type with the quarter wavelength TL, due to its impedance inverter characteristics.

Therefore, a RF-CAB transmitter can use any type of filter, as long as the S11(ω) at the voltage source output (in our case the SMPA) resembles the impedance characteristic of the T type filter. It is possible to determine the exact TL length, but its value is dependent on the filter characteristics and it is not unique because, after reaching the first solution it is possible to add half-wavelength to the TL length to have a full impedance rotation.

RF-CAB Power Efficiency

Now, the power efficiency analysis of the Class-F SMPA under the BPF+TL impedance variation is performed, because these two elements are the actual load of the SMPA and the previous filter analysis showed that it is possible to have a wide input impedance variation.

To do so, let's consider the transistor current-voltage (IV) characteristics based on a mosfet piece-wise model, as depicted in Fig. 53.

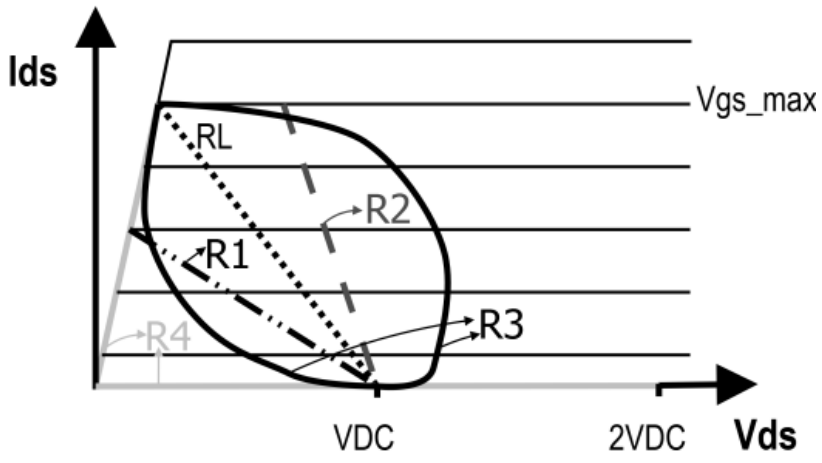


Fig. 53 – Class-F SMPA load line under different load impedances.

Since the Class-F SMPA is biased in Class-B, the small dotted load-line is the optimum to achieve maximum efficiency, which has been calculated to be *RL*. Considering that the Class-F has the harmonics shaping, its actual load line is *R4*. These load lines (*RL* and *R4*) are valid for a CW input signal with an amplitude of *Vgs_max,* infinite harmonics shaping

and for every BPF+TL, provided that the BPF has a 1:1 impedance ratio and the TL has a characteristic impedance equal to *RL*. The S11(ω), Fig. 52, corroborates this statement as the BPF+TL input impedance close to the central frequency does not significantly change for all filter + TL combinations.

However, as was previously observed, the input impedance in the other frequencies suffer from a significant change. Therefore, it is possible to relate the BPF+TL input current I_{inBPF} with the applied voltage V_S by the input impedance Z_{inBPF},

$$I_{inBPF}(\omega,\Omega)=\frac{V_S(\omega,\Omega)}{Z_{inBPF}(\omega,\Omega)}=Y_{inBPF}(\omega,\Omega)\cdot V_S(\omega,\Omega) \tag{20}$$

where ω is the pass-band frequencies and Ω the envelope frequencies. Since the input impedance can be considered constant at the filter passband, but not at the sidebands, it is possible to do the analysis taking into account the lowpass equivalent,

$$I_{inBPF}(\Omega)=Y_{inBPF}(\Omega)\cdot V_S(\Omega) \tag{21}$$

Let's see now what happens with the Class-F load line, when the input signal envelope is not constant. To accomplish that and for simplicity, we will consider that RF_CARRIER - Fig. 48 - is an unmodulated carrier and V_PULSE is a square wave with 10 MHz of fundamental frequency and variable duty-cycle (δ). Additionally, the filter input current can be calculated in time domain by translating the frequency multiplication (21) in a time convolution,

$$i_{inBPF}(t)=\int_{-\infty}^{+\infty} y_{inBPF}(\sigma)\cdot v_S(t-\sigma)d\sigma \tag{22}$$

Considering that the BPF+TL has an input impedance that resembles a T-Type filter (Fig. 52 (a)), *Z1a* and *Z1b* represent input impedances that are, not only complex conjugate, but also measured in the upper and lower bands equidistant from the central frequency of the filter. It can be proved that a filter with these characteristics has an input impedance (at the envelope) real and equal to RL/δ [56]. So, the load line that corresponds to this load change, falls in the *R1* area as shown in Fig. 52. The exact resistance value

depends on the envelope square wave duty-cycle, being coincident with *RL* when δ is 100% and coincident with the *Vds* axis (infinite value) when δ is 0%. The Class-F SMPA continues to be highly efficient with this load change, since it does not force the IV trajectory to enter in the active area.

When a TL is added, the input impedances rotate clockwise (Fig. 52 (a), *Z2*), as its length increases. In this case, the impedances at the same frequencies (*Z2a* and *Z2b*) are not complex conjugate. Therefore, the filter will have a complex lowpass equivalent response, which forces the input current (22) to be also complex, since the input voltage is real. As this model is a lowpass equivalent, this means that the phase of the BPF RF input current is not in phase with the input voltage RF source. The Class-F SMPA new complex load, forces an IV trajectory that is very difficult to predict. Yet, it will deviate the Class-F load line, Fig. 53, from its natural path (*R4*), to another (a possibility is *R3*) that will cross the active area, leading to an inherent power efficiency reduction.

If the TL has a quarter-wavelength, the T type BPF+TL resembles a Π type filter (Fig. 52 (b), *Z3*). The TL inverts the T type filter input impedance, which is now $RL*\delta$. The impedances at the same frequencies (*Z3a* and *Z3b*) are now complex conjugate, which means that (22) is composed by real quantities. Back to the Class-F load line, Fig. 53, the SMPA reaches its maximum efficiency when δ is 100% (load line coincident with *RL*). When the duty-cycle decreases, the load line enter the upper area (relatively to *RL*), but since the maximum *Ids* current is limited by the input signal (*Vgs_max*), the IV trajectory is forced to enter the active area, leading once again to power efficiency reduction. As a fact, when δ is close to 0%, the power efficiency is also close to 0%.

Lastly, when the TL is once again increased, *Z4* in Fig. 52 (b), since the impedance at the envelope is now capacitive, if a voltage source is used, the consequences are even worse than the case of *Z2* in Fig. 52 (a).

In summary, the previous analysis proves that, for burst signals, when a voltage source is used, the optimum BPF+TL combination is the one whose S11(ω) resembles the one of a T type filter.

4.2.3 Design and Components Impairments

The analysis performed up to this point proves that, as long as it is correctly implemented, this architecture has no fundamental limitations on either linearity or

efficiency. However, because it is also important to evaluate how the components or design imperfections, such as the ones modeled in Fig. 51, influence the system behavior, these will be enunciated below. The performance degradation caused by these impairments will be described in more detail in Chapter 4.3.

Design Impairments

a) Transmission lines (TL)

During the physical implementation, the presence of finite length transmission line connections, such as TL1 and TL2, is unavoidable to properly assemble the physical components. These undesirable short transmission lines will affect the circuit performance. TL1 moves the actual BPF presented to the SMPA from the desired T-type, and TL2 affects the BPF natural resonance frequency during the OFF periods, since it will act as an extra reactance present in the BPF's input resonator.

In presence of a short length of TL1 between the BPF and the SMPA, the equivalent voltage source amplifier is no longer terminated by an ideal T-type filter. Its load impedance for the switching frequency components (fundamental and harmonics of V_PULSE) ceases to be real and its reactance changes with the duty-cycle. So, not only the SMPA loses efficiency because its dynamic load-line is now traversing the transistor's active region (simultaneous high $v_{DS}(t)$ and $i_{DS}(t)$ in a FET), as the voltage applied to the BPF has a different value, depending on the duty-cycle of the modulated envelope, causing distortion.

Located in the flywheel path, TL2's effect is directly felt in the OFF period but indirectly impacts the SMPA ON period. During the OFF period, the BPF is left to its natural, un-forced, regime. So, the frequency of its natural response depends on its termination. Adding a short-length of transmission line terminated in a short-circuit– equivalent to a small inductor – between the FW transistor and the BPF input can be interpreted as an increase of the inductor of the input series resonator discussed on sub-Chapter 4.1.2. Consequently, ω_0 in (12) decreases, inducing a sliding phase shift between the instantaneous phase of this natural response and the RF_CARRIER reference phase. Therefore, at the end of the OFF period, and so at the start of the ON period, there will be a phase shift between the RF energy stored in the narrow-band BPF and the voltage to be forced by the SMPA. Similarly, to what was said to TL1, this corresponds to a shift in the

SMPA load impedance from its expected real value, causing further linearity and efficiency degradation.

From this analysis, it can be concluded that both TL1 and TL2 may have a dramatic impact in the RF-CAB performance. Fortunately, it will be shown that, in practice, their effects can be minimized if a careful attention is placed in their design and implementation. TL2 length must be minimized, while TL1 must be selected so that the BPF is seen by the SMPA as a T-type filter (presenting an ideal open circuit at the SMPA load reference plane for the lower and upper stop-bands).

b) Skew in the switches input signal

If the switches operate non-synchronously, two problems might occur. First, if SW2 closes before SW1 opens, the AC source will be short-circuited to GND causing a severe efficiency degradation. Second, if SW2 opens, before SW1 closes, the input BPF will be opened, not guaranteeing the input current continuity, which generates large voltage spikes. However, even though it is worth mentioning, this problem might be solved during the digital signal generation, by compensating the delay differences between the two paths.

Switch impairments

Although MEMS implementations could also be conceived, the switches in a real circuit are implemented, in the majority of the RF applications, with transistors. So, the impairments with larger impact are:

a) Non-zero internal resistance

The internal series losses of SW1, which can be mapped onto the ON-resistance of the transistor used to implement it, R_{on1}, will act as a voltage divider with the input variable BPF input resistance (11), causing a nonlinear behavior. The voltage envelope at the load is,

$$V_L = V_S \frac{R_L}{R_L + \delta R_{on1}} \delta \tag{23}$$

which will be nonlinearly dependent on the duty-cycle, and thus on the input signal amplitude.

b) Active region

Contrary to the desired triode-region, where the transistor is expected to operate as a switch, in the device's active region, the presence of simultaneous voltage and current leads to the well known transistor power dissipation, which naturally degrades the amplifier efficiency. Furthermore, in that region, the PA ceases to operate as the desired voltage source, and starts to behave as a current source, creating nonlinear distortion. The only way to obviate these detrimental effects is to assure that the transistor is always kept in its triode-region, guaranteeing that the SMPA load impedance is real and below the nominal R_L of maximum output power. As we have already seen when we discussed the transmission line impairments, this means that TL1 length must be specifically controlled to guarantee the desired filter type at the SMPA load termination reference plane.

c) Input bandwidth

The input signal that controls the switches might have rise and fall times that can be significant and different for each switch. The limited bandwidth can be caused by the switches' input capacitance and/or by the possible use of driver amplifiers necessary to properly amplify the input signal. Therefore, a wide enough bandwidth must be guaranteed for both the RF amplifier SMPA and flywheel driver amplifier chains. The value depend on the coded envelope spectral content. In the time domain, for the PWM, the modulator output signal is very similar to a variable duty-cycle square-wave, so a bandwidth equal to the 9th harmonic of the fundamental square-wave frequency guarantee that the rise and fall times are less than 4% of the wave period. Similar calculations can be done for the ΣΔM.

4.3 Efficiency and Linearity Analysis

4.3.1 Linearity

The distortion model previously developed, and depicted in Fig. 51, is now subjected to a dynamic simulation, so that its in-band and adjacent-band distortions can be revealed. Hence, the CDMA2000 signal with 1.23MHz of bandwidth is used, where the amplitude is modulated by a PWM with 10Mbps repetition rate. The BPF is a LC 5th order elliptic filter, centered at 450MHz, with 10MHz and 20MHz pass and attenuation bandwidths,

respectively. As is common practice in wireless communications, both time- and frequency-domain performance metrics were used. The former was characterized by the normalized mean squared error, NMSE, (independently for both amplitude and phase information as, in this architecture, these are separately processed) while the latter was evaluated through the adjacent-channel power ratio, ACPR. Table 7 summarizes the results for each of the described impairments.

Table 7 – RF-CAB linearity analysis of the output signal vs impairments.

Case	Impairment	ACPR (dBc)	NMSE PHASE (dB)	NMSE AMP. (dB)
A	No	54	-101	-73
B	TL1 10º	41	-56	-39
C	TL2 10º	41	-54	-42
D	R_{on1} = 4 Ω	46	-81	-31
E	R_{on2} = 4 Ω	47	-74	-31
F	TL2 10º ; R_{on1}	40	-54	-31
G	TL2 10º ; $R_{on1,2}$	40	-55	-43
H	$R_{on1,2}$	47	-71	-46

The reference result of Case A, presents the system linearity performance with no impairment, whose values serve as the base level for comparison with the remaining results.

The results of the other cases reflect the performance degradation imposed by the unavoidable impairments, as described in sub-Chapter 4.2.3. Among these, it should be noted that the transistor's *Ron* is always present. Therefore, it is not possible to eliminate its impact from the system. Regarding the transmission lines (TL), if the design is performed with hybrid or discrete components, their impact in the linearity must be considered, since, for instance, at 450MHz, 10º of TL is a cumulative extra PCB track of around 10mm (for

an ε_r of 4), which can easily come up in a layout. However, when an integrated solution is adopted, not only the physical dimensions are negligible when compared with the involved frequencies, but there is also an enormous increase in the accuracy and resolution of the design. Therefore the TL impairments may or may not be present in the system, depending on the specific implementation.

Based on the transistors available in the market, it was considered an internal series resistance for the switches of 4 Ω and a 10º TL was selected during the analysis.

Comparing the reference case with cases B and C, a performance degradation is observed, caused by the TL1 and TL2, respectively. This degradation is evidenced by the worse values of ACPR and NMSE. A similar situation occurs when R_{on1} and R_{on2} is considered in cases D and E, respectively. Observing these four cases, we conclude that with a careful design or in an integrated solution, as long as the TLs lengths are minimized or even the TLs are eliminated, the RF-CAB linearity performance has an upper limit imposed by the transistor's R_{on} and whose effect can be predicted by (23).

In the last three cases, F, G and H, a cumulative impairment effect is presented. As it can be seen, the influence of the parasitic TL is far more important than the one of the switches' internal resistance.

4.3.2 Efficiency

Regarding the efficiency, besides the load, the only elements that dissipate energy are the two transistors (switches in Fig. 51), in their ON-resistance and their active region, since the remaining elements are ideal, and thus non-dissipative. In order to verify the system power efficiency, a static test approach was used so that it would be possible to observe the power efficiency with duty-cycle changes (with the dynamic tests we only observe the average power efficiency). These tests consist in applying a non-modulated RF carrier multiplied by a square wave with 10 MHz of fundamental frequency. The duty-cycle is variable, but kept fixed during each of the system power efficiency calculations. These results are summarized in Fig. 54.

The top curve considers only the impairments associated with the SW1 (transistor's R_{on} – equal to 4 Ω – and its active region). At 100% of duty-cycle, CW, the efficiency is not 100% due to the R_{on} of the transistor. This impairment affects the performance of the system for the remaining duty-cycle values. But, when δ is lower than 30%, the absolute

value of the output power is quite low and the power dissipation in the active region (P_{ds}) has a larger impact, lowering the global power efficiency value. As already explained, every time the SMPA is switched ON, the phase and frequency mismatch between the SMPA input signal and the BPF natural oscillation will cause a stronger overlap in the voltage and current of Class-F transistor, increasing the power dissipation and leading to a power efficiency reduction. This happens during the initial RF Carrier cycles, after which, the synchronization is reacquired.

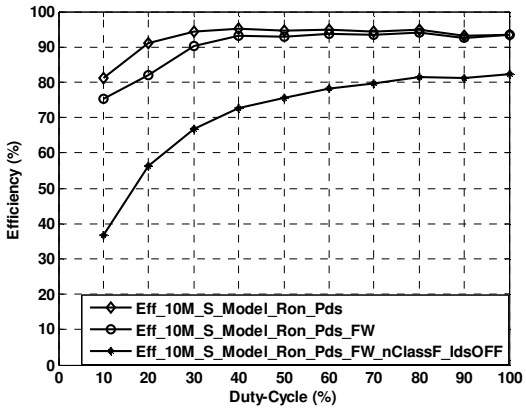


Fig. 54 – RF Carrier amplitude-burst transmitter efficiency vs Duty-Cycle.

When the SW2 (flywheel) R_{on} is considered – middle curve of Fig. 54 – the power efficiency is again affected more when the duty-cycle decreases. Since the OFF period is longer for lower duty-cycle values, the energy dissipated is higher in R_{on2}, relatively to the output power, causing a larger decrease of the power efficiency.

Before advancing to the analysis of the last curve of Fig. 54, it is worth noting that, in presence of a Class-F SMPA implementation, two additional sources of efficiency degradation must be considered. First, in the physical design, it is not possible to consider all the harmonics as is required in the ideal case, and so the maximum achievable power efficiency, η_F, is lower (82.3% for harmonics 2,3,4 and 6). Second, the transistor in the Class-F SMPA should be biased at cut-off, which ideally assures null I_{ds} current, when the input signal is OFF. However, due to the transistor's smooth turn-ON characteristics, a small quiescent I_{ds} value is always present near the threshold voltage, which leads to an inherent power dissipation during the OFF periods of the input burst signal.

Considering the energy ON and OFF during the instant period, T, of the envelope square wave, the load power as a function of the duty-cycle (δ) is,

$$P_L(\delta) = \frac{E_{ON} + E_{OFF}}{T} = P_{ON} \cdot \delta \tag{24}$$

Similarly, the DC power as function of the duty-cycle (δ) is,

$$P_{DC}(\delta) = \frac{E_{DCON} + E_{DCOFF}}{T} = \frac{P_{DCON} \cdot \delta}{\eta_F} + P_{DCOFF} \cdot (1-\delta) \tag{25}$$

which leads to a power efficiency of,

$$\eta(\delta) = \frac{P_L(\delta)}{P_{DC}(\delta)} = \eta_F \frac{P_{ON} \cdot \delta}{P_{ON} \cdot \delta + \eta_F \cdot P_{DCOFF} \cdot (1-\delta)} \tag{26}$$

Considering a DC power relation of 5% (value obtained as a compromise of measurement and simulation) between the OFF and ON periods, and combining (26) with the three previous impairments, the lower curve of Fig. 54 is achieved. As can be observed, a substantial efficiency degradation is visible, specially at the lower duty-cycle values.

4.4 Prototype Development

In order to validate the proposed theory, a proof-of-concept prototype was developed, whose blocks are described in the following Sub-Chapters.

4.4.1 Bandpass Filter

As previously stated, the BPF plays an important role in the system, guaranteeing that the output signal is free from the pulsed characteristics of the input signal. Although many times overlooked in the literature, this statement imposes not one, but two specifications on the BPF to be designed. The first one is the obvious frequency-domain transfer characteristic, in which the BPF should be transparent to the entire signal bandwidth, and opaque to the pulsed wave-form (its fundamental and harmonics). The second one, significantly subtler, is that the BPF input should present an input impedance that integrates the square wave voltage waveform into a small ripple input triangular current. This means that, beyond the input-output transfer characteristic, this input current

continuity condition determines that the BPF associated to the BPF-PA connection line input impedance must resemble the one of a high-Q series resonant circuit.

Thus, the BPF should have narrow bandwidth and small transition bands with high stop-band attenuation (at least 45 dB, found by simulation), i.e., $f_c \pm f_{sq}$ (where f_c is the carrier frequency and f_{sq} is the low frequency square wave, V_PULSE). Therefore, the used V_PULSE frequency, defines the main transfer-function characteristics of the filter. Considering that it could be possible to have a V_PULSE frequency as low as 5 MHz then, the stop-bandwidth of the BPF should be at least 10 MHz, in order to have a normalized transition band (relation between the stop-BW and pass-BW) with a practical value of 2, leading to a pass-bandwidth of 5 MHz. It is important to notice that this filter will be an integrant part of the whole amplifier. So, any loss of the filter will be directly reflected in both the output power and efficiency.

Considering a BPF insertion loss, *IL*, of -1dB, the input-output power relation will be 0.8, which immediately imposes a loss of 20% in the overall efficiency. So, to take profit of the efficiency improvement offered by this pulsed architecture, it is important to have very low BPF insertion loss.

From the canonical filter realization theory [54], the filters are composed by one or more resonators, whose individual characteristics have a strong influence in the filter performance. These resonators, in their ideal form, have the ability to store and deliver the energy without any losses. However, in real implementations some of the stored energy will be dissipated in the resonator itself, due to internal losses. Therefore, it is possible to define the resonator quality factor, valid for any resonator type and dependent on its physical characteristics, as the ratio of these two energies (27), [54],

$$Q = \frac{Energy\ \ Stored}{Energy\ \ Dissipated} \quad , per\ \ cycle \tag{27}$$

This parameter is also known as the unloaded quality factor since it is not dependent of any applied load. Additionally, when several resonators operate as a more complex filter, or a load is connected to the single resonator, a loaded quality factor is also possible to calculate and is defined by the ratio of the central frequency over the filter 3dB bandwidth, (28).

$$Q_L = \frac{f_0}{BW} \tag{28}$$

As previously stated, when the resonators are not ideal, they have some internal losses, which are the major cause of the filter insertion loss in the passband. It is possible to relate both the loaded (Q_L) and unloaded (Q_U) quality factors with the insertion loss at the central frequency f_0, (29).

$$Q_U = \frac{Q_L}{1 - 10^{\frac{IL(f_0)}{20}}} \tag{29}$$

Or, in a more general form (for all the spectrum), the insertion loss can be calculated as,

$$IL(f) = -10\log\left(\frac{1 + \left(2Q_L\frac{f - f_0}{f_0}\right)^2}{\left(1 - \frac{Q_L}{Q_U}\right)^2}\right) \xrightarrow[f=f_0]{} IL = -10\log\left(\frac{1}{\left(1 - \frac{Q_L}{Q_U}\right)^2}\right) \tag{30}$$

From this analysis we can conclude that the filter loss in band is dependent on the physical quality of the resonators but also on the bandwidth relation with the central frequency.

Taking that into account and considering the BW requirements of the selected ATC, we used in our system a f_c of 450 MHz, an *IL* of -0.5 dB and a BW_{3dB} of 6 MHz, resulting in a Q_L of 75 and a Q_U equal to 1340 (the BW_{3dB} was increased to reduce the Q_L). The usual range of Q_U depending on the available technology to build filter resonators is presented in Table 8.

The coaxial cavity technology was selected and with the coupling matrix method proposed by Cameron [59], a six cavity combline elliptical filter, Fig. 55, was designed and constructed (please consult Annex A for more details on cavity filter design and tuning).

Table 8 – Resonator unloaded quality factor vs technology.

Technology	Q_U
Lumped	… – 100
Microstrip	100 – 300
Helical Resonators	250 – 5000
Coaxial Cavity	1000 – 6000
Waveguide	4000 – 15000
Dielectric Resonators	5000 – 50000

The resulting measured amplitude response is presented in Fig. 56, where f_c is equal to 449.4 MHz, BW_{3dB}=5.8 MHz, -0.9 dB of *IL* at f_c and 44dBc attenuation at 10 MHz stop-bandwidth, increasing to 60 dBc at 12 MHz stop-bandwidth, which are in line with the design goals. In Fig. 57 and Fig. 58, a photo of the constructed BPF exterior and interior is respectively shown.

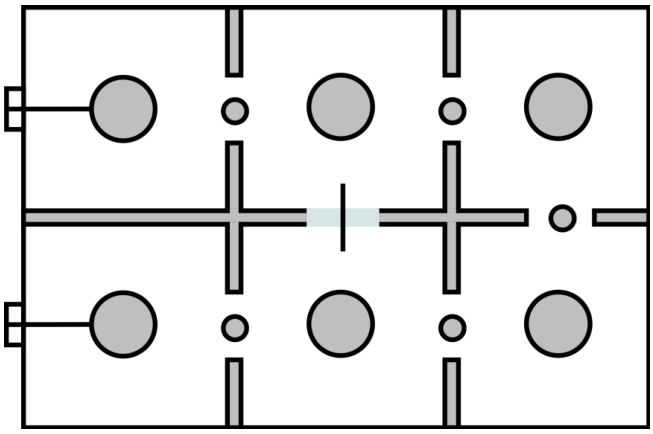


Fig. 55 – Construction diagram of a 6 cavity combline bandpass filter.

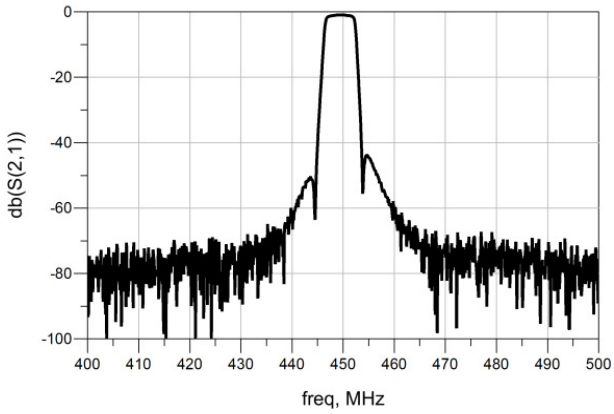


Fig. 56 – BPF measured amplitude frequency response.

. As far as the BPF input impedance is concerned, as depicted in Fig. 59, we realized that, contrary to specified, the implemented cavity filter is of the Π-type (determined by the shunt equivalent circuit of the first resonator), whereas it should be of the T type (series resonator at the input). So, it was necessary to insert an impedance transformer at its input, so that the switching mode PA output would be terminated by the required equivalent T-type filter. This impedance transformer was implemented with a PCB transmission line, included in the SMPA design, which will be described in the next Sub-Chapter.

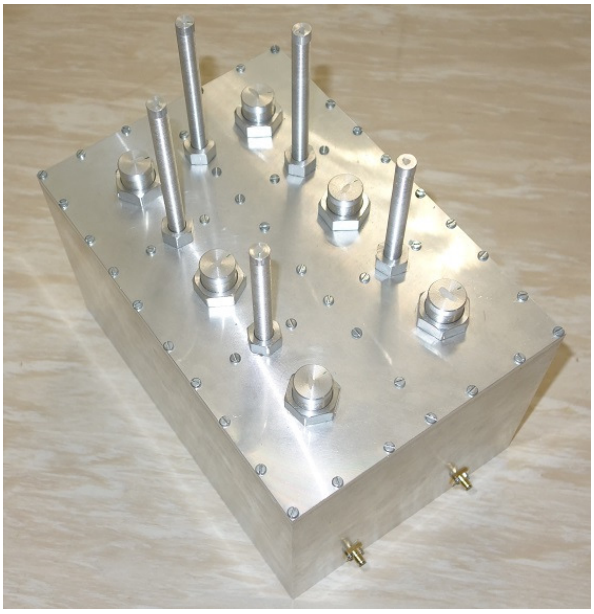


Fig. 57 – Photograph of the constructed BPF.

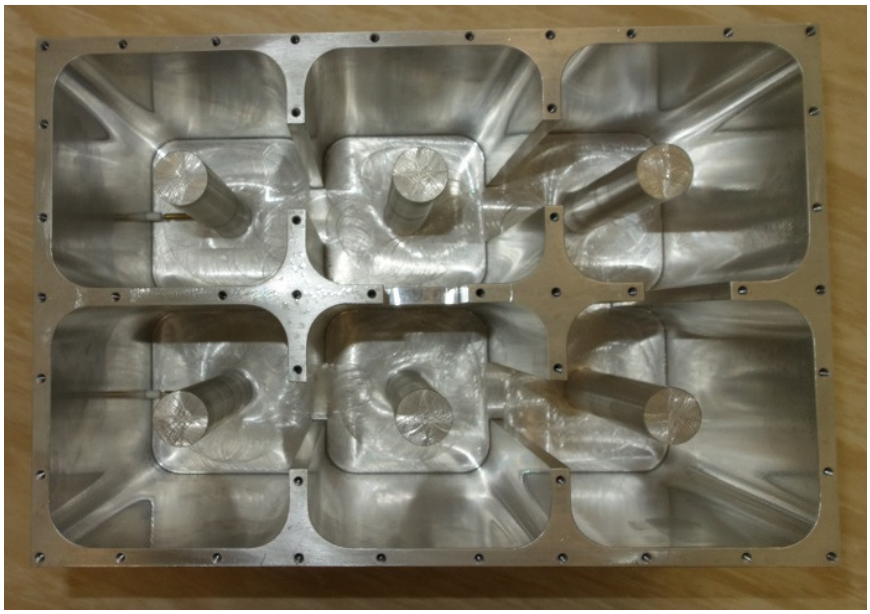


Fig. 58 – Photograph of the constructed BPF interior.

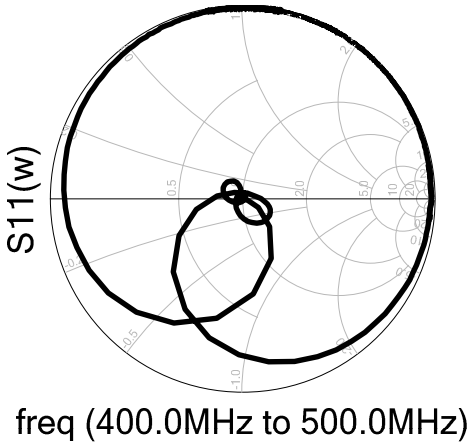


Fig. 59 – Measured BPF input reflection, $S_{11}(\omega)$.

4.4.2 Switched-mode Power Amplifier

The schematic of the RF-CAB SMPA is depicted in Fig. 60.The Class-F SMPA was built with a GaN die transistor (M1) from Cree (CGH60008D) and designed to operate at a central frequency of 450MHz. The bonding to the printed circuit board was performed in house. The output matching network provides a short-circuit to the even harmonics and an open circuit to the 3rd harmonic, while the broadband all pass input matching network was designed to absorb the transistor's input capacitance.

Another similar transistor (M2 operated as the flywheel), also from Cree (CGH60008D), implements the required path to ground - necessary to preserve the BPF input current continuity - and is connected at the Class-F SMPA output.

The output transmission line (TL) was dimensioned so that the Class-F load resembles a T-type BPF, necessary to the proper system functionality, as previously indicated.

A photo of the implemented SMPA prototype is presented in Fig. 61, containing also the indication of the signals connection.

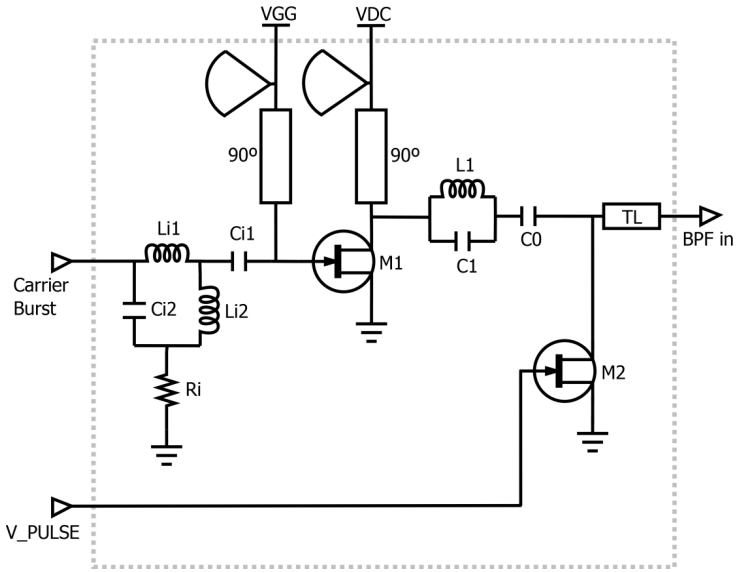


Fig. 60 – Class-F power amplifier and flywheel transistor schematic.

4.4.3 RF and FW Driver

The SMPA requires high input signal levels to be in saturation, so, a broadband amplifier from Mini-Circuits (ZHL-42W with a 15V power supply) was used to amplify the RF burst signal. The gain as function of frequency of the RF Driver is depicted in Fig. 62 (extracted from ZHL-42W datasheet). Since it is broadband and flat, it amplifies the signal with an almost imperceptible degradation.

The flywheel driving signal, V_PULSE must be boosted in amplitude by an amplifier, the FW Driver, so that the flywheel transistor is effectively ON and OFF during the RF-CAB operation. V_PULSE is a square wave signal with an instantaneous variable duty-cycle (0% up to 100%) and variable instantaneous frequency, whose minimum is fixed at 5MHz but whose maximum is dependent on the type of amplitude modulator used. Therefore, as this bandwidth might be limited by the FW Driver, it was implemented with

fast current op-amp stages based on the Texas Instruments THS3202. It provides an output level between -9V and +1V, with very fast transitions to efficiently turn ON and OFF the flywheel transistor.

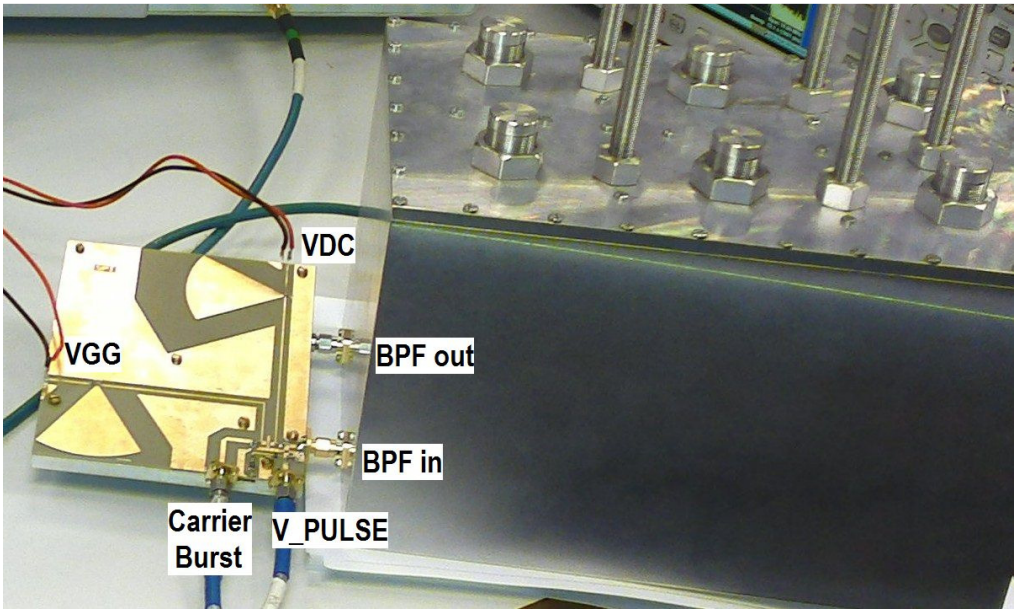


Fig. 61 – Photo of the SMPA prototype.

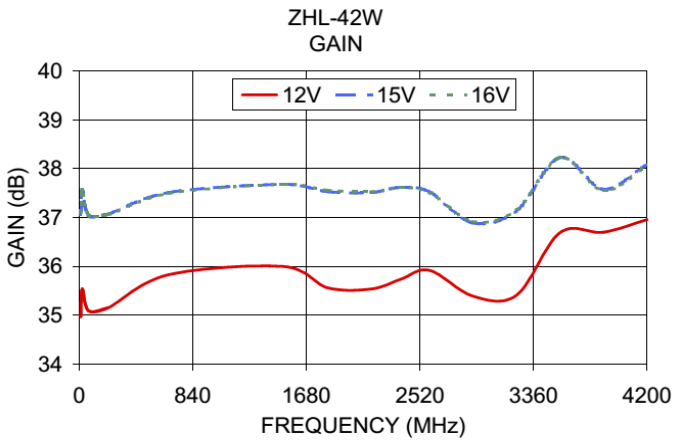


Fig. 62 – RF_Driver gain vs frequency (extracted from ZHL-42W manufacturer datasheet).

The schematic of the FW driver, as well as the simulated gain versus frequency are presented in Fig. 63 and Fig. 64 respectively.

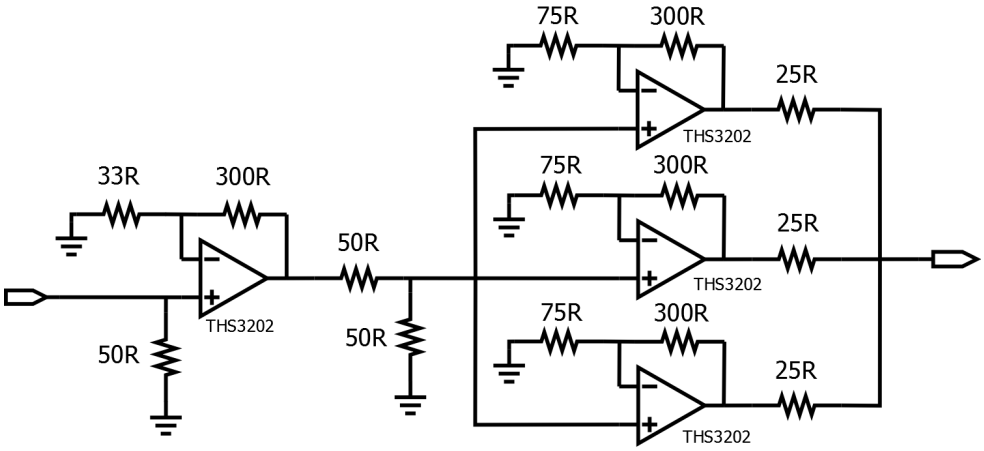


Fig. 63 – FW_Driver schematic.

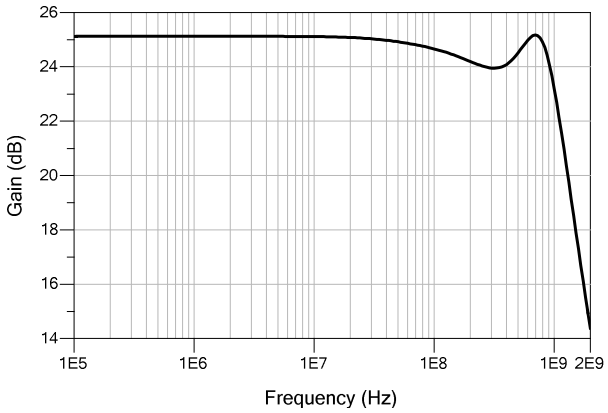


Fig. 64 – FW_Driver simulated gain vs frequency.

4.4.4 Complete Test Setup

The implemented prototype simplified schematic is presented in Fig. 65. The transmitter, Tx, is composed of a Class-F SMPA and its RF driver, of the flywheel transistor and its FW driver and at the SMPA output, it is connected the BPF. To guarantee that the output RF-CAB observed impairments are due to the Tx dynamics and not to any signal generation imperfections, the input amplitude burst signal was first generated as a Matlab® software script, and then the corresponding waveforms uploaded to an external arbitrary waveform generator (AWG). Therefore, at SMPA RF driver input, the desired amplitude burst signals (in Fig. 65 represented by the multiplication of RF_CARRIER by V_PULSE) and the signal to drive the FW Driver are provided by the Tektronix AWG7102.

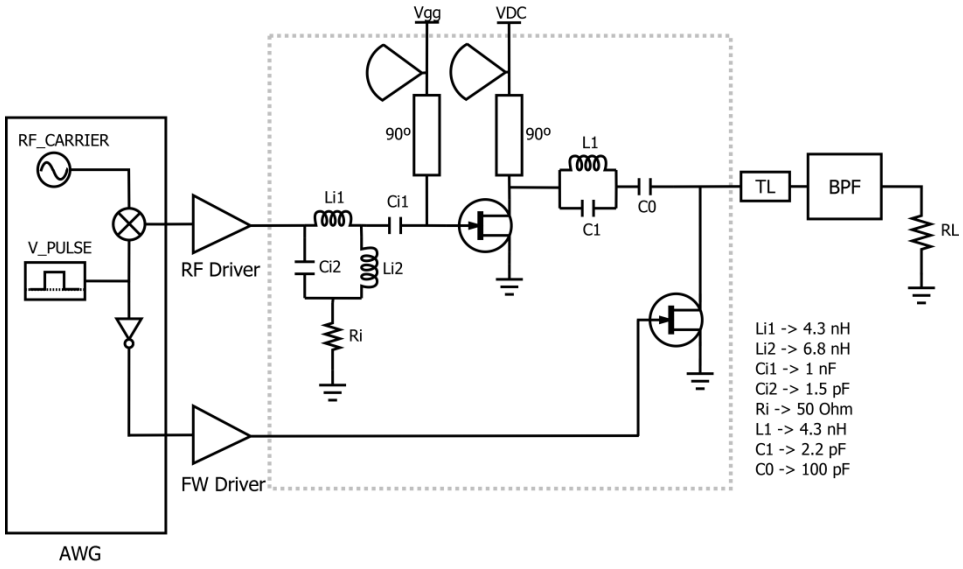


Fig. 65 – RF carrier amplitude-burst transmitter prototype schematic.

In addition, since the drain of the flywheel transistor is biased at 0V, when the output voltage amplitude of the Class-F amplifier is too high, during the negative sinusoidal voltage arcs, the flywheel transistor can be turned ON through the activation of its V_{gd}. To prevent this, the Class-F SMPA drain supply was limited to 10V.

The implemented prototype (SMPA and BPF) is shown in Fig. 66.

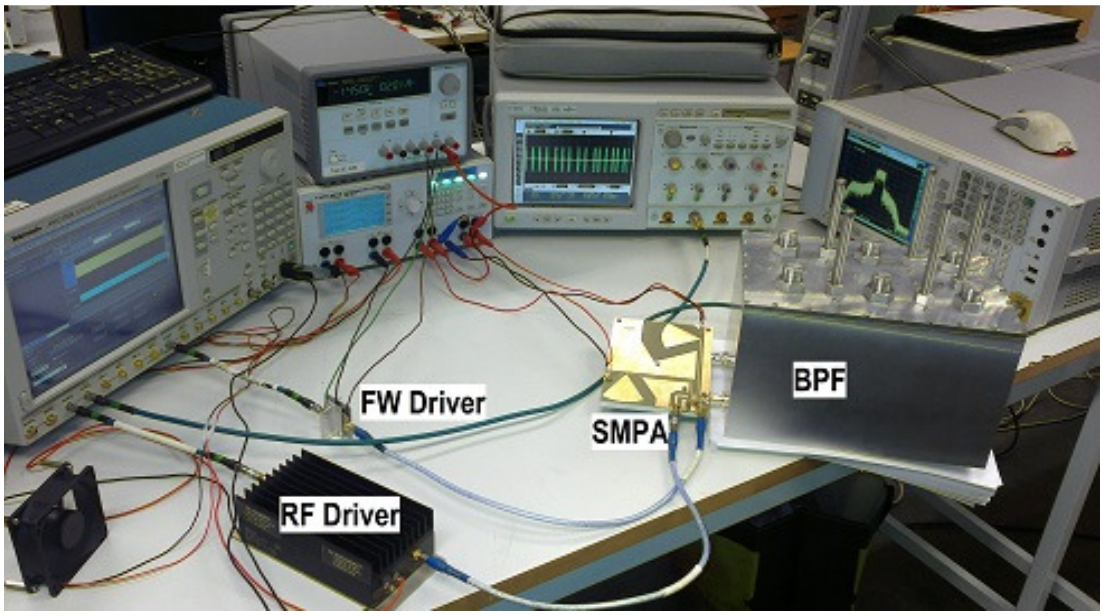


Fig. 66 – RF carrier amplitude-burst transmitter prototype and measurement setup.

4.5 Experimental Validation

4.5.1 Static Conditions

In order to validate the proposed theory, the same static tests as in Sub-Chapter 4.3 were conducted in the lab and verified by simulation.

The test results, for a 10 MHz envelope square wave and several duty-cycle values, are presented in Fig. 67. It depicts the measured Tx output envelope amplitudes (Vout_10M), their ideal values (Vout_Ideal), the simulated ones (Vout_10M_S) and the values predicted (Vout_Theory) by (23). As is possible to see, there is a good agreement not only on the measured and simulated values (validating the simulation model), but also with the ones predicted by the proposed theory (obtained using a FET's R_{on} of 4 Ohm). As was forecasted by (23), the obtained values are different from the ideal ones, especially in the high duty-cycles range, predicting some output distortion.

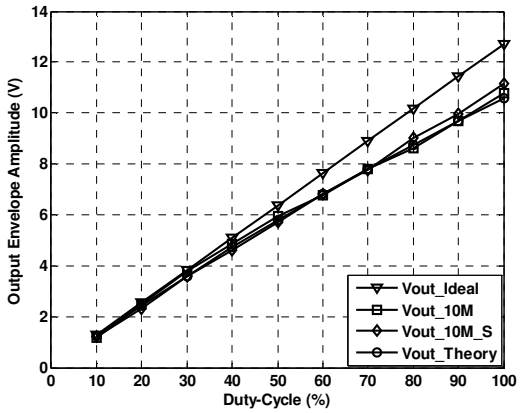


Fig. 67 – RF carrier amplitude-burst transmitter static linearity.

During the same test, the Tx power efficiency was also measured and simulated, whose results are depicted in Fig. 68. Please also note the proximity between the simulations (Eff_10M_S), the measurement results (Eff_10M) and the theory developed in Sub-Chapter 4.3, which constitutes a proof of the used prototype and the analytical model. As can be seen, promising efficiencies above 50% can be obtained up to a back-off of around 10.5dB, and above 65%, if this back-off is restricted to 6dB. These efficiency values are only due to the SMPA and do not include the BPF losses, because the filter can be independently optimized.

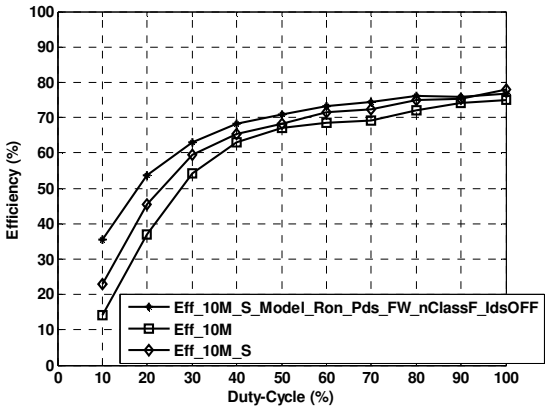


Fig. 68 – RF carrier amplitude-burst transmitter static efficiency.

4.5.2 Dynamic Conditions

As was already analyzed in Sub-Chapter 4.3, a CDMA2000 signal is used for dynamic simulations and measurements using the same prototype, and a 10 MHz PWM for the amplitude modulator. The power spectral densities of both the input (RF Driver output) and output (BPF output) signals are shown in Fig. 69 (measured) and Fig. 70 (simulated).

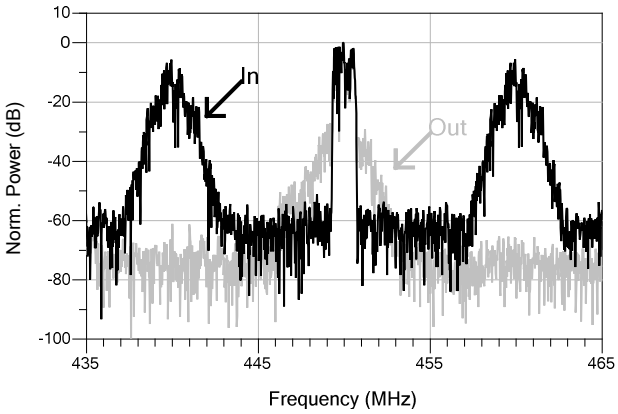


Fig. 69 – Measured input and output CDMA2000 signal with the PWM 10MHz ATC.

The simulated integrated output power was 26.1 dBm for a very good average efficiency of 70%, while close figures of 26.3 dBm and 67% were actually measured. As a complement to this data, the worst case linearity, evaluated as the adjacent channel power ratio, ACPR, was predicted to be 36.4 dBc (close to the 40dBc obtained in the linearity analysis) while the measured value was slightly lower: 30.8 dBc. It is worth noting that

these measurements and simulations were performed without any type of distortion compensation, which naturally leaves room for linearity improvement.

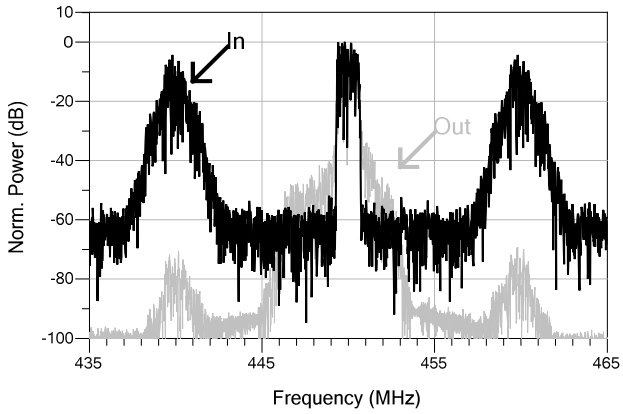


Fig. 70 – Simulated input and output CDMA2000 signal with the PWM 10MHz ATC.

The wideband spectrum is depicted in Fig. 14, where it is shown that the noise floor (limited by the equipment dynamic range) level is constant out of band, preventing any co-existence concern. Since the BPF was not fully optimized, the out-of-band output signal presents some peaks due to cavity filter parasitic resonances.

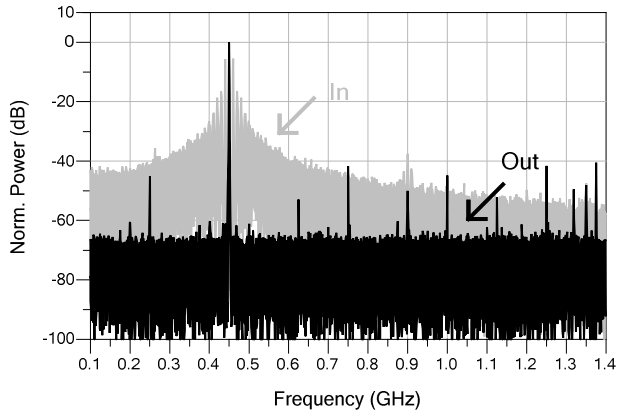


Fig. 71 – Measured CDMA2000 signal wideband spectrum.

Fig. 72 presents the normalized probability density function of the duty-cycle of the modulated envelope, which is directly correlated with the original amplitude values of the CDMA2000 input signal, and the measured static efficiency obtained for the same PWM. As can be seen, the low efficiency achieved at the low duty-cycle values has just a small impact on the overall efficiency, which justifies the remarkable average efficiency of 67%

achieved for a 6dB peak-to-average-ratio signal and with an amplifier whose peak efficiency is only 75%.

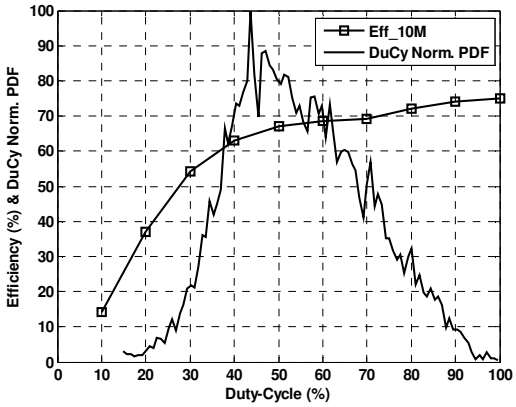


Fig. 72 – RF carrier amplitude-burst transmitter measured static efficiency and duty-cycle normalized PDF.

4.6 RF-CAB Performance Limits

Up to this point, the RF-CAB transmitter has been tested with just one type of envelope modulator, PWM 10MHz. However, as was shown in the architecture dimensioning, the output reconstruction filter bandwidth is dependent on the ability of the ATC to separate the switching noise from the band of interest. Therefore, it is important to verify the impact that different ATCs have on the RF-CAB circuit performance. To do so, the system is first tested within similar static conditions as previously presented. But now the frequency of the square wave is increased from 10MHz to 15, 30 and 60 MHz.

For the above mentioned square wave frequencies, the simulated and measured output envelope voltage versus the square wave duty-cycle are depicted in Fig. 73 and Fig. 74 respectively. These results show that the output envelope amplitude deviation increases from the ideal values, when the square wave frequency is higher.

Similarly, the drain efficiency of the RF-CAB transmitter is also poorer when the square wave frequency increase, as shown in Fig. 75 and Fig. 76 for the simulation and measurement environments respectively.

Based on these results, we conclude that both the linearity and efficiency are affected not only by the RF-CAB components impairments, as previously described, but also by the ATC time-frequency characteristics.

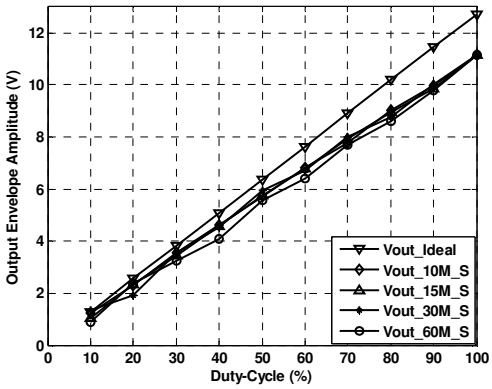


Fig. 73 – RF carrier amplitude-burst transmitter simulated static linearity for several square wave frequencies.

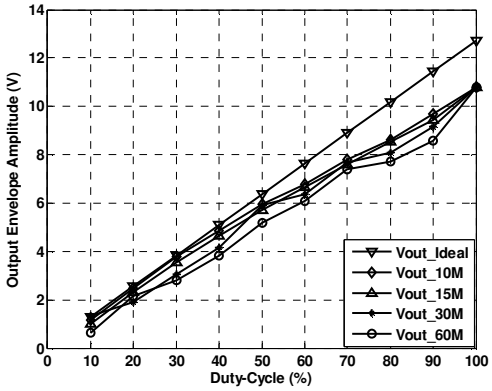


Fig. 74 – RF carrier amplitude-burst transmitter measured static linearity for several square wave frequencies.

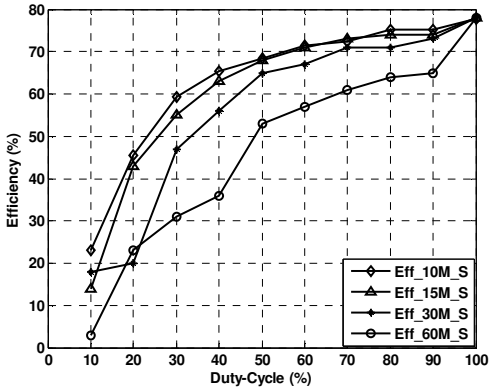


Fig. 75 – RF carrier amplitude-burst transmitter simulated static efficiency for several square wave frequencies.

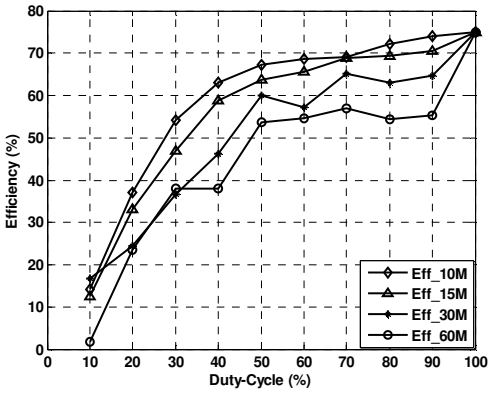


Fig. 76 – RF carrier amplitude-burst transmitter measured static efficiency for several square wave frequencies.

In order to further verify the previous statement, the RF-CAB system performance in the dynamic environment was tested by simulations and measurements, using the ATCs described in the architecture system design (Sub-Chapter 3.4). The input signal is also the CDMA2000 so that it is possible to compare the performance. The obtained results are presented in Table 9 and additionally, the normalized power spectrum for a CRFB3 90MHz ΔΣM is depicted in Fig. 77 (simulation) and Fig. 78 (measurement).

From these results, we can first conclude that, though the simulated linearity is more optimistic than the measured one, in general, the simulations corroborate the measurements, proving that the used model is also valid in these conditions. Furthermore, the best efficiency results are obtained for the PWM with lower comparison frequency, as was predicted by the static measurements, while the linearity is similar for all of the modulators.

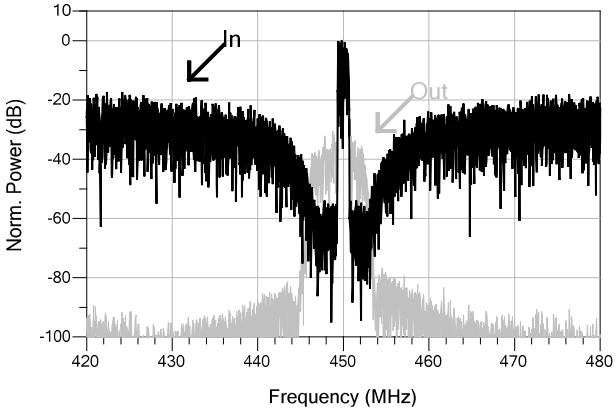


Fig. 77 – Simulated input and output CDMA2000 signal with CRFB3 90MHz envelope modulator.

Table 9 – RF carrier amplitude-burst transmitter measured and simulated performance (efficiency and linearity) for several envelope modulators.

Modulator	Measurements		Simulations	
	ACPR (dBc)	Efficiency (%)	ACPR (dBc)	Efficiency (%)
PWM 10MHz	30.8	67	36.4	70
PWM 15MHz	30.8	65	37.4	68
PWM 30MHz	30.9	53	37.3	62
SD3 90MHz	31.1	52	33.6	55
SD3 150MHz	31.4	45	34.1	49
CRFB3 90MHz	31.2	52	33.8	55
CRFB3 150MHz	31.6	45	34.5	49

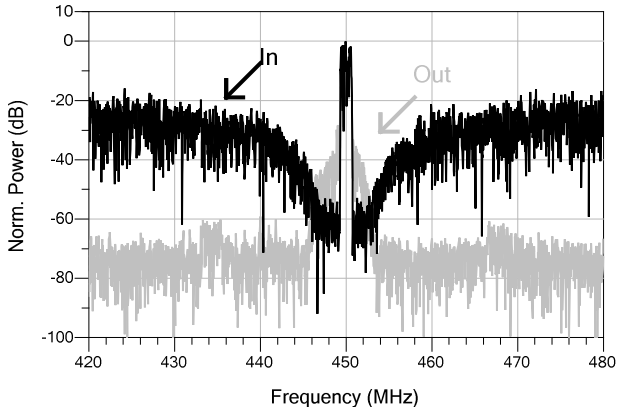


Fig. 78 – Measured input and output CDMA2000 signal with CRFB3 90MHz envelope modulator.

Since it is hard to compare the PWM and ΔΣM directly, because the former is based on the pulses duration and the later in the pulsed density, we devised another comparison method, which is also used to explain the performance differences. This method is based on the number of RF carrier cycles that the RF carrier amplitude-burst signal has during its

ON state duration. So, after the final calculation is completed for each ON pulse, the results where statistically treated to evidence their significance.

Hence, we calculated the cumulative distribution function (CDF) for each of the tested modulators, whose results are presented in Fig. 79 (the values of the ΔΣM SD3 are omitted, since they are very similar to the CRFB3 ones).

Comparing these results with the ones obtained for the RF-CAB performance (Table 9) we associate the best performance configurations as the ones who have the larger number of RF cycles during the ON periods. In fact, even if in the frequency domain the performance of the PWM 30MHz is superior to the CRFB3 90 MHz (the noise free bandwidth is wider, as indicated in Table 1), the performance of the RF-CAB when these two modulators are used is very similar in both efficiency and linearity.

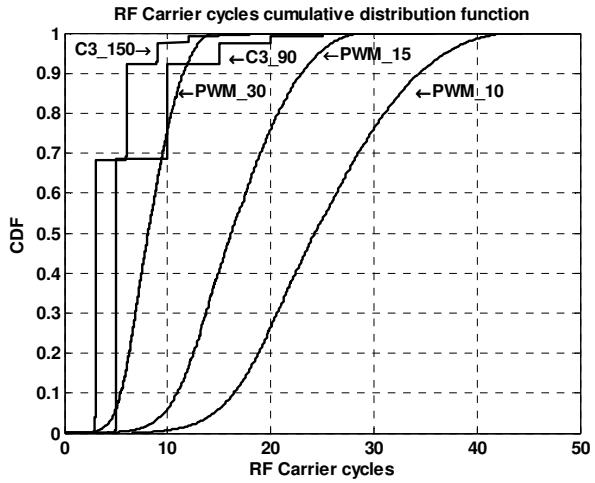


Fig. 79 – Cumulative distribution function of the RF carrier cycles number contained in the coded envelope ON level for ΣΔM and PWM.

The reason for this behavior is explained by the influence that the impairments have in the RF-CAB performance, as was described in Sub-Chapter 4.3. As was mentioned, every time the input signal changes its sate from OFF to ON, the dissipation in the SMPA main transistor during the initial RF cycles increases. The impact of this loss is higher when the total number of RF cycles is lower during the ON period, which is what happens when we increase the PWM comparison frequency or when we use the ΣΔM.

Another issue limits the potential use of the RF-CAB transmitters and is related with the flywheel implementation. The proposed solution, a transistor connected to ground at the

Class-F output, forces the flywheel device to have its drain DC biased at zero volt. When the Class-F PA is ON, the output AC signal has an amplitude higher than the Class-F power supply voltage. Hence, if the gate voltage of the flywheel transistor is not lower than the one applied to its drain, the device channel is activated, because the v_{GD} voltage is higher than the channel threshold voltage. Therefore, in order to prevent the Class-F output voltage clipping and because the FW driver has amplitude and slew rate limitations, the Class-F drain power supply was decreased to 10V. This handicap limits the RF-CAB output power capabilities, when this implementation and topology is used.

4.7 Conclusions

This Chapter presented a comprehensive and thorough study of the actual impairments that should be expected from RF-CAB transmitters. In addition, it provided a theoretical model capable of predicting values for the most significant linearity and efficiency degradations that should be expected from such a Tx architecture.

It was shown that, contrary to the common belief, this architecture is, theoretically, capable of both 100% efficiency and ideal linearity, but that this ideal behavior can be easily degraded if the circuit design and implementation do not consider several issues, such as the SMPA-BPF interaction, which is one of the design keys. It was developed a model that defines the conditions which the individual blocks must fulfill in order to safely implement the RF-CAB Tx. These include the SMPA characteristics, which must implement a voltage source with low internal resistance, must keep the linearity and efficiency with a variable load and must implement a low resistance path to ground during the OFF periods of the input signal. The SMPA unipolar implementation requires an additional transistor (flywheel) to guarantee the BPF input current continuity.

A practical prototype was developed, constructed and used to validate the proposed theory. The static measurements showed that the efficiency degradation obtained at the low signal amplitudes is determined by the amplifier quiescent current, proving the developed theory.

Additionally, measurements performed under dynamic pulse width and density modulation (CDMA2000 modulated signal), which were in agreement with the

corresponding simulations, corroborate our developed theory and validate the proposed implementation.

Furthermore, the major limitations and performance limits of this architecture were identified. As the output power limitation, due to the flywheel transistor, refrains the RF-CAB use in high power applications, the next chapter describes a possible solution to this issue.

Chapter 5 – RF Carrier Phase-Burst

5.1 Architecture Changes Phase-Burst vs Amplitude-Burst

Taking as a reference the RF-CAB transmitter, depicted in Fig. 18, our idea is to replace the SMPA binary ASK input signal by binary PSK, changing the output levels of the amplitude to time converter (PWM or ΣΔM) from {0;+1} (OFF;ON) to {-1;+1} (inverted ON;ON). Therefore, at the SMPA input, the signal will not have amplitude bursts (the amplitude envelope is now constant), but rapid phase changes of π rad – in addition to the analog phase modulation – at the frequency and pulse width or density change of the PWM or ΣΔM. An example of these two signals is depicted in Fig. 80.

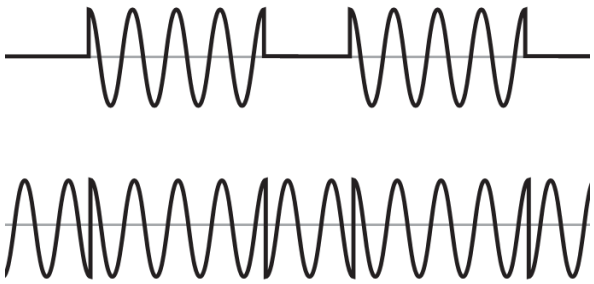


Fig. 80 – B-ASK (top) and B-PSK (bottom) modulated signals.

This means that the transmitter makes now use of phase burst signals instead of amplitude burst ones. Hence the name RF Carrier Phase-Burst (RF-CPB) that we chose for this architecture, to differentiate it from the RF-CAB one.

In order to construct this phase-burst signal, the ATC must be slightly modified and these changes have some important implications. Let's focus for now on the PWM. Referring back to Fig. 19, the comparator output signal is now bipolar and composed by two opposite levels {-1;+1}. However, to properly code the input signal, the triangular comparison wave must also be bipolar, which means that the input signal range can have now also negative values.

In Fig. 81 it is shown the input signal range versus the output signal duty-cycle, for both unipolar and bipolar PWM.

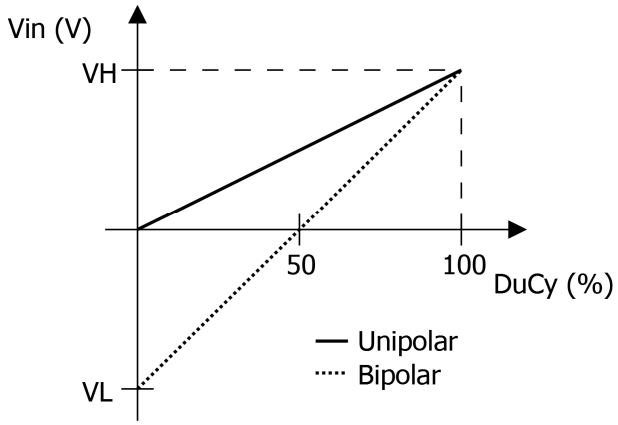


Fig. 81 – Unipolar and bipolar ATC input voltage vs duty-cycle.

Since the RF modulated signals envelope has only positive values, the duty-cycles of the bipolar modulator output signal are restricted to the range [50%..100%]. Therefore, in order to see if this restriction has any impact in the signal codification characteristics, as in Chapter 3, the signal with variable amplitude depicted in Fig. 20 was coded by the bipolar PWM. An excerpt of the input and output signals is presented in Fig. 82.

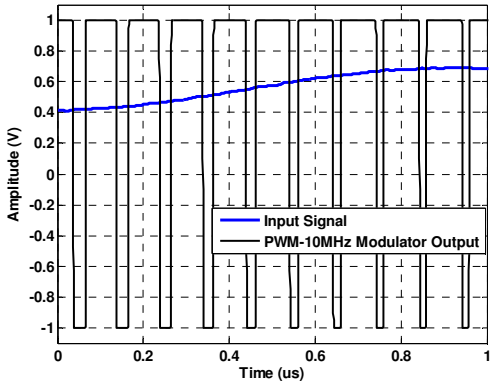


Fig. 82 – Bipolar envelope modulator output signal example.

This example shows that, when the input signal increases, the pulses duration at the high level also increases. This is the expected behavior that allows the average of the PWM output signal to follow the input signal value. So, in time domain, there is no major differences between the unipolar and bipolar coding.

In frequency domain, it is possible to verify that the bipolar codification provides a similar switching noise separation from the input signal spectrum as the unipolar

modulator. In Fig. 83 it is shown the normalized power spectrum of both the input signal and the bipolar PWM output signal.

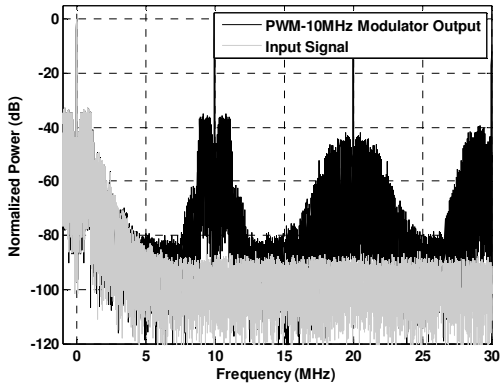


Fig. 83 – Variable amplitude input signal and bipolar PWM-10MHz amplitude to time converter output signal in frequency domain.

As before, it is possible to recover the input signal by filtering the coded signal with a lowpass filter. This can be checked in Fig. 84, where the input and recovered signals are compared in time domain, for an ideal rectangular lowpass filter with a bandwidth of 2.5 MHz. Visually, both signals are almost undistinguishable, but since these visual inspections are always prone to errors, the NMSE comparison between the input and recovered signals is more appropriate to access the modulator performance. Therefore, in Table 10 it is presented the NMSE values not only for the PWM 10MHz, but also for the all the used modulators in the RF-CAB tests. These modulators were modified so that it is possible to use them in the RF-CPB. A rectangular low pass filter with 2.5 MHz bandwidth was used to recover the initial signal.

These results are very similar those obtained using the unipolar ATC and prove that the bipolar ATC is able to efficiently code the input envelope.

Concerning additional architecture differences, at system level, the only block that is different between the RF-CPB and the RF-CAB is the ATC. All the remaining blocks are common and do not require any change.

5.2 Theoretical Analysis of the RF Carrier Phase-Burst Circuit

The output of the RF-CPB transmitter envelope modulator is a two level signal (+1;-1), and so the SMPA driving signal can be described by,

$$v_{in}(t) = \pm V_{AC} \sin(\omega_C t) = V_{AC} \sin(\omega_C t \pm \pi) \tag{31}$$

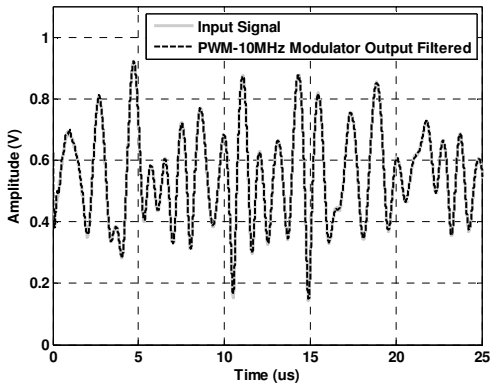


Fig. 84 – Variable amplitude input signal and the modulated version (by a bipolar PWM-10MHz amplitude to time converter) after being recovered by a 2.5 MHz rectangular lowpass filter.

Table 10 – Normalized mean squared error of the modulated bipolar signal after being recovered by a 2.5MHz BW square lowpass filter.

Modulator	NMSE (dB)
PWM 10MHz	-53
PWM 15MHz	-54
PWM 30MHz	-54
SD3 90MHz	-50
SD3 150MHz	-54
CRFB3 90MHz	-50
CRFB3 150MHz	-53

Therefore, a possible ideal circuit implementation of the RF-CPB Tx last stage is depicted in Fig. 85. Once a voltage source configuration is used, a BPF with a series input resonator is required, so that the BPF input voltage is integrated. The SW1, SW2 switches correspond to the SMPA, whose control is performed by the output signal of the envelope modulator. When positive (+1), SW1 closes and SW2 opens, applying an AC voltage to

the BPF. When negative (-1), SW1 opens, SW2 closes and a voltage source with opposite phase is applied to the BPF. From the system's perspective, the switching noise introduced by the envelope coding must be filtered out by the BPF, to keep the output signal integrity.

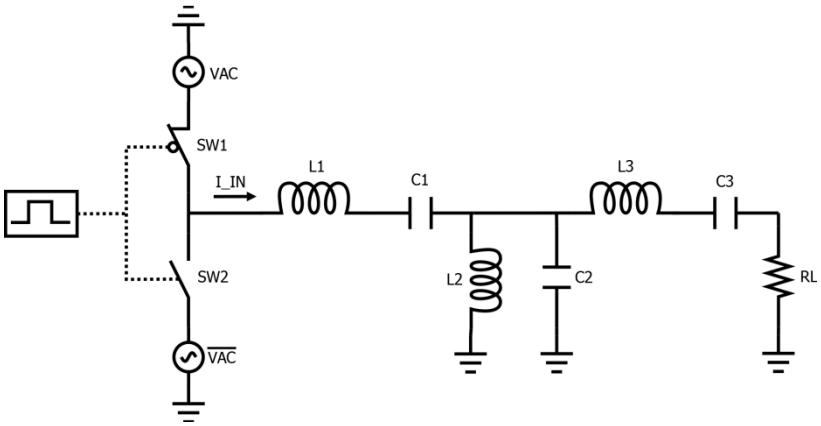


Fig. 85 – The ideal RF Carrier Phase-Burst transmitter structure.

Similarly to the RF-CAB, the use of a reactive (non-dissipative) BPF with a good attenuation in the rejection band, guarantees very high output power efficiency. So, when properly designed, the performance of such a transmitter architecture is not affected by the input signal coding efficiency, which can be demonstrated with the same procedure applied to the RF-CAB transmitter (Sub-Chapter 4.1.1).

Considering static Tx operation i. e., the input signal is an unmodulated sine-wave, whose constant envelope voltage after codification results in a square-wave with variable duty-cycle, it is expected that the output envelope voltage will be proportional to the duty-cycle of the square-wave.

In order to verify this hypothesis, we start by considering the low-pass equivalent of the circuit depicted in Fig. 85. The AC voltage sources are replaced by DC ones (VDC) and the BPF is replaced by a low-pass filter, which can be approximated by a series inductor. When a voltage is applied to the inductor, the input current is described by,

$$i_L(\tau) = i(\infty) + (i(0) - i(\infty)) \cdot e^{-\lambda\tau} \tag{32}$$

where τ is the envelope time and λ the time constant,

$$\lambda = \frac{L}{R_L} \tag{33}$$

If the inductance value is sufficiently high, so that the time constant is much higher than the period - T - of the coded envelope square-wave, then the inductor input current can be linearly approximated during T by,

$$i_{neg}(\tau) = I_{MAX} + \left(-\frac{V_{DC}}{R_L} - I_{MAX} \right) \cdot \lambda\tau \tag{34}$$

$$i_{pos}(\tau) = I_{\min} + \left(\frac{V_{DC}}{R_L} - I_{\min} \right) \cdot \lambda\tau \tag{35}$$

Defining the duty-cycle δ and (1- δ) as the time duration of the positive and negative pulses respectively, when τ reaches these values we have,

$$I_{\min} = I_{MAX} + \left(-\frac{V_{DC}}{R_L} - I_{MAX} \right) \cdot \lambda(1-\delta)T \tag{36}$$

$$I_{MAX} = I_{\min} + \left(\frac{V_{DC}}{R_L} - I_{\min} \right) \cdot \lambda\delta T \tag{37}$$

Combining (36) and (37),

$$I_{\min} = \frac{V_{DC}}{R_L} \frac{(2\delta - 1) - \lambda\delta(1-\delta)T}{1 - \lambda\delta(1-\delta)T} \tag{38}$$

$$I_{MAX} = \frac{V_{DC}}{R_L} \frac{(2\delta - 1) + \lambda\delta(1-\delta)T}{1 - \lambda\delta(1-\delta)T} \tag{39}$$

Knowing that the filter average input current is equal to the load current,

$$\frac{I_{MAX} + I_{\min}}{2} = \frac{V_O}{R_L} \tag{40}$$

Therefore, combining (38) and (39) in (40),

$$V_O = V_{DC} \frac{(2\delta - 1)}{1 - \lambda\delta(1-\delta)T} \tag{41}$$

which reduces to $V_O = V_{DC}(2\delta\text{-}1)$, when λ and/or T is close to zero or when $\lambda T << 1$.

In this low-pass equivalent analysis, the output voltage can, as expected, assume positive and negative values when the duty-cycle is higher or lower than 50% respectively. At δ equal to 50%, the filter is charged and discharged with the same amount of energy, forcing null output voltage. Another important aspect concerns the polarity of the filter input current. Taking a close look on (38) and (39), during the period T, for some duty-cycle values it is possible to have I_{min} and I_{MAX} with negative and positive values respectively, but still (40) is fulfilled.

Applying these results and observations to the band-pass system, RF-CPB, the negative values of voltage and current that are present in the low-pass equivalent cause, in the band-pass system, phase inversions of the RF carrier. For example, when δ is equal to 40% or 60% the load envelope voltage is the same, but the RF Carrier phase has opposite value.

A practical implementation of the circuit of Fig. 85, using a single-ended SMPA is shown in Fig. 86 where the output matching network (OMN) provides an open circuit at all harmonics except the fundamental.

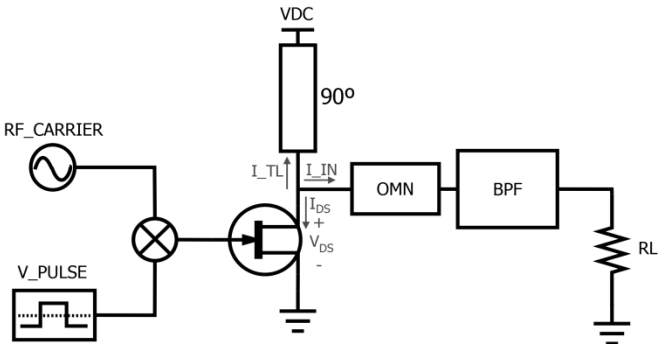


Fig. 86 – RF Carrier Phase-Burst transmitter with Class-F SMPA.

Ideally, when a CW signal is applied to a power amplifier (PA) forcing it to operate in Class-F mode, i.e., in voltage saturation, the Class-F PA behaves as an ideal AC voltage source as required by the initial RF-CPB model (Fig. 85). So, to identify the performance limits of this circuit, we wanted to first verify its behavior under static conditions. For that, we used a 450MHz RF carrier multiplied by a 10MHz square-wave of variable duty-cycle.

Fig. 87 depicts a selection of signals, labeled in Fig. 86, observed during a full 10 MHz square-wave period of 80% duty-cycle, whose +1 and -1 levels are identified by the *pos.* and *neg.* regions, respectively.

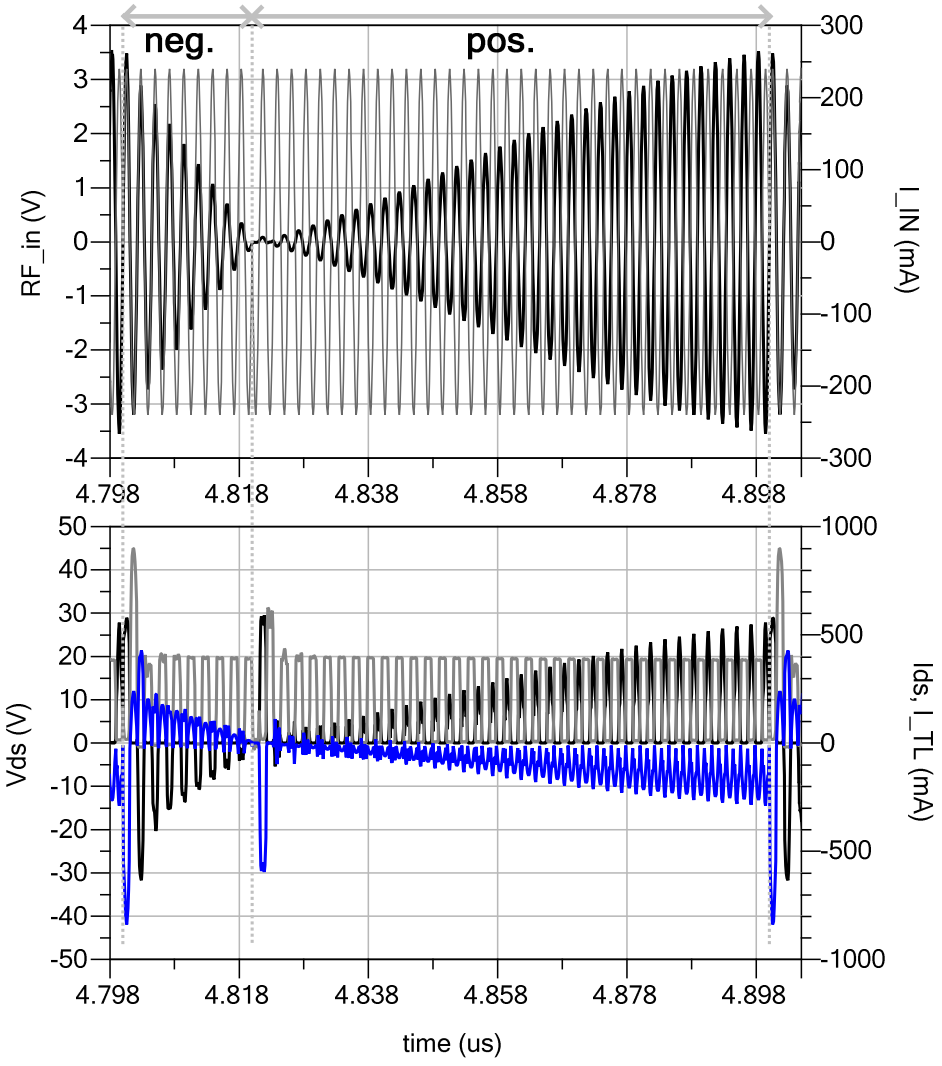


Fig. 87 – RF Carrier phase-burst waveforms for 80% envelope square-wave duty-cycle. (Top) Input phase-burst signal (*RF_in*, grey) and BPF input current (*I_IN*, black). (Bottom) transistor drain-source voltage (V_{ds}, grey), transistor drain-source current (I_{ds}, black) and bias TL current (I_{TL}, blue).

These regions, indicated in the input signal (*RF_in*, grey) and the BPF input current (*I_IN*, black) – shown on the top plot of Fig. 87 – serve as the reference for the input signal phase (*pos.* the reference and *neg.* the inverse). The presence of a rising amplitude in the BPF input current, *I_IN*, indicates that the filter is being charged by the SMPA during the *pos.* period, while the decreasing amplitude is an indication of a corresponding discharge during the *neg.* period. This could be surprising, at first sight, as we would only expect a one direction energy flow from the active SMPA amplifier to the passive BPF filter. However, the observation of the bottom plots of Fig. 87 will provide a clear explanation to such a unexpected behavior.

The bottom graph of Fig. 87 depicts the transistors' drain-source voltage (V_{ds}, grey) and current (I_{ds}, black), and also the drain bias transmission line current (I_{TL}, blue). During the *pos.* time, I_{ds} and V_{ds} waveforms are the ones expected from a class-F SMPA. So, as is indicated by the negative I_{TL} current values of this period, the transistor is converting DC power into RF power charging the BPF. However, this situation is reversed in the *neg.* period, as now the I_{ds} envelope decreases, but, more significant, it is negative, while I_{TL} has become positive. So, during this time window, the transistor is no longer operating as any conventional amplifier, but as a class-F switched-mode synchronous rectifier (SMSR), converting RF power, coming from the BPF, into DC power returned back to the power supply. This operating mode is forced by the high BPF inertia that imposes the phase continuity of its input current, while the FET's channel opening suffers a phase reversal induced by the input RF signal *RF_in*. As shown in the bottom graph of Fig. 87, and contrary to the *pos.* time, during the *neg.* time *I_IN* is in phase with *RF_in*, which is continuously exciting the transistors' gate. Hence, because the transistor never stops switching, and the drain harmonic terminations are the same, the FET and its output matching network constitute the referred class-F SMSR.

The efficiency is high in both modes because the class-F harmonic terminations guarantee non-overlapping V_{ds} and I_{ds} waveforms. However, when *RF_in* abruptly changes its phase, a transient is generated, increasing the losses due to an additional overlap between V_{ds} and I_{ds}. This problem is evidenced in Fig. 87 at each transition between *neg.* and *pos.* timings and, of course, it is aggravated either by increasing the PWM comparison frequency or the ΣΔM sampling frequency.

Unfortunately, besides the efficiency, also the linearity is affected by these transients. Because the class-F SMPA output voltage has to follow the FET's V_{ds} variations, during the input signal transitions the BPF integrates an incorrect SMPA output voltage, and the load voltage can no longer be proportional to the duty-cycle. Moreover, as is shown in Fig. 88 for a 60% duty-cycle, these transients vary themselves with the duty-cycle. The output SMPA voltage errors are more than a simply gain deviation, leading to the referred nonlinearities.

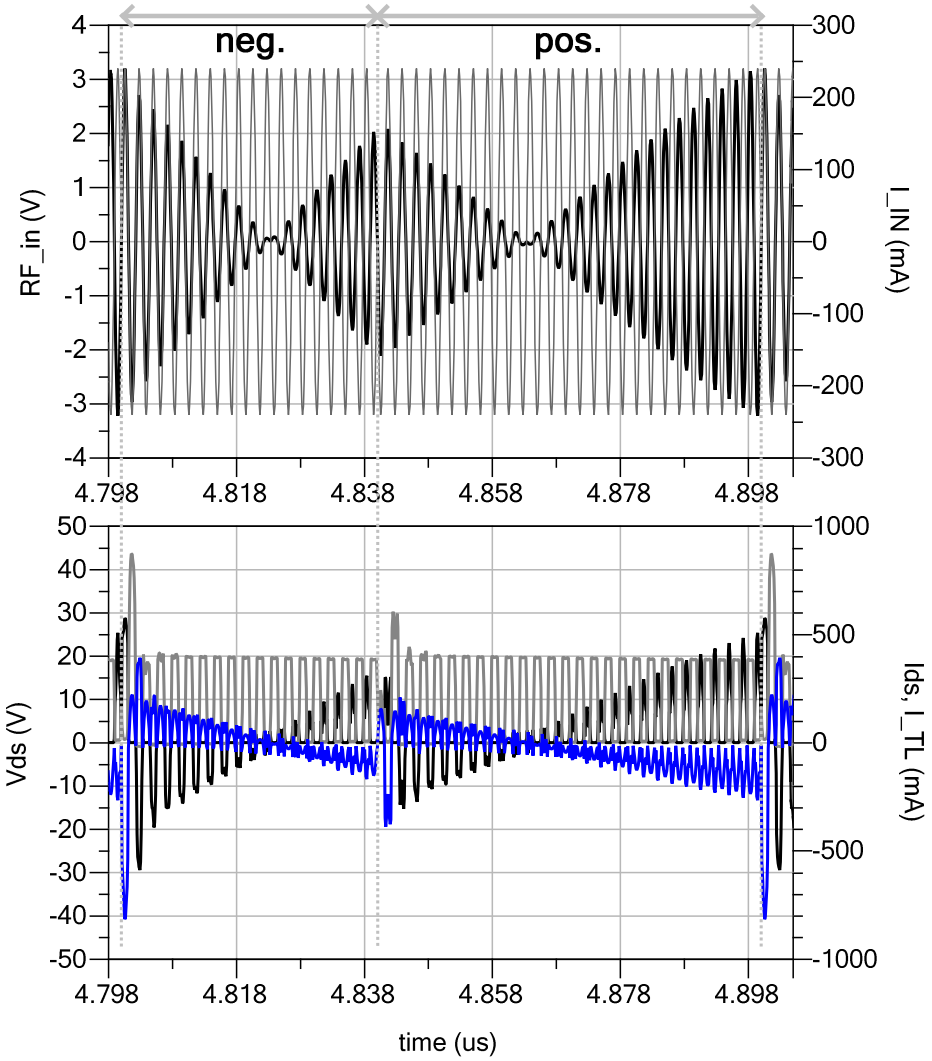


Fig. 88 – RF Carrier phase-burst waveforms for 60% envelope square-wave duty-cycle. (Top) Input phase-burst signal (*RF_in*, grey) and BPF input current (*I_IN*, black). (Bottom) transistor drain-source voltage (V_{ds}, grey), transistor drain-source current (I_{ds}, black) and bias TL current (I_{TL}, blue).

5.3 Circuit Impairments

In a practical implementation, due to the components non-idealities and design constraints, some impairments exist, which prevents the architecture to achieve its full potential. These impairments and the SMPA equivalent model are depicted in Fig. 89. The most relevant ones and the impact that each one causes in the circuit behavior is described in this Sub-Chapter.

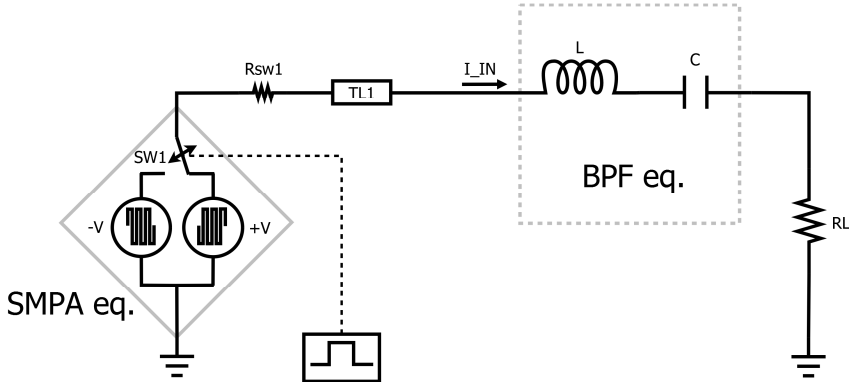


Fig. 89 – RF Carrier Phase-Burst transmitter equivalent circuit plus impairments.

a) Transmission lines (TL)

In a discrete implementation, in order to assemble the components in the circuit board, the presence of extra transmission lines (TL) is inevitable. The most important one is TL1, which directly affects the SMPA-BPF connection and has a similar effect as the one described for the RF-CAB in Sub-Chapter 4.2.3. With this additional TL the SMPA will no longer be terminated with the required T-type BPF. Therefore, the load impedance at the envelope modulator output switching signal frequency and its harmonics is reactive, forcing the transistor' dynamic load line to cross the active region, increasing the losses. Moreover, this impairment affects also the linearity, since the BPF output voltage will not depend exclusively on the envelope duty-cycle.

b) Transistor on resistance and active region

When the FET is in the triode region, it operates as a switch, but the internal resistance of the switch, caused by the FET's channel resistance, leads to a natural efficiency loss. Additionally, if the load has any reactive component, the transistor will operate in its active

region, where the overlap of the drain-source voltage and current causes the undesired transistor power dissipation. This impairment is unavoidable.

5.4 Efficiency and Linearity Analysis

Some of the impairments that have been identified are always present (switch internal resistance and active region), so it is mandatory to quantify their real impact in both efficiency and linearity. Another impairment was referred (parasitic TL), but although it is not always present in every RF-CPB Tx, it is important to quantify also its influence in the system performance.

5.4.1 Efficiency

The RF-CPB Tx equivalent circuit and associated impairments reveal that the potential sources of efficiency losses are reduced to the transistor, since the other components are ideal non-dissipative. In this analysis it is assumed that the switching noise is negligible at the load, provided that the BPF efficiently attenuates it without any losses.

Therefore, we developed a group of tests to verify the impairments' impact in the system efficiency. In order to better understand the performance limits, we wanted to access the efficiency variation when the input power also changed or, in our case, when the coded envelope duty-cycle changed. For that, we used as the SMPA input signal an unmodulated RF Carrier multiplied by a square-wave with 10MHz of fixed fundamental frequency, but with variable duty-cycle. Then we calculated the drain efficiency, whose results for several impairments' conditions are presented in Fig. 90.

The first curve from the top (Eff_10M_S_Model_Ron) was obtained using only the switch R_{on} of 4 Ω and considering that everything else is ideal. As expected, with a pure sine wave as the input signal (duty-cycle of 100%) the efficiency achieved is not 100% due to the R_{on} losses. When the duty-cycle is reduced, the efficiency keeps a considerably high value, but it starts to drop abruptly for lower duty-cycle values. In this range, the output power level decreases, but the dissipated power in the R_{on} is always present, leading to the efficiency degradation. In the limit, when the duty-cycle is 50%, the switch is always working charging and discharging the BPF in equal amounts so that the output power is zero. However, the R_{on} dissipated power is not zero, leading to the zero efficiency.

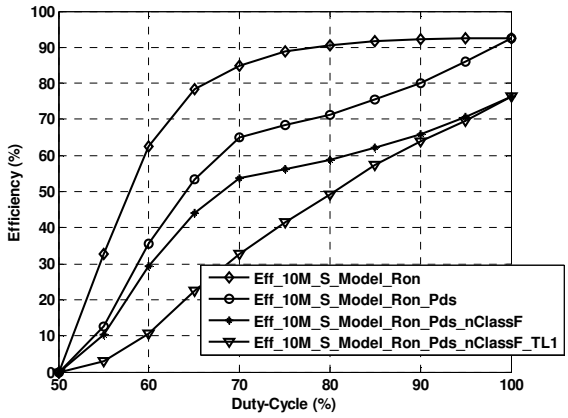


Fig. 90 – RF Carrier phase-burst efficiency vs Duty-cycle.

In the second top down curve (Eff_10M_S_Model_Ron_Pds), we replaced the switch model by a FET piecewise model with a similar R_{on}, but now considering that the FET has an active region. So, we are now modeling the effect of both R_{on} and active region.

As it can be seen, the efficiency starts to degrade immediately after the duty-cycle is changed back from 100%. This efficiency decrease is due to the increased overlap of the voltage and current in the transistor, whose effect was identified and described in Sub-Chapter 5.2.

In the third curve (Eff_10M_S_Model_Ron_Pds_nClassF), besides the previous effects, it is included the fact that, it is not possible to implement in practice, a Class-F PA with all the RF harmonics. So, in this case, we changed the output matching network to consider only the 2nd, 3rd, 4th and 6th, limiting the maximum achievable efficiency to 82.3%.

In the last case (Eff_10M_S_Model_Ron_Pds_nClassF_TL1), TL1 was inserted (10º) and, as expected, the efficiency degraded even further, evidencing that the T-type BPF rotation changed the transistor load line introducing more energy dissipation in its active area.

5.4.2 Linearity

Regarding the linearity, since these systems are mostly used with complex modulation signals, it is important to access the adjacent-band and in-band distortions. In order to obtain these results, the model previously developed, Fig. 89, is now tested with the dynamic input signal - CDMA2000 with 1.23 MHz of bandwidth. The amplitude is modulated by a PWM with 10 MHz of comparison frequency and the BPF is a LC 5th

order elliptic filter, centered at 450MHz, with 10MHz and 20MHz pass and attenuation bandwidths, respectively.

The distortion introduced by the identified impairments is verified by performance metrics in both frequency-domain (adjacent-channel power ratio, ACPR) and time-domain (normalized mean squared error, NMSE). The NMSE was independently evaluated for both amplitude and phase information as, in this architecture, these quantities are separately processed. Table 11 summarizes the results.

Table 11 – RF-CPB linearity analysis of the output signal vs impairments.

Case	Impairment	ACPR (dBc)	NMSE PHASE (dB)	NMSE AMP. (dB)
A	No	53	-86	-64
B	$R_{on} = 4\ \Omega$	52	-81	-58
C	TL1 10º ; R_{on}	52	-81	-58
D	R_{on} ; P_{ds}	43	-61	-31
E	TL1 10º ; R_{on} ; P_{ds}	42	-60	-30
F	TL1 20º ; R_{on} ; P_{ds}	41	-58	-29
G	TL1 30º ; R_{on} ; P_{ds}	39	-51	-28
H	PWM30M ; R_{on} ; P_{ds}	31	-52	-15

The reference Case A, presents the system linearity performance with no impairment, whose values serve as the base level for comparison with the remaining results.

Comparing the reference case with case B (R_{on}), the performance did not significantly changed. Almost no change was observed also in case C, where a small 1 mm (10º at 450 MHz for a board with ε_r of 4) TL was cumulatively introduced with case B. Now, when the transistor active region was introduced, case D, a significant performance degradation was observed. This degradation is evidenced by the worse values of ACPR and NMSE. A similar situation occurs when the TL1 is considered in cases E. The TL1 influence is

relatively small since when its size is further increased (cases F and G), the performance slightly degraded. Based in this observation, we conclude that the RF-CPB has some tolerance to the T-type filter rotation.

Additionally, in the last case (H), the envelope modulator was changed to a PWM with 30 MHz of comparison frequency, and both the ACPR as the amplitude NMSE suffered a considerable degradation, indicating that the issues caused by the input signal phase inversions, observed in the theoretical analysis, have also a large impact in the system linearity.

5.5 Prototype Development

Even if the use of a bipolar ATC in the RF-CPB transmitter has a small influence in the system level design, at circuit level, the impact is enormous.

Since the input SMPA signal exhibits now a constant envelope, as depicted in Fig. 80, the SMPA can have just one transistor. In the RF-CAB architecture, and during the input signal OFF periods, the second transistor-switch needs to close to keep the current continuity of the BPF. That is no longer necessary with the new modulation, as the amplitude voltage applied to the BPF is already continuous. In addition, it should be noted that, ideally, the carrier phase-burst keeps the 100% efficient and perfect linearity of the carrier amplitude-burst Tx. Therefore, the SMPA does not need the flywheel transistor neither its control signal, V_PULSE.

The schematic of the RF-CPB SMPA is depicted in Fig. 91.

As in RF-CAB, the Class-F SMPA was built with a GaN die transistor from Cree (CGH60008D) and designed to operate at a central frequency of 450MHz. The other elements are the same, such as the output matching network, the broadband input matching network and the output transmission line to achieve the required T-type BPF at the Class-F output. The bonding to the printed circuit board was also performed in house.

Besides the Class-F PA, the remaining blocks are also the same as in the RF-CAB. The Mini-Circuits ZHL-42W RF_Driver is used to properly drive the Class-F transistor into saturation, the same BPF recovers the envelope and the Tektronix AWG generates the RF phase-burst signal. Both the complete schematic of the used test prototype and the complete measurement setup are depicted in Fig. 92.and Fig. 93 respectively.

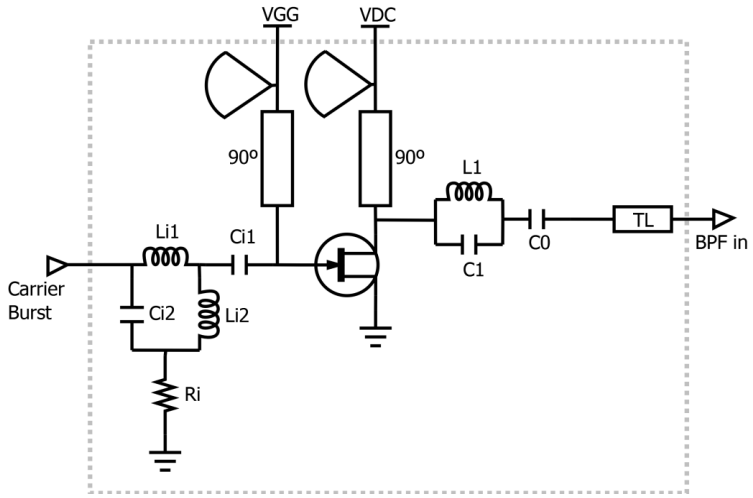


Fig. 91 – Schematic of the Class-F power amplifier.

5.6 Experimental Validation

5.6.1 Static Conditions

During the experimental validation we wanted to verify both the RF-CPB system functionality and performance. The devised architecture changes should overcome the main issue associated with the flywheel transistor, the output power limitation.

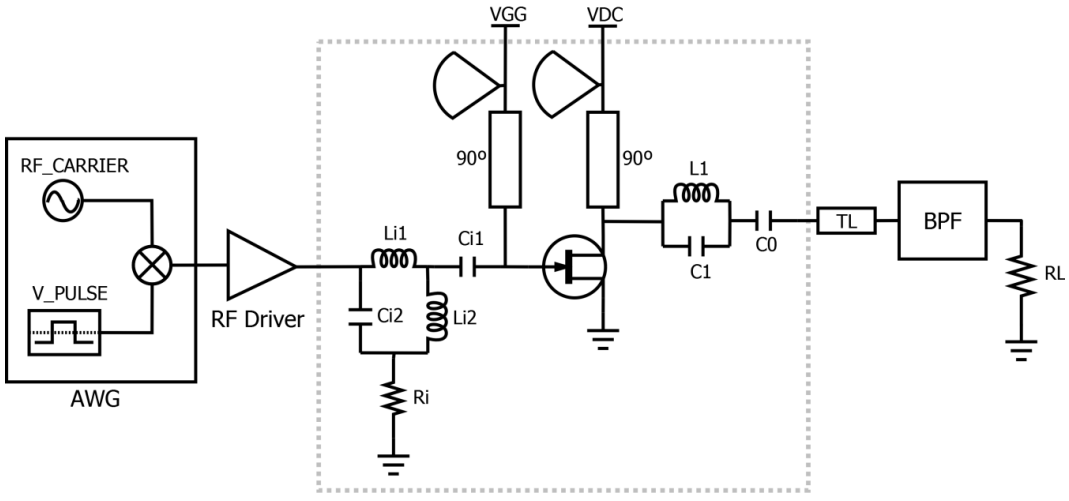


Fig. 92 – RF carrier phase-burst transmitter prototype schematic.

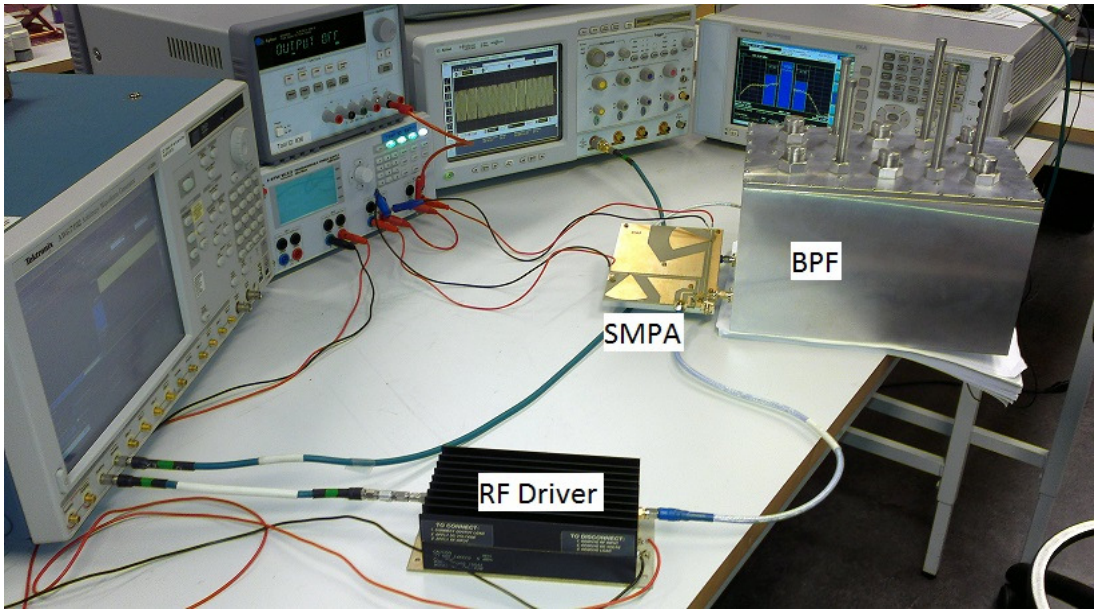


Fig. 93 – RF carrier phase-burst transmitter prototype and measurement setup.

Hence, we followed the same strategy as in the RF-CAB experimental tests. First the static tests, where the SMPA RF phase-burst input signal is constructed by the multiplication of a fixed frequency square wave with variable duty-cycle(to mimic a variable DC coded envelope) by a unmodulated RF carrier. The difference here is that the square wave levels are now +1 and -1 in order to achieve the desired RF phase-burst signal. At the BPF output the envelope amplitude is measured for each of the square wave duty-cycle values.

Fig. 94 shows the results of the prototype simulations (Vout_10M_S) and measurements (Vout_10M) compared with ideal ones (Vout_ideal). The simulated and measured values are in an almost straight line revealing that the system prototype seems to have a lower gain than the one ideally forecasted. Therefore, in order to have a better notion about the static linearity, the gain was compensated in the obtained data. The processed results are depicted in Fig. 95.

Although the measured values follow pretty well the simulated ones, which proves the simulation system validity, the results still deviates from the ideal line, indicating that the system is non-linear.

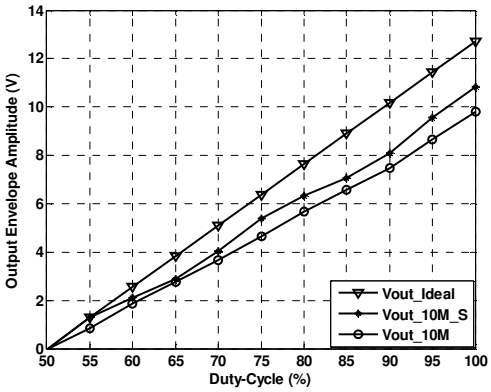


Fig. 94 – RF carrier phase-burst transmitter static linearity.

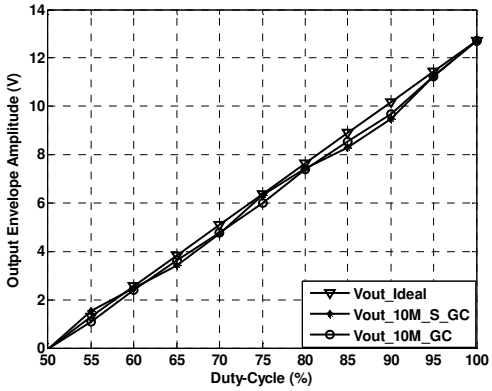


Fig. 95 – RF carrier phase-burst transmitter static linearity with gain compensation.

Regarding the Tx drain efficiency, Fig. 96 depicts the results for both prototype simulations (Eff_10M_S) and measurements (Eff_10M), compared with the values obtained with the impairments model (Eff_10M_S_Model_Ron_Pds_nClassF). Once again, not only the prototype measurements follow the simulations, which is another proof that the system prototype model is valid, but also the results are very similar to the ones forecasted by the impairments model. However, even though the CW efficiency is considerably good (78%), at the lower duty cycle values, the efficiency drops considerably.

The reason for this deterioration lie in the inherent system behavior, as previously referred. Since the SMPA is continuously working, when the duty-cycle decreases, so does the output power, but the SMPA is still sinking a DC power, leading to the efficiency decrease. The worse condition is the 50% duty-cycle, where it is expected to have zero output power and any DC power consumption result in a zero efficiency.

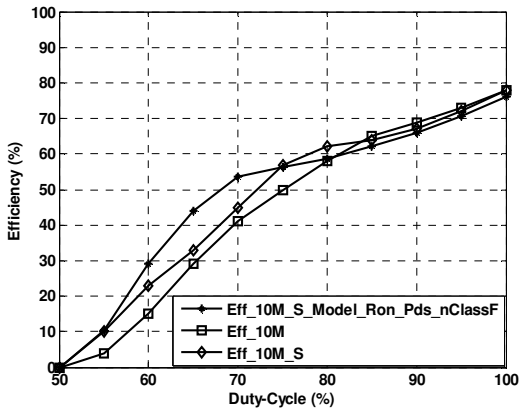


Fig. 96 – RF carrier phase-burst transmitter static efficiency.

5.6.2 Dynamic Conditions

In the dynamic environment, the RF-CPB system was tested with the CDMA2000 input signal. The RF carrier phase-burst signal was constructed, as previously described, with the envelope coded with a PWM 10MHz ATC.

Table 12 summarizes the obtained results from both simulations and measurements. It is presented the average output power, efficiency and linearity as the adjacent channel power ratio (ACPR). Comparing these results with the RF-CAB system ones, the RF-CPB performance, in similar conditions, provides slightly less output power (around 1dB), better linearity (around 3dB) and lower efficiency (around 10%) despite the good 60% average value. These results prove the system validity, showing that it is possible to have a burst system with a single unipolar SMPA.

In a step forward to further verify the RF-CPB system flexibility, the previous output bias conditions (V_{DC} equal to 10 V) was changed and the tests repeated. The results are presented in Table 13, where it is possible to see that when the power supply voltage increases, the output power also increases (the RF_Driver output signal was adjusted accordingly), proving once again that the flywheel transistor independency. However, the efficiency and linearity do not significantly change.

Table 12 – Measured and simulated output power, efficiency and linearity for a PWM-10MHz ATC.

	Power	Efficiency	ACPR
Simulation	25.2 dBm	60%	34.0 dBc
Measurement	24.7 dBm	59%	34.9 dBc

Table 13 – Measured output power, efficiency and linearity for a PWM-10MHz ATC and for different power supply values.

V_{DC}	Power	Efficiency	ACPR
15 V	28.2 dBm	60%	34.4 dBc
20 V	30.5 dBm	59%	34.3 dBc

5.7 RF-CPB Performance Limits

The previous tests, used in the majority of the conditions, the PWM 10MHz ATC so that it was possible to compare the RF-CPB and RF-CAB performance. However, as previously described, it is also possible to use other ATCs, which have different timing characteristics. So, before we present the results of the RF-CPB performance for other ATCs, we use the same procedure as in the RF-CAB analysis, by first presenting the static performance. Therefore, the simulated and measured output envelope voltage versus the square wave duty-cycle are respectively depicted in Fig. 97 and Fig. 98. The gain was compensated to ease the comparison.

When the envelope square wave frequency increases, the difference between the results (simulated and measured) and the ideal ones is higher. This indicates that, similarly to what happened with the RF-CAB, the RF-CPB system linearity is directly influenced by the ATC time characteristics.

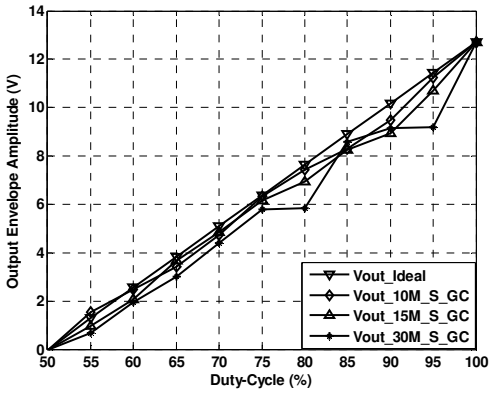


Fig. 97 – RF carrier phase-burst transmitter simulated static linearity for several square wave frequencies.

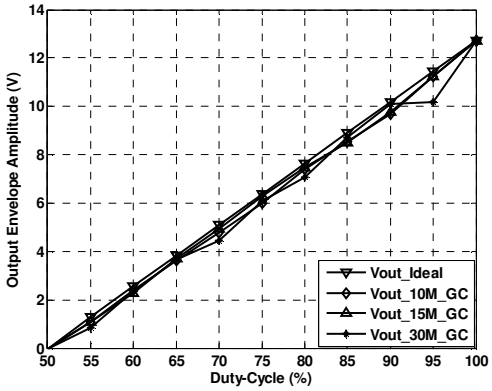


Fig. 98 – RF carrier phase-burst transmitter measured static linearity for several square wave frequencies.

Similar behavior is observed when the static efficiency is analyzed. Fig. 99 and Fig. 100 illustrate respectively the simulated and measured efficiency for several square wave frequencies, where it is showed the efficiency decrease when the coded envelope frequency increases.

To complete the analysis, the RF-CPB was tested in the dynamic environment using the aforementioned ATC and the CDMA2000 signal. The results are presented in Table 14. In this case, the values for the SD3 ΣΔM are not presented, because they are very similar to the CRFB3 ΣΔM ones. Once again, the simulations and measurements have close figures. As expected from the static results, both linearity and efficiency degrade when the PWM frequency increases and when the ΣΔM sampling frequency also increases.

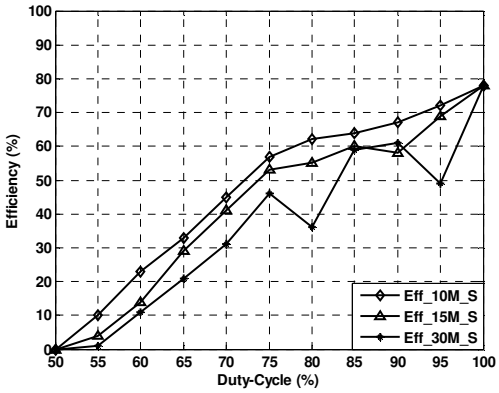


Fig. 99 – RF carrier phase-burst transmitter simulated static efficiency for several square wave frequencies.

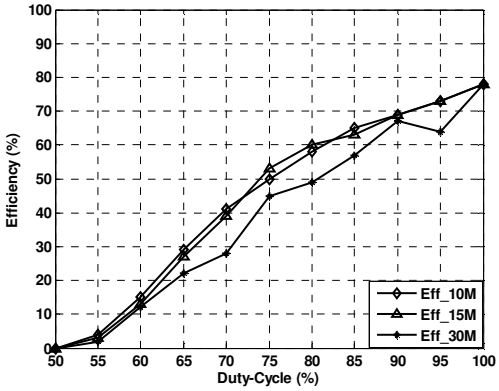


Fig. 100 – RF carrier phase-burst transmitter measured static efficiency for several square wave frequencies.

Additionally, the normalized power spectrum for a CRFB3 150MHz ΔΣM is depicted in Fig. 101 (simulation) and Fig. 102 (measurement).

5.8 Conclusions

This Chapter presented the RF-CPB, an alternative to the RF-CAB, proposed to overcome one of its main issues, the flywheel. We have shown that this architecture shares some of the RF-CAB characteristics, namely the ideal perfect efficiency and linearity.

We have shown that, a change of the amplitude to time converter output levels, to bipolar symmetrical values, allowed us to do significant improvements to the carrier amplitude-burst transmitter implementation. The new proposed implementation – with just

one transistor – overcomes the output power limitations present in binary amplitude carrier-burst transmitters and keeps the same efficiency and linearity.

Measurements performed in a practical prototype under both static and dynamic excitations (CDMA2000 modulated signal) under duty-cycle modulation, which were in agreement with the corresponding simulations, served to corroborate our described mode of operation and the promised potentiality of this new SMPA based wireless transmitter.

Table 14 – RF carrier phase-burst transmitter measured and simulated performance (efficiency and linearity) for several envelope modulators.

Modulator	Measurements		Simulations	
	ACPR (dBc)	Efficiency (%)	ACPR (dBc)	Efficiency (%)
PWM 10MHz	34.9	59	34.0	60
PWM 15MHz	35.0	57	34.3	56
PWM 30MHz	33.6	48	30.5	45
CRFB3 90MHz	29.0	45	26.0	41
CRFB3 150MHz	26.1	35	25.5	34

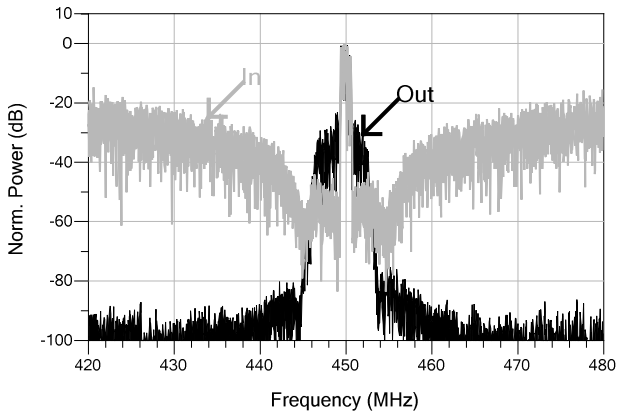


Fig. 101 – Simulated input and output CDMA2000 signal with CRFB3-150MHz envelope modulator.

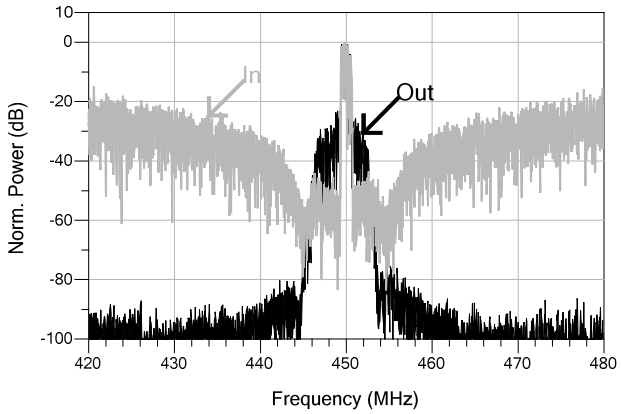


Fig. 102 – Measured input and output CDMA2000 signal with CRFB3-150MHz envelope modulator.

Chapter 6 – Conclusions and Future Research

This thesis addresses the reconfigurability and efficiency of wireless transmitters. In particular it was presented the study of the RF carrier amplitude-burst architecture, which was selected after a thorough state-of-the-art review of digital intensive transmitters.

It was proved that this architecture can ideally achieve perfect linearity and efficiency, being immune to the amplitude to time converter (ATC) coding efficiency. At system level, the design is straightforward, being only necessary to guarantee that, the ATC properly codes the envelope up to the desired linearity level, and that the switching noise introduced by the ATC is removed by the BPF, to fully recover the smooth envelope. The blocks' definition and design requirements can be specified entirely in the frequency domain, but when the system is translated into a practical circuit, this type of analysis is not enough. It was found that the circuits' interaction, in particular the SMPA and BPF, due to the input signal burst characteristics, also demands a time domain analysis. This aspect was one of my major difficulties, because after years of designing power amplifiers based in the spectrum characteristics, it was not easy to develop new time analysis skills. In fact, this thesis contributes also to lessen the literature lack of information in this field.

With this new information, it was proved that, not only there is a one to one matching between the amplifier types and BPF topologies that can be used in a RF-CAB transmitter, but also that the usage of voltage mode single-ended SMPAs requires the insertion of a flywheel to guarantee the proper system functionality. With the presented new general methods, the observed performance is far better than the one previously reported by other researchers, but the architecture is affected by the components impairments and limitations, which restrains its practical potential.

The success achieved with this thesis, in which the complete model for the RF-CAB transmitter was presented, paves the way to the identification of its strengths and weaknesses for future improvements. Therefore, in order to overcome some of the identified problems of the RF-CAB, another architecture was proposed: the RF carrier phase-burst. Although this architecture can be implemented in practice without the flywheel, this solution still shares some of the RF-CAB difficulties, which also limits its full potential.

Considering other architectures that are also digital intensive, such as the earlier described RF-PWM, BP-ΣΔM or even RF-DAC, I believe that the methods presented in this thesis for the RF-CAB architecture, can also be considered for these other architectures. Since the switching signals are often used to increase the transmitters' efficiency, the time domain analysis provides an essential complement when the observed blocks interaction is studied, especially when the repeatedly neglected BPF is inserted.

So, though the presented proposals for this architecture are a considerable contribute to the state of the art, there is still room for further future improvements. In particular, it was concluded that the reconstruction bandpass filter requirements must be relaxed, especially the bandwidth that must be wider. This is a key factor for the RF-CAB or RF-CPB to be able to operate with larger channel bandwidths. However, in order to achieve this performance, the ATC must be able to increase its noise free bandwidth. A solution presented by Hori in [60] is worth to be further explored. In the RF-CAB transmitter, it was proposed to implement the ATC with a first order sigma delta modulator and whose clock signal is the phase modulated RF carrier. With this method, the noise free bandwidth is very wide allowing a simpler BPF implementation. However, the potential issue of the idle tones should be investigated.

As was proved in this thesis, single-ended SMPAs used in the RF-CAB experience a significant degradation when the coded envelope frequency increases, or the pulse duration decreases. Therefore, since the Hori solution uses a very high sampling frequency, the sigma delta pulse duration is very short, being expected a significant performance degradation. So, another alternative is necessary.

With the technology evolution, the Class-D power amplifiers are having an increasing interest by the research community, [61]. The researchers reported a CW drain efficiency of 84% for 5 W output power at 0.85 GHz central frequency. In that work, it was used the totem pole configuration for the Class-D, which is also the more suitable option for the RF-CAB architecture, but the performance difference between the N channel and P channel devices, puts additional difficulties during its implementation. In [61] it was proposed two N channel devices, but this solution requires an extremely high driving voltage signal for the top device. Nevertheless, this option might be subject of future investigation.

In the civil telecommunications context, the small cells application can be a niche market for this architecture, due to its lower maximum power requirements. However, in

addition to the BPF bandwidth that must be increased, to be commercially more attractive, the multiband capabilities must also be further developed. Regarding this subject the BPF reconfigurability is an area that can also be explored.

In a final remark, although there so much to explore with these transmitter types, this thesis will be very helpful to clarify some of the doubts that may arise when the SDR developers, regardless of the switching transmitter type, insert a BPF to reduce their systems switching noise.

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Annex A - Design of Cavity Filters

Filters are an integrant part of almost every radio system and its performance requirements have been increasing in parallel with the complexity rise of nowadays wireless systems. The filters are so important that a great deal of material on the theory and design is widely available in the literature [54], [57], [62–64].

Nowadays, many RF systems (e.g. RF-CAB transmitter) demand high performance filters, such as cavity filters, which are not easy to design and implement. So, based in the current literature, this annex describes a procedure to design these filter types.

A.I Lowpass Prototype

A.I.1 Butterworth and Chebyshev

Fig. 103 depicts the lumped element circuit of a n-order lowpass prototype filter. Either Butterworth or Chebyshev approximations use this circuit or its dual, shown in Fig. 104, where the first reactive element is connected in shunt to ground.

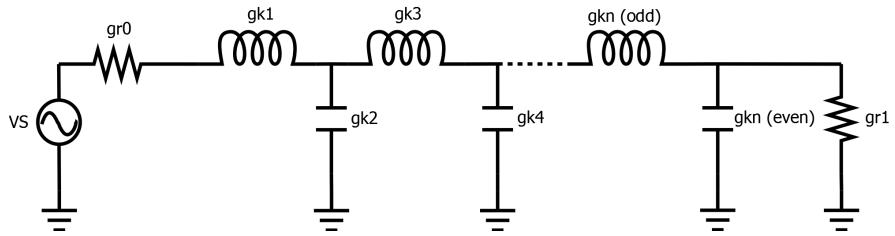


Fig. 103 – Butterworth or Chebyshev lowpass filter prototype schematic with a series first element.

In both forms, *gkx* represent the values of the inductances and capacitances of the reactive elements, while *grx* are the values of the terminal impedances (usually pure resistances) of the source and load. The *g* values of these lowpass filters and for the desired frequency response can be either calculated through closed equations, or selected from tabulated data whose values have been previously obtained. All values are normalized, which means that *grx* equals to 1 Ω or 1 S.

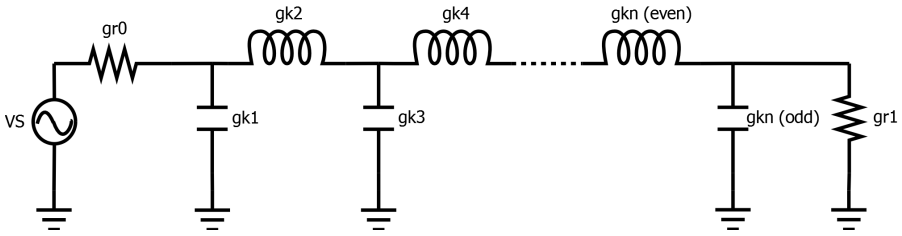


Fig. 104 – Butterworth or Chebyshev lowpass filter prototype schematic with a parallel first element.

In the amplitude frequency response, the cutoff frequency (*Wp*) is also normalized to 1 rad/s, as indicated in Fig. 105 for the Butterworth approximation.

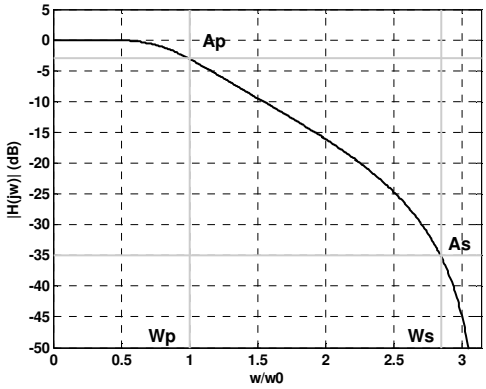


Fig. 105 – Butterworth lowpass filter amplitude frequency response.

Wp is defined as the frequency value where the amplitude frequency response drops 3 dB from its maximum and represents the passband limit. *Ws* is another parameter also necessary to calculate the filter coefficients, which defines the frequency at which the desired attenuation (*As*) must be achieved. The difference between *Ws* and *Wp* is called the transition band.

Contrary to the Butterworth maximum flat passband, in Chebyshev type I filter shown in Fig. 106, it is necessary to define the passband ripple (*G*) in dB. This value also defines the passband frequency (*Wp*). However, it is possible to obtain the filter coefficients also for 3 dB cutoff frequency, even if the *G* has another value. Just for reference, the Chebyshev type II filter has the ripple defined in the stopband instead.

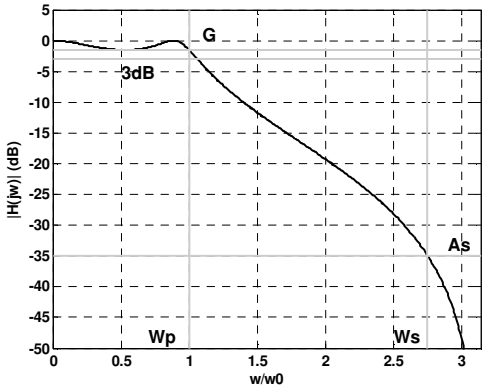


Fig. 106 – Chebyshev I lowpass filter amplitude frequency response.

The coefficients can then be scaled to another cutoff frequency and adjusted to different load and source impedances, using (42) and (43).

$$\left.\begin{matrix} g_r = 1\,\Omega \\ \omega_0 = 1\ rad\ /\ s \end{matrix}\right\} \Rightarrow \left\{\begin{matrix} G_r = R\,\Omega \\ \Omega_0 = 2\pi f_0\ rad\ /\ s \end{matrix}\right. \tag{42}$$

$$\begin{cases} X_1 = \dfrac{g_r}{G_r}\dfrac{1}{2\pi f_0}\, g_{k1} \\ X_2 = \dfrac{g_r}{G_r}\dfrac{1}{2\pi f_0}\, g_{k2} \end{cases} \tag{43}$$

A.I.2 Quasi-Elliptic

Contrary to the Butterworth and Chebyshev type I responses, in which all the transmission zeros are at infinite frequencies, the Chebyshev type II and the elliptic responses have the transmission zeros at finite frequencies. This difference increases the elliptic and the type II Chebyshev filters performance, because for the same attenuation and similar number of elements (order), the transition band is lower. However, since it is difficult to synthesize and implement these filters, a quasi-elliptic alternative is used, which has the transmission zeros at both finite and infinite frequencies. The typical response of quasi-elliptic filters is shown in Fig. 107.

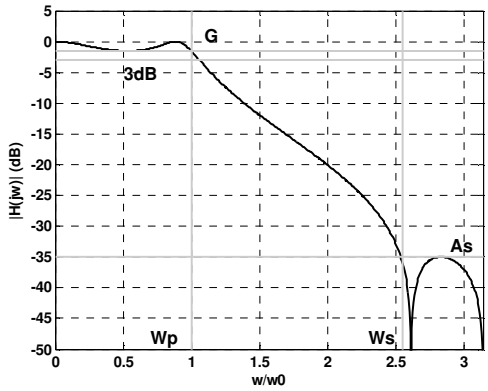


Fig. 107 – Quasi-elliptic lowpass filter amplitude frequency response.

The lowpass prototype schematic is slightly different from the Butterworth and Chebyshev ones, as depicted in Fig. 108 and Fig. 109 (its dual). As the transmission zeros are now also at finite frequencies, either a horizontal LC parallel or a vertical LC series must be present to implement them.

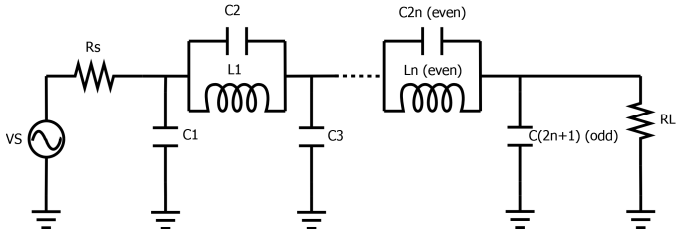


Fig. 108 – Quasi-elliptic lowpass filter prototype schematic with series transmission zeros.

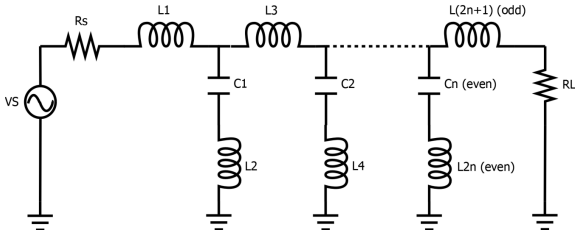


Fig. 109 – Quasi-elliptic lowpass filter prototype schematic with parallel transmission zeros.

Unlike the Butterworth and Chebyshev lowpass prototype filters, there is no simple formula available for determining element values of the quasi-elliptic function lowpass prototype filters. Several algorithms have been developed for providing a suitable approximation to the filter desired response, which are also used for the frequency scaling.

A.II Lowpass to Bandpass Transformation

The bandpass filters are largely used in RF systems, being necessary to find a proper mapping that can relate the lowpass to the bandpass response. Starting from the lowpass filter scaled in frequency, whose amplitude frequency response is represented in the left side of Fig. 110, the objective is to achieve the bandpass response depicted in the right side of Fig. 110.

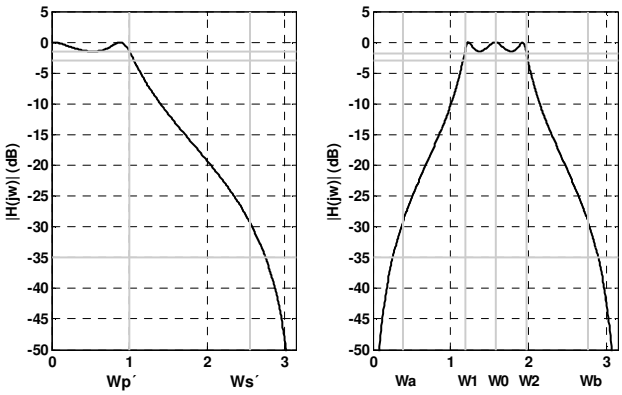


Fig. 110 – Lowpass and bandpass filters equivalent amplitude frequency response.

Therefore, the difference between the upper and lower cutoff frequencies (ω_1 and ω_2) is equal to the lowpass filter bandwidth $\omega_{p'}$,

$$\omega_p' = \omega_2 - \omega_1 \tag{44}$$

and their geometric mean is equal to the bandpass filter central frequency,

$$\omega_0 = \sqrt{\omega_2 \times \omega_1} \tag{45}$$

With these two equations, it is possible to determine the bandpass frequency response, but in order to have a proper circuit, the lowpass circuit (Fig. 103) must be changed into the one depicted in Fig. 111.

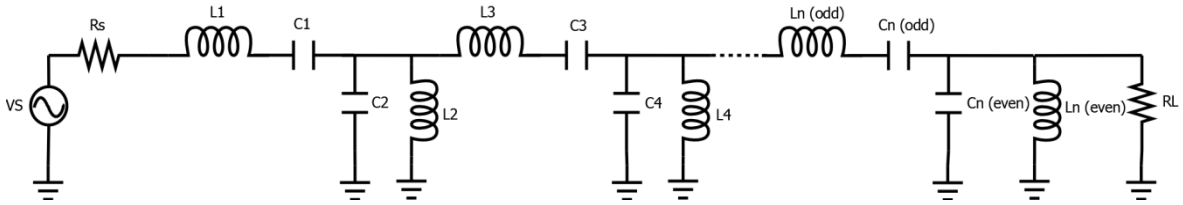


Fig. 111 – Butterworth or Chebyshev Bandpass filter schematic example from a lowpass prototype with a series first element.

At each of the series inductor, a series capacitor was added, whose value can be calculated as,

$$C_S = \frac{1}{(2\pi f_0)^2 L_S} \tag{46}$$

Similarly, at each parallel capacitor, a parallel inductor is added, and its value is,

$$L_{SH} = \frac{1}{(2\pi f_0)^2 C_{SH}} \tag{47}$$

This procedure is valid for the Butterworth and Chebyshev responses, but for the quasi-elliptic, an algorithm must be used.

A.III Coaxial Cavities

Among the large variety of ways to construct filters, the cavity ones are well known for their very low insertion loss due to resonators high quality factor. It is possible to implement cavity filters in many structures, but for the GHz range of frequencies, the coaxial cavity filters are one of the most popular configurations.

A.III.1 Coaxial cavity filters

In Fig. 112 it is presented the interdigital and combline, two of the most common coaxial cavity filter types.

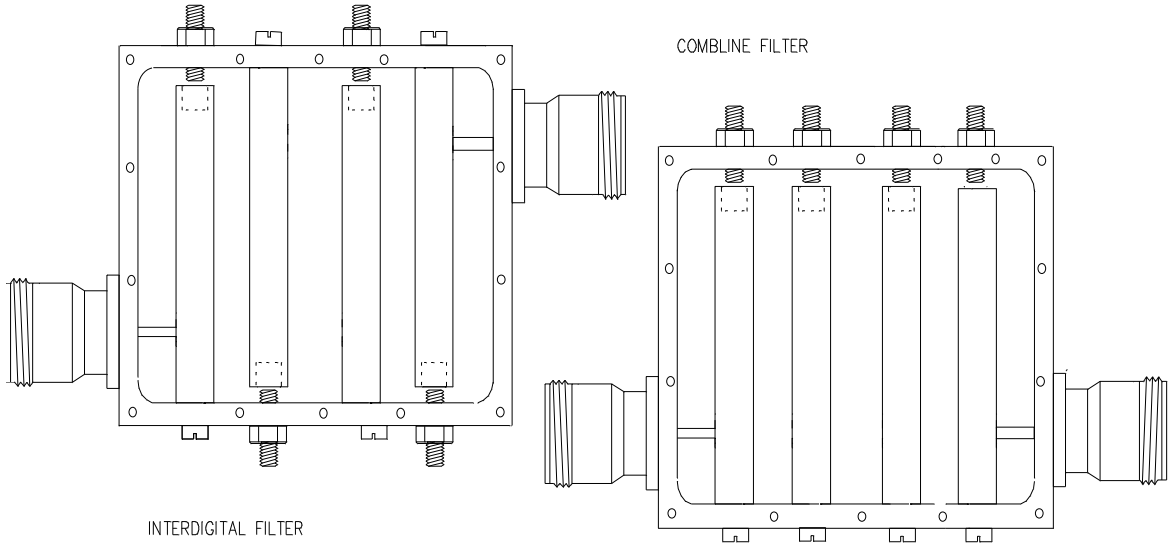


Fig. 112 – Interdigital and combline cavity filter drawing example.

The interdigital filter is composed by resonators, symmetrically coupled, with the resonators connected to ground at opposite ends and enclosed by a metal cavity. This cavity provides a shield that prevents the electromagnetic field to radiate to the free space. The input and output is placed at the extremities, bonding the external connectors to the resonators placed at each end.

The combline filter is slightly different, where the resonators have the ground connection at the same end. Usually, the combline structure is more compact and provides a better stopband performance.

In both types, the cavities resonating frequency is dependent on their physical dimensions. The vertical electrical length of the central rod must be $\lambda/4$ to achieve resonance, but due to reasons that will be later clarified, the physical length is usually smaller (between [0.5 ... 0.8]x$\lambda/4$).

A.III.2 Resonator Model

Fig. 113 depicts the face view of a single cavity. As briefly introduced, each cavity is composed by a fixed rod (*FR*), which has one end connected to ground and a tuning rod (*TR*) whose separation to the *FR* can be adjusted.

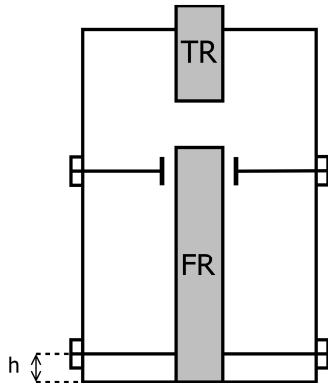


Fig. 113 – Combline single cavity resonator face view.

The connection to the exterior can be magnetic with a lower connection, which physically links the external connector to the *FR*. Or it can be electrical, with a upper connection made by an electrical coupling. Usually the magnetic connection provides a better mechanic stability.

This physical element is equivalent to a parallel RLC resonator, as shown in Fig. 114, which can be used to model its electrical behavior. The inductance (*L*) is dependent on the length of the *FR*, the capacitance (*C*) is related to the separation distance between the *FR* and the *TR* and the resistance (*Rsh*) accounts for the cavity dimensions and construction quality (quality factor).

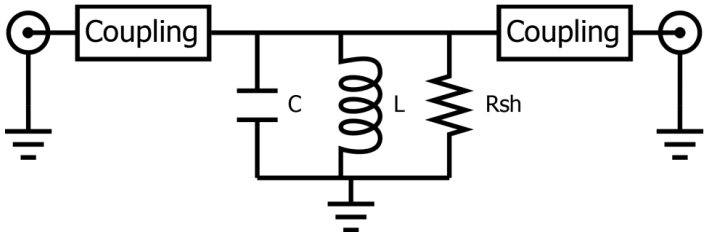


Fig. 114 – Combline single cavity resonator equivalent model with lumped elements.

As previously described in (27), every resonator has the ability to store and deliver energy, but with some losses, which depend on its physical characteristics. In the case of combline cavities, the unloaded quality factor can be calculated as,

$$Q_U = \frac{0.75 n \lambda \sqrt{4\pi^2 f_0 \sigma 10^{-7}}}{4 + n \frac{\lambda}{D_2} \frac{1 + \frac{D_2}{D_1}}{\ln\left(\frac{D_2}{D_1}\right)}} \tag{48}$$

where, f_0 is the resonant frequency, σ is the material conductivity, D_2 is the cavity side length, D_1 is the *FR* diameter, λ is the wavelength at f_0, n is the resonator length expressed in quarter wavelength and 0.75 is a factor to estimate material and construction imperfections (roughness, influence of tuning screws,...)

These cavities can be constructed using an horizontal squared shape (more usual), as depicted in Fig. 115, or circular, as shown in Fig. 116.

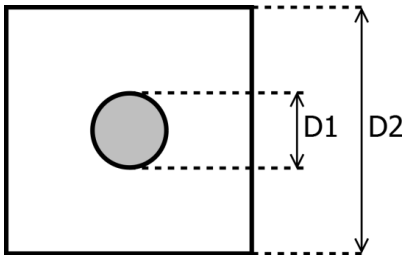


Fig. 115 – Combline squared cavity resonator horizontal dimensions.

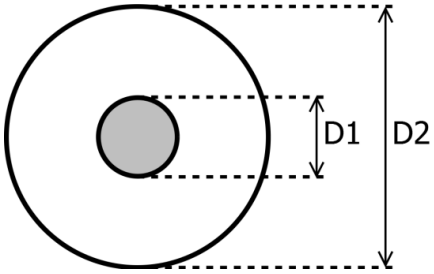


Fig. 116 – Combline circular cavity resonator horizontal dimensions.

In either cases, the *Qu* approximation provided by (48) can be used.

A.III.3 Approximate Analysis

Taking into account the coaxial line physical dimensions, its characteristic impedance can be calculated by,

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{D_2}{D_1}\right) \tag{49}$$

In our case, as the outer configuration is rectangular and the dielectric is air (ε_r=1),

$$Z_0 = 59.952\left[\ln\left(\frac{D_2}{D_1}\right) + 0.06962\right] \tag{50}$$

Considering that the lower losses are present when Z_0 = 77 Ω, then,

$$\frac{D_2}{D_1} = 3.369 \tag{51}$$

However, *Qu* increases when this ratio increases, so the integer value of 4 is consensual. D_1 and D_2 absolute values are then calculated using the desired unloaded quality factor and knowing that the best characteristic impedance is 77 Ω and the relation between these two dimensions must be 4.

Extending this analysis, using a transmission line, in Fig. 117 it is shown the cavity equivalent circuit.

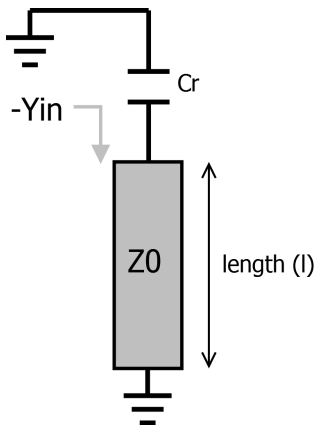


Fig. 117 – Combline cavity resonator equivalent circuit.

It is composed by the transmission line with length *l* and characteristic impedance Z_0, and by *Cr*, which represents the total capacitance between the center rod and the walls plus tuning rod

At resonance (ω_0), the total parallel admittance of the transmission line and the capacitor must be zero,

$$Y_{in} + j\omega_0 C_r = \frac{Y_0}{j\tan(\theta_0)} + j\omega_0 C_r = 0 \Rightarrow C_r = \frac{1}{Z_0 \tan(\theta_0)\omega_0} \quad (52)$$

where θ_0 is the electrical length of the central rod.

If l equals $\lambda/4$ then θ_0 equals $\pi/2$, so Cr should be zero. It would require an infinite distance between the center rod and the walls. This is the main reason for which the fixed rod electrical length must be less than $\lambda/4$.

The exact determination of Cr is not simple, due to other factors involved (cavities imperfections and construction margins), so a certain margin is kept for fine tuning.

A.IV Lumped Circuit Adaptation

The filter shown in Fig. 111 consist of series tuned resonators alternating with shunt tuned resonators. It is very difficult, if not impossible, to directly implement this filter with cavity resonators. A way to modify the circuit is to use impedance (K) and admittance (J) inverters, so that all the resonators can be of the same type, and still keeping the same transfer function characteristics.

A.IV.1 Inverters

One of the most common is the quarter wavelength transformer, where the input impedance is inversely related with the load impedance by the characteristic impedance squared,

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (53)$$

In a more general way, the ideal impedance inverter is a block, depicted in Fig. 118, which, when connected to a load, presents at its input and at all frequencies, the inverted load impedance. K is the impedance inverting factor.

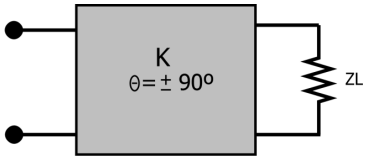


Fig. 118 – Impedance inverter connected to a load.

Referring back to the quarter wavelength transmission line, the impedance inverting factor, K, is the characteristic impedance Z_0,

$$Z_{in} = \frac{K^2}{Z_L} \quad \Rightarrow \quad K = \sqrt{Z_{in} Z_L} \tag{54}$$

The ABCD matrix of this impedance inverter is,

$$\begin{bmatrix} 0 & \pm jK \\ \pm \dfrac{j}{K} & 0 \end{bmatrix} \tag{55}$$

Similarly, as shown in Fig. 119, an ideal admittance inverter is also definable,

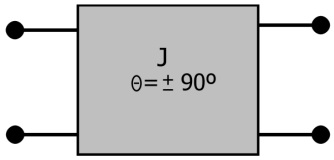


Fig. 119 – Admittance inverter block diagram.

whose ABCD matrix is,

$$\begin{bmatrix} 0 & \pm \dfrac{j}{J} \\ \pm jJ & 0 \end{bmatrix} \tag{56}$$

These inverters can be used to transform the resonator circuits. For example, a LC parallel resonator, Fig. 120, with the resonant frequency defined by (57), can be implemented by the circuit depicted in Fig. 121.

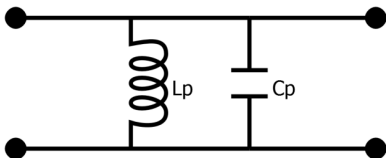


Fig. 120 – Parallel LC resonator schematic.

$$L_p C_p = \frac{1}{\omega_0^2} \tag{57}$$

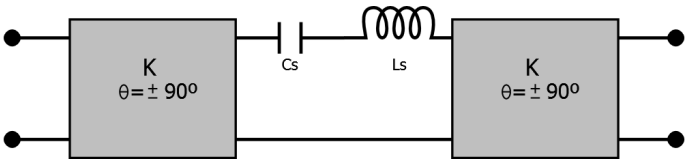


Fig. 121 – Equivalent circuit of a parallel LC resonator - Series LC resonator with equal impedance inverters at each end.

This circuit consists of a LC series resonator with an impedance inverter connected at each end, whose inverting factor is defined by,

$$K = \omega_0 \sqrt{L_s L_p} \tag{58}$$

Additionally, L_s and C_s can be calculated by,

$$\begin{cases} C_s = \dfrac{1}{L_s \omega_0^2} \\ L_s C_s = L_p C_p = \dfrac{1}{\omega_0^2} \end{cases} \tag{59}$$

The above example showed a transformation from a LC parallel resonator into a LC series resonator, but the opposite is also possible. Therefore, the resonator shown in Fig. 122, whose resonant frequency is defined by (60), can be transformed into the LC parallel resonator with the impedance inverters connected at each end, as depicted in Fig. 123.

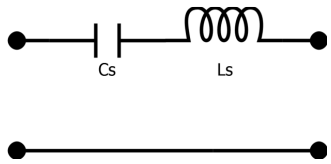


Fig. 122 – Series LC resonator schematic.

$$L_s C_s = \frac{1}{\omega_0^2} \tag{60}$$

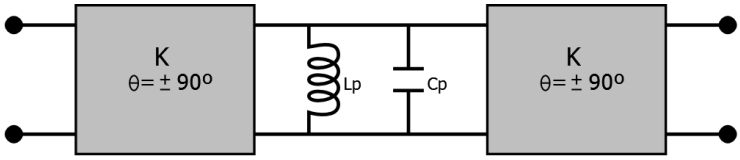


Fig. 123 – Equivalent circuit of a series LC resonator - Parallel LC resonator with equal impedance inverters at each end.

The impedance factor is as expected the same as in the previous example,

$$K = \omega_0 \sqrt{L_s L_p} \tag{61}$$

Once again, L_p and C_p can be calculated by,

$$\begin{cases} C_p = \dfrac{1}{L_p \omega_0^2} \\ L_s C_s = L_p C_p = \dfrac{1}{\omega_0^2} \end{cases} \tag{62}$$

In Fig. 124 it is represented an equivalent circuit of a parallel LC resonator, using two different impedance inverters.

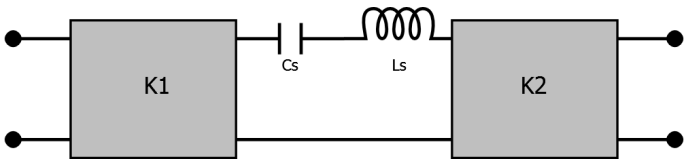


Fig. 124 – Equivalent circuit of a parallel LC resonator - Series LC resonator with different impedance inverters at each end.

This circuit can be transformed into an equivalent circuit, implemented with the same impedance inverter at each end, as shown in Fig. 125. In this transformation, not only the impedance inverters must be changed, but also the LC series resonator values, by using,

$$\begin{cases} K = K_1\sqrt{\dfrac{L_s^{'}}{L_s}} \\ K = K_2\sqrt{\dfrac{L_s^{'}}{L_s}} \\ C_s^{'} = \dfrac{1}{L_s^{'}\omega_0^2} \\ L_s C_s = L_s^{'} C_s^{'} = \dfrac{1}{\omega_0^2} \end{cases} \tag{63}$$

If a parallel LC resonator is used in Fig. 124, implementing an equivalent circuit for a LC series resonator, the same calculation method described by (63) can used, being necessary to replace the inductor and capacitor values.

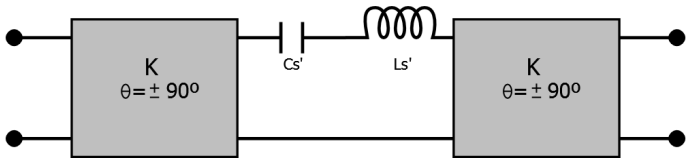


Fig. 125 – Equivalent circuit of the series LC resonator with different impedance inverters at each end.

The above described transformation properties are very useful to change the circuits according to our needs. For instance, the circuit depicted in Fig. 126 is composed by two different LC series resonators connected at each end by an impedance inverter.

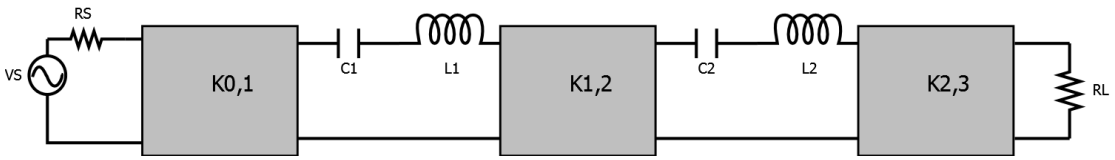


Fig. 126 – Two different series LC resonators coupled with different impedance inverters.

The resonance frequency values are dependent on the component values,

$$\begin{cases} C_1 = \dfrac{1}{L_1 \omega_1^2} \\ C_2 = \dfrac{1}{L_2 \omega_2^2} \end{cases} \tag{64}$$

Depending on the components availability, or their internal characteristics, it might be beneficial to replace them. So, the resulting circuit is depicted in Fig. 127, where both the resonators components and the impedance inverters have changed.

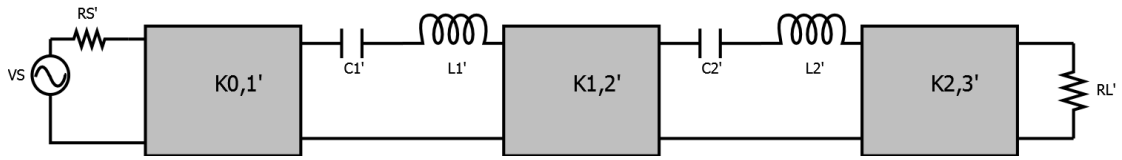


Fig. 127 – Transformation of the two different series LC resonators coupled with different impedance inverters into an equivalent circuit with equal LC series resonators.

Consequently, the blocks' individual values can be calculated by,

$$\begin{cases} K'_{0,1} = K_{0,1}\sqrt{\dfrac{R'_s}{R_s}\dfrac{L'_1}{L_1}} \\ K'_{1,2} = K_{1,2}\sqrt{\dfrac{L'_1}{L_1}\dfrac{L'_2}{L_2}} \\ K'_{2,3} = K_{2,3}\sqrt{\dfrac{L'_2}{L_2}\dfrac{R'_L}{R_L}} \\ C'_1 = \dfrac{1}{L'_1 \omega_1^2} \\ C'_2 = \dfrac{1}{L'_2 \omega_2^2} \end{cases} \tag{65}$$

The same procedure can be applied to a circuit with just parallel resonators, as shown in Fig. 128. In this case, as will be explained in the next Sub-Chapter, the admittance inverters are used, replacing the impedance ones, but this difference do not affect the procedure application. The modified circuit is depicted in Fig. 129.

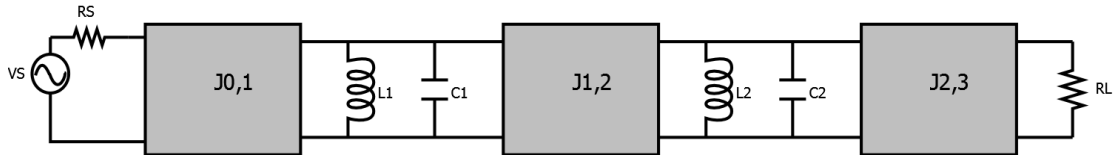


Fig. 128 – Two different parallel LC resonators coupled with different admittance inverters.

$$\begin{cases} L_1 = \dfrac{1}{C_1 \omega_1^2} \\ L_2 = \dfrac{1}{C_2 \omega_2^2} \end{cases} \tag{66}$$

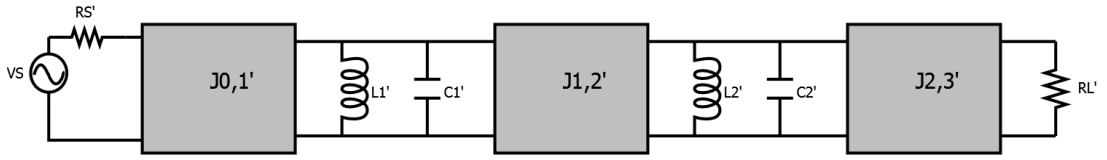


Fig. 129 – Transformation of the two different parallel LC resonators coupled with different admittance inverters into an equivalent circuit with equal LC parallel resonators.

In a similar way, the blocks' individual values can be calculated by,

$$\begin{cases} J_{0,1}^{'} = J_{0,1}\sqrt{\dfrac{R_s^{'}}{R_s}\dfrac{C_1^{'}}{C_1}} \\ J_{1,2}^{'} = J_{1,2}\sqrt{\dfrac{C_1^{'}}{C_1}\dfrac{C_2^{'}}{C_2}} \\ J_{2,3}^{'} = J_{2,3}\sqrt{\dfrac{C_2^{'}}{C_2}\dfrac{R_L^{'}}{R_L}} \\ L_1^{'} = \dfrac{1}{C_1^{'}\omega_1^2} \\ L_2^{'} = \dfrac{1}{C_2^{'}\omega_2^2} \end{cases} \tag{67}$$

A.IV.2 Inverters Implementation

The impedance and admittance inverters used in the previous analysis where assumed to be ideal and frequency independent. Obviously these inverters do not exist, but they can be applicable in narrowband filters. In the small pass bandwidth the response of the inverters can be approximated to the ideal behavior. As said before, the quarter-wavelength transmission line acts as an inverter, but there are situations in which a lumped element inverter model, is more convenient.

Let's consider the Fig. 130 circuit where two parallel LC resonators are magnetically coupled.

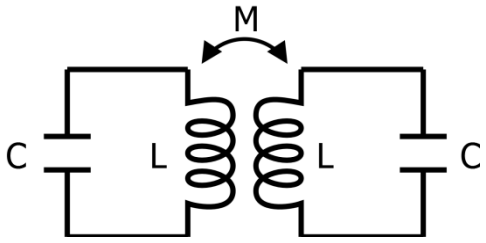


Fig. 130 – Example of two parallel LC resonators magnetically coupled.

It is possible to translate this circuit into an equivalent one (with equal loop currents and resonant frequencies), as shown in Fig. 131, where the inductance of both resonators decreases by the amount of coupling inductance.

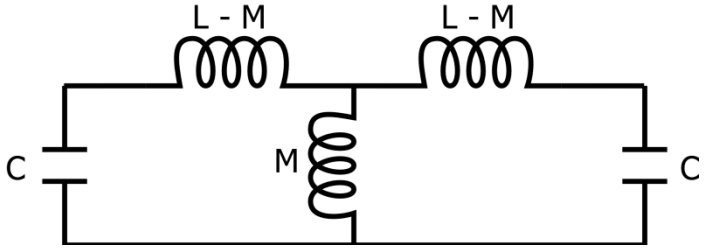


Fig. 131 – Equivalent circuit of the two parallel LC resonators magnetically coupled.

Therefore, isolating the components responsible for the coupling, we end up having the following circuit, which implements an impedance inverter.

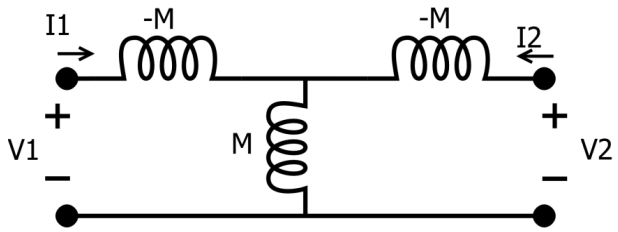


Fig. 132 – Impedance inverter inductor equivalent T circuit.

To check the above statement, the ABCD matrix of this model is,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -j\omega M \\ -\dfrac{j}{\omega M} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{68}$$

So, the input impedance of this network is,

$$Z_{in} = \frac{V_1}{I_1} = \frac{j\omega M I_2}{1/j\omega M\, V_2} = -(\omega M)^2 \frac{1}{-Z_L} = \frac{(\omega M)^2}{Z_L} \tag{69}$$

which proves that this network is in fact an impedance inverter with $K=\omega M$.

Using the same procedure with a different Π-network coupling element,

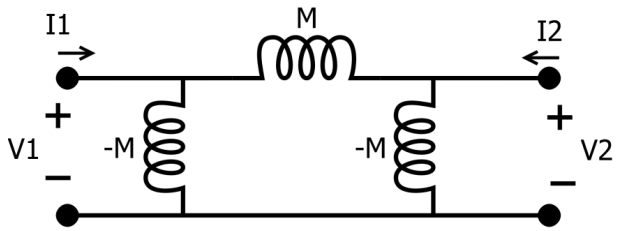


Fig. 133 – Admittance inverter inductor equivalent Π circuit.

The ABCD matrix is,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -j\omega M \\ -\dfrac{j}{\omega M} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{70}$$

The input impedance is then,

$$Y_{in} = \frac{I_1}{V_1} = \frac{1/j\omega M \, V_2}{j\omega M I_2} = \frac{1}{-(\omega M)^2} \frac{1}{-Y_L} = \frac{1/(\omega M)^2}{Y_L} \tag{71}$$

This network is an admittance inverter with $J = 1/(\omega M)$.

These two previous examples showed the equivalent circuits of both an impedance and an admittance inverter for magnetic coupling. When the electric coupling is used, it is also possible to define both inverter types, using equivalent circuits with capacitances. These four circuits are summarized in Table 15.

A.IV.3 Inverters' Effect in the Coupled Resonators

Each of the resonators depicted in Fig. 130 have, individually, the same resonating frequency, but when the inductors are coupled, the resonators' pair supports two different resonant modes. In the same circuit, considering that the left and right side resonators have a current I_1 and I_2 respectively, it is possible to describe the coupling equations of this network in the matrix form as,

$$\begin{bmatrix} j\left(\omega L - \frac{1}{\omega C}\right) & j\omega M \\ j\omega M & j\left(\omega L - \frac{1}{\omega C}\right) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = 0 \tag{72}$$

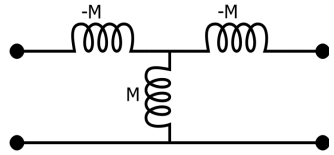
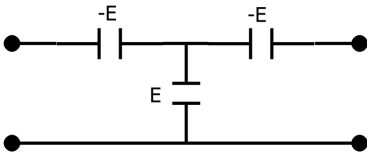
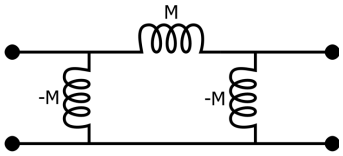
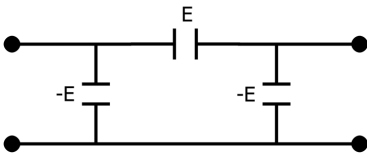
Besides the obvious solution ($I_1 = I_2 = 0$), these equations are true at the resonant frequencies of the system. Therefore, after some manipulation, those frequencies are,

$$f_L = \frac{1}{2\pi\sqrt{(L+M)C}} \tag{73}$$

and,

$$f_H = \frac{1}{2\pi\sqrt{(L-M)C}} \tag{74}$$

Table 15 – Lumped elements circuits for inverters implementation and corresponding types.

Circuit	Inverter type	Inverter value	Coupling
	Impedance	K = ωM	Magnetic Positive for M>0
	Impedance	K = 1/ωE	Electric Negative for E>0
	Admittance	J = 1/ωM	Magnetic Positive for M>0
	Admittance	J = ωE	Electric Negative for E>0

In order to verify visually the impact of the resonators' coupling, a simple test using the Agilent's ADS simulator was devised. The circuit presented in Fig. 134 was used in the tests.

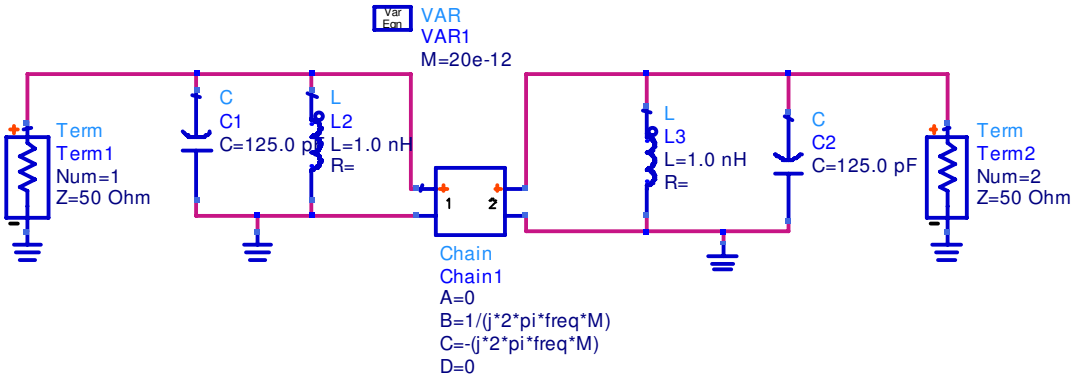


Fig. 134 – Simulation schematic of two parallel LC resonators coupled by a Π inductive admittance inverter.

It is composed by two equal LC parallel resonators, whose oscillating frequency is equal to 450 MHz, connected by an admittance inverter. The simulation results, namely the amplitude response versus frequency is depicted in Fig. 135.

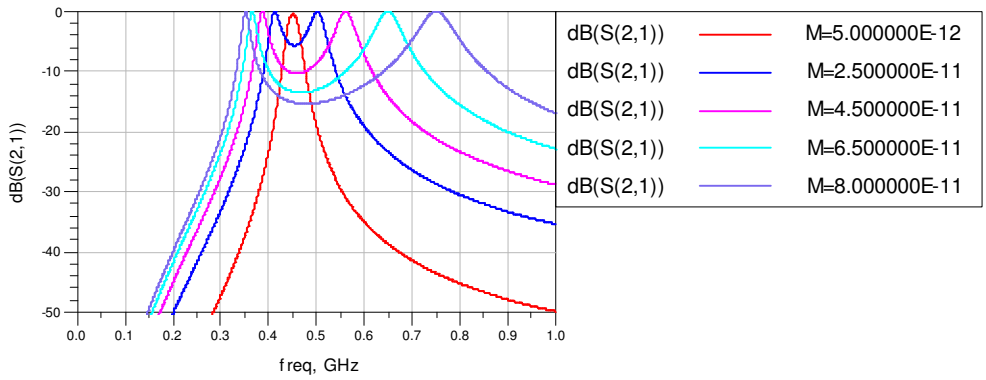


Fig. 135 – Coupled LC parallel resonators amplitude frequency response for several admittance coupling coefficient values.

As expected, when the coupling coefficient is very low, the oscillation frequency of both resonators is almost indistinguishable, but when the coupling increases, it is visible the two resonant frequencies.

As a consequence, in this case, it is more important to know the relation between the coupling coefficient, M, and the inductance value, L, which is called the the magnetic coupling coefficient and can be found by,

$$k = \frac{f_H^2 - f_L^2}{f_H^2 + f_L^2} = \frac{M}{L} \tag{75}$$

k is lower case, different from the impedance inverter, K.

When several resonators are coupled, the individual coupling coefficients is,

$$k_{ij} = \frac{f_{H_{ij}}^2 - f_{L_{ij}}^2}{f_{H_{ij}}^2 + f_{L_{ij}}^2} \tag{76}$$

These coupling coefficients are related with the impedance or admittance inverters by,

$$k_{ij} = \frac{K_{ij}}{\sqrt{\alpha_i \alpha_j}} = \frac{J_{ij}}{\sqrt{\beta_i \beta_j}} \tag{77}$$

where α and β are respectively, the reactance and susceptance slope parameters of the resonators (serial or parallel),

$$\alpha_i = \frac{\omega_0}{2} \frac{dX(\omega)}{d\omega}\bigg|_{\omega=\omega_0} \tag{78}$$

$$\beta_i = \frac{\omega_0}{2} \frac{dB(\omega)}{d\omega}\bigg|_{\omega=\omega_0} \tag{79}$$

In the majority of the situations it is not easy to derive these slope parameters, but these can be found directly from the lowpass prototype filter coefficients (valid for Butterworth and Chebyshev filters),

$$k_{ij} = \frac{BW_p}{f_0} \frac{1}{\sqrt{g_i g_j}} \tag{80}$$

if all the resonators are equal,

$$k_{ij} = \frac{K_{ij}}{\alpha} = \frac{J_{ij}}{\beta} \tag{81}$$

There are two special couplings, the input and output, which have a dramatic impact in the overall performance of the filter. They are often called Q_{ein} and Q_{eout} and are defined by,

$$Q_{ein} = \frac{\alpha_1 R_s}{K_{0,1}^2} \quad \vee \quad Q_{ein} = \frac{\beta_1 G_s}{J_{0,1}^2} \tag{82}$$

$$Q_{eout} = \frac{\alpha_n R_L}{K^2_{n,n+1}} \quad \vee \quad Q_{eout} = \frac{\beta_n G_L}{J^2_{n,n+1}} \tag{83}$$

These can also be calculated from the lowpass filter prototype coefficients,

$$Q_{ein} = \frac{f_0}{BW_p} g_{r0} g_{k1} \tag{84}$$

$$Q_{eout} = \frac{f_0}{BW_p} g_{kn} g_{r1} \tag{85}$$

A.V Filter Implementation

In cavity filter design, the coupling coefficients described in the previous Sub-Chapter are used to physically design the filters.

A.V.1 Option A

The filter has a slabline structure, as shown in Fig. 136, where the resonators cavities are open.

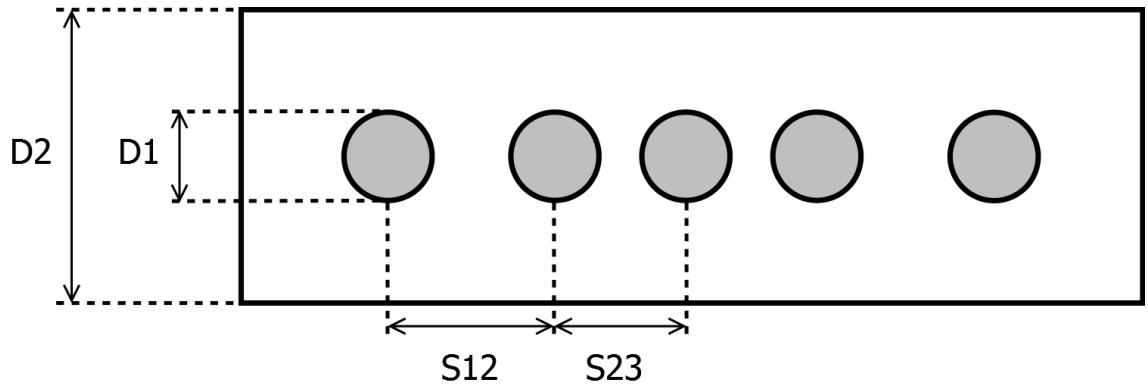


Fig. 136 – Slabline cavity filter top view.

In this case, the coupling is controlled by the resonators rod separation, which can be calculated using the cavity dimensions and the resonators coupling coefficients,

$$S_{ij} = \frac{D_2}{1.37}\left(0.91\frac{D1}{D2} + 0.1529 - \log\left(\frac{\left(\frac{2\theta}{\sin(2\theta)}\right)^{k_{ij}}}{f_0}\right)\right) \tag{86}$$

The dimensions are all in mm and θ is the electrical length of the fixed rod and equal to $2\pi l/\lambda_0$ (l is the physical length of the fixed rod)

A.V.2 Option B

The option A has the disadvantage of not being possible to easily adjust the couplings, if any tuning in bandwidth or central frequency is necessary. Hence, the structure presented in Fig. 137 is also very popular.

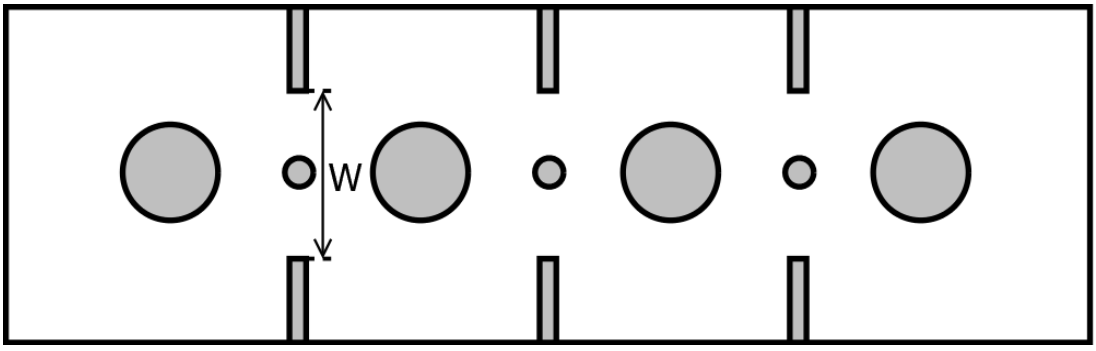


Fig. 137 – Top view of a cavity filter with equal cavity resonators and magnetically coupled.

The resonators cavity have all equal dimensions and the couplings are adjusted by the window (*W*) separation and by the tuning coupling rods (the small ones on top of *W*). These coupling rods have usually lower diameter than the cavity rods but its length can cover all the vertical dimension of the cavity.

The right aperture is found by Electro-Magnetic (EM) simulation, but as depicted in Fig. 138, the coupling increases when the aperture also increases.

Usually W is designed to be slightly smaller than the one required by design, to allow a certain margin for tuning. The tuning is performed by the coupling rods (more coupling when this small rod is deeper inside the cavity).

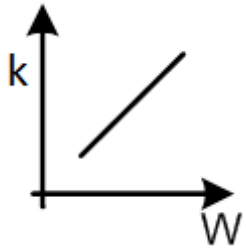


Fig. 138 – Internal coupling coefficient (K) evolution versus coupling window (W) width.

A.V.3 External Couplings

In both options, the external tap point must be found. It can be inductive or capacitive, but usually, the former is preferred, because it would not require another machined part and it is more mechanically stable.

The height of the tap point has a strong influence on the external coupling, as shown in Fig. 139.

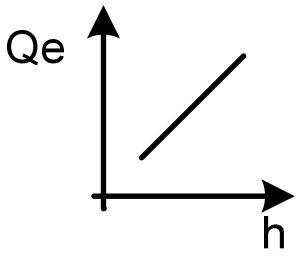


Fig. 139 – External coupling coefficient (Qe) evolution versus coupling position (h) height.

In this case, when the tap height is lower, the coupling is also lower. The exact point must be simulated and/or measured, but can be estimated by,

$$h = \frac{833}{f_0}\theta_h \tag{87}$$

in which, f_0 is the resonant frequency in MHz and θ_h is the height electrical length calculated by,

$$\theta_h = \sin^{-1}\left(\sqrt{\frac{Z_0 Q_e\left(\sin\left(2\theta\right)+2\theta\right)}{4Z_0}}\right) \tag{88}$$

Z0 is the resonator impedance, which can be calculated using (50).

A.V.4 Design Procedure

This method of designing cavity filters can be summarized by,

- Determine the filter requirements.
- Calculate the cavity resonator dimensions.
- Calculate the lowpass prototype elements (using the mentioned formulas or by tabulated data).
- Calculate the coupling coefficients.
- Determine the input and output coupling coefficients.
- Calculate the filter dimensions (spacing, apertures, tap height, etc).
- Simulate and design the filter in a electromagnetic simulator.
- Build and measure the filter.

The simulation step is of extreme importance to achieve a first time right design. However, some margin for tuning is mandatory to prevent unexpected problems.

A.VI Coupling Matrix

The previous method has some drawbacks,

- It is only applicable to Butterworth and Chebyshev approximations
- The filters are always symmetrical
- The resulting filter degree (number of resonators) is high when the rejection ratio increases

To overcome these issues, Cameron [59] proposed a new method, which allow the design of almost any filter type. This method is based on a coupling matrix representation

of the filter. It assumes that all the resonators are equal, only changing the coupling coefficients. For example, a 5 degree filter has the following coupling matrix (89), where,

1,2...6 -> resonators
s -> self coupling
m -> main line of couplings
x -> cross couplings
- -> zero coupling values
o -> the matrix is symmetric by the main diagonal

	1	2	3	4	5	6
1	s	m	-	-	-	-
2	o	s	m	-	x	-
3	o	o	s	m	-	-
4	o	o	o	s	m	-
5	o	o	o	o	s	m
6	o	o	o	o	o	s

(89)

This method increased the filter construction topology possibilities, where the resonators and the input/output connection placement is flexible. For this particular filter, described by the above coupling matrix can be implemented in the configuration presented in Fig. 140.

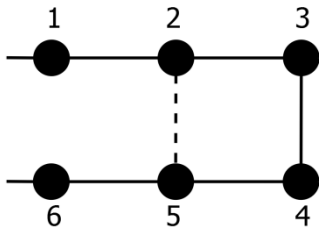


Fig. 140 – Resonator and coupling diagram of a 6 cavity filter.

The resonator number, the type of coupling (solid line for magnetic positive coupling and dashed line for negative capacitive coupling) and the input/output connection points are described.

As an example, Fig. 141, Fig. 142 and Fig. 143 depicts other possible representations and configurations for a 6, 10 and 16 cavity filter.

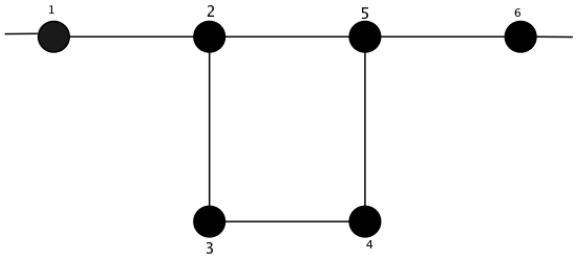


Fig. 141 – Resonator and coupling diagram of another option of a 6 cavity filter.

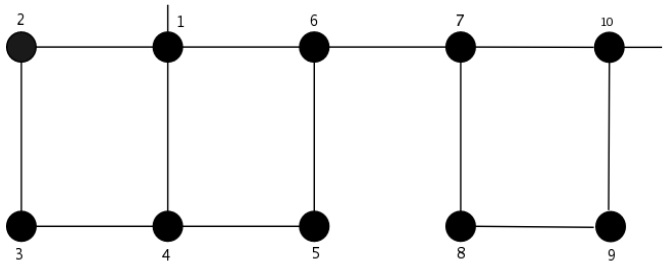


Fig. 142 – Resonator and coupling diagram of a 10 cavity filter.

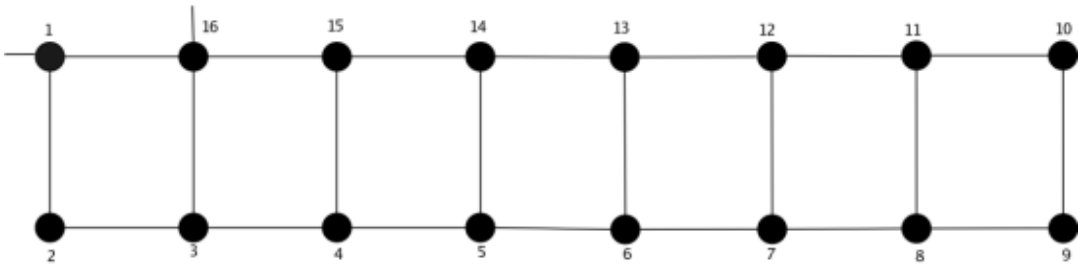


Fig. 143 – Resonator and coupling diagram of a 16 cavity filter.

With this method, virtually any type of filter can be realized, even 3D. Sometimes, *s* (self coupling) is not calculated, because it represents the resonant frequencies of each resonator (assumed to be equal). The analysis around the matrix calculation is not straightforward, but there are some software packages, which implement this method. Some of them are the Guided Wave Technology (GWT) and the Dedale HF.

A.VII Filter Tuning

After the cavity filter is constructed, it must be tuned. Although nowadays automatic mechanical tools are available to do it, usually this procedure is done by hand and it is a cumbersome and difficult task. To do it well, it requires large experience and patience to achieve good results. Some of the methods used to help this process are described in the next Sub-Chapters.

A.VII.1 Gross Tuning

Ness, [62] demonstrated a simple methodic procedure to tune cavity filters based in the S11 group delay, (90). It uses the center frequency and also the couplings tuning.

$$\tau_{gd}(\omega) = -\frac{d\angle S11}{d\omega} \tag{90}$$

The specific values of the group delay can be achieved using the standard coupling coefficients and external quality factors.

$$\begin{aligned} Q_{ein} &= \frac{\omega_0 - t_{d1}}{4} \\ k_{1,2} &= \frac{4}{\omega_0\sqrt{t_{d1}t_{d2}}} \\ k_{2,3} &= \frac{4}{\omega_0\sqrt{t_{d2}(t_{d3} - t_{d1})}} \\ k_{3,4} &= \frac{4}{\omega_0\sqrt{(t_{d3} - t_{d1})(t_{d4} - t_{d2})}} \\ &\ldots \end{aligned} \tag{91}$$

The basic steps of the method are:

- Short all resonators except the first one.
- Adjust the first resonator center frequency and external coupling to achieve a defined group delay t_{d1}.
- Tune the second resonator center frequency and coupling to the first resonator to achieve t_{d2}.
- Progress throughout the filter using this procedure.

- At the last resonator, try to achieve the correct frequency response.

Normally, this method does not provide excellent results.

A.VII.2 Fine Tuning

The previous procedure provides a reasonable approximation of the filter tuning, but to achieve maximum performance, other methods are required. One of them is presented by Lindner [65] and is based on the filter' S11 and S21 observation.

The method is the following,

1. In the network analyzer configure the measurements scale as follows,

- |S11| linear
- |S22| log

This configuration is the best to observe all the dips in S11, as depicted in Fig. 144, corresponding to each resonator. At the beginning, the filter must be tuned so that these dips are all present and observable. The previous Ness method can be used to achieve this state. The cross couplings must not be used at this point.

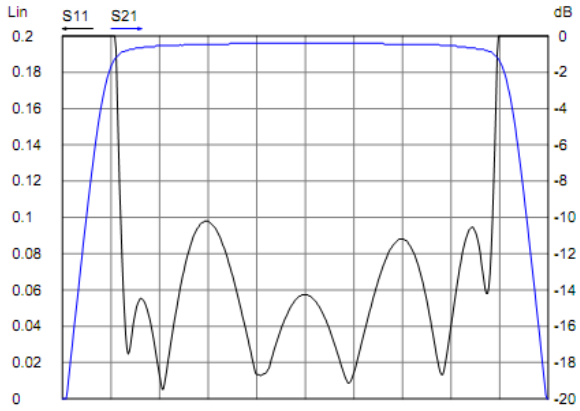


Fig. 144 – Bandpass filter transmission and reflection coefficients after first tuning step.

2. In this second step, tuning only the first half of the resonators, the dips must be lowered as possible, as shown in Fig. 145.

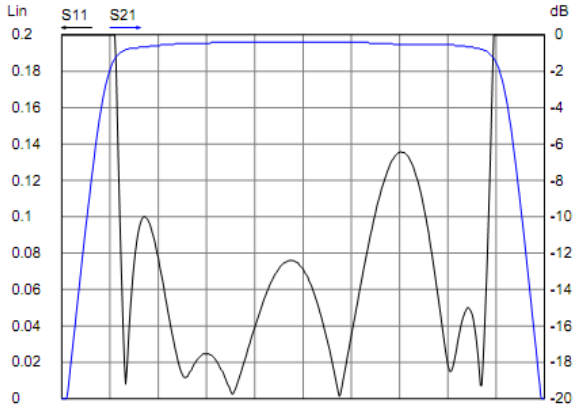


Fig. 145 – Bandpass filter transmission and reflection coefficients after second tuning step.

3. Using symmetric resonators, the filter response must be tuned for symmetry, as depicted in Fig. 146. However, the dips must not raise.

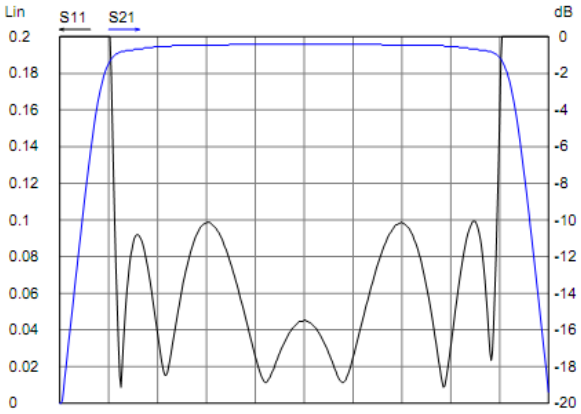


Fig. 146 – Bandpass filter transmission and reflection coefficients after third tuning step.

4. Using all resonators, simultaneously and with the same amount, tune to achieve the right center frequency.

5. Tune the filter BW, using all couplings, except the cross ones.

6. Tune the ripple, using all couplings (except the cross ones) and resonators.

7. Tune the cross couplings.

8. Repeat 2-6 if necessary, to adjust any detuning caused by the cross couplings, until a the desired response is achieved, Fig. 147.

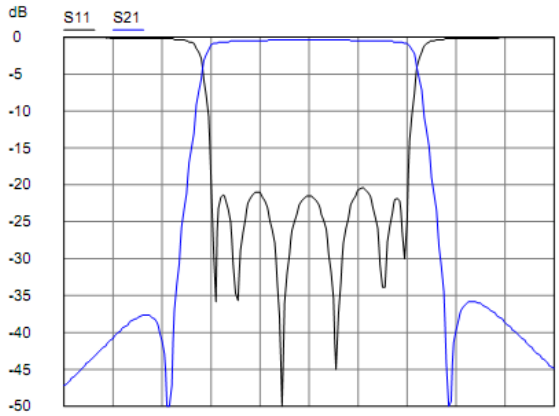


Fig. 147 – Bandpass filter transmission and reflection coefficients after final tuning step.

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References

[1] Q. Gu, *RF System Design of Transceivers for Wireless Communications*. Springer, 2005.

[2] P. Camana, "Integrated communications, navigation, identification avionics (ICNIA)-the next generation," *IEEE Aerospace and Electronic Systems Magazine*, vol. 3, no. 8, pp. 23–26, 1988.

[3] F. M. Torre, "Speakeasy-a new direction in tactical communications for the 21st century," in *Tactical Communications Conference, 1992. Vol. 1 Tactical Communications: Technology in Transition., Proceedings of the*, 1992, pp. 139–142.

[4] J. III Mitola, "Software radios: Survey, critical evaluation and future directions," *IEEE Aerospace and Electronic Systems Magazine*, vol. 8, no. 4, pp. 25–36, 1993.

[5] J. Mitola, "The software radio architecture," *IEEE Communications Magazine*, vol. 33, no. 5, pp. 26–38, 1995.

[6] C. Bergstrom, S. Chuprun, and D. Torrieri, "Adaptive spectrum exploitation using emerging software defined radios," in *Radio and Wireless Conference, 1999. RAWCON 99. 1999 IEEE*, 1999, pp. 113–116.

[7] D. W. Bennett, P. B. Kenington, and J. P. McGeehan, "The ACTS FIRST project and its approach to software radio design," in *Adaptable and Multistandard Mobile Radio Terminals (Ref. No. 1998/406), IEE Colloquium on*, 1998.

[8] T. Makelainen, T. Eriksson, J. Posti, and R. Suoranta, "Wideband radio prototyping environment," in *Radio and Wireless Conference, 1998. RAWCON 98. 1998 IEEE*, 1998, pp. 79–82.

[9] P. Eloranta and P. Seppinen, "Direct-digital RF modulator IC in 0.13 um CMOS for wide-band multi-radio applications," in *Proc. Digest of Technical Papers Solid-State Circuits Conference ISSCC. 2005 IEEE International*, 2005, pp. 532–615 Vol. 1.

[10] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A Multimode Transmitter in 0.13um CMOS Using Direct-Digital RF Modulator," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, 2007.

[11] P. Eloranta, P. Seppinen, and A. Parssinen, "Direct-digital RF-modulator: a multi-function architecture for a system-independent radio transmitter," *IEEE Communications Magazine*, vol. 46, no. 4, pp. 144–151, Apr. 2008.

[12] K. Parikh, T. Balsara, and E. Eliezer, "All Digital Quadrature Modulator Based Wideband Wireless Transmitters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, no. 99, pp. 1–1, 2003.

[13] V. K. Parikh, P. T. Balsara, and O. E. Eliezer, "A fully digital architecture for wideband wireless transmitters," in *Proc. IEEE Radio and Wireless Symposium*, 2008, pp. 147–150.

[14] R. B. Staszewski, K. Muhammad, and D. Leipold, "Digital RF Processor Techniques for Single-Chip Radios," in *Proc. IEEE Custom Integrated Circuits Conference 2006*, 2006, pp. 789–796.

[15] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and transmitter for mobile phones," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, 2005.

[16] R. B. Staszewski and P. T. Balsara, "All-Digital PLL With Ultra Fast Settling," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 2, pp. 181–185, 2007.

[17] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. Asbeck, "Linear high-efficiency microwave power amplifiers using bandpass delta-sigma modulators," *IEEE Microwave and Guided Wave Letters*, vol. 8, pp. 121–123, 1998.

[18] A. Jayaraman, P. Asbeck, K. Nary, S. Beccue, and K.-C. Wang, "Bandpass delta-sigma modulator with 800 MHz center frequency," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1997. Technical Digest 1997., 19th Annual*, 1997, pp. 95–98.

[19] S. M. Taleie, T. Copani, B. Bakkaloglu, and S. Kiaei, "A Linear Sigma Delta Digital IF to RF DAC Transmitter With Embedded Mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1059–1068, 2008.

[20] Y. Wang, "An improved Kahn transmitter architecture based on delta-sigma modulation," in *IEEE MTT-S International Microwave Symposium Digest*, 2003, vol. 2, pp. 1327–1330.

[21] Z. Richard; Regev Posner, "Transmission of Multiple Carrier Signals in a Nonlinear System," U.S. Patent 52492011993.

[22] M. Ozen, R. Jos, C. M. Andersson, M. Acar, and C. Fager, "High-Efficiency RF Pulsewidth Modulation of Class-E Power Amplifiers," *IEEE Journal of Microwave Theory and Techniques*, vol. 59, no. 11, pp. 2931–2942, 2011.

[23] C. Berland, I. Hibon, J. F. Bercher, M. Villegas, D. Belot, D. Pache, and V. Le Goascoz, "A transmitter architecture for nonconstant envelope modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 1, pp. 13–17, Jan. 2006.

[24] J. Jeong and Y. E. Wang, "A Polar Delta-Sigma Modulation (PDSM) Scheme for High Efficiency Wireless Transmitters," in *Proc. IEEE/MTT-S International Microwave Symposium*, 2007, pp. 73–76.

[25] M. Nielsen and T. Larsen, "A Transmitter Architecture Based on Delta–Sigma Modulation and Switch-Mode Power Amplification," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, pp. 735–739, 2007.

[26] J.-H. Chen, H.-S. Yang, and Y.-J. E. Chen, "A Multi-Level Pulse Modulated Polar Transmitter Using Digital Pulse-Width Modulation," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 5, pp. 295–297, 2010.

[27] J. Choi, J. Yim, J. Yang, J. Kim, J. Cha, D. Kang, D. Kim, and B. Kim, "A Delta Sigma Digitized Polar RF Transmitter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2679–2690, 2007.

[28] B. Francois, E. Kaymaksut, and P. Reynaert, "Burst mode operation as an efficiency enhancement technique for RF power amplifiers," in *Proc. XXXth URSI General Assembly and Scientific Symp*, 2011, pp. 1–4.

[29] P. Nuyts, B. Francois, W. Dehaene, and P. Reynaert, "A CMOS Burst-Mode Transmitter With Watt-Level RF PA and Flexible Fully Digital Front-End," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 10, pp. 613–617, 2012.

[30] D. R. Parveg, P. Singerl, A. Wiesbauer, H. Mashad Nemati, and C. Fager, "A broadband, efficient, overdriven class-J RF power amplifier for burst mode operation," in *Proc. European Microwave Conf. (EuMC)*, 2010, pp. 1666–1669.

[31] H. Yang, H. Shih, J. Chen, and Y. E. Chen, "A Pulse Modulated Polar Transmitter for CDMA Handsets," in *Proc. IEEE/MTT-S International Microwave Symposium*, 2010, pp. 808–811.

[32] Y.-S. Jeon, H.-S. Yang, and S. Nam, "A novel high-efficiency linear transmitter using injection-locked pulsed oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 4, pp. 214–216, 2005.

[33] C. Schuberth, P. Singerl, M. Gadringer, H. Arthaber, A. Wiesbauer, and G. Magerl, "Highly Efficient Switched-Mode Transmitter Using a Current Mode Class-D RF Amplifier," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 20, pp. 446–457, 2010.

[34] B. Francois, P. Reynaert, A. Wiesbauer, and P. Singerl, "Analysis of burst-mode RF PA with direct filter connection," in *Proc. European Microwave Conf. (EuMC)*, 2010, pp. 974–977.

[35] A. Dupuy and Y. E. Wang, "High efficiency power transmitter based on envelope delta-sigma modulation (EDSM)," in *Vehicular Technology Conference, 2004. VTC2004-Fall. 2004 IEEE 60th*, 2004, vol. 3, pp. 2092–2095.

[36] J. Jeong and Y. E. Wang, "Pulsed Load Modulation (PLM) Technique for Efficient Power Amplification," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 10, pp. 1011–1015, 2008.

[37] S. Liao and Y. E. Wang, "High Efficiency WCDMA Power Amplifier With Pulsed Load Modulation (PLM)," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 99, pp. 1–8, 2010.

[38] B. D. Bedford, "Electric amplifying circuits," U.S. Patent 18741591932.

[39] M. Iwamoto, A. Jayaraman, G. Hanington, P. F. Chen, A. Bellora, W. Thornton, L. E. Larson, and P. M. Asbeck, "Bandpass delta-sigma class-S amplifier," *Electronics Letters*, vol. 36, pp. 1010–1012, 2000.

[40] J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital generation of RF signals for wireless communications with band-pass delta-sigma modulation," in *IEEE MTT-S International Microwave Symposium Digest*, 2001, vol. 3, pp. 2127–2130.

[41] J. J. Hinrichs Rode and P. Asbeck, "Transmitter architecture using digital generation of RF signals," in *Radio and Wireless Conference, 2003. RAWCON '03. Proceedings*, 2003, pp. 245–248.

[42] J. Dooley, T. Podsiadlik, A. Canniff, and R. Farrell, "Reconfigurable Class S power amplifiers at RF and microwave frequencies," in *Proc. Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits INMMIC*, 2008, pp. 43–46.

[43] J. Ketola, J. Sommarek, J. Vankka, and K. Halonen, "Transmitter utilising bandpass delta-sigma modulator and switching mode power amplifier," in *Proceedings of the 2004 International Symposium on Circuits and Systems*, 2004, vol. 1, pp. 633–636.

[44] N. V. Silva, A. S. R. Oliveira, U. Gustavsson, and N. B. Carvalho, "A Novel All-Digital Multichannel Multimode RF Transmitter Using Delta-Sigma Modulation," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 3, pp. 156–158, 2012.

[45] J. Keyzer, R. Uang, Y. Sugiyama, M. Iwamoto, I. Galton, and P. M. Asbeck, "Generation of RF pulsewidth modulated microwave signals using delta-sigma modulation," in *IEEE MTT-S International Microwave Symposium Digest*, 2002, vol. 1, pp. 397–400.

[46] F. M. Ghannouchi, S. Hatami, P. Aflaki, M. Helaoui, and R. Negra, "Accurate Power Efficiency Estimation of GHz Wireless Delta-Sigma Transmitters for Different Classes of Switching Mode Power Amplifiers," *IEEE Journal of Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2812–2819, 2010.
[47] F. H. Raab, "Effects of circuit variations on the class E tuned power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 2, pp. 239–247, 1978.
[48] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters - Theory, Design and Simulation*. IEEE Press, 1997.
[49] U. Gustavsson, T. Eriksson, H. Mashad Nemati, P. and Singerl, and C. Fager, "An RF Carrier Bursting System Using Partial Quantization Noise Cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 99, no. 99, p. 1, 2011.
[50] F. H. R. Charles W. Bostian Herbert L. Krauss, *Solid State Radio Engineering*. John Wiley and Sons, 1980.
[51] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley and Sons, 2004.
[52] AnalogDevices, *The data conversion handbook*. Newnes, 2005.
[53] P. M. Aziz, H. V. Sorensen, and J. vn der Spiegel, "An overview of sigma-delta converters," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 61–84, 1996.
[54] E. M. T. J. Leo Young George L. Matthaei, *Microwave Filters, impedance-matching networks, and coupling structures*. Artech House, 1980.
[55] T. Johnson and S. Stapleton, "Available load power in a RF class D amplifier with a sigma-delta modulator driver," in *Proc. IEEE Radio and Wireless Conference*, 2004, pp. 439–442.
[56] S. Kim and Y. E. Wang, "Theory of Switched RF Resonators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 12, pp. 2521–2528, 2006.
[57] A. I. Zverev, *Handbook of Filter Synthesis*. John Wiley and Sons, 1967.
[58] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814–826, Mar. 2002.
[59] R. J. Cameron, "Advanced coupling matrix synthesis techniques for microwave filters," *IEEE Journal of Microwave Theory and Techniques*, vol. 51, no. 1, pp. 1–10, 2003.
[60] S. Hori, K. Kunihiro, K. Takahashi, and M. Fukaishi, "A 0.7-3GHz envelope ΔΣ modulator using phase modulated carrier clock for multi-mode/band switching amplifiers," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, 2011, pp. 1–4.
[61] A. Wentzel, S. Chevtchenko, P. Kurpas, and W. Heinrich, "A Dual-Band Voltage-Mode Class-D PA for 0.8/1.8 GHz Applications," in *Microwave Symposium Digest (MTT), 2013 IEEE MTT-S International*, 2013.
[62] J. B. Ness, "A unified approach to the design, measurement, and tuning of coupled-resonator filters," *IEEE Journal of Microwave Theory and Techniques*, vol. 46, no. 4, pp. 343–351, 1998.
[63] R. W. Rhea, *HF Filter Design and Computer Simulation*. Noble, 1994.
[64] M. Steer, *Microwave and Rf Design: A Systems Approach*. SciTech Publishing, Inc., 2010.
[65] A. Lindner and E. Biebl, "A Manual Tuning Method for Coupled Cavity Filters," in *Proc. 36th European Microwave Conf*, 2006, pp. 1340–1342.