Chapter 1

New Processes and Technologies to Reduce the Low-Frequency Noise of Digital and Analog Circuits

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Additional information is available at the end of the chapter

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Abstract

The chapter is intended to provide the reader with means to reduce low-frequency noise in Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). It is demonstrated that low-resistivity source and drain electrodes can greatly lower the low-frequency noise level by suppressing their contribution to the total noise. Furthermore, new plasma processes having the advantages to work at low electron temperature can achieve a further reduction, thanks to the fabrication of a better gate oxide and to a reduction of damages generally induced by conventional plasma processes. Reducing the impact of the traps on the carrier flowing inside the channel by burying the channel can also achieve a reduction of the noise level, but unfortunately at the cost of a degradation of the electrical performances. Finally, the noise analysis of the low-frequency noise in accumulation-mode MOSFETs showed that these newly developed devices have a lower noise level than conventional structures, which, in addition to their superiority in term of electrical performances, establishes them as a serious platform for the next Complementary Metal-Oxide-Semiconductor Field-Effect-Transistor (CMOS) technology.

Keywords: low-frequency noise, radical oxidation, silicide, series resistances, accumulation-mode, MOSFET, buried-channel, fabrication process

1. Introduction

Since the dawn of electronics more than 50 years ago, manufacturers have been providing customers with faster and smaller chips by fabricating increasingly better devices and improving processes. The main strategy adopted has been to shrink the gate size of the MOSFETs to improve chip performances, especially speed. Since the signal-to-noise ratio was large enough, the noise

was not an issue and its reduction dragged very little effort among the scientific community. After a steady working frequency doubling every year, the recent downscaling of the dimension has led to high stress and increased variability and, in turn, stagnation of performances of chips. There is no doubt that the increased noise is to blame for that standstill, even if other problems such as the doping concentration could be implicated as well. Nevertheless, the distinction between noise and signal has become critical and the noise issue must be tackled. A suppressed noise level should pave the way to once again lower biases leading to less heat, better reliability, and better performances.

Noise is a fluctuation of a quantity that shifts back and forth with uncertainty. In electronics, it is generally noted as a fluctuation of the voltage or current around its mean value and is ascribed to stochastic events which find their origin at a microscopic level trough the discrete nature of the transport or the Brownian nature of the carrier. There are several types of noises such as thermal noise, shot noise, generation-recombination noise, inter-band noise, and low-frequency noise. They are generally classified upon their origin. Among these, the thermal noise and low-frequency noise are of paramount importance in MOSFETs, with the latter one being of most concern since its origin is still in debate and that its evaluation for a given technology is made extremely difficult. Even if the low-frequency noise has been a limiting factor of performances for analog circuits for several years, it has recently become as well an issue for digital ones. Indeed, even though its limitation applies in the low range of frequency, it is up-converted into phase noise leading to time domain instabilities and therefore problems in the high-frequency range. Its reduction is therefore mandatory not only for analog but also for digital circuits.

In Section 1, the theory of the low-frequency noise in MOSFETs is briefly reviewed. While Sections 2 and 3 present new technologies to suppress it by the means of, respectively, silicide and damage free processes, Sections 4 and 5 introduce improved MOSFETs. Thus, the results regarding buried-channel and accumulation-mode MOSFETs are reported, respectively, in Sections 4 and 5.

2. Low-frequency noise in MOSFETs

The MOSFET is a complex device composed of purely resistive parts surrounding the channel whose resistance is controlled by the bias applied at the gate electrode. It is therefore natural that the noise generated inside each region is propagating up to the source and the drain electrodes. However, the noise stemming from the channel is generally the most dominant one, even though the one coming from the surrounding areas can play an important role and can even take over as the main noise source [1]. **Figure 1(a)** shows a schematic of a MOSFET structure while **Figure 1(b)** represents its equivalent noise circuit. The source access resistance, the drain access resistance, and the channel are the three main regions the noise is coming from and the total measured noise S_{Id} at a given frequency can be written [2].

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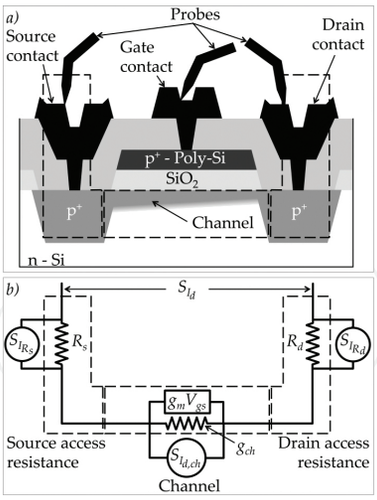

Figure 1. Representation of (a) MOSFET and (b) its equivalent circuit noise.

$$S_{I_d}(f) = \frac{S_{I_{d,ch}}(f)}{\left[1 + g_m R_s + g_{ch}\left(R_s + R_d\right)\right]^2} + \frac{g_m^2 R_s^2 S_{I_{R_s}}(f) + g_{ch}^2\left[R_s^2 S_{I_{R_s}}(f) + R_d^2 S_{I_{R_d}}(f)\right]}{\left[1 + g_m R_s + g_{ch}\left(R_s + R_d\right)\right]^2} \quad (1)$$

where $S_{Id,ch}$, $S_{IRs,}$ and S_{IRd} are the noises generated, respectively, inside the channel, the source R_s and drain R_d access resistances. G_m and g_{ch} are, respectively, the transconductance and conductance of the channel. The left-hand side term is the contribution coming from the channel while the right-hand side one is the contribution coming from the access resistances.

It is worth noticing that S_{Id} can become equal to $S_{Id,ch}$ meaning that the measured noise will be the noise of the channel, whereas even if the series resistances are the main noise source, it is their contribution that will be measured and not their pure noise. The noise in a resistive material such as the access resistances of a MOSFET is either thermal noise or 1/*f* noise at low frequencies [3]. This 1/*f* noise is known to originate from the fluctuations of the fundamental mobility and it follows the Hooge's empirical formulae [3]:

$$\frac{S_I(f)}{I^2} = \frac{\alpha_H}{fN}, \quad (2)$$

which represents the normalized noise of the current *I* while *N* is the number of carriers. α_H is the Hooge parameter suggested to be constant and to reflect the quality of the crystal. After several decades of controversies between the Hooge theory and the Mc. Whorter one [4], the latter explaining the noise in terms of fluctuation of the carrier number, Mikoshiba [5] devel-

oped a new theory able to gather all data into a single model to explain the noise stemming from the channel.

His theory has been confirmed afterward by several researchers and is now well accepted among the scientific community. Within this theory, the noise is given by [6]

$$\frac{S_{\mathrm{I_d}}(f)}{I_d^2} = \frac{g_m^2}{I_d^2}\left(1 \pm \alpha\mu_{\mathrm{eff}} C_{\mathrm{ox}} \frac{I_d}{g_m}\right)^2 S_{V_{fb}}(f), \tag{3}$$

where C_{ox} is the gate oxide capacitance, g_m is the transconductance, and μ_{eff} is the effective mobility of the carriers flowing inside the channel. This theory is known as the insulator and induced mobility fluctuations, and is ascribing the origin of the noise to the traps located inside the gate insulator near the interface. The constant dynamic capture and release of carriers from and to traps generate interfacial insulator charge variation and, in turn, fluctuation of the insulator charge. These fluctuations are equivalently generating flat band variations. These fluctuations are summarized on the left-hand side term in Eq. (3) and are proportional to the flat band voltage fluctuations $S_{\mathrm{Vfb,}}$ expressed as [6]

$$S_{V_{fb}}(f) = \frac{\lambda k_{\mathrm{B}} T q^2 N_t}{WLC_{\mathrm{ox}}^2 f}, \tag{4}$$

with k_{B} being the Boltzmann constant, q the electron charge, T the temperature, and λ the tunnel attenuation length of the traps in the insulator equal to 0.1 nm for SiO_2. N_t is the interface trap density. In addition to the variation of the insulator charge, the capture and release mechanism is locally affecting the surface potential at the interface, resulting in a Coulomb interaction between the locally deformed potential surface and the carriers flowing inside the channel. The localized scattering rate will vary and will induce fluctuations of the mobility. These fluctuations are ascribed to the right-hand side term in Eq. (3) and are related to the fluctuations of the insulator charge through the Coulomb parameter α, which measures the strength between both quantities. With nowadays miniaturization of the gate of the MOSFETs, two kinds of noises are at stake, although they are both explained in the frame of the previous theory. Indeed, it is obvious that in the case of very small gate size involving a very limited number of carriers, the removal or introduction of a single free carrier scared within the total number of free carriers involved in the conduction will have a tremendous impact on the current, making it jump between two or several levels like randomly disposed crenels. This type of noise is called random telegraph noise and is commonly an issue for sensors, especially optical ones [7]. However, when the number of traps is more significant and for a specific distribution of their energy within the bandgap, the resulting noise is commonly called 1/*f* or even Flicker noise and it follows a distribution, proportional to the inverse of the frequency when plotted as a function of the frequency [1]. This noise is an issue for analog circuits, and even for some digital ones, and will even impact at high frequency due to its conversion into

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phase noise. Finally, the noise in MOSFETs can be summarized as depicted in **Figure 2**. The noise measured at the electrode of a MOSFET is the sum of three terms: the fluctuation of the insulator charge, induced fluctuation of the mobility, and the contribution coming from the access resistances. It is worth mentioning that there is a fourth term, the cross-correlation term between the fluctuation of the insulator charge and the induced mobility one even though it does not have a physical origin.

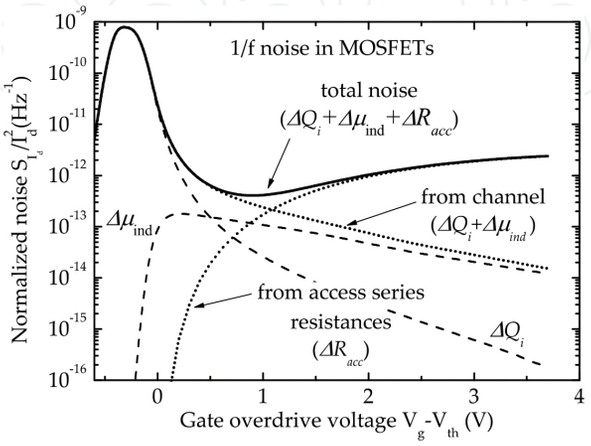

Figure 2. Normalized noise in a MOSFET. The several contributions of each noise sources have been reported with the non-full lines.

3. Source and drain contacts

When it comes to low-frequency noise, the contribution stemming from the source and drain access series resistances is generally overlooked. This negligence can have tremendous impact on the noise analysis especially at high gate voltage where their contribution will mostly take over as the dominant noise.

As a matter of fact, this is not the noise generated inside the source and drain access series resistances, which is at stake but their contribution. Rather than reducing the noise sources, reducing their contribution is more efficient and easier. Indeed, the reduction of the resistance of the source and drain access contacts does not only mean a better drivability and a better transconductance but can guarantee a reduction of the propagation of the noise generated by the noise sources inside the contacts and, in turn, a reduction of the contribution of the source and drain contact noise to the total measured noise [8]. The performance improvement of CMOS has become of paramount importance with scaled dimension. Much effort is being made to increase the carrier mobility by several means such as strained technology [9], different silicon orientation [10], or even different semiconductor [11]. The reduction of the source and drain electrode series resistances is another means to improve the drivability and silicide has already been used for such purposes. Nitride alloy silicide is widely used to lower the Schottky barrier height to either n^+ or p^+ silicon down with contact resistance as low as 2×10^{-9} Ω cm^2 in

the best case [12]. A new structure [13] and new processes [14] have been developed in order to further lower down the series resistances. Instead of using the same silicide for both p^- and n-MOSFETs, erbium has been selected to perfectly fit the requirement of n-MOSFETs and palladium for the p-MOSFETs. Additionally, tungsten metal stack above the thin silicide layer was introduced to reduce the sheet resistance and protect erbium from being oxidized. In order to confirm the above statement, two kinds of MOSFETs have been fabricated following the very same process flow, except during the source and drain contact fabrication stage. The source and drain contacts of the reference transistors have been fabricated with aluminum (Al), while erbium silicide associated with tungsten ($ErSi_2$/W) has been used for the second set of transistors. The respective structures have been represented in **Figure 3(a)** and **(b)**. While both wafers followed the same process flow until the contact lithography step, the $ErSi_x$/W wafer followed an advanced process entirely developed at New Industry Creation Hatchery Center (NICHe). In this advanced process, the wafer has been loaded in an N_2 sealed cleaning chamber after a total room temperature five-step cleaning, which has been followed by the dipping of the cleaned wafer in O_3 dissolved ultra pure water in order to form a chemical oxide at the silicon surface. The removal of the chemical oxide has been carried out by diluted HF solution and the wafer has been then transferred in clustered sputter equipment, still in N_2 ambient, where the formation of a thin film of erbium followed by the deposition of a tungsten capping layer has been done by Radio Frequency (RF) sputtering.

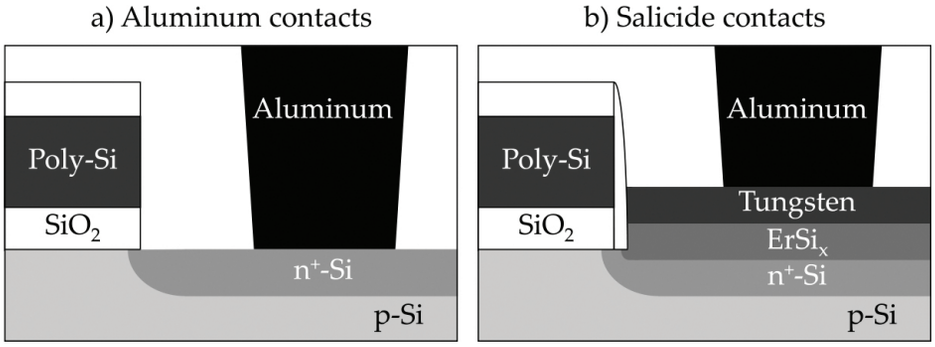

Figure 3. Schematic of the structure of (a) reference contacts fabricated with aluminum (Al) and (b) salicide contacts fabricated with erbium silicide ($ErSi_x$) and tungsten (W) layer. Copyright 2011 The Japan Society of Applied Physics [8].

The wafer has been then loaded in lamp annealing chamber to finally form $ErSi_x$. The wafer has been then brought back to the conventional process flow to finally form aluminum contacts. Electric characterization has been carried out and the main results are summarized in **Figure 4(a)** and **(b)**. As expected, the drivability has been improved by a factor of 2 on account of silicide contacts [8]. Furthermore, the maximum of the transconductance also increased and confirms the interest of low-resistivity source and drain contacts to enhance performances of electronic circuits. Noise measurements have been performed in the linear regime and for f = 10 Hz. The result is presented in **Figure 5**. When compared with the noise level of the reference transistor, the noise level of the transistor featuring $ErSi_x$/W contacts is greatly reduced for positive gate overdrive voltages while it remains equivalent for lower values. The same noise

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level below 0 V is explained by the fact that within this range of measurement the channel is exclusively contributing to the total noise and by the fact that both devices have indeed almost the same channel, since they followed the same process flow with regard to the fabrication of the gate stack. The noise modeling has been carried out and is reported with the lines in **Figure 5**. The modeling reveals that from 0 V the noise from the reference device moves away from the noise stemming from the channel. The contribution of the series resistances to the total noise is increasing and is ultimately taking over as the main contribution. However, the noise of the device featuring $ErSi_2$/W contacts is following the curve depicting the noise stemming from the channel and starts to slightly move away at high voltages. The impact of the series resistances on the noise is barely visible. The use of low-resistivity contacts allows a drastic reduction in the contribution of the series resistances to the total noise and let the channel be the sole source of noise over the entire measurement range [8]. About 10 times reduction of the access resistance has led to 100 times reduction of the noise level.

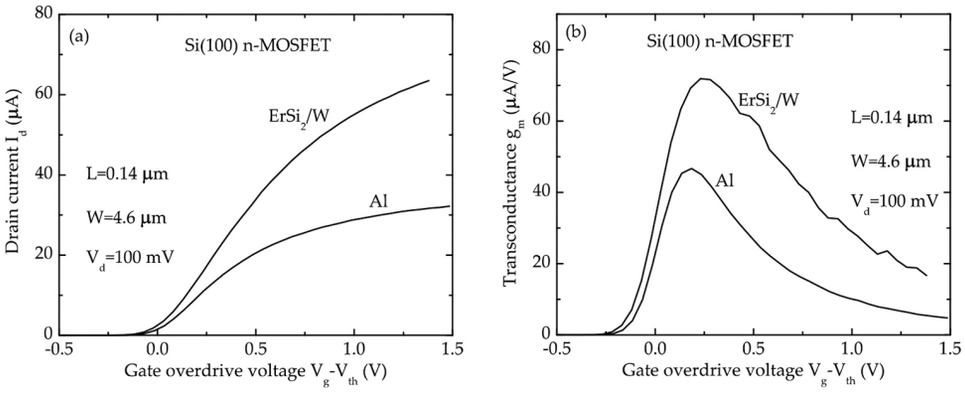

Figure 4. (a) Drain current and (b) transconductance versus gate overdrive voltage for n-MOSFETs featuring Al and $ErSi_2$/W contacts. Copyright 2011 The Japan Society of Applied Physics [8].

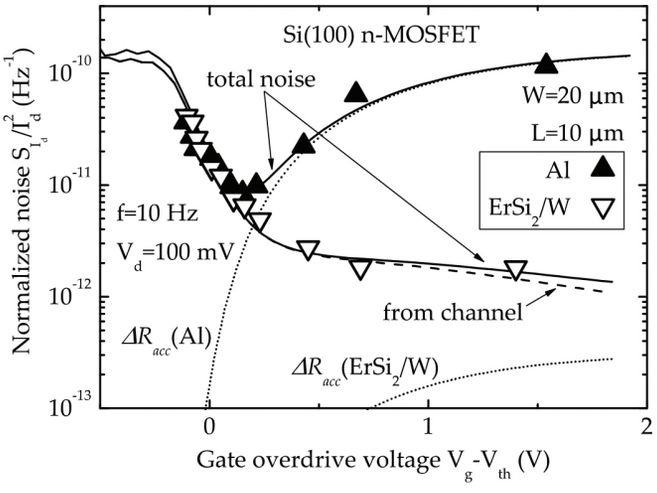

Figure 5. Normalized noise of n-MOSFETs with contacts fabricated with either aluminum(Al) or erbium silicide/tungsten($ErSi_2$/W). (W) layer. Copyright 2011 The Japan Society of Applied Physics [8].

4. Radical oxidation

The gate stack, especially, the gate insulator, is the most critical part of the MOSFET, mainly because of the defects that can appear during the fabrication and its tremendous impact on the device performance [15]. It is absolutely true these days that the need of always-faster devices and smaller chips also promote the appearance of undesirable effects such as increase of variability and random telegraph noise. Thermal oxidation has been the way, since the establishment of the MOSFET, to fabricate the gate insulator and while the generated SiO_2 was at the beginning of poor quality, leading to high S parameters, the process has greatly evolved since and the growth of quality oxide can be achieved now [15]. Unfortunately, the dimension of nowadays MOSFETs has reached a threshold where S parameter and V_{th} variability are a major issue, as well as, noise level prevision [16].

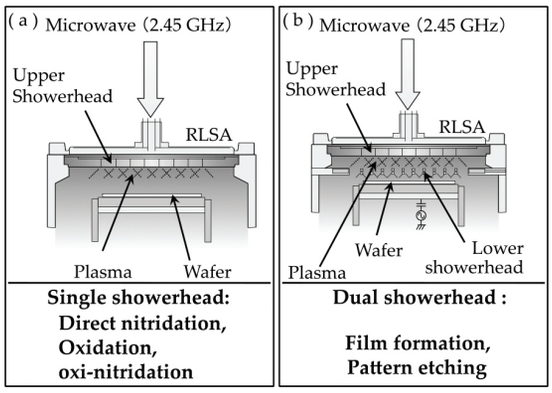

Figure 6. Diagrams of (a) single shower plate and (b) double shower plate equipment based radicals formed by the low electron temperature microwave high-density plasma.

Thermal oxidation, from its intrinsic chemical reaction, cannot be optimized anymore and will always promote the formation of damage (either inside the gate stack or cap layers) and will partly invalidate the flattening process and, in turn, deteriorate the surface roughness of the wafer. Thus, new oxidation processes have been developed to avoid these issues. They are all based on radical oxidation rather than chemical reaction to form SiO_2 [17]. The specificity of the damage-free very low electron temperature microwave exited high-density plasma is, as represented in **Figure 6**, that it can be employed for oxidation at low temperature, chemical vapor deposition, or even reactive ion etching. Very high quality gate insulator and reduced damages generally occurring during the etching and the fabrication of interconnect can be achieved thanks to this advanced process as shown in **Figure 7** [15, 18, 19]. Contrary to the thermal oxidation, the radical oxidation has an oxidation rate that is almost regardless of the orientation of the silicon crystal on which the oxide is grown [20]. Additionally, the radical oxidation does not only help reduce the interface trap density but also help preserve and even improve the flatness of the Si/SiO_2 interface. Two sets of p-MOSFETs have been fabricated in our clean room. They followed almost the same process flow; however, they differed in such a way that the first set featuring a radically grown oxide has been processed exclusively with

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advanced plasma equipment, while the second set has been processed using conventional processes, among which the thermal oxidation process.

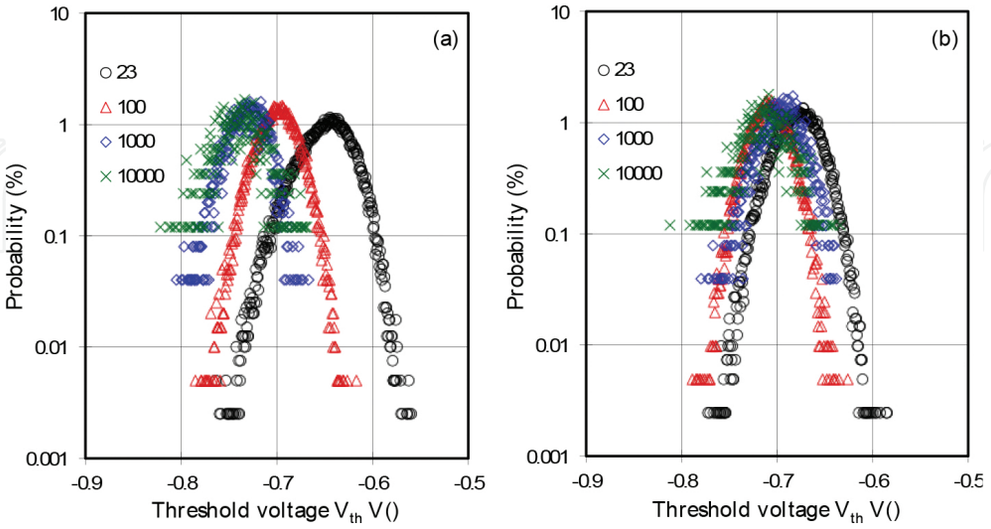

Figure 7. V_{th} distributions of p-MOSFETs fabricated by applying (a) conventional plasma processes and (b) radial line slot antenna plasma processes plotted for antenna ratio of 23, 100, 1000, and 10,000.

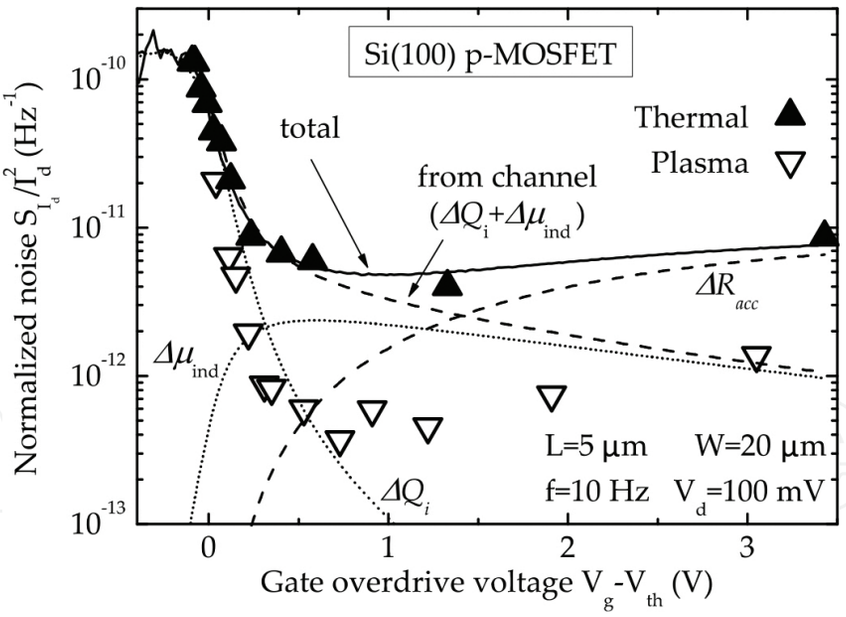

Figure 8. Normalized noise of p-MOSFETs with a gate oxide fabricated by either thermal or plasma oxidation as a function of the gate overdrive voltage. The modeling, reported with the lines, refers exclusively to the transistor with a gate oxide thermally grown. Copyright 2011 The Japan Society of Applied Physics [8].

Noise measurements have been performed in the linear and saturated region and for different gate sizes. The noise analysis has been carried out at 10 Hz. Results are presented in **Figure 8**, and they clearly indicate that the p-MOSFET with a gate oxide fabricated by radical oxidation

has a lower noise level than when the thermal oxidation process is used used, with a maximal reduction of over a decade. As expected, the noise stemming from series resistances and the noise from the channel are both contributing to the total noise, with the latter one being ascribed to the insulator charge and induced mobility fluctuations. In order to understand the origin of the noise reduction, the modeling of the p-MOSFETs, featuring a gate oxide, fabricated by radical oxidation has been carried out. The result is reported in **Figure 9** and it revealed an unexpected behavior, i.e., no induced mobility fluctuations. The contribution of the series resistances added to the sole insulator charge fluctuations has been enough to model the total noise. Even though the trapping/release mechanism at the origin of the 1/*f* noise induces fluctuation of the mobility, these fluctuations are, in the present case, too small to be visible when compared to the other fluctuations. The interface trap density has been extracted for both sets of devices and revealed a three-time reduction in favor of the transistors fabricated using plasma processes with $N_d = 2 \times 10^{16}$ cm^{-3} eV^{-1}, testifying the high integrity of the oxide when fabricated by radical oxidation.

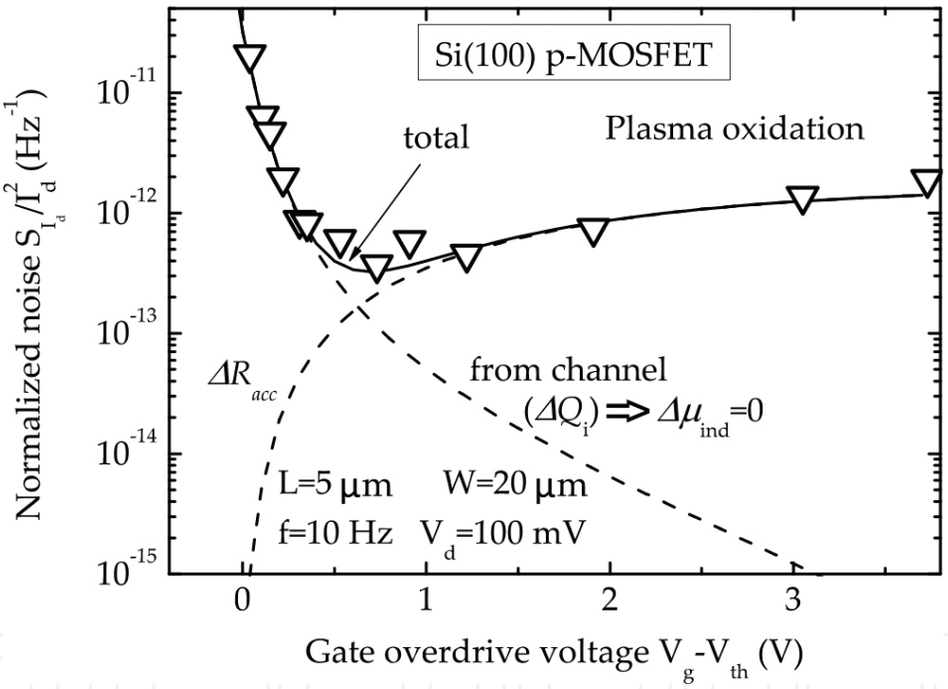

Figure 9. Normalized noise of p-MOSFETs with a gate oxide fabricated by plasma oxidation as a function of the gate overdrive voltage. Copyright 2011 The Japan Society of Applied Physics [8].

5. Buried-channel MOSFETs

5.1. Structure of buried-channel MOSFET

The low-frequency noise, such as 1/*f* noise and random telegraph noise, is basically caused by the defects at the gate insulator and silicon interface in MOSFETs. To reduce the low-frequency

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noise, the number of defects or the influence of the defects has to be reduced. Here, the channel of the buried-channel MOSFETs is separated from the gate insulator/Si interface, and then the carriers in the channel are hard to be influenced by the defects at the interface. Usually, the buried-channel MOSFETs are characterized as high mobility but weak short channel Field-Effect-Transistor (FET) [21–23] because the carriers flow through the bulk. In this case, the separated channel location of buried-channel MOSFETs is very important for reducing the low-frequency noise. **Figure 10** shows the schematic illustration of the buried-channel n-MOSFET. The buried layer was formed by the ion implantation at the V_{th} adjustment process [24, 25]. **Figure 11** shows the band diagram of the conventional surface channel (a) and the buried-channel MOSFETs (b), respectively [25]. The buried layer depth was set as 170 nm from the SiO_2/Si interface, and the channel was appeared at around 30 nm from the SiO_2/Si interface at the bias conditions of back bias (V_{BS}) =1.5 V and drain current (I_{DS}) =100 nA for a gate length (L) of 0.22 μm and a gate width (W) of 0.28 μm MOSFETs.

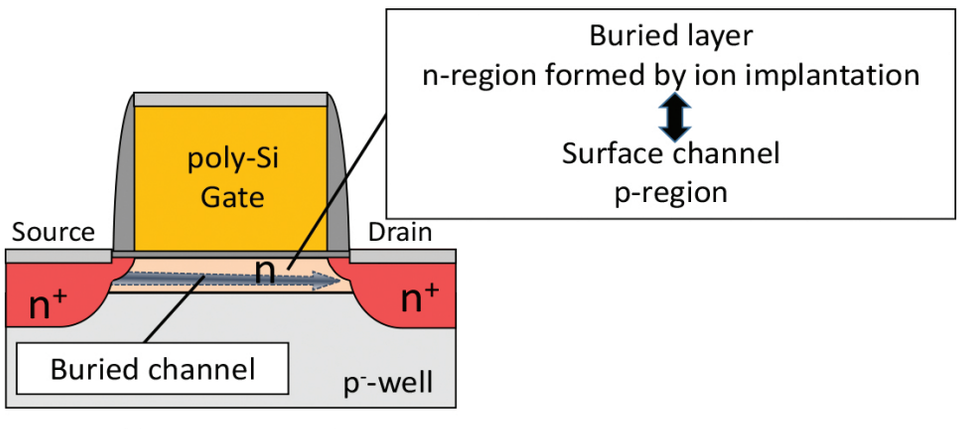

Figure 10. Schematic illustration of the buried-channel MOSFET.

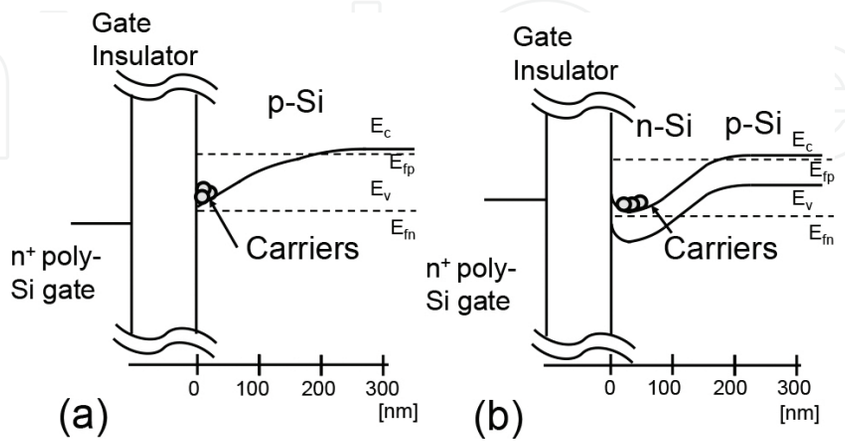

Figure 11. Diagrams of surface channel (a) and buried-channel MOSFETs. The bias condition was set at V_{BS} = 1.5 V and I_{DS} = 100 nA.

5.2. Low-frequency noise characteristics

Figure 12 shows the 1/*f* noise characteristics for the surface channel and buried-channel MOSFETs. Five samples were measured for each MOSFET. The size (*W*/*L*) of MOSFETs was 10 μm/5 μm and bias conditions were set as V_{DS} = 1.5 V, V_{BS} = 0 V, I_{DS} = 1, 10, and 100 μA. S_{Id} increases as the drain current increasing for both MOSFETs. The noise power S_{Id} of the surface channel MOSFETs is proportional to 1/*f*. In contrast, S_{Id} of the buried-channel MOSFETs for the low I_d cases is not proportional to 1/*f*, because the noise level was smaller than the floor noise of the measurement system. For the same drain current I_d, the noise power of the buried-channel MOSFETs are less than that of the surface channel MOSFETs, especially their differences are observed for the low drain current cases. In this experiment, the gate voltage controlled the drain current. When the gate voltage increases, the distance between the channel and the interface decreases, and then it influences the defects. This indicates that the noise reduction of buried channel is very effective for the low gate voltage conditions.

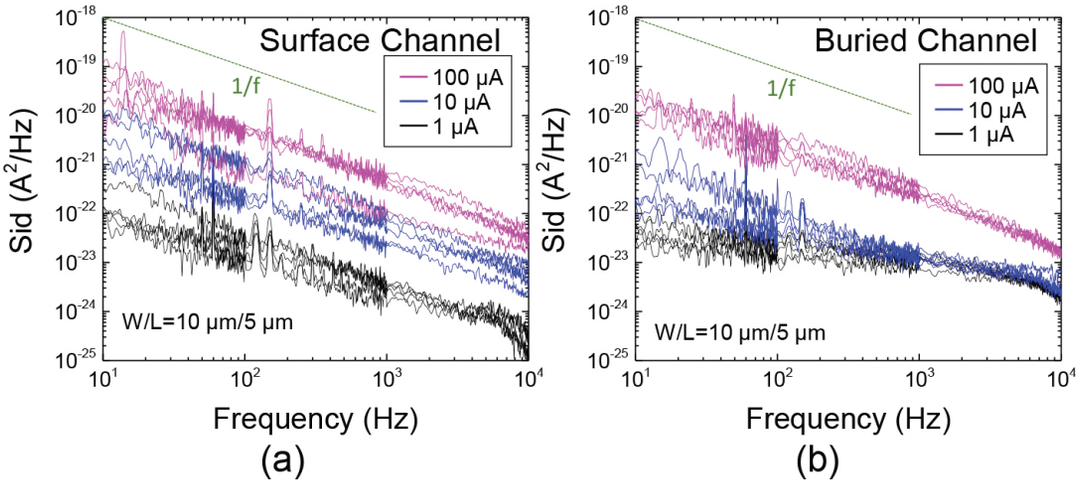

Figure 12. 1/*f* noise characteristics of (a) surface channel and (b) buried-channel MOSFETs.

5.3. V_{th} variability

In the previous section, it is described that the noise can be reduced by introducing the buried-channel MOSFETs because the channel is separated from the SiO_2/Si interface. However, this means the gate capacitance becomes lower compared to the surface channel MOSFETs. Then, the V_{th} control becomes difficult compared with the surface channel. **Figure 13** shows distributions of (a) V_{th} and (b) the channel charge (Q_{ch}) with 65536 MOSFETs for the buried- and surface channel MOSFETs [24]. These distributions are measured by the array test circuit, which can measure the V_{th} variation and the random telegraph signal for many MOSFETs (>1 million MOSFETs) during very short time (<1 s) [26–29]. The horizontal axis of both the graphs shows the difference values between the average values of all MOSFETs (65536 MOSFETs). The V_{th} variability of the buried-channel MOSFET is larger than that the surface channel MOSFETs as shown in **Figure 13(a)**. It is considered that the gate capacitance of buried channel is smaller than that of the surface channel. Then, the horizontal axis is converted from V_{th} to

Q_{ch} by using the gate-channel capacitance. Almost the same distributions are observed, and then the variability is caused by the small capacitance between the gate and the channel. Moreover, it is noticed that the noise increases by the excess capacitance decrease with the other transistor characteristics degradation, such as short channel effect and subthreshold swing degradation [22, 30].

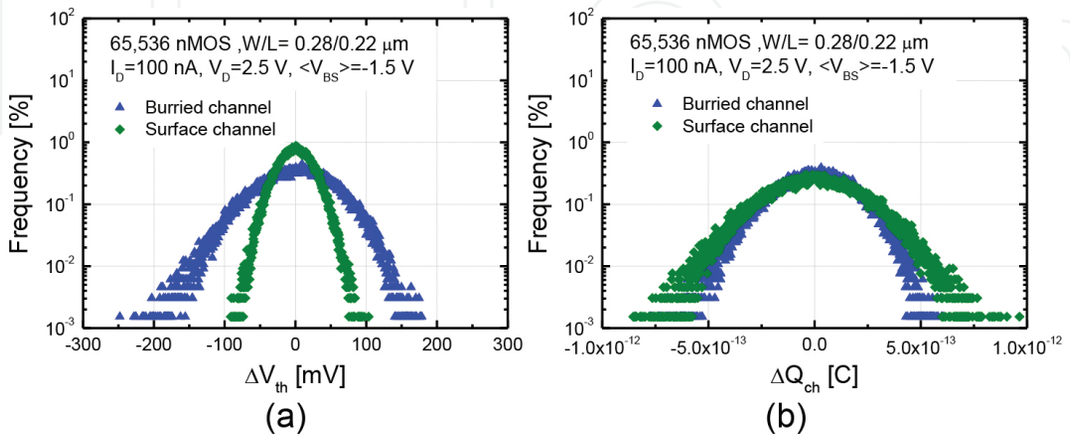

Figure 13. Distributions of (a) V_{th} and (b) Q_{ch} with 65536 MOSFETs for the buried- and surface channel MOSFETs.

6. Accumulation-mode MOSFETs

The separation between the interface and the channel is effective in reducing the noise in buried-channel MOSFETs; however, the controllability of V_{th} is worse than conventional MOSFETs because the gate capacitance is reduced. Then the introduction of Silicon-on-Insulator (SOI) wafer and a new structure can solve this issue [31, 32]. The so-called accumulation-mode MOSFET has been developed keeping this in mind. As depicted in **Figure 14**, the accumulation-mode MOSFETs differ from MOSFETs in such a way that the type of the SOI layer is the same as that of the contact. Additionally, the type of polysilicon must also be adjusted as required. Although the working of the conventional inversion-mode MOSFETs is based on the generation of an inversion layer made of the minority carrier, the accumulation-mode one is making use of an accumulation layer composed of majority carrier. Actually, the accumulation-mode MOSFET without bias is at first on the off-state since the SOI layer is completely depleted. When a bias is applied at the gate, a thin conductive layer of majority carrier is first generated at the back interface between the Buried Oxide (BOX) and the SOI. Then accumulation-mode MOSFETs become on the on-state. A current at the back interface flows from the source to the drain. A further increase in the bias makes this layer disappear and makes a short portion of the originally depleted SOI layer become neutral. A bulk current is generated on the BOX side. This current continues to increase with the expansion of the neutral region (due to the shrinking of the depleted region) inside the SOI until the bias applied at the gate reaches the flat-band voltage.

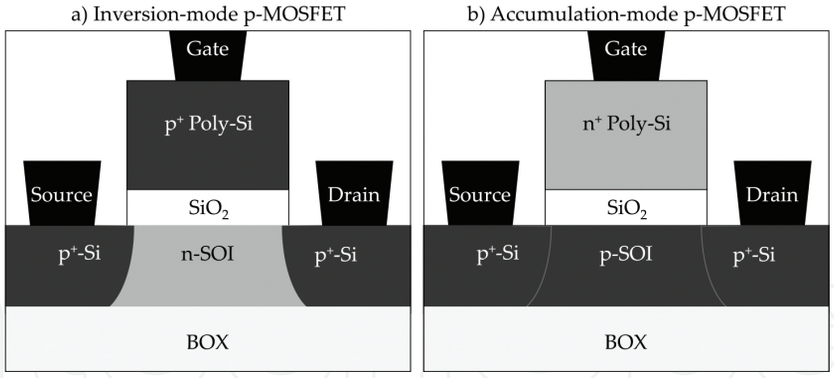

Figure 14. Schematic representation of (a) inversion-mode and (b) accumulation-mode p-MOSFETs.

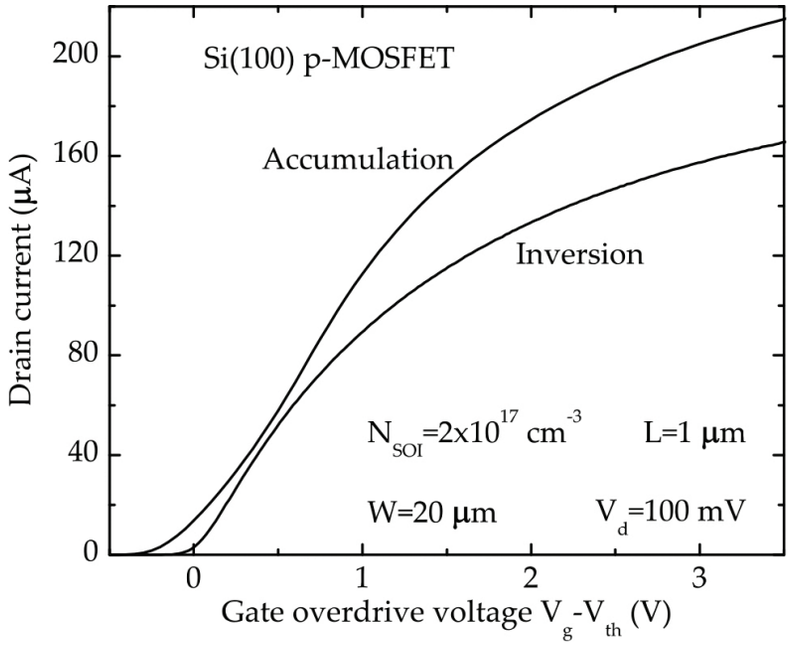

Figure 15. Drivability of accumulation- and inversion-mode p-MOSFETs.

The current generated inside the accumulation layer then adds to the bulk current. Therefore, in addition to, among other things, having an improved reliability [33] and being immune to radiation effects [34], they also have a better drivability than inversion-mode MOSFETs since the total current is the sum of those generated inside the SOI and the accumulation layer [35]. When the bulk current has reached its maximum, corresponding to the SOI completely neutral, the majority carrier accumulates at the front interface between the gate insulator and the SOI. Accumulation-mode fully depleted SOI MOSFETs have been fabricated on Si(100) surface to investigate the noise characteristics. The SOI layer impurity has been adjusted by ion implantation to 2×10^{17} cm^{-3}. The thickness of the SOI layer has been reduced down to 50 nm. In order to avoid the increase of noise due to the defects at the front interface and the impact of the surface roughness of the interface, the radical oxidation [17] added to the five-step-cleaning

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process [20] has been repeated four times until reaching a flattened interface with a roughness R_a of 0.08 nm. A 7-nm gate oxide has been formed by radical oxidation using a low electron temperature microwave high-density plasma process at 400°C. As expected and as shown in **Figure 15**, the accumulation-mode MOSFETs feature a better drivability than those of the inversion-mode MOSFETs. The better drivability does not only owe to two distinctive currents but also from the higher carrier mobility thanks to a lower transversal electric field at the front interface [35].

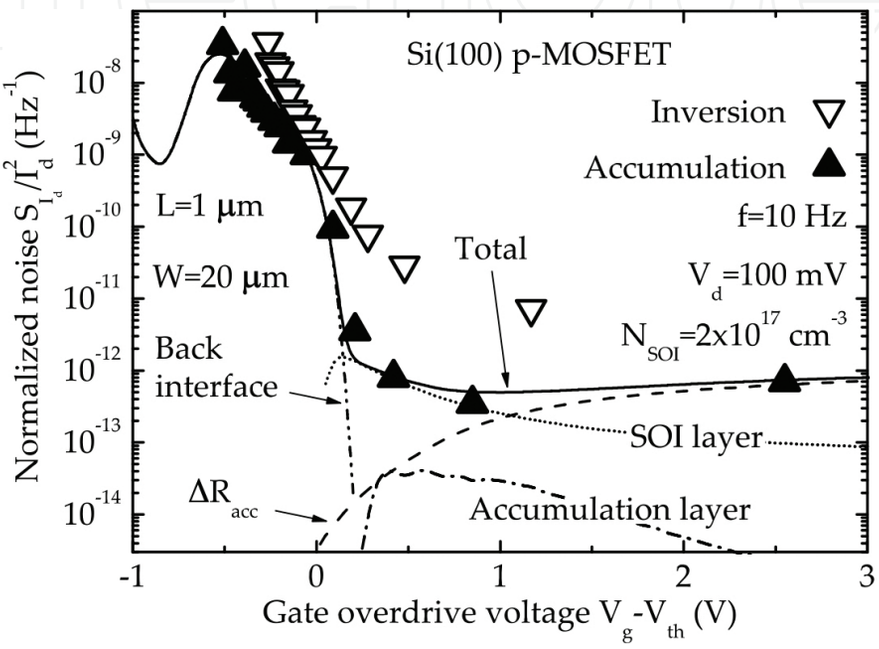

Figure 16. Normalized noise of accumulation- and inversion-mode p-MOSFETs. Lines refer to the modeling of the noise of the sole accumulation-mode device and represent the noise generated by each region.

The noise of the inversion- and accumulation-mode MOSFETs has been reported in **Figure 16**. Even though their noise level is similar at low gate overdrive voltage, the superiority of the accumulation-mode MOSFET over the inversion mode one becomes clear for voltage over 0 V. A gap of more than 1 decade is achieved at the best. While the noise of the inversion-mode MOSFET can be ascribed to the interface traps [6] and series resistances at high bias [3], the origin of the noise for the accumulation-mode one must be investigated with care. Indeed, as discussed earlier, three conduction mechanisms generate the current and are therefore generating their own noise. The modeling of each noise and finally the total modeled noise have been reported with lines in **Figure 16**. The noise stemming from the front and back interfaces is originating from the interface traps [5], like for the inversion-mode MOSFET while the noise from the SOI layer and access resistances is explained in terms of fundamental fluctuations of the mobility of the Hooge model [3]. Contrary to the inversion-mode MOSFET, the front interface does not contribute to the total noise. The lower noise can be attributed to a change in the origin of the noise stemming from the channel, with the SOI region becoming the main contributor to the noise with regard to the channel and a significant shift toward the

high gate voltage to turn the accumulation layer on. It is worth mentioning that the advantage of the accumulation-mode MOSFET is effective for high doping concentration; otherwise, the accumulation layer will act like an inversion one [36] since it implies no contribution from either the back interface or the SOI layer to the total current.

7. Conclusion

In this chapter, we reviewed several ways to suppress the low-frequency noise of MOSFETs and, in turn, the noise of analog and digital circuits. One of the most underrated approaches is to optimize the contacts and interconnects by the means of low-resistive materials, so that their contribution to the total noise can be drastically reduced. It has also been shown that a great deal must be paid to the fabrication processes. Indeed, the use of processes demonstrating very low damage generation at all the stages of fabrication can lead to MOSFETs with better performances and especially reduced noise level due to a reduction of induced defects located at the gate stack and its surroundings. Additionally, these low-defect processes based on the damage-free, low-temperature, high-density plasma technology achieved a further reduction by means of the disappearance of one component of the low-frequency noise, the induced mobility fluctuations one, bringing the noise of MOSFETs to the sole fluctuations of the insulator charges. Focusing on a different electronic structure can also achieve low-noise MOSFETs. For example, minimizing the interaction carrier-traps by moving away the channel – so that fewer traps are activated and less variations of the insulator charge are generated – can achieve a reduced noise. Unfortunately, this reduction is obtained at the cost of a degradation of the electrical performances. So, the most promising structure to suppress noise is in the form of the accumulation-mode MOSFETs. Indeed, in addition to offer reduced low-frequency noise when compared to conventional MOSFETs, their electrical performances are greatly improved. These devices obviously feature various assets, which should consequently pave the road for a new era of very low noise and high-performance MOSFETs and bring microelectronic manufacturers back to the realization of highly performances and high-speed analog and digital circuits.

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