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## **Amorphous Silicon Photonics**

Ryohei Takei

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#### Abstract

This chapter introduces our research on amorphous silicon photonics. By exploring our high-quality silicon thin-film technology, we have demonstrated hydrogenated amorphous silicon (a-Si:H) waveguides with ultra-low-loss, vertical interlayer transition (VIT) devices for cross coupling between vertically stacked optical circuits. These device technologies are promising for three-dimensional photonic integrated circuits integrated in microelectronics chips. A record low loss of 0.6 dB cm<sup>-1</sup> was achieved for a submicron-scale single-mode waveguide, and the VIT devices allow low-loss, broadband, and polarization-insensitive operation.

**Keywords:** hydrogenated amorphous silicon, silicon photonics, 3D integration, photonic integrated circuit, backend integration

## 1. Introduction

Amorphous silicon (a-Si) is a well-known and industrially proven non-crystalline material. It is widely used in commercial applications; for example, thin-film transistors in liquid crystal displays, thin-film solar cells, and microbolometers for thermal cameras [1]. Recently, the mature silicon (Si) thin-film technology has advanced toward a new research field: Si photonics. Si photonics is an ultrahigh-density integration technology for optical devices using submicronscale optical waveguides with a core composed of Si, which is mainly attractive for data communication applications. Typically, optical Si-integrated devices are fabricated on siliconon-insulator (SOI) wafers consisting of crystalline Si (c-Si) and buried oxide (BOX). The large difference in refractive index (n) between Si ( $n = \sim 3.5$ ) and silica (SiO<sub>2</sub>) ( $n = \sim 1.4$ ) enables



© 2016 The Author(s). Licensee InTech. This chapter is distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/3.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited. miniaturization of such optical devices. Meanwhile, Si thin films have received attention because of their favorable deposition and optical properties. Through deposition of Si, three-dimensional (3D) photonic integrated circuits (PICs) can be constructed by vertical stacking of multiple a-Si waveguide layers clad with an amorphous insulating material such as SiO<sub>2</sub>. Such vertical stacking would be inherently infeasible on a c-Si platform because it is virtually impossible to deposit c-Si on an amorphous substrate such as thermal oxide. Furthermore, a-Si has higher optical nonlinearity and lower nonlinear absorption than the corresponding values of c-Si. Thus, a-Si is an attractive material for use in optical nonlinear devices such as parametric amplifiers, all-optical signal processing devices, and all-optical modulators [2–9].

A disadvantage of a-Si is that it has an optical absorption loss in the infrared wavelength range assigned for optical telecommunication. In a-Si, Si atoms form a random network and have dangling bonds that cause absorption loss of infrared light. This disadvantage has been overcome by passivation of the dangling bonds by hydrogen. Two decades ago, Cocorullo et al. [10] reported the first example of hydrogenated a-Si (a-Si:H) waveguides. They deposited a-Si:H films through plasma decomposition of silane (SiH<sub>4</sub>). In 2005, Harke and colleagues developed a single-mode a-Si:H waveguide on a thermal oxide with a propagation loss of 2.0 dB cm<sup>-1</sup> at a wavelength of 1.55 µm for the ridge waveguide with a height of 1.3 µm and a width of 1.1 µm [11]. Researchers at Ghent university demonstrated an a-Si:H nanophotonic waveguide using a complementary metal-oxide semiconductor (CMOS)-compatible process [12]. A propagation loss of 3.5 dB cm<sup>-1</sup> was achieved for the wire waveguide with a width of 480 nm and height of 220 nm. The optimized KrF lithography and Si dry-etching process decreased the roughness at the waveguide sidewalls, resulting in a low-loss wire waveguide. Also, Zhu et al. [13] from the Institute of Microelectronics reported a-Si:H wire waveguides fabricated using a CMOS-compatible process. The propagation loss of the waveguides was 3.2 dB cm<sup>-1</sup>, and they were 200 nm high and 500 nm wide. Chemical mechanical polishing (CMP) was used to smooth the a-Si:H top surface. Sun et al. [14] from the Massachusetts Institute of Technology achieved a propagation loss of 2.7 dB cm<sup>-1</sup> for waveguides with a width of 700 nm and height of 100 nm with a thin interlayer cladding made of silicon nitride (SiN). SiN has *n* =  $\sim 2.0$  which is between those of Si and SiO<sub>2</sub>. Thus, the SiN interlayer mitigates the difference of *n* between Si and SiO<sub>2</sub>, resulting in a decreased propagation loss. Kang et al. [15] from Tokyo Institute of Technology reported vertically stacked a-Si:H waveguides with two waveguide layers on an SOI waveguide layer by repeated deposition of a-Si:H and SiO<sub>2</sub>.

We have focused on a-Si:H 3D PIC technology, which is promising to replace electrical interconnect in CMOS chips with optical interconnects. Electrical interconnects are currently one of the bottlenecks for the performance improvement of CMOS chips because the aggregate bandwidth of intra-chip data transmission is physically limited by power consumption and the frequency of the clock signal. In contrast, optical interconnects could provide higher speed and larger bandwidth data transmission than electrical ones because the frequency of light as a data carrier is much higher than that of electricity and wavelength division multiplexing is available. Furthermore, a-Si:H photonics has two additional advantages: potential feasibility of 3D PICs and process compatibility with CMOS backend processes. Regarding the former, 3D PIC could increase the bandwidth by stacking of multiple optical layers. Meanwhile,

integration of optical interconnection with CMOS chips in a back-end-of-line configuration is possible because the deposition temperature of a-Si:H is less than 400°C. In this chapter, we summarize our research achievements. In Section 2, we report a-Si:H waveguides with ultralow loss together with high-quality a-Si:H technology, which is fundamental for high-performance PICs. In Section 3, the concept of vertical interlayer transition (VIT) devices is described. The optimal design, fabrication, and measurement results of our VIT devices are presented.

## 2. Low-loss a-Si:H waveguide

### 2.1. High-quality a-Si:H

Because a-Si has an absorption loss in the telecommunication wavelength range, development of low-loss a-Si:H is important. High-quality a-Si:H films can be obtained by plasma-enhanced chemical vapor deposition (PECVD) through plasma decomposition of a source gas mixture of SiH<sub>4</sub> and hydrogen (H<sub>2</sub>). The deposition conditions strongly influence the characteristics of the deposited film. Deposition temperature is the most important factor affecting film quality. On the growth surface during the deposition, the main precursor (SiH<sub>3</sub> radicals) reaches the surface and then diffuses on it to find energetically stable sites. As the deposition temperature increases, the diffusion of the precursor is enhanced. As a result, the defect density is lowered. However, desorption of the hydrogen covering the surface occurs above 250°C, which increases the defect density. Thus, the defect density is determined by the balance of these two reactions: diffusion and desorption. The lowest defect density is achieved in a-Si:H films deposited at 250°C [16].

We measured the sub-gap absorption coefficient of a 1-µm-thick a-Si:H film deposited at 250°C [17]. A highly sensitive measurement technique is required to do this because a well-passivated a-Si:H film has low absorption. The absorption of the film was measured using the constant photocurrent method (CPM) calibrated with the transmittance and reflection (T&R) spectra. CPM is a highly sensitive but relative measurement, whereas T&R spectra are absolute measurements but have low sensitivity. In the high-absorption region, the absorption coefficient of a material can be determined from T&R spectra. In contrast, CPM can measure the relative absorption over the whole wavelength region including those with high and low absorption. The absorption coefficient in the low-absorption region can be determined by calibrating the CPM spectra with the T&R measurements in the high-absorption region. The measured absorption coefficient in **Figure 1** was  $10^{-2}$  cm<sup>-1</sup> at a 1550 nm, corresponding to a loss of 0.04 dB cm<sup>-1</sup>. The defect density of the film was  $4.2 \times 10^{15}$  cm<sup>-3</sup>, which was evaluated from the integrated defect absorption using a conversion factor of  $1.9 \times 10^{16}$  cm<sup>-2</sup> eV<sup>-1</sup> [18]. **Table 1** compares the material losses of a-Si:H reported to date, showing that the loss of our a-Si:H film is the lowest obtained so far.

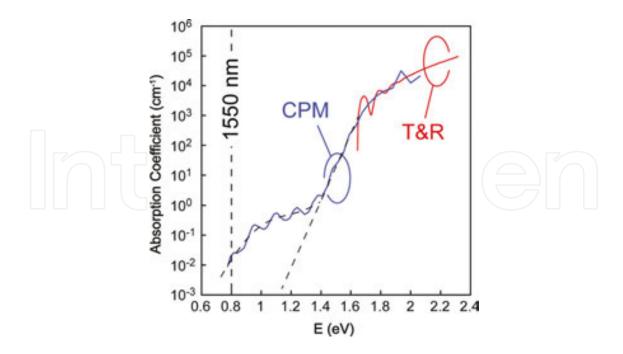


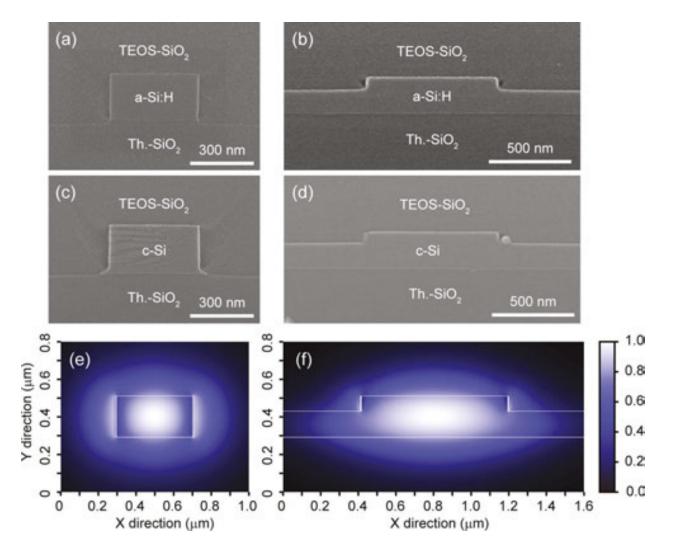
Figure 1. Sub-gap absorption spectrum of a 1-µm-thick a-Si:H film measured using the CPM and T&R approach.

Reference	Deposition temp.	Material	Method
	(°C)	loss (dB/cm)	
[19]	Not stated	<1	Estimation from waveguide loss dependence on width
[20]	Not stated	0.5	Prism coupling method
[12]	300	0.7	Estimation from waveguide loss
[21]	220	1.1	Photothermal deflection spectroscopy
Our work [17]	250	0.04	CPM calibrated with T&R spectra

Table 1. Comparison of material losses in a-Si:H films.

#### 2.2. Waveguide fabrication

Nanophotonic waveguides with a core made of our low-absorption a-Si:H films were fabricated and their propagation losses were evaluated [17]. Two types of waveguides were tested: one composed of 420-nm-wide wires and another with 780-nm-wide ridges. For reference, c-Si waveguides with the same geometry were also tested. The waveguides were fabricated as follows. First, 220-nm-thick a-Si:H films were deposited by PECVD using a gas mixture of SiH<sub>4</sub> and H<sub>2</sub> at 250°C on a Si wafer with a 2-µm-thick thermal oxide layer. The waveguides were formed using a standard microfabrication technology including i-line lithography. The a-Si:H film used for the wires was dry etched through inductively coupled plasma (ICP)reactive ion etching (RIE) using a gas mixture of sulfur hexafluoride (SF<sub>6</sub>) and octafluorocyclobutane (C<sub>4</sub>F<sub>8</sub>). In contrast, the a-Si:H film used for the ridges was etched by carbon tetrafluoride-based capacitively coupled plasma-RIE. After removing the remaining photoresist and by using a wafer-cleaning process, the 1.5-µm-thick upper cladding of the waveguides was deposited by plasma decomposition of a gas mixture of tetraethyl orthosilicate and oxygen at 350°C. The reference c-Si waveguides were fabricated following a similar process on an SOI wafer composed of a 220-nm-thick top Si layer and underlying 2-µm-thick BOX layer. Finally, the wafers were cleaved to form smooth edge facets for light coupling from/to optical fibers. **Figure 2** depicts cross-sectional scanning electron microscope (SEM) images of the fabricated waveguides. The main electrical field profiles of the quasi-transverse electric (q-TE) mode are also shown. The field profiles were numerically calculated by the finite difference method (FDM). Although both c-Si and a-Si:H were etched under the same conditions, the etching depth of a-Si:H was slightly deeper than that of c-Si. This indicates that the etching rate of a-Si:H may be slightly higher than that of c-Si. The difference in the etching depths did not affect the waveguide performance.

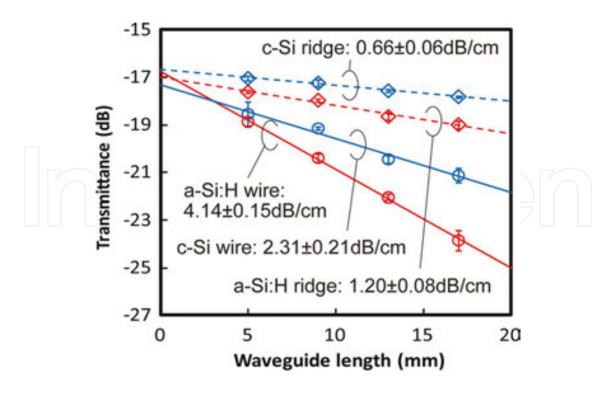


**Figure 2.** (a)–(d) Cross-sectional SEM images of the fabricated wire and ridge waveguides. (a) a-Si:H wire, (b) a-Si:H ridge, (c) c-Si wire, and (d) c-Si ridge waveguides. (e)–(f) Normalized main electrical field profiles calculated by the finite difference method.

#### 2.3. Results and discussion

The propagation losses of the fabricated waveguides were evaluated using a standard cutback method. To laterally couple light from/to all waveguides through the common edge of a device chip, waveguides were arranged in a convoluted manner with a curve radius of 10  $\mu$ m for the wire waveguides and 400  $\mu$ m for the ridge waveguides. The device chips contained 12 wire waveguides or 16 ridge waveguides with lengths ranging from 0.5 to 1.7 cm. Numerical analysis based on FDM indicated that the single mode conditions were satisfied for both the wire and ridge waveguides. The bending losses were also estimated to be negligible for the q-TE mode at 1.55  $\mu$ m. The loss measurement was carried out for the q-TE mode only because the ridge waveguides do not support a quasi-transverse magnetic (q-TM) mode.

Light emitted from an amplified spontaneous emission (ASE) source was filtered by wavelength-tunable filters with 1-nm bandwidth and polarized, resulting in transverse electric (TE)polarized light around 1.55  $\mu$ m. The light was directed into the waveguides through a lenstipped polarization maintaining fiber. The output light was collected using a lens-tipped single-mode fiber to send the output to an optical power meter. **Figure 3** plots the measured transmittance against waveguide length. The propagation losses were extracted from the slopes of the linear fittings. The propagation losses were 4.14 ± 0.15 and 1.20 ± 0.08 dB cm<sup>-1</sup> for the wire and ridge a-Si:H waveguides, respectively. The SOI waveguides had losses of 2.31 ± 0.21 and 0.66 ± 0.06 dB cm<sup>-1</sup> for the wire and ridge waveguides, respectively.



**Figure 3.** Measured propagation losses of wire and ridge waveguides with 220-nm-thick Si cores. The error bars show the standard deviations ( $\pm \sigma$ ) of the measured transmittances.

To measure the wavelength dependence of the transmittance of the waveguides in the C-band from 1530 to 1565 nm, TE-polarized ASE light was fed into the 17-mm-long waveguides, and the output light was measured using an optical spectrum analyzer. **Figure 4** shows the measured dependences of transmittance on wavelength. The ridge waveguides have smoother curves than the wire waveguides, indicating that the ripples may originate from light scattering by the roughness of the waveguide sidewall. Such roughness is unintentionally formed during the lithography and etching processes.

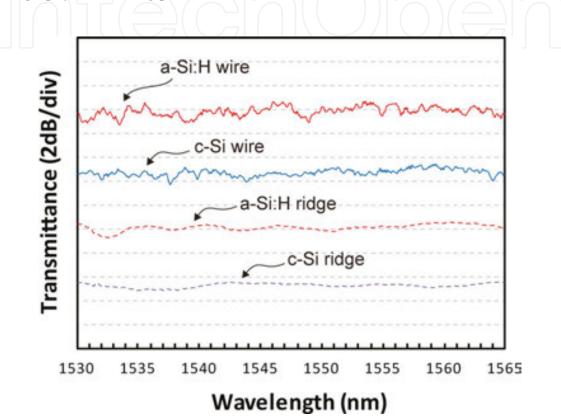


Figure 4. Measured dependences of the transmittance of each fabricated waveguide on wavelength.

Our a-Si:H has a comparable material loss to c-Si. However, the a-Si:H waveguides show higher propagation loss than their c-Si counterparts even though both the a-Si:H and c-Si waveguides were fabricated using the same process. The presence of microvoids in the a-Si:H films is a possible origin of their propagation loss. It has been argued that the dihydride SiH<sub>2</sub> and trihydride SiH<sub>3</sub> make a-Si:H films heterogeneous, producing H clusters or microvoids in the films [22]. Fourier transform infrared absorption spectroscopy of our a-Si:H films revealed a stretching mode from the monohydride SiH around 2000 cm<sup>-1</sup> (7–8% H content); no shoulder or peak was observed at higher wavenumber. Therefore, the density of microvoids in our a-Si:H films would be sufficiently low that the light scattering at the microvoids is negligible. In contrast, the top surface of the as-grown a-Si:H is approximately three times rougher than that of the c-Si on a SOI wafer, as illustrated in the atomic force microscope (AFM) images in **Figure 5**. The loss differences between the a-Si:H and c-Si waveguides probably originates from the roughness of the top surface, considering that the absorption of the upper and lower cladding materials is negligible [23].

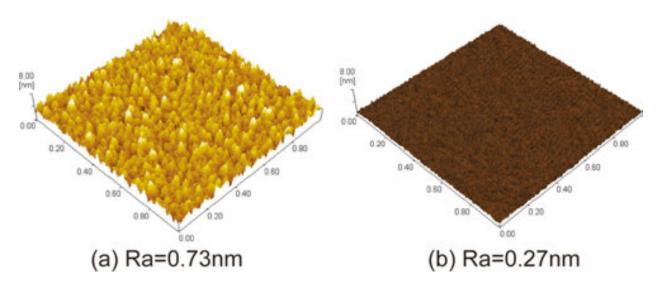


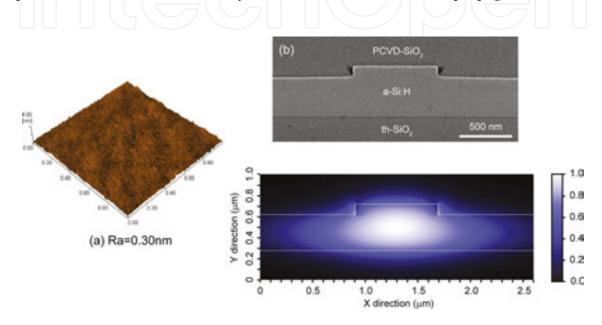
Figure 5. AFM images of the surfaces of (a) as-grown a-Si:H and (b) a commercially available SOI wafer.

Photoinduced degradation is an intrinsic problem of a-Si:H, which is caused by the Si dangling bonds that are generated through non-radiative recombination of photoexcited electron-hole pairs [24]. The degradation of a-Si:H in the telecommunication wavelength range has been reported [5, 9]. In waveguide applications of a-Si:H, the dangling bonds may cause an additional absorption loss. In particular, several research groups are concerned about photo-induced degradation because high-power light is input into the waveguides for optical nonlinear devices. Fortunately, the loss of our a-Si:H waveguides did not increase during measurement. This is probably because our a-Si:H has an optical gap of 1.75 eV, as determined by Tauc plot. Such a wide bandgap markedly decreases two-photon absorption, which suppresses non-radiative recombination of photogenerated carriers and thus photoinduced degradation.

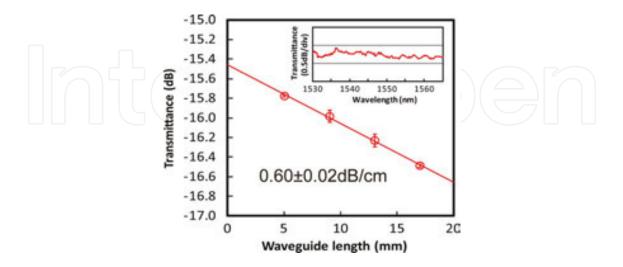
#### 2.4. Waveguide with ultra-low loss

In the previous section, we showed that a-Si:H has a rougher surface than c-Si, resulting in an increased propagation loss. Similarly, the roughness of the waveguide sidewalls contributes to the loss. Thus, minimizing roughness is an effective way to further lower the loss in a-Si:H waveguides. In this work, two approaches to lower roughness were tested. One is a planarization of the top surface of a-Si:H by CMP. The other was introduction of a shallow-ridge geometry. When the material loss of a core is sufficiently low, shallow ridges can lower the propagation loss because of the low depth of the etched sidewalls. First, a 500-nm-thick a-Si:H film was deposited on a 2-µm-thick thermal oxide top layer on a Si wafer. Then, the as-grown surface layer was polished by CMP, resulting in the removal of approximately 60 nm of the a-Si:H layer. **Figure 6(a)** shows the polished surface observed by AFM, which has a roughness comparable to that of a c-Si surface. Ridge waveguides with a ridge height of 100 nm were

then formed on the polished a-Si:H, as depicted in **Figure 6(b)**. **Figure 7** presents the measurement results for the a-Si:H shallow-ridge waveguide. The measured propagation loss was  $0.60 \pm 0.02$  dB cm<sup>-1</sup> for the q-TE mode at 1.55 µm, which is the lowest reported propagation loss for an a-Si:H waveguide. Also, the dependence of the transmittance on the wavelength in the C-band is within a 0.5-dB range for the 17-mm-long waveguide (inset of Figure 7). Zhu et al. [13] reported that the CMP process may generate new Si dangling bonds at the surface, substantially increasing the propagation losses. While our CMP process lowered the losses, the passivation of surface defects may be needed to further decrease propagation losses.



**Figure 6.** (a) AFM image of a polished a-Si:H surface, (b) cross-sectional SEM image, and (c) main electrical mode profile of the q-TE mode for a shallow-ridge waveguide.



**Figure 7.** Measured transmittances of waveguides with 440-nm-thick a-Si:H cores. The error bars show the standard deviations  $(\pm \sigma)$  of the measured values. The inset shows the wavelength dependence of the waveguide in the C-band for a 17-mm-long shallow-ridge waveguide.

## 3. Vertical interlayer transition devices

## 3.1. VIT device structure and design

## 3.1.1. Structure of the VIT device

An optical VIT is required to construct 3D PICs. The optical connection of vertically stacked optical circuit layers dramatically enhances the architecture flexibility of a circuit. Figure 8 shows our concept of a VIT device [25]. The lower Si waveguide is optically coupled with the upper a-Si:H waveguide through the silicon oxynitride (SiON) secondary core (SC). The upper and lower waveguides are isolated with a SiO<sub>2</sub> interlayer. The SiON SC is located on the SiO<sub>2</sub> interlayer, meaning that the lower Si waveguide is spatially separated from the SC. Here, a wide, thin SiON SC is used because it enables efficient optical coupling from the lower Si tapered waveguide to the overlying SC. The evanescent field of the SC expands outward from the SC core. With regard to the coupling of the SC with the upper a-Si:H tapered waveguide, the coupling mechanism is similar to that of a typical inverse-taper spot-size converter [26– 29]. Such a VIT device is predicted to achieve efficient, broadband and polarization-insensitive vertical light coupling. We employed a knife-edge taper technique that can form unique inverse tapers using a CMOS backend-compatible process. The tapered waveguides have a trapezoidal cross-section. Near the taper end, the cross-section becomes triangular, with its height gradually decreasing toward the end. Figure 9 shows a schematic diagram of the knifeedge tapered waveguide together with its optical mode fields calculated by the FDM [30]. The details of the fabrication process are described in Section 3.2.

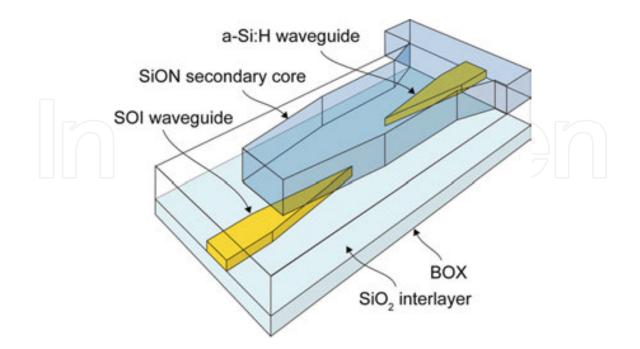
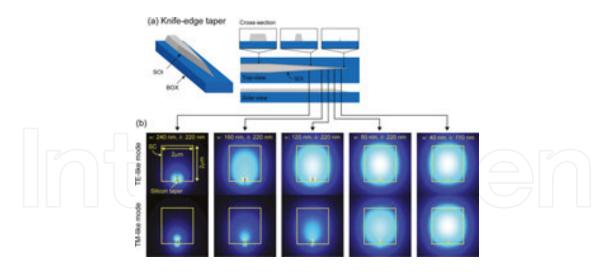


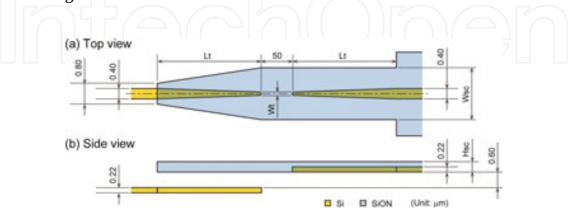
Figure 8. Schematic diagram of a VIT device.



**Figure 9.** (a) Schematic diagrams of the knife-edge tapered waveguide. (b) Main electrical fields for the optical modes of the knife-edge tapered waveguide at 1.55  $\mu$ m calculated using FDM. The refractive index of the secondary core was assumed to be 1.535, and the cladding material was assumed to be SiO<sub>2</sub>.

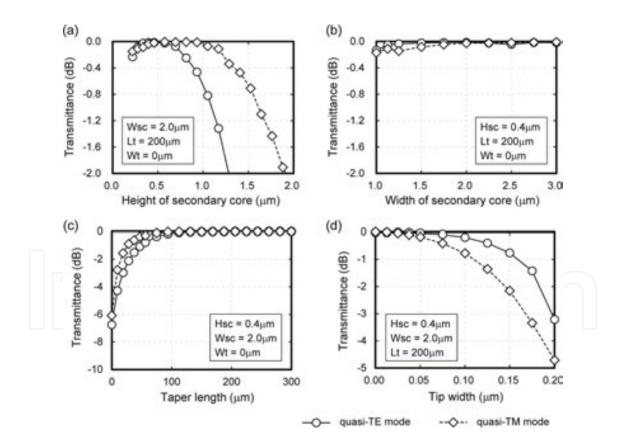
#### 3.1.2. Design of the VIT device

The dimensions of the SiON SC were optimized to minimize the insertion losses for both q-TE and q-TM modes of light at 1.55  $\mu$ m using a numerical analysis based on an eigenmode expansion (EME) method. **Figure 10** presents the structural parameters used in the simulation. The Si waveguide was 400 nm wide and 220 nm high, and the distance between the two tapered tips of the waveguides was 50  $\mu$ m. The upper and lower waveguides were isolated by a 0.6- $\mu$ m-thick SiO<sub>2</sub> interlayer. The interlayer thickness satisfied design requirements for optical loss and crosstalk at orthogonal crossings between vertically adjacent Si waveguides [31]. The SC had a tapered structure near its end to lower loss caused by refractive index discontinuity. The tip width was 0.8  $\mu$ m, which was a critical dimension for processing. The refractive indices of Si, SiON, and SiO<sub>2</sub> used in the simulation were 3.48, 1.62, and 1.44, respectively. In the actual devices, knife-edge tapers were used, but the simulation used standard inverse tapers, as depicted in **Figure 10**.



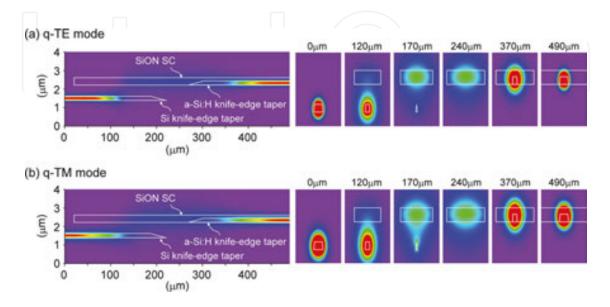
**Figure 10.** (a) Top view and (b) side view of the simulation model. The dimensions in these views are given in micrometers.

Figure 11(a) displays the transmittances calculated for various SiON SC heights (Hsc) when the SC width (Wsc) was fixed at 2.0 µm. The Si taper length (Lt) was set at 200 µm while the tip width of the Si tapers (Wt) was fixed at 0 µm; that is, ideal horizontally inverse tapers were assumed. Maximum transmittances for both the q-TE and TM modes were obtained at Hsc of around 0.4 µm. A thick SC (over 0.6 µm) decreases the transmittance because of smaller overlap of the optical field between the SC and lower Si taper. In contrast, Figure 11(b) shows the width of the SC is insensitive to the transmittance when Hsc is 0.4 µm, Lt is 200 µm, and Wt is 0 µm. According to the above EME simulations, the transition losses are minimized to 0.013 and 0.025 dB for the q-TE and TM modes, respectively, when Hsc is 0.4 µm and Wsc is 2.0 µm. The dependence of transmittance on Lt when Hsc is 0.4 µm, Wsc is 2.0 µm, and Wt is 0 µm is illustrated in Figure 11(c). A taper that is more than 150 µm long is required to achieve low loss (<1%) and polarization-independent operation. In the above simulation, Wt was assumed to be 0 µm. However, the width of a taper tip is actually a finite value. Figure 11(d) summarizes the dependence of transmittance on Wt. A knife-edge tapered structure could achieve a tip width of less than 50 nm [28–30]. Assuming Wt is 50 nm, the worst transition loss caused by the finite tip of the knife-edge taper would be 0.054 and 0.18 dB for q-TE and TM modes, respectively.



**Figure 11.** Calculated transmittances of VIT devices as a function of (a) SiON secondary core (SC) height (Hsc) when SC width (Wsc) =  $2.0 \mu m$ , (b) Wsc when Hsc =  $0.4 \mu m$ , (c) taper length (Lt) when Wsc =  $2.0 \mu m$  except in (d) tip width of the Si tapers (Wt) when Wsc =  $2.0 \mu m$  Hsc =  $0.4 \mu m$ . Lt was fixed at 200  $\mu m$  except in (c), while Wt was 0  $\mu m$  except in (d). Circles on the solid lines are the transmittances for the q-TE mode, and diamonds on the dashed lines are the transmittances for the q-TM mode.

**Figure 12** presents the simulated light propagation in a VIT device that incorporates the knifeedge tapered waveguides with the optimized structural parameters from above. The sidewall angle of the Si waveguide tapers was assumed to be 80°. The light in the lower Si waveguide was transferred to the upper Si waveguide with no apparent loss for both the q-TE and q-TM modes.



**Figure 12.** Side and cross-sectional views of the simulated light propagation in a VIT device with knife-edge tapered waveguides for (a) q-TE and (b) q-TM modes. The figure above each cross-sectional view shows its position shown in the side view.

### 3.2. Fabrication of a VIT device

First, the fabrication process for the knife-edge tapered waveguides is described. The knifeedge tapered waveguides were produced by a combination of a double-patterning technique and angled sidewall Si etching. Figure 13 outlines the principle of the knife-edge tapering approach. In the initial wafer processing, a Si waveguide is formed, accompanied with an additional parallelogram structure. Subsequently, Si in the additional structure is partly removed under the same process conditions, resulting in the formation of a knife-edge tapered structure. In the middle of the taper, the edge of the second pattern is on the flat top of the Si parallelogram structure. In this case, the Si remaining after the etching has a trapezoidal crosssection. Near the taper tip, the edge of the second pattern is at the sloped sidewall. In this case, the remaining Si has a triangular cross-section, the height of which tapers down toward the end. Combining these two individual patterns enabled us to form ultrafine patterns beyond the photolithographic resolution limit. Furthermore, this technique possesses a large fabrication tolerance. Irrespective of the overlay misalignment, the second pattern crosses the first pattern because of the margin of the first pattern. The sidewalls of the etched Si were angled by controlling the etching chemistry; that is, the mixing ratio of SF<sub>6</sub> to  $C_4F_8$ . Figure 14(a) shows SEM images of the cross-sections of etched silicon with mixing ratios of SF<sub>6</sub> to C<sub>4</sub>F<sub>8</sub> of 33 and 25%, which gave sidewall angles of ~80° and ~60°, respectively. The AFM image of the fabricated knife-edge taper in **Figure 14(b)** reveals that an ultra-narrow taper structure was successfully formed.

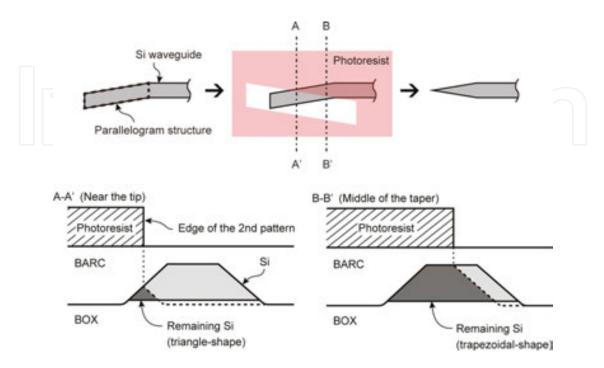
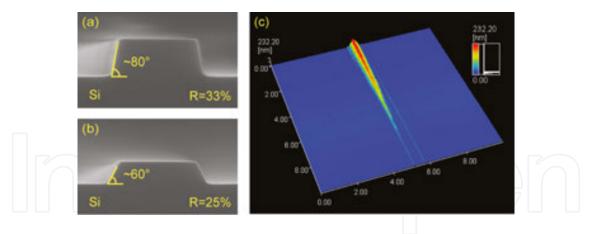


Figure 13. Schematic diagrams of the principle of knife-edge tapering. BARC is bottom anti-reflective coating.



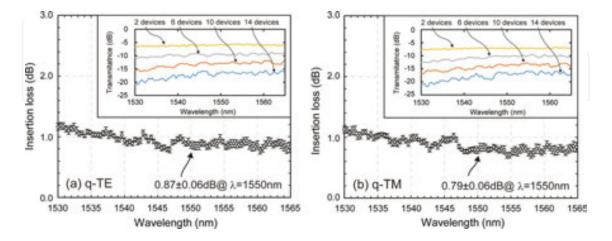
**Figure 14.** Cross-sectional SEM images of the etched silicon with mixing ratios of SF<sub>6</sub> to  $C_4F_8$  of (a) 33% and (b) 25%. (c) AFM image of the fabricated knife-edge taper near its end.

VIT devices were fabricated on an SOI wafer with a 220-nm-thick top Si layer and a 2- $\mu$ m-thick BOX layer. Si waveguides that were terminated with the knife-edge tapers were fabricated using an i-line stepper and ICP-RIE. This step was followed by SiO<sub>2</sub> deposition at 350°C by PECVD followed by top surface planarization by CMP. SiO<sub>2</sub> was again deposited by PECVD to adjust the SiO<sub>2</sub> thickness to precisely 0.6  $\mu$ m. Subsequently, a 220-nm-thick a-Si:H film was deposited using our low-loss a-Si:H thin-film technology described in Section 2. The a-Si:H

waveguides were fabricated by the same procedure that was used to produce the lower SOI layer. A 0.4- $\mu$ m-thick SiON film was deposited at 350°C by PECVD. SiON SCs with a width of 2  $\mu$ m were then fabricated using an i-line stepper and fluoroform-based dry etching. Refractive indices of the deposited a-Si:H and SiON measured using ellipsometry were 3.50 and 1.62, respectively. Finally, the wafer was covered with a 1.5- $\mu$ m-thick SiO<sub>2</sub> film that served as a cladding layer.

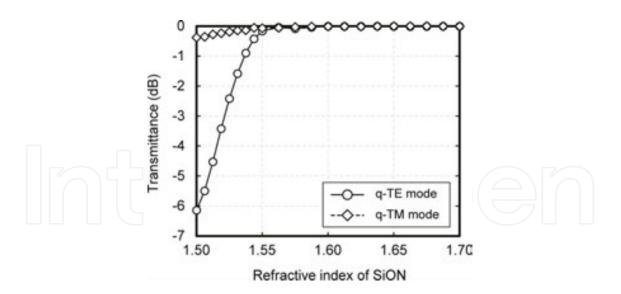
#### 3.3. Results and discussion

The fabricated VIT devices were evaluated in the C-band wavelength range. The insertion losses of the fabricated VIT devices were extracted from their transmittance differences between the optical paths of different numbers of VIT devices. That is, paths with 2, 6, 10, and 14 VIT devices were investigated. All paths used Si and a-Si:H waveguides of the same length. An ASE light source was used to measure the transmittance of the devices in the wavelength range from 1530 to 1565 nm. The ASE light was polarized and then the polarized light was sent using a polarization maintaining fiber. The light was fed into each device chip using condenser lenses. The output light was collected by condenser lenses and measured by an optical spectrum analyzer. Figure 15 shows the insertion losses of the VIT devices together with the measured transmittances of the optical paths with different numbers of VIT devices. The measured insertion losses at 1550 nm were  $0.87 \pm 0.06$  and  $0.79 \pm 0.06$  dB for the q-TE and q-TM modes, respectively. These values correspond to transition efficiencies of 82 and 83% for the q-TE and q-TM modes, respectively. Also, the wavelength dependences of the insertion losses were less than ~0.5 dB in the C-band for both polarizations. In the shorter wavelength region, the insertion loss increased slightly. This tendency contrasts with the EME simulation results that predicted flat wavelength dependences in the C-band. The slight increase is caused by the absorption of the SiON film around 1510 nm. This absorption originates from the higherorder vibrational modes of the N-H bonds in the SiON film fabricated by low-temperature PECVD.



**Figure 15.** Measured insertion losses of VIT devices for (a) q-TE and (b) q-TM modes. The insets show the measured transmittances of the optical paths when they contain 2, 6, 10, and 14 VITs. Each transmittance value is averaged from the same four optical paths. The error bars show the standard errors.

The experimental losses are larger than those predicted by the EME simulation. To investigate these discrepancies, we performed numerical analyses with varying refractive indices of the a-Si:H and the SiON. The analyses revealed that the discrepancies cannot be explained by the refractive index variation of a-Si:H. Actually, our experiments indicated that the deposition of a-Si:H films is reasonably reproducible, so the variation of refractive index is typically less than  $\pm 2\%$ . Even when the refractive index of a-Si:H fluctuates by  $\pm 5\%$ , the numerical analyses suggested the loss deterioration of the VIT devices was less than 0.01 dB. Because the measured refractive index of a-Si:H was 3.50, the deviation from the value (3.48) used for the device design should be negligible. However, the numerical analyses showed that loss deterioration caused by variation of the refractive index of SiON would be considerable when its refractive index is less than 1.55, as shown in Figure 16. However, as long as the refractive index of SiON exceeds 1.55, low transition loss can be obtained for both polarizations. Because measured refractive index of SiON was 1.62, and is unlikely to drop below 1.55, the refractive index variation of SiON does not affect the performance of the VIT devices. Overall, the discrepancies between simulated and experimental losses of the VIT devices cannot be explained by the variations of the refractive indices of either a-Si:H or SiON. Furthermore, additional loss of the VIT devices caused by the finite tip width makes only a minor contribution (see Figure 11(d)). Therefore, we concluded that these discrepancies originate mainly from the waveguide losses of the Si and SiON waveguides. It should be noted that these numerical analyses indicate the VIT devices are more robust against unwanted variation of refractive index than interlayer coupling devices based on grating couplers, which are sensitive to the refractive indices of both waveguide and cladding materials.



**Figure 16.** Calculated transmittances of the VIT devices as a function of the refractive index of SiON. The structural parameters are as follows: Hsc =  $0.4 \mu m$ , Wsc =  $2.0 \mu m$ , Lt =  $200 \mu m$ , and Wt =  $0 \mu m$ . The refractive index of a-Si:H was set at 3.48 to match that of the SOI.

**Table 2** compares the performance of optical cross-coupling devices using a-Si:H deposited at low temperature that have been reported to date. All the devices are highly efficient. The vertical directional coupler has the most compact device, and its fabrication is simple, but the

interlayer isolation is insufficient for 3D PICs [31]. The grating coupler effectively isolates the layers, but its bandwidth is relatively narrow and grating couplers have strong polarization dependence. In addition, metal mirrors are required to increase the efficiency of these couplers, resulting in complex fabrication. The VIT devices showed broadband, polarization-insensitive performance. However, long tapered waveguides are required in the VIT devices to suppress the losses and their fabrication process is complex because of the SC. Although the taper length was 200  $\mu$ m in our work, the length of the tapers can be shortened to 150  $\mu$ m with only a small increase of loss (see **Figure 11(c)**), resulting in a total device length of 350  $\mu$ m. A parabolic taper structure would be advantageous to make the taper length shorter while keeping the mode conversion loss low [32].

Reference	[33]	[34]	Our work
Туре	Inverse tapers	Grating coupler + mirrors	Inverse tapers + secondary core
Interlayer	200-nm-thick SiO2	1000-nm-thick SiO2	600-nm-thick SiO <sub>2</sub>
Efficiency	~90% (TE)	83% (TE)	82% (TE), 83% (TM)
Polarization	Single	Single	Both
Length	30 µm	114 µm	450 μm
1-dB Bandwidth	Not described	~20 nm	> 35 nm
Process	Simple	Complex	Complex

Table 2. Performance comparison of optical cross-coupling devices with vertically stacked optical circuits.

In our work, VIT devices were demonstrated on SOI wafers. If the lower Si layer on the BOX was replaced with a-Si:H on  $SiO_2$  deposited at low temperature, the VIT device performance could be equivalent to that of the VIT devices reported in this section. This means that these VIT devices can be realized on  $SiO_2$ -passivated CMOS chips. Therefore, 3D on-chip optical interconnects with efficient, broadband, and polarization-insensitive VIT functionality that are compatible with CMOS metal wiring layers are potentially available.

## 4. Conclusions

In this chapter, we described our research on a-Si:H photonics. Importantly, a-Si:H photonics is promising to achieve CMOS backend integration of optical interconnects because a-Si:H with ultra-low loss can be obtained at a deposition temperature of less than 400°C. Using our high-quality Si thin-film technology, we demonstrated a-Si:H waveguides with ultra-low loss and high-performance VIT devices. Also, electrically driven refractive index changes in a-Si:H were realized by introduction of  $\mu$ c-Si:H. These device technologies provide a fundamental platform for design of 3D PICs. Further development of a-Si:H photonics will drive the realization of on-chip optical interconnects in the future.

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