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Chapter 6

Low-Temperature PureB CVD Technology for CMOS Compatible Photodetectors

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Additional information is available at the end of the chapter

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Abstract

In this chapter, a new technology for low-temperature (LT, 400°C) boron deposition is developed, which provides a smooth, uniform, closed LT boron layer. This technology is successfully employed to create near-ideal LT PureB (pure boron) diodes with low, deep junction-like saturation currents, allowing full integration of LT PureB photodiodes with electronic interface circuits and other sensors on a single chip. In this way, smart-sensor systems or even charge-coupled device (CCD) or complementary metal oxide semiconductor (CMOS) ultraviolet (UV) imagers can be realised.

Keywords: low-temperature boron deposition, ultrashallow p^+n junction photodiode, chemical vapour deposition, UV photodetector, CMOS imager

1. Introduction

Over the last few years, we have witnessed an increase in the demand for both high-performance ultraviolet and low-energy electron detectors. These detectors are used in high-tech applications such as optical lithography and electron microscopy, medical imaging, protein analysis and DNA sequencing, forensic analysis, disinfection and decontamination, space observation, etc.

To meet these demands, a new silicon detector technology has been proposed by TU Delft called "PureB" (pure boron) technology [1]. Conventional PureB technology is employed to fabricate high-performance photodiodes for vacuum/extreme/deep-UV (VUV/EUV/DUV) light, low-energy electrons down to 200 eV, and X-ray drift detectors [2–5]. A comparison of

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PureB technology to state-of-the-art Si-based UV and electron detectors is presented in **Tables 1** and **2**, respectively.

Detector	ETH PtSi-nSi	IRD AXUV	IRD SXUV[a]	IRD UVG	Hamamatsu (S5226)	PureB[b]
Junction type	Schottky		n-on-p		p-on-n	p-on-n
EUV sensitivity (A/W) at 13.5 nm	~0.2[c]	~0.265	~0.23	Unknown	Unknown	0.267
Stability under EUV	Unknown[d]	Not stable	Good[e]	Unknown	Unknown	Δ ~ 3%[f]
VUV sensitivity (A/W) at 193 nm	~0.03	~0.1	~0.01	~0.137	~0.1	0.102
VUV sensitivity (A/W)at 157 nm	~0.02	~0.1	<0.01	Unknown	Unknown	0.123
VUV sensitivity (A/W)at 121 nm	≤0.02	Unknown	<0.01	<0.05	Unknown	0.116
Stability under DUV/VUV	Δ ~ 2%	Not stable	Unknown	Δ ~ 10%	Not stable	Δ ~ 4%
References	[6, 7]	[6, 8–10]	[9, 10]	[6, 8]	[6]	[2, 3]

[a]SXUV: Si-based n-on-p junction photodiodes with nitride metal silicide front window.
[b]Data are based on as-deposited PureB photodetectors without any post-processing thermal annealing.
[c]Value from measurement at PTB [2, 3].
[d]Stability proven only in the VUV range [6].
[e]No more information is given in the reference.
[f]Δ: reduction in responsivity based on the data reported in the mentioned references.

Table 1. Performance overview of representative commercially available Si-based UV detectors compared to the PureB UV photodetector.

Detector	Commercial BSE	Commercial vCD	Delta doped e2V CCD 97	PureB BSE
Electron signal gain[a] at 1 KeV	~46	~126	~112	213
Electron signal gain at 500 eV	~18	~52	~47	102
Electron signal gain at 200 eV	Unknown	Unknown	~13	34
Stability	Δ ~ 5%	Δ ~ 5%	Unknown	Δ ~ 4%
References	[11, 12]	[11, 12]	[13]	[4]

[a]Electron signal gain, G_{ph}, is defined as I_{ph}/I_{beam}, where I_{ph} is the output current of the photodiode and I_{beam} is the current of the incident electron beam, assuming a negligible dark current.

Table 2. Performance overview of representative commercially available, research-reported Si-based electron detectors compared to the PureB electron detector.

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However, due to the relatively high temperature (HT) of boron deposition (500–700°C), it is hard to integrate this technology fully into a standard integrated circuit/ complementary metal oxide semiconductor (IC/CMOS) process flow.

In this chapter, a newly developed technology for low-temperature (LT, 400°C) boron chemical vapour deposition (CVD) is presented, providing a smooth, uniform, closed LT boron layer. This technology is successfully employed to create near-ideal LT PureB diodes with low, deep-junction-like saturation currents. The low-temperature deposition at 400°C makes it possible to integrate the LT PureB photodiodes fully with electronic interface circuits and other sensors on a single chip. In this way, smart-sensor systems or even charge-coupled device (CCD) or CMOS ultraviolet (UV) imagers can be realised.

What this chapter demonstrates is near ideal[1], highly sensitive, radiation-hard, low leakage current diode characteristics. Moreover, since the boron deposition is conformal and highly selective to Si, PureB technology is shown to be an attractive candidate for creating junctions on silicon nanowires and advanced CMOS transistors including a source/drain in p-type FinFETs. The impressive properties that PureB devices provide have resulted in this technology becoming commercially available very quickly for ASML EUV lithography tools and scanning electron microscopy (SEM) systems.

2. An analytical kinetic model for boron CVD

In references [14] and [15], the pattern dependency and the loading effect of CVD boron deposition are identified as sources of non-uniformity of the boron layer. Since investigating these two effects requires a thickness-monitoring technique, an end-of-line resistance measurement is introduced as a non-destructive, accurate means of monitoring the boron layer uniformity with fine resolution [16].

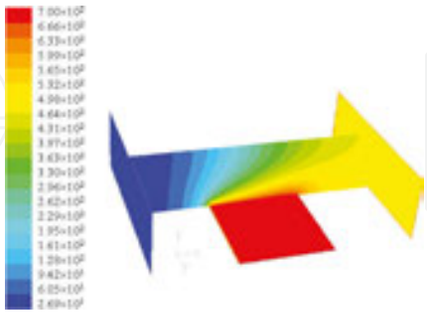

Figure 1. Temperature distribution profile simulated by commercial FLUENT© software for an ASM Epsilon One CVD reactor when the total pressure is ATM. The hydrogen gas is considered to be the main gas flowing over the susceptor, in order to simplify the simulation. The susceptor is heated up by an assembly of lamps to the deposition temperature (here 700°C) [19].

[1] Diode ideality factor, n≈1

In this section, an analytical model is established to describe the deposition kinetics and the deposition chamber characteristics that determine the deposition rate (DR) over the wafer. This pre-deposition prediction tool can be used to improve the set-up and control of the final deposition [17, 18]. It is also very useful for transferring recipes from one reactor to the other.

Some considerations such as the diffusion behaviour of the reactant (here BH_3 species) through the stationary boundary layer over the wafer with the mechanism of the diffusion, the gas-phase processes and the related surface reactions are taken into account by this model. To develop the model, the actual parabolic gas velocity and temperature-gradient profiles in the reactor are considered as well, both of which have been calculated theoretically and also simulated with FLUENT® software as shown in **Figure 1**.

The starting point for developing a mathematical model for the chemical and physical behaviour of the CVD process is the expression for the temperature and velocity profile for a fully developed flow. This can be calculated by solving the equation for energy conservation, the continuity equation and the equation for the motion of the carrier gas:

$$c_g \rho_g u_x \frac{\partial T}{\partial x} = \frac{\partial}{\partial x}\left(\mathrm{k}_0 T^{\beta} \frac{\partial T}{\partial x} \right) = 0 \tag{1}$$

$$\frac{\partial}{\partial y}\left(\mu_0 T^{\gamma} \frac{\partial u_x}{\partial y} \right) = \text{constant} \tag{2}$$

where $u_x(y)$, x, y, $\mu_0 T^{\gamma}$, and $\mathrm{k}_0 T_{\beta}$ are, respectively, the gas velocity profile, axial position in the direction of the gas flow, lateral position perpendicular to the direction of the gas flow, temperature-dependent thermal conductivity and dynamic viscosity of the carrier gas.

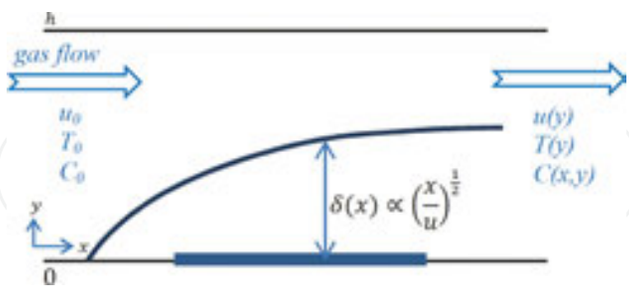

Figure 2. Schematic illustration of a classical boundary layer and reactor conditions over the susceptor.

To develop an analytical model, first we consider a system with a constant temperature in which the active component rapidly decomposes at the susceptor, $y = 0$, for all axial flow positions $x \geq 0$ (**Figure 2**). Therefore, the concentration of the reactant species at $y = 0$ is zero across the entire decomposition zone. The transport of material towards the susceptor in the y-direction goes entirely via gas-phase diffusion (i.e. laminar flow through the stationary boundary layer over the susceptor).

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The equation for mass conservation for this case is as follows:

$$u(y)\frac{\partial C(x,y)}{\partial x} = D\frac{\partial^2 C(x,y)}{\partial y^2} \tag{3}$$

where C and D are the concentration profiles and the gas-phase diffusion coefficient of the active component in the carrier gas, respectively, and $u(y)$ is an expression for the parabolic velocity profile found by solving Eqs. (1) and (2) in the reactor chamber, which is given by

$$u(y) = 4u_0\left(\frac{y}{h} - \frac{y^2}{h^2}\right) \tag{4}$$

Equation (4) is difficult to solve for a parabolic velocity profile. Therefore, the problem is first solved for a constant flow velocity. Thereafter, the influence of a parabolic flow profile on the obtained results is evaluated.

By following the derivation procedure described in more detail in reference [18], the concentration profiles at $y = 0$ can be calculated as

$$\bar{C}(x) = 0.692C_0\exp\left[\frac{-2.52D}{h^2u_0}x\right] \tag{5}$$

This is the average concentration profile of the reactants over the susceptor with a linear velocity profile. This profile will be used to develop the final deposition rate model for boron layer deposition.

Next, the deposition rate of the boron layer deposited in a CVD system by using B_2H_6 over a bare, non-rotating silicon wafer can be calculated as [18]:

$$\mathrm{DR}^{\mathrm{B}}_{\mathrm{BnR}}(x) = 0.264\eta\gamma\beta_1\beta_2 P_{\mathrm{BH_3}} \times \exp\left(-\frac{2.52D}{h^2u_0}x\right) \tag{6}$$

Where

$$\beta_1 = \frac{1}{N_0}\frac{\left(1-\theta_{\mathrm{H(B)}}\right)}{\left(m_{\mathrm{BH_3}}\mathrm{k}T\right)^{\frac{1}{2}}}$$

and

$$\beta_2 = \left(\frac{E_{BH_3-on-B}}{kT} + 1 \right) \exp\left(-\frac{E_{BH_3-on-B}}{kT} \right)$$

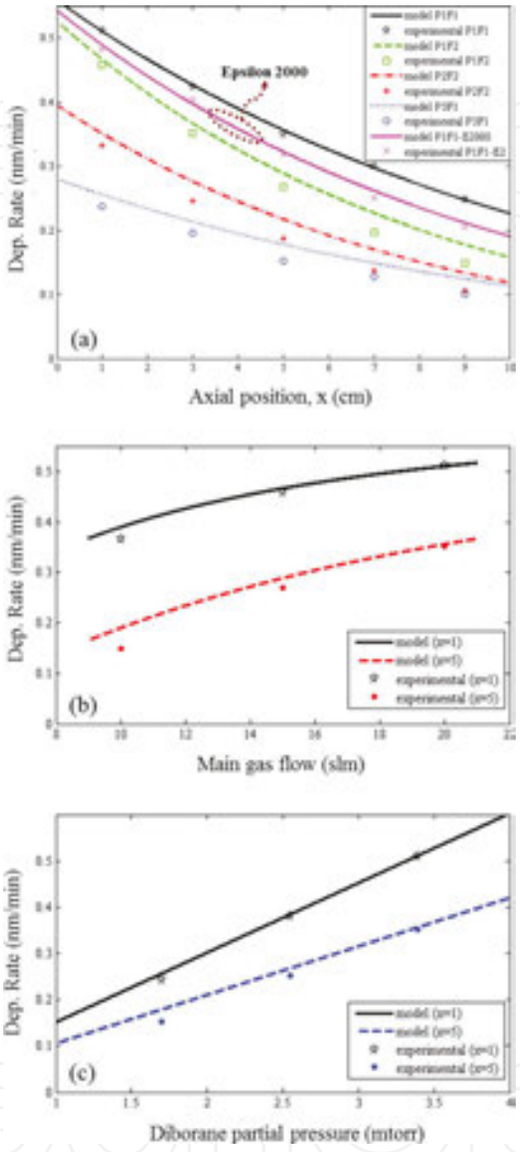

Figure 3. Boron deposition rate extracted either from the model or experimentally as a function of (a) axial position, *x*, (b) main gas flow over the susceptor and (c) diborane partial pressure. In the figure, P_1, P_2 and P_3 are the diborane partial pressure applied, that is, 3.39, 2.55 and 1.7 mtorr, respectively. F_1, F_2 and F_3 are the gas flow applied, that is, 20, 15 and 10 slm, respectively. All experiments were performed at atmospheric pressure [18].

In **Figure 3**, several experimental results are compared to model predictions. It should be noted that a parameter fitting was performed for the ASM Epsilon One. The boron deposition rates are extracted as a function of (a) the axial position, *x*, for different gas flow and diborane partial pressure conditions; (b) gas flow over the susceptor; and (c) input diborane partial pressure including curves for two different axial positions. By only adjusting the reactor/process parameters, this model was also successfully transferred from the ASM Epsilon One to the

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Epsilon 2000 reactor, which has completely different reactor conditions. The experimental results and model predictions for the Epsilon 2000 are shown in **Figure 3a**. It is worth noting that this model is capable of predicting the deposition rate on any two-dimensional (2D) uniformly or non-uniformly patterned wafer such as those used for advanced device fabrication. The very small (less than 5%) deviation of the experimental results and model prediction is plausibly related to the lateral diffusion of the diborane molecules, which becomes more evident at lower gas flow and diborane partial pressure.

It can be seen that the data calculated on the basis of this model fit well with the experimental results and have been very useful not only in the development of uniform boron layers with little pattern dependence but also in the transferring of recipes from one reactor to the other.

3. Low-temperature boron deposition at 400°C

In this section, a newly developed technology for low-temperature (400°C) boron deposition is discussed. The temperature dependency of the kinetics of the boron deposition on patterned Si/SiO_2 surfaces in the temperature range of 700°C–400°C is examined. The recipe-to-deposit pure boron layer is explained. Also, selectivity issues that arise when the boron deposition temperature is reduced from 700°C to 400°C are analysed. Lastly, some provisions are recommended for minimising the undesirable boron deposition on oxide.

3.1. Temperature dependency of boron deposition

To develop a new technology for low-temperature (400°C) boron deposition on silicon, the temperature dependency of the deposition has to be studied to understand the kinetics of the boron deposition on patterned Si/SiO_2 surfaces. This study will be described in this section.

No.	Reaction[a]	Description
[R1]	$B_2H_6(g) + 2Si/B(s) \underset{T}{\Leftrightarrow} 2B\_Si/B(s) + 3H_2(g)$	B-deposition
[R2]	$H(g) + H\_Si/B(s) \underset{T}{\Leftrightarrow} {}^{\circ}Si/B(s) + H_2(g)$	H desorption
[R3]	$H\_Si/B(s) + H\_Si/B(s) \underset{T}{\Leftrightarrow} Si/B\_Si/B(s) + H_2(g)$	Cross-linked
[R4]	$H_2B\_B(s) + {}^{\circ}B(s) \underset{T}{\Leftrightarrow} {}^{\circ}B(s) + H_2B\_B(s)$	Migration

[a]H_Si/H_B and ∘Si/∘B are the silicon/boron atoms with H-terminated dangling bonds or with free dangling bonds, respectively.

Table 3. Chemical reactions of the CVD boron deposition.

The kinetics of boron CVD is investigated in references [17] and [18]. The lateral gas-phase diffusion length of boron atoms over silicon/boron surfaces during the CVD of pure boron

layers is investigated in reference [20]. The chemical reactions contributing to the pure boron CVD are listed in **Table 3**.

For high-temperature deposition (700°C), as described in reference [21], there would be enough energy to facilitate a reaction [R2]. This reaction releases hydrogen from the Si and/or B surface sites as H_2 and leaves Si and/or B sites free for deposition. In this case, the deposition starts very fast, that is, after a few seconds of the surface being exposed to diborane gas under these conditions, and a monolayer of boron appears and covers the surface [1]. **Figure 4** shows a schematic of the HT deposition mechanisms for the first few monolayers of boron layers when a Si surface is exposed to diborane. In the high-temperature deposition, the temperature-related reactions [R1]–[R4] proceed, leading to the adsorption of boron atoms, which are deposited and/or suspended, as well as migration of the boron atoms along the surface. This leads to a smooth, uniform, closed boron layer [17]. Triggering the intermediate reactions also ensures very smooth layers with a roughness that can be around 2 angstroms, as measured by HRTEM imaging and atomic-force microscopy (AFM). This is illustrated by the analysis results shown in **Figure 5** for a 2-nm-thick layer.

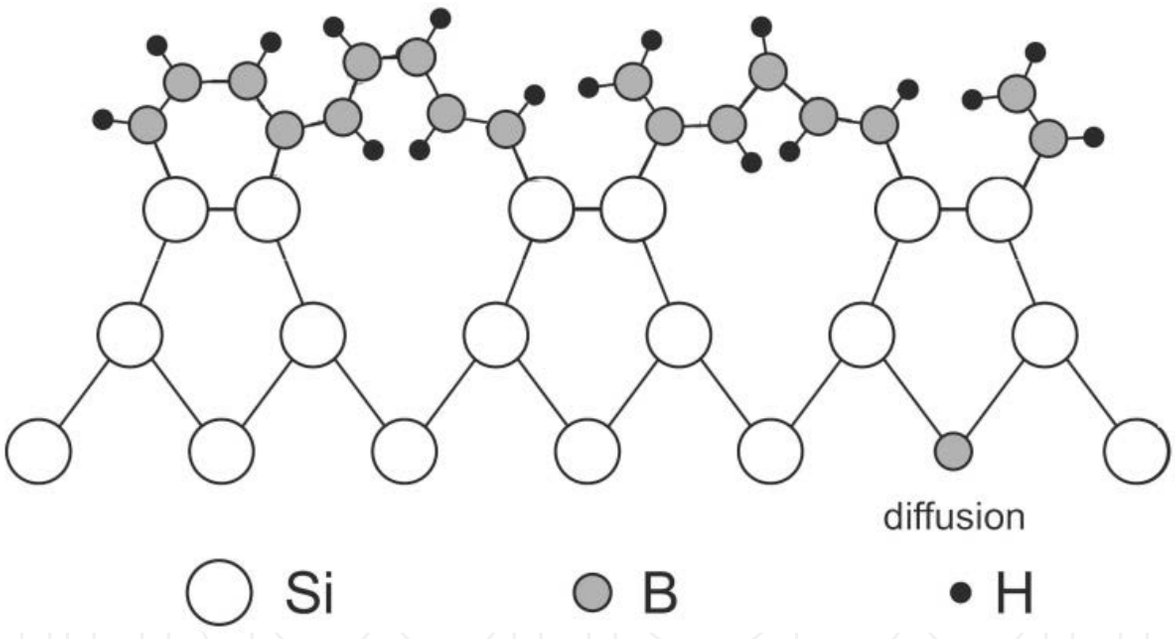

Figure 4. Schematic of the deposition of the first few monolayers of boron layers for HT, 700°C, deposition when an Si surface is exposed to B_2H_6 [22].

However, the experiments show that by lowering the boron deposition temperature from 700 to 400°C, the deposition rate drops considerably from 0.4 to less than 0.01 nm/min for deposition in an H_2 environment, with a laminar gas flow of 20 slm. In this case, even after a long deposition time at 400°C there is almost no measurable layer formed. Moreover, if such a layer is deposited, it is not closed enough to make it suitable for device applications. As a result, the performance of these devices is not comparable to the ones made by conventional 700°C boron deposition.

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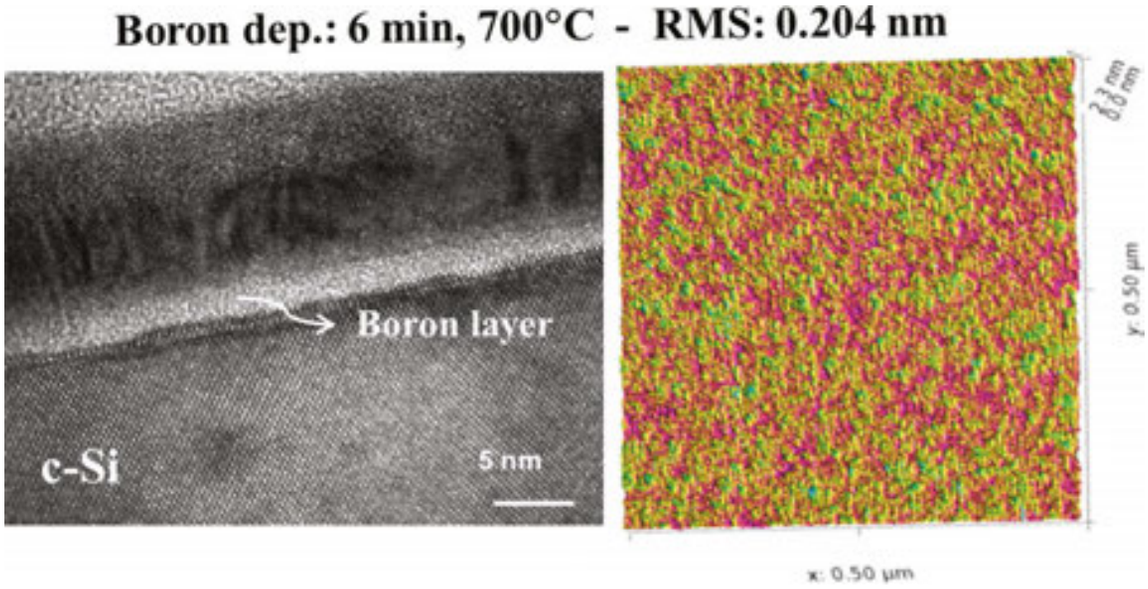

Figure 5. HRTEM image (left) and atomic-force microscopy (AFM) measurement (right) of a 6-min HT-deposited boron layer surface. The AFM image was taken in a 500×500 nm^2 scanning area. This HT layer is smooth and uniform at a thickness of about 2 nm with a root-mean-square (rms) roughness value of 0.204 nm [21].

Several factors are responsible for this negative effect. Firstly, as shown with the previously developed analytical kinetic model given in Eq. (6) [18], the deposition rate varies with the deposition temperature *T*; that is, by lowering the *T*, the DR will drop significantly. Secondly, at such a low deposition temperature, the gas-phase diffusion length is very short. Lastly, by lowering the deposition temperature, the intermediate reactions that produce adsorption at 700°C are no longer effective.

For example, due to the very low amount of energy available, reactions [R2]–[R4] are not promoted in their forward direction. In addition, the presence of hydrogen in the reactor as a carrier gas can suppress the deposition reaction of [R1] because most of the surface sites are occupied by hydrogen that will not readily desorb at 400°C. Consequently, the first monolayer coverage takes more time at this temperature than at 700°C. Also, the inhibited removal of H from the Si surface at low temperatures plays an important role in increasing the roughness. This can be seen in **Figure 6** where the schematics of the deposition of the first few monolayers of boron are shown at LT, 400°C. The HRTEM image and AFM measurement of the LT-deposited boron layer at 400°C with the newly developed recipe discussed in the next section is shown in **Figure 7**. A layer roughness of around 6–8 angstroms was found for a 5-nm-thick layer.

By switching to N_2 as a carrier gas, reactions [R1–[R3] are triggered to proceed in the forward direction, while reaction [R4] is suppressed, which is the necessary intermediate reaction for providing a smooth, uniform, closed boron layer. Thus, only lowering the temperature in the conventional 700°C PureB recipe to 400°C does not guarantee a sufficient layer deposition as a promising capping layer. Therefore, for boron deposition at 400°C, a compromise between the layer deposition rate and layer uniformity and smoothness is necessary, which demands the development of a new recipe, to be discussed in detail in the next section.

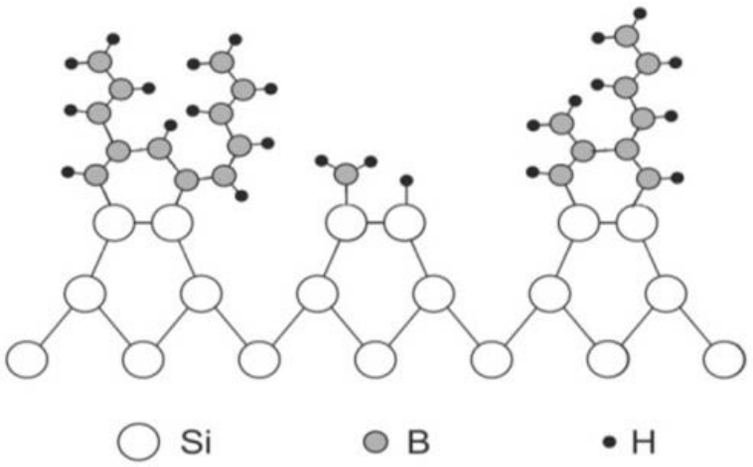

Figure 6. Schematic of the deposition of the first few monolayers of boron layers for (a) HT, 700°C, and (b) LT, 400°C, deposition when an Si surface is exposed to B_2H_6 [22].

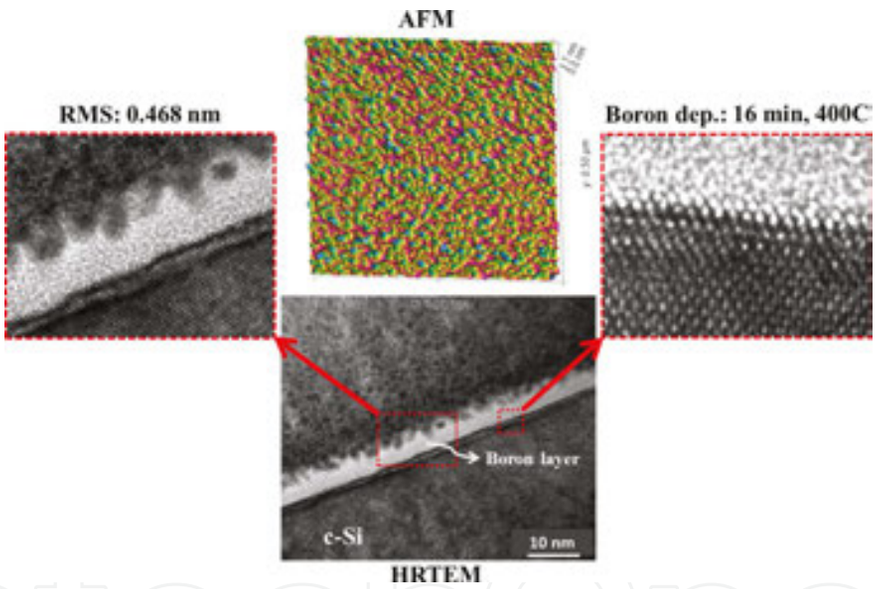

Figure 7. High-resolution TEM image (bottom) and AFM measurement (top) of a boron layer deposited at 400°C for 16 min. In both cases, the thickness of the LT boron layer was extracted to about 5 nm, with a surface rms roughness value of around 4–6 angstroms. The pictures on the left and right show a close-up of the LT boron layer surface roughness and the interface with the Si substrate, respectively [22].

The final point to discuss about the temperature dependency of boron deposition is the investigation conducted of the deposition at the intermediate temperatures 600°C, 500°C and 450°C. By lowering the deposition temperature, the gas-phase diffusion coefficient is lowered and the deposition rate based on Eq. (6) is reduced. In addition, the lower temperatures mean that intermediate reactions [R2]–[R4] are triggered less in their forward direction, resulting in a higher H-coverage of the surface. Moreover, the gas-phase diffusion lengths of boron atoms on both the Si and oxide surfaces also decrease. Altogether, this causes the deposited layer to become increasingly rough when shifting from 600°C to 500°C and 450°C. The properties of

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layers deposited on bare Si at temperatures between 700°C and 400°C are given in **Table 4**. What can be clearly seen is the increase in the roughness of the layers as the deposition temperature decreases.

For deposition at the lower temperatures, 450°C and 400°C, the ellipsometry measurement gave a roughness that is much greater than the average layer thickness, which may not be relevant. These parameters become very dependent on the exact deposition conditions because of both the absence of the other intermediate reactions ([R2]–[R4]) and the fact that the gas-phase diffusion lengths of the boron atoms on both the Si and oxide surfaces decrease.

Next, we will discuss the process and recipe requirements needed to make the boron deposition possible at 400°C.

Pure boron	**Dep. Temp.**[a]				
	700°C	**600°C**	**500°C**	**450°C**	**400°C**
Dep. time (min)	10	10	16	20	60
Thickness (nm)	3.74	3.21	3.14	1.77	1.62
Roughness (nm)	0.38	0.81	1.23	2.64	3.73

[a]The recipes only differ in time and temperature. Their structure is the same in all cases, even for 400°C, and the depositions were done only in an H_2 ambient environment.

Table 4. Thickness and roughness of deposited layers extracted from ellipsometry measurements, as a function of deposition temperature and time.

3.2. LT boron deposition at 400°C

As discussed above, the presence of hydrogen gas can suppress the forward direction of reaction [R2]. This is necessary to release the hydrogen from the surface, to decrease the H-surface coverage, and to suppress reactions [R1] and [R3]. Therefore, the deposition rate is limited by reaction [R2]. The release of hydrogen is important as it facilitates the migration of deposited boron atoms along boron/silicon surfaces via the intermediate reactions [R3] and [R4], leading to a smooth, uniform, closed boron layer deposition. However, in the case of deposition in N_2, unlike that of H_2, reactions [R1]–[R3] are not suppressed, causing hydrogen atoms to be released more easily from the surface and reducing the H-surface coverage. This leads to a higher deposition rate. However, due to the lower mobility of boron atoms in this environment, an increase in boron layer roughness was also expected. Therefore, for boron deposition at 400°C it is necessary to start the deposition in a nitrogen environment to facilitate the first monolayer deposition, and then switch to a hydrogen environment to make the surface smoother and to maintain the boron coverage over the entire silicon opening. This procedure can be repeated a few times with different cycle lengths, as shown schematically in **Figure 8**, to achieve a smooth, uniform, closed boron layer. Lowering the chamber pressure can also facilitate the release of hydrogen from the surface and decrease the H-surface coverage. Thus, deposition at a lower ambient pressure is preferable.

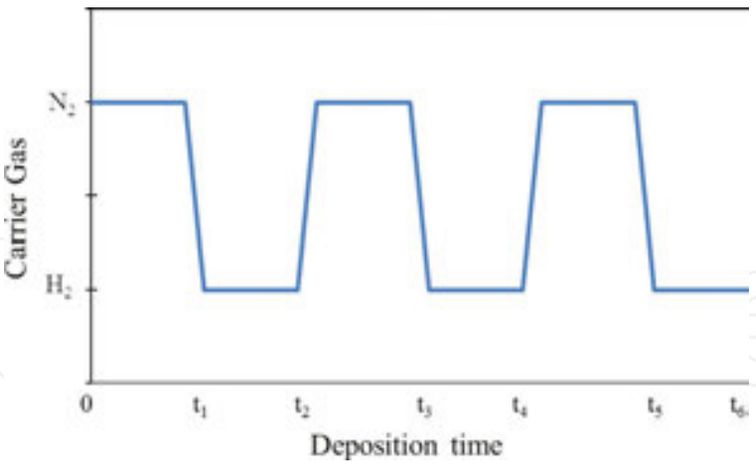

Figure 8. Schematic illustration of carrier gases switching sequences in the LT PureB recipe [22].

The HRTEM image in **Figure 9** shows an LT boron layer deposited at 400°C at a chamber pressure of 95 torr, with the newly developed recipes applied in four- and six-cycle sequences of carrier gas switching. As can be seen in these images, with more switching sequences a smoother boron layer can be created.

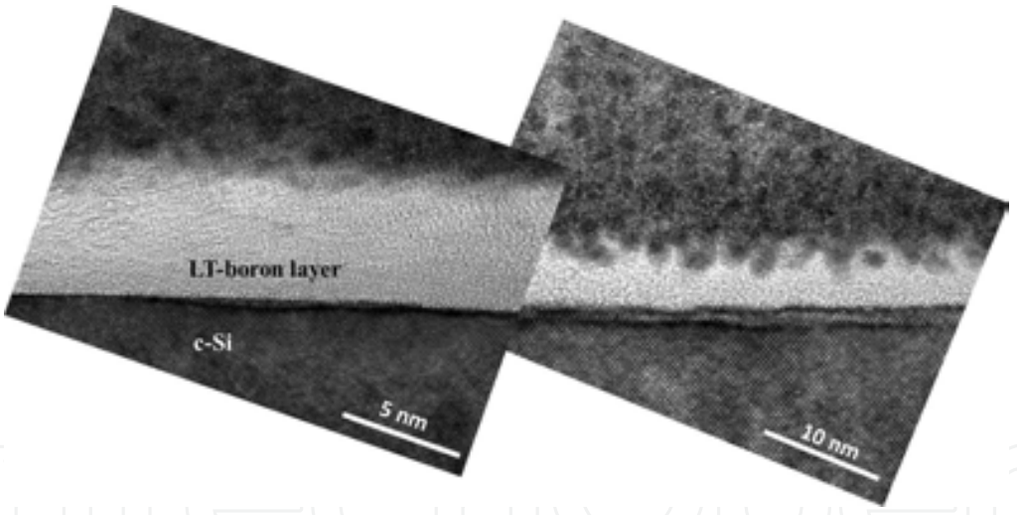

Figure 9. HRTEM image of an LT boron layer deposited after (left) the six- (right) and four-cycle recipe sequences. The deposition chamber pressure was 95 torr [22].

Besides a new recipe, some additional treatments were also needed prior to the wafers being loaded into the reactor. The first treatment was a standard ex situ-cleaning procedure prior to deposition (i.e. 10 min: HNO_3 100% at 25°C; 5 min: DI water; 10 min: HNO_3 70% at 110°C; and 5 min: DI water), immediately followed by a 4-min HF (0.55%) dip to remove native oxide and H-passivate the surface to prevent native oxide formation. This was followed by Marangoni drying, which is an effective substitute for spin-rinse drying, to prevent the formation of wet spots. These wet spots readily form on mixed hydrophilic-hydrophobic surfaces during spin-rinse drying, resulting in particle contamination from residues left behind after evaporation

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[23]. Unlike the 700°C deposition, for the 400°C deposition there was no in situ baking step [1]. Thus, the wafers were directly loaded into the pre-prepared reactor at the 400°C deposition temperature. The lack of the in situ bake made the HF dip with Marangoni drying a very crucial step and meant that the wafers had to be loaded immediately into the N_2-purged load lock of the reactor to prevent any native oxide formation.

3.3. Issues with lowering the deposition temperature of the boron layers

During an HT (700°C) deposition, there is sufficient energy; therefore, the boron atoms that arrive above the oxide-covered surfaces are very mobile and can move around and diffuse laterally to reach the Si surface and become available for the layer deposition. However, during an LT (400°C) deposition, due to the very low amount of available energy, all those boron atoms are very limited in terms of movement and therefore they remain wherever they are. This means that the concentration of the boron atoms over oxide-covered surfaces can increase significantly so that the probability of desorption from the oxide-free sites and/or defects becomes much lower than in the 700°C case. In fact, a significant amount of boron was observed to be deposited on the oxide. This was also promoted by the longer deposition time needed to achieve a reliably closed layer because of the low deposition rate and extra thickness needed to compensate for the large amount of roughness, as can be seen in **Figure 10**.

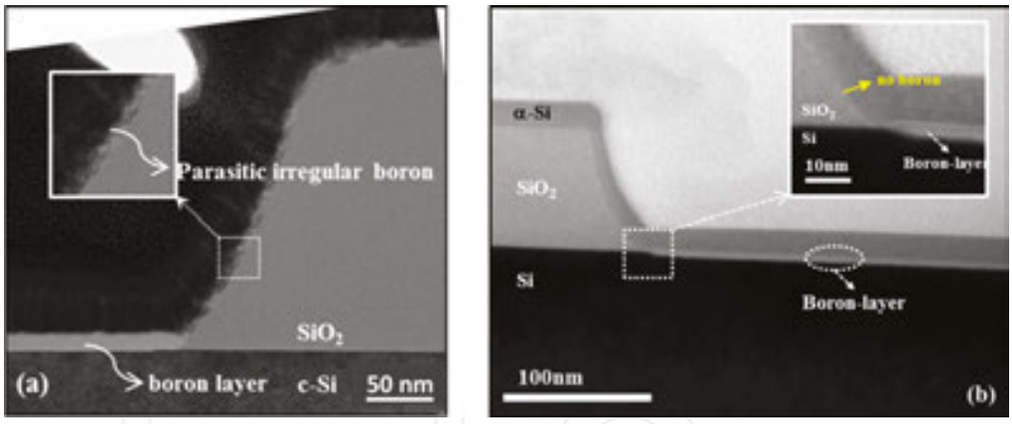

Figure 10. HRTEM images of flat/bevelled oxide surfaces of a small 40×40 μm²Si window with (a) LT and (b) HT boron layers [21, 22].

These parasitic boron depositions on the flat/bevelled oxide are unwanted and can cause problems in the subsequent processing steps. For example, the adhesion of plasma-enhanced chemical vapour deposition (PECVD) layers of TEOS-SiO_2 was seen to degrade. This is illustrated in the SEM images of **Figure 11**. Similar adhesion issues were also witnessed in the case of physical vapour deposited (PVD) Al deposition on these surfaces. Boron depositions at 500°C can be performed without any parasitic deposition over most oxide surfaces, even at micron-sized windows. However, still for some oxide qualities this kind of unwanted parasitic deposition was observed. An example is given in **Figure 12b** and **c**, where two different dyes with the same layout are shown with and without adhesion issues for subsequent PECVD TEOS and PVD Al layer depositions.

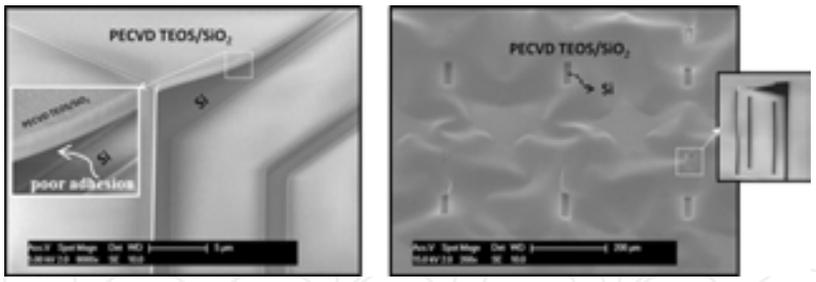

Figure 11. Examples of poor PECVD TEOS-SiO_2 adhesion as a result of parasitic boron deposition during LT deposition of boron on flat/bevelled oxide surfaces near micron-sized Si windows where the LOR is high [21].

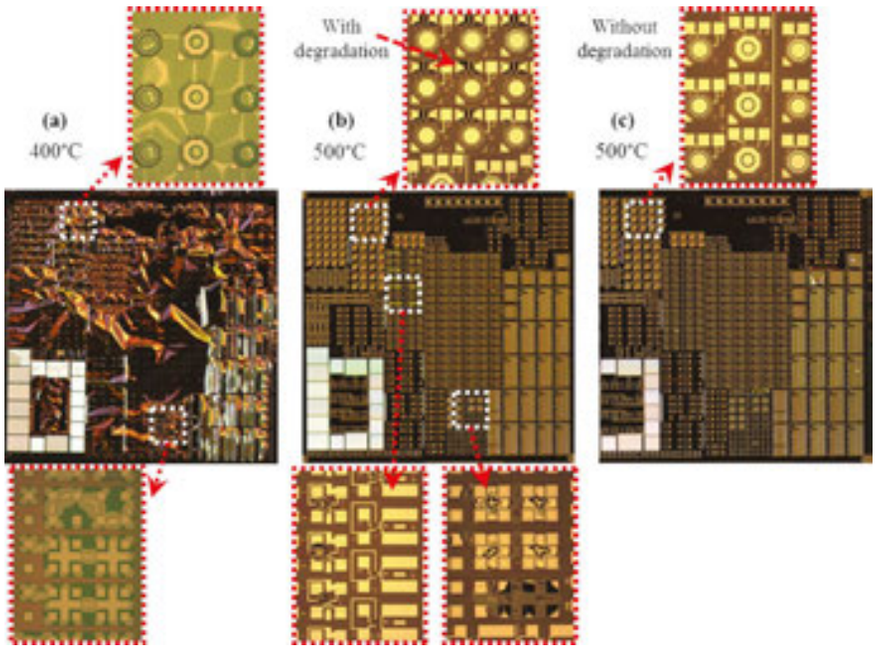

Figure 12. Examples of poor adhesion and layer delamination for the same layout. Die (a) shows PECVD TEOS deposited over 400°C boron. PVD Al was deposited after PECVD TEOS deposition over 500°C boron for two different dies on the same wafer. Die (b) displays the adhesion problems. However, die (c) does not display the same adhesion problems as die (b). The insets show the zoom-in for different structures with micron-sized openings [21].

3.4. Precautions to minimise the parasitic boron deposition at low temperatures

To minimise the undesirable parasitic boron deposition on the oxide, there are a few precautions that can be taken into account. Firstly, the chances of parasitic boron deposition can be reduced by using the higher quality oxide, which has a lower density of oxide surface-free sites and/or defects. Secondly, the global and local oxide coverage ratios can be optimised in the layout of the oxide mask to reduce the unnecessary boron atom accumulation over the oxide areas. Likewise, the deposition and process parameters, such as diborane partial pressure, gas flow and total deposition pressure, can be optimised to minimise the loading effects [15, 24]. These will otherwise also increase the accumulation of boron atoms over certain oxide areas, thus increasing the probability of parasitic boron deposition there. Also, we have found that

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this poor adhesion could depend on the ex/in situ treatments before the PECVD TEOS-SiO_2 or PVD Al layers are deposited. Furthermore, the adhesion of these extra layers after boron deposition is also influenced by the exact conditions on the surface. For example, a large amount of hydrogen resides on the surface just after boron deposition and is in general known to reduce adhesion. This H coverage can be reduced by carrying out the baking steps in air. An investigation of these extra treatments would have to be included in the process development when working with LT boron deposition.

By taking the aforementioned precautions into account, the LT boron deposition was successfully performed to create near-ideal LT PureB photodiodes with low, deep-junction-like saturation currents.

4. LT PureB UV photodiode fabrication

The post-metal LT boron deposition was successfully performed to create p^+n photodiodes with nm-thin, boron-only beam entrance windows and near-theoretical UV sensitivity with negligible optical and electrical degradation [25]. **Figure 13** shows the processing steps of the

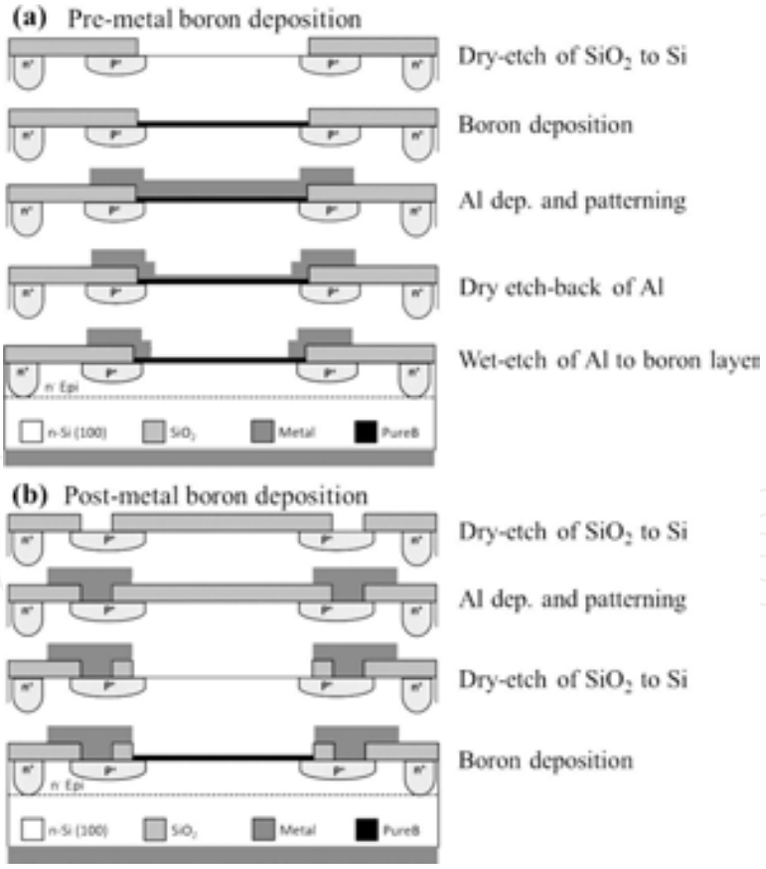

Figure 13. Processing steps of the fabricated photodiodes with boron-only beam entrance windows, for boron deposition both before (a) and after (b) metallisation [25].

fabricated photodiodes with boron-only beam entrance windows, for boron deposition both before and after metallisation.

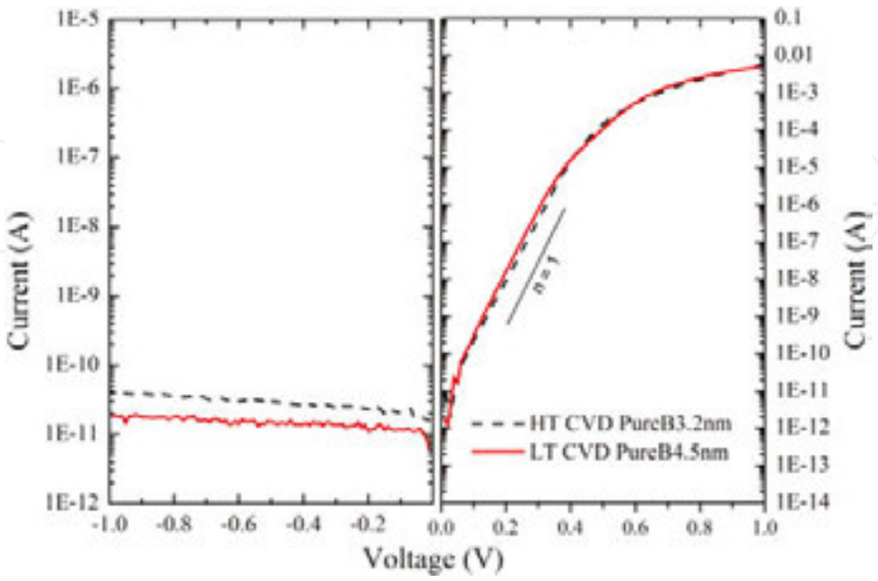

Figure 14. Measured I-V characteristics of both pre-metal HT and post-metal LT PureB photodiodes with an active area of 9.6×9.6 mm^2. Schematics of the fabricated photodiodes are shown in **Figure 13**. The boron layer thickness was measured by ellipsometry to be 3.2 and 4.5 nm for the HT and LT photodiodes, respectively [25].

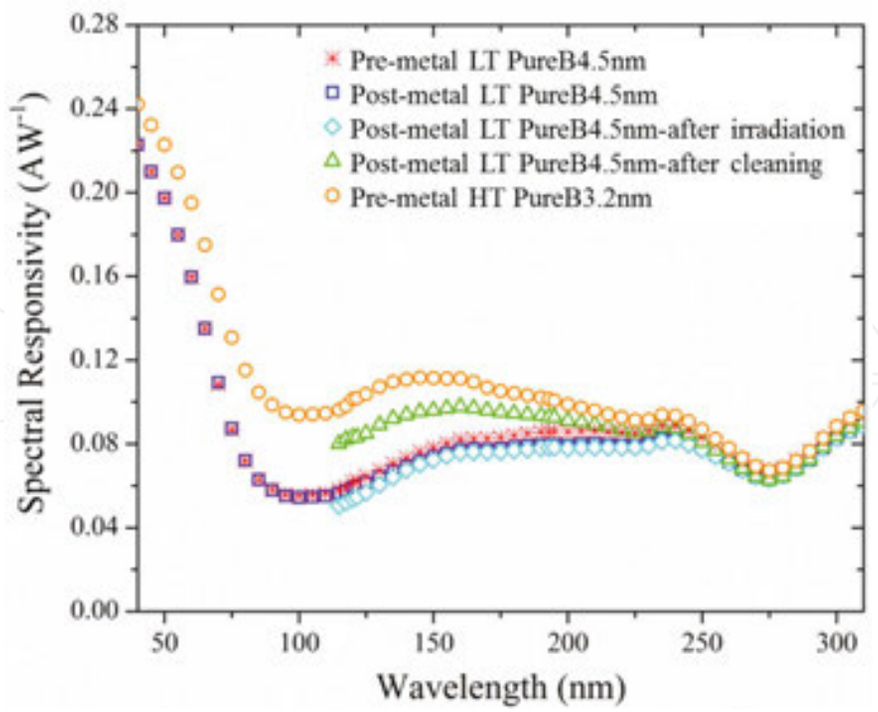

Figure 15. Measured VUV spectral responsivity as a function of wavelength for HT and LT PureB photodiodes (area: 9.6×9.6 mm^2) before and after high-level irradiation and after a final cleaning procedure [22].

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The I-V characteristics measured for both pre-metal HT and post-metal LT PureB photodiodes with an active area of 9.6×9.6 mm^2 are shown in **Figure 14**. The boron layer thickness was measured by ellipsometry to be 3.2 and 4.5 nm for the HT and LT photodiodes, respectively. As can be seen, low deep-junction-like saturation currents and near-ideal diode characteristics can be provided by LT boron deposition.

Figure 15 shows the measured responsivity in the VUV spectral range (120–400 nm) for both pre-metal and post-metal LT PureB photodiodes. As can be seen in this figure, the response for pre-metal photodiodes is slightly higher than that for post-metal ones. This could be explained by a small thinning of the boron layer due to the extra processing necessary to open the light entrance window (see **Figure 13**). The HT PureB device is also shown in **Figure 15** as a reference. As will be commented on subsequently, the rough LT boron surface proves to be much less chemically resilient than the smooth HT boron layers.

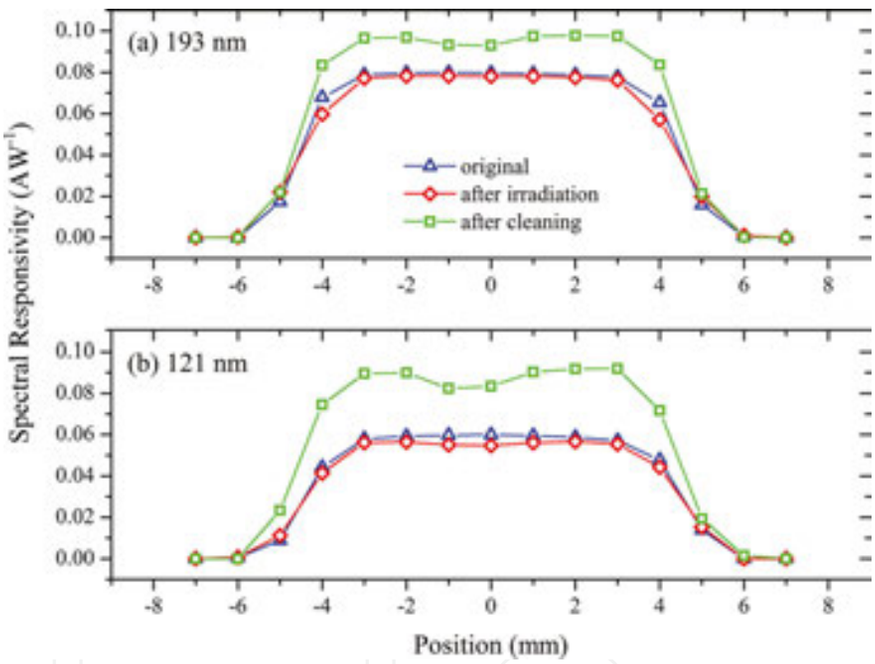

Figure 16. Measured responsivity across the surface in one direction of a 9.6×9.6 mm^2 LT PureB photodiode at wavelengths of 193 and 121 nm, before and after high-dose exposure, and after cleaning. The high-dose exposure was performed with a circular beam spot of ø1 mm with a radiant exposure of 37 J/cm^2 [22].

The optical stability of the post-metal LT PureB photodetector was measured by exposing the centre of the 10×10 mm^2 dies to high-dose VUV irradiation. The high-dose exposure was performed with a circular beam spot with a diameter of 1 mm, to a radiant exposure of 37 J/cm^2. The LT PureB photodiodes were found to be highly stable. To illustrate, the resulting responsivity at the centre of the post-metal LT PureB photodiode is included in **Figure 16**.

A slight dip in responsivity is visible after the 121-nm exposure. This is the result of the build-up of carbon contamination during exposure. To remove this layer, an ozone-cleaning procedure was performed. For HT devices, the cleaning procedure successfully removes the contamination, and the original high responsivity is regained [26]. By contrast, this treatment

cannot effectively remove the carbon contamination of the LT device, probably due to the rougher surface structure as shown in **Figure 13**. As can be seen, the rougher surface makes the carbon contamination removal more difficult than the smooth surface structures. Additionally, this rougher surface structure makes the silicon surface below the boron layer more susceptible to oxidation [27]. The higher responsivity after standard ozone-cleaning suggests that the boron layer is thinned considerably, as can be seen in **Figures 15** and **16**. On closer look at these figures, a reduced thinning can be clearly seen where the carbon contamination was present for both measurement wavelengths (i.e. in the middle of the active area). Therefore, although the as-deposited LT boron layer is optically robust, it is more vulnerable to carbon contamination due to its rougher surface compared to HT boron layer, as can be seen in **Figure 9**.

5. Summary

In this chapter, an analytical model is developed to describe the deposition kinetics and deposition chamber characteristics that determine the deposition rate over the wafer, which can be used as a pre-deposition prediction tool to improve the set-up and control of the final deposition. The model has been very useful both in the development of uniform boron layers with minimal pattern dependence and in the transferring of recipes from one reactor to the other.

A new technology for low-temperature (400°C) boron deposition is presented, which provides a smooth, uniform, closed boron layer. The temperature dependency of the boron deposition on patterned Si/SiO_2 surfaces in the temperature range of 400–700°C is investigated. Some selectivity issues that arise when the boron deposition temperature is reduced from 700°C to 400°C are discussed. Some provisions are recommended to minimise the undesirable boron deposition on the oxide. For boron deposition at 400°C, it is necessary to start the deposition in a nitrogen environment to facilitate the first monolayer deposition, and then switch to a hydrogen environment to make the surface smoother and to maintain the boron coverage over the entire silicon opening.

The LT PureB technology is then successfully employed to create near-ideal LT PureB photodiodes with nm-thin, boron-only beam entrance windows and a near-theoretical sensitivity for irradiation with either VUV/DUV/EUV light down to a wavelength of 10 nm. Very low dark current of only 15 pA at -1 V bias voltage was measured for post-metal LT PureB photodiodes with an anode area of 9.6×9.6 mm^2, which we relate to the fact that no post-PureB processing was performed.

It is believed that at temperatures of 400°C and lower, no silicon doping is possible during the boron deposition. Yet, the LT boron layers provide a structure with excellent p-n junction-like I-V characteristics. Based on this observation, we make the assumption that during the damage-free LT boron deposition, which is most likely a result of a chemical reaction, a kind of effective "hole" layer is built between the boron and silicon. This interface "hole" layer

creates an electric field that repels the injected minority carriers (electrons) away from the interface.

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