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Chapter 6

Novel Developments and Challenges for the SiC Power Devices

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Abstract

Silicon Carbide (SiC) is believed to be a revolutionary semiconductor material for power devices of the future; many SiC power devices have emerged as superior alternative power switch technology, especially in harsh environments with high temperature or high electric field. In this chapter, the challenges and recent developments of SiC power devices are discussed. The first part is focused on SiC power diodes including SiC Schottky barrier diode (SBD), SiC PiN diodes (PiN,) SiC junction/Schottky diodes (JBS), then SiC UMOSFETs, DMOSFETs and several MESFETs are introduced, and the third part is about SiC bipolar devices such as BJT and IGBT. Finally, the challenges during the development of SiC power devices, especially about its material growth and packaging are discussed.

Keywords: Silicon Carbide, Power Device, Diode, MOSFETs, MESFETs

1. Introduction

The first-generation and second-generation semiconductor materials are represented by silicon (Si) and gallium arsenide (GaAs), respectively. Wide band gap materials, such as silicon carbide (SiC) and gallium nitride (GaN), are known as the third generation semiconductor materials. SiC was discovered in 1824 by Berzelius during his diamond synthesis experiment. The first use of SiC was as an abrasive. This was followed by electronic applications. In the beginning of the 20th century, SiC was used as a detector in the first radios, and then became

popular since 1907 when Henry Joseph Round produced the first LED by applying voltage to a SiC crystal and observing yellow, green, and orange emissions at the cathode. This attracted much of the electronic researchers' attention and about half a century ago, the potential of SiC in the semiconductor industry was recognized. Compared with Si, the most widely-used semiconductor material, SiC has many remarkable electronic properties including wide band gap, large critical electric field, high thermal conductivity, high electron saturation velocity, chemical inertness, and radiation hardness [1-3]. These excellent properties make SiC very well-suited for high-voltage, high-power, and high-temperature applications.

SiC power devices began to be developed during the 1970s. Based on the efforts of many researchers, great improvement had been achieved in its crystal quality and fabrication technology during the 1980s, then various kinds of SiC devices were developed, and their performance has rapidly improved.

Nowadays, the primary theoretical stage of SiC power devices had been completed. The commercial availability stage is developing rapidly; process technology, such as single-crystal substrate and device fabrication processes, has had great progress. Since 2001, Infineon Corporation started to supply SiC Schottky diodes. Now SiC diodes, MOSFETs, JFTs, BJTs, and other SiC three-terminal devices are available, CREE, Toshiba, STMicroelectronics and other companies have the ability to supply SiC power devices.

However, the main obstacles for the development of SiC-based devices are the quality and costs of SiC materials compared with its Si-based counterparts. With the recent progress in the process of SiC epitaxial materials, it is feasible to obtain high-quality 4H-SiC substrates and epilayers, and thus achieve excellent power performances for SiC power devices. For instance, 100-mm 4H-SiC substrates and epilayers are readily available for manufacturing power devices. Since more and more researchers and companies are paying attention to SiC materials, a massive drop in costs is forthcoming and affordable costs can be expected in the near future; which, in turn, will promote the development of SiC power devices.

2. Silicon carbide diode

Power diodes are the key components in modern power applications. The classical rectification function was upgraded by high demands of turn-on and turn-off speeds. In order to fabricate SiC power devices, ohmic contacts play a very important role in the signal transfer between the semiconductor and the external circuitry. A large number of ohmic contacts materials have been investigated during the last decades, both in terms of structural characterization and electrical performance. For ohmic contacts on the n-type SiC material, the most promising metal is nickel (Ni). It has been demonstrated that Ni films annealed in the range of 900-1000ºC can form good ohmic contacts on n-type SiCs with a specific contact resistance of $1\times10^{-6}\ \Omega\cdot cm^2$ [4]. For the p-type materials, due to the higher Schottky barrier, ohmic contact formation is even more difficult than n-type materials. Much research has been focused on aluminum/titanium (Al/Ti) contacts, which give a specific contact resistance of about $10^{-5}\Omega\cdot cm^2$ [5].

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2.1. Schottky Barrier Diode (SBD)

As a unipolar device, SBD has zero reverse recovery current. Figure 1 shows a general structure of SiC SBD; it is formed by an electrically nonlinear contact between a metal and a semiconductor bulk region. SBD fabricated by SiC offers a new degree in the design of power circuits, which has been commercially available since 2001. The most remarkable advantage of SiC SBD is the continuing increase in blocking voltage and conduction current ratings, which have been increased from the initial 300 V, 10 A and 600 V, 6 A [6] to the current 600 V, 20 A [7]. Furthermore, it is expected that SBD can be applied with a blocking voltage up to 2,000 V (as merged solutions also up to 3 kV) [8]. 4H-SiC with field plate terminal technology had been reported for the first time with a breakdown voltage of 1,750 V [9]. It is even foreseen that this type of diode may replace Si bipolar diodes in medium-power motor drive modules. Due to the absence of reverse recovery charge in SBD, it has an extremely fast turn-on performance, which is well suited for high-speed switching applications and for drastically reducing the dynamic losses for typical circuits. The high thermal conductivity of SiC is also a great advantage for SiC SBD in comparison with Si and GaAs diodes since it allows the SBD to operate at higher current density ratings with smaller size cooling systems. However, its reverse leakage current is large, especially at high temperatures, due to its lower built-in potential barrier.

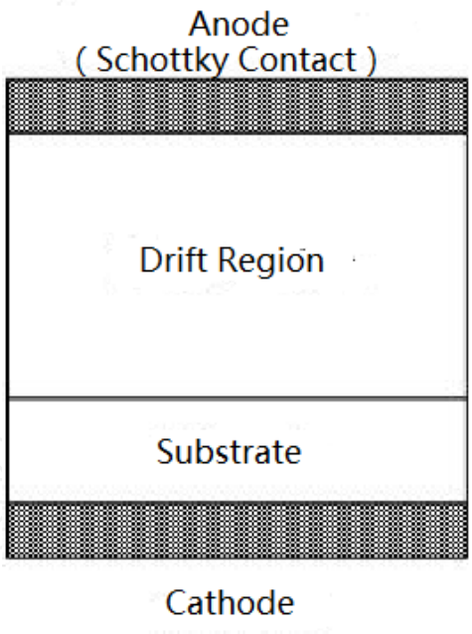

Figure 1. Conventional structure of SiC SBD.

2.2. Silicon carbide PiN diodes (PiN)

Owing to the absence of conductivity modulation effects, the drift region resistance of SBD increases so fast with the rise of breakdown voltage, so the maximum breakdown voltage of SBD cannot compete with PiN diodes due to the unacceptably large ON-state resistance.

Figure 2 shows a general structure of a SiC PiN diode, it consists of a highly doped n-type substrate, a lightly doped n-type epitaxial layer with specified thickness, and a highly doped p-type region for the anode. The advantage of the SiC PiN diode is its low leakage current and low ON-state voltage drop in high current conduction due to minority carrier injection in the epitaxial drift region resulting in conductivity modulation. However, conductivity modulation causes significant reverse recovery current during switching, which is undesirable because it causes additional turn-on loss in the active switch. Since SiC PiN diodes are gaining more and more attention due to its higher breakdown voltage and smaller size and weight, its switching speed has been greatly improved. Recently, Johji Nishio et al. have fabricated the mesa SiC PiN diodes, which have a blocking voltage of 10.2 kV [10]. In 2007, Cree Company has reported a 8.7×8.7 mm^2 SiC PiN diodes with the blocking voltage of 10 kV, as is shown in Figure 3 [11]. However, it has been reported that high power SiC PiN diodes exhibit an increase in the static forward voltage drop after exposing it to long-term operation during the test [12]. Various physical characterization techniques have shown that structural defects would be created in the epilayers during the operation. Encouragingly, Cree researchers have reported [13] that a process modification, which suppresses this degradation phenomenon, has been found but they have not released any details. Tsunenobu Kimoto et al. have reported 15 kV SiC PiN diodes with various junction terminal technologies [14]. In Ref. [15], 4H-SiC PiN had been applied in high temperature and high power circumstance with the breakdown voltage of 1,000 V.

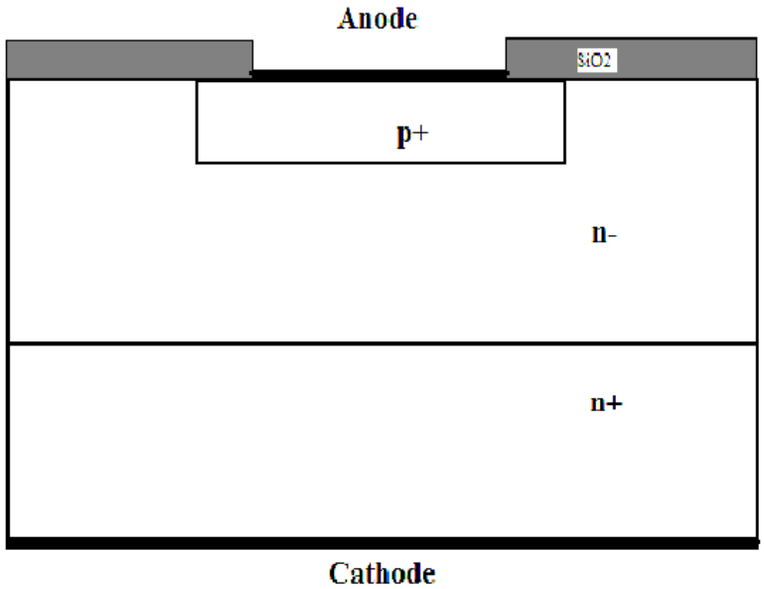

Figure 2. Conventional structure of SiC PiN.

2.3. Silicon carbide junction/schottky diodes (JBS)

Schottky rectifiers are expected to dominate in power devices with a blocking voltage below 3 kV. However, the reverse leakage current of SBD is generally excessive, particularly at high

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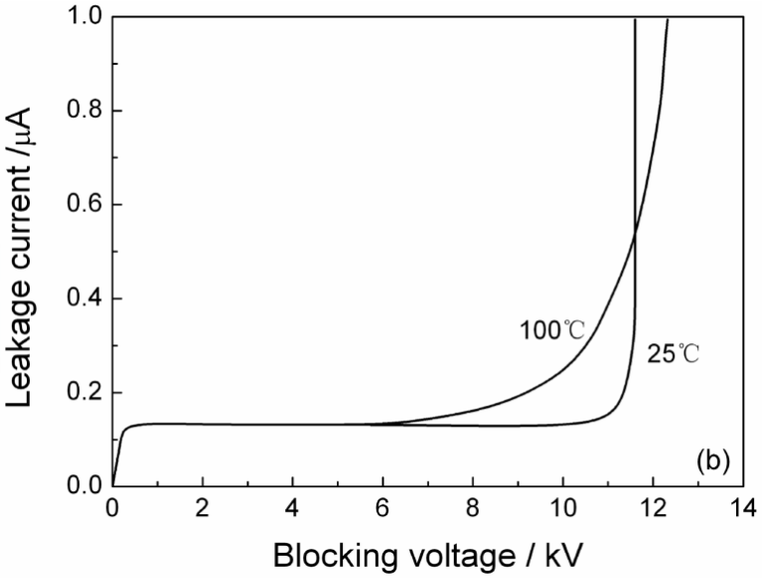


Figure 3. Blocking voltages characteristics of 10 kV SiC PiN diodes [11].

temperatures, due to lower Schottky barrier at high reverse voltage. The second-generation SiC diodes usually combine the attractive benefits of low ON-state voltage drop of a Schottky contact and the high blocking voltage of PiN diodes. These diodes have Schottky-like ON-state and switching behavior and PiN-like OFF-state characteristics at the same time. The basic JBS diode is fabricated by merging a Schottky diode and PiN diode structure [16]. Figure 4 shows a general structure of the SiC JBS; it consists of interleaved Schottky and p+ doped regions.The adjacent pn junction is used to suppress the rise of the electric field at the Schottky junction. When operating at voltages lower than the turn-on voltage of the pn junction, JBS exhibits faster switching speed than PiN diodes due to the absence of minority carrier injection. In recent time, Cree has manufactured a series of JBS with voltage ratings of 300, 600, and 1200 V and single-die current ratings from 1 to 10 Amps. In conclusion, the ON-state and switching characteristics of JBS are similar to Schottky diodes. The blocking characteristic is optimized due to the merged PiN diode structure compared with the SiC SBD.

3. Silicon carbide unipolar devices

3.1. Silicon carbide MOSFETs

Metal oxide semiconductor field effect transistors (MOSFETs) have been of interest since Si devices have become the most successful devices. Due to the excellent material properties of SiC, SiC power MOSFETs can operate at higher switching frequency and operating temperatures compared with conventional Si MOSFETs. It has been expected to be the next-generation switching device to replace conventional Si power devices in many applications. The first SiC power MOSFET was demonstrated in 1994 in the form of a vertical trench gate structure (UMOSFET) [17]. The reported device had a breakdown voltage of 150 V and specific on-

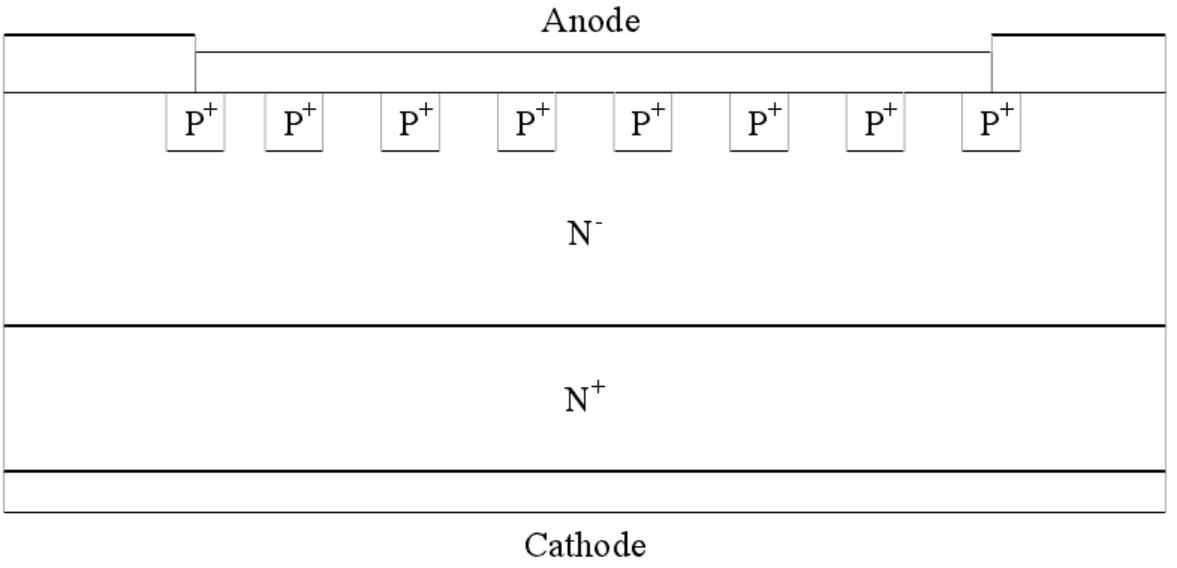


Figure 4. Conventional structure of SiC JBS.

resistance of 3.3 mΩ·cm^2. The breakdown voltage of the device was restricted by the high electric field in the gate oxide at the trench corner. To avoid the high electric field in a UMOSFET, a SiC planar gate MOSFET with a p-base formed by a double implantation MOS process was fabricated (DMOSFET), this 6H-SiC DMOSFET has a breakdown voltage of 760 V based on a 10μm-thick and 6.5×10^{15} cm^3-doped n-type drift layer. [18]. Figure 5 is the schematic diagram of the structure of the typical UMOSFET (UMOS) and DMOSFET (DMOS).

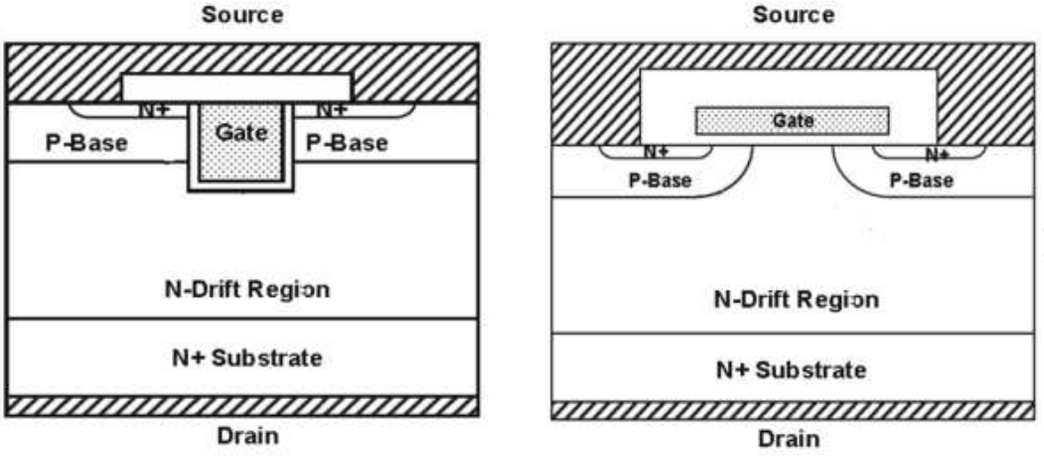


Figure 5. Schematic diagram of SiC (a) UMOS and (b) DMOS.

Later on, a 10 kV, 123 mΩ·cm^2 4H-SiC power DMOSFET was reported [19]. The effective channel carrier mobility is only 22 cm^2/V·s. However, the very low inversion channel electron mobility in 4H-SiC has prevented the fabrication of the low-resistance MOSFETs for many

years. Besides, electron mobility in the channel has been proved to be low when measured on p-implanted regions due to the implantation damage. SiC has a higher density of dangling Si and C bonds at the SiC/SiO_2 interface due to its higher surface density of atoms per unit area compared with Si. Therefore, various intrinsic defects not related to dopants or impurities can be observed at the SiC/SiO_2 interface, these defects appeared in the energy gap of SiC as traps for electrons leading to the low channel mobility in 4H-SiC. This made the reduction of interface state density at the SiO_2/SiC boundary play a critical role in increasing channel mobility and improving high temperature performance, as well as the reliability of power SiC MOSFETs or IGBTs. In the past few decades, a lot of efforts have been devoted to developing SiC power devices, and great progress has been achieved. With the advanced process technology, there are two approaches that are effective in improving the quality of the metal-oxide-semiconductor interface. One is using nitrogen during post-oxidation annealing and the other is selecting specific crystal faces for the formation of the MOS channel. Now, the SiC MOSFETs with peak mobility of 140 $cm^2/V \cdot s$ and 216 $cm^2/V \cdot s$ in the channel have been fabricated. However, interface state densities are still two orders of magnitude higher than those devices achieved by using Si MOS technology, which has been adopted by Cree to fabricate high-current (2 A), large-area (2 mm^2) lateral MOSFETs. The University of Tokyo has reported a lateral DMOSFET (LDMOSFET) with its blocking voltage and specific on-resistance of 1.5 kV and 54 $m\Omega \cdot cm^2$, respectively [20]. A breakdown voltage of 3,520 V was achieved for the 4H-SiC lateral MOSFETs with specific on-resistance of 600 $m\Omega \cdot cm^2$ [21]. This is the best result for SiC LDMOSFET.

Since 2012, Takuji Hosoi reported an AlON high-k gate dielectric technology implemented into both planar and trench SiC MOSFETs. The high-k gate dielectric technology can efficiently reduce the gate leakage and its higher dielectric breakdown field would be beneficial in improving the devices' reliability and channel carrier mobility. In 2013, a 1,600 V/150 A 4H-SiC DMOSFETs are presented by Lin Cheng. The SiC DMOSFET with smaller chip size shows superior static and dynamic performance over the commercially available 1,200 V/200 A trench gate Si IGBT from 25°C up to 200°C. In 2014, Ryota Nakamura presented a 1,200 V 4H-SiC MOSFETs with double-trench structure SiC MOSFETs. The trench structure can reduce the on-resistance by about 50% from 25℃ to 150℃.

3.2. Silicon carbide MESFETs

For the SiC power metal semiconductor field effect transistors (MESFETs), the breakdown voltage is a very important parameter that allows the power devices to achieve a specific power density and power conversion. Figure 6 is the schematic diagram of the conventional SiC MESFET. Prior research has proposed many techniques to improve the breakdown voltage [22, 23]. In order to optimize the surface electric field and improve the breakdown voltage, new technologies had been proposed, which includes the REBULF (reduced bulk field) [24] and complete 3D Reduced SURface Field (RESURF) [25]. The high breakdown had been obtained on the ultra-thin epitaxial layer with the REBULF technology. It can be ensured that these new technologies can be transplanted directly onto SiC power MESFETs. Thus, several new SiC power MESFETs had been designed to optimize the characteristic of the breakdown voltage, specific on-resistance, frequency, and transconductance.

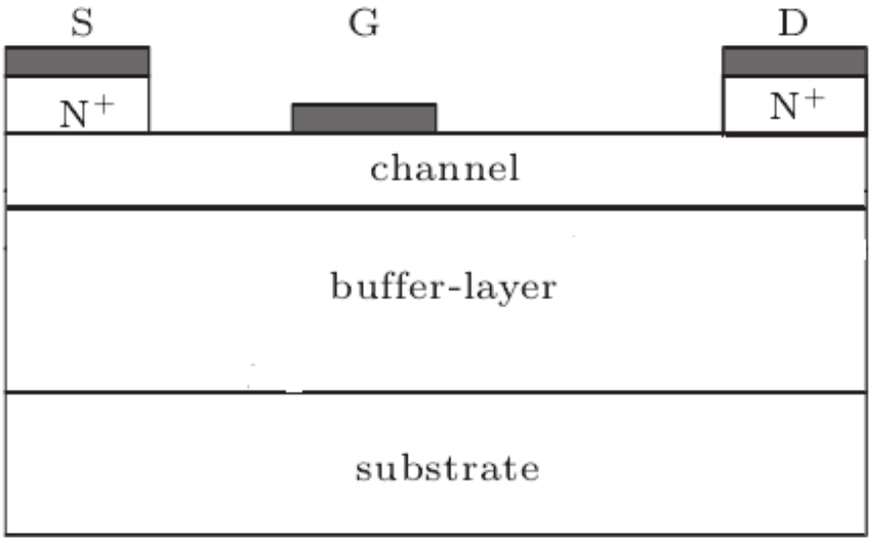


Figure 6. Schematic diagram of the conventional SiC MESFET structure.

Figure 7 is the schematic diagram of the structure of the Buffer-Gate SiC MESFETs structure [26]. Compared with the conventional 4H-SiC MESFETs (Figure 6), a low-doped, gate-buffer layer is introduced between the gate and channel layer. In Buffer-Gate 4H-SiC MESFETs, the gate length is 0.7 μm. Meanwhile, the thickness and doping concentration for the channel layer are 0.26 μm and 1.7×10^{17} cm^{-3}; between the gate and channel is the gate-buffer layer that has a thickness of 0.15 μm and doping concentration of 1×10^{15} cm^{-3}.

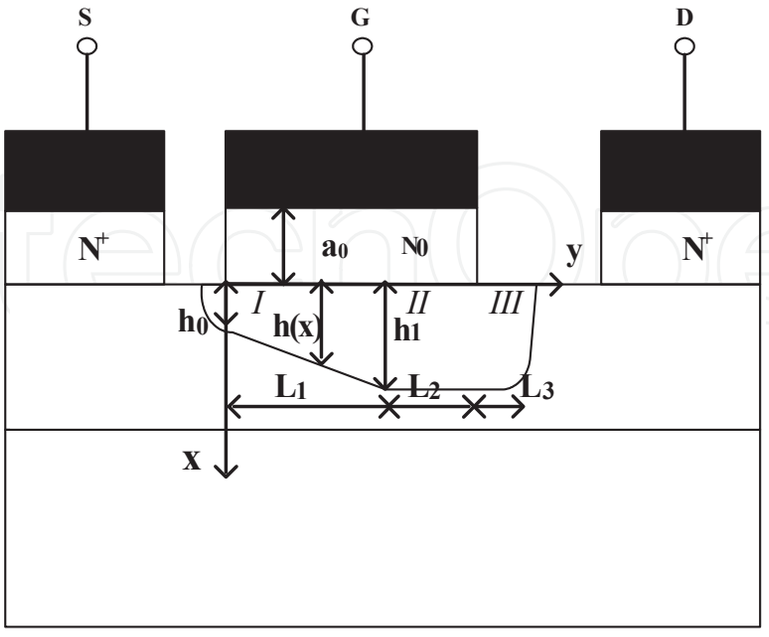


Figure 7. Schematic diagram of the structure of the Buffer-Gate SiC MESFET in saturation mode operation.

The channel current in the channel for the structure above can be expressed by (1):

$$I_C = qWn(\mathrm{x})\mu(\mathrm{E})\mathrm{E}(\mathrm{x})\left[a - h(\mathrm{x})\right] \tag{1}$$

Where q is the magnitude of the electronic charge, W is the channel width, a is the channel layer thickness, $E(x)$ is the lateral electric field strength, and $n(x)$ is the electron concentration of the channel. $h(x)$ is the thickness of the depletion layer in the channel layer and obtained by solving the 1-D Poisson's equation (2):

$$h(\mathrm{x}) = a_0\left(1 - \frac{N_0}{N_D} + \frac{V(\mathrm{x}) + V_G + V_{bi}}{\frac{qN_D}{2\varepsilon}a_0^2}\right) - a_0 \tag{2}$$

Where N_0 is the uniform doping concentration of the gate-buffer layer, which is smaller than N_D, a_0 is the gate-buffer layer thickness, and ε is the dielectric constant. $V(x)$ is the potential at the point x away from the source, V_G is the gate bias and V_{bi} the build-in voltage. To solve the 2-D Poisson's equation:

$$u_1(\mathrm{V_G}, \mathrm{V_D}) = \frac{h_1}{a} = \sqrt{\left(1 - \frac{N_0}{N_D}\right)\frac{a_0^2}{a^2} + \frac{V(\mathrm{L_1}) + V_G + V_{bi}}{V_p}} - \frac{a_0}{a} \tag{3}$$

$$V(\mathrm{L}+\mathrm{L_3})\text{-}V(\mathrm{L_1}) = \left(\frac{2(au_1 + a_0)}{\pi} + \frac{\mathrm{L_3}}{3}\right)E_s\sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\exp\left(\frac{-\pi \mathrm{L_3}}{2(au_1 + a_0)}\right) + \\ + \frac{E_s}{3}\left(2\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) + 1\right) \tag{4}$$

$$\mathrm{L_3}^2\left[\frac{qN_D a u_1}{\varepsilon} - E_s\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) + \frac{E_s}{\eta}\sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\left(1 + \tan\left(\frac{\pi a_0}{2(au_1 + a_0)}\right)\right)\right) \\ = (au_1)^2 E_s\left[\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) - 1 - \sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\exp\left(\frac{-\pi \mathrm{L_3}}{2(au_1 + a_0)}\right)\right. \tag{5}$$

$$\eta = \tan\left(\frac{\pi a_0}{2(au_1 + a_0)}\right)\cos\left(\frac{\pi a u_1}{2(au_1 + a_0)}\right) + \sin\left(\frac{\pi a u_1}{2(au_1 + a_0)}\right) \tag{6}$$

$$V\left(L+L_3\right)=V_D-I_C R_D \tag{7}$$

From equations (1-7), the drain current can be achieved when the structure parameters (L, W, a, a_0, N_D, N_0) and bias voltage (V_G,V_D) are given.

ISE TCAD is used in the simulation. To obtain accurate results, several basic physical models such as band gap and electron affinity models, generation-recombination models, quantization models, and incomplete ionization models are utilized, which precisely describe the material properties. Figure 8 (a) shows the effect of the gate-buffer layer on the current in the channel. It reveals that the drain current increased as the gate-buffer layer gets thicker at first, but if the thickness of the gate-buffer layer gets thicker than 0.3 μm, this correlation doesn't exist, the drain current is saturated. And the heavier the doping concentration is the bigger the drain-saturated current is. This is because the decrease of the depletion layer thickness in the channel decreased with the increase of the doping concentration and thickness of the gate-buffer layer dcrease so the channel width would increase, which makes the drain current get bigger. Figure 8 (b) shows the breakdown characteristics for the two structures. It can be seen that the breakdown voltage (V_b) of the Buffer-Gate SiC MESFETs is significantly increased, compared with that of the conventional structure (a_0=0μm, shown in Figure 5). This is because the breakdown happens at the gate corner near to the drain side due to the electric field crowding here for both structures. Different from the conventional 4H-SiC MESFETs, Buffer-Gate SiC MESFETs have an inserted lower-doped gate-buffer layer that makes the surface electric field more uniform, so the electric field peak at the gate corner is also lowered. Figure 8 (c) shows the electric field distribution. The mechanism for the suppression of the electric field at the gate corner in the Buffer-Gate SiC MESFETs is similar to the lightly-doped drain (LDD) in the MOSFETs [27].

The schematic diagram of the GDSE (Gate-Drain Surface Epitaxial layer) MESFETs is shown in Figure 9 [28]. Compared with the conventional 4H-SiC MESFETs, a low-doped p-type surface epitaxial layer is introduced between the gate and drain, which has a doping concentration two orders lower than that of the channel layer. As the layer has been introduced, firstly, the electric field peak at the gate corner will be reduced by the build-in potential in the p-n junction between the p-type epitaxial layer and n-type channel layer or n^+ cap layer, which makes the electric field distribution more uniform. Secondly, due to the much lower doping concentration of the p-type epitaxial layer, most of the depletion region in the p-n junction lies in the p-type region. Therefore, the gate-drain p-type epitaxial layer has little bad effect on the current density.

As mentioned above, the two-dimensional simulator ISE TCAD is used, to precisely describe the surface trap effect along the SiC/SiO_2 interfaces. The density and capture cross section of the near interface trap(NIT) are set to 5.3×10^{12} cm^{-2} and 1×10^{-19} cm^2, while the density and capture cross section of the deep interface trap(DIT) are set to 1.2×10^{13} cm^{-2} and 1.4×10^{-15} cm^2 [29, 30]. Schottky barrier tunneling (SBT) and initial trap populating (ITP) are taken into account for transient investigation. Similar studies concerning these mechanisms can be found elsewhere and the accuracy of relevant models has been verified [31].

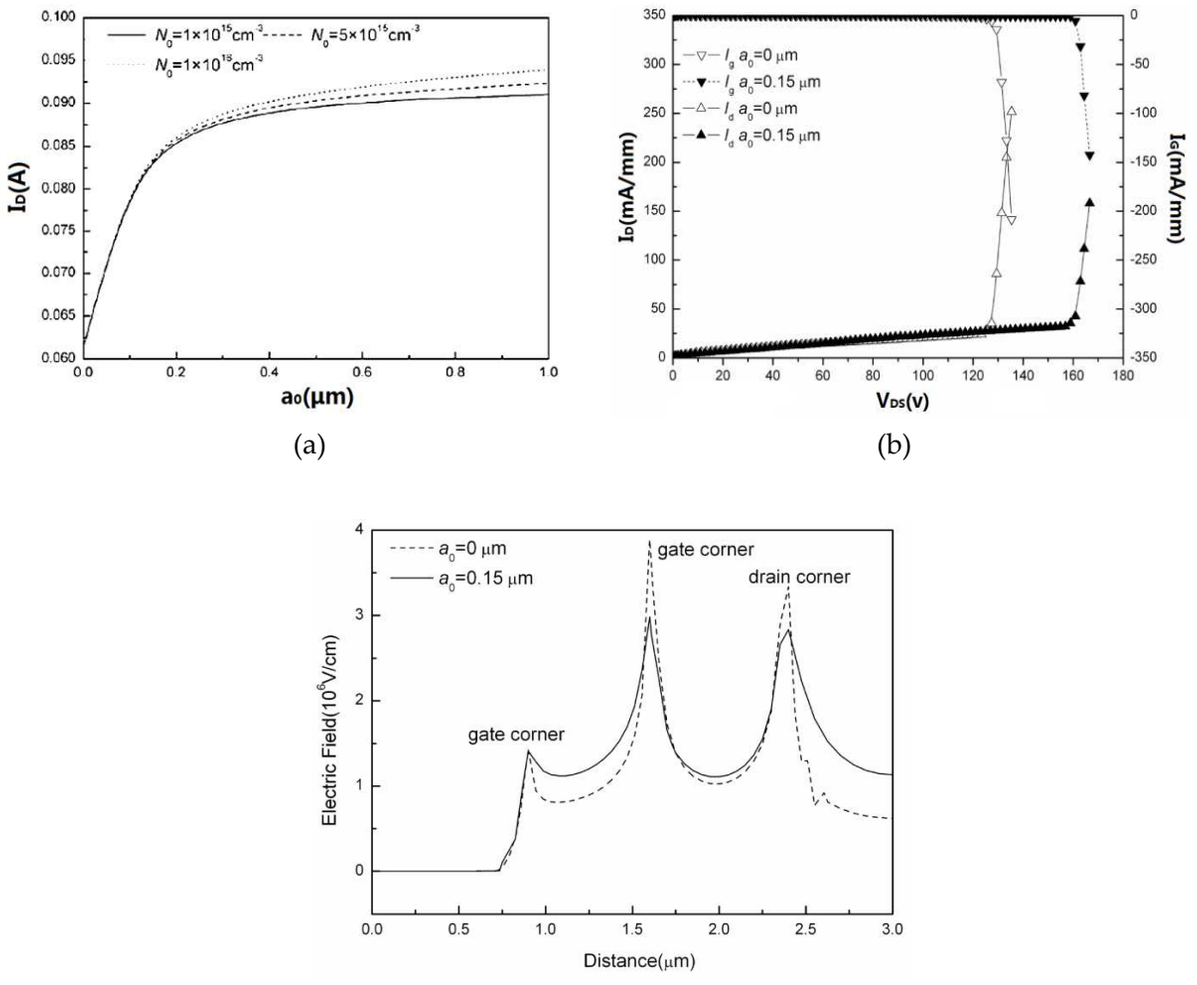


Figure 8. (a) Dependence of the drain current on the gate-buffer layer for N_0=1×10^{15} cm^{-3} N_0=5×10^{15} cm^{-3} and N_0=1×10^{16} cm^{-3}.V_{GS}=0 V, V_{DS}=5 V. (b) The simulated breakdown characteristics for a_0=0 μm (open) and a_0=0.15 μm (filled). (c) The distribution of the surface electric field for a_0=0 μm (dash) and a_0=0.15 μm (solid).

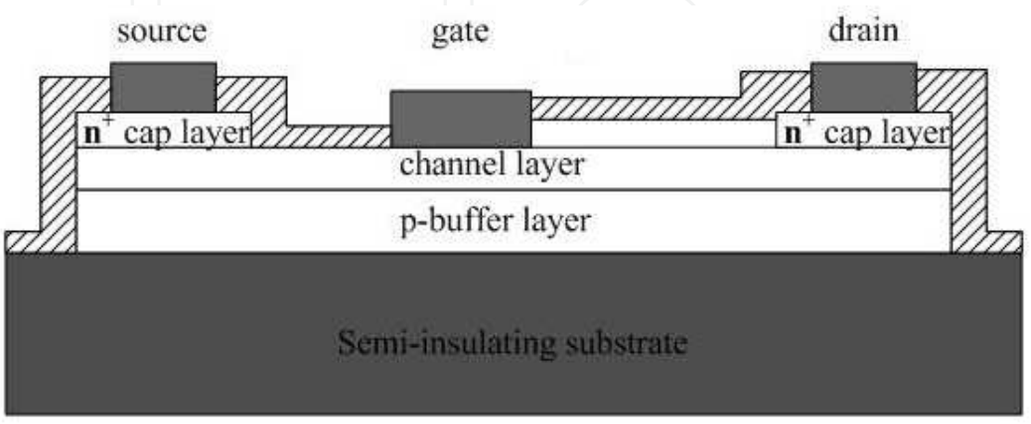
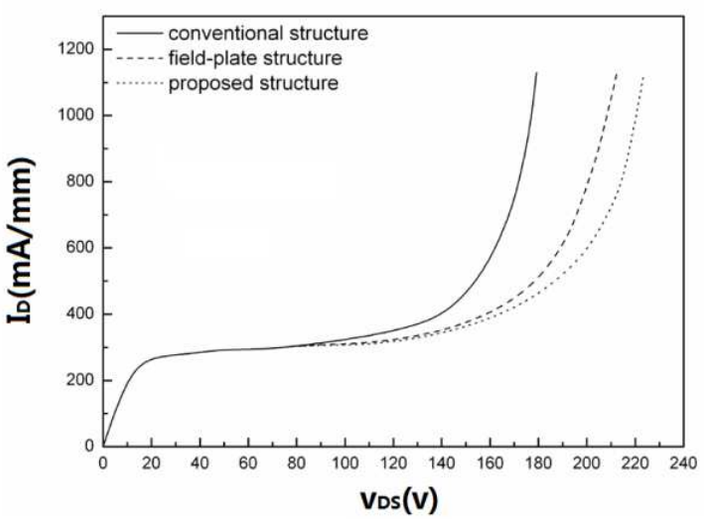
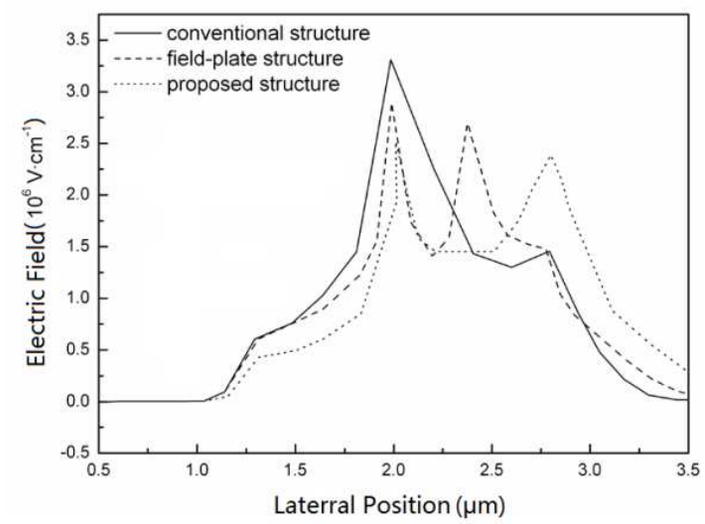


Figure 9. The schematic diagram of MESFETs with gate-drain surface epi-layer [28].

The introduced p-type spacer layer has a thickness of 0.1 μm and a doping concentration of 3×10^{15} cm^{-3}, the thickness and doping concentration of the n-type channel used as the conductive channel for device operation is 0.22 μm and 3×10^{17} cm^{-3}. And the buffer layer is 0.6 μm thick with a doping concentration of 5×10^{15} cm^{-3}. The breakdown characteristics and surface electric field distribution are shown in Figure 10. It had been shown that the breakdown voltage of the GDSE structure is the largest one for the three structures in Figure 10 (a) owing to the inserted lower-doped p-type epitaxial layer the electric field peak at the gate corner is significantly lowered (i.e., the surface electric field is more uniform), so the breakdown voltage for the GDSE MESFETs increased as is shown in Figure 10 (b).



(a)



(b)

Figure 10. Comparison of the (a) breakdown voltage and the (b) surface electric field for the conventional, field-plated, and the GDSE structure.

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The schematic diagram of the L-gate 4H-SiC MESFETs with partial p-type spacer is shown in Figure 11. Compared with the conventional 4H-SiC MESFETs, the L-gate and partial p-type spacer are introduced. The L-gate structure has lower and upper gates that effectively controls a thinner and a thicker part of the channel, respectively. It can decrease the gate capacitance and reduce the depletion layer under the gate, which makes the conduct channel under the L-gate wider, so the saturation drain current increases effectively. Since the p-n junction formed between the p-spacer and the n-channel also leads a distinct reduction of the gate-drain capacitance, the proposed structure has a significant improvement of the DC and RF performances compared with conventional SiC MESFETs.

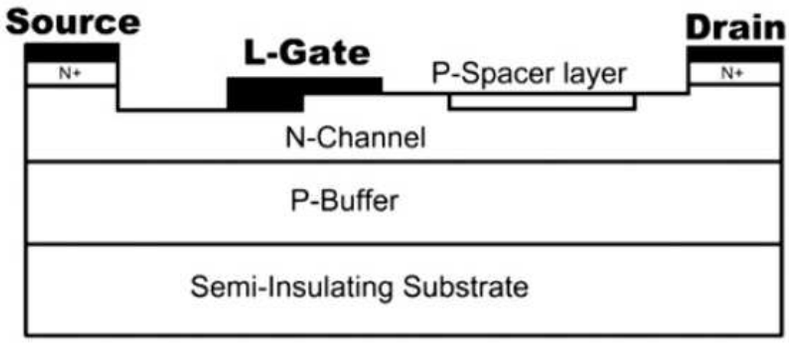

Figure 11. The schematic diagram of the L-gate 4H-SiC MESFETs with partial p-type spacer.

Figure 12 (a) shows the simulated output characteristics of C-MESFET, L-gate-MESFET, and LP-MESFET under the gate bias (V_{GS}) vary from 0 V to -12 V with a step of 4 V. It can be seen that due to the thicker gate-drain drift region and wider channel region outside the L-gate, the LP-MESFET has a higher saturation drain current (I_{Dsat}) than that of conventional ones at V_{GS}=0 V. It also should be noted that the p-n junction formed between the p-spacer and n-channel that leads to a reduction in effective thickness of the gate-drain drift region slightly decreases the saturated drain current of the LP-MESFET comparing with that of the L-gate-MESFET.

Figure 12 (b) shows the three-terminal breakdown characteristics for 4H-SiC C-MESFET, L-gate-MESFET, and LP-MESFET simulated with an applied V_{GS}=V_T. The drain current (I_D) and the gate leakage current (I_G) with respect to V_{DS} are displayed for the three MESFETs. It can be seen that the drain current will increase with the gate leakage current increasing, this illustrates that the breakdown of 4H-SiC MESFETs at the applied V_{GS} occurs at the gate-drain drift region, which is because the electric field for all the structures crowding at the gate corner near the drain. Therefore, owing to the extension of gate metal on the surface acted as a field plate resulting in a gradual field distribution, the high electric field peak at the bottom edge of gate toward the drain side is suppressed, the MESFETs with a L-Gate has an improvement of the breakdown voltages shown in Figure 11 (a) [32]. It can be seen that the breakdown voltages are 250 V for the C-MESFET, 360 V for the L-gate-MESFET, and 340 V for the proposed structure LP-MESFET, which is 36% higher than that of C-MESFET. The maximum output power density Pmax for the 4H-SiCC-MESFET, L-gate-MESFET, and LP-MESFET at V_{GS}=4 V and V_{DS}=40 V is

4.2 W/mm, 9.1 W/mm, and 8.2W/mm, respectively. Output power density of the LP-MESFET structure is about 95% larger than that of the C-MESFET structure. [33].

Figure 12 (c) shows the simulated C_{GD} versus frequency at V_{DS}=40 V and V_{GS}=-5 V. It can be seen that the C_{GD} of the LP-MESFET structure is smaller than that of the C-MESFET structure and the L-gate-MESFET structure. As is known to all, the C_{GD} consists of depletion layer capacitance and drift region diffuse capacitance. From the device structure, we can see that the partial p-type spacer has a distance from the gate edge towards the drain, so the decrease of C_{GD} is not derived from the reducing depletion layer extension to drain. That means the reducing C_{GD} is mainly attributed to the decreased gate-drain drift region diffused capacitance brought by the partial p-type spacer.

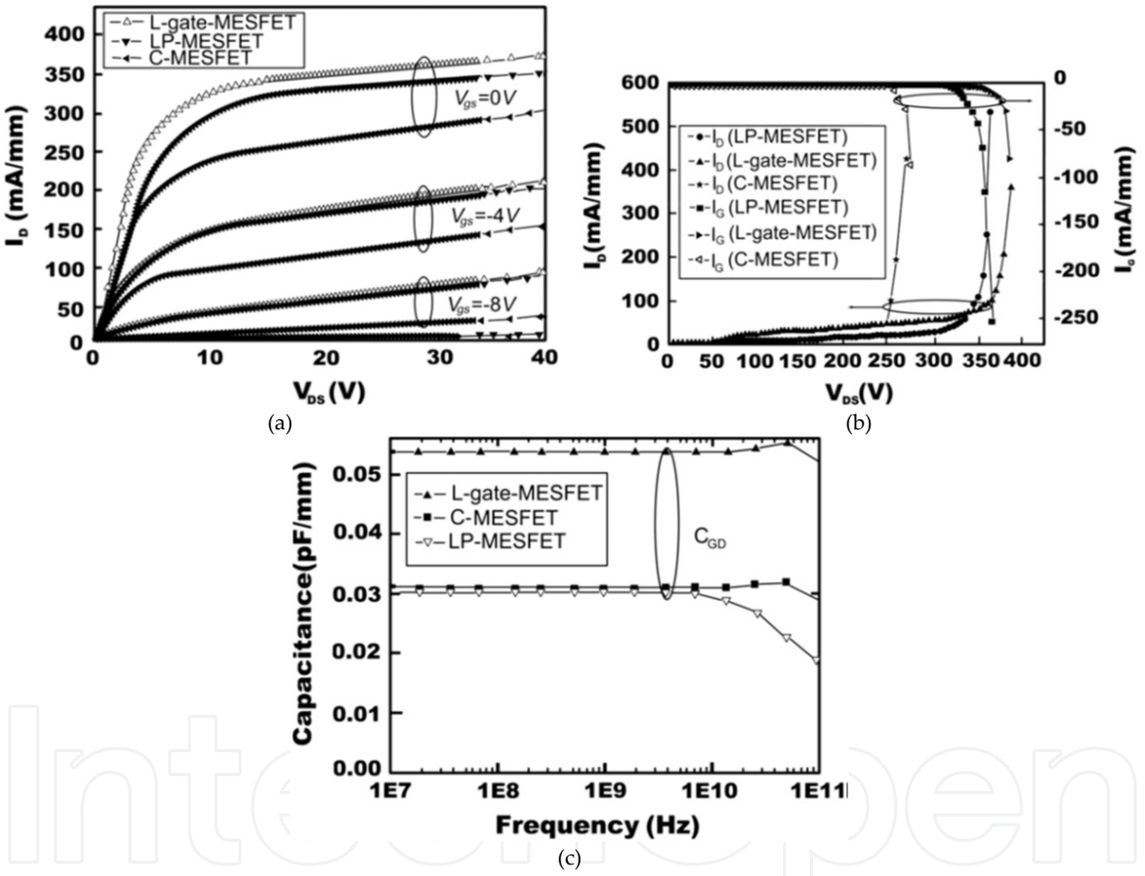

Figure 12. (a) The simulated I_D-V_{DS} characteristics of different structures. (b) Simulated three-terminal breakdown characteristics for 4H-SiC C-MESFET, L-gate-MESFET. and LP-MESFET. (c) Dependences of the simulated drain-gate capacitance (C_{GD}) on the frequency of the three structures under DC bias conditions of V_{DS}=40 V and V_{GS}=-5 V.

4. Silicon carbide bipolar devices

There has been great progress in SiC bipolar power devices such as BJT and IGBT. SiC BJT exhibits 20~50 times lower than Si BJT in switching losses and ON-state voltage. In Si BJT, the

second breakdown is widespread, which significantly affects the devices' performance. However, it is negligible in SiC BJT since the critical current density is 100 times lower than that of Si BJT. Moreover, the base region and collector region are allowed to be fabricated very thin so as to improve the current gain and switching speed due to the large critical electric field of SiC material. The Cree company has reported another 4H-SiC BJT with its current gain of 44, blocking voltage of 3.2 kV, and specific on-resistance of 8.1 $m\Omega \cdot cm^2$ [34]. The driving circuit of SiC BJT is complex compared with that of a MOSFET. However, its manufacturing process is simpler than that of a JFET. In the area of SiC IGBT, Q. Zhang has reported a UMOSFET 4H-SiC IGBT with a blocking voltage and specific on-resistance of 10 kV and 175 $m\Omega \cdot cm^2$ at 25°C [35]. In 2007, Purdue University fabricated a p-IGBT with a p-region width of 175 μm, as high as 20 kV in blocking voltage [36]. This IGBT can provide approximately twice the ON-state current as MOSFETs at 177°C, which is superior to the IGBT based on the Si. In the same year, Cree reported a SiC n-IGBT with a blocking voltage of 12 kV, and its switching characteristic is shown in Figure 13 in comparison with that of Si-IGBT [37].

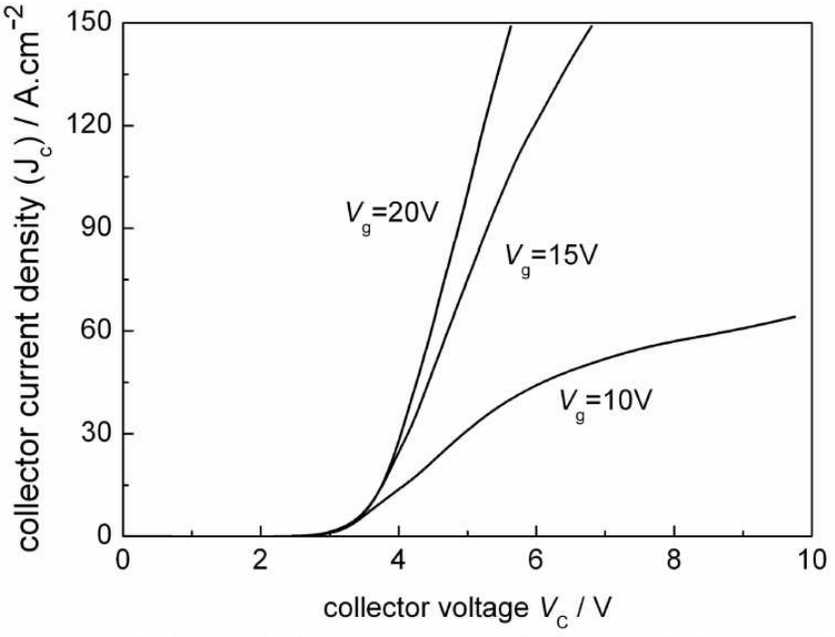

Figure 13. 12kV 4H-SiC N-IGBT ON-state characteristics [35].

Since key technologies, such as low mobility in the inverse channel layer and reliability of the gate oxide layer with the high electric field, have not been overcome, SiC MESFETs (or JFETs) and BJTs may be the only widespread SiC devices commercially. At present, process technologies, such as injection, oxidation, and etching processes, should be improved in order to optimize device structures. In the long run, researchers should focus their attentions on the process theory and technology of gate oxidation for fabricating superior MOSFETs and IGBTs.

5. Forthcoming challenges for silicon carbide power devices

5.1. Defects for silicon carbide materials

Reducing and eliminating the defects density in the SiC wafer is a knotty task, which is the main reason that is limiting the wafer dimension. There has been significant development in reducing and eliminating defects density. Cree has been supplying 4-inch SiC wafers with zero micro-pipe since 2007. Now, the research of defects is focusing on the effects of dislocation, such as screw dislocation, basal plane dislocations, edge dislocation, and other defects on the characteristics of the devices.

5.2. Challenges for silicon carbide power devices

This technical review is one of the series of reports on semiconductor power devices. Three IETE articles have been reported on the application of electric field modulation to silicon and silicon-on-insulator power devices [36,37]. There are two bottleneck techniques in SiC MOSFETs that need to be broken down, the low electron mobility in the inversion channel layer and gate oxide reliability with high temperature or high electric field. The recent reported electron mobility is 30-250 $cm^2/V \cdot s$, which does not manifest the advantage of the SiC MOSFET. Therefore, special gate oxidation technologies are needed to eliminate the SiC/SiO_2 interface defects and increase the mobility of the electron in the inversion layer, such as the post-oxidation annealing in the H_2 environment, and gate oxidation or annealing in NO or N_2O environment. It is unknown what causes the current gain instability; one possible reason may be the stacking fault in the epitaxial base region. The new SiC power devices can be designed by applying the electric field modulation effect. Electric field modulation had been proposed by the authors for the first time [38-40]. Several new structures for the silicon power devices and AlGaN/GaN HEMTs had been reported, which can be used to design new SiC power devices [41-47].

The packaging of the SiC power device is also a pressing problem. The packaging reliability for SiC devices will be a key factor affecting the performance of the circuits once the material and process challenges are overcome. Packaging reliability is also important when the devices operate at high temperatures (≥ 200°C) or the coolant temperature require the operation temperature should above today's limits of ~150°C. For example, the automotive motor drives using engine coolant, oil and gas drilling and extraction, avionics power supplies, space power supplies, and military applications. It's important to increase the power handling capability to reduce the expensive chip area and cooling cost. Thus, new package materials for high temperature application are necessary.

As the great reduction of switching energy is attained by very fast switching and when SiC power devices are applied in the fast switching area, the internal electromagnetic parasitic issues between the device and package should be taken into account. The advanced power module architectures are very important.

During the application of SiC power devices, people should think about the high electric field issue. Due to the high device internal electric field, the field stress in the passivation layer and

at the chip surfaces is so high that the average electric field for the chip/gel interface at the terminal edge is around 3 times higher than the SiC diode. With such high surface field strengths, any contamination in the form of particles or mobile ions may lead to possible electrochemical driven corrosion processes; any material defect in the passivation layers and any delamination/insufficient adhesion of encapsulation may become extremely critical. This makes the advanced insulation technology of great importance.

6. Conclusion

In conclusion, SBD has an extremely fast turn-on performance due to the absence of reverse recovery charge, which is well suited for high-speed switching applications, drastically reducing the dynamic losses of typical circuits, and yet minimizing the size of cooling systems. The SiC PiN diodes have the characteristics of low gate leakage current and high breakdown voltage, and thus can be used as switches in high voltage and low frequency circumstances. The JBS shows the ON-state and switching characteristics similar to Schottky diodes and blocking characteristics similar to PiN diodes. MESFETs have superior RF performance compared to JFETs due to the reduced gate capacitance and higher transconductance. SiC BJT exhibits much lower switching losses and ON-state voltage than Si BJT. Unless the electron mobility in the inverse channel layer and reliability of the gate oxidation layer are broken through, SiC MOSFETs will not be commercially widespread.

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