Chapter 11

Open-End Winding Induction Motor Drive Based on Indirect Matrix Converter

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Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/61157

Abstract

Open-end winding induction machines fed from two standard two-level voltage source inverters (VSI) provide an attractive arrangement for AC drives. An alternative approach is to use a dual output indirect matrix converter (IMC). It is well known that IMC provides fully bidirectional power flow operation, with small input size filter requirements. Whilst a standard IMC consists of an AC–DC matrix converter input stage followed by a single VSI output stage, it is possible to replicate the VSI to produce multiple outputs. In this chapter, an open-end winding induction machine fed by an IMC with two output stages is presented. Different modulation strategies for the power converter are analyzed and discussed.

Keywords: Open-end winding, Electrical drive, Matrix converter, Pulse width modulation (PWM)

1. Introduction

An open-end winding induction machine, fed by two 2-level VSIs, offers several advantages when compared to a standard wye or delta connected induction machine drive. The main features of an open-end winding induction machine drive can be summarized as [1, 2]: equal power input from both sides of each winding, thus each VSI is rated at half the machine power rating; each phase stator current can be controlled independently; possibility to have twice the effective switching frequency (depending on the modulation strategy); extensibility to more

phases, therefore multiphase induction machines can be considered if current reduction is required; possibility of reducing common-mode voltage; and certain degree of fault tolerance, as there is voltage space vector redundancy.

However, an open-end winding induction machine drive can have some drawbacks, such as [1]: possibility of zero sequence current flowing in the machine because of the occurrence of zero sequence voltage; increased conduction losses; more complex power converter requirements, i.e., more power devices, circuit gate drives, etc.

To supply energy to an open-end winding machine, different power converter topologies have been developed; for instance, [3–6] propose an open-end winding induction machine drive based on two 2-level VSIs fed from isolated DC sources. This topology has the advantage of avoiding the circulation of zero sequence current; however, two isolation transformers are needed. On the other hand, [7–11] present a topology based on two 2-level VSIs fed by a single DC source. In this case, a zero sequence current could circulate in the machine windings (depending on the modulation strategy used), but just one transformer is needed, reducing the volume and cost of the drive.

Multilevel topologies for open-end winding AC drives are presented in [12–16] where different voltage levels can be achieved in the machine phase windings with certain power converter configurations, then reducing the output voltage distortion but increasing the system cost and complexity.

In the past decades, significant research effort has been focused on direct frequency changing power converters, such as the matrix converter (MC) [17] or the indirect matrix converter [18]. It is known that these power converter topologies offer a suitable solution for direct AC–AC conversion, achieving sinusoidal input and output currents, bidirectional power flow capability and controllable input power factor, without using bulky energy storage elements [18]. Matrix converters have been utilized to supply open-end winding AC machines such as reported in [19–21].

In this chapter, the application of an IMC with two output stages to supply energy to an open-end winding induction machine is described [22–24]. For evaluation purposes, simulations and experimental results are presented.

2. Power converter topologies for open-end winding induction machine drives

An open-end winding induction machine drive can be supplied by different configurations of power converters. Some of the most common topologies will be reviewed in this chapter.

2.1. Two 2-level voltage source inverters fed by isolated DC sources

This is the basic power converter for open-end winding AC drives. The circuit configuration is shown in Figure 1 where a standard two-level VSI is connected at each side of the machine stator winding [3]. The VSIs are supplied by isolated DC power sources.

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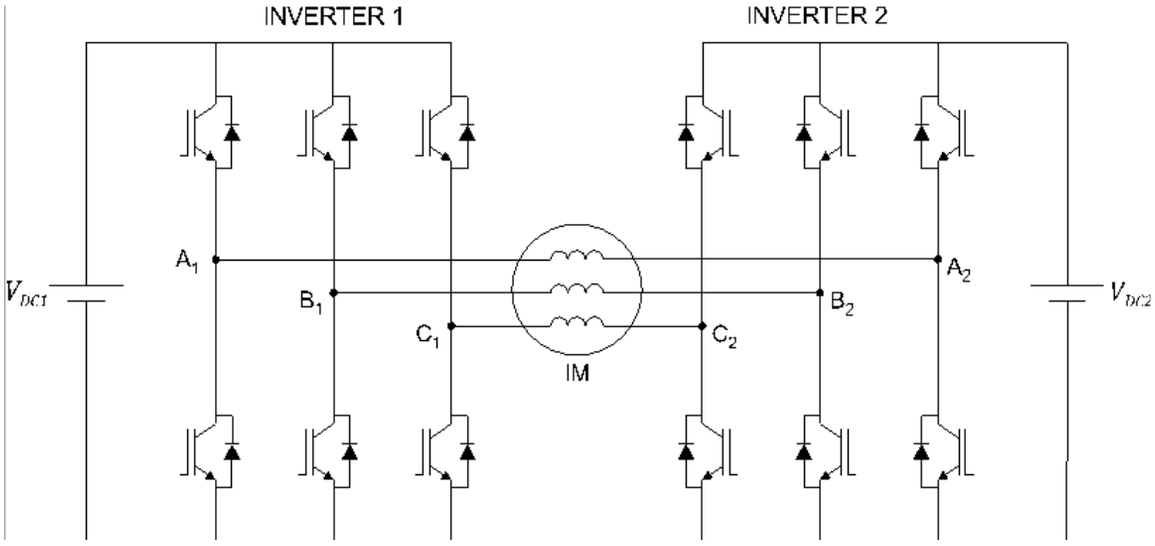

Figure 1. Two 2-level VSIs fed by isolated DC sources for an open-end winding AC machine drive.

The voltage vectors for inverter 1 are shown in Table 1; the same space vectors are valid for inverter 2, but with superscript 2. As each VSI can produce eight voltage space vector locations independent of the other, there are 64 voltage vector combinations of the full converter, resulting in a vector locus similar to a three-level neutral point clamped (NPC) inverter [6].

States of inverter 1 $[S_{A1}S_{B1}S_{C1}]$			
V_1^1=[1 0 0]	V_2^1=[1 1 0]	V_3^1=[0 1 0]	V_7^1=[1 1 1]
V_4^1=[0 1 1]	V_5^1=[0 0 1]	V_6^1=[1 0 1]	V_8^1=[0 0 0]

Table 1. Switching states of the individual inverters

Let $V_{ij}=[V_i^1 V_j^2]$ with $i,\ j=1...8$ be the phase voltage vector combination of the dual-inverter output. A representation of the vector locations is shown in Figure 2 [6].

2.2. Two 2-level voltage source inverters fed by a single DC source

This topology is basically the same described in Section 2.1, but now just one DC supply is considered for the drive, as shown in Figure 3. The disadvantage of this converter is that zero sequence current could circulate in the machine windings because of the generation of output zero sequence voltage; however, this issue can be addressed with an appropriate modulation strategy for the inverters [7].

2.3. Multilevel topologies

Several multilevel power converters have been developed for open-end winding induction motor drives. For example, Figure 4a shows a three-level inverter [12] and Figure 4b shows a

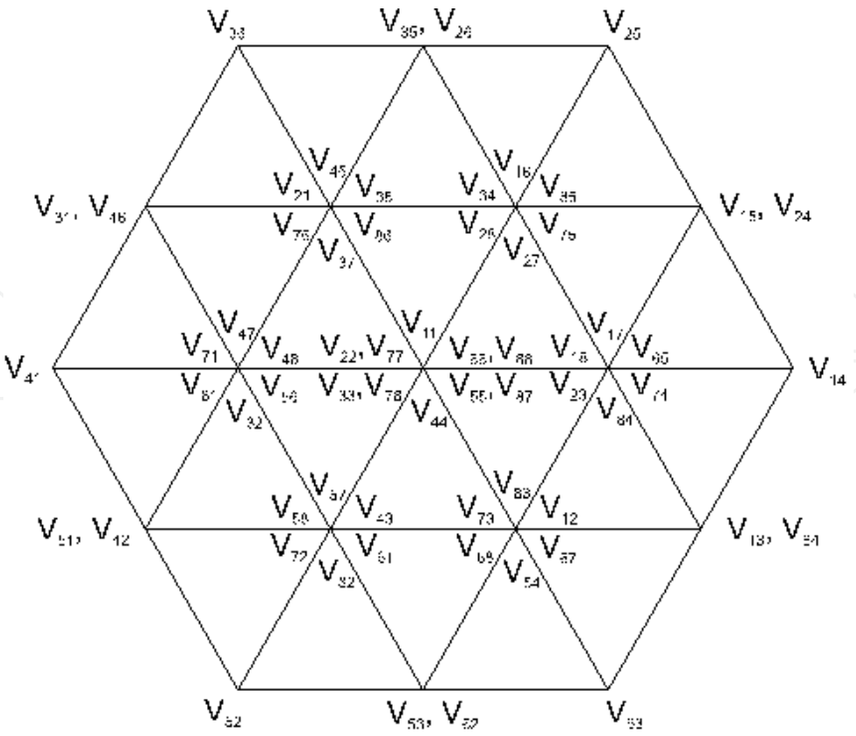

Figure 2. Space vector locations of the dual-inverter scheme.

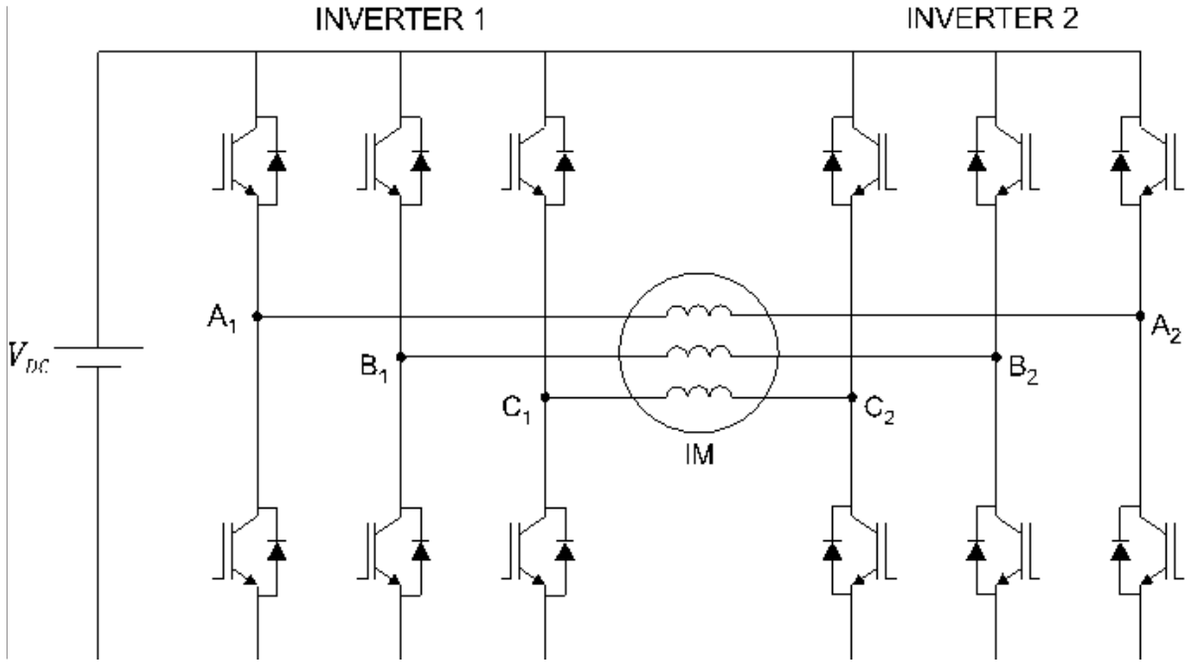

Figure 3. Two 2-level VSIs fed by a single DC source for an open-end winding AC machine drive.

five-level inverter [16]. The main advantage of the multilevel topologies is that the machine phase voltage presents lower voltage distortion, increasing the performance of the drive; but on the other hand, the complexity and cost of the system are also increased.

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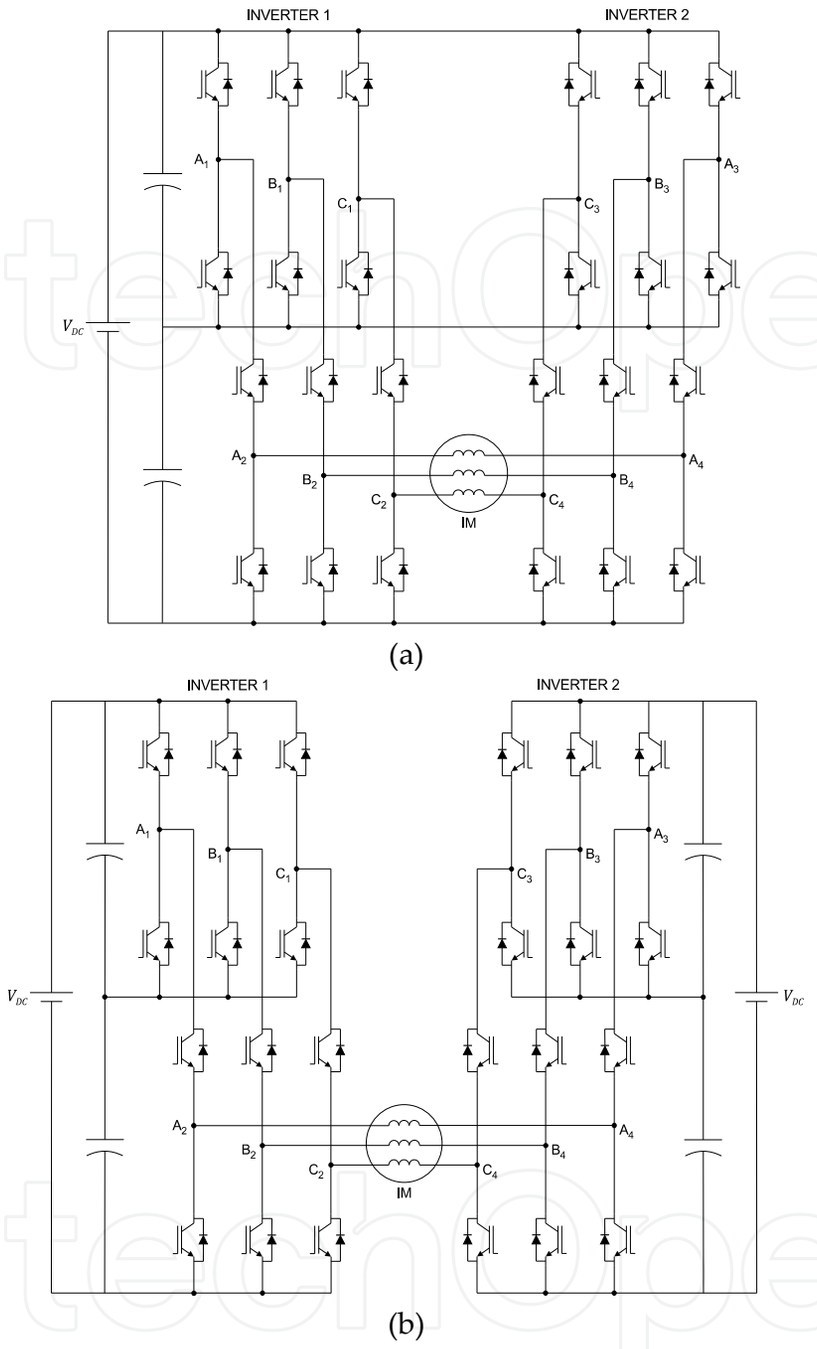

Figure 4. (a) Three-level inverter and (b) five-level inverter for open-end winding AC machine drives.

2.4. Direct power converters

Modern direct power converters consider matrix converter and indirect matrix converters. A matrix converter [17] is a direct frequency converter consisting of nine bidirectional switches (three switches per phase) allowing to connect any of the output terminals to any of the input voltages. For an open-end winding induction motor drive, two MCs are required, connected

in the arrangement shown in Figure 5. The main features of a matrix converter are: bidirectional power flow capability, sinusoidal input and output currents without bulky energy storage elements, and controllable input power factor. For a standard matrix converter, a total of 36 IGBTs and diodes are required in this topology.

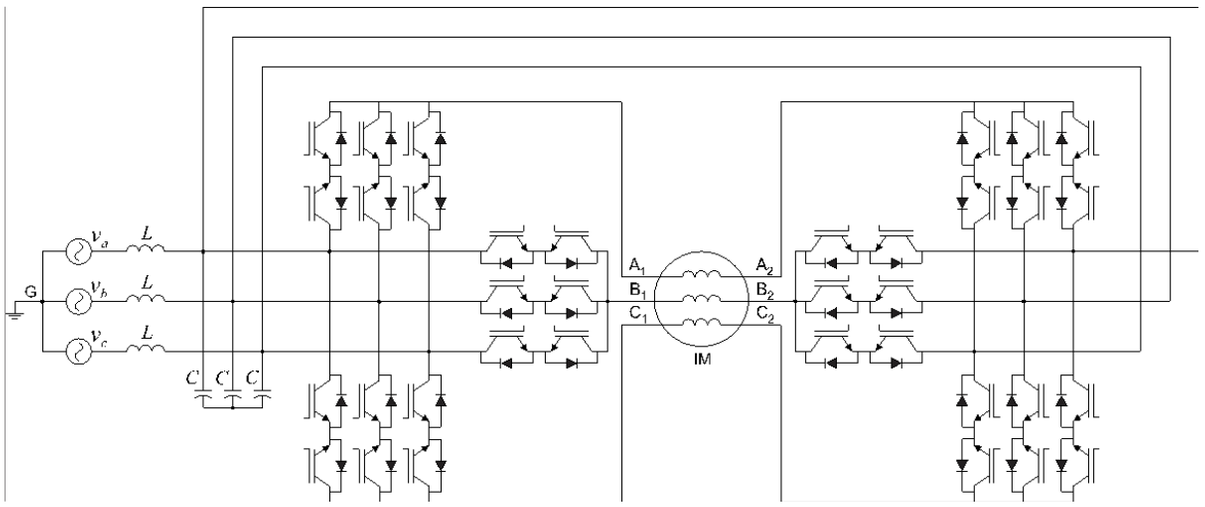

Figure 5. Open-end winding induction motor drive based on matrix converters.

An indirect matrix converter [18] is also a direct frequency converter having the same features of an MC, but now a DC stage is clearly identified in the topology. The IMC consists of an input rectifier, an AC–DC matrix converter, built of six bidirectional switches; this rectifier produces the DC voltage to supply the converter output stage which is a standard two-level VSI. To supply an open-end winding AC machine, two output inverters are required as can be seen in Figure 6. Considering the six bidirectional switches of the input stage and the two output stages, a total of 24 discrete IGBTs and diodes are required in this topology.

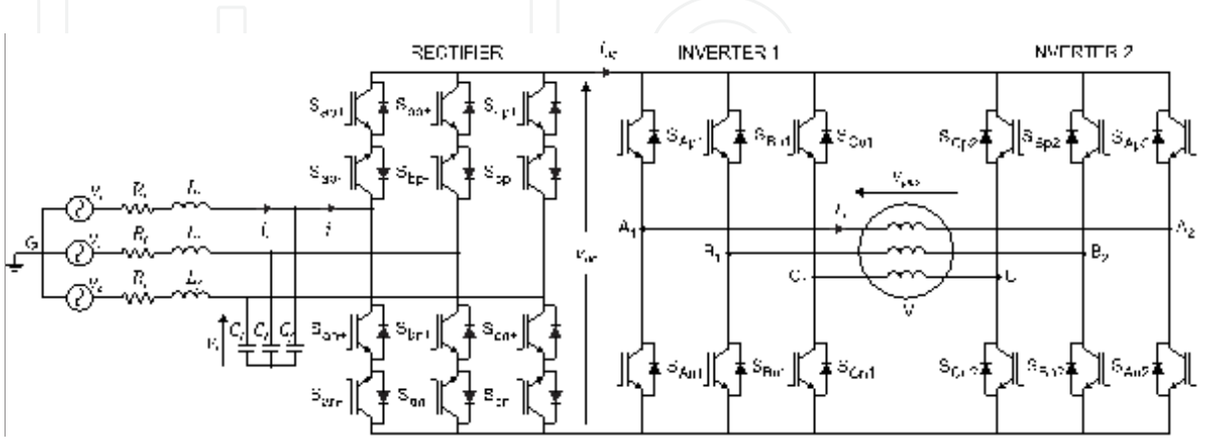

Figure 6. Open-end winding induction motor drive based on indirect matrix converter.

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3. Model of the open-end winding induction motor drive based on IMC

The complete drive of Figure 6 can be modeled by state equations which describe the dynamic behavior of the system. The effects of power devices dead-times on zero sequence voltages are neglected. All the equations derived below are written in fixed *abc* coordinates.

The differential equations for the input side are:

$$\boldsymbol{v_s} = R_f \boldsymbol{i_s} + L_f \frac{d\boldsymbol{i_s}}{dt} + \boldsymbol{v_i} \tag{1}$$

$$\boldsymbol{i_s} = C_f \frac{d\boldsymbol{v_i}}{dt} + \boldsymbol{i_i} \tag{2}$$

where

$$\boldsymbol{v_s} = \begin{bmatrix} v_{sa} & v_{sb} & v_{sc} \end{bmatrix}^T, \boldsymbol{i_s} = \begin{bmatrix} i_{sa} & i_{sb} & i_{sc} \end{bmatrix}^T \tag{3}$$

$$\boldsymbol{v_i} = \begin{bmatrix} v_{ia} & v_{ib} & v_{ic} \end{bmatrix}^T, \boldsymbol{i_i} = \begin{bmatrix} i_{ia} & i_{ib} & i_{ic} \end{bmatrix}^T \tag{4}$$

are the source voltage and current (3), and the rectifier input voltage and current (4).

The DC link voltage can be obtained as:

$$v_{DC} = \boldsymbol{S_r}^T \cdot \boldsymbol{v_i} \tag{5}$$

with the rectifier switching matrix:

$$\boldsymbol{S_r} = \begin{bmatrix} S_{ap} - S_{an} \\ S_{bp} - S_{bn} \\ S_{cp} - S_{cn} \end{bmatrix} \tag{6}$$

where S_{xp}, $S_{xn} \in \{0, 1\}$ with $x = a, b, c$. The output pole voltage of Inverter 1 (v_{o1}) and Inverter 2 (v_{o2}), with respect to the negative DC link rail, are defined in (7).

$$\boldsymbol{v_{o1}} = \boldsymbol{S_{i1}} \cdot v_{DC}, \boldsymbol{v_{o2}} = \boldsymbol{S_{i2}} \cdot v_{DC} \tag{7}$$

where the switching matrices of Inverter 1 ($\boldsymbol{S}_{i1}$) and Inverter 2 ($\boldsymbol{S}_{i2}$) are:

$$\boldsymbol{S}_{i1}=\begin{bmatrix}S_{A1}\\S_{B1}\\S_{C1}\end{bmatrix}=\begin{bmatrix}S_{Ap1}-S_{An1}\\S_{Bp1}-S_{Bn1}\\S_{Cp1}-S_{Cn1}\end{bmatrix},\boldsymbol{S}_{i2}=\begin{bmatrix}S_{A2}\\S_{B2}\\S_{C2}\end{bmatrix}=\begin{bmatrix}S_{Ap2}-S_{An2}\\S_{Bp2}-S_{Bn2}\\S_{Cp2}-S_{Cn2}\end{bmatrix} \tag{8}$$

and $S_{xpk}=\bar{S}_{xnk}\in\{0,\ 1\}$ with $x=a,\ b,\ c\ ,\ \ k=1,\ 2$. The output phase voltage corresponds to the difference of both inverters pole voltages:

$$\boldsymbol{v}_{\boldsymbol{ph,o}}=\begin{bmatrix}v_{ph,oa} & v_{ph,ob} & v_{ph,oc}\end{bmatrix}^{T}=\boldsymbol{v}_{\boldsymbol{o}1}-\boldsymbol{v}_{\boldsymbol{o}2}=\left(\boldsymbol{S}_{i1}-\boldsymbol{S}_{i2}\right)v_{DC} \tag{9}$$

Considering a model of the AC machine with R_s the stator resistance, the output phase voltage can be written as:

$$\boldsymbol{v}_{\boldsymbol{ph,o}}=R_s\boldsymbol{i}_{\boldsymbol{o}}+\frac{d\boldsymbol{\Psi}_s\left(\boldsymbol{i}_{\boldsymbol{o}},\boldsymbol{i}_{\boldsymbol{r}},\theta_r\right)}{dt} \tag{10}$$

where Ψ_s is the stator flux linkage vector given by:

$$\boldsymbol{\Psi}_{\boldsymbol{s}}=\begin{bmatrix}\Psi_{sa} & \Psi_{sb} & \Psi_{sc}\end{bmatrix}^{T} \tag{11}$$

The rotor angle is θ_r and the output (stator) current vector $\boldsymbol{i}_{\boldsymbol{o}}$ and rotor current vector $\boldsymbol{i}_{\boldsymbol{r}}$ are given by (12):

$$\boldsymbol{i}_{\boldsymbol{o}}=\begin{bmatrix}i_{oa} & i_{ob} & i_{oc}\end{bmatrix}^{T},\boldsymbol{i}_{\boldsymbol{r}}=\begin{bmatrix}i_{ra} & i_{rb} & i_{rc}\end{bmatrix}^{T} \tag{12}$$

As Ψ_s is an implicit function of t, (10) can be rewritten by using the chain rule for the derivative:

$$\boldsymbol{v}_{\boldsymbol{ph,o}}=R_s\boldsymbol{i}_{\boldsymbol{o}}+\frac{\partial\boldsymbol{\Psi}_s}{\partial\boldsymbol{i}_{\boldsymbol{o}}}\frac{d\boldsymbol{i}_{\boldsymbol{o}}}{dt}+\boldsymbol{\psi}_2\left(t\right) \tag{13}$$

where

$$\boldsymbol{\psi}_2\left(t\right)=\frac{\partial\boldsymbol{\Psi}_s}{\partial\boldsymbol{i}_{\boldsymbol{r}}}\frac{d\boldsymbol{i}_{\boldsymbol{r}}}{dt}+\frac{\partial\boldsymbol{\Psi}_s}{\partial\theta_r}\frac{d\theta_r}{dt} \tag{14}$$

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Assuming $\partial\Psi_s/\partial \boldsymbol{i}_o$ is a bijective function of t, it can be defined as:

$$\frac{\partial \boldsymbol{\Psi}_s}{\partial \boldsymbol{i}_o} = \boldsymbol{\psi}_1^{-1}(t) \tag{15}$$

and (13) can be redefined by:

$$\boldsymbol{v}_{ph,o} = R_s \boldsymbol{i}_o + \boldsymbol{\psi}_1^{-1}(t)\frac{d\boldsymbol{i}_o}{dt} + \boldsymbol{\psi}_2(t) \tag{16}$$

The DC link current is:

$$i_{DC} = \left(\boldsymbol{S}_{i1} + \boldsymbol{S}_{i2}\right)^T \boldsymbol{i}_o \tag{17}$$

and the rectifier input current:

$$\boldsymbol{i}_i = \boldsymbol{S}_r i_{DC} \tag{18}$$

Taking into account (1) – (18), the state space model of the drive is given by (19) –(21):

$$\frac{d\boldsymbol{i}_s}{dt} = -\frac{R_f}{L_f}\boldsymbol{i}_s - \frac{1}{L_f}\boldsymbol{v}_i + \frac{1}{L_f}\boldsymbol{v}_s \tag{19}$$

$$\frac{d\boldsymbol{v}_i}{dt} = \frac{1}{C_f}\boldsymbol{i}_s - \frac{1}{C_f}\boldsymbol{S}_r\left(\boldsymbol{S}_{i1} + \boldsymbol{S}_{i2}\right)^T \boldsymbol{i}_o \tag{20}$$

$$\frac{d\boldsymbol{i}_o}{dt} = -\boldsymbol{\psi}_1(t)R_s\boldsymbol{i}_o - \boldsymbol{\psi}_1(t)\boldsymbol{\psi}_2(t) + \boldsymbol{\psi}_1(t)\left(\boldsymbol{S}_{i1} - \boldsymbol{S}_{i2}\right)\boldsymbol{S}_r^T \cdot \boldsymbol{v}_i \tag{21}$$

4. Zero sequence voltage

As mentioned before, the dual-inverter fed open-ended winding induction motor drive may suffer from zero sequence current caused by zero sequence voltage. This zero sequence voltage is produced because of the asymmetry of the instantaneous phase voltages applied to the machine windings (due to the voltage space vectors used). In general, zero sequence currents

may give rise to increased RMS phase current, thus increasing the system losses, high current/voltage THD, and machine over-heating and vibrations. The zero sequence voltage is given by [11]:

$$v_{zs} = \frac{v_{A1A2} + v_{B1B2} + v_{C1C2}}{3} \tag{22}$$

The zero sequence voltage contributions from the 64 space vector combinations are shown in Table 2. As can be noted, there are twenty voltage space vectors that do not produce zero sequence voltage; thus in order to avoid the circulation of zero sequence current in the machine windings, only these space vector combinations could be used in the modulation strategy for the dual inverter [9].

V_{zs}	Voltage vector combinations
$-V_{DC}/2$	V_{87}
$-V_{DC}/3$	V_{84}, V_{86}, V_{82}, V_{57}, V_{37}, V_{17}
$-V_{DC}/6$	V_{85}, V_{83}, V_{54}, V_{34}, V_{81}, V_{56}, V_{52}, V_{36} V_{32}, V_{47}, V_{14}, V_{16}, V_{12}, V_{67}, V_{27}
0	V_{88}, V_{55}, V_{53}, V_{35}, V_{33}, V_{44}, V_{51}, V_{31}, V_{46}, V_{42} V_{15}, V_{13}, V_{64}, V_{24}, V_{11}, V_{66}, V_{62}, V_{26}, V_{22}, V_{77}
$+V_{DC}/6$	V_{58}, V_{38}, V_{45}, V_{43}, V_{18}, V_{65}, V_{25}, V_{63} V_{23}, V_{74}, V_{41}, V_{61}, V_{21}, V_{76}, V_{72}
$+V_{DC}/3$	V_{48}, V_{68}, V_{82}, V_{75}, V_{73}, V_{71}
$+V_{DC}/2$	V_{78}

Table 2. Zero sequence voltage contributions from different space vector combinations

Moreover, from Table 2 and Figure 2, it can be noted that there are two different but equivalent sets of active vectors producing null zero sequence voltage (see Table 3), which could be used along with the zero vectors: V_{11}, V_{22}, V_{33}, V_{44}, V_{55}, V_{66}, V_{77}, and V_{88}.

Set 1	V_{15}	V_{35}	V_{31}	V_{51}	V_{53}	V_{13}
Set 2	V_{24}	V_{26}	V_{46}	V_{42}	V_{62}	V_{64}

Table 3. Active space vectors producing null zero sequence voltage

5. Common-mode voltage

Conventional PWM inverters generate alternating common-mode voltages relative to ground which generate currents through the motor parasitic capacitances to the rotor iron [25]. These

currents find their way via the motor bearings back to the grounded stator case. The so-called bearing currents have been found to be a major cause of premature bearing failure in PWM inverter motor drives [26].

One of the main features of an open-end winding induction machine drive is the possibility of reducing the common-mode voltage by using certain space vector combinations of the dual-inverter topology (Figure 2). In general, for an open-end winding machine, the common-mode voltage is given by [8]:

$$v_{cm} = \frac{1}{6}\left(v_{A1} + v_{B1} + v_{C1} + v_{A2} + v_{B2} + v_{C2}\right) \tag{23}$$

where v_{Ai}, v_{Bi}, v_{Ci}, with $i=1, 2$, are the pole voltages of each inverter with respect to a common point of the drive (usually ground).

For the topology depicted in Figure 6, the common-mode voltage is given by:

$$v_{cm} = \frac{1}{6}\left(v_{A1G} + v_{B1G} + v_{C1G} + v_{A2G} + v_{B2G} + v_{C2G}\right) \tag{24}$$

where the common point G is the grounded neutral point of the source. These voltages can also be expressed as:

$$\begin{aligned} v_{AiG} &= S_{Api}v_{pG} + S_{Ani}v_{nG} \\ v_{BiG} &= S_{Bpi}v_{pG} + S_{Bni}v_{nG} \\ v_{CiG} &= S_{Cpi}v_{pG} + S_{Cni}v_{nG} \end{aligned} \tag{25}$$

where v_{pG} and v_{nG} are the voltages of the positive and negative rail of the DC link with respect to the grounded neutral point of the source, respectively; S_{xpi}, $S_{xni} \in \{0, 1\}$ with $x = A, B, C$, $i = 1, 2$ are the switching functions of the inverter devices (0: switch opened, 1: switch closed) and $S_{xni} = 1 - S_{xpi}$ (because of the complementary operation of the upper and lower switches of each inverter leg). Therefore,

$$\begin{aligned} v_{cm} = \frac{1}{6}\Big[&\left(S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}\right)v_{pG} \\ &+\left(S_{An1} + S_{Bn1} + S_{Cn1} + S_{An2} + S_{Bn2} + S_{Cn2}\right)v_{nG}\Big] \end{aligned} \tag{26}$$

Let $N_{sw} = S_{Ap1} + S_{Bp1} + S_{Cp1} + S_{Ap2} + S_{Bp2} + S_{Cp2}$, thus

$$v_{cm} = \frac{1}{6}\left[N_{sw} v_{pG} + \left(6 - N_{sw}\right) v_{nG} \right] \tag{27}$$

where N_{sw} is the number of upper inverter switches closed. The squared RMS value of the common-mode voltage is:

$$v_{cm_{RMS}}^2 = \frac{1}{36T} \int_0^T \left[N_{sw} v_{pG} + \left(6 - N_{sw}\right) v_{nG} \right]^2 dt \tag{28}$$

where T is the period of v_{pG} (equals the period of v_{nG}). Further expansion yields:

$$36 v_{cm_{RMS}}^2 = N_{sw}^2 \frac{1}{T} \int_0^T v_{pG}^2 dt + 2N_{sw}\left(6 - N_{sw}\right) \frac{1}{T} \int_0^T v_{pG} v_{nG} dt + \left(6 - N_{sw}\right)^2 \frac{1}{T} \int_0^T v_{nG}^2 dt \tag{29}$$

The voltages of the DC link rails are given by:

$$\begin{aligned} v_{pG} &= S_{ap} v_{ra} + S_{bp} v_{rb} + S_{cp} v_{rc} \\ v_{nG} &= S_{an} v_{ra} + S_{bn} v_{rb} + S_{cn} v_{rc} \end{aligned} \tag{30}$$

where v_{ra}, v_{rb}, and v_{rc} are the converter input phase voltages and S_{xp}, S_{xn} with $x = a,\ b,\ c$ are the switching functions of the rectifier. Accordingly, v_{pG} and v_{nG} will always be segments of different input phase voltages and

$$\left| v_{pG}(t) \right| = \left| v_{nG}\left(t - t_o\right) \right|,\ t_o \in \mathbb{R} \tag{31}$$

thus

$$\int_0^T v_{pG}^2 dt = \int_0^T v_{nG}^2 dt \tag{32}$$

Differentiating (29) with respect to N_{sw} and equating to zero, it can be found that $v_{cm_{RMS}}^2$ (and implicitly $v_{cm_{RMS}}$) achieves a minimum value at N_{sw}=3, which means that in order to reduce the RMS common-mode voltage at the machine terminals, only three upper inverter switches should be closed at each switching period.

This can be further investigated by considering a virtual midpoint of the DC link as a reference point (see point 0 in Figure 6). Then, (24) can be rewritten as:

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$$v_{cm} = \frac{1}{6}\left(v_{A10} + v_{B10} + v_{C10} + v_{A20} + v_{B20} + v_{C20}\right) + v_{0G} = v_{cm0} + v_{0G} \tag{33}$$

where the contributions of the input and output stages to the overall common-mode voltage have been separated (v_{0G} and v_{cm0}, respectively). The voltage v_{0G} is the voltage between the reference point 0 and the grounded neutral point of the source. This voltage can be calculated as:

$$v_{0G} = \frac{1}{2}\left[\left(S_{ap} + S_{an}\right)v_{ra} + \left(S_{bp} + S_{bn}\right)v_{rb} + \left(S_{cp} + S_{cn}\right)v_{rc}\right] \tag{34}$$

It can be seen in (34) that v_{0G} depends on the modulation of the input stage, which is totally defined by the duty cycles of the rectifier stage. On the other hand, the voltage v_{cm0} can be rewritten as:

$$v_{cm0} = \frac{1}{6}\left[N_{sw}\frac{v_{DC}}{2} + \left(6 - N_{sw}\right)\left(\frac{v_{DC}}{2}\right)\right] = \frac{1}{6}\left[N_{sw}v_{DC} - 3v_{DC}\right] \tag{35}$$

Therefore, it can be seen in (35) that by using N_{sw}=3, the contribution of the output inverters to the common-mode voltage is eliminated [8]. Table 4 shows the voltage space vector combinations of the dual-inverter topology which do not produce common-mode voltage.

As can be noted from Table 4 and Figure 2, there are larger and lower active vectors available which produce zero common-mode voltage. Any of them could be considered in the modulation strategy for the dual-inverter system depending on the machine voltage requirement. However, from Table 2 and Table 4, it can be appreciated that the space vectors which reduce the common-mode voltage are not the same vectors which reduce the zero sequence voltage; thus, if a common-mode voltage is required, a compensation should be done for the zero sequence voltage; in other case, large zero sequence current components will circulate in the machine windings; a type of compensation will be reviewed in the following section.

Space vector combinations $[S_{Ap1}S_{Bp1}S_{Cp1}S_{Ap2}\ S_{Bp2}S_{Cp2}]$	
V_{14}=[1 0 0 0 1 1]	V_{56}=[0 0 1 1 0 1]
V_{25}=[1 1 0 0 0 1]	V_{61}=[1 0 1 1 0 0]
V_{36}=[0 1 0 1 0 1]	V_{43}=[0 1 1 0 1 0]
V_{41}=[0 1 1 1 0 0]	V_{12}=[1 0 0 1 1 0]
V_{52}=[0 0 1 1 1 0]	V_{16}=[1 0 0 1 0 1]
V_{63}=[1 0 1 0 1 0]	V_{65}=[1 0 1 0 0 1]

Space vector combinations $[S_{Ap1}S_{Bp1}S_{Cp1}S_{Ap2}\ S_{Bp2}S_{Cp2}]$	
V_{23}=[1 1 0 0 1 0]	V_{54}=[0 0 1 1 1 0]
V_{34}=[0 1 0 0 1 1]	V_{32}=[0 1 0 1 1 0]
V_{45}=[0 1 1 0 0 1]	V_{21}=[1 1 0 1 0 0]
V_{78}=[1 1 1 0 0 0]	V_{87}=[0 0 0 1 1 1]

Table 4. Space vectors with zero common mode

6. Pulse width modulation strategies

In this section, PWM strategies for an open-end winding induction motor drive based on a two-output IMC are described.

6.1. Modulation strategies for the input stage of the IMC

The modulation for the input (rectifier) stage of the converter aims to obtain a positive DC link voltage in each sampling period and unity displacement factor at the input [27]. Two different space vector modulation (SVM) strategies can be used for the rectifier [28]. One modulation maximizes the DC voltage by commutating between the largest and the second largest positive line input voltage (Figure 7). The other modulation produces a reduced DC voltage commutating between the lowest and the second lowest input line voltage (Figure 8).

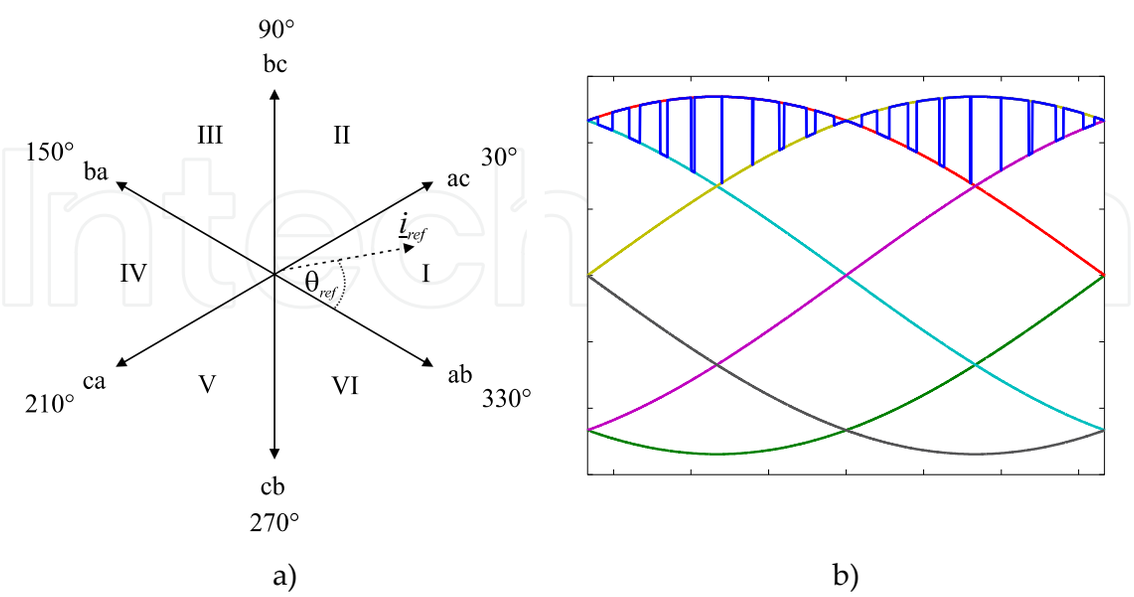

Figure 7. (a) Space vector locations for maximum DC voltage. (b) Maximum DC voltage

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If $\theta_{ref,i}$ is the angle of the voltage reference vector; the $\gamma-\delta$ duty cycles for both modulation strategies are given in (36)–(38). Further details about the modulations for the input stage can be found in [27, 28].

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta},\ d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{36}$$

with

$$d_\gamma = \sin\left(\pi/3 - \theta_{ref,i}\right),\ d_\delta = \sin\left(\theta_{ref,i}\right) \tag{37}$$

the duty cycles for maximum DC voltage and

$$d_\gamma = \cos\left(\theta_{ref,i}\right),\ d_\delta = \cos\left(\pi/3 - \theta_{ref,i}\right) \tag{38}$$

the duty cycles for reduced DC voltage. Figure 9a shows the transition from reduced DC voltage to maximum DC voltage and Figure 9b shows the opposite situation.

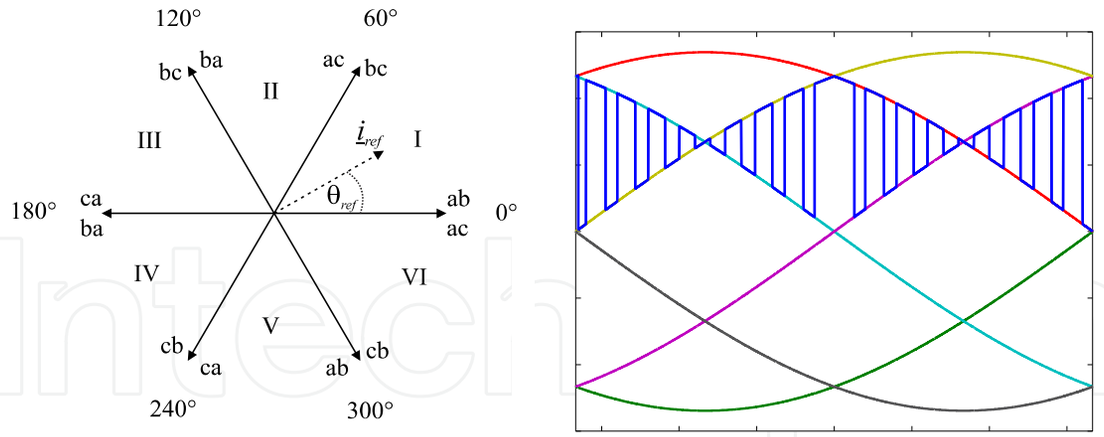

Figure 8. (a) Space vector locations for reduced DC voltage. (b) Reduced DC voltage.

The rectifier SVM for reduced DC link voltage decreases the voltage gain by $\sqrt{3}$. Thus, the transition between reduced and maximum DC link voltage should take place when the output voltage reference is higher than $\frac{1.5}{\sqrt{3}} \cdot V_{ph,input} = 0.866 \cdot V_{ph,input}$.

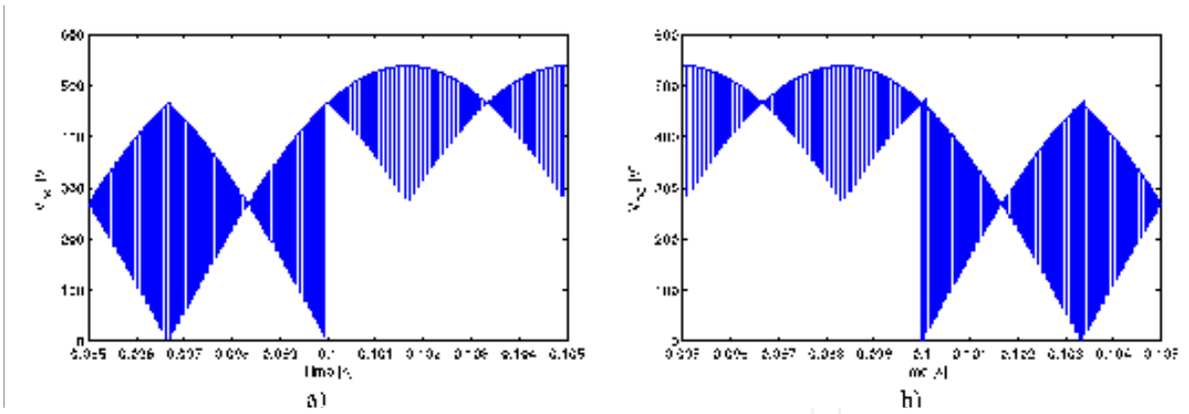

Figure 9. Transition between both rectifier modulation strategies.

6.2. Modulation strategies for the output stages of the IMC

6.2.1. Carrier-based modulation strategy

In a PWM strategy based on a triangular carrier (SPWM), the duty cycles for each leg of inverter 1 are [29]:

$$d_a = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k\right)+1\right) \tag{39}$$

$$d_b = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k-\frac{2\pi}{3}\right)+1\right) \tag{40}$$

$$d_c = \frac{1}{2}\left(m(t)\cos\left(\frac{2\pi}{m_f}k+\frac{2\pi}{3}\right)+1\right) \tag{41}$$

In this case, It is necessary a variable modulation index given by $m(t)=m_o(d_\gamma + d_\delta)$ to compensate the fluctuations of the DC link voltage, m_o is the final modulation index ($0\le m_o\le 1$), $m_f = f_s / f_o$ is the frequency index (f_o: output frequency, f_s: switching frequency) and $0\le k\le m_f$. Duty cycles of inverter 2 are obtained using (39)–(41), but considering a phase shift of 180° for the cosine functions. For implementation purposes, the duty cycles d_a, d_b, and d_c are transformed into equivalent $\alpha-\beta-0$ duty cycles. Thus, considering Figure 10, the $\alpha-\beta-0$ duty cycles are:

$$d_0 = 1 - d_{max} \tag{42}$$

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$$d_\alpha = d_{max} - d_{mid} \tag{43}$$

$$d_\beta = d_{mid} - d_{min} \tag{44}$$

$$d_7 = d_{min} \tag{45}$$

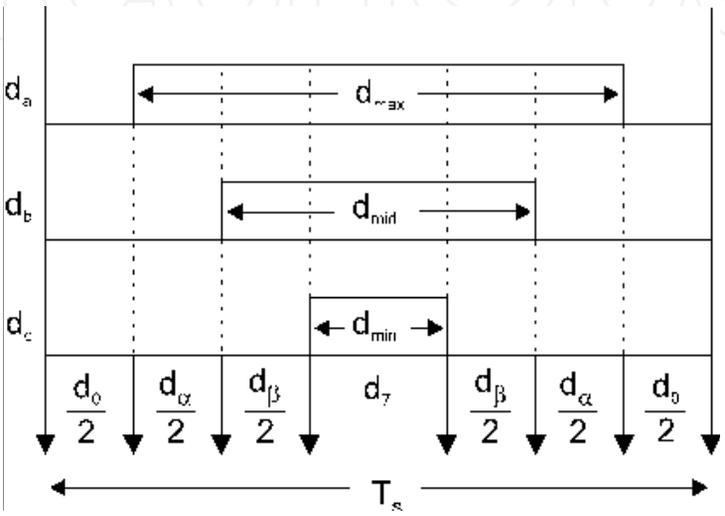

Figure 10. A single inverter stage duty cycles.

To obtain a correct balance of the input currents and the output voltages in a switching period, the modulation pattern should produce all combinations of the rectification and the inversion switching states [27], resulting in the following duty cycles for the active vectors:

$$d_{\alpha\gamma} = d_\alpha d_\gamma^R, d_{\beta\gamma} = d_\beta d_\gamma^R, d_{\alpha\delta} = d_\alpha d_\delta^R, \; d_{\beta\delta} = d_\beta d_\delta^R \tag{46}$$

The duty cycle corresponding to the switching state $[S_{Ap}S_{Bp}S_{Cp}]$=[0 0 0] is:

$$d_{00} = d_{0,tot} - d_{min} \tag{47}$$

and the combined zero vectors duty cycles are:

$$d_{0\gamma} = d_{00} d_\gamma^R, d_{0\delta} = d_{00} d_\delta^R \tag{48}$$

The output stages duty cycles are different for each inverter and are represented in Figure 11 [23] for inverter i (i=1, 2).

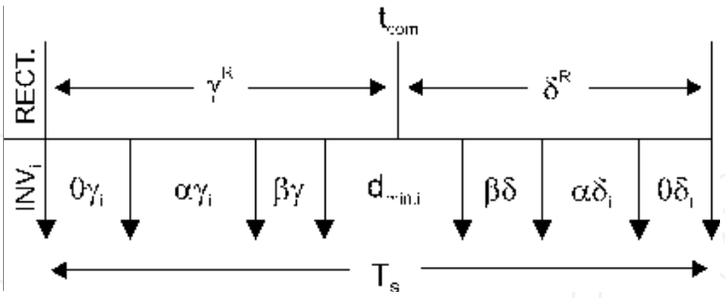

Figure 11. Inverters duty cycles.

6.2.2. Space vector modulation strategy for zero sequence reduction

As mentioned in Section 4, in an open-end winding induction machine drive, the zero sequence voltage can be reduced by using the active space vectors given in Table 3. The zero vectors are mapped depending on the sector information [9]. The mapping is shown in Table 5.

Sector	I	II	III	IV	V	VI
Set 1 zero vectors	V_{55}	V_{33}	V_{11}	V_{55}	V_{33}	V_{11}
Set 2 zero vectors	V_{22}	V_{66}	V_{44}	V_{22}	V_{66}	V_{44}

Table 5. Mapping of zero vectors

The duty cycles for the output stages are calculated as:

$$d_\alpha = m(t)\sin\left(\pi/3 - \theta_{ref,o}\right), d_\beta = m(t)\sin\left(\theta_{ref,o}\right) and\, d_0 = 1 - d_\alpha - d_\beta \tag{49}$$

where $m(t)=m_o(d_\gamma + d_\delta)$ and $0 \le m_o \le 1$. $\theta_{ref,o}$ is the angle of the output reference voltage space vector. As in the carrier-based modulation strategy, the duty cycles of the rectifier and the inverters should be combined; thus the active vector duty cycles are given in (46).

The combined zero vectors duty cycles are:

$$d_{0\gamma} = d_0 d_\gamma^R, d_{0\delta} = d_0 d_\delta^R \tag{50}$$

Thus, the switching sequence, which is the same for both output stages, is shown in Figure 12, commutating the input stage with zero DC current [27].

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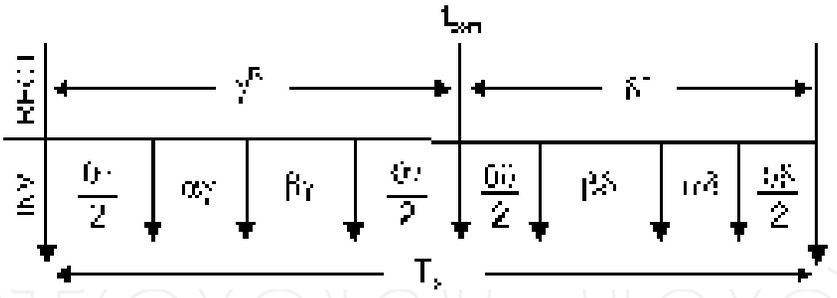

Figure 12. Standard switching sequence for IMCs.

6.2.3. Space vector modulation strategy for common-mode voltage reduction

If only the voltage space vectors shown in Table 4 are used in the modulation strategy for the output stages of the IMC, the contribution of the dual-inverter to the overall common-mode voltage can be eliminated. The duty cycles for the IMC outputs are calculated as in (49) – (50). However, as mentioned in Section 5, the space vectors producing null v_{cm0} are not the same vectors producing null zero sequence voltage. Hence, as in this SVM strategy, the vectors used to modulate the converter output stages will eliminate the common-mode voltage; a compensation must be performed to avoid the circulation of zero sequence current in the machine.

The average zero sequence voltage within a sampling interval can be eliminated by forcing the zero sequence volt-seconds to zero [11] by applying the null voltage vectors with unequal times. Accordingly, the standard switching sequence used in the IMC [27] is modified in order to reduce/eliminate the average zero sequence voltage within a sampling period. For the modulation strategy presented, the duty cycles for both output VSIs are the same, which can be noted in Figure 13.

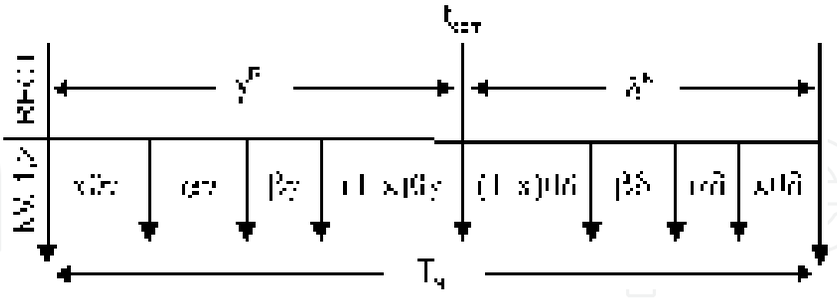

Figure 13. Modified switching sequence for the IMC with two outputs.

Taking into account that the same space vectors sequence applied in γ^R interval is applied in the δ^R interval but in reverse order, then the value of x, which causes the cancellation of the zero sequence volt-seconds, is calculated at every sampling period to satisfy [11]:

$$v_{zs1}x\left(0\gamma+0\delta\right)+v_{zs2}\left(\alpha\gamma+\alpha\delta\right)+v_{zs3}\left(\beta\gamma+\beta\delta\right)+v_{zs4}\left(1-x\right)\left(0\gamma+0\delta\right)=0 \tag{51}$$

where v_{zsk} with $k=1,\ \ 2,\ \ 3,\ \ 4$, is the zero sequence voltage value at intervals $x0\gamma$, $\alpha\gamma$, $\beta\gamma$, and $(1-x)0\gamma$, respectively. The value of v_{zsk} can be calculated by using (22) and considering the space vectors used in the modulation strategy.

7. Open-end winding induction machine drive

In this section, the application of a two-output IMC supplying an open-end winding induction machine will be presented. The performance of the drive by using some of the modulation strategies discussed above will be shown and analyzed via simulation and experimental results. The simulations are carried out in a PSIM/MATLAB simulation platform. On the other hand, experimental results are obtained using the setup shown in Figure 14. The IMC has been designed and built at the Power Electronics, Machines and Control lab facilities, University of Nottingham, UK. A six-pole induction machine rated at 7.5 kW is used. A DSP board, based on the TMS320C6713 processor, is used as the control platform. The calculation of duty cycles is carried out on the DSP among several other tasks. An FPGA interface board, designed at Nottingham University, is used to implement the modulation strategies and data acquisition. Communication between the DSP and a PC is achieved using a DSK6713HPI (Host Port Interface) daughter card. The converter input stage uses SK60GM123 modules and the output stages use SK35GD126 modules. The switching frequency is 10 kHz and voltages and currents are also sampled at 10 kHz. The load used in the experimental system is a DC generator, supplying a resistive load, coupled with the induction motor shaft.

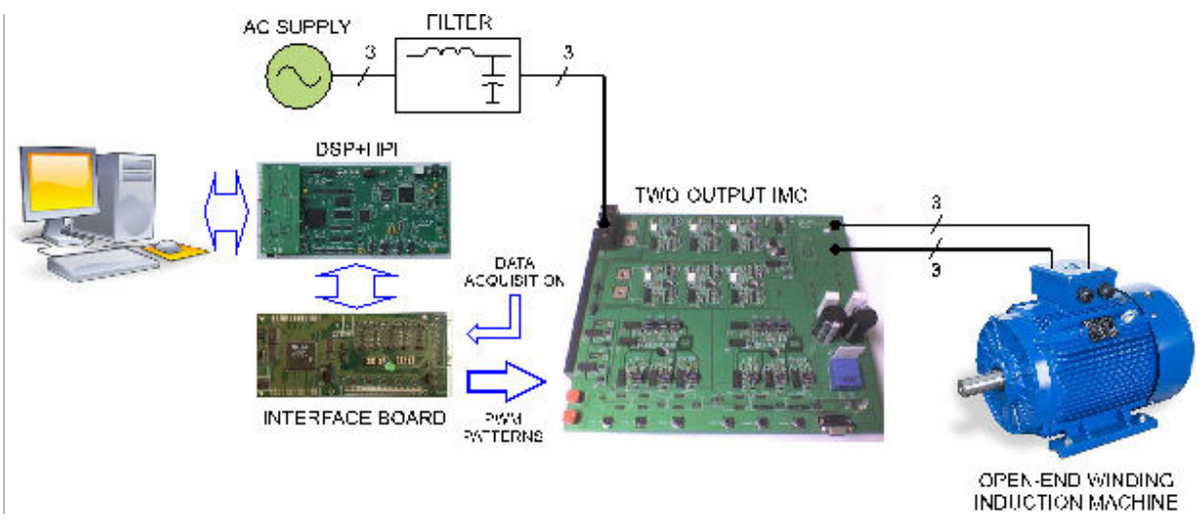

Figure 14. Experimental setup.

7.1. SVM strategy for zero sequence voltage reduction and changing DC voltage

The modulation strategies, presented in Section 6.1 and 6.2.2, are used to implement a standard feedforward vector control scheme [30] for the machine currents (Figure 15). Simulation and experimental results are shown in Sections 7.1.1 and 7.1.2, respectively.

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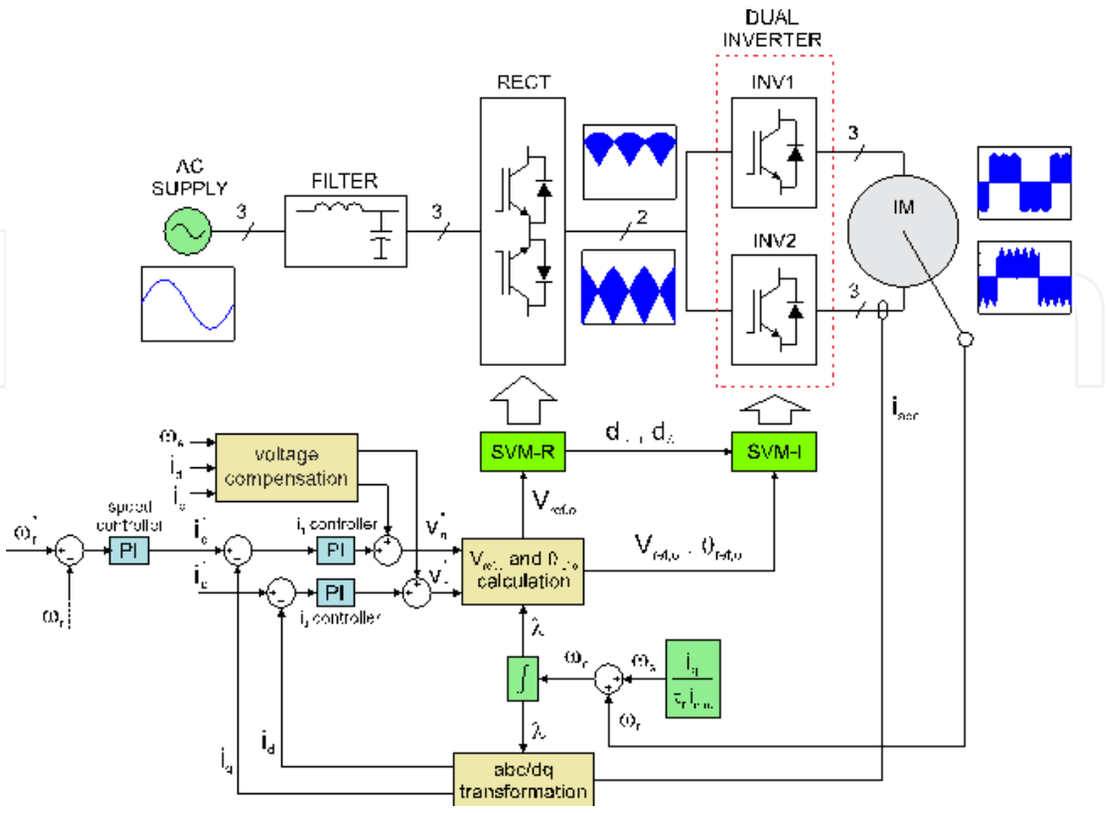

Figure 15. Feedforward vector control scheme of induction machine.

7.1.1. Simulation results

The performance of the vector control scheme is verified by applying step changes in the *dq*-axis reference currents. Figure 16 shows the waveforms obtained by applying a step change in the *q*-axis reference current from 7.7 to 10 A at $t = 0.16$ *s*, while *d*-axis current is kept constant at 6 A. Figure 16a shows *dq* reference currents and their corresponding responses. A good tracking of the reference currents is obtained. The motor currents and phase *a* voltage are shown in Figure 16b. The step change in *q*-axis current is followed with changes in the magnitude and phase of the instantaneous machine currents. Moreover, a transition between reduced virtual DC voltage to maximum virtual DC voltage can be noticed in the output phase voltage of Figure 16b (bottom).

Figure 17a shows the performance of the control scheme when a step change from 6 to 8 A is applied in *d*-axis reference current while *q*-axis current is kept constant at 7.7 A. The motor currents and phase- *a* voltage are shown in Figure 17b. Again, the transition between both modulation strategies for the input rectifier can be noticed.

Figure 18 (top) shows the converter input phase voltage and current; the unity input displacement factor can be noted. Figure 18 (bottom) shows the output zero sequence voltage that has been obtained from the voltage across the load in each phase and then applying (22). As can be seen, the zero sequence voltage has been eliminated due to the modulation strategy used for the output stages.

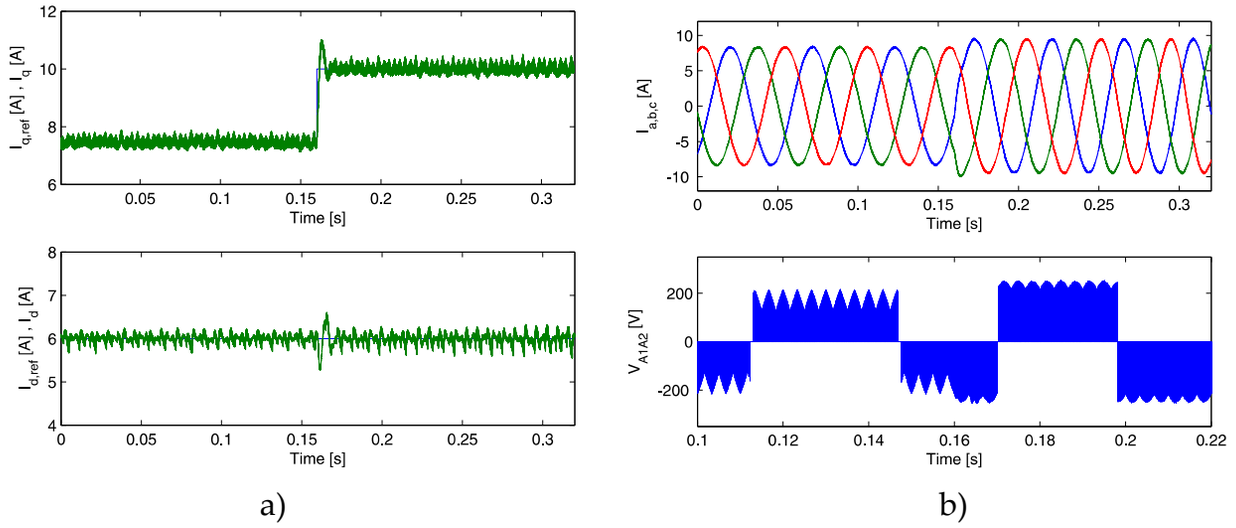

Figure 16. *q*-axis current step change. (a) Motor *q*-axis current (top) and *d*-axis current (bottom). (b) Motor currents (top) and phase voltage (bottom).

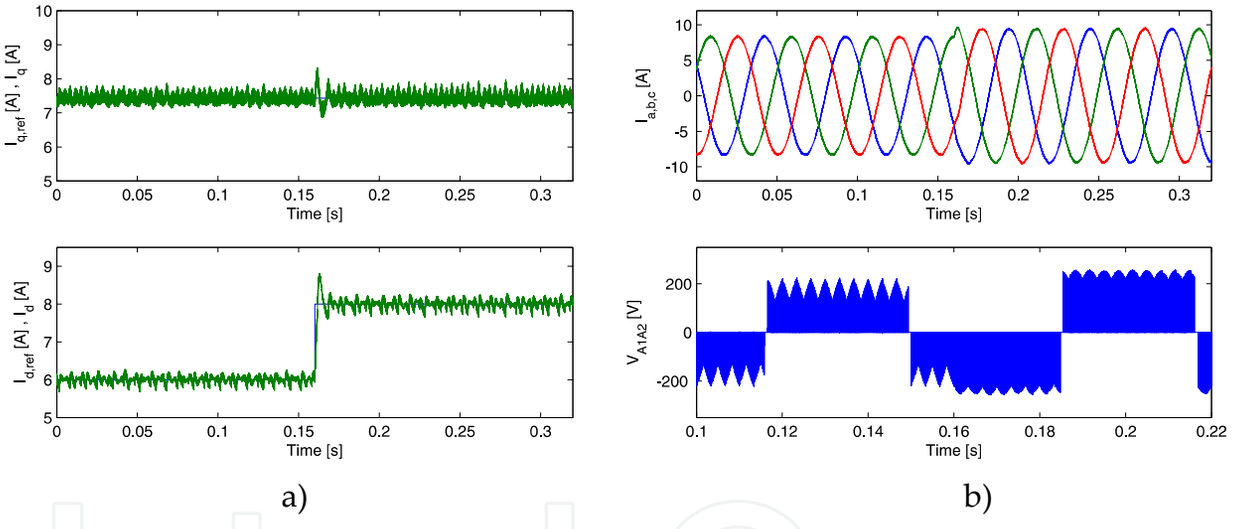

Figure 17. *d*-axis current step change. (a) Motor *q*-axis current (top) and *d*-axis current (bottom). (b) Motor currents (top) and phase voltage (bottom).

7.1.2. Experimental results

The *dq*-axis currents are shown in Figure 19a. As the speed controller saturates when a step change in the speed reference takes place, a step change in *q*-axis current reference is applied. The *d*-axis current reference is kept constant at 6 A. A good performance of the control scheme can be appreciated agreeing with the simulated results. The instantaneous motor currents and phase *a* voltage are shown in Figure 19b. Again, the transition between both rectifier modulation strategies can be noted in the output phase voltage (Figure 19b bottom) when the change in *q*-axis reference current is applied.

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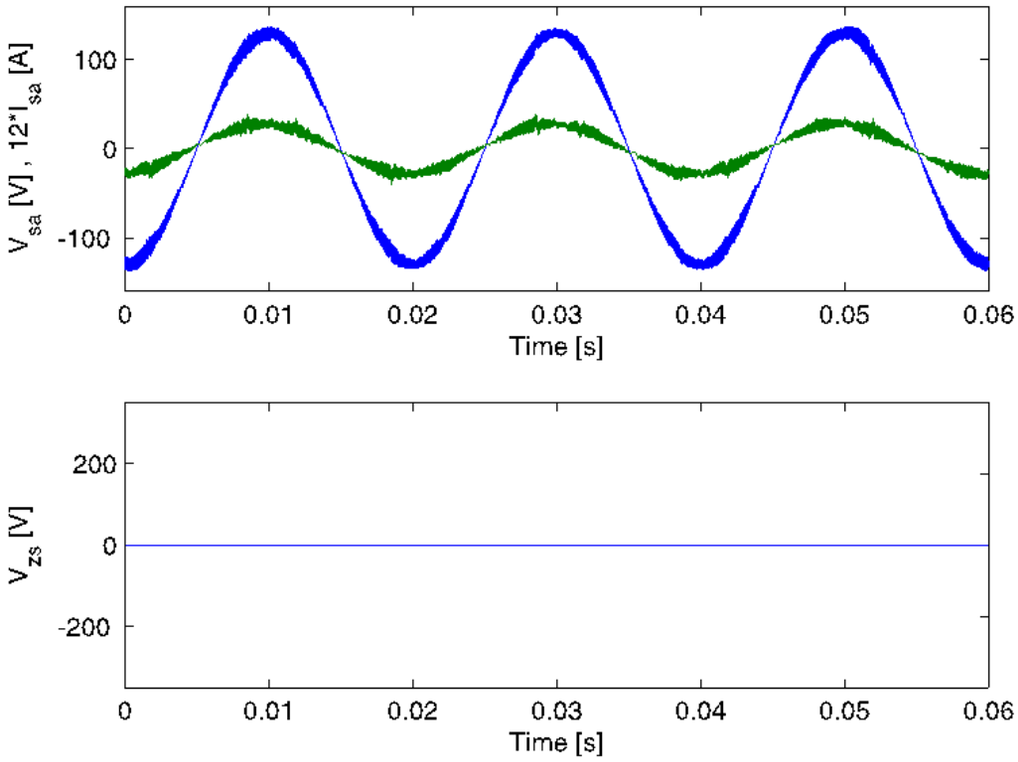

Figure 18. Input phase voltage and current (top) and zero sequence voltage (bottom).

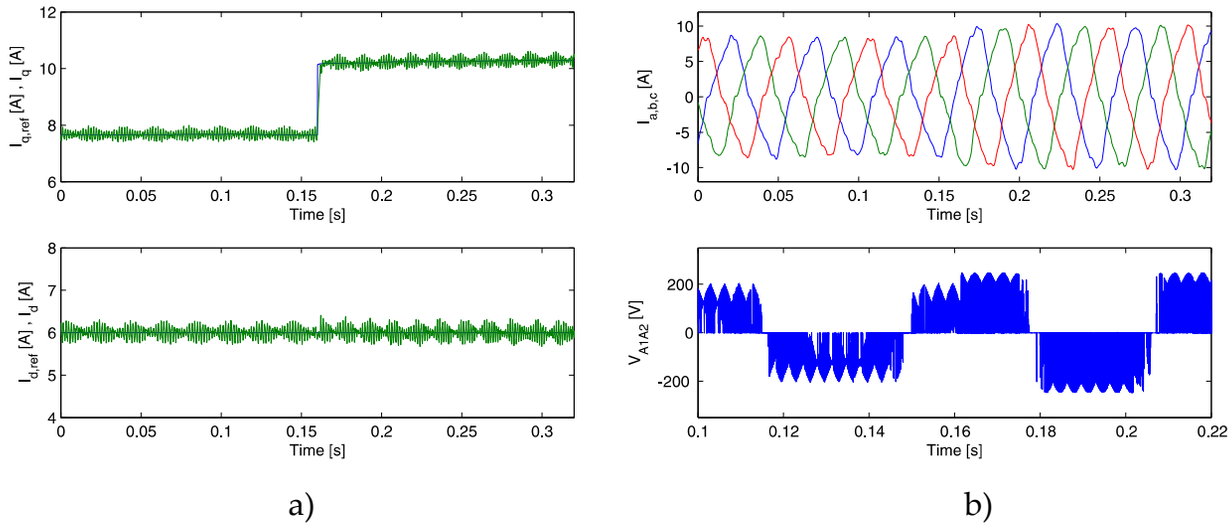

Figure 19. *q*-axis current step change. (a) Motor *q*-axis current (top) and *d*-axis current (bottom). (b) Motor currents (top) and phase voltage (bottom).

Figure 20a shows the *dq* machine currents when a step change in *d*-axis reference current is applied while *q*-axis current is kept constant at 7.7 A. The motor currents and phase- *a* voltage are shown in Figure 20b. A good correspondence with the simulation results can be noted.

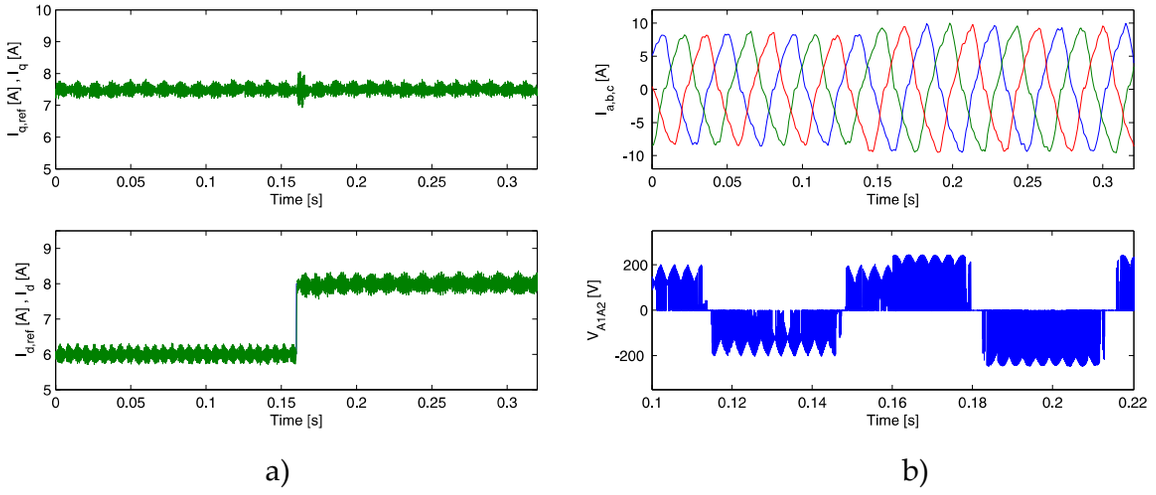

Figure 20. *q*-axis current step change. (a) Motor *q*-axis current (top) and *d*-axis current (bottom). (b) Motor currents (top) and phase voltage (bottom).

Finally, Figure 21 (top) shows the input phase voltage and current. The zero sequence voltage shown in Figure 21 (bottom) is not exactly zero, but this is probably due to the measurement procedure because not all of the channels are sampled at the same time and because in Figure 18 the input switches are ideal.

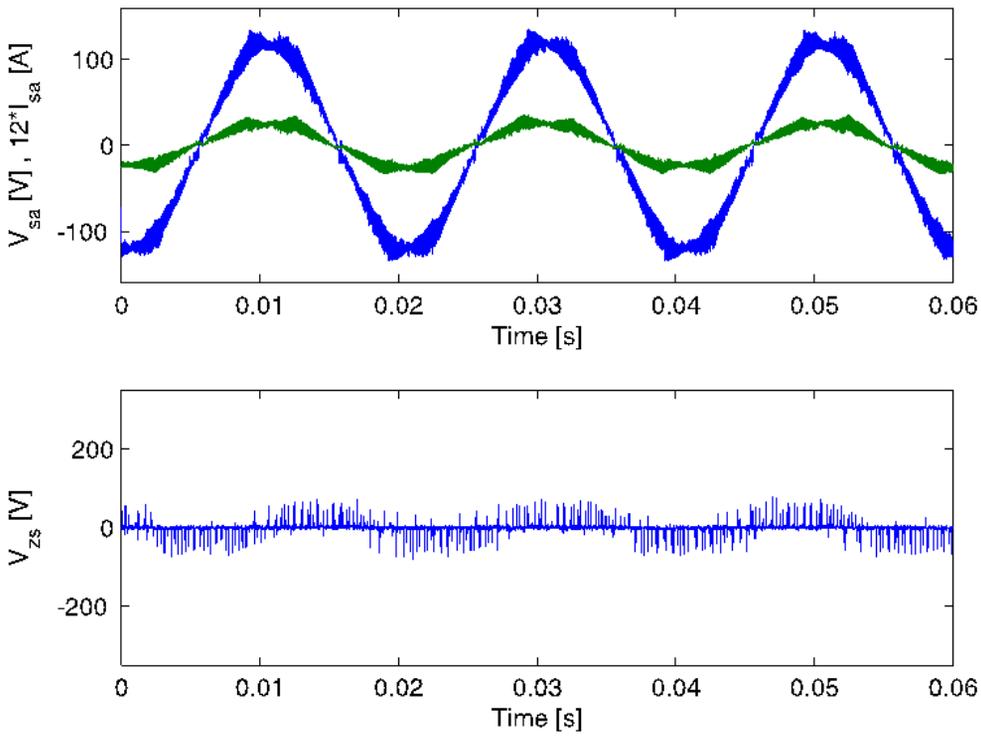

Figure 21. Input rectifier voltage and current (top) and zero sequence voltage (bottom).

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7.2. SVM strategy for common-mode voltage reduction and zero sequence voltage compensation

Simulation and experimental results for the modulation strategy presented in Section 6.2.2 will be shown in this section. The rectifier is modulated to maximize the DC link voltage (Figure 7) and the full drive is tested in open-loop *v/f* operation.

7.2.1. Simulation results

The DC link voltage and phase- *a* machine voltage are shown in Figure 22a, top and bottom, respectively. The reference output voltage and frequency were set to 150 V and 50 Hz, respectively. The machine currents for 25 Hz operation are shown in Figure 22b (top), while Figure 22b (bottom) shows machine currents for 50 Hz operation.

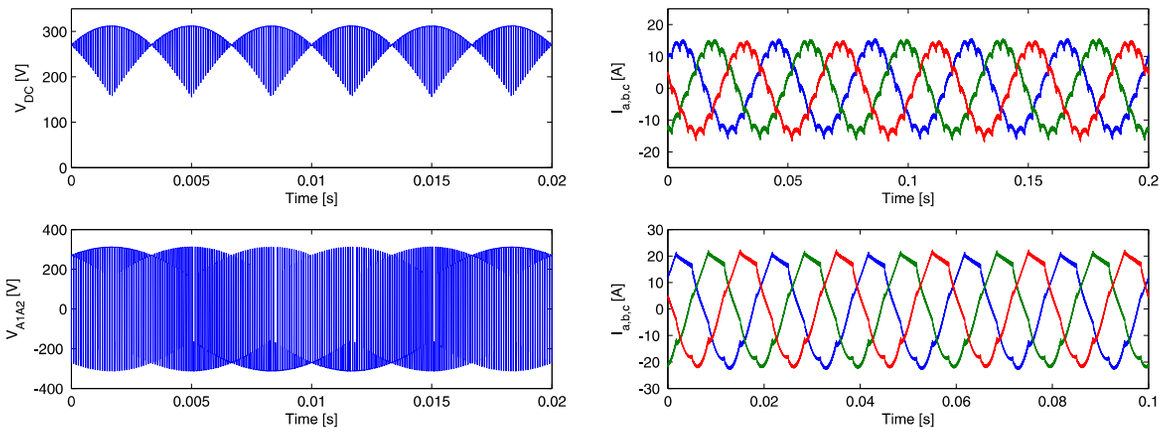

Figure 22. (a) DC link voltage (top) and output phase voltage (bottom). (b) Machine currents for 25 Hz output (top) and 50 Hz output (bottom).

Small disturbances, occurring every 60°, can be noted in the motor currents shown in Figure 22b. These current disturbances are due to the application of zero voltage vectors to machine windings, see PWM pattern in Figure 13, aiming to reduce the zero sequence voltage. During the application of zero voltage vectors, each machine phase winding is supplied with a voltage of $-V_{DC}$ or $+V_{DC}$. When $-V_{DC}$ voltage is applied to the machine windings, the current decreases according to the zero vector duty cycle. Figure 23 shows the current disturbance along with the corresponding DC link voltage and output phase voltage.

The input (supply) currents are shown in Figure 24 (top) while Figure 24 (bottom) shows the converter input phase voltage (blue) and current (green) for an output reference of 150 V and 50 Hz. The unity displacement factor is evident in Figure 24 (bottom).

The low-order harmonics of the machine currents are presented in Table 6.

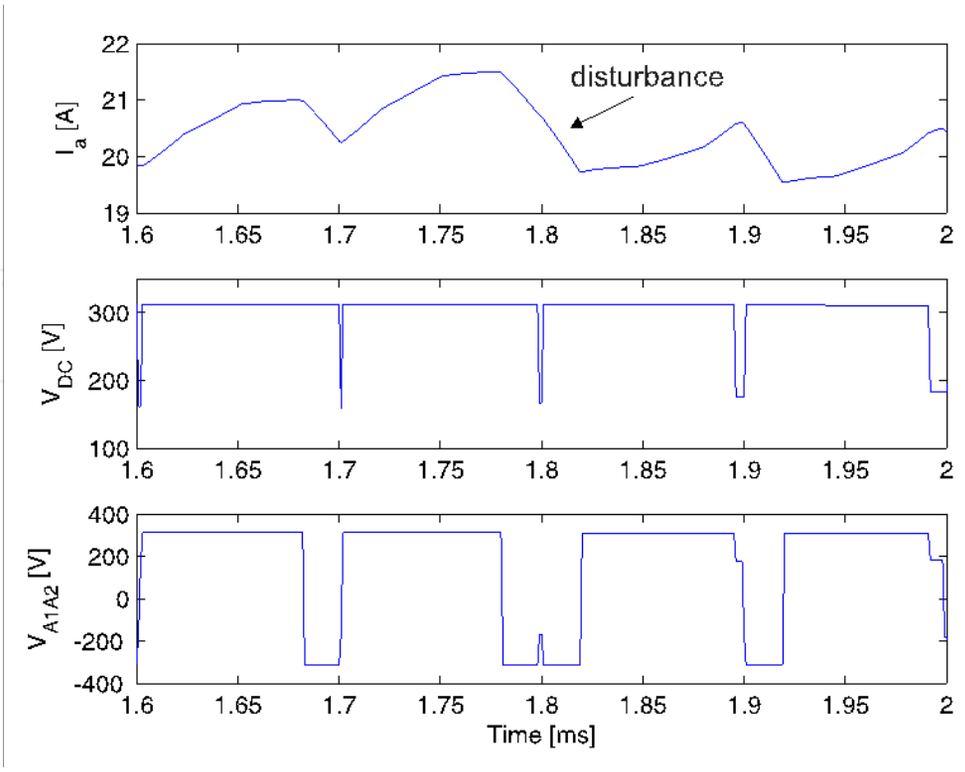

Figure 23. Phase a machine current (top), DC link voltage (middle), and machine phase- *a* voltage (bottom).

Current Harmonic	RMS Value (A)
Fundamental	14.400
2nd	0.250
3rd	0.184
4th	0.112
5th	0.025
6th	0.815

Table 6. Harmonic content of the machine currents

Figure 25a shows the common-mode voltage separated into v_{0G} and v_{cm0} as defined in (33)–(35). Due to absence of the reference point 0 in the real (and also simulated) converter, the common-mode voltages v_{0G} and v_{cm0} shown in Figure 25a top and bottom, respectively, are obtained as:

$$v_{0G} = v_{nG} + \frac{v_{DC}}{2}$$
$$v_{cm0} = \frac{1}{6}\left(v_{A1n} + v_{B1n} + v_{C1n} + v_{A2n} + v_{B2n} + v_{C2n}\right) - \frac{v_{DC}}{2} \quad (52)$$

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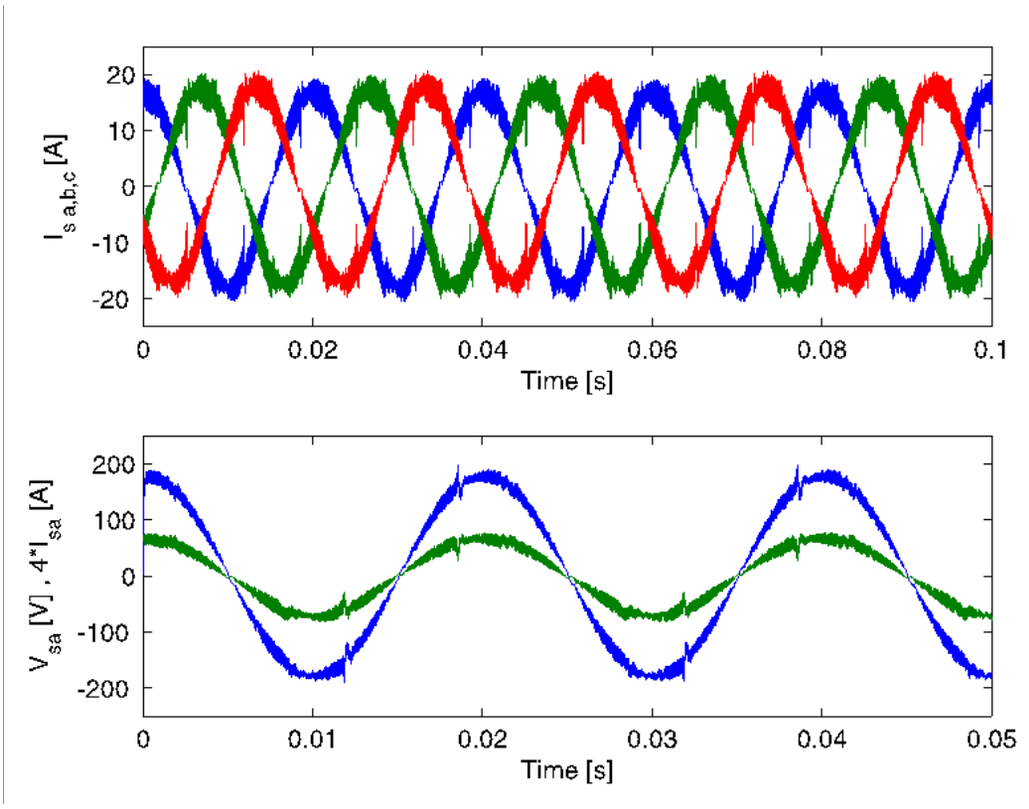

Figure 24. Input currents (top) and input phase voltage and current (bottom).

where n is the negative rail of the DC link.

It can be seen in the simulation results that the contribution of the output inverters to the common-mode voltage is completely eliminated due to the modulation strategy used. Figure 25b shows the zero sequence voltage (top) and its frequency spectrum (bottom). It can be noted that the low-order zero sequence harmonics are reduced because of the asymmetry of the null vector duty cycles used in the switching sequence for each output stage.

7.2.2. Experimental results

Figure 26a (top) shows the DC link voltage while Figure 26a (bottom) shows the voltage across the machine phase- *a* winding. The output phase voltage presents a fundamental component of 141 V, 50 Hz, slightly less than the voltage reference (150 V) because of the device voltage drops. As can be seen, the modulation strategy used results in a bipolar pulse width modulated voltage at the converter output. The machine currents for 25 Hz and 50 Hz operation are shown in Figure 26b (top and bottom), respectively. The reference output voltages are set to 75 and 150 V, respectively. Correspondence between the simulation and the experimental result can be observed.

In Figure 26b, the effect of the zero voltage vectors in the PWM pattern shown in Figure 13 is also observed. The supply currents are shown in Figure 27 (top), again with good correspondence with the simulation study. Figure 27 (bottom) shows the input phase voltage and current.

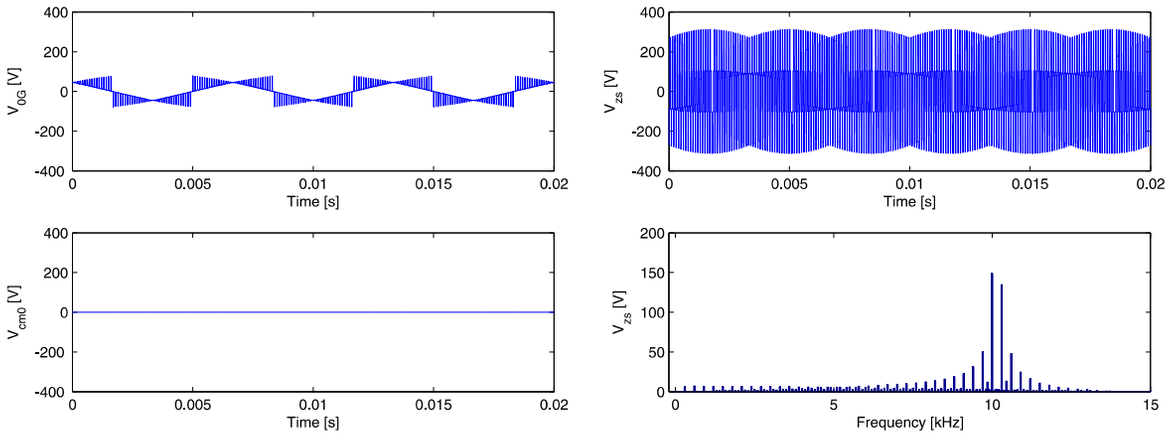

Figure 25. (a) Common-mode voltages v_{0G} (top) and v_{cm0} (bottom). (b) Zero sequence voltage (top) and its frequency spectrum (bottom).

Figure 28a shows the common-mode voltages v_{0G} (top) and v_{cm0} (bottom). The voltage v_{0G} follows very closely the simulation results shown in Figure 25. The voltage v_{cm0} is not exactly zero, but this is probably due to the measurement procedure because not all of the channels are sampled at the same time and because in Figure 25 the input switches are ideal. Finally, Figure 28b shows the zero sequence voltage (top) and its frequency spectrum (bottom), agreeing closely with the simulation results.

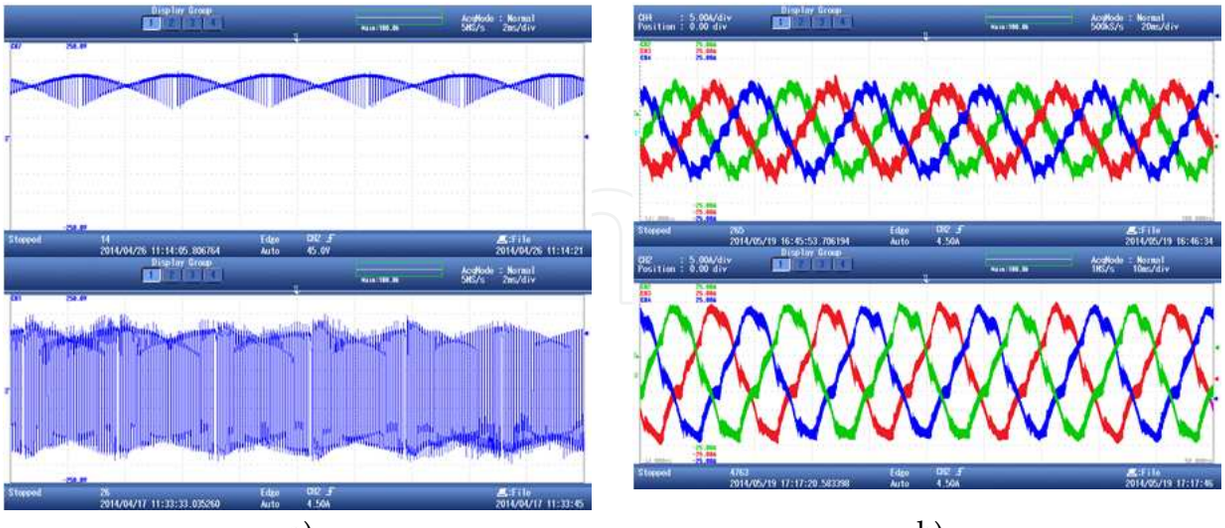

Figure 26. (a) DC link voltage (top) and output phase voltage (bottom). (b) Machine currents for 25 Hz output (top) and 50 Hz output (bottom).

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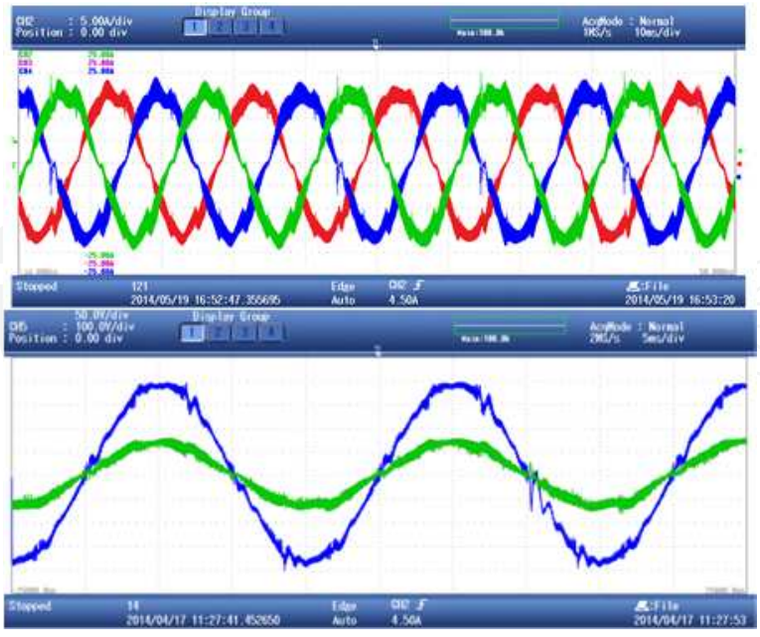

Figure 27. Input currents (top) and input phase voltage and current (bottom).

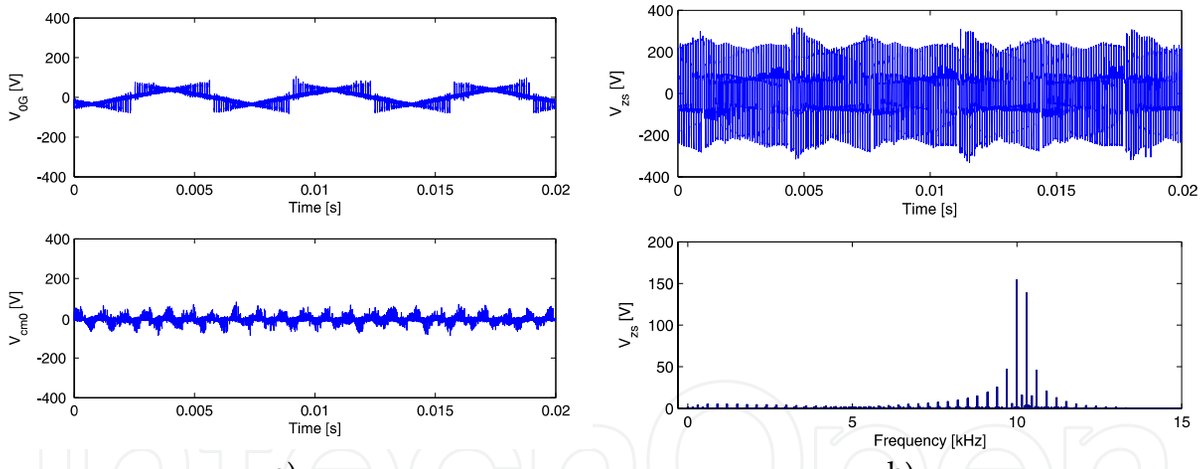

Figure 28. a) Common-mode voltages v_{0G} (top) and v_{cm0}. (bottom). (b) Zero sequence voltage (top) and its frequency spectrum (bottom).

8. Conclusion

The open-end winding induction machine has been presented in this chapter. Different power converter topologies for this type of machine connection have been shown and briefly discussed. Because of the advantages of indirect matrix converter, emphasis has been done in

the application of this converter to control the machine. Therefore, an indirect matrix converter with two outputs stages has been proposed to supply energy to the open-end winding induction motor. This topology has been thoroughly modeled and pulse width modulation strategies for the input and output stages of the proposed topology have been shown. Issues such as zero sequence voltage and common-mode voltage, presented in the dual-inverter configuration, have been analyzed and strategies to eliminate and/or reduce such effects have been presented. The control and modulation strategies have been simulated and experimentally tested in a prototype rig. Results for open and closed-loop operation of the open-end winding topology based on IMC have been shown.

Acknowledgements

This work was funded by Fondecyt Chile under Grant 1151325. The financial support of CONICYT/FONDAP/15110019 is also acknowledged.

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